Data Sheet May 6, 2005 FN7348.2

500MHz Rail-to-Rail Amplifier

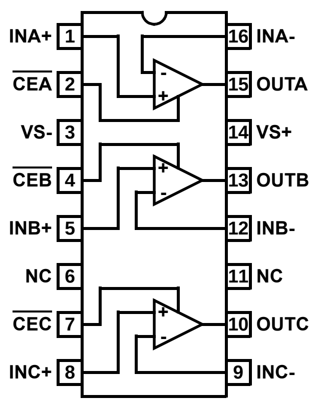
The EL8302 represents a triple rail-to-rail amplifier with a -3dB bandwidth of 500MHz and slew rate of 600V/µs. Running off a very low supply current of 5.6mA per channel, the EL8302 also features inputs that go to 0.15V below the V_S- rail.

The EL8302 includes a fast-acting disable/power-down circuit. With a 25ns disable and a 200ns enable, the EL8302 is ideal for multiplexing applications.

The EL8302 is designed for a number of general purpose video, communication, instrumentation, and industrial applications. The EL8302 is available in an 16-pin SO and 16-pin QSOP packages and is specified for operation over the -40°C to +85°C temperature range.

Pinout

EL8302
(16-PIN SO, QSOP)
TOP VIEW



Features

- 500MHz -3dB bandwidth
- 600V/µs slew rate
- Low supply current = 5.6mA per amplifier
- Supplies from 3V to 5.5V
- Rail-to-rail output
- Input to 0.15V below V_S-
- Fast 25ns disable
- Low cost
- Pb-Free available (RoHS compliant)

Applications

- Video amplifiers
- Portable/hand-held products
- Communications devices

Ordering Information

PART NUMBER	PACKAGE	TAPE & REEL	PKG. DWG. #
EL8302IS	16-Pin SO	-	MDP0027
EL8302IS-T7	16-Pin SO	7”	MDP0027
EL8302IS-T13	16-Pin SO	13”	MDP0027
EL8302ISZ (See Note)	16-Pin SO (Pb-free)	-	MDP0027
EL8302ISZ-T7 (See Note)	16-Pin SO (Pb-free)	7”	MDP0027
EL8302ISZ-T13 (See Note)	16-Pin SO (Pb-free)	13”	MDP0027
EL8302IU	16-Pin QSOP	-	MDP0040
EL8302IU-T7	16-Pin QSOP	7”	MDP0040
EL8302IU-T13	16-Pin QSOP	13”	MDP0040
EL8302IUZ (See Note)	16-Pin QSOP (Pb-free)	-	MDP0040
EL8302IUZ-T7 (See Note)	16-Pin QSOP (Pb-free)	7”	MDP0040
EL8302IUZ-T13 (See Note)	16-Pin QSOP (Pb-free)	13”	MDP0040

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage from V_S+ to V_S- 5.5V
Input Voltage . . . . V_S+ + 0.3V to V_S- -0.3V
Differential Input Voltage 2V
Continuous Output Current 40mA

Power Dissipation . . . . See Curves
Storage Temperature . . . .-65°C to +125°C
Ambient Operating Temperature . . . .-40°C to +85°C
Operating Junction Temperature . . . . +125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S+ = 5V, V_S- = GND, T_A = 25°C, V_{CM} = 2.5V, R_L to 2.5V, A_V = 1, Unless Otherwise Specified

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Offset Voltage		-7	-0.8	+7	mV
TCV_{OS}	Offset Voltage Temperature Coefficient	Measured from T_{MIN} to T_{MAX}		3		µV/°C
IB	Input Bias Current	V_{IN} = 0V	-10	-6		µA
I_{OS}	Input Offset Current	V_{IN} = 0V		0.1	0.6	µA
TCI_{OS}	Input Bias Current Temperature Coefficient	Measured from T_{MIN} to T_{MAX}		2		nA/°C
CMRR	Common Mode Rejection Ratio	V_{CM} = -0.15V to +3.5V	70	95		dB
CMIR	Common Mode Input Range		V_S- -0.15		V_S+ - 1.5	V
R_{IN}	Input Resistance	Common Mode		7		MΩ
C_{IN}	Input Capacitance			0.5		pF
AVOL	Open Loop Gain	V_{OUT} = +1.5V to +3.5V, R_L = 1kΩ to GND	75	100		dB
		V_{OUT} = +1.5V to +3.5V, R_L = 150Ω to GND		80		dB
OUTPUT CHARACTERISTICS						
R_{OUT}	Output Resistance	A_V = +1		30		mΩ
V_{OP}	Positive Output Voltage Swing	R_L = 1kΩ	4.85	4.9		V
		R_L = 150Ω	4.65	4.7		V
V_{ON}	Negative Output Voltage Swing	R_L = 150Ω		150	200	mV
		R_L = 1kΩ		50	70	mV
I_{OUT}	Linear Output Current			65		mA
I_{SC} (source)	Short Circuit Current	R_L = 10Ω	50	80		mA
I_{SC} (sink)	Short Circuit Current	R_L = 10Ω	90	150		mA
POWER SUPPLY						
PSRR	Power Supply Rejection Ratio	V_S+ = 4.5V to 5.5V	70	95		dB
I_{S-ON}	Supply Current - Enabled per Amplifier			5.6	6.2	mA
I_{S-OFF}	Supply Current - Disabled per Amplifier			40	90	µA
ENABLE						
t_{EN}	Enable Time			200		ns
t_{DS}	Disable Time			25		ns
V_{IH-ENB}	$\overline{\text{ENABLE}}$ Pin Voltage for Power-up			0.8		V
V_{IL-ENB}	$\overline{\text{ENABLE}}$ Pin Voltage for Shut-down			2		V

Electrical Specifications V_S+ = 5V, V_S- = GND, T_A = 25°C, V_{CM} = 2.5V, R_L to 2.5V, A_V = 1, Unless Otherwise Specified

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
$I_{IH\text{-}ENB}$	$\overline{\text{ENABLE}}$ Pin Input Current High			8.6		µA
$I_{IL\text{-}ENB}$	$\overline{\text{ENABLE}}$ Pin Input for Current Low			0.01		µA
AC PERFORMANCE						
BW	-3dB Bandwidth	A_V = +1, R_F = 0Ω, C_L = 1.5pF		500		MHz
		A_V = -1, R_F = 1kΩ, C_L = 1.5pF		140		MHz
		A_V = +2, R_F = 1kΩ, C_L = 1.5pF		165		MHz
		A_V = +10, R_F = 1kΩ, C_L = 1.5pF		18		MHz
BW	±0.1dB Bandwidth	A_V = +1, R_F = 0Ω, C_L = 1.5pF		36		MHz
Peak	Peaking	A_V = +1, R_L = 1kΩ, C_L = 1.5pF		1		dB
GBWP	Gain Bandwidth Product			200		MHz
PM	Phase Margin	R_L = 1kΩ, C_L = 1.5pF		55		°
SR	Slew Rate	A_V = 2, R_L = 100Ω, V_{OUT} = 0.5V to 4.5V	500	600		V/µs
t_R	Rise Time	2.5V_{STEP}, 20% - 80%		4		ns
t_F	Fall Time	2.5V_{STEP}, 20% - 80%		2		ns
OS	Overshoot	200mV step		10		%
t_{PD}	Propagation Delay	200mV step		1		ns
t_S	0.1% Settling Time	200mV step		15		ns
dG	Differential Gain	A_V = +2, R_F = 1kΩ, R_L = 150Ω		0.01		%
dP	Differential Phase	A_V = +2, R_F = 1kΩ, R_L = 150Ω		0.01		°
e_N	Input Noise Voltage	f = 10kHz		12		nV/√Hz
i_N+	Positive Input Noise Current	f = 10kHz		1.7		pA/√Hz
i_N-	Negative Input Noise Current	f = 10kHz		1.3		pA/√Hz
e_S	Channel Separation	f = 100kHz		95		dB

Pin Descriptions

PIN	NAME	FUNCTION
1, 5, 8	INA+, INB+, INC+	Non-inverting input for each channel
2, 4, 7	$\overline{\text{CEA}}$, $\overline{\text{CEB}}$, $\overline{\text{CEC}}$	Enable and disable input for each channel
3	VS-	Negative power supply
6, 11	NC	Not connected
9, 12, 16	INC-, INB-, INA-	Inverting input for each channel
10, 13, 15	OUTC, OUTB, OUTA	Amplifier output for each channel
14	VS+	Positive power supply

Typical Performance Curves

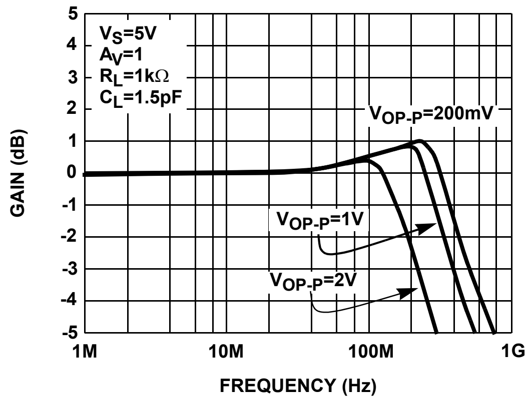


FIGURE 1. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGE LEVELS

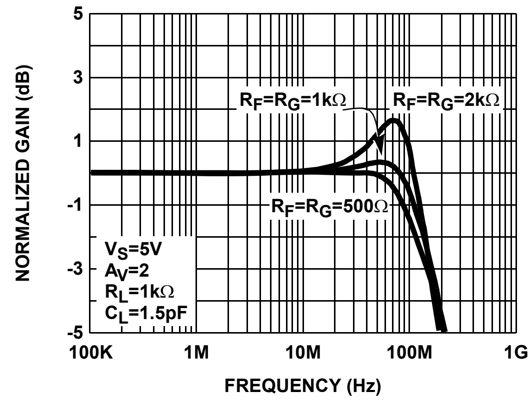


FIGURE 2. SMALL SIGNAL FREQUENCY RESPONSE vs R_F AND R_G

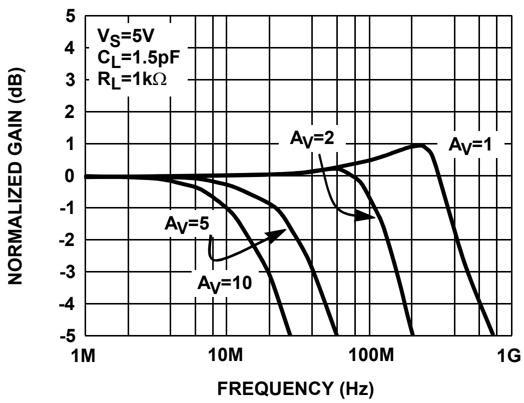


FIGURE 3. SMALL SIGNAL FREQUENCY RESPONSE FOR VARIOUS NON-INVERTING GAINS

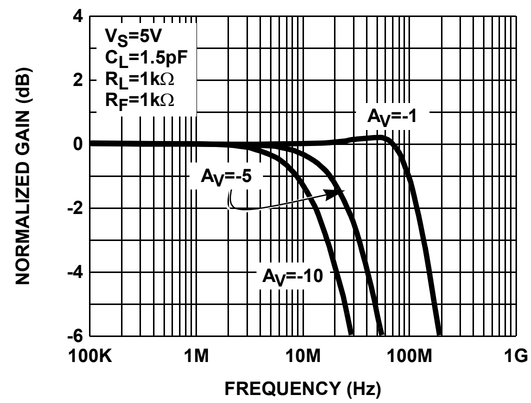


FIGURE 4. SMALL SIGNAL FREQUENCY RESPONSE FOR VARIOUS INVERTING GAINS

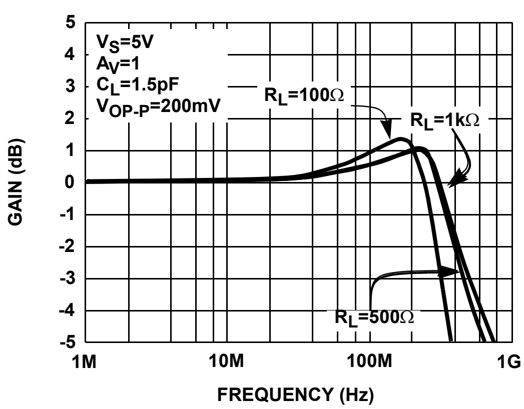


FIGURE 5. SMALL SIGNAL FREQUENCY RESPONSE FOR VARIOUS R_{LOAD}

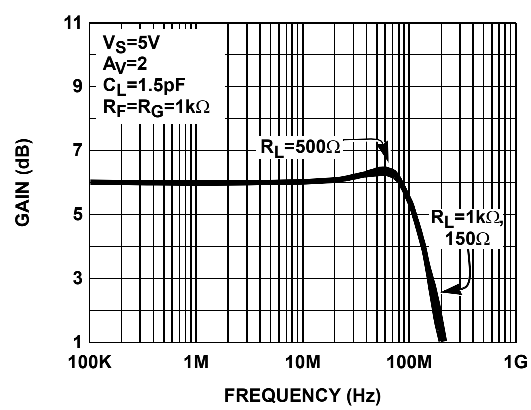


FIGURE 6. SMALL SIGNAL FREQUENCY RESPONSE vs VARIOUS R_{LOAD}

Typical Performance Curves (Continued)

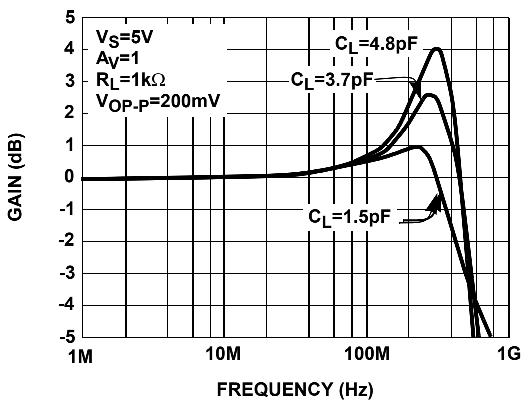


FIGURE 7. SMALL SIGNAL FREQUENCY RESPONSE vs C_L

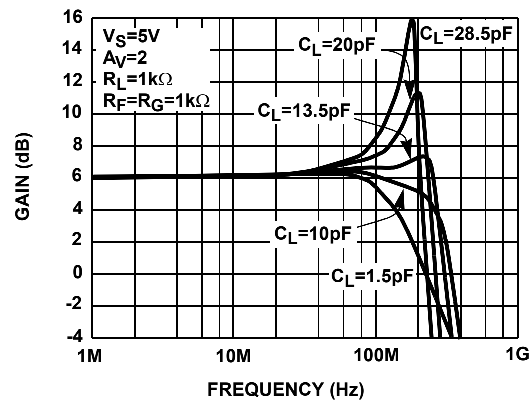


FIGURE 8. SMALL SIGNAL FREQUENCY RESPONSE FOR VARIOUS C_L

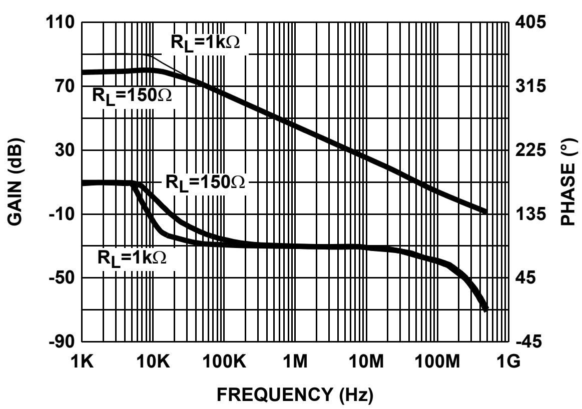


FIGURE 9. OPEN LOOP GAIN AND PHASE vs FREQUENCY

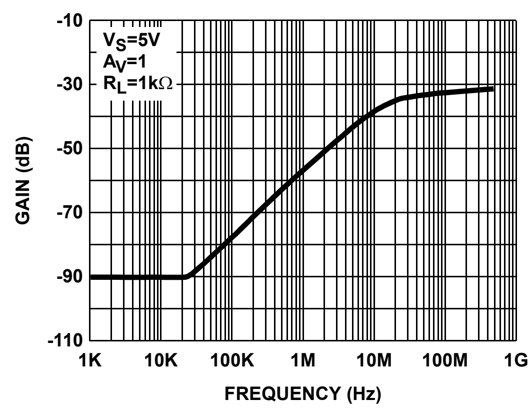


FIGURE 10. DISABLED OUTPUT ISOLATION FREQUENCY RESPONSE

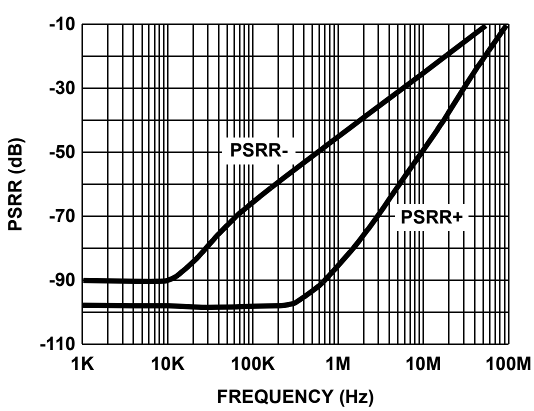


FIGURE 11. POWER SUPPLY REJECTION RATIO vs FREQUENCY

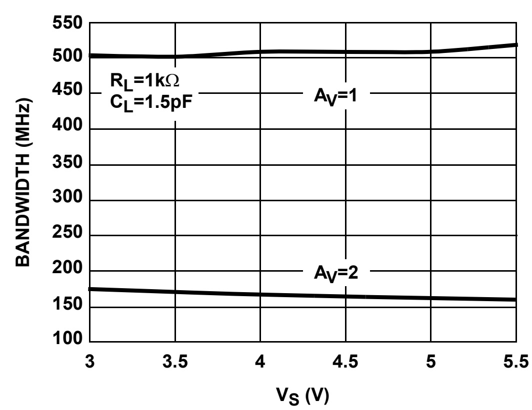


FIGURE 12. SMALL SIGNAL BANDWIDTH vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

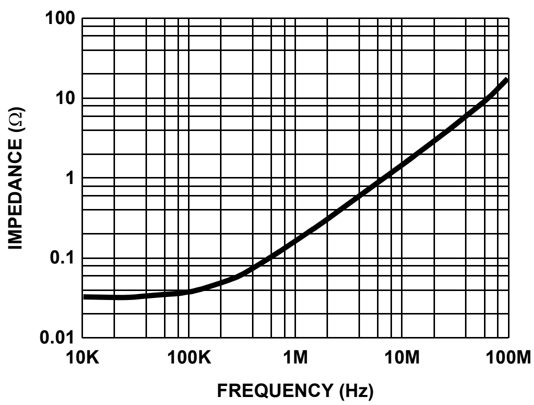


FIGURE 13. OUPUT IMPEDANCE vs FREQUENCY

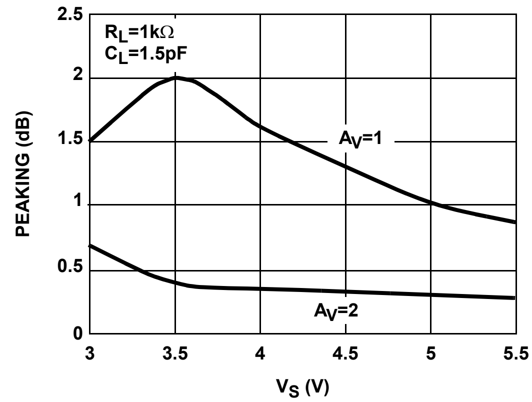


FIGURE 14. SMALL SIGNAL PEAKING vs SUPPLY VOLTAGE

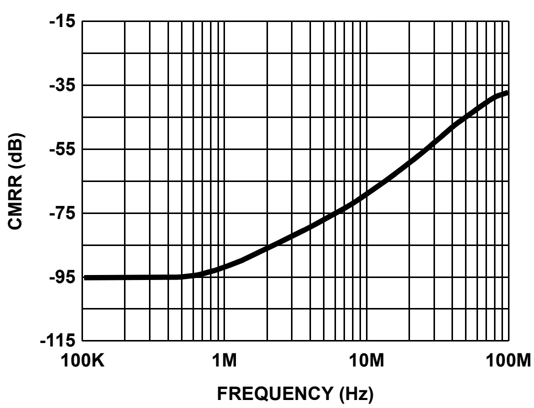


FIGURE 15. COMMON-MODE REJECTION RATIO vs FREQUENCY

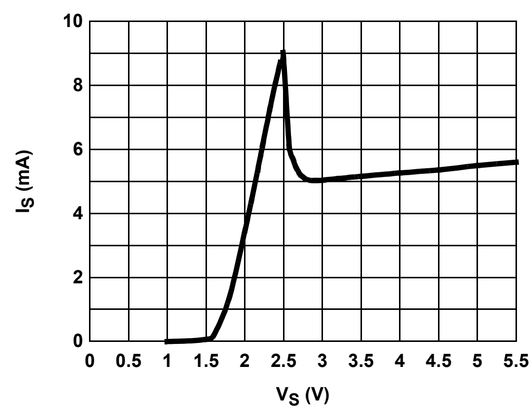


FIGURE 16. SUPPLY CURRENT vs SUPPLY VOLTAGE (PER AMPLIFIER)

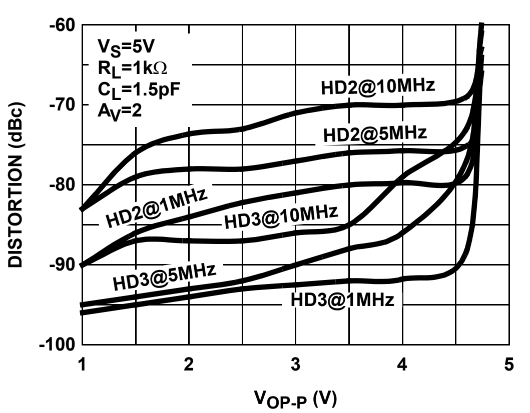


FIGURE 17. HARMONIC DISTORTION vs OUTPUT VOLTAGE

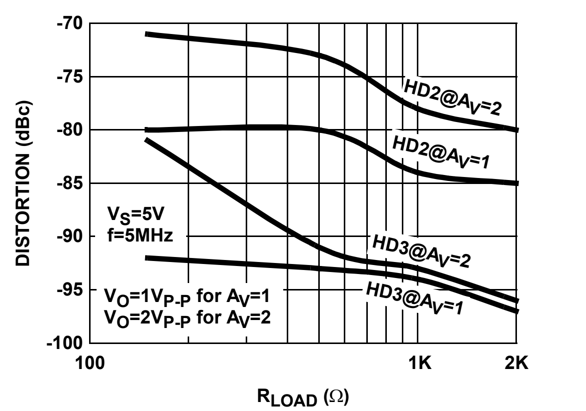


FIGURE 18. HARMONIC DISTORTION vs LOAD RESISTANCE

Typical Performance Curves (Continued)

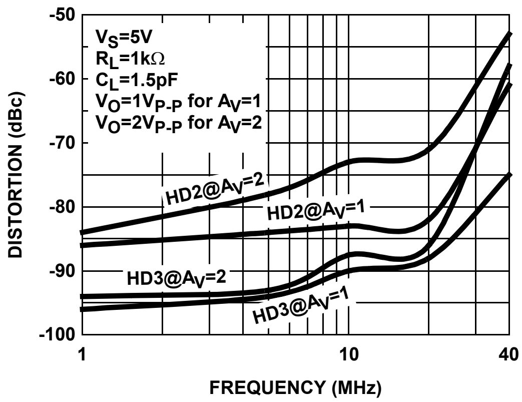


FIGURE 19. HARMONIC DISTORTION vs FREQUENCY

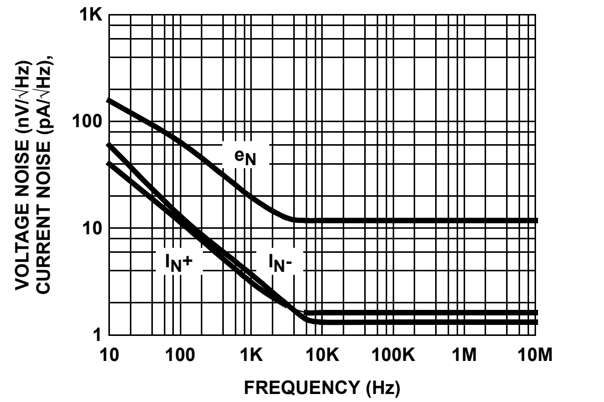


FIGURE 20. VOLTAGE AND CURRENT NOISE vs FREQUENCY

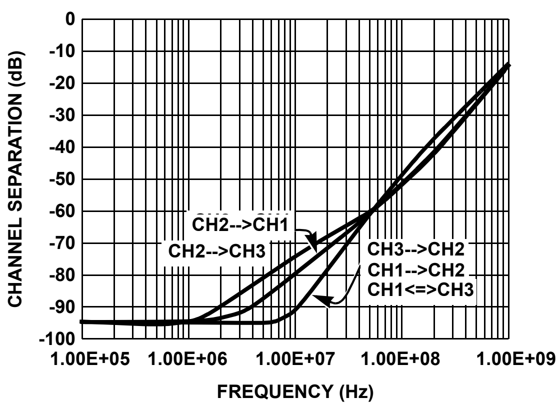


FIGURE 21. CHANNEL SEPARATION vs FREQUENCY

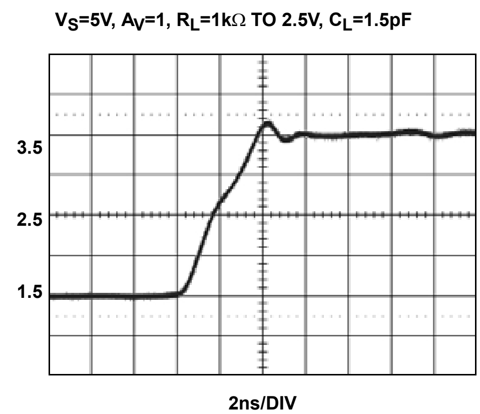


FIGURE 22. LARGE SIGNAL TRANSIENT RESPONSE - RISING

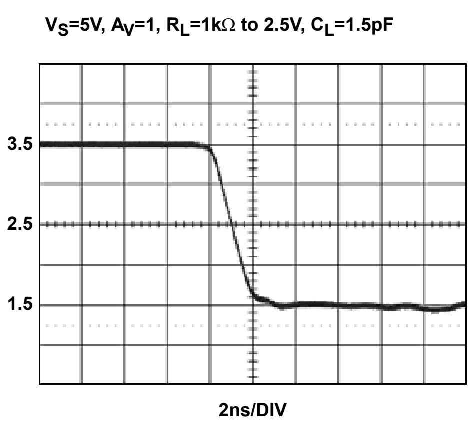


FIGURE 23. LARGE SIGNAL TRANSIENT RESPONSE - FALLING

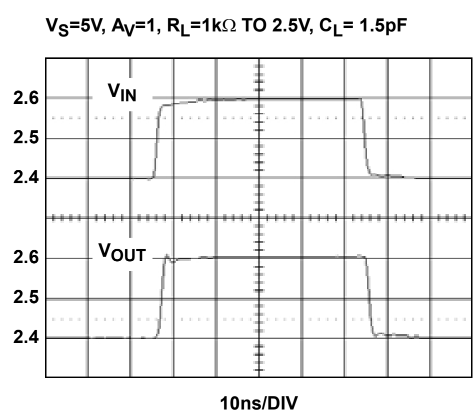


FIGURE 24. SMALL SIGNAL TRANSIENT REPONSE

Typical Performance Curves (Continued)

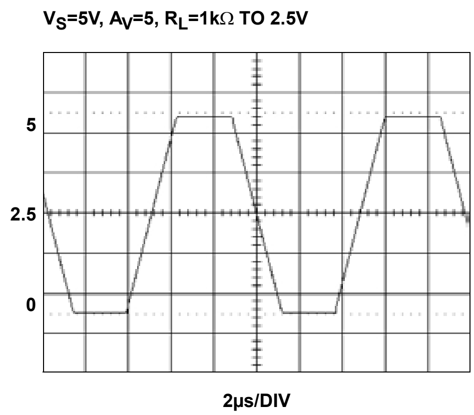


FIGURE 25. OUTPUT SWING

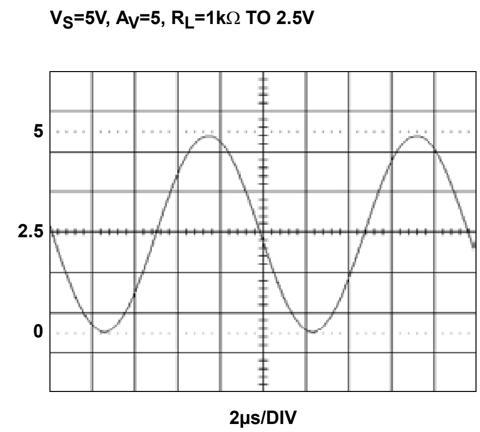


FIGURE 26. OUTPUT SWING

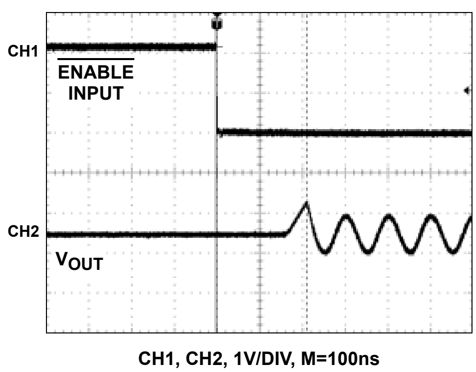


FIGURE 27. ENABLED RESPONSES

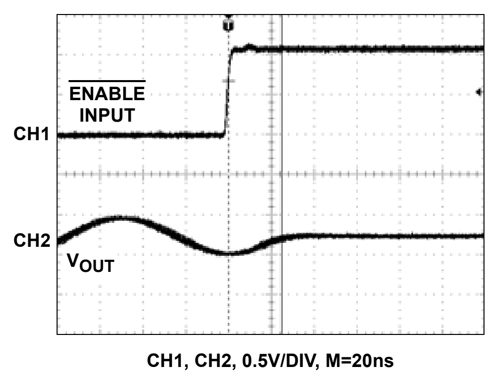


FIGURE 28. DISABLED RESPONSE

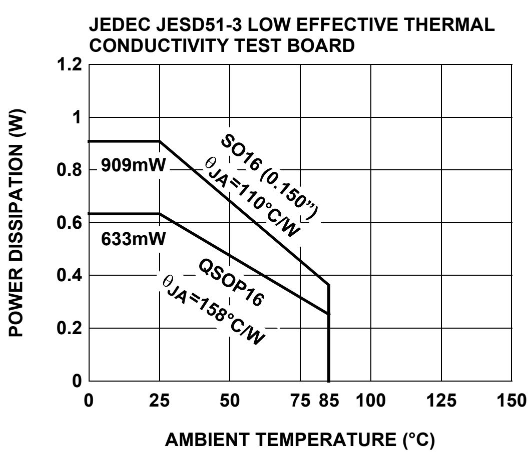


FIGURE 29. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

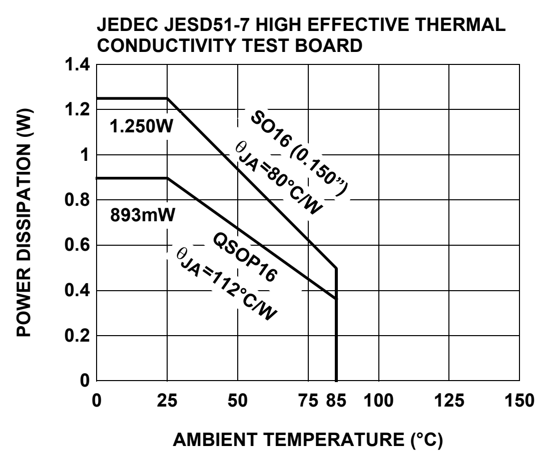
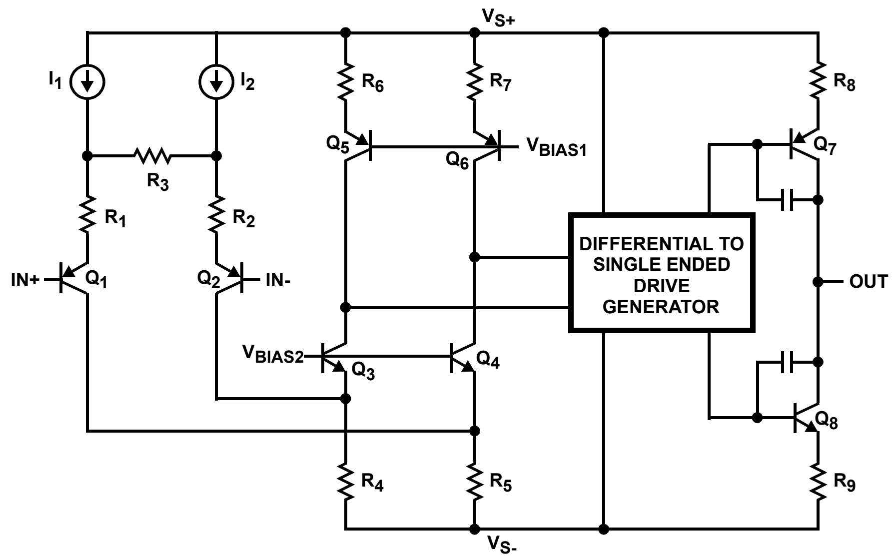


FIGURE 30. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Simplified Schematic Diagram



Description of Operation and Application Information

Product Description

The EL8302 is wide bandwidth, single supply, low power and rail-to-rail output voltage feedback operational amplifiers. The amplifiers are internally compensated for closed loop gain of +1 of greater. Connected in voltage follower mode and driving a 1kΩ load, the EL8302 has a -3dB bandwidth of 500MHz. Driving a 150Ω load, the bandwidth is about 350MHz while maintaining a 600V/us slew rate. The EL8302 is available with a power down pin for each channel to reduce power to 30µA typically while the amplifier is disabled.

Input, Output and Supply Voltage Range

The EL8302 has been designed to operate with a single supply voltage from 3V to 5.0V. Split supplies can also be used as long as their total voltage is within 3V to 5.0V. The amplifiers have an input common mode voltage range from 0.15V below the negative supply (V_S- pin) to within 1.5V of the positive supply (V_S+ pin). If the input signal is outside the above specified range, it will cause the output signal to be distorted.

The output of the EL8302 can swing rail to rail. As the load resistance becomes lower, the ability to drive close to each rail is reduced. For the load resistor 1kΩ, the output swing is about 4.9V at a 5V supply. For the load resistor 150Ω, the output swing is about 4.6V.

Choice of Feedback Resistor and Gain Bandwidth Product

For applications that require a gain of +1, no feedback resistor is required. Just short the output pin to the inverting input pin. For gains greater than +1, the feedback resistor forms a pole with the parasitic capacitance at the inverting input. As this pole becomes smaller, the amplifier's phase margin is reduced. This causes ringing in the time domain and peaking in the frequency domain. Therefore, R_F has some maximum value that should not be exceeded for optimum performance. If a large value of R_F must be used, a small capacitor in the few pF range in parallel with R_F can help to reduce the ringing and peaking at the expense of reducing the bandwidth.

As far as the output stage of the amplifier is concerned, the output stage is also a gain stage with the load. R_F and R_G appear in parallel with R_L for gains other than +1. As this combination gets smaller, the bandwidth falls off. Consequently, R_F also has a minimum value that should not be exceeded for optimum performance. For gain of +1, R_F=0 is optimum. For the gains other than +1, optimum response is obtained with R_F between 300Ω to 1kΩ.

The EL8302 has a gain bandwidth product of 200MHz. For gains ≥5, its bandwidth can be predicted by the following equation:

$$\text{Gain} \times \text{BW} = 200\text{MHz}$$

Video Performance

For good video performance, an amplifier is required to maintain the same output impedance and the same frequency response as DC levels are changed at the output. This is especially difficult when driving a standard video load of 150Ω, because the change in output current with DC level. Special circuitry has been incorporated in the EL8302 to reduce the variation of the output impedance with the current output. This results in dG and dP specifications of 0.01% and 0.01°, while driving 150Ω at a gain of 2. Driving high impedance loads would give a similar or better dG and dP performance.

Driving Capacitive Loads and Cables

The EL8302 can drive 5pF loads in parallel with 1kΩ with less than 5dB of peaking at gain of +1. If less peaking is desired in applications, a small series resistor (usually between 5Ω to 50Ω) can be placed in series with the output to eliminate most peaking. However, this will reduce the gain slightly. If the gain setting is greater than 1, the gain resistor R_G can then be chosen to make up for any gain loss which may be created by the additional series resistor at the output.

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, a back-termination series resistor at the amplifier's output will isolate the amplifier from the cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination resistor. Again, a small series resistor at the output can help to reduce peaking.

Disable/Power-Down

The EL8302 can be disabled and placed its output in a high impedance state. The turn off time is about 25ns and the turn on time is about 200ns. When disabled, the amplifier's supply current is reduced to 30µA typically, thereby effectively eliminating the power consumption. The amplifier's power down can be controlled by standard TTL or CMOS signal levels at the $\overline{\text{ENABLE}}$ pin. The applied logic signal is relative to V_S- pin. Letting the $\overline{\text{ENABLE}}$ pin float or applying a signal that is less than 0.8V above V_S- will enable the amplifier. The amplifier will be disabled when the signal at $\overline{\text{ENABLE}}$ pin is 2V above V_S-.

Output Drive Capability

The EL8302 does not have internal short circuit protection circuitry. They have a typical short circuit current of 80mA sourcing and 150mA sinking for the output is connected to half way between the rails with a 10Ω resistor. If the output is shorted indefinitely, the power dissipation could easily increase such that the part will be destroyed. Maximum reliability is maintained if the output current never exceeds ±40mA. This limit is set by the design of the internal metal interconnections.

Power Dissipation

With the high output drive capability of the EL8302, It is possible to exceed the 125°C absolute maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if the load conditions or package types need to be modified for the amplifier to remain in the safe operating area.

The maximum power dissipation allowed in a package is determined according to:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}}$$

Where:

T_{JMAX} = Maximum junction temperature

T_{AMAX} = Maximum ambient temperature

θ_{JA} = Thermal resistance of the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or:

For sourcing:

$$PD_{MAX} = V_S \times I_{SMAX} + \sum_{i=1}^{3} (V_S - V_{OUTi}) \times \frac{V_{OUTi}}{R_{Li}}$$

For sinking:

$$PD_{MAX} = V_S \times I_{SMAX} + \sum_{i=1}^{3} (V_{OUTi} - V_S-) \times I_{LOADi}$$

Where:

V_S = Total supply voltage

I_{SMAX} = Maximum quiescent supply current

V_{OUTi} = Maximum output voltage of the application for each channel

R_{LOADi} = Load resistance tied to ground for each channel

I_{LOADi} = Load current for eachh channel

By setting the two PD_{MAX} equations equal to each other, we can solve the output current and R_{LOAD} to avoid the device overheat.

Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, a good printed circuit board layout is necessary for optimum performance. Lead lengths should be as short as possible. The power supply pin must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the V_S- pin is connected to the ground plane, a single 4.7µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor from V_S+ to GND will suffice. This same capacitor combination should be placed at each supply pin to ground if split supplies are to be used. In this case, the V_S- pin becomes the negative supply rail.

For good AC performance, parasitic capacitance should be kept to a minimum. Use of wire wound resistors should be avoided because of their additional series inductance. Use of sockets should also be avoided if possible. Sockets add parasitic inductance and capacitance that can result in compromised performance. Minimizing parasitic capacitance at the amplifier's inverting input pin is very important. The feedback resistor should be placed very close to the inverting input pin. Strip line design techniques are recommended for the signal traces.

Typical Applications

VIDEO SYNC PULSE REMOVER

Many CMOS analog to digital converters have a parasitic latch up problem when subjected to negative input voltage levels. Since the sync tip contains no useful video information and it is a negative going pulse, we can chop it off. Figure 31 shows a gain of 2 connections for EL8302. Figure 32 shows the complete input video signal applied at the input, as well as the output signal with the negative going sync pulse removed.

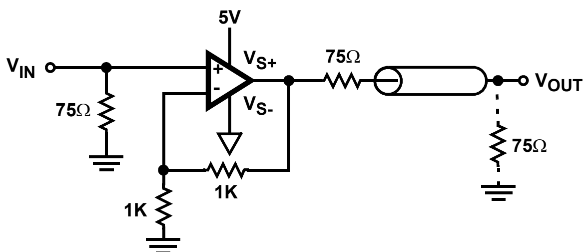


FIGURE 31. SYNC PULSE REMOVER

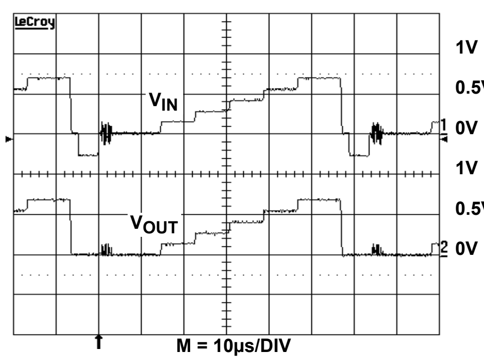


FIGURE 32. VIDEO SIGNAL

MULTIPLEXER

Besides the normal power down usage, the $\overline{\text{ENABLE}}$ pin of the EL8302 can be used for multiplexing applications. Figure 33 shows two channels with the outputs tied together, driving a back terminated 75Ω video load. A $2V_{P-P}$ 2MHz sine wave is applied to Amp A and a $1V_{P-P}$ 2MHz sine wave is applied to Amp B. Figure 34 shows the $\overline{\text{ENABLE}}$ signal and the resulting output waveform at V_{OUT}. Observe the break-before-make operation of the multiplexing. Amp A is on and V_{IN1} is passed through to the output when the $\overline{\text{ENABLE}}$ signal is low and turns off in about 25ns when the $\overline{\text{ENABLE}}$ signal is high. About 200ns later, Amp B turns on and V_{IN2} is passed through to the output. The break-before-make operation ensures that more than one amplifier isn't trying to drive the bus at the same time.

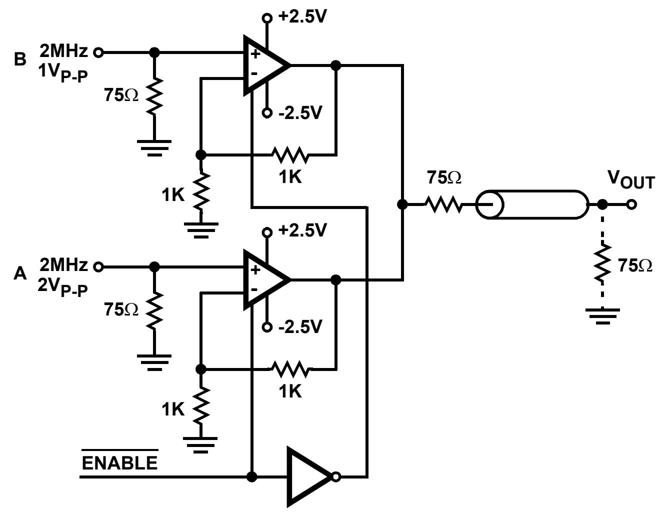


FIGURE 33. TWO TO ONE MULTIPLEXER

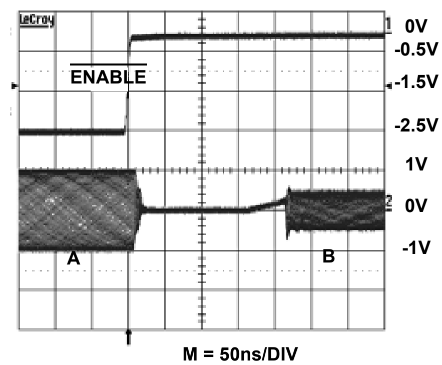


FIGURE 34.

SINGLE SUPPLY VIDEO LINE DRIVER

The EL8302 is wideband rail-to-rail output op amplifiers with large output current, excellent dG, dP, and low distortion that allow them to drive video signals in low supply applications. Figure 35 is the single supply non-inverting video line driver configuration and Figure 36 is the inverting video ling driver configuration. The signal is AC coupled by C_1. R_1 and R_2 are used to level shift the input and output to provide the largest output swing. R_F and R_G set the AC gain. C_2 isolates the virtual ground potential. R_T and R_3 are the termination resistors for the line. C_1, C_2 and C_3 are selected big enough to minimize the droop of the luminance signal.

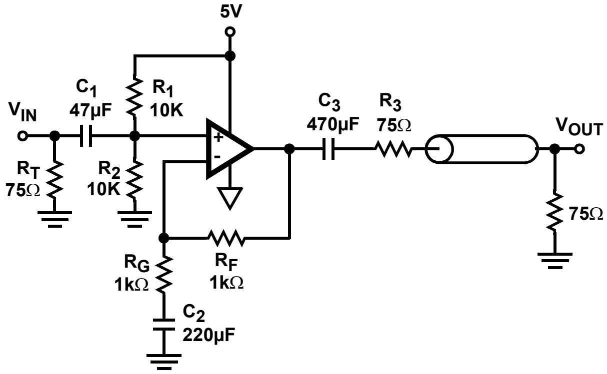


FIGURE 35. 5V SINGLE SUPPLY NON INVERTING VIDEO LINE DRIVER

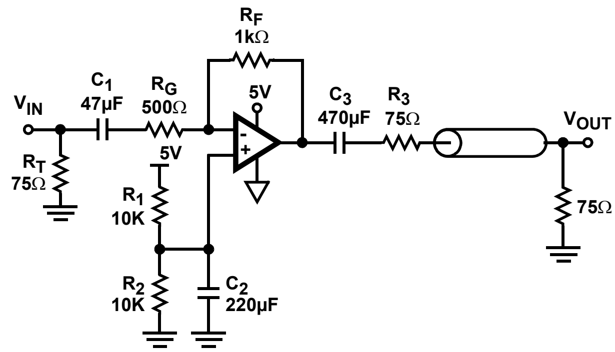


FIGURE 36. SINGLE SUPPLY INVERTING VIDEO LINE DRIVER

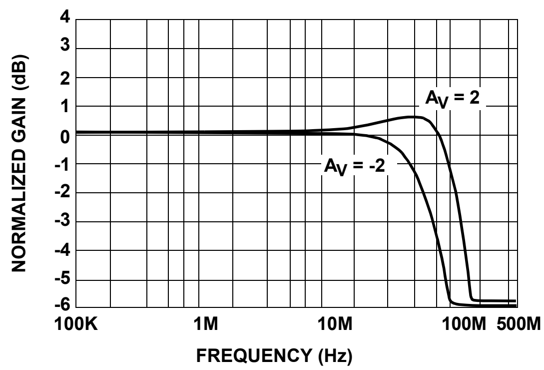
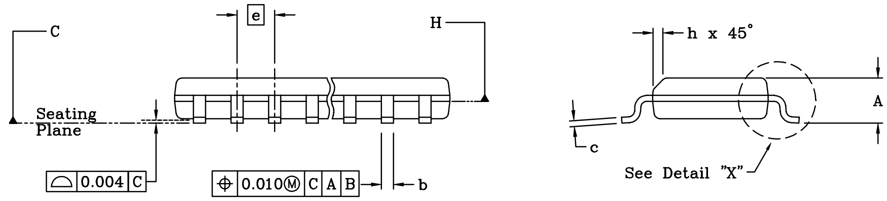
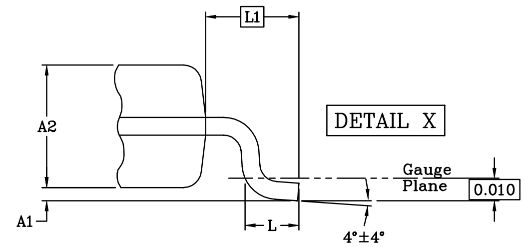
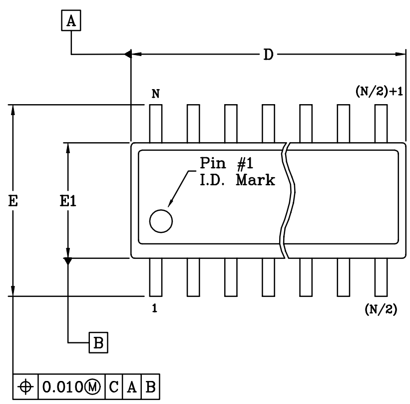


FIGURE 37. VIDEO LINE DRIVER FREQUENCY RESPONSE

SO Package Outline Drawing







DIMENSION TABLE

Symbol	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)	Tolerance
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX.
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	+/- 0.003
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	+/- 0.002
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	+/- 0.003
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	+/- 0.001
D (1)(3)	0.193	0.341	0.390	0.406	0.504	0.606	0.704	+/- 0.004
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	+/- 0.008
E1 (2)(3)	0.154	0.154	0.154	0.295	0.295	0.295	0.295	+/- 0.004
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	+/- 0.009
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference
N	8	14	16	16	20	24	28	Reference

Drawing #: MDP0027	PACKAGE OUTLINE DRAWING SMALL OUTLINE (SO) PACKAGE FAMILY
Rev: L	
Date: 2/15/01	
Units: Inches	élantec Semiconductor, Inc. HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS
JEDEC Reg: MS-012/013	

Notes:

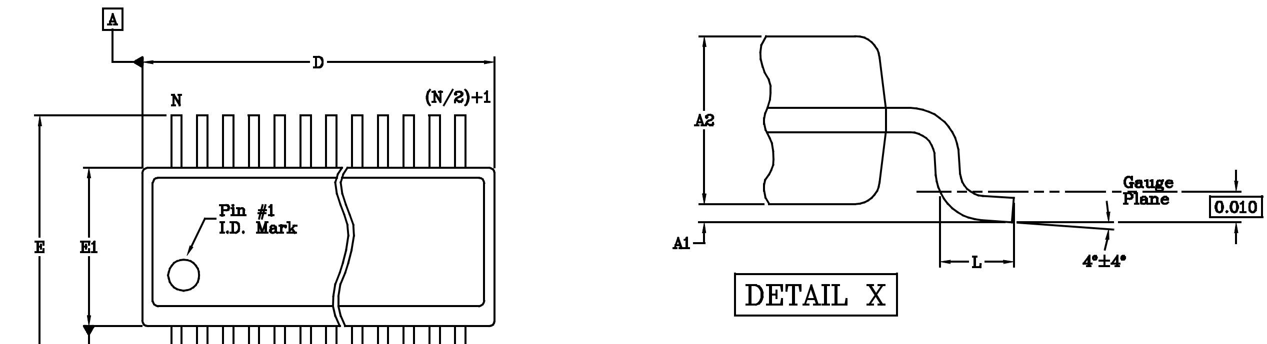
(1) Plastic or metal protrusions of 0.006" maximum per side are not included.

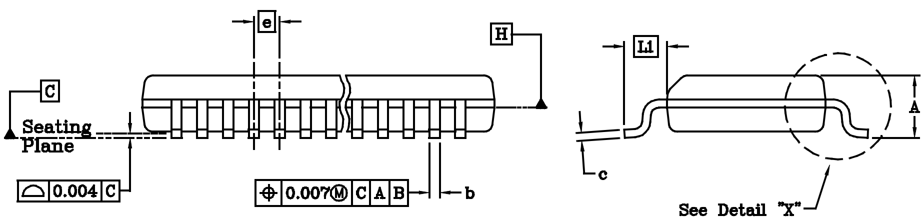
(2) Plastic interlead protrusions of 0.010" maximum per side are not included.

(3) Dimensions "D" and "E1" are measured at Datum Plane "H".

(4) Dimensioning and tolerancing per ASME Y14.5M-1994.

QSOP Package Outline Drawing





DIMENSION TABLE				
Symbol	QSOP16	QSOP24	QSOP28	Tolerance
A	0.068	0.068	0.068	MAX.
A1	0.006	0.006	0.006	+/− 0.002
A2	0.056	0.056	0.056	+/− 0.004
D (1)(3)	0.193	0.341	0.390	+/− 0.004
E	0.236	0.236	0.236	+/− 0.008
E1 (2)(3)	0.154	0.154	0.154	+/− 0.004
L	0.025	0.025	0.025	+/− 0.009
L1	0.041	0.041	0.041	Basic
b	0.010	0.010	0.010	+/− 0.002
c	0.008	0.008	0.008	+/− 0.001
e	0.025	0.025	0.025	Basic
N	16	24	28	Reference

Drawing #: MDP0040
Rev: E
Date: 3/19/01
Units: Inches
JEDEC Reg: MO-137

PACKAGE OUTLINE DRAWING
QSOP – 0.150" NARROW BODY PACKAGE

élantec Semiconductor, Inc.
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Notes:
(1) Plastic or metal protrusions of 0.006" maximum per side are not included.
(2) Plastic interlead protrusions of 0.010" maximum per side are not included.
(3) Dimensions "D" and "E1" are measured at Datum Plane "H".
(4) Dimensioning and tolerancing per ASME Y14.5M-1994.

NOTE: The package drawing shown here may not be the latest version. To check the latest revision, please refer to the Intersil website at http://www.intersil.com/design/packages/index.asp