National Semiconductor

October 2007

LMV841/LMV842/LMV844 CMOS Input, RRIO, Wide Supply Range Operational Amplifiers

General Description

The LMV841/LMV842/LMV844 are low-voltage and low-power operational amplifiers that operate with supply voltages ranging from 2.7V to 12V and have rail-to-rail input and output capability. Their low offset voltage, low supply current, and MOS inputs make them ideal for sensor interface and battery-powered applications.

The single LMV841 is offered in the space-saving 5-Pin SC70 package, the dual LMV842 in the 8-Pin MSOP and 8-Pin SOIC packages, and the quad LMV844 in the 14-Pin TSSOP and 14-Pin SOIC packages. These small packages are ideal solutions for area-constrained PC boards and portable electronics.

Features

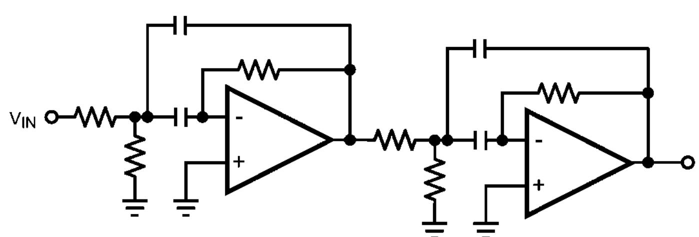
Unless otherwise noted, typical values at T_A = 25°C, V^+ = 5V.

- Space saving 5-Pin SC70 package
- Supply voltage range 2.7V to 12V
- Guaranteed at 3.3V, 5V and ±5V
- Low supply current 1 mA per channel
- Unity gain bandwidth 4.5 MHz
- Open loop gain 133 dB
- Input offset voltage 500 µV max
- Input bias current 0.3 pA
- CMRR 112 dB
- Input voltage noise 20 nV/√Hz
- Temperature range –40°C to 125°C
- Rail-to-Rail input
- Rail-to-Rail output

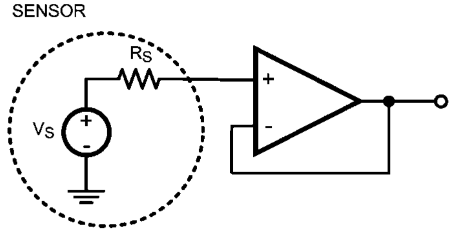
Applications

- High impedance sensor interface
- Battery powered instrumentation
- High gain amplifiers
- DAC buffer
- Instrumentation amplifiers
- Active filters

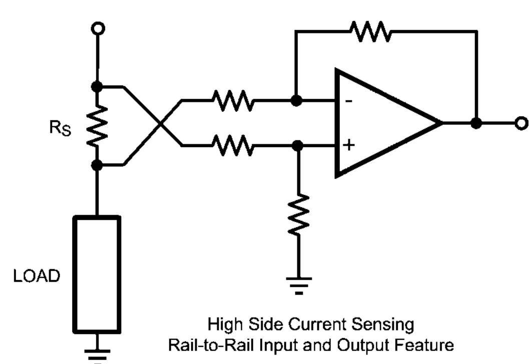
Typical Applications



Active Band-Pass Filter



High Impedance Sensor Interface
CMOS Input Feature



High Side Current Sensing
Rail-to-Rail Input and Output Feature

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Human Body Model	2 kV
Machine Model	200V
V_{IN} Differential	±300 mV
Supply Voltage ($V^+ – V^-$)	13.2V
Voltage at Input/Output Pins	V^++0.3V, V^- −0.3V
Input Current	10 mA
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 3)	+150°C
Soldering Information	
Infrared or Convection (20 sec)	235°C
Wave Soldering Lead Temp. (10 sec)	260°C

Operating Ratings (Note 1)

Temperature Range (Note 3)	−40°C to +125°C
Supply Voltage ($V^+ – V^-$)	2.7V to 12V
Package Thermal Resistance (θ_{JA} (Note 3))	
5-Pin SC70	334 °C/W
8-Pin MSOP	205 °C/W
8-Pin SOIC	126 °C/W
14-Pin TSSOP	110 °C/W
14-Pin SOIC	93 °C/W

3.3V Electrical Characteristics (Note 4)

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V^+ = 3.3V, V^- = 0V, V_{CM} = V^+/2, and R_L > 10 MΩ to V^+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
V_{OS}	Input Offset Voltage			±50	±500 **±800**	μV
TCV_{OS}	Input Offset Voltage Drift (Note 7)			0.5	**±5**	μV/°C
I_B	Input Bias Current (Notes 7, 8)			0.3	10 **300**	pA
I_{OS}	Input Offset Current			40		fA
CMRR	Common Mode Rejection Ratio LMV841	0V ≤ V_{CM} ≤ 3.3V	84 **80**	112		dB
	Common Mode Rejection Ratio LMV842 and LMV844		77 **75**	106		
PSRR	Power Supply Rejection Ratio	2.7V ≤ V^+ ≤ 12V, V_O = V^+/2	86 **82**	108		dB
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 50 dB	**−0.1**		**3.4**	V
A_{VOL}	Large Signal Voltage Gain	R_L = 2 kΩ V_O = 0.3V to 3.0V	100 **96**	123		dB
		R_L = 10 kΩ V_O = 0.2V to 3.1V	100 **96**	131		
V_O	Output Swing High, (measured from V^+)	R_L = 2 kΩ to V^+/2		52	80 **120**	mV
		R_L = 10 kΩ to V^+/2		28	50 **70**	
	Output Swing Low, (measured from V^-)	R_L = 2 kΩ to V^+/2		65	100 **120**	mV
		R_L = 10 kΩ to V^+/2		33	65 **75**	
I_O	Output Short Circuit Current (Notes 3, 9)	Sourcing V_O = V^+/2 V_{IN} = 100 mV	20 **15**	32		mA
		Sinking V_O = V^+/2 V_{IN} = −100 mV	20 **15**	27		
I_S	Supply Current	Per Channel		0.93	1.5 **2**	mA
SR	Slew Rate (Note 10)	A_V = +1, V_O = 2.3 V_{PP} 10% to 90%		2.5		V/μs
GBW	Gain Bandwidth Product			4.5		MHz

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
Φ_m	Phase Margin			67		Deg
e_n	Input-Referred Voltage Noise	f = 1 kHz		20		$nV/\sqrt{Hz}$
R_{OUT}	Open Loop Output Impedance	f = 3 MHz		70		Ω
THD+N	Total Harmonic Distortion + Noise	f = 1 kHz , A_V = 1 R_L = 10 kΩ		0.005		%
C_{IN}	Input Capacitance			7		pF

5V Electrical Characteristics (Note 4)

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = $V^+/2$, and R_L > 10 MΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
V_{OS}	Input Offset Voltage			±50	±500 **±800**	μV
TCV_{OS}	Input Offset Voltage Drift (Note 7)			0.35	**±5**	μV/°C
I_B	Input Bias Current (Notes 7, 8)			0.3	10 **300**	pA
I_{OS}	Input Offset Current			40		fA
CMRR	Common Mode Rejection Ratio LMV841	0V ≤ V_{CM} ≤ 5V	86 **80**	112		dB
	Common Mode Rejection Ratio LMV842 and LMV844		81 **79**	106		
PSRR	Power Supply Rejection Ratio	2.7V ≤ V^+ ≤ 12V, V_O = $V^+/2$	86 **82**	108		dB
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 50 dB	**−0.2**		**5.2**	V
A_{VOL}	Large Signal Voltage Gain	R_L = 2 kΩ V_O = 0.3V to 4.7V	100 **96**	125		dB
		R_L = 10 kΩ V_O = 0.2V to 4.8V	100 **96**	133		
V_O	Output Swing High, (measured from V^+)	R_L = 2 kΩ to $V^+/2$		68	100 **120**	mV
		R_L = 10 kΩ to $V^+/2$		32	50 **70**	
	Output Swing Low, (measured from V^-)	R_L = 2 kΩ to $V^+/2$		78	120 **140**	mV
		R_L = 10 kΩ to $V^+/2$		38	70 **80**	
I_O	Output Short Circuit Current (Notes 3, 9)	Sourcing V_O = $V^+/2$ V_{IN} = 100 mV	20 **15**	33		mA
		Sinking V_O = $V^+/2$ V_{IN} = −100 mV	20 **15**	28		
I_S	Supply Current	Per Channel		0.96	1.5 **2**	mA
SR	Slew Rate (Note 10)	A_V = +1, V_O = 4 V_{PP} 10% to 90%		2.5		V/μs
GBW	Gain Bandwidth Product			4.5		MHz
Φ_m	Phase Margin			67		Deg
e_n	Input-Referred Voltage Noise	f = 1 kHz		20		$nV/\sqrt{Hz}$
R_{OUT}	Open Loop Output Impedance	f = 3 MHz		70		Ω

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
THD+N	Total Harmonic Distortion + Noise	f = 1 kHz , A_V = 1 R_L = 10 kΩ		0.003		%
C_{IN}	Input Capacitance			6		pF

±5V Electrical Characteristics (Note 4)

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V^+ = 5V, V^- = –5V, V_{CM} = 0V, and R_L > 10 MΩ to V_{CM}. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
V_{OS}	Input Offset Voltage			±50	±500 **±800**	µV
TCV_{OS}	Input Offset Voltage Drift (Note 7)			0.25	**±5**	µV/°C
I_B	Input Bias Current (Notes 7, 8)			0.3	10 **300**	pA
I_{OS}	Input Offset Current			40		fA
CMRR	Common Mode Rejection Ratio LMV841	–5V ≤ V_{CM} ≤ 5V	86 **80**	112		dB
	Common Mode Rejection Ratio LMV842 and LMV844		86 **80**	106		
PSRR	Power Supply Rejection Ratio	2.7V ≤ V^+ ≤ 12V, V_O = 0V	86 **82**	108		dB
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 50 dB	**–5.2**		**5.2**	V
A_{VOL}	Large Signal Voltage Gain	R_L = 2 kΩ V_O = –4.7V to 4.7V	100 **96**	126		dB
		R_L = 10 kΩ V_O = –4.8V to 4.8V	100 **96**	136		
V_O	Output Swing High, (measured from V^+)	R_L = 2 kΩ to 0V		95	130 **155**	mV
		R_L = 10 kΩ to 0V		44	75 **95**	
	Output Swing Low, (measured from V^-)	R_L = 2 kΩ to 0V		105	160 **200**	mV
		R_L = 10 kΩ to 0V		52	80 **100**	
I_O	Output Short Circuit Current (Notes 3, 9)	Sourcing V_O = 0V V_{IN} = 100 mV	20 **15**	37		mA
		Sinking V_O = 0V V_{IN} = –100 mV	20 **15**	29		
I_S	Supply Current	Per Channel		1.03	1.7 **2**	mA
SR	Slew Rate (Note 10)	A_V = +1, V_O = 9 V_{PP} 10% to 90%		2.5		V/µs
GBW	Gain Bandwidth Product			4.5		MHz
Φ_m	Phase Margin			67		Deg
e_n	Input-Referred Voltage Noise	f = 1 kHz		20		$nV/\sqrt{Hz}$
R_{OUT}	Open Loop Output Impedance	f = 3 MHz		70		Ω
THD+N	Total Harmonic Distortion + Noise	f = 1 kHz , A_V = 1 R_L = 10 kΩ		0.006		%
C_{IN}	Input Capacitance			3		pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics Tables.

Note 2: Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

Note 3: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Note 4: Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.

Note 5: Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

Note 6: Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlations using statistical quality control (SQC) method.

Note 7: This parameter is guaranteed by design and/or characterization and is not tested in production.

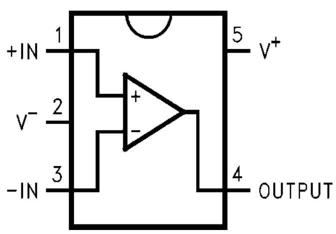
Note 8: Positive current corresponds to current flowing into the device.

Note 9: Short circuit test is a momentary test.

Note 10: Number specified is the slower of positive and negative slew rates.

Connection Diagrams

5-Pin SC70



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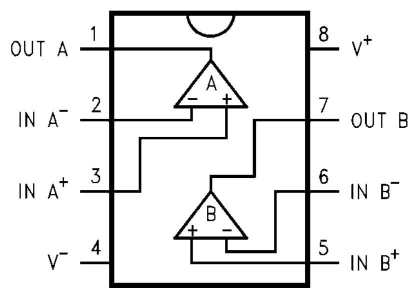
Top View

8-Pin SOIC and MSOP



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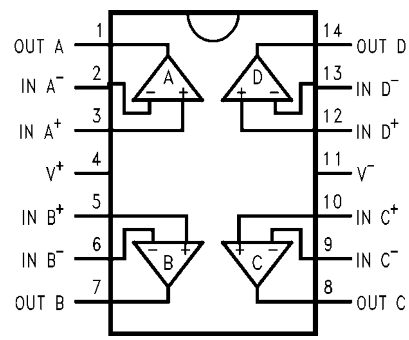
Top View

14–Pin SOIC and TSSOP



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Top View

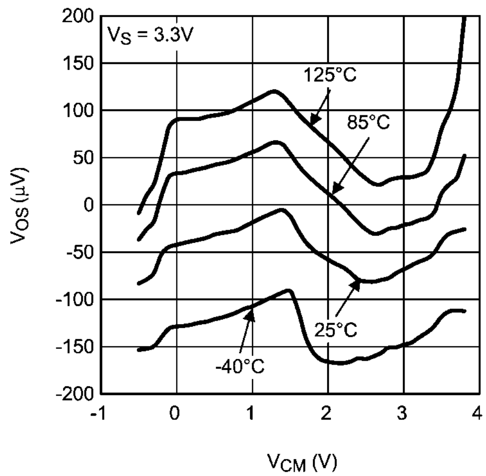
Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
5-Pin SC70	LMV841MG	A97	1k Units Tape and Reel	MAA05A
	LMV841MGX		3k Units Tape and Reel	
8-Pin MSOP	LMV842MM	AC4A	1k Units Tape and Reel	MUA08A
	LMV842MMX		3.5k Units Tape and reel	
8-Pin SOIC	LMV842MA	LMV842MA	95 Units/Rail	M08A
	LMV842MAX		2.5k Units Tape and Reel	
14-Pin SOIC	LMV844MA	LMV844MA	55 Units/Rail	M14A
	LMV844MAX		2.5k Units Tape and Reel	
14-Pin TSSOP	LMV844MT	LMV844MT	94 Units/Rail	MTC14
	LMV844MTX		2.5k Units Tape and Reel	

Typical Performance Characteristics

At T_A = 25°C, R_L = 10 kΩ, V_S = 5V. Unless otherwise specified.

V_{OS} vs. V_{CM} Over Temperature at 3.3V



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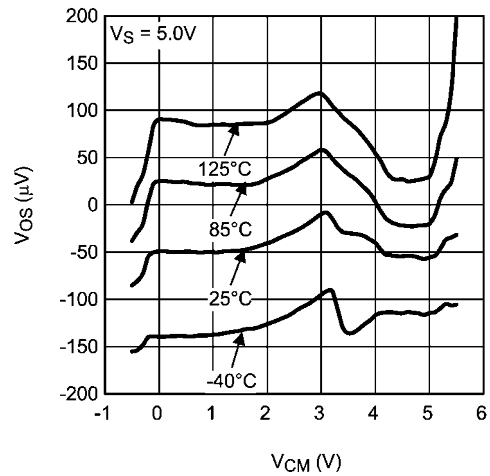
V_{OS} vs. V_{CM} Over Temperature at 5.0V



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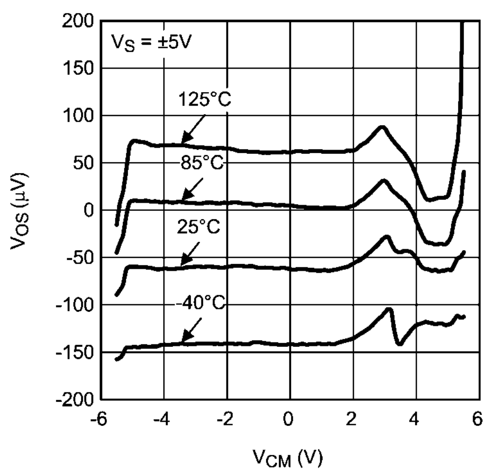
V_{OS} vs. V_{CM} Over Temperature at ±5.0V



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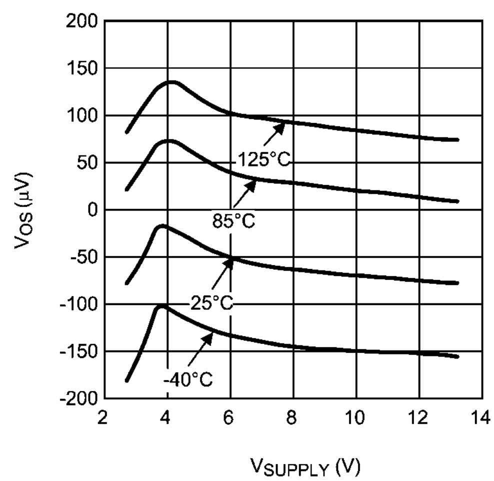
V_{OS} vs. Supply Voltage



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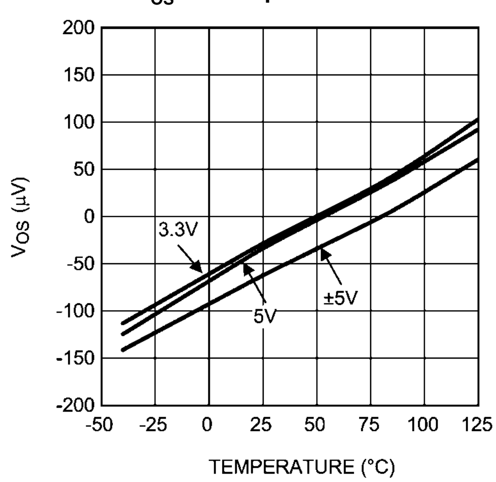
V_{OS} vs. Temperature



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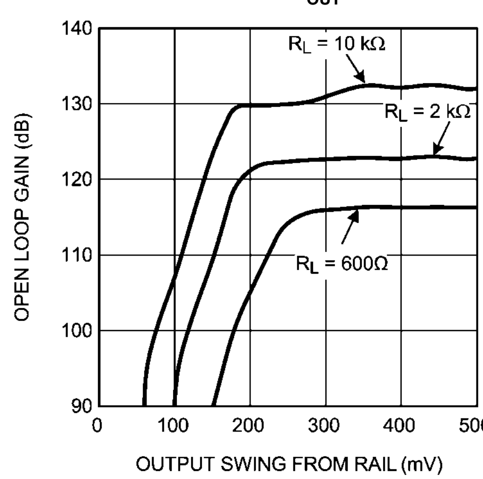
DC Gain vs. V_{OUT}



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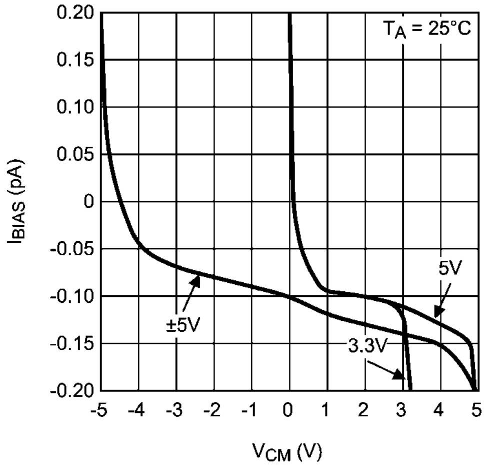
Input Bias Current vs. V_{CM}



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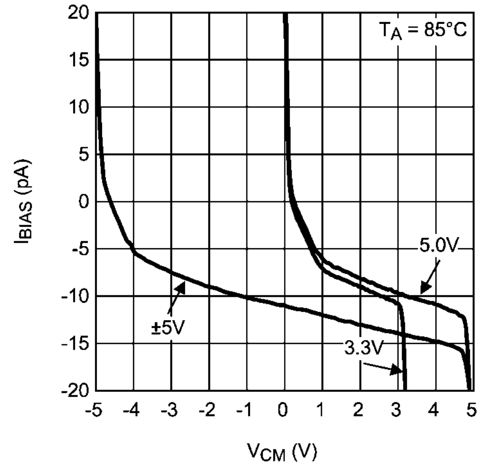
Input Bias Current vs. V_{CM}



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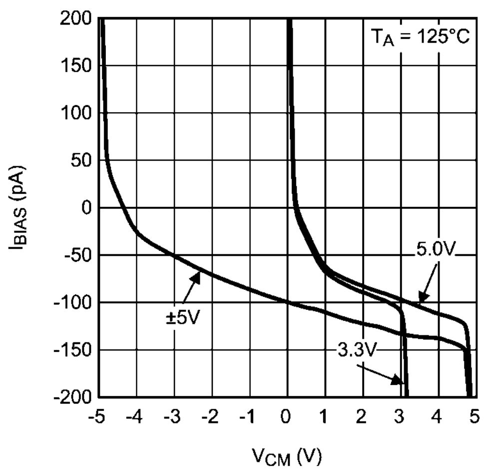
Input Bias Current vs. V_{CM}



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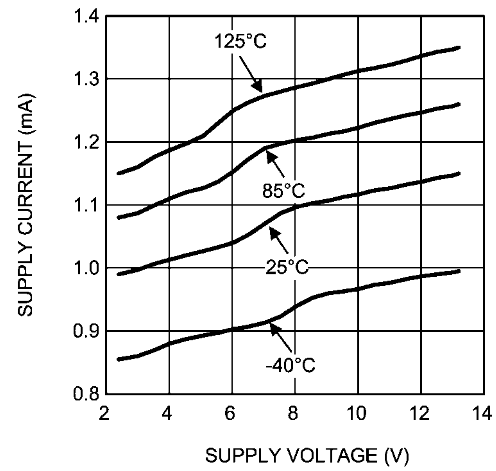
Supply Current per Channel vs. Supply Voltage



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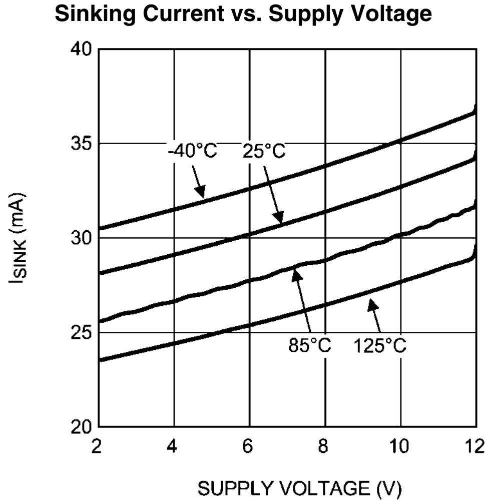
Sinking Current vs. Supply Voltage



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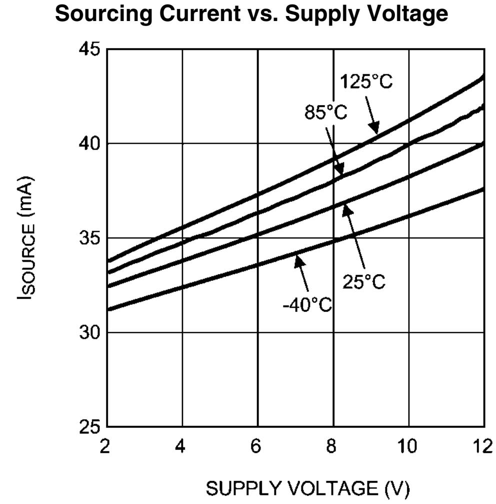
Sourcing Current vs. Supply Voltage



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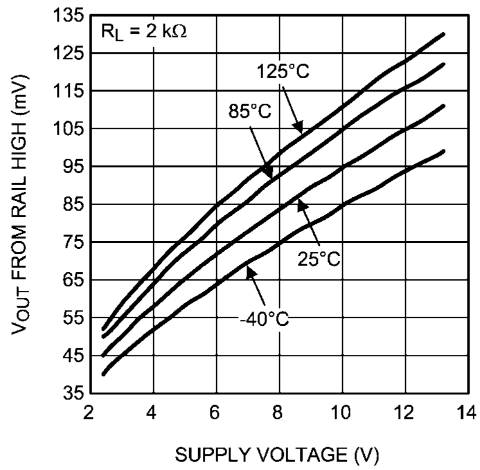
Output Swing High vs. Supply Voltage R_L = 2 kΩ



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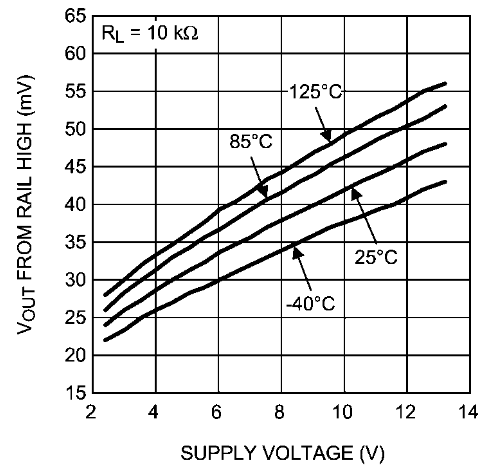
Output Swing High vs. Supply Voltage R_L = 10 kΩ



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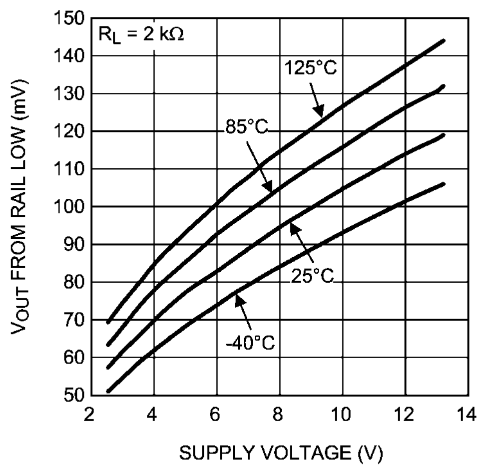
Output Swing Low vs. Supply Voltage R_L = 2 kΩ



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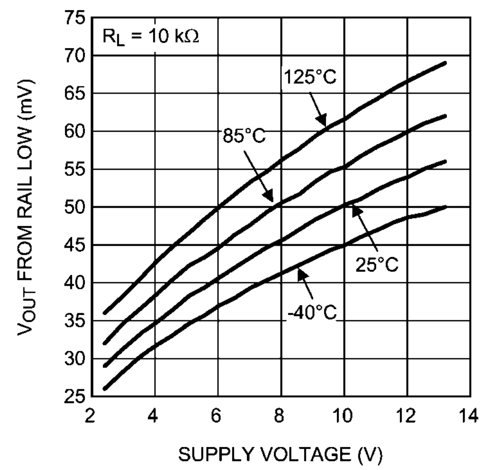
Output Swing Low vs. Supply Voltage R_L = 10 kΩ



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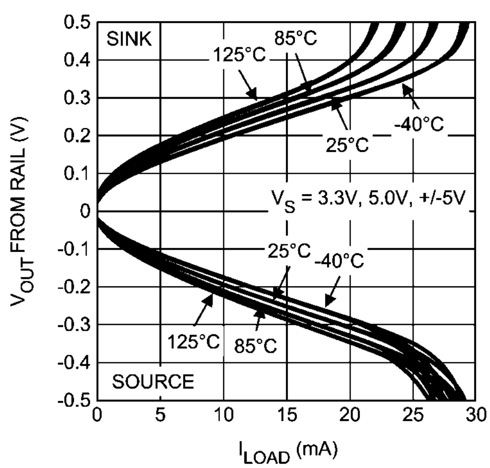
Output Voltage Swing vs. Load Current



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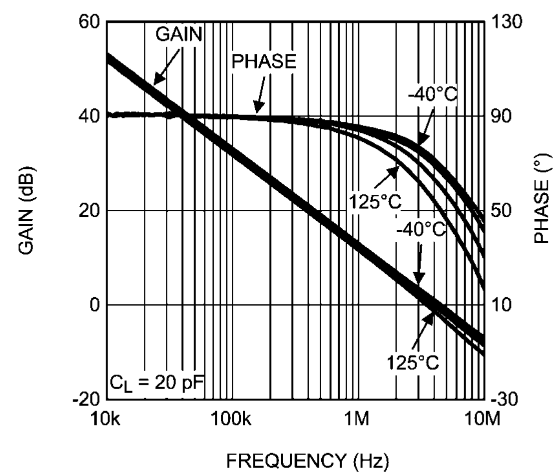
Open Loop Frequency Response Over Temperature



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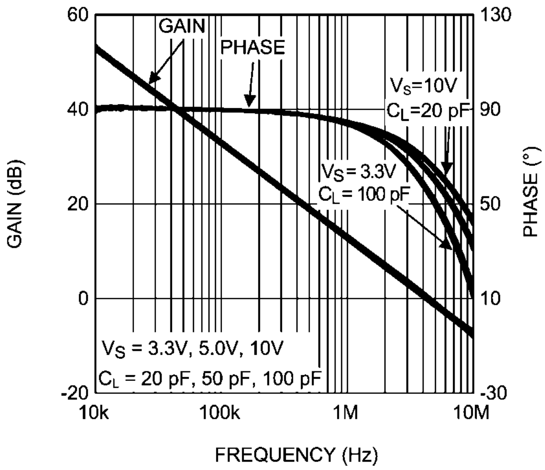
Open Loop Frequency Response Over Load Conditions



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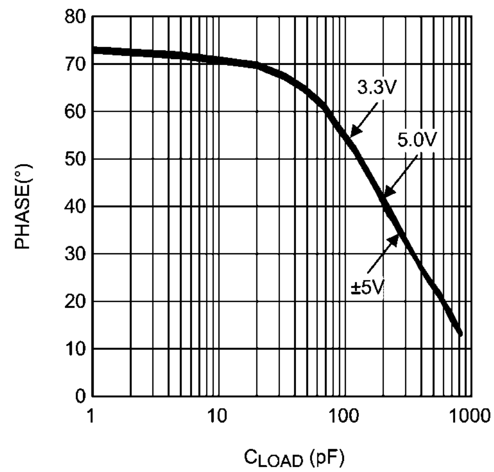
Phase Margin vs. C_L



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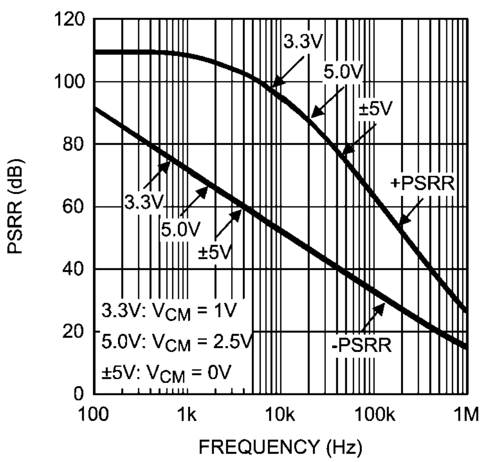
PSRR vs. Frequency



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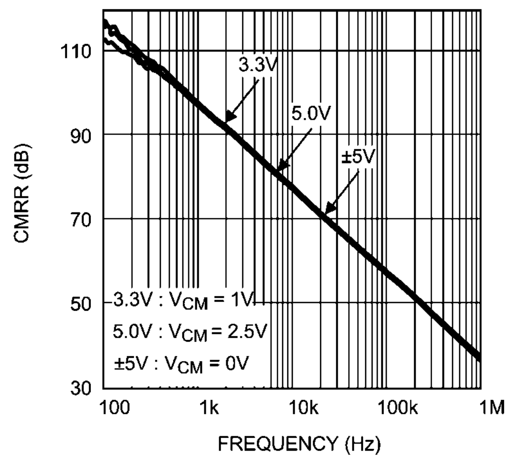
CMRR vs. Frequency



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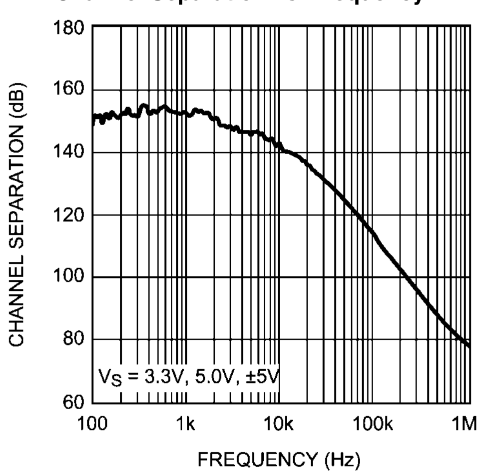
Channel Separation vs. Frequency



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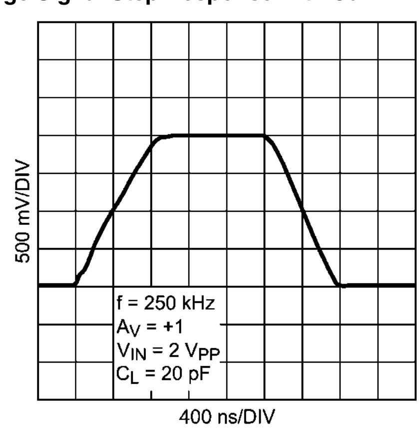
Large Signal Step Response with Gain = 1



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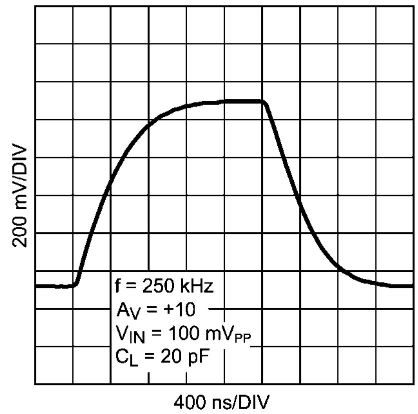
Large Signal Step Response with Gain = 10



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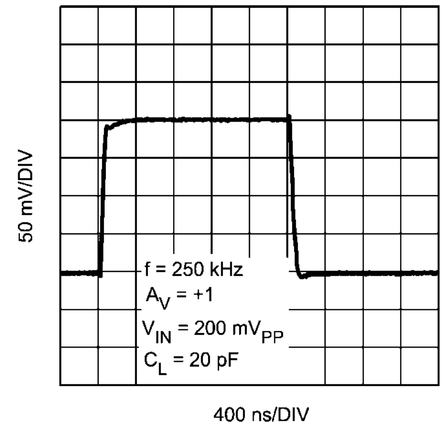
Small Signal Step Response with Gain = 1



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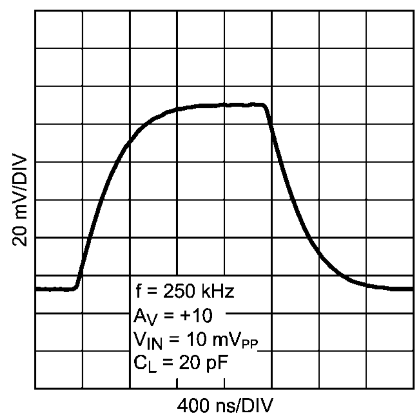
Small Signal Step Response with Gain = 10



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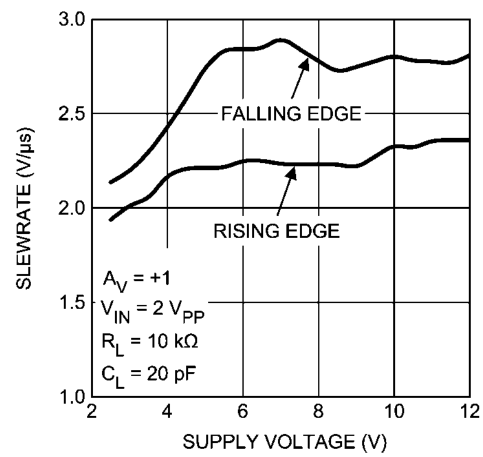
Slew Rate vs Supply Voltage



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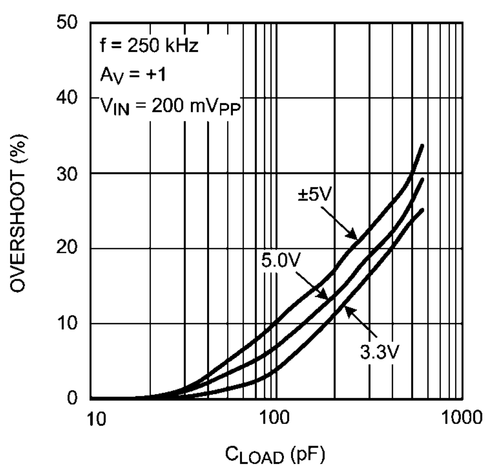
Overshoot vs. C_L



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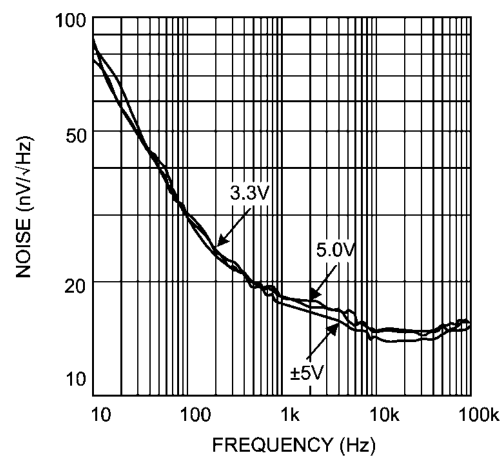
Input Voltage Noise vs. Frequency



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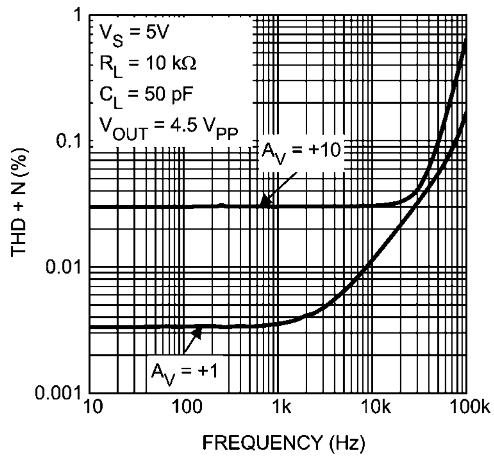
THD+N vs. Frequency



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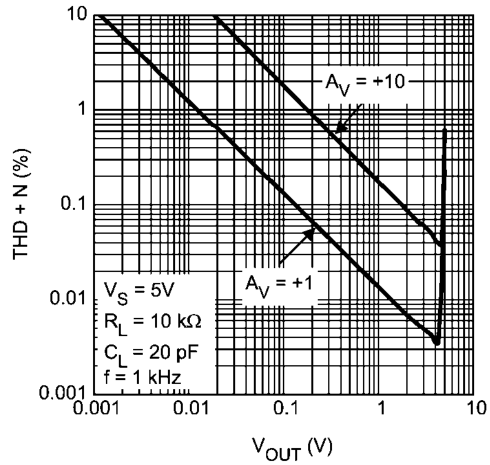
THD+N vs. V_{OUT}



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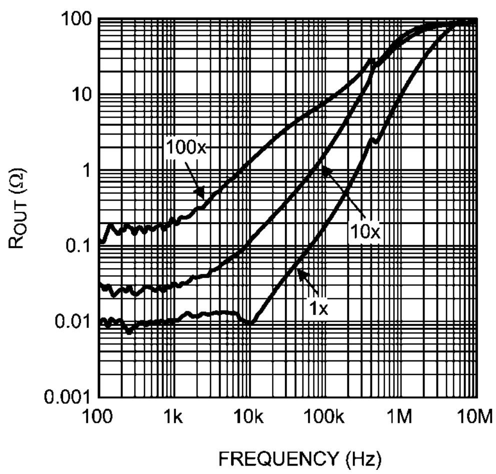
Closed Loop Output Impedance vs. Frequency



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Application Information

INTRODUCTION

The LMV841/LMV842/LMV844 are operational amplifiers with near-precision specifications: low noise, low temperature drift, low offset, and rail-to-rail input and output. Possible application areas include instrumentation, medical, test equipment, audio, and automotive applications.

Its low supply current of 1mA per amplifier, temperature range of −40°C to 125°C, 12V supply with CMOS input, and the small SC70 package for the LMV841 make the LMV841/LMV842/LMV844 a unique op amp family and a perfect choice for portable electronics.

INPUT PROTECTION

The LMV841/LMV842/LMV844 have a set of anti-parallel diodes D_1 and D_2 between the input pins, as shown in *Figure 1*. These diodes are present to protect the input stage of the amplifier. At the same time, they limit the amount of differential input voltage that is allowed on the input pins.

A differential signal larger than one diode voltage drop can damage the diodes. The differential signal between the inputs needs to be limited to ±300 mV or the input current needs to be limited to ±10 mA.

Note that when the op amp is slewing, a differential input voltage exists that forward biases the protection diodes. This may result in current being drawn from the signal source. While this current is already limited by the internal resistors R_1 and R_2 (both 130Ω), a resistor of 1 kΩ can be placed in the feedback path, or a 500Ω resistor can be placed in series with the input signal for further limitation.

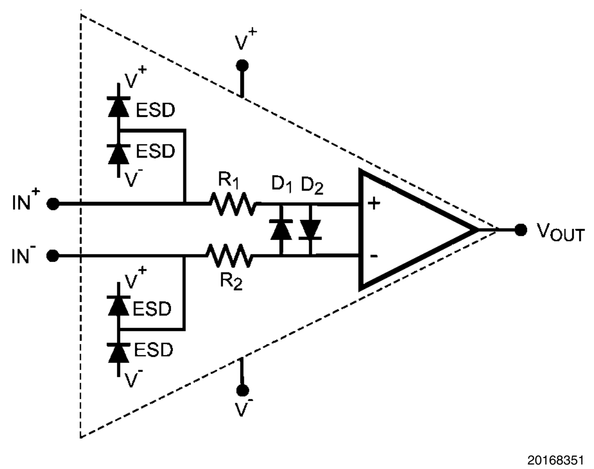

FIGURE 1. Protection Diodes between the Input Pins

INPUT STAGE

The input stage of this amplifier consists of both a PMOS and an NMOS input pair to achieve a rail-to-rail input range. For input voltages close to the negative rail, only the PMOS pair is active. Close to the positive rail, only the NMOS pair is active. In a transition region that extends from approximately 2V below V^+ to 1V below V^+, both pairs are active, and one pair gradually takes over from the other. In this transition region, the input-referred offset voltage changes from the offset voltage associated with the PMOS pair to that of the NMOS pair. The input pairs are trimmed independently to guarantee an input offset voltage of less then 0.5 mV at room temperature over the complete rail-to-rail input range. This also significantly improves the CMRR of the amplifier in the transition region. Note that the CMRR and PSRR limits in the tables are large-signal numbers that express the maximum variation of the amplifier's input offset over the full common-mode voltage and supply voltage range, respectively. When the amplifier's common-mode input voltage is within the transition region, the small signal CMRR and PSRR may be slightly lower than the large signal limits.

CAPACITIVE LOAD

The LMV841/LMV842/LMV844 can be connected as non-inverting unity gain amplifiers. This configuration is the most sensitive to capacitive loading. The combination of a capacitive load placed on the output of an amplifier along with the amplifier's output impedance creates a phase lag, which reduces the phase margin of the amplifier. If the phase margin is significantly reduced, the response will be underdamped which causes peaking in the transfer and, when there is too much peaking, the op amp might start oscillating.

The LMV841/LMV842/LMV844 can directly drive capacitive loads up to 100 pF without any stability issues. In order to drive heavier capacitive loads, an isolation resistor, R_{ISO}, should be used, as shown in *Figure 2*. By using this isolation resistor, the capacitive load is isolated from the amplifier's output, and hence, the pole caused by C_L is no longer in the feedback loop. The larger the value of R_{ISO}, the more stable the output voltage will be. If values of R_{ISO} are sufficiently large, the feedback loop will be stable, independent of the value of C_L. However, larger values of R_{ISO} result in reduced output swing and reduced output current drive.

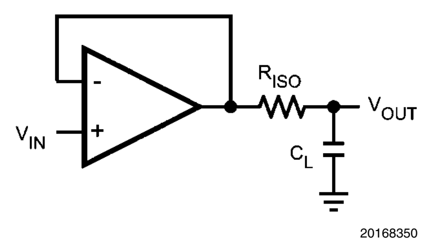

FIGURE 2. Isolating Capacitive Load

DECOUPLING AND LAYOUT

For decoupling the supply lines it is suggested that 10 nF capacitors be placed as close as possible to the op amp.

For single supply, place a capacitor between V^+ and V^-. For dual supplies, place one capacitor between V^+ and the board ground, and the second capacitor between ground and V^-.

OP AMP CIRCUIT NOISE

The LMV841/LMV842/LMV844 have good noise specifications, and will frequently be used in low-noise applications. Therefore it is important to determine the noise of the total circuit. Besides the input referred noise of the op amp, the feedback resistors may have an important contribution to the total noise.

For applications with a voltage input configuration it is, in general, beneficial to keep the resistor values low. In these configurations high resistor values mean high noise levels. However, using low resistor values will increase the power consumption of the application. This is not always acceptable for portable applications, so there is a trade-off between noise level and power consumption.

Besides the noise contribution of the signal source, three types of noise need to be taken into account for calculating the noise performance of an op amp circuit:

- Input referred voltage noise of the op amp
- Input referred current noise of the op amp
- Noise sources of the resistors in the feedback network, configuring the op amp

To calculate the noise voltage at the output of the op amp, the first step is to determine a total equivalent noise source. This requires the transformation of all noise sources to the same reference node. A convenient choice for this node is the input of the op amp circuit. The next step is to add all the noise sources. The final step is to multiply the total equivalent input voltage noise with the gain of the op amp configuration.

The input referred voltage noise of the op amp is already located at the input, we can use the input referred voltage noise without further transferring. The input referred current noise needs to be converted to an input referred voltage noise. The current noise is negligibly small, as long as the equivalent resistance is not unrealistically large, so we can leave the current noise out for these examples. That leaves us with the noise sources of the resistors, being the thermal noise voltage. The influence of the resistors on the total noise can be seen in the following examples, one with high resistor values and one with low resistor values. Both examples describe an op amp configuration with a gain of 101 which will give the circuit a bandwidth of 44.5 kHz. The op amp noise is the same for both cases, i.e. an input referred noise voltage of 20 nV/$\sqrt{Hz}$ and a negligibly small input referred noise current.

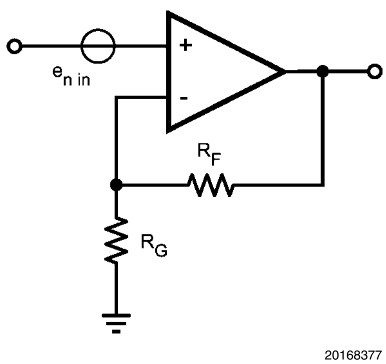

FIGURE 3. Noise Circuit

To calculate the noise of the resistors in the feedback network, the equivalent input referred noise resistance is needed. For the example in *Figure 3*, this equivalent resistance R_{eq} can be calculated using the following equation:

$$R_{eq} = \frac{R_F \times R_G}{R_F + R_G}$$

The voltage noise of the equivalent resistance can be calculated using the following equation:

$$e_{nr} = \sqrt{4kTR_{eq}}$$

where:

e_{nr} = thermal noise voltage of the equivalent resistor R_{eq} (V/$\sqrt{Hz}$)

k = Boltzmann constant (1.38 x 10^{-23} J/K)

T = absolute temperature (K)

R_{eq} = resistance (Ω)

The total equivalent input voltage noise is given by the equation:

$$e_{n\ in} = \sqrt{e_{nv}^2 + e_{nr}^2}$$

where:

$e_{n\ in}$ = total input equivalent voltage noise of the circuit

e_{nv} = input voltage noise of the op amp

The final step is multiplying the total input voltage noise by the noise gain, which is in this case the gain of the op amp configuration:

$$e_{n\ out} = e_{n\ in} \times A_{noise}$$

The equivalent resistance for the first example with a resistor R_F of 10 MΩ and a resistor R_G of 100 kΩ at 25°C (298 K) equals:

$$R_{eq} = \frac{R_F \times R_G}{R_F + R_G} = \frac{10\ M\Omega \times 100\ k\Omega}{10\ M\Omega + 100\ k\Omega} = 99\ k\Omega$$

Now the noise of the resistors can be calculated, yielding:

$$\begin{aligned} e_{nr} &= \sqrt{4kTR_{eq}} \\ &= \sqrt{4 \times 1.38 \times 10^{-23}\ J/K \times 298K \times 99\ k\Omega} \\ &= 40\ nV/\sqrt{Hz} \end{aligned}$$

The total noise at the input of the op amp is:

$$\begin{aligned} e_{n\ in} &= \sqrt{e_{nv}^2 + e_{nr}^2} \\ &= \sqrt{\left(20\ nV/\sqrt{Hz}\right)^2 + \left(40\ nV/\sqrt{Hz}\right)^2} = 45\ nV/\sqrt{Hz} \end{aligned}$$

For the first example, this input noise will, multiplied with the noise gain, give a total output noise of:

$$\begin{aligned} e_{n\ out} &= e_{n\ in} \times A_{noise} \\ &= 45\ nV/\sqrt{Hz} \times 101 = 4.5\ \mu V/\sqrt{Hz} \end{aligned}$$

In the second example, with a resistor R_F of 10 kΩ and a resistor R_G of 100Ω at 25°C (298 K), the equivalent resistance equals:

$$R_{eq} = \frac{R_F \times R_G}{R_F + R_G} = \frac{10\ k\Omega \times 100\Omega}{10\ k\Omega + 100\Omega} = 99\Omega$$

The resistor noise for the second example is:

$$e_{nr} = \sqrt{4kTR_{eq}}$$
$$= \sqrt{4 \times 1.38 \times 10^{-23}\ \text{J/K} \times 298\text{K} \times 99\Omega}$$
$$= 1\ \text{nV}/\sqrt{\text{Hz}}$$

The total noise at the input of the op amp is:

$$e_{n\ in} = \sqrt{e_{nv}^2 + e_{nr}^2}$$
$$= \sqrt{\left(20\ \text{nV}/\sqrt{\text{Hz}}\right)^2 + \left(1\ \text{nV}/\sqrt{\text{Hz}}\right)^2}$$
$$= 20\ \text{nV}/\sqrt{\text{Hz}}$$

For the second example the input noise will, multiplied with the noise gain, give an output noise of

$$e_{n\ out} = e_{n\ in} \times A_{noise}$$
$$= 20\ \text{nV}/\sqrt{\text{Hz}} \times 101 = 2\ \mu\text{V}/\sqrt{\text{Hz}}$$

In the first example the noise is dominated by the resistor noise due to the very high resistor values, in the second example the very low resistor values add only a negligible contribution to the noise and now the dominating factor is the op amp itself. When selecting the resistor values, it is important to choose values that don't add extra noise to the application. Choosing values above 100 kΩ may increase the noise too much. Low values will keep the noise within acceptable levels; choosing very low values however, will not make the noise even lower, but will increase the current of the circuit.

ACTIVE FILTER

The rail-to-rail input and output of the LMV841/LMV842/LMV844 and the wide supply voltage range make these amplifiers ideal to use in numerous applications. One of the typical applications is an active filter as shown in *Figure 4*. This example is a band-pass filter, for which the pass band is widened. This is achieved by cascading two band-pass filters, with slightly different center frequencies.

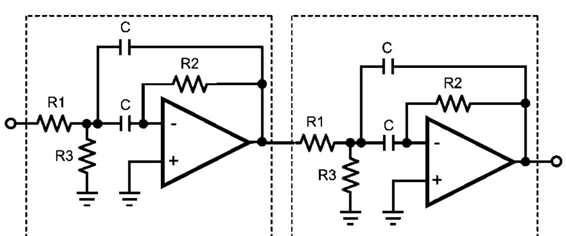

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FIGURE 4. Active Filter

The center frequency of the separate band-pass filters can be calculated by:

$$f_{mid} = \frac{1}{2\pi C}\sqrt{\frac{R_1 + R_3}{R_1\ R_2\ R_3}}$$

In this example a filter was designed with its pass band at 10 kHz. The two separate band-pass filters are designed to have a center frequency of approximately 10% from the frequency of the total filter:

C = 33 nF
R1 = 2 kΩ
R2 = 6.2 kΩ
R3 = 45 Ω

This will give for filter A:

$$f_{mid} = \frac{1}{\pi \times 33\ \text{nF}}\sqrt{\frac{2\ \text{k}\Omega + 6.2\ \text{k}\Omega}{2\ \text{k}\Omega \times 6.2\ \text{k}\Omega \times 45\Omega}} = 9.2\ \text{kHz}$$

and for filter B with C = 27 nF:

$$f_{mid} = \frac{1}{\pi \times 27\ \text{nF}}\sqrt{\frac{2\ \text{k}\Omega + 6.2\ \text{k}\Omega}{2\ \text{k}\Omega \times 6.2\ \text{k}\Omega \times 45\Omega}} = 11.2\ \text{kHz}$$

Bandwidth can be calculated by:

$$B = \frac{1}{\pi R_2 C}$$

For filter A this will give:

$$B = \frac{1}{\pi \times 6.2\ \text{k}\Omega \times 33\ \text{nF}} = 1.6\ \text{kHz}$$

and for filter B:

$$B = \frac{1}{\pi \times 6.2\ \text{k}\Omega \times 27\ \text{nF}} = 1.9\ \text{kHz}$$

The response of the two filters and the combined filter is shown in *Figure 5*.

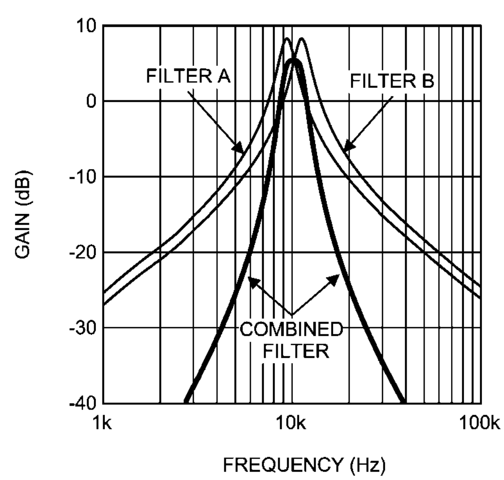

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FIGURE 5. Active Filter Curve

The responses of filter A and filter B are shown as the thin lines in *Figure 5*; the response of the combined filter is shown as the thick line. Shifting the center frequencies of the separate filters farther apart, will result in a wider band; however, positioning the center frequencies too far apart will result in a less flat gain within the band. For wider bands more band-pass filters can be cascaded.

Tip: Use the WEBENCH internet tools at www.national.com for your filter application.

HIGH-SIDE CURRENT SENSING

The rail-to-rail input and the low V_{OS} features make the LMV841/LMV842/LMV844 ideal op amps for high-side current sensing applications.

To measure a current, a sense resistor is placed in series with the load, as shown in *Figure 6*. The current flowing through this sense resistor will result in a voltage drop, that is amplified by the op amp.

Suppose it is necessary to measure a current between 0A and 2A using a sense resistor of 100 mΩ, and convert it to an output voltage of 0 to 5V. A current of 2A flowing through the load and the sense resistor will result in a voltage of 200 mV across the sense resistor. The op amp will amplify this 200 mV to fit the current range to the output voltage range. Use the formula:

$$V_{OUT} = R_F/R_G * V_{SENSE}$$

to calculate the gain needed. For a load current of 2A and an output voltage of 5V the gain would be V_{OUT}/V_{SENSE} = 25.

If the feedback resistor, R_F, is 100 kΩ, then the value for R_G will be 4 kΩ. The tolerance of the resistors has to be low to obtain a good common-mode rejection.

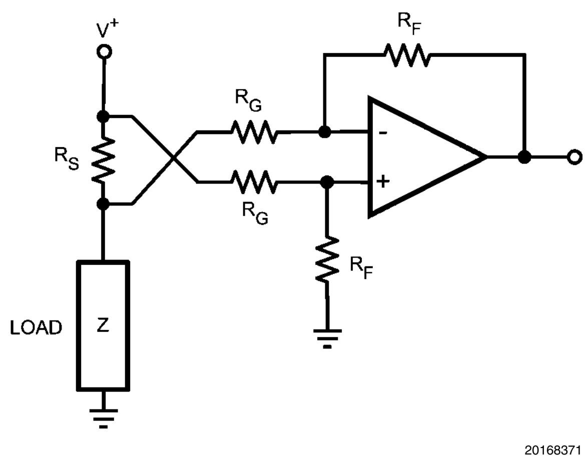


FIGURE 6. High-Side Current Sensing

HIGH IMPEDANCE SENSOR INTERFACE

With CMOS inputs, the LMV841/LMV842/LMV844 are particularly suited to be used as high impedance sensor interfaces.

Many sensors have high source impedances that may range up to 10 MΩ. The input bias current of an amplifier will load the output of the sensor, and thus cause a voltage drop across the source resistance, as shown in *Figure 7*. When an op amp is selected with a relatively high input bias current, this error may be unacceptable.

The low input current of the LMV841/LMV842/LMV844 significantly reduces such errors. The following examples show the difference between a standard op amp input and the CMOS input of the LMV841/LMV842/LMV844.

The voltage at the input of the op amp can be calculated with

$$V_{IN+} = V_S - I_B * R_S$$

For a standard op amp the input bias Ib can be 10 nA. When the sensor generates a signal of 1V (V_S) and the sensors impedance is 10 MΩ (R_S), the signal at the op amp input will be

$$V_{IN} = 1V - 10\ nA * 10\ M\Omega = 1V - 0.1V = 0.9V$$

For the CMOS input of the LMV841/LMV842/LMV844, which has an input bias current of only 0.3 pA, this would give

$$V_{IN} = 1V – 0.3\ pA * 10\ M\Omega = 1V - 3\ \mu V = 0.999997V$$

The conclusion is that a standard op amp, with its high input bias current input, is not a good choice for use in impedance sensor applications. The LMV841/LMV842/LMV844, in contrast, are much more suitable due to the low input bias current. The error is negligibly small; therefore, the LMV841/LMV842/LMV844 are a must for use with high impedance sensors.

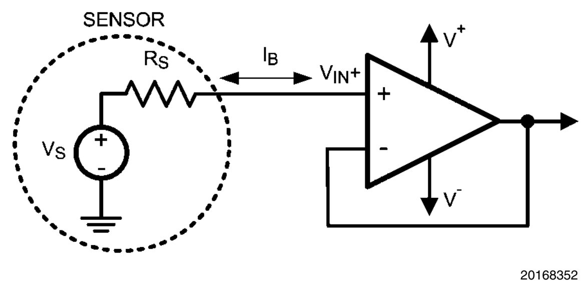


FIGURE 7. High Impedance Sensor Interface

THERMOCOUPLE AMPLIFIER

The following is a typical example for a thermocouple amplifier application using an LMV841, LMV842, or LMV844. A thermocouple senses a temperature and converts it into a voltage. This signal is then amplified by the LMV841, LMV842, or LMV844. An ADC can then convert the amplified signal to a digital signal. For further processing the digital signal can be processed by a microprocessor, and can be used to display or log the temperature, or the temperature data can be used in a fabrication process.

Characteristics of a Thermocouple

A thermocouple is a junction of two different metals. These metals produce a small voltage that increases with temperature.

The thermocouple used in this application is a K-type thermocouple. A K-type thermocouple is a junction between Nickel-Chromium and Nickel-Aluminum. This is one of the most commonly used thermocouples. There are several reasons for using the K-type thermocouple. These include temperature range, the linearity, the sensitivity, and the cost.

A K-type thermocouple has a wide temperature range. The range of this thermocouple is from approximately –200°C to approximately 1200°C, as can be seen in *Figure 8*. This covers the generally used temperature ranges.

Over the main part of the range the behavior is linear. This is important for converting the analog signal to a digital signal.

The K-type thermocouple has good sensitivity when compared to many other types; the sensitivity is 41 uV/°C. Lower sensitivity requires more gain and makes the application more sensitive to noise.

In addition, a K-type thermocouple is not expensive, many other thermocouples consist of more expensive materials or are more difficult to produce.

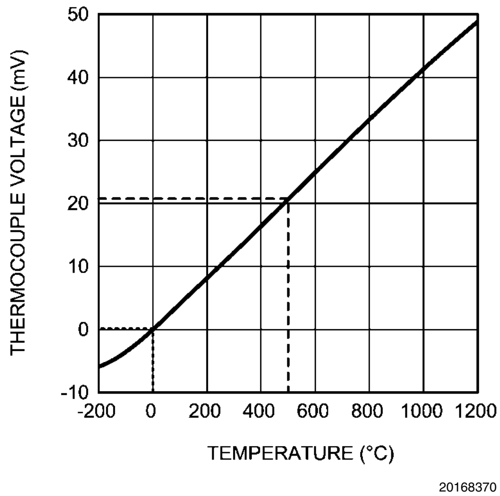


FIGURE 8. K-Type Thermocouple Response

Thermocouple Example

For this example suppose the range of interest is from 0°C to 500°C, and the resolution needed is 0.5°C. The power supply for both the LMV841, LMV842, or LMV844 and the ADC is 3.3V.

The temperature range of 0°C to 500°C results in a voltage range from 0 mV to 20.6 mV produced by the thermocouple. This is shown in *Figure 8*

To obtain the best accuracy the full ADC range of 0 to 3.3V is used and the gain needed for this full range can be calculated as follows: A_V = 3.3V/0.0206V = 160.

If R_G is 2 kΩ, then the value for R_F can be calculated with this gain of 160. Since $A_V = R_F/R_G$, R_F can be calculated as follow: $R_F = A_V * R_G$ = 160 x 2 kΩ = 320 kΩ.

To get a resolution of 0.5°C a step smaller then the minimum resolution is needed. This means that at least 1000 steps are necessary (500°C/0.5°C). A 10-bit ADC would be sufficient as this will give 1024 steps. A 10-bit ADC such as the two channel 10-bit ADC102S021 would be a good choice.

Unwanted Thermocouple Effect

At the point where the thermocouple wires are connected to the circuit, usually copper wires or traces, an unwanted thermocouple effect will occur.

At this connection, this could be the connector on a PCB, the thermocouple wiring forms a second thermocouple with the connector. This second thermocouple disturbs the measurements from the intended thermocouple.

Using an isothermal block as a reference will compensate for this additional thermocouple effect . An isothermal block is a good heat conductor. This means that the two thermocouple connections both have the same temperature. The temperature of the isothermal block can be measured, and thereby the temperature of the thermocouple connections. This is usually called the cold junction reference temperature.

In the example, an LM35 is used to measure this temperature. This semiconductor temperature sensor can accurately measure temperatures from –55°C to 150°C.

The ADC in this example also coverts the signal from the LM35 to a digital signal. Now the microprocessor can compensate the amplified thermocouple signal, for the unwanted thermocouple effect.

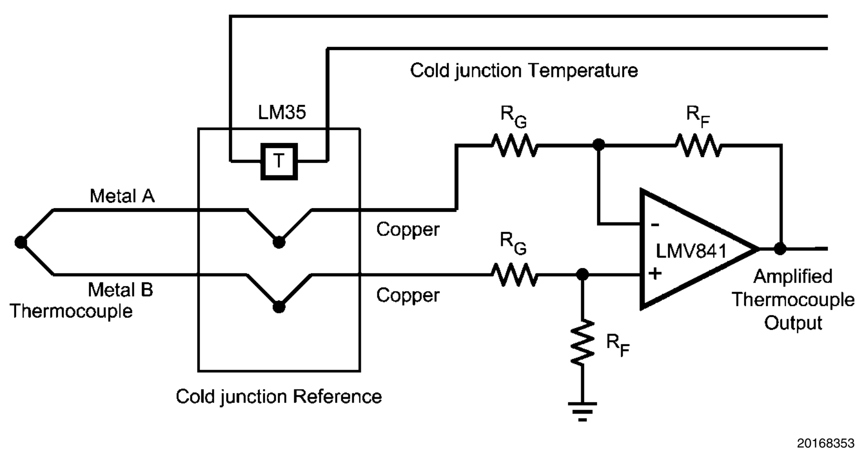
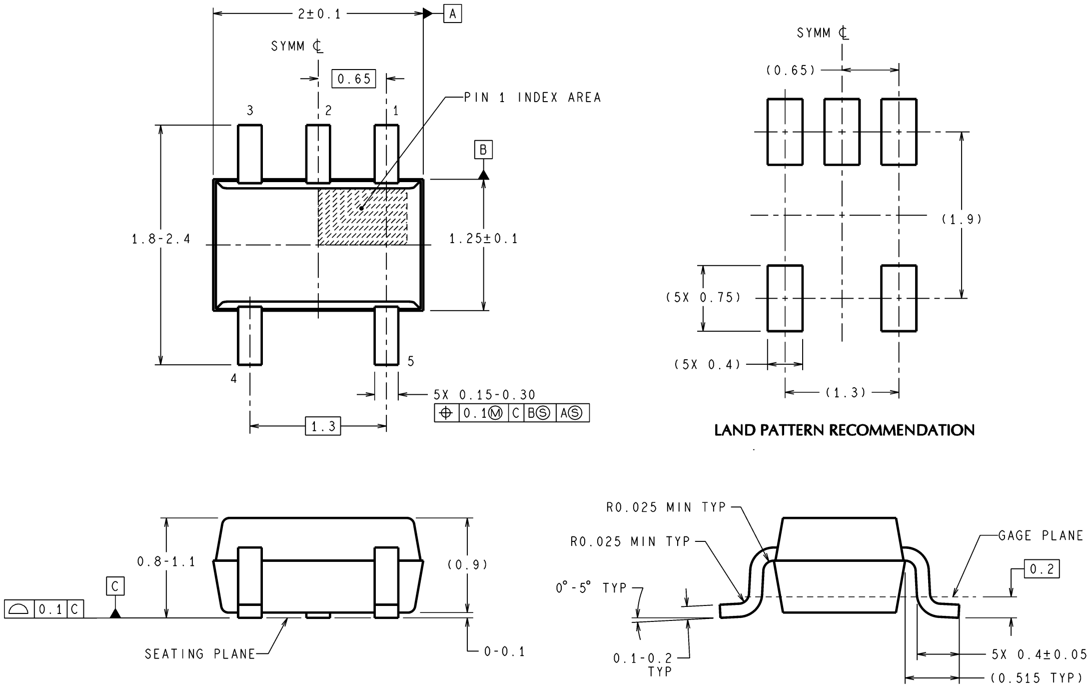


FIGURE 9. Thermocouple Amplifier

Physical Dimensions inches (millimeters) unless otherwise noted



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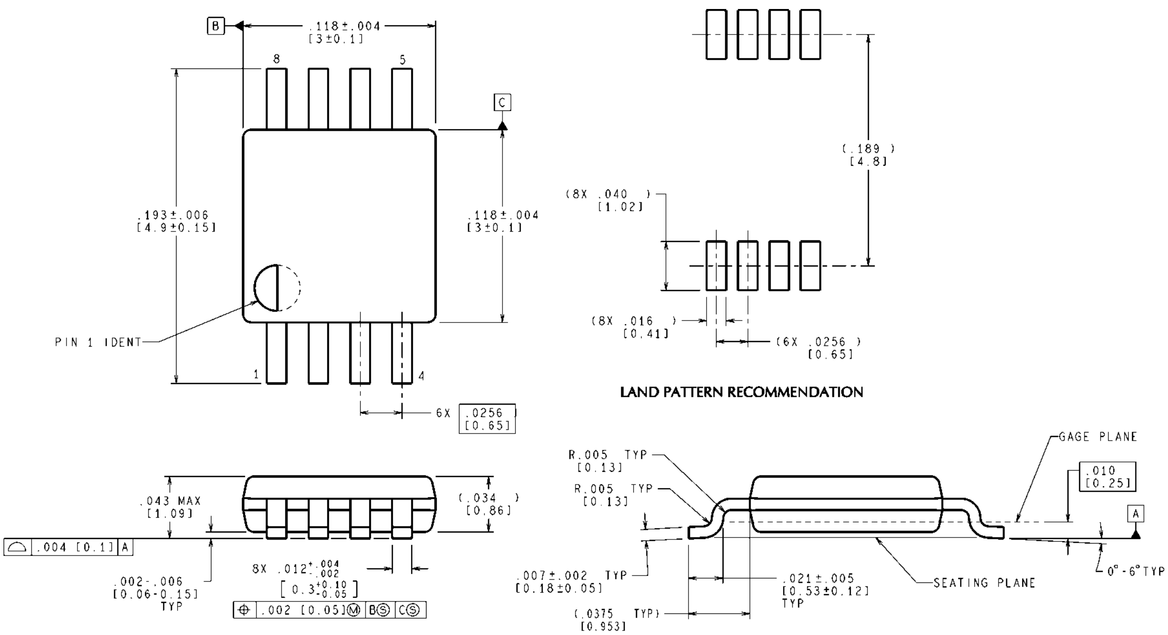
MAA05A (Rev D)

5-Pin SC70
NS Package Number MAA05A



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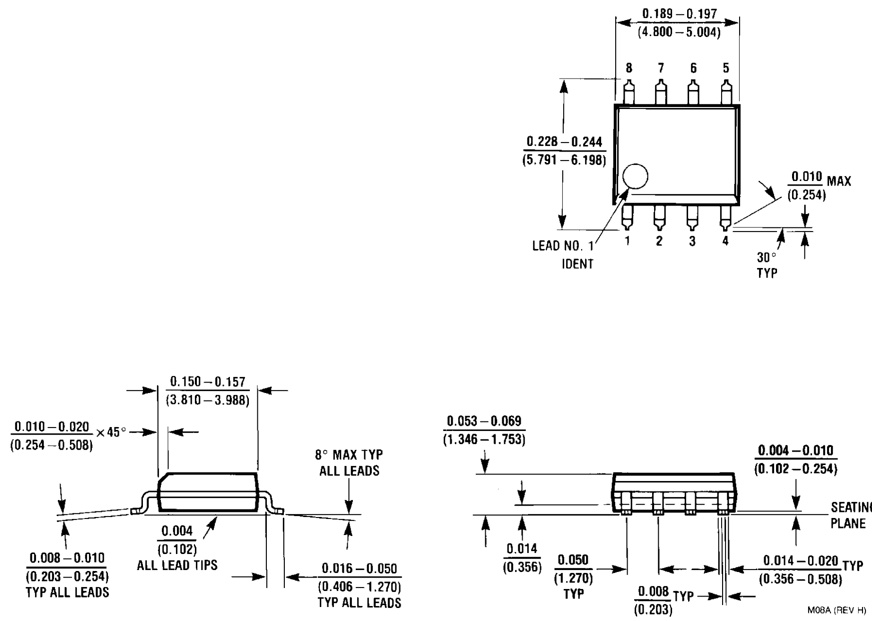
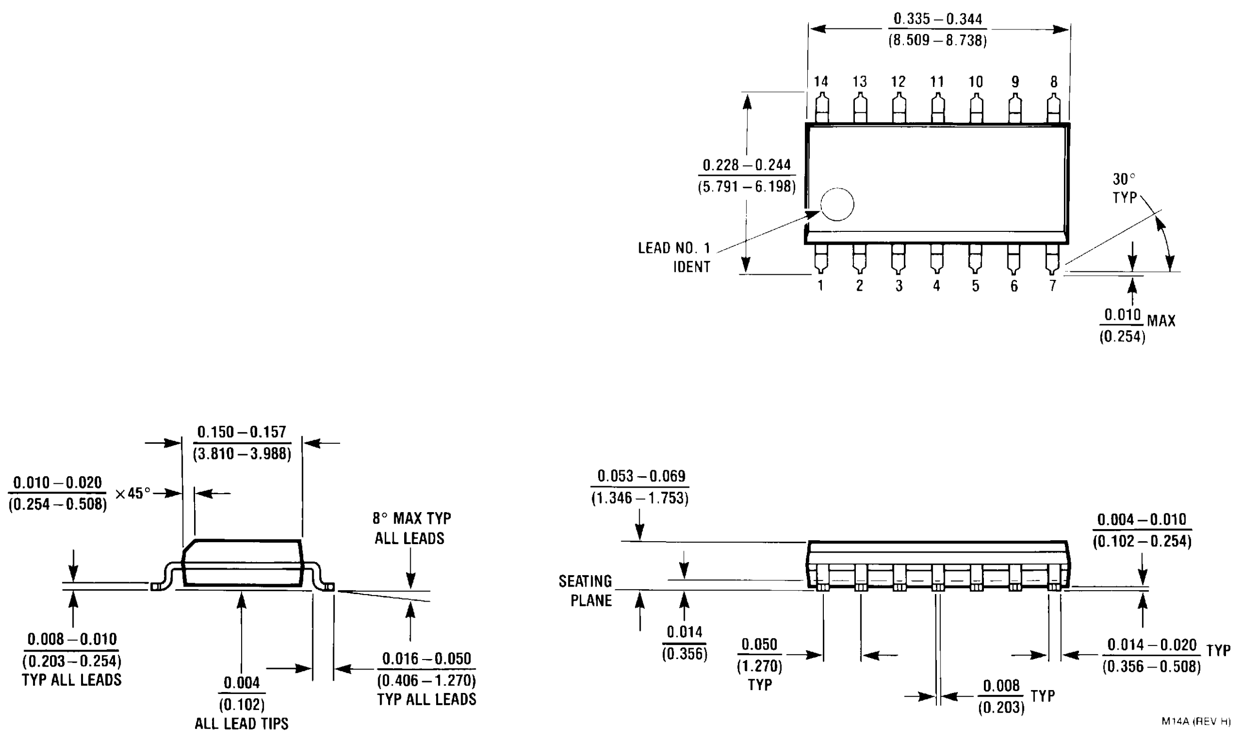
MUA08A (Rev E)

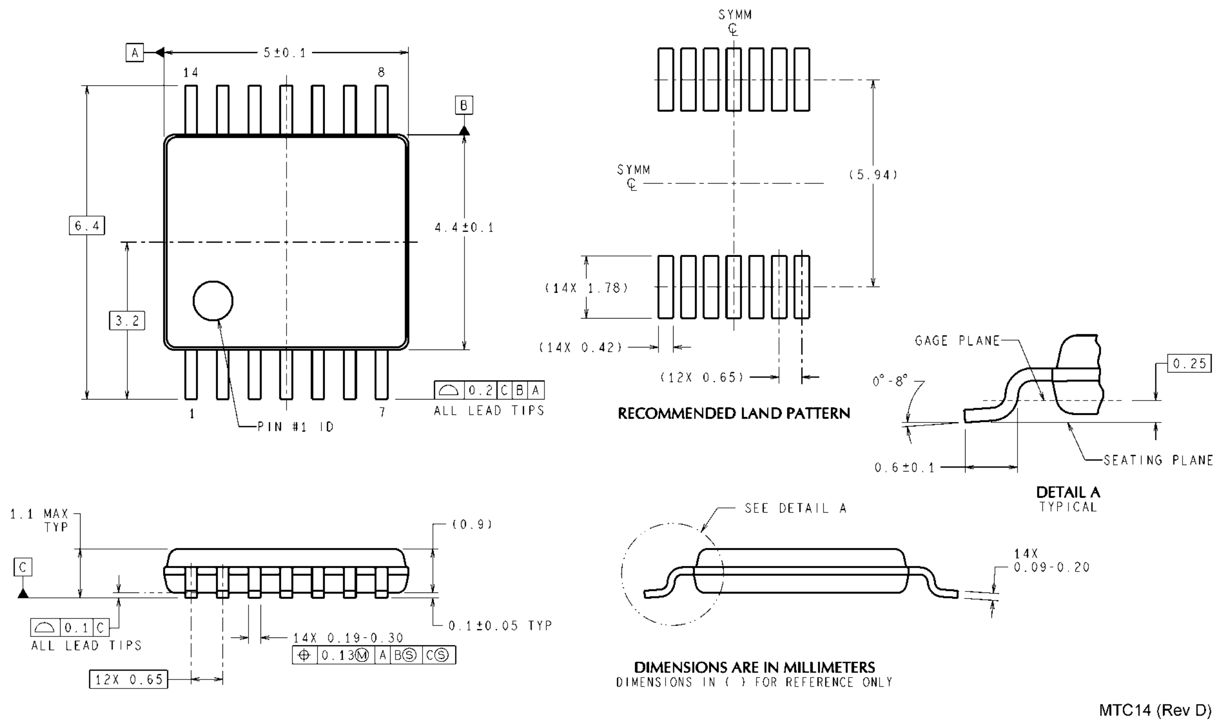
8-Pin MSOP
NS Package Number MUA08A



8-Pin SOIC
NS Package Number M08A



14-Pin SOIC
NS Package Number M14A



14-Pin TSSOP
NS Package Number MTC14

Notes

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