

TOSHIBA CMOS Linear Integrated Circuit Silicon Monolithic

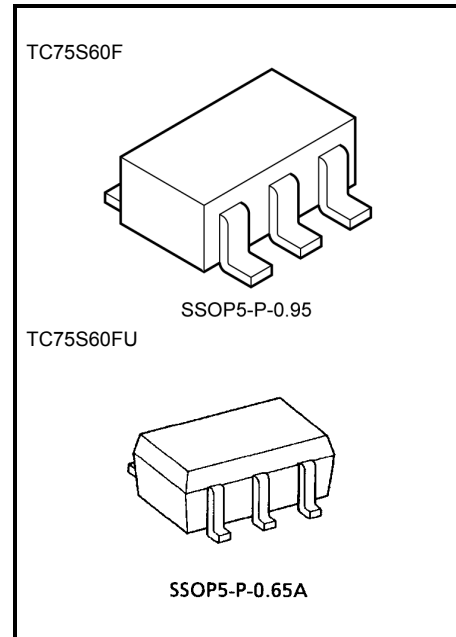
TC75S60F, TC75S60FU

Single Operational Amplifier

TC75S60F, TC75S60FU are CMOS operational amplifier with low supply voltage, low supply current.

Features

- High slew rate: SR ($V_{DD} = 3\text{ V}$) = 5.1 V/ μs (typ.)
- The power supply operation range is:
 $V_{DD} = \pm 0.9\sim 3.5\text{ V}$ or $1.8\sim 7\text{ V}$
- Low supply current: I_{DD} ($V_{DD} = 3\text{ V}$) = 330 μA (typ.)
- The internally phase compensated operational amplifier.
- Small package



Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

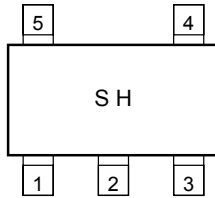
Characteristics	Symbol	Rating	Unit
Supply voltage	V_{DD}, V_{SS}	7	V
Differential input voltage	DV_{IN}	± 7	V
Input voltage	V_{IN}	$V_{DD}\sim V_{SS}$	V
Power dissipation	P_D	200	mW
Operating temperature	T_{opr}	$-40\sim 85$	$^\circ\text{C}$
Storage temperature	T_{stg}	$-55\sim 125$	$^\circ\text{C}$

Weight
 SSOP5-P-0.95 : 0.014 g (typ.)
 SSOP5-P-0.65A : 0.006 g (typ.)

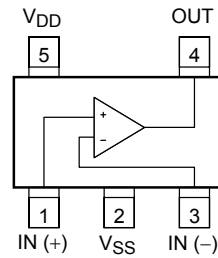
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Marking (top view)



Pin Connection (top view)



Electrical Characteristics

DC Characteristics ($V_{DD} = 3.0\text{ V}$, $V_{SS} = \text{GND}$, $T_a = 25^\circ\text{C}$)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input offset voltage	V_{IO}	1	$R_S = 1\text{ k}\Omega$	—	2	7	mV
Input offset current	I_{IO}	—	—	—	1	—	μA
Input bias current	I_I	—	—	—	1	—	μA
Common mode input voltage	CMV_{IN}	2	—	0.0	—	2.1	V
Voltage gain (open loop)	G_V	—	—	60	70	—	dB
Maximum output voltage	V_{OH}	3	$R_L = 100\text{ k}\Omega$	2.9	—	—	V
	V_{OL}	4	$R_L = 100\text{ k}\Omega$	—	—	0.1	
Common mode rejection ratio	CMRR	2	$V_{IN} = 0.0\sim 2.1\text{ V}$	54	70	—	dB
Supply voltage rejection ratio	SVRR	1	$V_{DD} = 1.8\sim 7.0\text{ V}$	60	70	—	dB
Supply current	I_{DD}	5	—	—	330	500	μA
Source current	I_{source}	6	—	330	700	—	μA
Sink current	I_{sink}	7	—	600	1250	—	μA

DC Characteristics ($V_{DD} = 1.8\text{ V}$, $V_{SS} = \text{GND}$, $T_a = 25^\circ\text{C}$)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input offset voltage	V_{IO}	1	$R_S = 10\text{ k}\Omega$	—	2	7	mV
Input offset current	I_{IO}	—	—	—	1	—	μA
Input bias current	I_I	—	—	—	1	—	μA
Common mode input voltage	CMV_{IN}	2	—	0.3	—	0.9	V
Voltage gain (open loop)	G_V	—	—	—	70	—	dB
maximum output voltage	V_{OH}	3	$R_L = 100\text{ k}\Omega$	1.7	—	—	V
	V_{OL}	4	$R_L = 100\text{ k}\Omega$	—	—	0.1	
Common mode rejection ratio	CMRR	2	$V_{IN} = 0.3\sim 0.9\text{ V}$	50	60	—	dB
Supply current	I_{DD}	5	—	—	300	450	μA
Source current	I_{source}	6	—	300	600	—	μA
Sink current	I_{sink}	7	—	550	1150	—	μA

AC Characteristics ($V_{DD} = 3.0\text{ V}$, $V_{SS} = \text{GND}$, $T_a = 25^\circ\text{C}$)

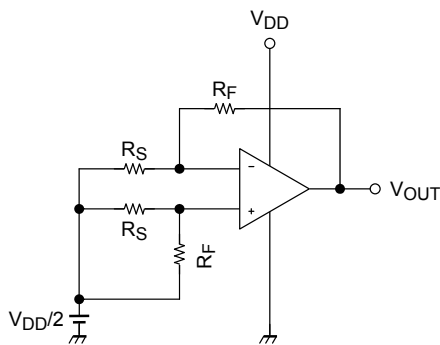
Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Slew rate	SR	—	—	—	5.1	—	V/ μs
Unity gain cross frequency	f_T	—	—	—	3.7	—	MHz

AC Characteristics ($V_{DD} = 1.8\text{ V}$, $V_{SS} = \text{GND}$, $T_a = 25^\circ\text{C}$)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Slew rate	SR	—	—	—	4.0	—	V/ μs
Unity gain cross frequency	f_T	—	—	—	3.0	—	MHz

Test Circuit

1. SVRR, V_{IO}



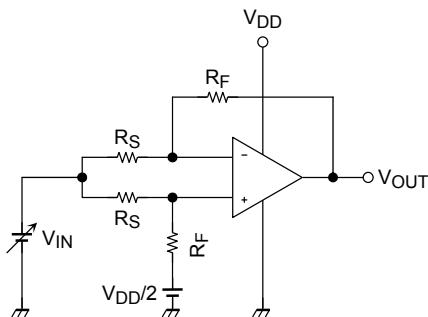
- SVRR
 $V_{DD} = 1.8\text{ V}$: $V_{DD} = V_{DD1}$, $V_{OUT} = V_{OUT1}$
 $V_{DD} = 7.0\text{ V}$: $V_{DD} = V_{DD2}$, $V_{OUT} = V_{OUT2}$

$$SVRR = 20 \log \left(\left| \frac{V_{OUT1} - V_{OUT2}}{V_{DD1} - V_{DD2}} \right| \times \frac{R_S}{R_F + R_S} \right)$$

- V_{IO}

$$V_{IO} = \left(V_{OUT} - \frac{V_{DD}}{2} \right) \times \frac{R_S}{R_F + R_S}$$

2. CMRR, CMV_{IN}

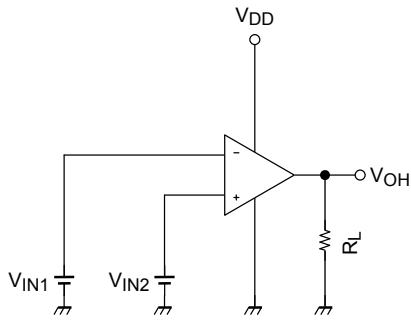


- CMRR
 $V_{IN} = 0.0\text{ V}$: $V_{IN} = V_{IN1}$, $V_{OUT} = V_{OUT1}$
 $V_{IN} = 2.1\text{ V}$: $V_{IN} = V_{IN2}$, $V_{OUT} = V_{OUT2}$

$$CMRR = 20 \log \left(\left| \frac{V_{OUT1} - V_{OUT2}}{V_{IN1} - V_{IN2}} \right| \times \frac{R_S}{R_F + R_S} \right)$$

- CMV_{IN}

3. V_{OH}

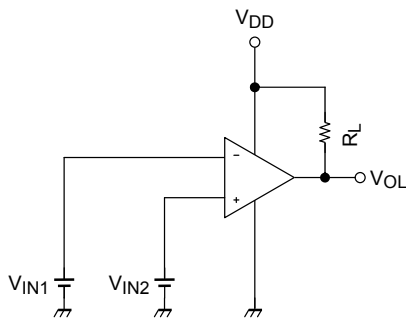


- V_{OH}

$$V_{IN1} = \frac{V_{DD}}{2} - 0.05 \text{ V}$$

$$V_{IN2} = \frac{V_{DD}}{2} + 0.05 \text{ V}$$

4. V_{OL}

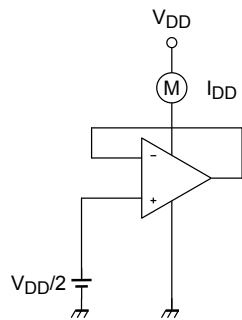


- V_{OL}

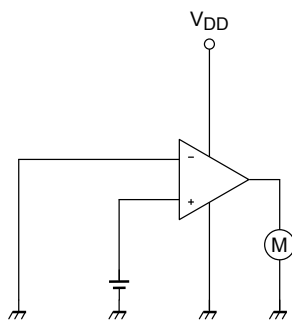
$$V_{IN1} = \frac{V_{DD}}{2} + 0.05 \text{ V}$$

$$V_{IN2} = \frac{V_{DD}}{2} - 0.05 \text{ V}$$

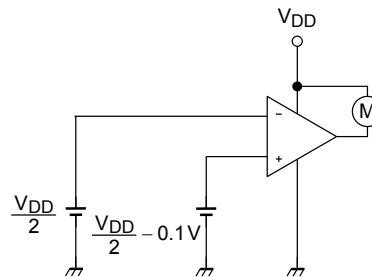
5. I_{DD}

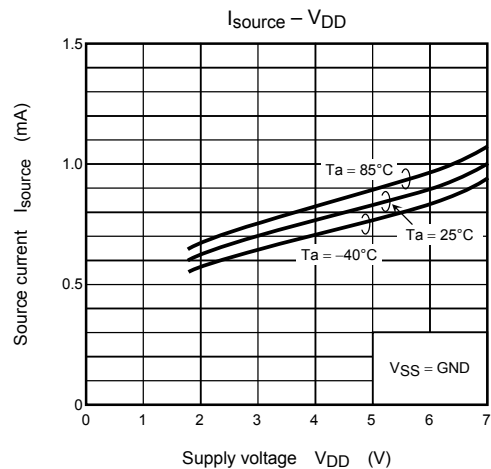
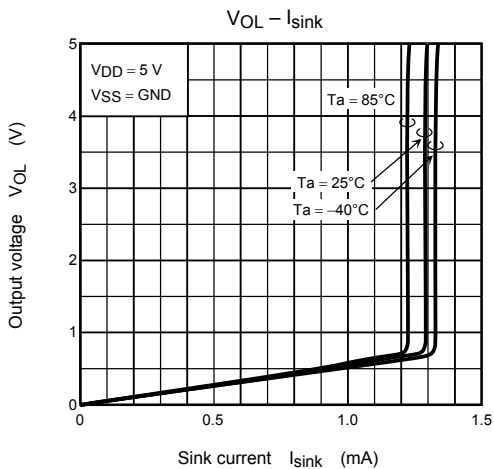
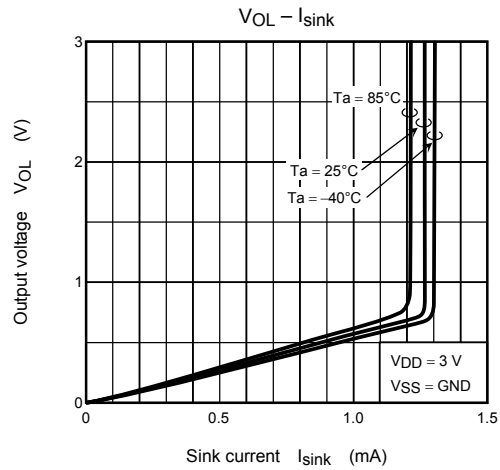
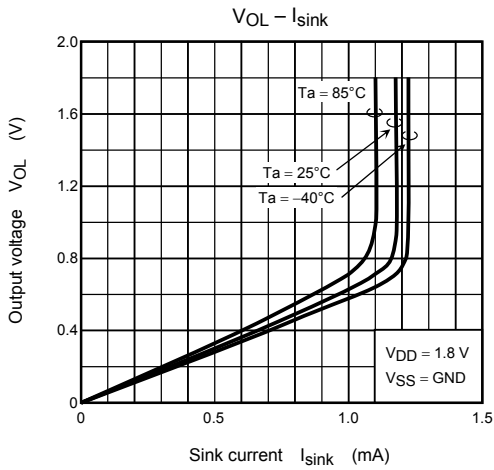
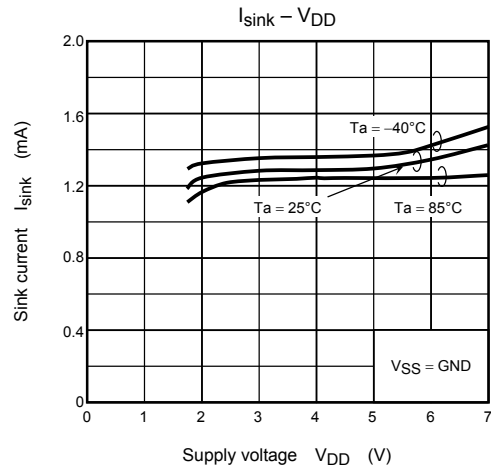
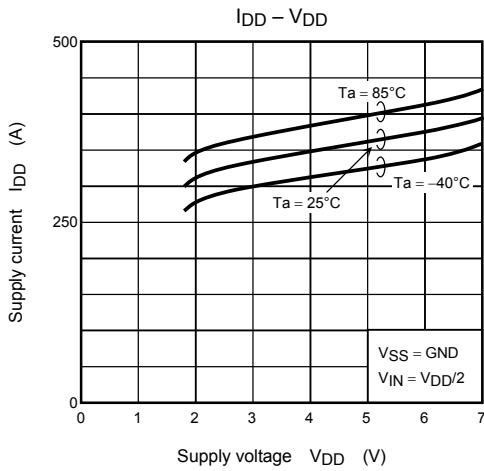


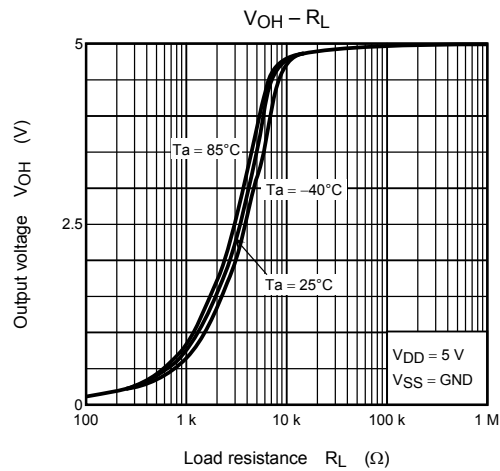
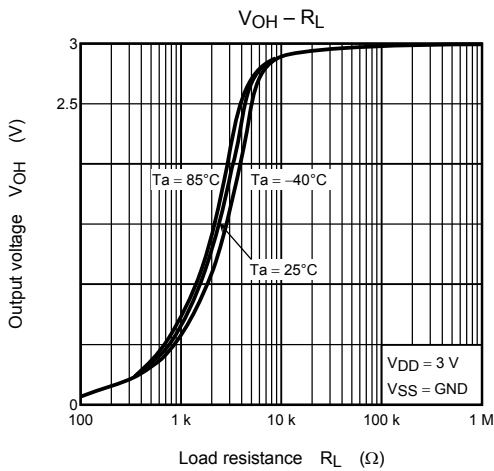
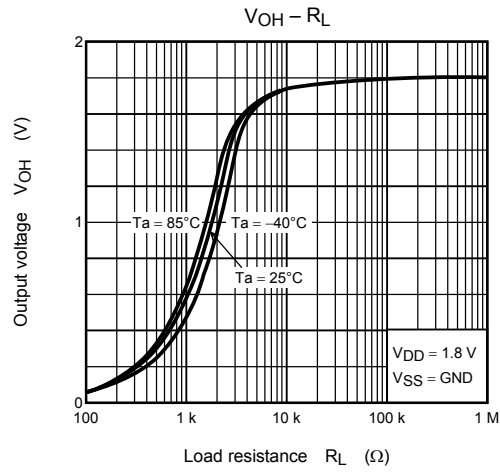
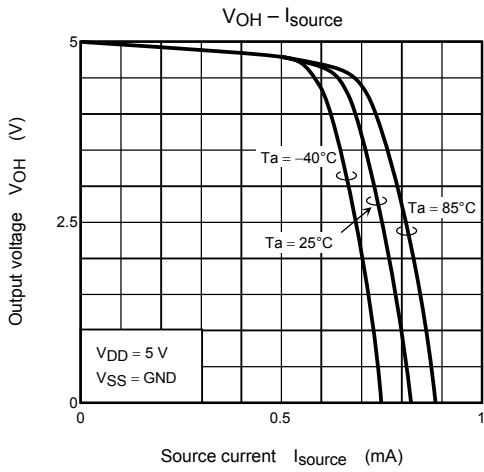
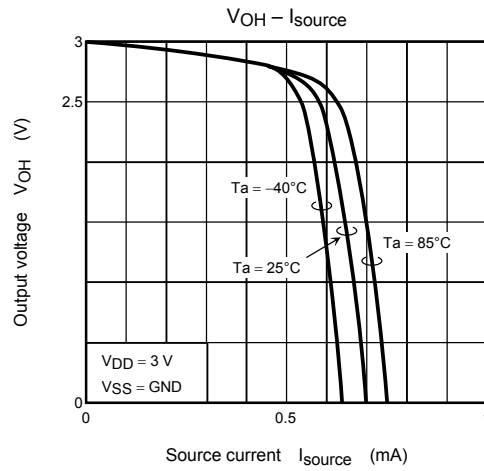
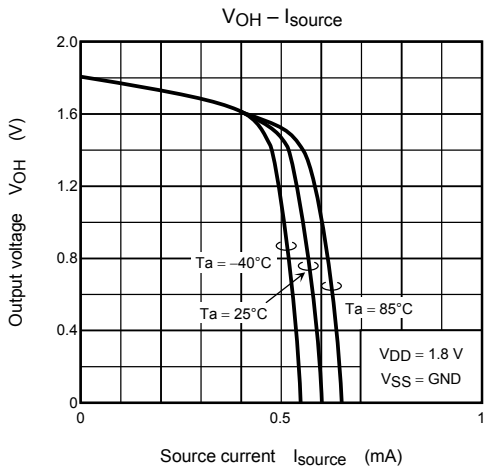
6. I_{source}

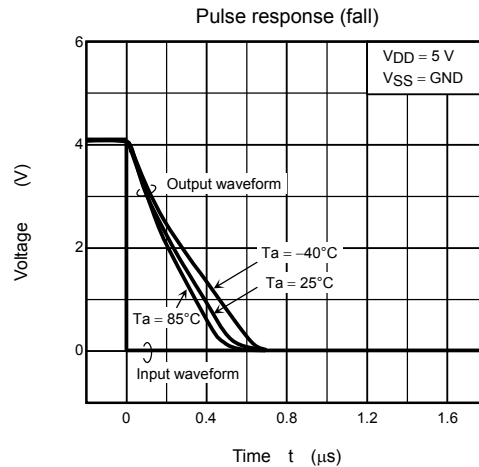
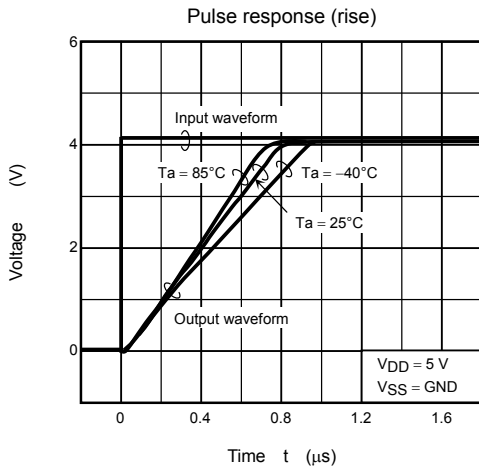
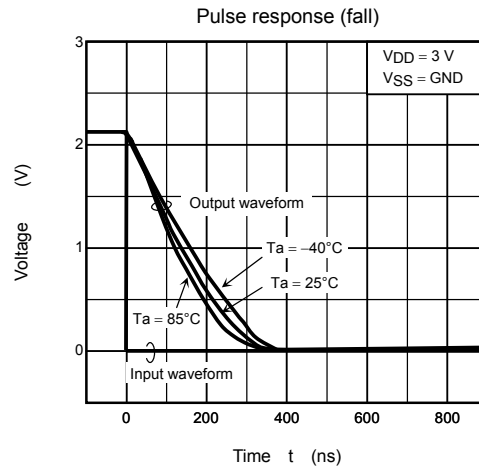
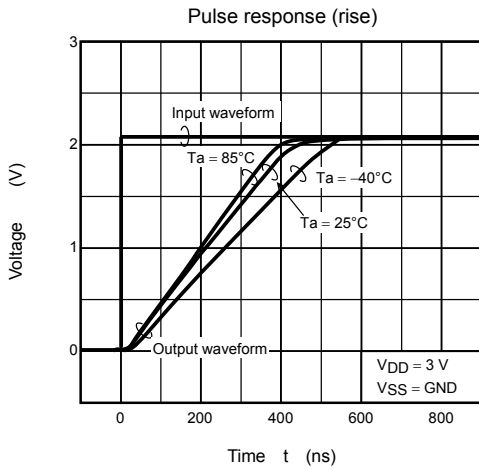
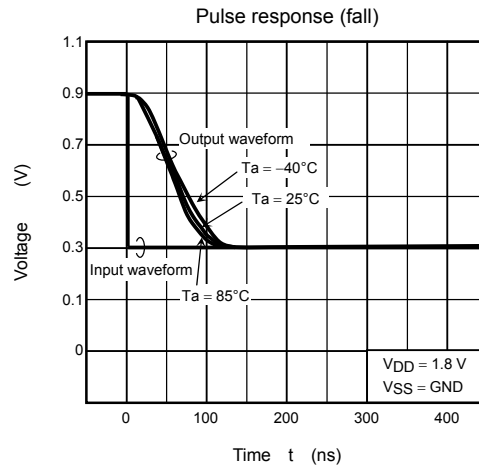
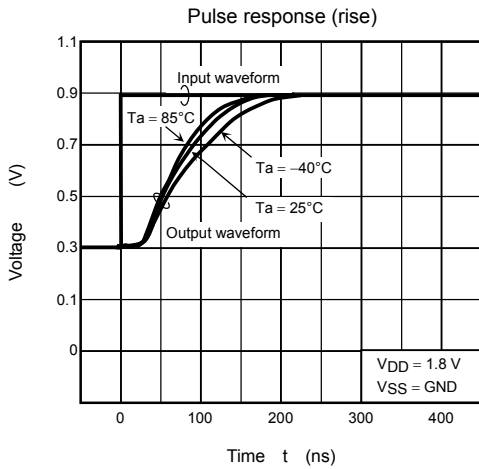


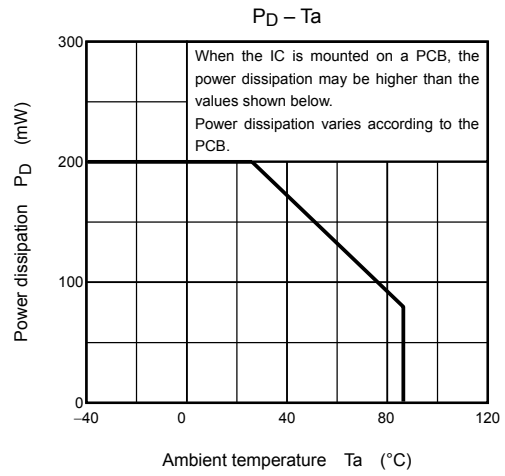
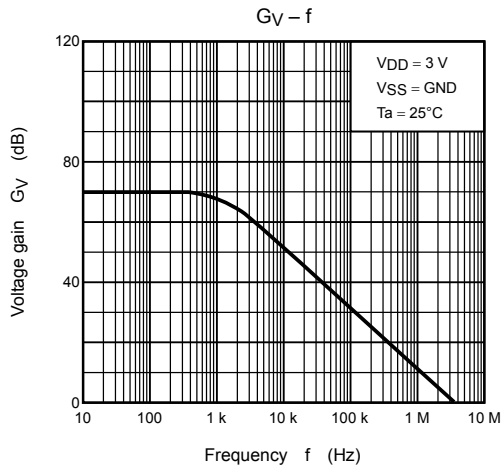
7. I_{sink}







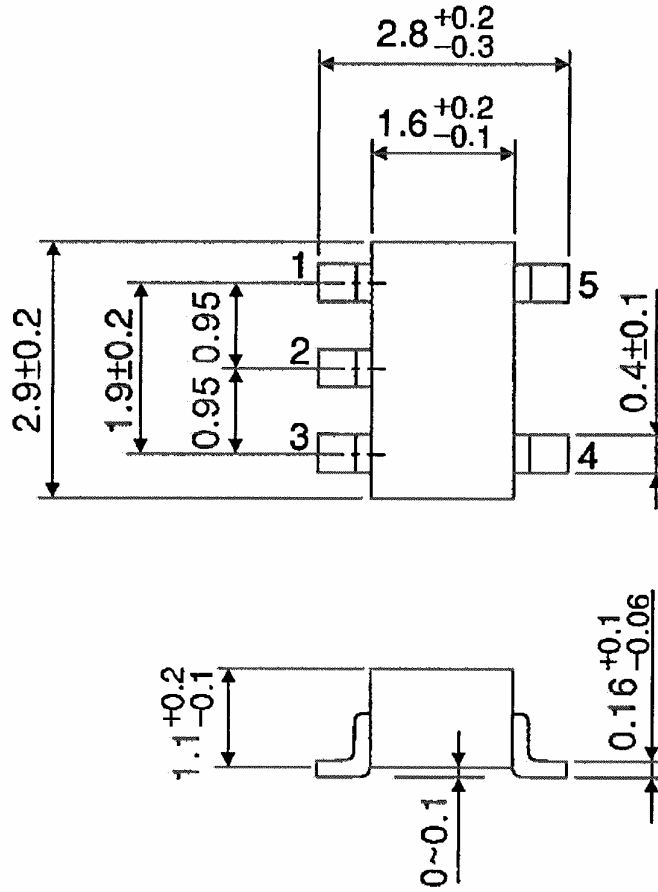




Package Dimensions

SSOP5-P-0.95

Unit : mm

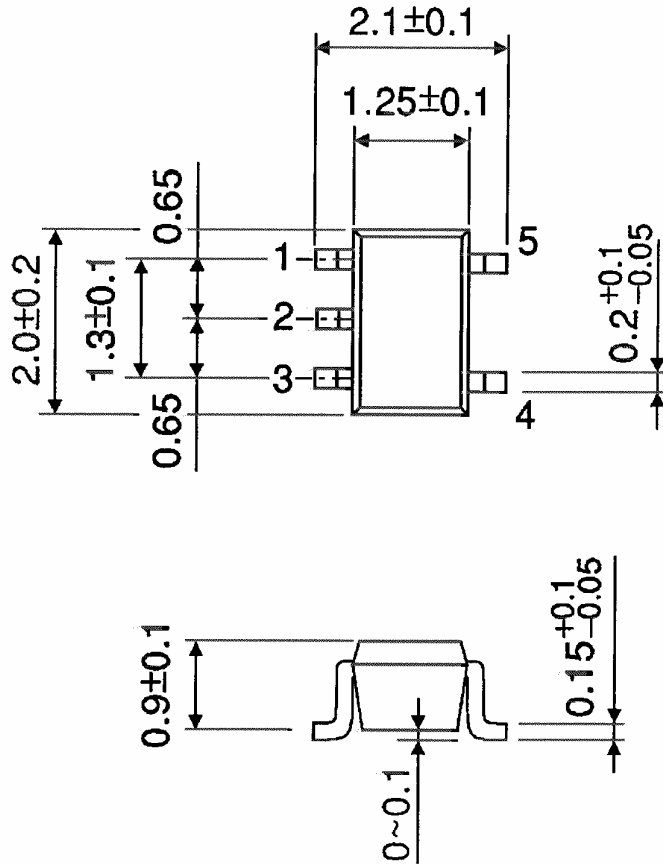


Weight: 0.014 g (typ.)

Package Dimensions

SSOP5-P-0.65A

Unit : mm



Weight: 0.006 g (typ.)

RESTRICTIONS ON PRODUCT USE

20070701-EN GENERAL

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