TSH80-TSH81-TSH82

Wide band rail-to-rail operational amplifier with standby function

Features

- Operating range from 4.5V to 12V
- 3dB-bandwidth: 100MHz
- Slew-rate 100V/µs
- Output current up to 55mA
- Input single supply voltage
- Output rail-to-rail
- Specified for 150Ω load
- Low distortion, THD 0.1%
- SOT23-5, TSSOP and SO packages

Applications

- Video buffers
- A/D converters driver
- Hi-fi applications

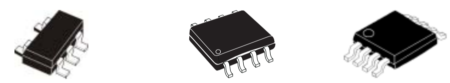
Description

The TSH8x series offers single and dual operational amplifiers featuring high video performance with large bandwidth, low distortion and excellent supply voltage rejection. These amplifiers also feature large output voltage swing and high output current capability to drive standard 150Ω loads.

Running at single or dual supply voltage from 4.5V to 12V, these amplifiers are tested at 5V (±2.5V) and 10V (±5V) supplies.

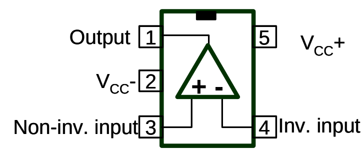
The TSH81 also features a standby mode, which allows the operational amplifier to be put into a standby mode with low power consumption and high output impedance. This function allows power saving or signal switching/multiplexing for high-speed applications and video applications.

For board space and weight saving, the TSH8x series is proposed in SOT23-5, TSSOP8 and SO-8 plastic micropackages.

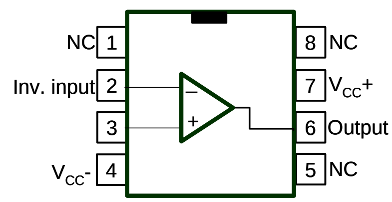


SOT23-5 SO-8 TSSOP8

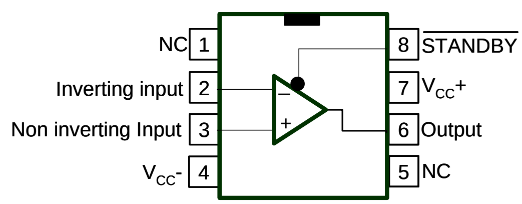
Pin connections TSH80/SOT23-5



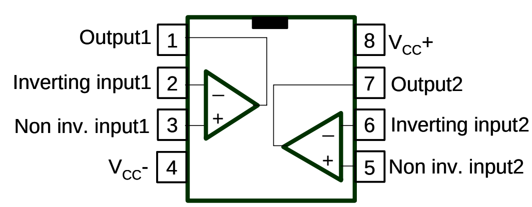
Pin connections TSH80/SO-8



Pin connections TSH81 SO-8/TSSOP8



Pin connections TSH82 SO-8/TSSOP8



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1 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1)	14	V
V_{id}	Differential input voltage (2)	±2	V
V_i	Input voltage (3)	±6	V
T_{oper}	Operating free air temperature range	-40 to +85	°C
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{thjc}	Thermal resistance junction to case (4) SOT23-5 SO8 TSSOPO8	 80 28 37	°C/W
R_{thja}	Thermal resistance junction to ambient area SOT23-5 SO8 TSSOPO8	 250 157 130	°C/W
ESD	Human body model (HBM)	2	kV

1. All voltage values, except differential voltage are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting terminal.
3. The magnitude of input and output must never exceed V_{CC} +0.3V.
4. Short-circuits can cause excessive heating.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	4.5 to 12	V
V_{IC}	Common mode input voltage range	V_{CC}^- to (V_{CC}^+ -1.1)	V
Standby (pin 8)	Threshold on pin 8 for TSH81	(V_{CC}^-) to (V_{CC}^+)	V

2 Electrical characteristics

Table 3. V_{CC}^+ = +5V, V_{CC}^- = GND, V_{ic} = 2.5V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$\|V_{io}\|$	Input offset voltage	T_{amb}= 25°C $T_{min} < T_{amb} < T_{max}$		1.1	10 12	mV
ΔV_{io}	Input offset voltage drift vs. temperature	$T_{min} < T_{amb} < T_{max}$		3		µV/°C
I_{io}	Input offset current	T_{amb}= 25°C $T_{min} < T_{amb} < T_{max}$		0.1	3.5 5	µA
I_{ib}	Input bias current	T_{amb}= 25°C $T_{min} < T_{amb} < T_{max}$		6	15 20	µA
C_{in}	Input capacitance			0.3		pF
I_{CC}	Supply current per operator	T_{amb}= 25°C $T_{min} < T_{amb} < T_{max}$		8.2	10.5 11.5	mA
CMR	Common mode rejection ratio ($\delta V_{ic}/\delta V_{io}$)	+0.1<V_{ic}<3.9V and V_{out}=2.5V T_{amb}= 25°C $T_{min} < T_{amb} < T_{max}$	 72 70	 97		dB
SVR	Supply voltage rejection ratio ($\delta V_{CC}/\delta V_{io}$)	T_{amb}= 25°C $T_{min} < T_{amb} < T_{max}$	68 65	75		dB
PSR	Power supply rejection ratio ($\delta V_{CC}/\delta V_{out}$)	Positive & negative rail		75		dB
A_{vd}	Large signal voltage gain	R_L=150Ω connected to 1.5V and V_{out}=1V to 4V T_{amb}= 25°C $T_{min} < T_{amb} < T_{max}$	 75 70	 84		dB
I_o	|Source|	V_{id}=+1, V_{out} connected to 1.5V T_{amb}= 25°C $T_{min} < T_{amb} < T_{max}$	 35 28	 55		mA
	Sink	V_{id}=-1, V_{out} connected to 1.5V T_{amb}= 25°C $T_{min} < T_{amb} < T_{max}$	 33 28	 55		
V_{oh}	High level output voltage	T_{amb}= 25°C R_L = 150Ω connected to GND R_L = 600Ω connected to GND R_L = 2kΩ connected to GND R_L = 10kΩ connected to GND R_L = 150Ω connected to 2.5V R_L = 600Ω connected to 2.5V R_L = 2kΩ connected to 2.5V R_L = 10kΩ connected to 2.5V $T_{min} < T_{amb} < T_{max}$ R_L = 150Ω connected to GND R_L = 150Ω connected to 2.5V	 4.2 4.5 4.1 4.4	 4.36 4.85 4.90 4.93 4.66 4.90 4.92 4.93		V

Table 3. V_{CC}^{+} = +5V, V_{CC}^{-} = GND, V_{ic} = 2.5V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{ol}	Low level output voltage	T_{amb}= 25°C R_L = 150Ω connected to GND R_L = 600Ω connected to GND R_L = 2kΩ connected to GND R_L = 10kΩ connectedto GND R_L = 150Ω connected to 2.5V R_L = 600Ω connected to 2.5V R_L = 2kΩ connected to 2.5V R_L = 10kΩ connected to 2.5V $T_{min} < T_{amb} < T_{max}$ R_L = 150Ω connected to GND R_L = 150Ω connected to 2.5V		48 54 55 56 220 105 76 61	150 400 200 450	mV
GBP	Gain bandwidth product	F=10MHz A_{VCL}= +11 A_{VCL}= -10		65 55		MHz
Bw	Bandwidth @-3dB	A_{VCL}= +1 R_L= 150Ω connected to 2.5V		87		MHz
SR	Slew rate	A_{VCL}=+2 R_L=150Ω // C_L to 2.5V C_L = 5pF C_L = 30pF	 60	 104 105		V/µs
ϕm	Phase margin	R_L= 150Ω // 30pF to 2.5V		40		° (degree)
en	Equivalent input noise voltage	F= 100kHz		11		nV/√Hz
THD	Total harmonic distortion	A_{VCL}= +2, F= 4MHz R_L= 150Ω // 30pF to 2.5V V_{out}= $1V_{pp}$ V_{out}= $2V_{pp}$		-61 -54		dB
IM2	Second order intermodulation product	A_{VCL}= +2, V_{out}= $2V_{pp}$ R_L= 150Ω connected to 2.5V F_{in1}= 180kHz, F_{in2}= 280kHz spurious measurement @100kHz		-76		dBc
IM3	Third order intermodulation product	A_{VCL}= +2, V_{out}= $2V_{pp}$ R_L= 150Ω to 2.5V F_{in1}=180kHz, F_{in2}= 280kHz spurious measurement @400kHz		-68		dBc
ΔG	Differential gain	A_{VCL}=+2, R_L=150Ω to 2.5V F= 4.5MHz, V_{out}= $2V_{pp}$		0.5		%
Df	Differential phase	A_{VCL}= +2, R_L=150Ω to 2.5V F= 4.5MHz, V_{out}= $2V_{pp}$		0.5		° (degree)
Gf	Gain flatness	F= DC to 6MHz, A_{VCL}= +2		0.2		dB
Vo1/Vo2	Channel separation	F= 1MHz to 10MHz		65		dB

Table 4. $V_{CC}^+ = +5V$, $V_{CC}^- = -5V$, $V_{ic} = GND$, $T_{amb} = 25^\circ C$ (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$\|V_{io}\|$	Input offset voltage	T_{amb}= 25°C $T_{min} < T_{amb} < T_{max}$		0.8	10 12	mV
ΔV_{io}	Input offset voltage drift vs. temperature	$T_{min} < T_{amb} < T_{max}$		2		µV/°C
I_{io}	Input offset current	T_{amb}= 25°C $T_{min} < T_{amb} < T_{max}$		0.1	3.5 5	µA
I_{ib}	Input bias current	T_{amb}= 25°C $T_{min} < T_{amb} < T_{max}$		6	15 20	µA
C_{in}	Input capacitance			0.7		pF
I_{CC}	Supply current per operator	T_{amb}= 25°C $T_{min} < T_{amb} < T_{max}$		9.8	12.3 13.4	mA
CMR	Common mode rejection ratio ($\delta V_{ic}/\delta V_{io}$)	-4.9 < V_{ic} < 3.9V and V_{out}=GND T_{amb}= 25°C $T_{min} < T_{amb} < T_{max}$	81 72	106		dB
SVR	Supply voltage rejection ratio ($\delta V_{CC}/\delta V_{io}$)	T_{amb}= 25°C $T_{min} < T_{amb} < T_{max}$	71 65	77		dB
PSR	Power supply rejection ratio ($\delta V_{CC}/\delta V_{out}$)	Positive & negative rail		75		dB
A_{vd}	Large signal voltage gain	R_L=150Ω connected to GND V_{out}= -4 to +4 T_{amb}= 25°C $T_{min} < T_{amb} < T_{max}$	75 70	86		dB
I_o	|Source|	V_{id}=+1, V_{out} connected to 1.5V T_{amb}= 25°C $T_{min} < T_{amb} < T_{max}$	35 28	55		mA
	Sink	V_{id}=-1, V_{out} connected to 1.5V T_{amb}= 25°C $T_{min} < T_{amb} < T_{max}$	30 28	55		
V_{oh}	High level output voltage	T_{amb}= 25°C R_L = 150Ω connected to GND R_L = 600Ω connected to GND R_L = 2kΩ connected to GND R_L = 10kΩ connected to GND $T_{min} < T_{amb} < T_{max}$ R_L = 150Ω connected to GND	4.2 4.1	4.36 4.85 4.9 4.93		V
V_{ol}	Low level output voltage	T_{amb}= 25°C R_L = 150Ω connected to GND R_L = 600Ω connected to GND R_L = 2kΩ connected to GND R_L = 10kΩ connected to GND $T_{min} < T_{amb} < T_{max}$ R_L = 150Ω connected to GND		-4.63 -4.86 -4.9 -4.93	-4.4 -4.3	mV

Table 4. V_{CC}^+ = +5V, V_{CC}^- = -5V, V_{ic} = GND, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
GBP	Gain bandwidth product	F=10MHz A_{VCL}= +11 A_{VCL}= -10		 65 55		MHz
Bw	Bandwidth @-3dB	A_{VCL}= +1 R_L=150Ω // 30pF to GND		100		MHz
SR	Slew rate	A_{VCL}=+2 R_L=150Ω // C_L to GND C_L = 5pF C_L = 30pF	 68	 117 118		V/µs
ϕm	Phase margin	R_L= 150Ω connected to GND		40		° (degree)
en	Equivalent input noise voltage	F= 100kHz		11		nV/√Hz
THD	Total harmonic distortion	A_{VCL}= +2, F=4 MHz R_L=150Ω // 30pF to GND V_{out}= 1V_{pp} V_{out}= 2V_{pp}		 -61 -54		dB
IM2	Second order intermodulation product	A_{VCL}= +2, V_{out}= 2V_{pp} R_L= 150Ω to GND F_{in1}= 180kHz, F_{in2}= 280kHz spurious measurement @100kHz		-76		dBc
IM3	Third order intermodulation product	A_{VCL}= +2, V_{out}= 2V_{pp} R_L=150Ω to GND F_{in1}= 180kHz, F_{in2}= 280kHz spurious measurement @400kHz		-68		dBc
ΔG	Differential gain	A_{VCL}=+2, R_L=150Ω to GND F= 4.5MHz, V_{out}= 2V_{pp}		0.5		%
Df	Differential phase	A_{VCL}= +2, R_L= 150Ω to GND F= 4.5MHz, V_{out}= 2V_{pp}		0.5		° (degree)
Gf	Gain flatness	F=DC to 6MHz, A_{VCL}=+2		0.2		dB
Vo1/Vo2	Channel separation	F=1MHz to 10MHz		65		dB

Table 5. Standby mode - V_{CC}^+, V_{CC}^-, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{low}	Standby low level		V_{CC}^-		$(V_{CC}^- +0.8)$	V
V_{high}	Standby high level		$(V_{CC}^- +2)$		(V_{CC}^+)	V
$I_{CC-STBY}$	Current consumption per operator when Standby is active	pin 8 (TSH81) to V_{CC}^-		20	55	µA
Z_{out}	Output impedance (R_{out}//C_{out})	R_{out} C_{out}		10 17		MΩ pF
T_{on}	Time from Standby mode to Active mode			2		µs
T_{off}	Time from Active mode to Standby mode	Down to $I_{CC-STBY}$ = 10µA		10		µs

Table 6. TSH81 standby control pin 8 ($\overline{\text{STANDBY}}$)

TSH81 standby control pin 8 ($\overline{\text{STANDBY}}$)	Operator status
V_{low}	Standby
V_{high}	Active

Figure 1. Closed loop gain and phase vs. frequency

Gain=+2, V_{CC}= ±2.5V, R_L=150Ω, T_{amb} = 25°C

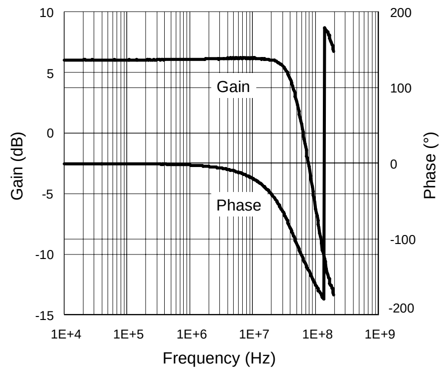


Figure 2. Overshoot vs. output capacitance

Gain=+2, V_{CC}= ±2.5V, T_{amb} = 25°C

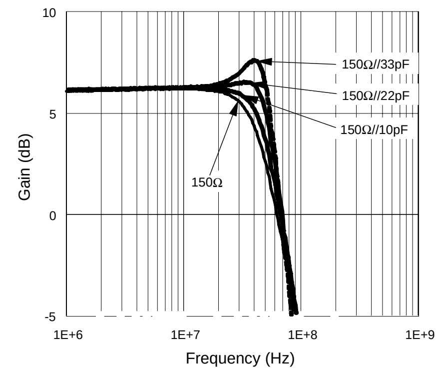


Figure 3. Closed loop gain and phase vs. frequency

Gain=-10, V_{CC}= ±2.5V, R_L=150Ω, T_{amb} = 25°C

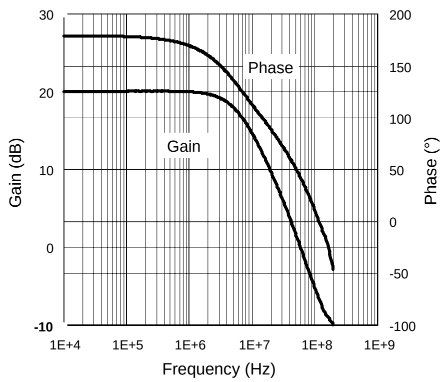


Figure 4. Closed loop gain and phase vs. frequency

Gain=+11, V_{CC}= ±2.5V, R_L=150Ω, T_{amb} = 25°C

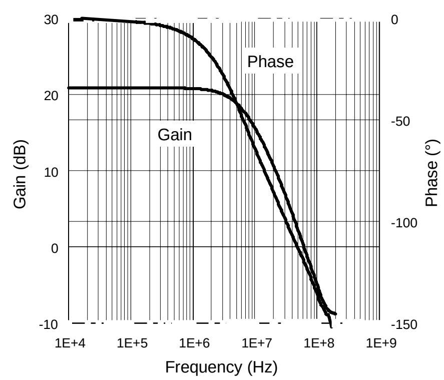


Figure 5. Large signal measurement - positive slew rate

Gain=2, V_{CC}=±2.5V, Z_L=150Ω//5.6pF, V_{in}=400mVpk

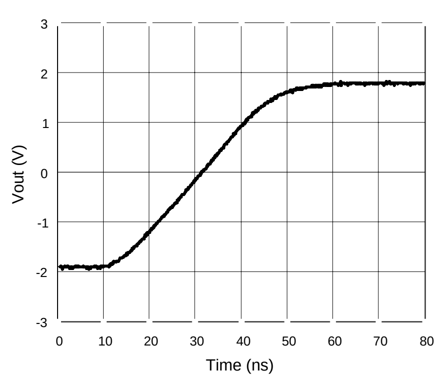


Figure 6. Large signal measurement - negative slew rate

Gain=2, V_{CC}=±2.5V, Z_L=150Ω//5.6pF, V_{in}=400mVpk

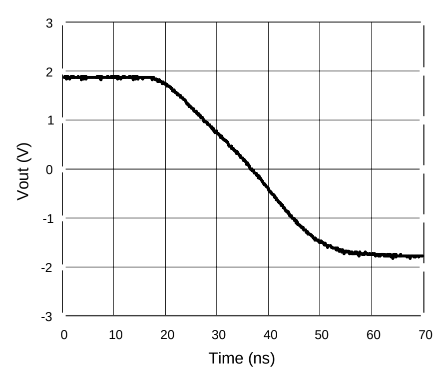


Figure 7. Small signal measurement - rise time

Gain=2, V_{CC}=±2.5V, R_L=150Ω, V_{in}=400mVpk

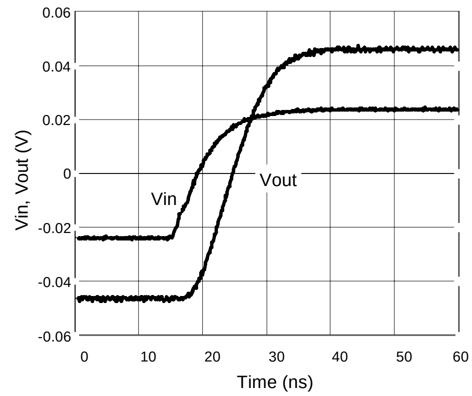


Figure 8. Small signal measurement - fall time

Gain=2, V_{CC}=±2.5V, R_L=150Ω, V_{in}=400mVpk

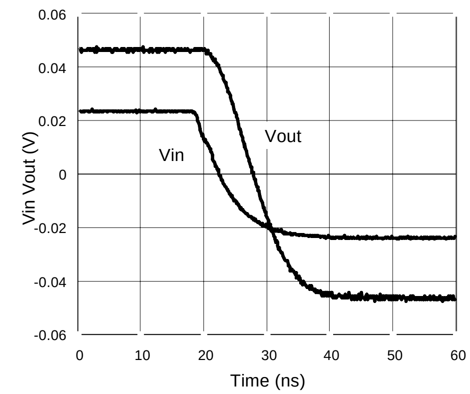


Figure 9. Channel separation (crosstalk) vs. frequency

Measurement configuration: crosstalk=20log(V0/V1)

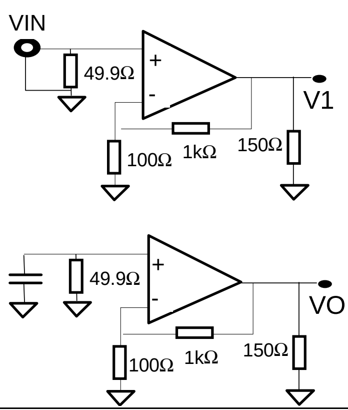


Figure 10. Channel separation (crosstalk) vs. frequency

Gain=+11, V_{CC}=±2.5V, Z_L=150Ω//27pF

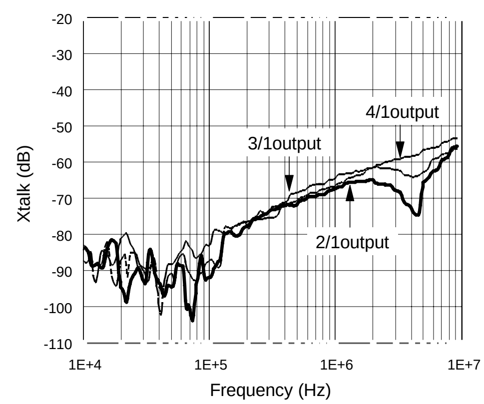


Figure 11. Equivalent input noise voltage

Gain=100, V_{CC}=±2.5V, no load

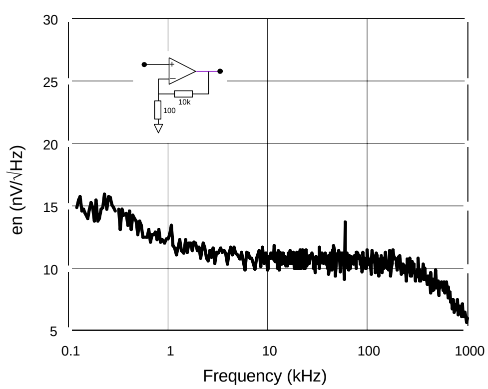


Figure 12. Maximum output swing

Gain=11, V_{CC}=±2.5V, R_L=150Ω

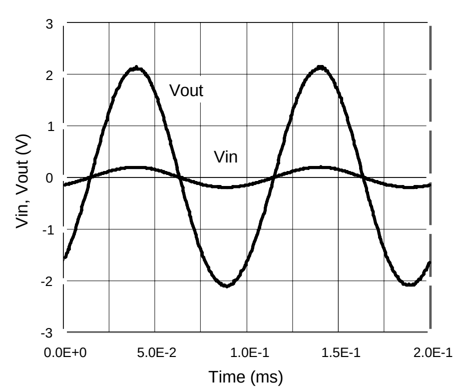


Figure 13. Standby mode - T_{on}, T_{off}

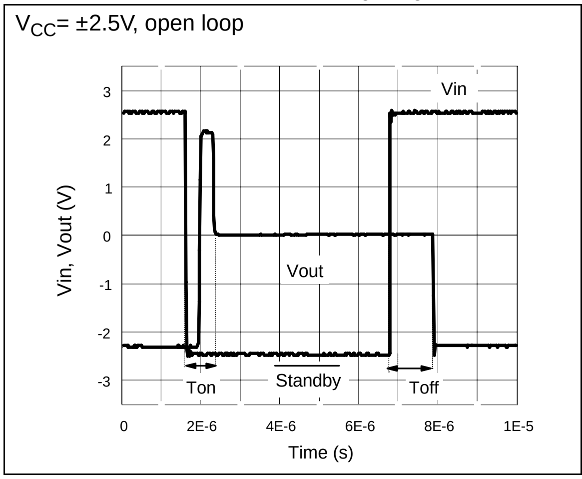
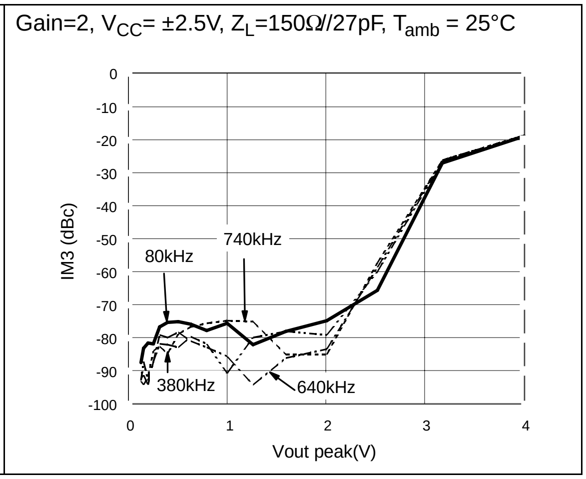


Figure 14. Third order intermodulation(1)



1. The IFR2026 synthesizer generates a two-tone signal (F1=180kHz, F2=280kHz), each tone having the same amplitude. The HP3585 spectrum analyzer measures the intermodulation products as a function of the output voltage. The generator and the spectrum analyzer are phase locked for better accuracy.

Figure 15. Group delay

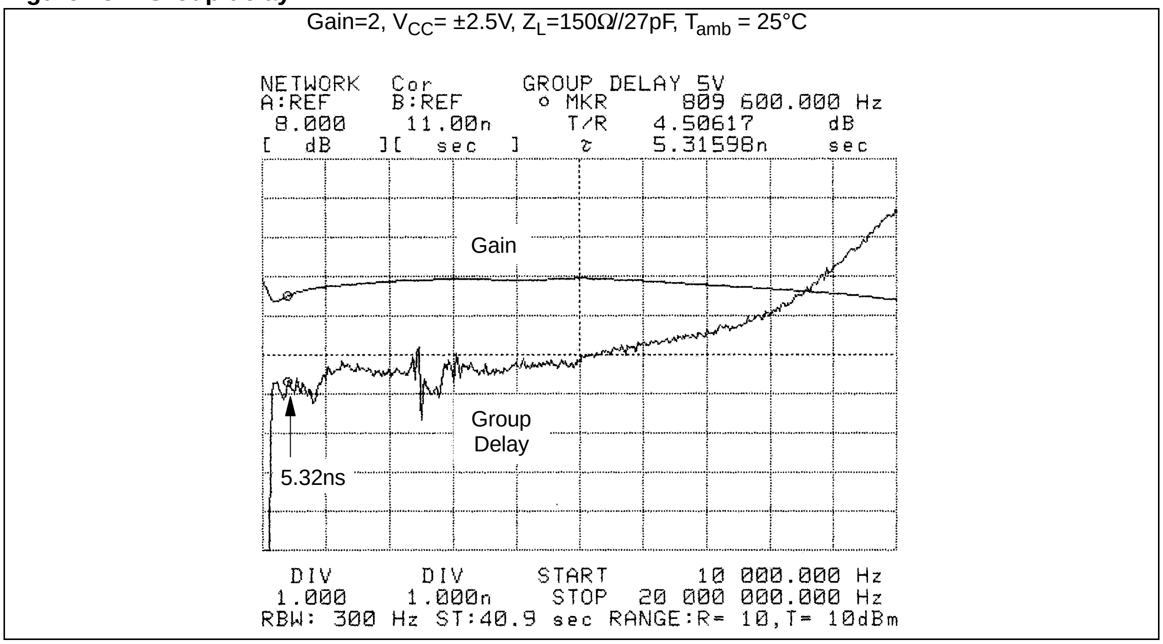


Figure 16. Closed loop gain and phase vs. frequency

Gain=+2, V_{CC}= ±5V, R_L=150Ω, T_{amb} = 25°C

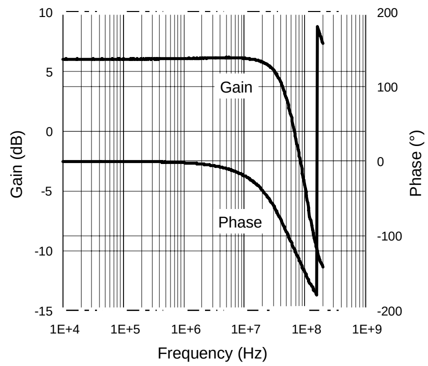


Figure 17. Overshoot vs. output capacitance

Gain=+2, V_{CC}= ±5V, T_{amb} = 25°C

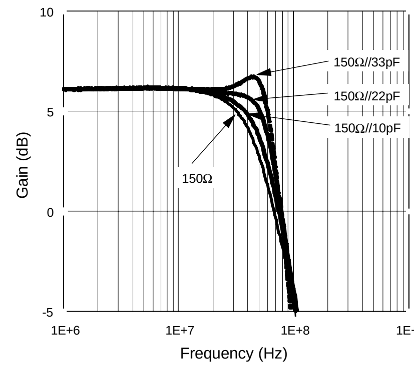


Figure 18. Closed loop gain and phase vs. frequency

Gain=-10, V_{CC}= ±5V, R_L=150Ω, T_{amb} = 25°C

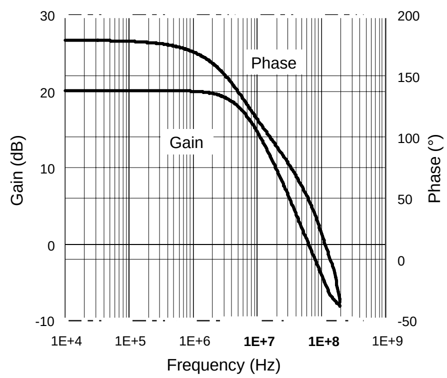


Figure 19. Closed loop gain and phase vs. frequency

Gain=+11, V_{CC}= ±5V, R_L=150Ω, T_{amb} = 25°C

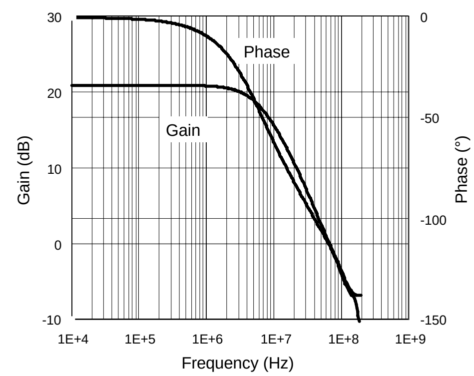


Figure 20. Large signal measurement - positive slew rate

Gain=2, V_{CC}=±5V, Z_L=150Ω//5.6pF, V_{in}=400mVpk

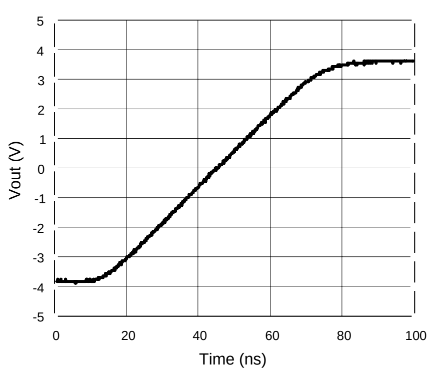


Figure 21. Large signal measurement - negative slew rate

Gain=2, V_{CC}=±5V, Z_L=150Ω//5.6pF, V_{in}=400mVpk

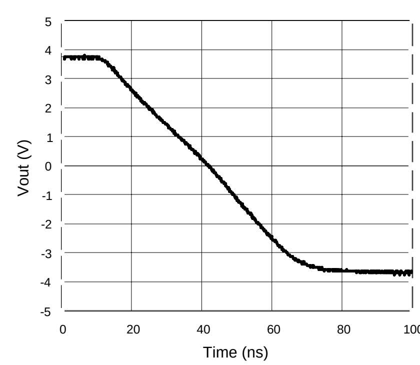


Figure 22. Small signal measurement - rise time

Gain=2, V_{CC}=±5V, R_L=150Ω, V_{in}=400mVpk

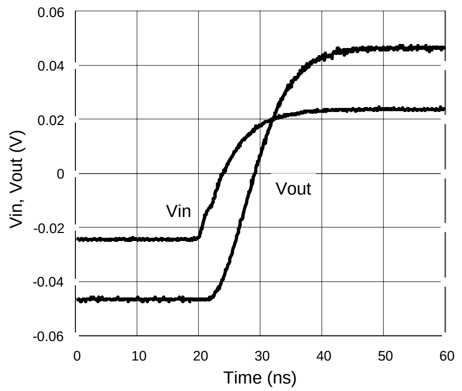


Figure 23. Small signal measurement - fall time

Gain=2, V_{CC}=±5V, R_L=150Ω, V_{in}=400mVpk

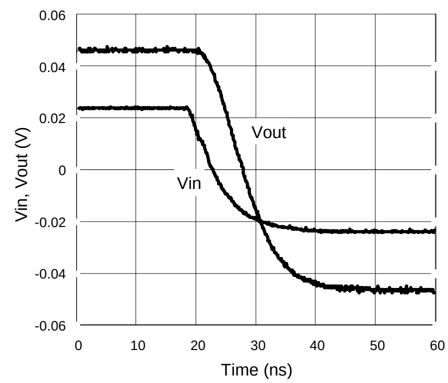


Figure 24. Channel separation (crosstalk) vs. frequency

Measurement configuration: crosstalk=20log(V0/V1)

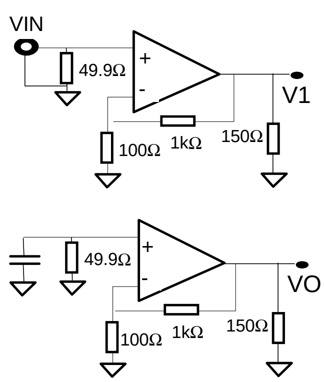


Figure 25. Channel separation (crosstalk) vs. frequency

Gain=+11, V_{CC}=±5V, Z_L=150Ω/ /27pF

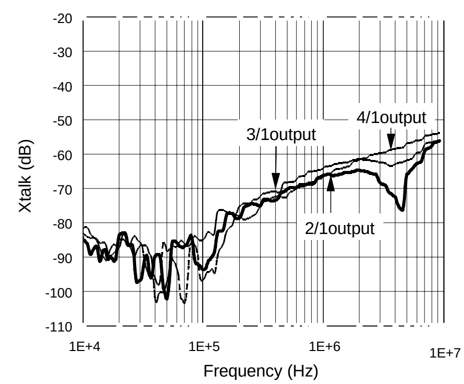


Figure 26. Equivalent input noise voltage

Gain=100, V_{CC}=±5V, no load

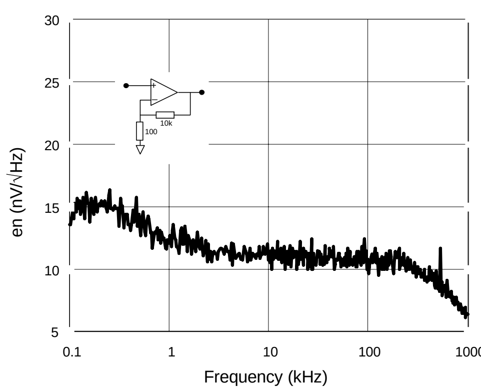


Figure 27. Maximum output swing

Gain=11, V_{CC}=±5V, R_L=150Ω

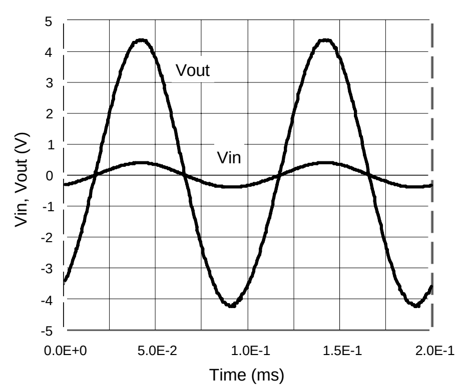


Figure 28. Standby mode - T_{on}, T_{off}

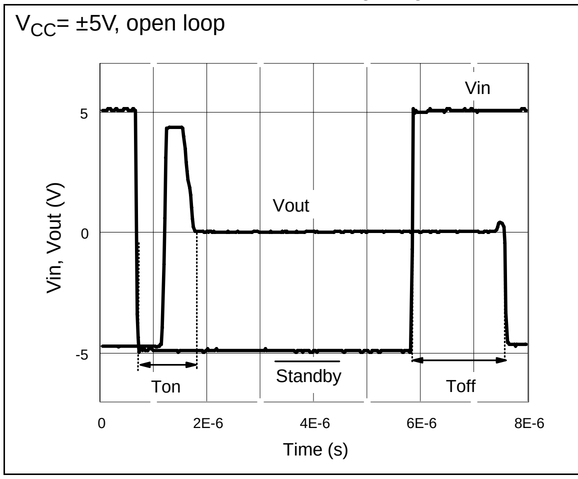
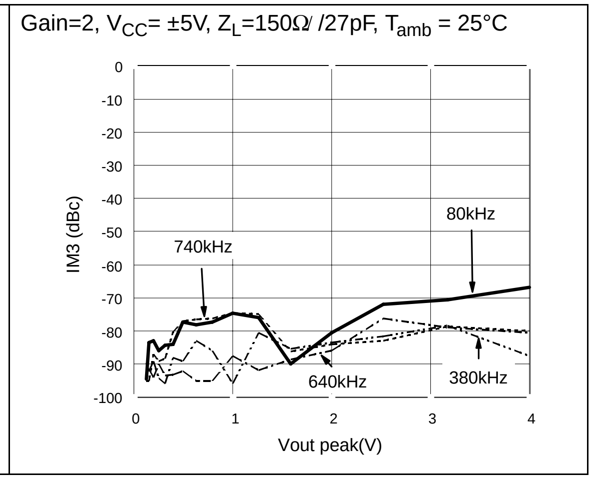
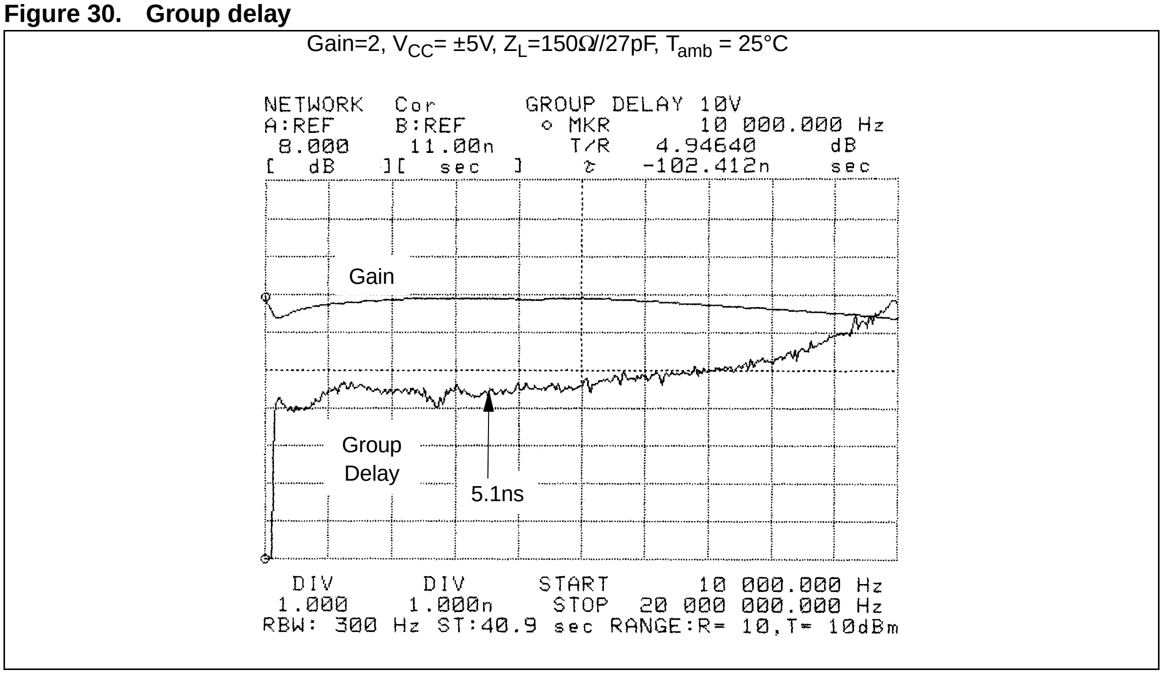


Figure 29. Third order intermodulation[1]



1. The IFR2026 synthesizer generates a two-tone signal (F1=180kHz, F2=280kHz), each tone having the same amplitude. The HP3585 spectrum analyzer measures the intermodulation products as a function of the output voltage. The generator and the spectrum analyzer are phase locked for better accuracy.

Figure 30. Group delay



3 Test conditions

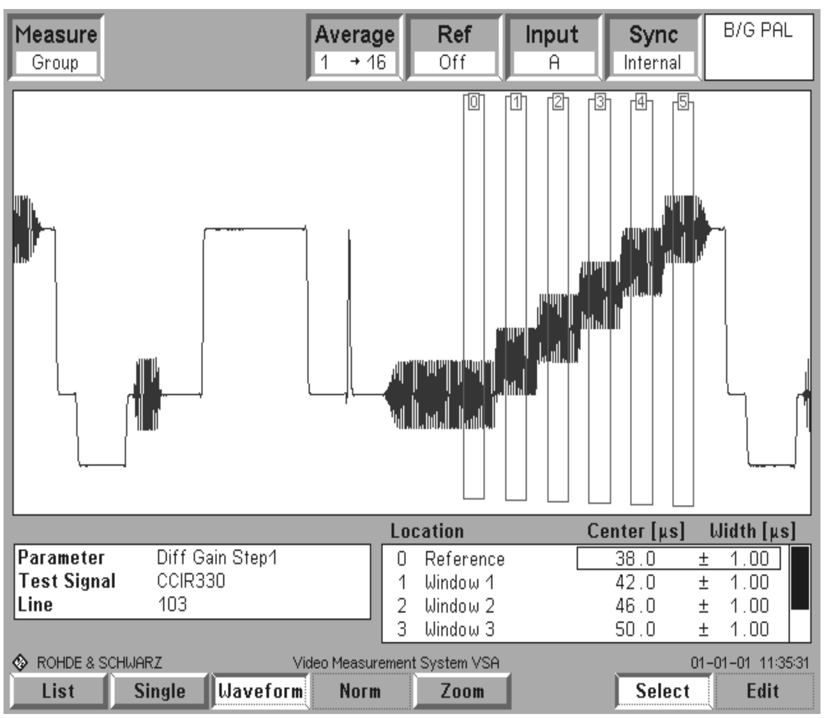
3.1 Layout precautions

To use the TSH8X circuits in the best manner at high frequencies, some precautions have to be taken for power supplies:

- In high-speed circuit applications, the implementation of a proper ground plane on both sides of the PCB is mandatory to ensure low inductance and low resistance common return.
- Power supply bypass capacitors (4.7µF and ceramic 100pF) should be placed as close as possible to the IC pins in order to improve high frequency bypassing and reduce harmonic distortion. The power supply capacitors must be incorporated for both the negative and the positive pins.
- All inputs and outputs must be properly terminated with output resistors; thus, the amplifier load is resistive only and the stability of the amplifier will be improved.

  All leads must be wide and as short as possible especially for op-amp inputs and outputs in order to decrease parasitic capacitance and inductance.
- In lower gain applications, use a low feedback resistance (under 1kΩ) to reduce the time constant with parasitic capacitance.
- Choose component sizes as small as possible (SMD).
- On the output, the load capacitance must be negligible to maintain good stability. You can put a serial resistance as close as possible to the output pin to minimize the effect of the load capacitance.

Figure 31. CCIR330 video line



3.2 Video capabilities

To characterize the differential phase and differential gain a CCIR330 video line is used.

The video line contains 5 (flat) levels of luminance onto which the chrominance signal is superimposed. The luminance gives various amplitudes which define the saturation of the signal. The chrominance gives various phases which define the color of the signal.

Differential phase (or differential gain) distortion is present if a signal chrominance phase (gain) is affected by luminance level. Differential phase and gain represent the ability to uniformly process the high frequency information at all luminance levels.

When differential gain is present, color saturation is not correctly reproduced.

The input generator is the Rhode & Schwarz CCVS. The output measurement is done by the Rhode and Schwarz VSA.

Figure 32. Measurement on Rhode and Schwarz VSA

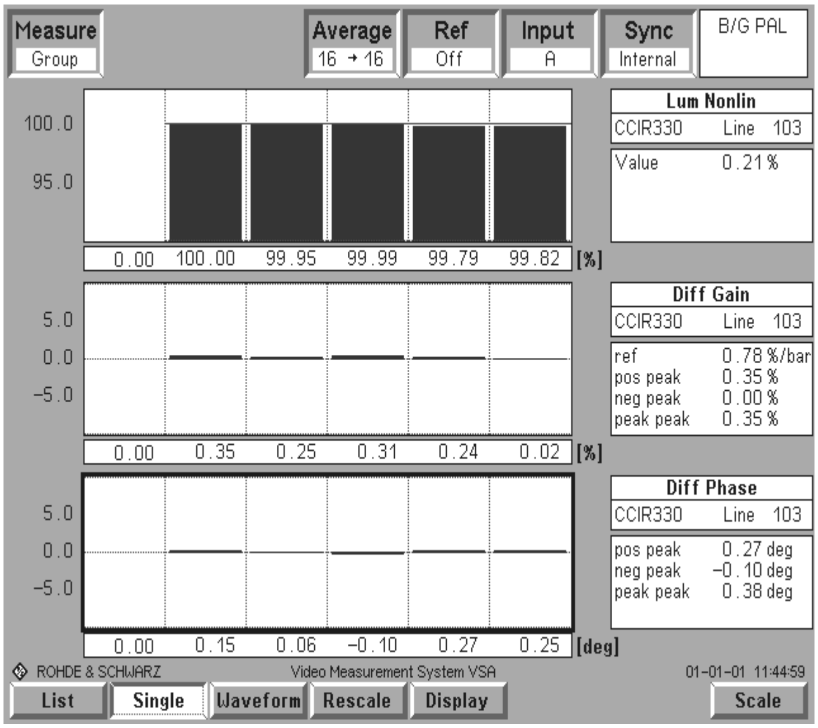


Table 7. Video results

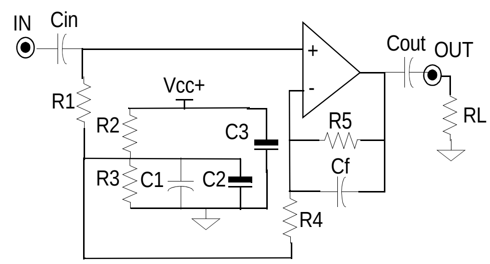
Parameter	Value (V_{CC}=±2.5V)	Value (V_{CC}=±5V)	Unit
Lum NL	0.1	0.3	%
Lum NL Step 1	100	100	%
Lum NL Step 2	100	99.9	%
Lum NL Step 3	99.9	99.8	%
Lum NL Step 4	99.9	99.9	%
Lum NL Step 5	99.9	99.7	%
Diff Gain pos	0	0	%
Diff Gain neg	-0.7	-0.6	%
Diff Gain pp	0.7	0.6	%
Diff Gain Step1	-0.5	-0.3	%
Diff Gain Step2	-0.7	-0.6	%
Diff Gain Step3	-0.3	-0.5	%
Diff Gain Step4	-0.1	-0.3	%
Diff Gain Step5	-0.4	-0.5	%
Diff Phase pos	0	0.1	degree
Diff Phase neg	-0.2	-0.4	degree
Diff Phase pp	0.2	0.5	degree
Diff Phase Step1	-0.2	-0.4	degree
Diff Phase Step2	-0.1	-0.4	degree
Diff Phase Step3	-0.1	-0.3	degree
Diff Phase Step4	0	0.1	degree
Diff Phase Step5	-0.2	-0.1	degree

4 Precautions on asymmetrical supply operation

The TSH8x can be used either with a dual or a single supply. If a single supply is used, the inputs are biased to the mid-supply voltage ($+V_{CC}/2$). This bias network must be carefully designed, in order to reject any noise present on the supply rail.

As the bias current is 15µA, you should use a high resistance R1 (approximately 10kΩ) to avoid introducing an offset mismatch at the amplifier inputs.

Figure 33. Asymmetrical supply schematic diagram



C1, C2, C3 are bypass capacitors intended to filter perturbation from V_{CC}. The following capacitor values are appropriate:

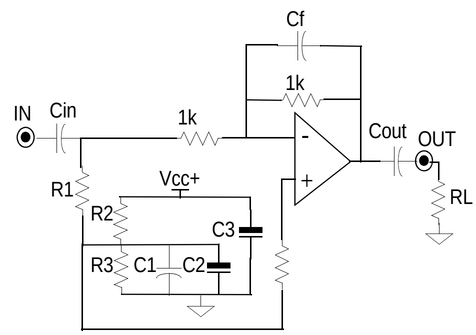
C1=100nF and C2=C3=100µF

R2 and R3 are such that the current through them must be superior to 100 times the bias current. Therefore, you could use the following resistance values:

R2=R3=4.7kΩ

C_{in} and C_{out} are chosen to filter the DC signal by the low pass filters (R1, C_{in}) and (R_{out}, C_{out}). With R1=10kΩ, $R_{out}=R_L$=150Ω, and C_{in}=2µF, C_{out}=220µF the cutoff frequency obtained is lower than 10Hz.

Figure 34. Use of the TSH8x in gain = -1 configuration

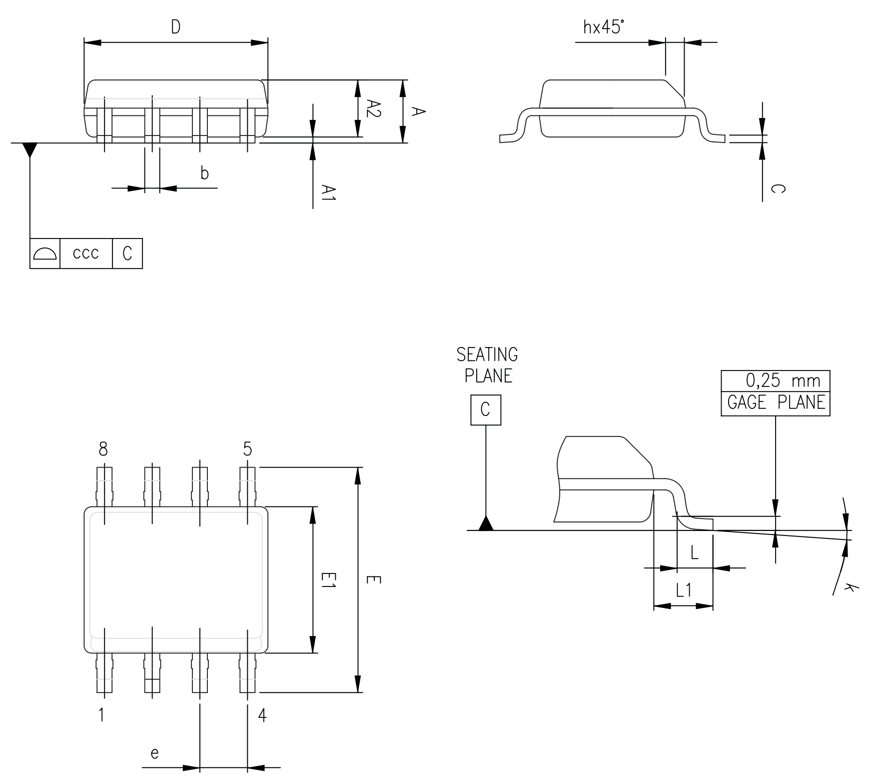


5 Package information

In order to meet environmental requirements, STMicroelectronics offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: www.st.com.

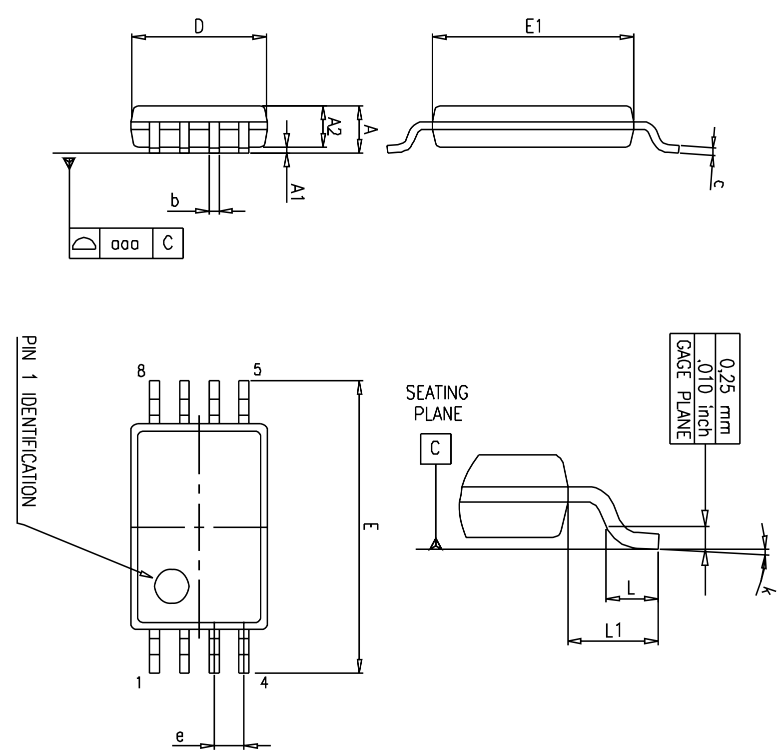
5.1 SO-8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
H	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	1°		8°	1°		8°
ccc			0.10			0.004



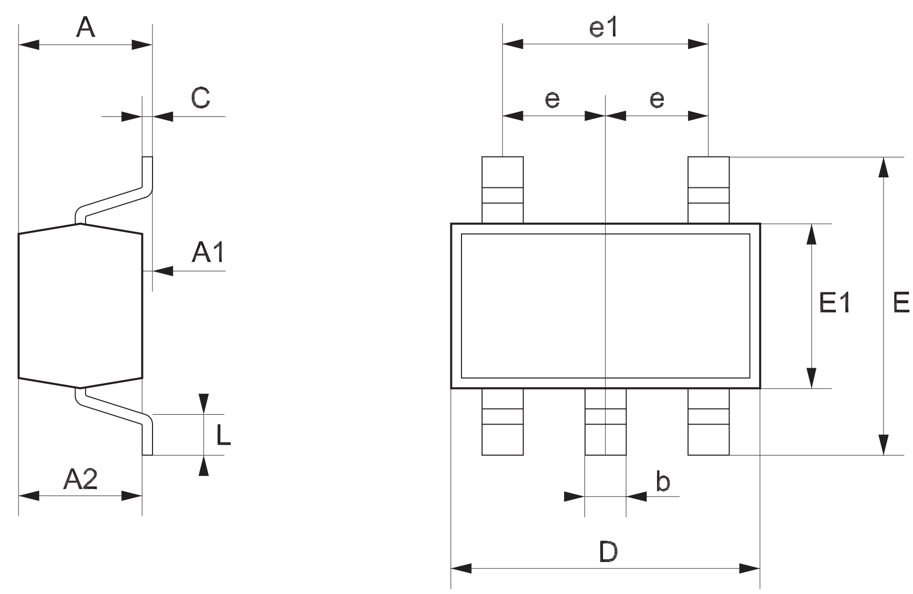
5.2 TSSOP8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65			0.0256	
k	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1			0.039	
aaa		0.1			0.004	



5.3 SOT23-5 package mechanical data

Ref.	Dimensions					
	Millimeters			Mils		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90		1.45	35.4		57.1
A1	0.00		0.15	0.00		5.9
A2	0.90		1.30	35.4		51.2
b	0.35		0.50	13.7		19.7
C	0.09		0.20	3.5		7.8
D	2.80		3.00	110.2		118.1
E	2.60		3.00	102.3		118.1
E1	1.50		1.75	59.0		68.8
e		0.95			37.4	
e1		1.9			74.8	
L	0.35		0.55	13.7		21.6



6 Ordering information

Table 8. Order codes

Type	Temperature range	Package	Packaging	Marking
TSH80ILT	-40°C to +85°C	SOT23-5	Tape & reel	K303
TSH80IYLT(1)		SOT23-5 (Automotive grade level)		K310
TSH80ID/DT		SO-8	Tube or tape & reel	TSH80I
TSH80IYD/IYDT(1)		SO-8 (Automotive grade level)		SH80IY
TSH81ID/DT		SO-8		TSH81I
TSH81IPT		TSSOP8	Tape & reel	SH81I
TSH81IYPT(1)		TSSOP8 (Automotive grade level)		H81IY
TSH82ID/DT		SO-8	Tube or tape & reel	TSH82I
TSH82IPT		TSSOP8	Tape & reel	SH82I
TSH82IYD/IYDT(1)		SO-8 (Automotive grade level)	Tube or tape & reel	SH82IY

1. Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q 002 or equivalent are on-going.

7 Revision history

Date	Revision	Changes
1-Feb-2003	1	First release.
2-Aug-2005	2	PPAP references inserted in the datasheet, see *Table 8: Order codes on page 23*.
12-Apr-2007	3	Corrected temperature range for TSH80IYD/IYDT and TSH82IYD/IYDT order codes in *Table 8: Order codes on page 23*.
24-Oct-2007	4	TSH81IYPT PPAP references inserted in the datasheet, see *Table 8: Order codes on page 23*.