

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

# TC9181P, TC9181F

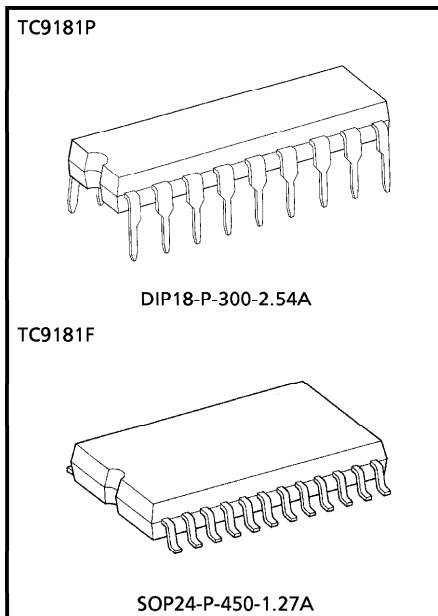
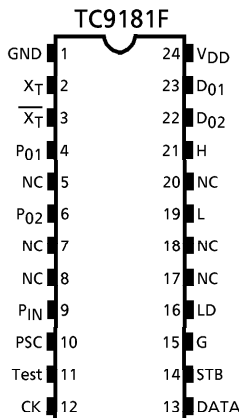
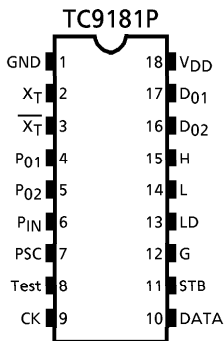
## PLL FREQUENCY SYNTHESIZER LSI FOR COMMUNICATION USE

The TC9181P and TC9181F are developed as PLL frequency synthesizer LSI for communication use and has following features.

### FEATURES

- Enable to be used as PLL LSI in many communication equipments e.g., Personal radio, Mobil telephone, CB radio and so on, because of it's various purposive system design.
- Built in 12 bits programmable counter as a reference frequency divider, so frequency division range of programmable counter is 5~4095 divisions according to serial data.
- Built in swallow type programmable counter to generate very high frequency.
- Phase comparator circuit has 3 types of output and replace of it inputs is possible.
- With 2 wide purposive output ports.
- Enable to be controlled by only 3 serial lines (DATA, CK, STB).

### PIN CONNECTION



Weight  
 DIP18-P-300-2.54A : 1.12g (Typ.)  
 SOP24-P-450-1.27A : 0.44g (Typ.)

980910EBA2

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**OPERATIONS**

1. Serial data input

Serial data can control 4 group functions separately.

Data is always input from LSB and final 2bit data selects the group.

- Group 1  Reference divider frequency division ratio.  
Phase comparator S, R inputs replace.
- Group 2  Programmable counter frequency division ratio.
- Group 3  Wide purposive output ports.
- Group 4  Phase comparator D<sub>02</sub> output ON/OFF control.  
Lock detector compulsory set.

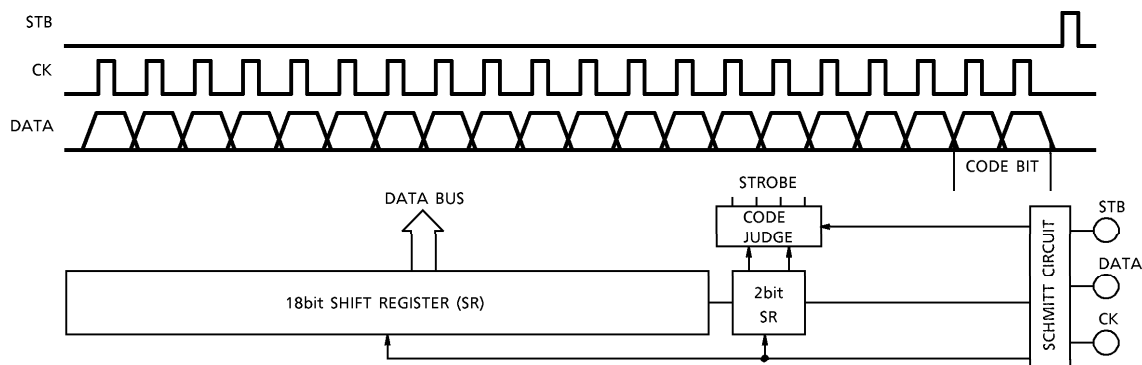
Serial data is composed of 3 lines of DATA, CK and STB.

DATA is input orderly in internal shift register at going rising edge of CK.

By setting STB "H" level after all DATA is input, DATA is transferred to the latch selected by the group code and this LSI can be controlled.

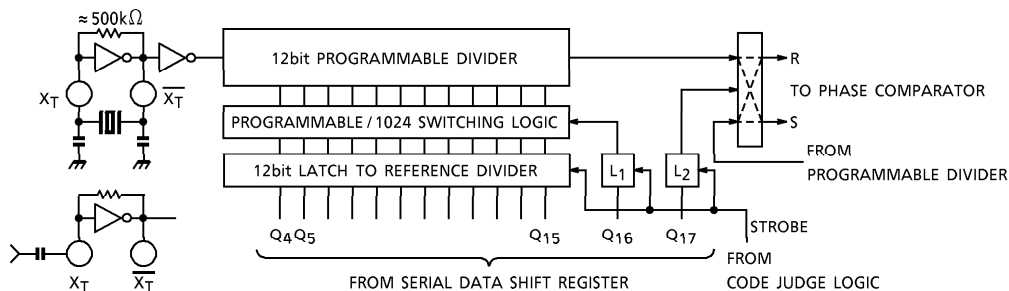
Serial data input 3 terminals build in schmitt trigger circuits that protect from data error by noise.

Concerning the data status of each group, refer to the respective block explanations.

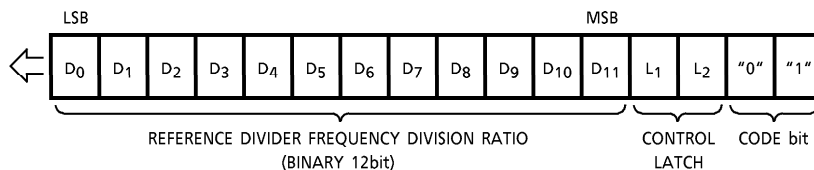


2. Reference divider

This block generates PLL reference frequency and is composed of Crystal oscillation amp, 12bit programmable divider and 2 control ports.



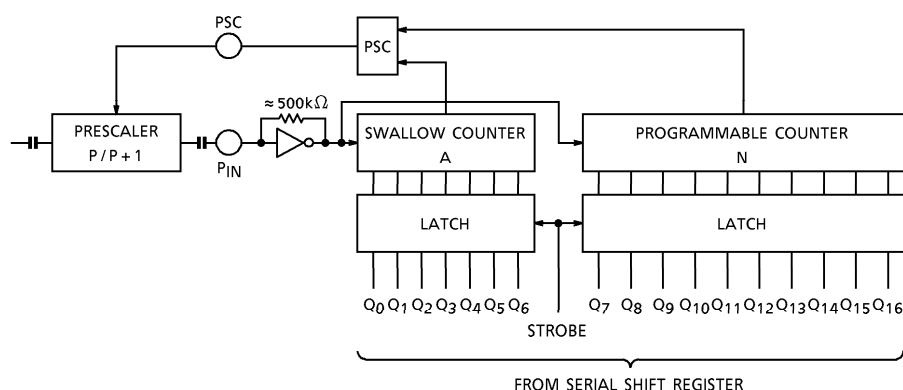
- Crystal oscillation amp allows crystal oscillation up to 15MHz and inputting signal in XT terminal externally up to 15MHz through a coupling capacitor.
- Programmable divider is composed of binary 12bit. Voluntary frequency division of range 5~4095 division is possible by serial data given externally. So a crystal to generate reference frequency can be selected freely and common use of the crystal using other purpose is possible. By setting Latch-1 (L<sub>1</sub>) at "H" level, frequency division ratio is fixed at 1024 division neglecting serial data. And at this time serial data becomes brief.
- Latch-2 (L<sub>2</sub>) is a control latch to replace reference divider output and programmable counter output before inputting to phase comparator circuit. Set L<sub>2</sub> at "L" level when external low pass filter is an inversion type, and set "H" level when not an inversion type.
- Serial data  
Serial data to control reference divider block is of 16bit as following construction.



\* D<sub>0</sub>~D<sub>11</sub> is binary code N of frequency division ratio intended.  
5 ≤ N ≤ 4,095

### 3. Programmable counter

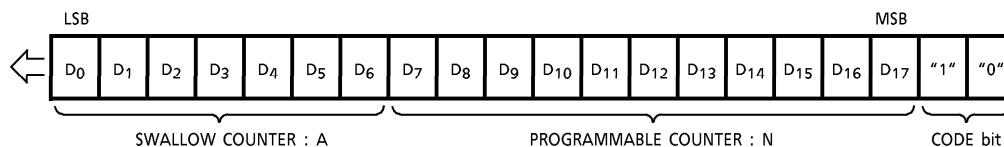
Programmable counter circuit adopts swallow system to generate high frequency and is composed of 7bit swallow counter, 11bit programmable counter and prescaler control logic to switch frequency division ratio of 2 modulus prescaler connected externally.



- Total frequency division ratio is defined as follows.  

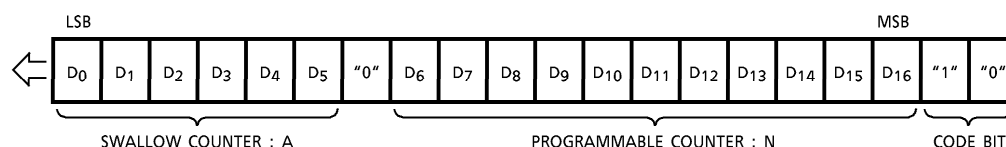
$$\text{Frequency division ratio} = (P + 1) \cdot A + P \cdot (N - A)$$

$$= P \cdot N + A \quad (\text{Note}) : N > A$$
- Frequency division ratio of the external prescaler should be "P + 1" when PSC is "L" level and "P" when PSC is "H" level.
- Serial data  
 Serial data which defines frequency division ratio of programmable counter is composed of 20bit but changes according to "P" of external prescaler.
  - (1) When used with an external prescaler of P = 128



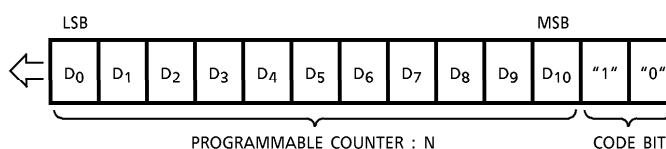
\* D<sub>0</sub>~D<sub>17</sub> is binary code D of frequency division ratio intended.  
 Generally  $16,384 \leq D \leq 262,143$

(2) When used with an external prescaler of P = 64



\* D<sub>0</sub>~D<sub>16</sub> is binary code D of frequency division ratio intended.  
 The 7th bit should be fixed at "L".  
 Generally  $4,096 \leq D \leq 131,071$

(3) When used as a normal programmable counter



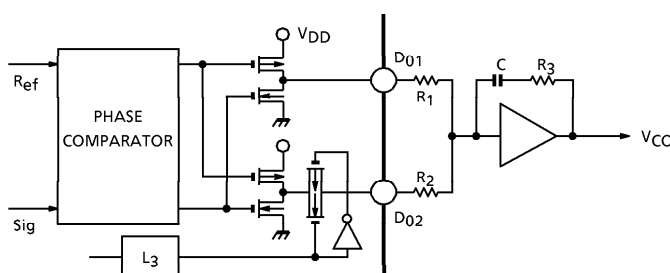
\* D<sub>0</sub>~D<sub>10</sub> is binary code D of frequency division ratio intended.  
 $5 \leq D \leq 2,047$

#### 4. Phase comparator

Phase comparator converts phase difference of reference divider output and programmable counter output into V<sub>CO</sub> control voltage and has features as following.

- Always operating ordinary tri-state output (D<sub>01</sub>).
- Tri-state output (D<sub>02</sub>) which can be controlled ON/OFF according to serial data given externally.
- Phase comparator outputs (H, L) to connect high voltage charge pump externally.
- Lock detector output (LD) which can be compulsorily set by data given externally.

(1) Example use of D<sub>01</sub>, D<sub>02</sub> terminal

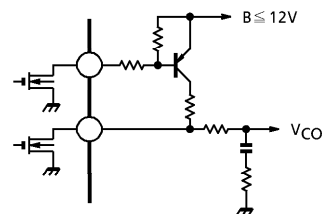


When change a channel, ON the D<sub>02</sub> output and make the time constant of the low pass filter smaller to make PLL lock state fastly.

And after PLL is locked, OFF the D<sub>02</sub> output and make the time constant larger to improve side-band spurious feature and stability.

(2) Example use of H, L terminals

When connect an external passive low pass filter, supply voltage of charge pump should be high. In this case connect an external PNP transistor as a right figure.

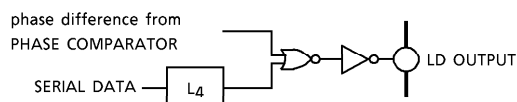


● Lock detector

Lock detector (LD) outputs pulse signal during phase deference time detected by phase detector circuit.

Additionally this lock detector output can be fixed unlocked state compulsorily by serial data given externally.

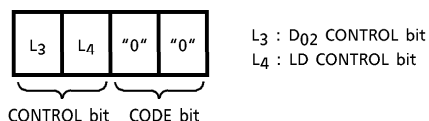
By fixing LD unlocked state just before channel changing to stop transmission output and canceling unlocked state after a definite time from the channel changing, troubles at channel changing e.g., overshoot can be prevented from.



● Serial data

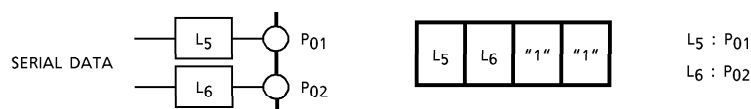
Serial data controls concerning phase comparator circuit are tri-state output ON/OFF control and lock detector compulsory set mentioned before.

They are composed of 4 bits serial data as below.



5. Wide purposive output port

P01, P02 output ports are available to many functions e.g., transmitter/receiver switching signal, band switching signal, sensibility switching and frequency band switching, according to serial data.



6. Test circuit

When Test terminal (8 pin) is placed at "H" level, this LSI is placed in the test mode as followings.

1. P01 terminal outputs reference divider output.
2. P02 terminal outputs programmable counter output.

## MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V <sub>DD</sub>	-0.3~7.0	V
Input Voltage	V <sub>IN</sub>	-0.3~V <sub>DD</sub> +0.3	V
Power Dissipation	P <sub>D</sub>	300	mW
Operating Temperature	T <sub>opr</sub>	-30~85	°C
Storage Temperature	T <sub>stg</sub>	-55~125	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta = 25°C, V<sub>DD</sub> = 5V)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage	V <sub>DD</sub>	—	f <sub>OSC</sub> = f <sub>PIN</sub> = 10MHz, V <sub>PIN</sub> = 0.5V <sub>p-p</sub> , Ta = -30~85°C	4.0	5.0	6.0	V
Operating Supply Current	I <sub>DD</sub>	—	f <sub>OSC</sub> = f <sub>PIN</sub> = 10MHz, V <sub>PIN</sub> = 0.5V <sub>p-p</sub> , Ta = -30~85°C	—	2.0	5.0	mA

## Reference divider block

X'tal Oscillating Frequency	f <sub>OSC</sub>	—	V <sub>DD</sub> = 4~6V	1.0	—	15.0	MHz
X <sub>T</sub> Input Frequency	f <sub>X<sub>T</sub>in</sub>	—	V <sub>DD</sub> = 4~6V, V <sub>X<sub>T</sub>in</sub> = 100mV <sub>rms</sub>	1.0	—	15.0	MHz
X <sub>T</sub> Input Voltage	V <sub>X<sub>T</sub>in</sub>	—	V <sub>DD</sub> = 4~6V, f <sub>X<sub>T</sub></sub> = 10MHz	100	—	—	mV <sub>rms</sub>

## Programmable counter block

P <sub>IN</sub> Frequency	f <sub>Pin</sub>	—	V <sub>DD</sub> = 4~6V, V <sub>Pin</sub> = 0.5V <sub>p-p</sub>	1k	—	10M	Hz
P <sub>IN</sub> Input Voltage	V <sub>Pin</sub>	—	V <sub>DD</sub> = 4~6V, f <sub>Pin</sub> = 10MHz	0.5	—	—	V <sub>p-p</sub>

Phase comparator block (D<sub>01</sub>, D<sub>02</sub>, LD, H, L)

Output Current	"H" Level	I <sub>OH</sub>	—	D <sub>01</sub> , D <sub>02</sub> , LD V <sub>DD</sub> = 5V, V <sub>OH</sub> = 4V	0.5	1.5	3.0	mA
	"L" Level	I <sub>OL</sub>	—	D <sub>01</sub> , D <sub>02</sub> , LD, H, L V <sub>DD</sub> = 5V, V <sub>OL</sub> = 1V	0.5	1.5	3.0	mA
Breakdown Voltage	V <sub>O</sub>	—	H, L, V <sub>DD</sub> = 4~6V	—	—	12.0	V	
Off Leak Current	I <sub>L</sub>	—	D <sub>01</sub> , D <sub>02</sub> , H, L V <sub>DD</sub> = 6V	—	—	0.1	μA	

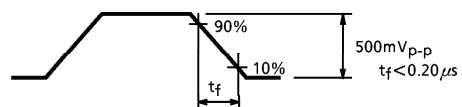
Output port (P<sub>01</sub>, P<sub>02</sub>)

Output Current	"H" Level	I <sub>OH</sub>	—	V <sub>DD</sub> = 5V, V <sub>OH</sub> = 4V	0.5	1.5	3.0	mA
	"L" Level	I <sub>OL</sub>		V <sub>DD</sub> = 5V, V <sub>OL</sub> = 1V	0.5	1.5	3.0	



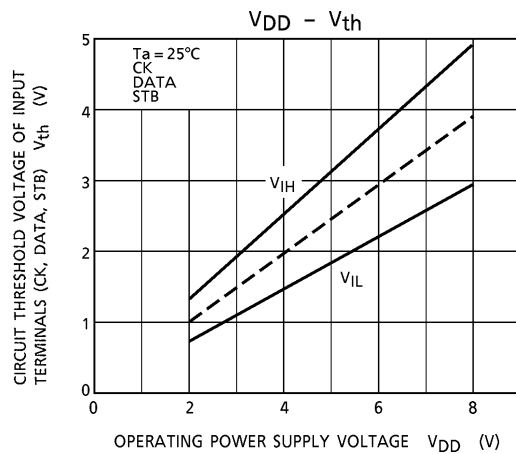
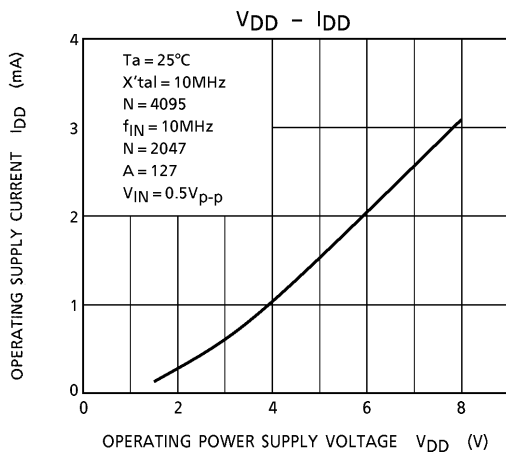
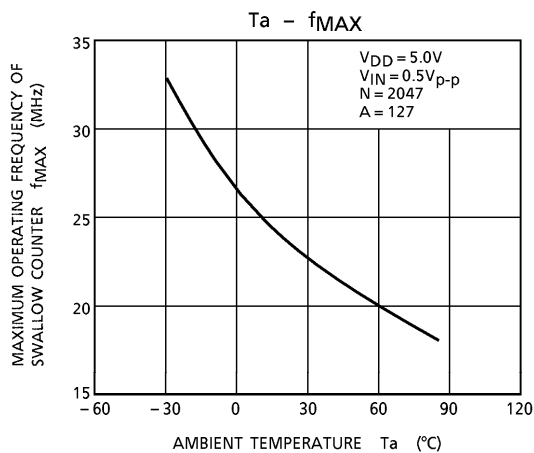
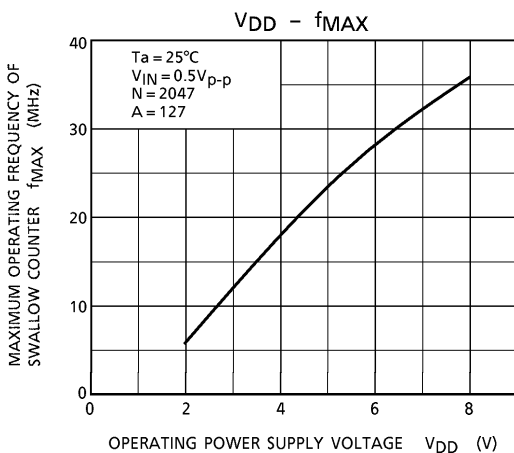
Serial input (CK, DATA, STB)

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage	"H" Level	$V_{IH}$	—	$V_{DD} = 5V$	3.8	—	5.0	V
	"L" Level	$V_{IL}$	—	$V_{DD} = 5V$	0.0	—	1.2	
Input Speed		SIN	—	—	5	—	—	$\mu s$

(Note 1)  $X_T$  : SIN wave input $P_{IN}$  : SQ wave input(Note 2) Falling of  $P_{IN}$  input wave have a rule as following.\* t<sub>f</sub> < 0.20 μs

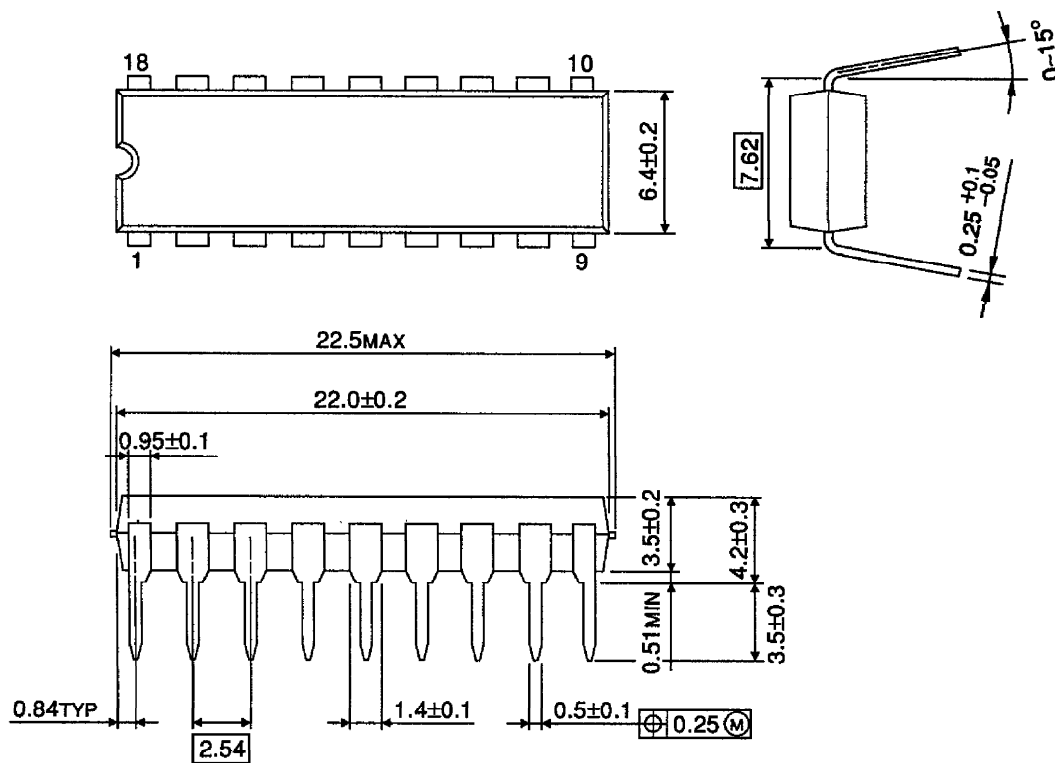
(Note 3) Choose a crystal oscillator that has a small CI value and good startup characteristics.

CHARACTERISTIC DATA



**OUTLINE DRAWING**  
DIP18-P-300-2.54A

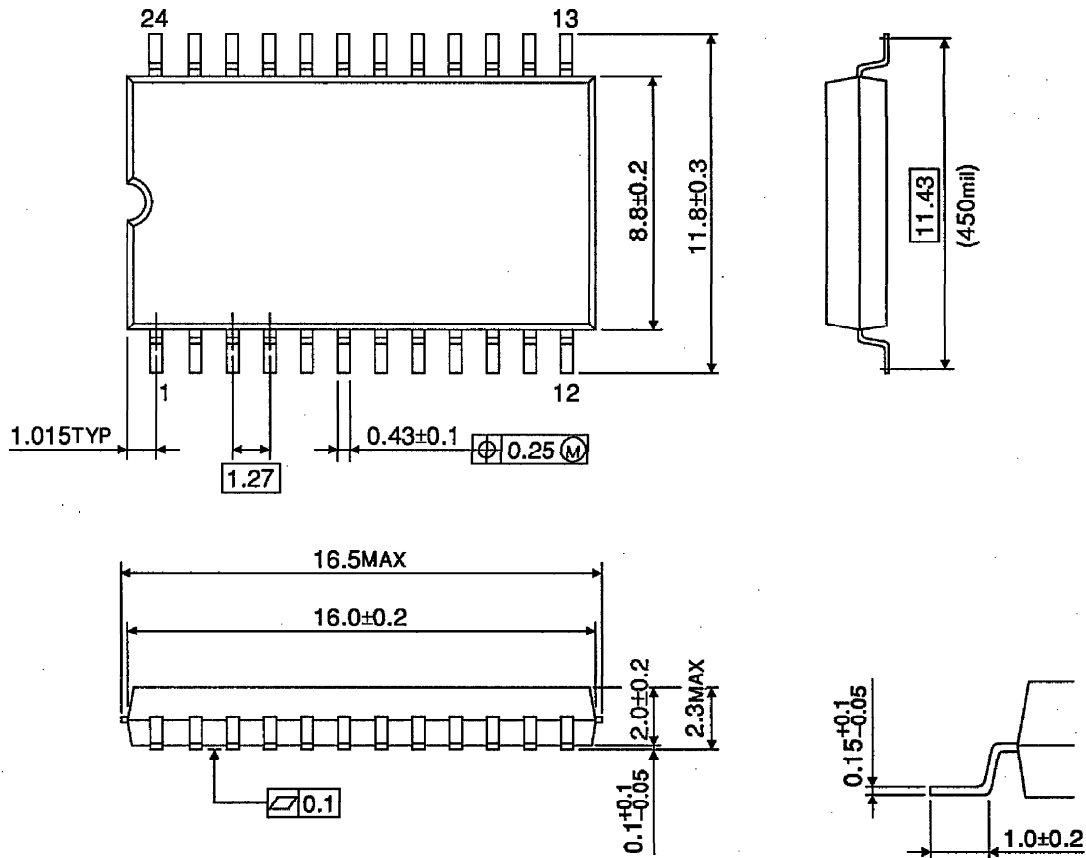
Unit : mm



Weight : 1.12g (Typ.)

OUTLINE DRAWING  
SOP24-P-450-1.27A

Unit : mm



Weight : 0.44g (Typ.)