TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC9198P, TC9198F

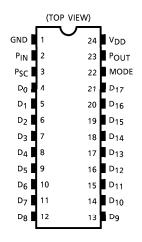
PROGRAMMABLE COUNTER

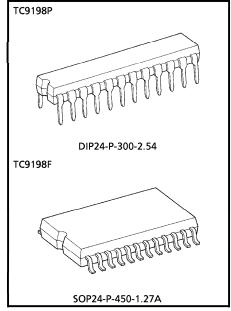
TC9198P, TC9198F are high speed programmable counters developed for dividing PLL circuits and other various circuits.

FEATURES

- Setting of number of divisions can be made directly from the input terminals.
- The counter allows changing-over of swallow system/ simple division.
- At simple division, changing-over of BCD code/BINARY code can be performed.
- The number of division is 262, 143 in maximum in swallow mode, and can be 5 to 65,535 at BINARY in simple division mode and can be 5 to 15,999 at BCD
- Owing to CMOS construction, the operating power voltage range is wide, and the power consumption is
- The package is DIP-24PIN for TC9198P and SOP-24PIN for TC9198F.

PIN CONNECTION





Weight

DIP24-P-300-2.54 : 1.2g (Typ.) SOP24-P-450-1.27A : 0.48g (Typ.)

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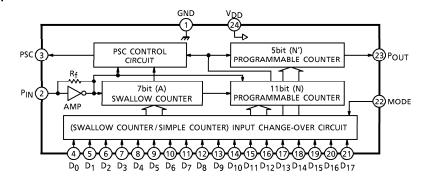
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1999-03-19

BLOCK DIAGRAM



PIN FUNCTION

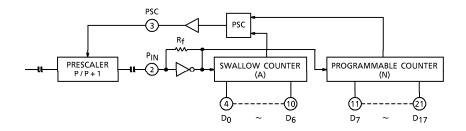
PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	NOTE
1	GND	Ground Terminal	_	
24	V_{DD}	Power Supply Terminal	_	_
₂	PIN	Programmable	Programmable counter input terminal.	Amp. Circuit
	1111	Counter Input	Prescaler output is input by the capacitor coupling.	built in
3	PSC	Prescaler Control	No. of division control signal output prescaler. It	_
		Output	becomes P in "H" level, and P+1 in "L" level.	
22	MODE	Counter Operation Change-over Input	Change-over input for swallow counter operation and simple counter operation. It becomes swallow counter at "L" level, or open and simple counter operation at "H" level.	
4	D ₀		Input terminal for setting number of division of	
5	D ₁		programmable counter.	
6	D ₂		(1) MODE (22PIN) = at "L" level	
7	D ₃		D ₀ ~D ₆ →Swallow counter : A	
8	D ₄		 D₇~D₁₇→Programmable counter: N 	
9	D ₅		(2) MODE = at "H" and D ₁₇ = at "L" level	Pull down
10	D ₆		 Simple counter operation in setting BINARY 	resistance
11	D ₇		code.	built in
12	D ₈	Number of Division	D ₀ ~D ₁₅ →Programmable counter: N	
13	Dg	Setting Input	● D ₁₆ →NC	
14	D ₁₀		(3) MODE = at "H" and D ₁₇ = at "H" level ■ Simple counter operation in setting BCD	
15	D ₁₁		code.	
16	D ₁₂		 D₀~D₃→N = 1~9 setting 	
17	D ₁₃		• D ₄ ~D ₇ →N = 10~90 setting	
18 19	D ₁₄		• $D_8 \sim D_{11} \rightarrow N = 100 \sim 900 \text{ setting}$	
20	D ₁₅		D ₁₂ ~D ₁₅ →N = 1000~15000 setting	
21	D ₁₆		• D ₁₆ →NC	
41	D ₁₇	Programmable		
23	POUT	Programmable Counter Output Terminal	1/N of P _{IN} input frequency is output pulse width corresponds to 4 cycles of input frequency.	_

DESCRIPTION ON FUNCTION AND OPERATION

1. Programmable counter

When the MODE INPUT (Pin 22) is set to "L" level (or opened), the programmable counter becomes swallow system.

The system consists of a 7bit swallow counter, 11bit programmable counter and a prescaler logic which change-over the number of divisions of the 2-module prescaler connected to the outside.



• Total number of divisions can be determined by the following formula

Number of divisions =
$$(P + 1) \cdot A + P \cdot (N - A)$$

= $N \cdot P + A$ Where, $N > A$

- The prescaler used requires to be the number of divisions of P+1 when the PSC terminal is in "L" level and of P when it is in "H" level.
- The input for setting the number of divisions of the programmable counter consists of 18bits, but it should be cared that it changes by the number of divisions P of the prescaler used. (P≤128)
 - (1) When prescaler is P = 128

D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	D ₈	D9	D ₁₀	D ₁₁	D ₁₂	D ₁₃	D ₁₄	D ₁₅	D ₁₆	D ₁₇
2 ⁰	2 ¹	2 ²	2 ³	2 ⁴	2 ⁵	2 ⁶	2 ⁷	2 ⁸	2 ⁹	2 ¹⁰	2 ¹¹	2 ¹²	2 ¹³	2 ¹⁴	2 ¹⁵	2 ¹⁶	2 ¹⁷

- (*) The BINARY code D of the number of division is $16,384 \le D \le 262,143$, as a rule.
- (2) When prescaler is P = 64

D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	D ₈	D9	D ₁₀	D ₁₁	D ₁₂	D ₁₃	D ₁₄	D ₁₅	D ₁₆	D ₁₇
2 ⁰	2 ¹	2 ²	2 ³	2 ⁴	2 ⁵	"0"	2 ⁶	2 ⁷	2 ⁸	2 ⁹	2 ¹⁰	2 ¹¹	2 ¹²	2 ¹³	2 ¹⁴	2 ¹⁵	2 ¹⁶

- (*) The BINARY code D of the number of divisions is $4,096 \le D \le 131,071$, as a rule.
- (*) D₆ (Pin 10) is used as GND or in open.

(3) When prescaler is P = 32

D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	D ₈	D9	D ₁₀	D ₁₁	D ₁₂	D ₁₃	D ₁₄	D ₁₅	D ₁₆	D ₁₇
2 ⁰	2 ¹	2 ²	2 ³	24	"0)"	2 ⁵	2 ⁶	2 ⁷	2 ⁸	2 9	2 ¹⁰	2 ¹¹	2 ¹²	2 ¹³	2 ¹⁴	2 ¹⁵

- (*) The BINARY code D of the number of divisions is $1,024 \le D \le 65,535$, as a rule.
- (*) D₅ (Pin 9) and D₆ (Pin 10) are used as GND or in open.
- (4) When prescaler is P = 16

ı	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	D ₈	D9	D ₁₀	D ₁₁	D ₁₂	D ₁₃	D ₁₄	D ₁₅	D ₁₆	D ₁₇
	2 0	2 ¹	2 ²	2 ³		"0"		2 ⁴	2 ⁵	2 ⁶	2 ⁷	2 ⁸	2 9	2 ¹⁰	2 ¹¹	2 ¹²	2 ¹³	2 ¹⁴

- (*) The BINARY code D of the number of divisions is $256 \le D \le 32,767$, as a rule.
- (*) D₄~D₆ (Pin 8~Pin 9) are used as GND or in open.

2. Simple program counter

When the MODE INPUT (Pin 22) is set to "H" level, the simple counter system is established. When D_{17} (Pin 21) is made to "H" level, the system operates in BCD mode, and to "L" level, in BINARY mode.

(1) Operation in BINARY MODE : D_{17} (Pin 21) = D_{16} (Pin 20) = "L" level or in open

D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	D ₈	D9	D ₁₀	D ₁₁	D ₁₂	D ₁₃	D ₁₄	D ₁₅
2 ⁰	2 ¹	2 ²	2 ³	2 ⁴	2 ⁵	2 ⁶	2 ⁷	2 ⁸	2 9	2 ¹⁰	2 ¹¹	2 ¹²	2 ¹³	2 ¹⁴	2 ¹⁵

- % The BINARY code D of number of divisions becomes 5≤D≤65,535
- (2) Operation in BCD MODE: D_{17} (Pin 21) = "H", D_{16} (Pin 20) = "L" level or open

	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	D ₈	D9	D ₁₀	D ₁₁	D ₁₂	D ₁₃	D ₁₄	D ₁₅
	1	2	4	8	1	2	4	8	1	2	4	8	1	2	4	8
i	1 2 4 8 1					— ×	10 —	•		— x	100 —			— × 1	000 —	

- (*) $D_0 \sim D_3$, $D_4 \sim D_7$, $D_8 \sim D_{11}$ set number of divisions by BCD code. It should be cared that it does not operate when it is set N = 10 or more.
- (*) In $D_{12}\sim D_{15}$, the number of division can be set by the BINARY code.

 $D_{12} \sim D_{15} = 0101 (A) \rightarrow N = 10,000$

 $D_{12} \sim D_{15} = 1101 (B) \rightarrow N = 11,000$

 $D_{12} \sim D_{15} = 0011 (C) \rightarrow N = 12,000$

 $D_{12} \sim D_{15} = 1011 (D) \rightarrow N = 13,000$

 $D_{12} \sim D_{15} = 0111 (E) \rightarrow N = 14,000$

 $D_{12} \sim D_{15} = 1111 (F) \rightarrow N = 15,000$

(*) The BCD code of the number of divisions becomes $5 \le D \le 15,999$

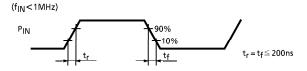
MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{DD}	-0.3~7.0	V
Input Voltage	VIN	-0.3~V _{DD} +0.3	V
Power Dissipation	PD	300	mW
Operating Temperature	T _{opr}	- 40~85	°C
Storage Temperature	T _{stg}	-65∼150	°C

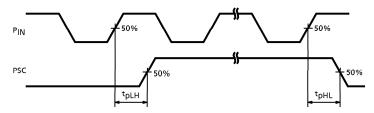
ELECTRICAL CHARACTERISTICS (Unless otherwise specified, $Ta = -40 \sim 85^{\circ}C$, $V_{DD} = 5.0V$)

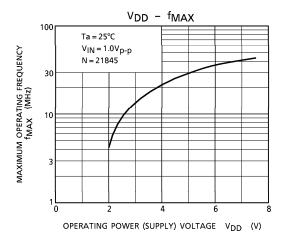
CHARACTI	ERISTIC	SYMBOL	TEST CIR- CUIT	TEST CON	DITION	MIN.	TYP.	MAX.	UNIT
Operating Sup	ply Voltage	V_{DD}	_	f 1 EN / U = \/.	1 0\/	4.0	5.0	6.0	٧
Operating Sup	ply Current	lDD	_	$f_{IN} = 15MHz, V_I$	N = 1.0Vp-p	_	5.0	10	mΑ
Maximum Ope	rating	f _{opr (1)}	_	V _{IN} = 1.0V _{p-p} , BINARY mode		1.0	_	15	MHz
Frequency		f _{opr} (2)	_	$V_{IN} = 1.0V_{p-p}$, B	CD mode	1.0	_	15	
Minimum Oper Frequency	rating	fMIN	_	$V_{IN} = 1.0V_{p-p}$	(Note 1)		0.5	1.0	kHz
Operating Inpu	ut	V _{IN}	_	f _{IN} = 15MHz		1.0	~	V _{DD} – 0.1	V _{p-p}
Input Voltage	"H" Level	VIH	_	D D (-1	$V_{DD} \times 0.7$	~	V_{DD}	V
Imput voitage	"L" Level	V _{IL}	_	D ₀ ~D ₁₇ termin		0	~	$V_{DD} \times 0.3$	٧
Pull-down Resi	stance	R _{DW}	_	WIODE terminal		32	47	62	kΩ
Output	"H" Level	O H	_	PSC, POUT	$V_{OH} = 4.0V$	0.5	1.0	_	mΑ
Current	"L" Level	οΓ	_	terminal	$V_{OL} = 1.0V$	0.5	1.0	_	ША
Input Resistance		R _f	_	P _{IN} terminal		82	125	250	kΩ
Transfer	Transfer "H" Level		_	P _{IN} →PSC transf	_	100	200	nc	
Time	"L" Level	t _{pHL}	_	$C_L = 15pF$	(Note 2)	_	100	200	ns

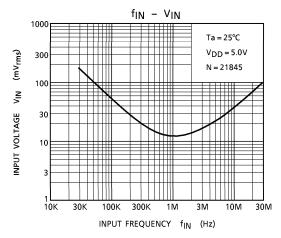
(Note 1) At the test of the minimum operating frequency, the input waveform is specified as follows.

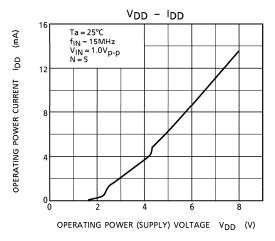


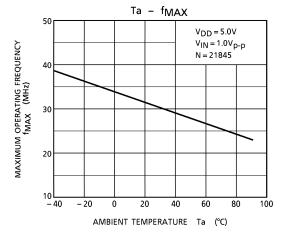
(Note 2) $P_{IN} \rightarrow P_{SC}$ transfer time





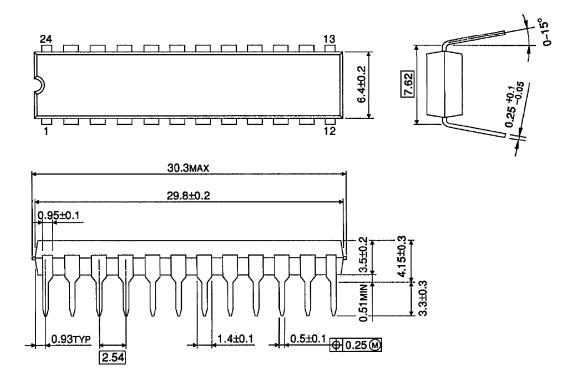




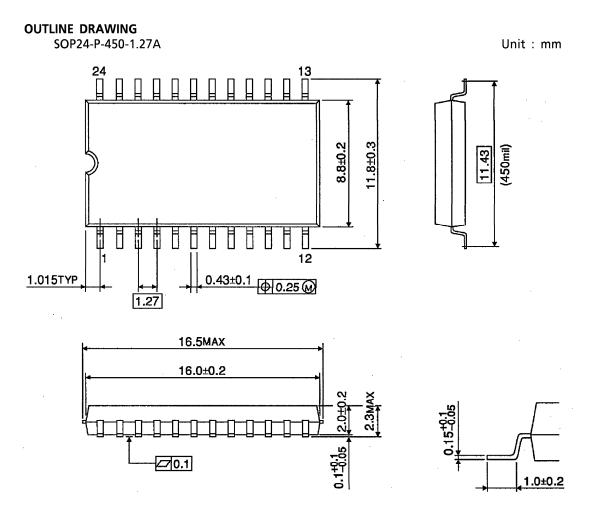


OUTLINE DRAWING DIP24-P-300-2.54

Unit: mm



Weight: 1.2g (Typ.)



Weight: 0.48g (Typ.)