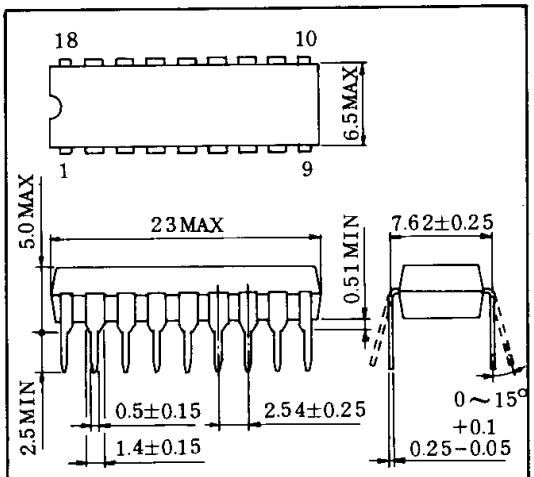
TC9192P/F

DOUBLE PLL FOR MOTOR CONTROL

This is a LSI designed for motor-controlling the copying machine of which motor-rotation speed is necessary to be varied freely. With built-in PLL and VCO for reference signal generation, reference frequency can voluntarily be varied externally.

- Through using built-in VCO, P_D, phase comparator and divider reference frequencies can be obtained.
- AFC and APC applied with 8-bit D/A converter system is incorporated, and transistor of bipolar type is provided at the output for Buffer Amplifier
- Lock range can be switched.
- Reference voltage output for filiter-amplifier is provided.
- Lock detection output and reverse rotation signal output are provided.

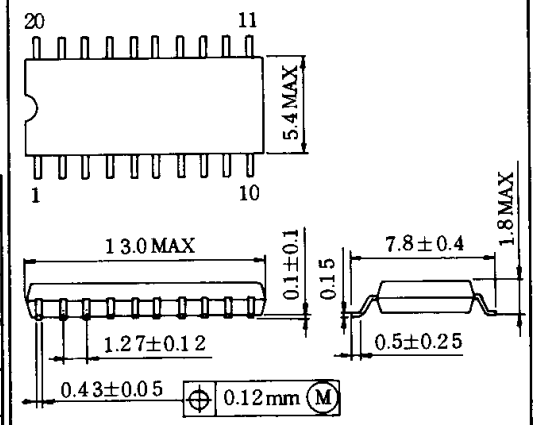
Unit in mm



Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.18 leads.

JEDEC	—
TOSHIBA	3D18A-P

Unit in mm



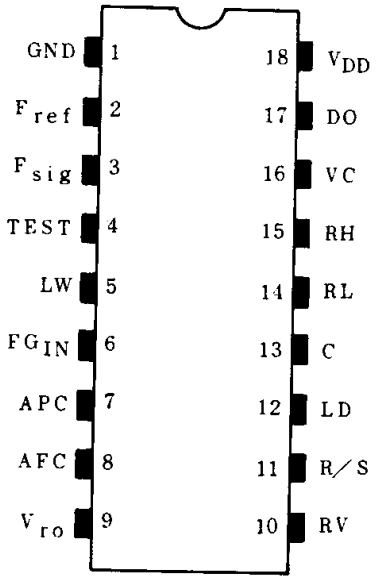
JEDEC	—
TOSHIBA	F-20GA-P

MAXIMUM RATINGS (Ta=25°C)

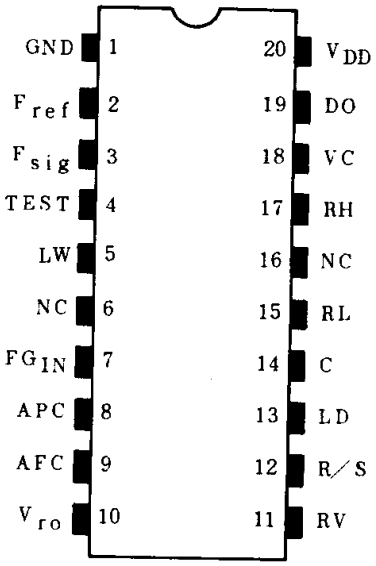
CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{DD}	-0.3~7.0	V
Input Voltage	V_{IN}	-0.3~V_{DD}+0.3	V
Power Dissipation	P_D	300	mW
Operating Temperature	Topr	-30~75	°C
Storage Temperature	Tstg	-55~125	°C

PIN CONNECT

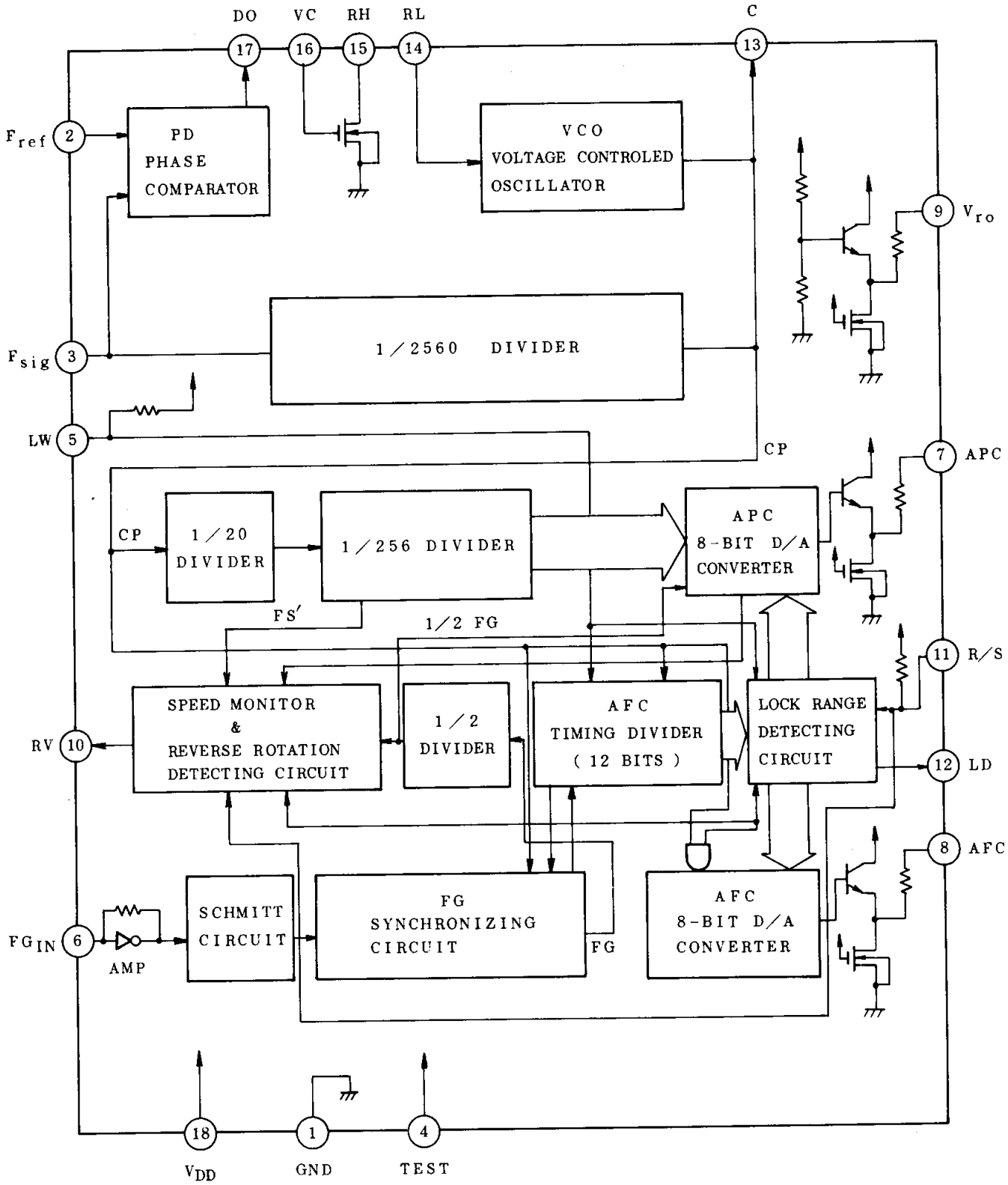
TC9192P



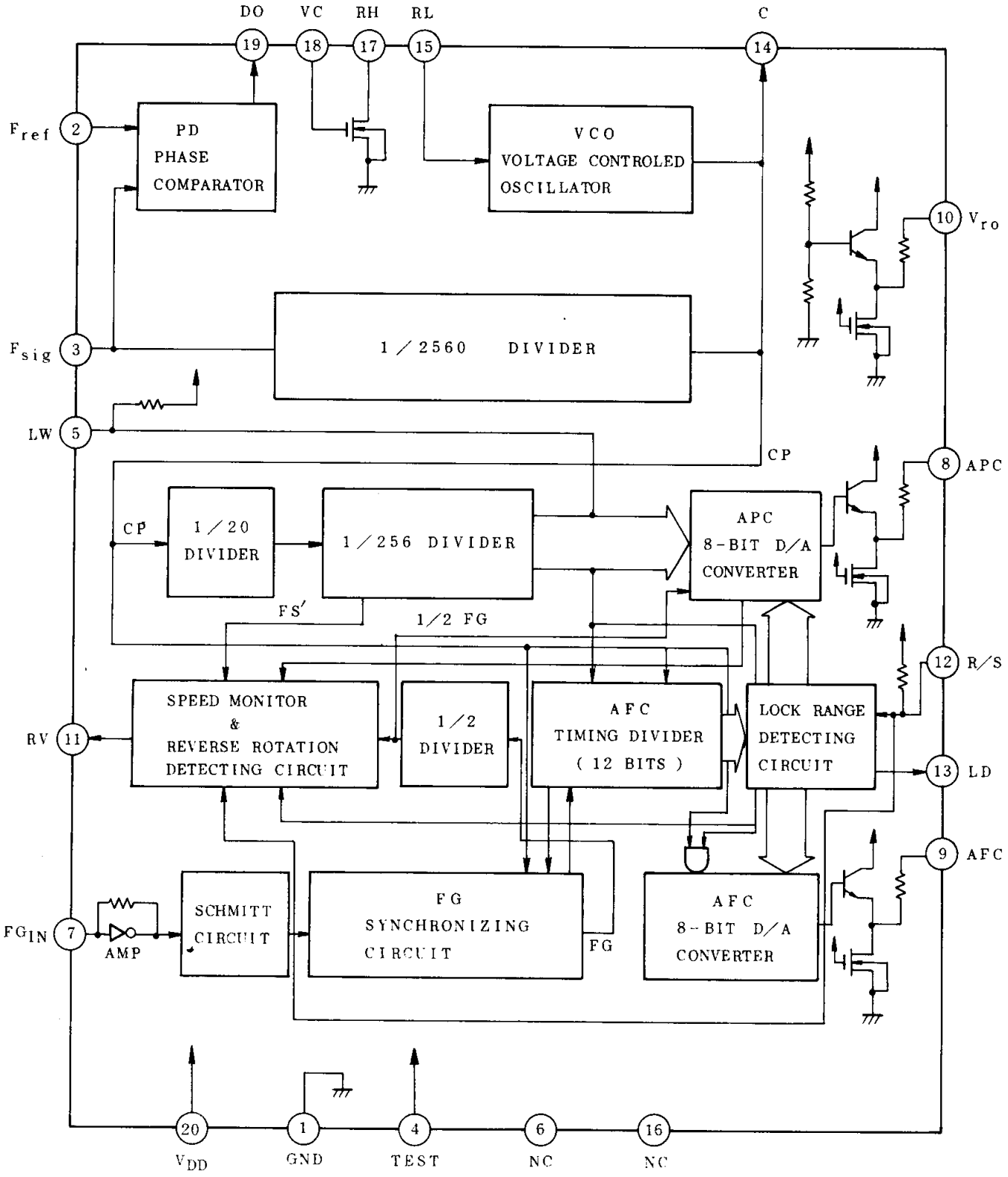
TC9192F



BLOCK DIAGRAM TC9192P



BLOCK DIAGRAM TC9192F

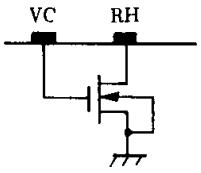


ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta=25°C, V_{DD}=5V)

CHARACTERISTIC	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Operating Power Supply Voltage	V_{DD}			4.5	~	5.5	V
Power Supply Current	I_{DD}		*	-	7	20	mA
VCO BLOCK							
Max. Operating Frequency	$f_{VCO\ Max}$	C=33pF, R_L=0V	*	4.0	6.0	-	MHz
VCO Applicable Range	f_{VCO}	Constant of C is varied with f_{VCO}	*	0.5	~	4.0	MHz
VCO Deviation	Δf_{VCO}	C=Constant, R_L=2.0V	*	-	±50	-	%
VCO Fsig Frequency Range	f_{CPIN}	Fsig N=2560	*	0.5	~	4.0	MHz
FG AMPLIFIER BLOCK							
Operating Frequency Range	f_{FG}	V_{IN}=0.5Vp-p	*	-	~	10	kHz
Input Operating Voltage	VFG	f_{fg}=10kHz, Sine wave	*	0.5	~	V_{DD}-0.5	Vp-p
Fref Frequency Range	fref		*	0.2	~	2.0	kHz
APC, AFC, D/A CONVERTER BLOCK							
Max. Deviation		Measuring at buffer output		-	±2.5	±6.5	LSB
Resolution				-	V_{DD}/256	-	
Ladder Resistance	RD			30	50	70	kΩ
BIPOLAR TRANSFORMER OUTPUT CURRENT (APC, AFC, V_{ro} TERMINAL)							
Output Current	"H" Level	I_{OHB}	V_{OH}=3V	-	-1.6	-0.8	mA
	"L" Level	I_{OLB}	V_{OL}=2V	30	50	200	μA
Output Voltage		V_{ro}	Reference Output Voltage	1.6	1.9	2.2	V
PHASE COMPARATOR CHARACTERISTIC (DO TERMINAL)							
Output Current	"H" Level	I_{OHDO}		~	-	-1.0	mA
	"L" Level	I_{OLDO}		1.0	2.0	~	
Output Leak Current at OFF		I_{OZDO}		-	-	±0.1	μA
Input Leak Current		I_{IH}/I_{IL}	Fref, VC terminal	~	-	±1.0	μA
Pull-up Resistance		R_{IN}	LW, R/S terminal	15	30	45	kΩ
Input Voltage	"H" Level	V_{IH}	FG_{IN}, LW, R/S terminal	0.7×V_{DD}	~	V_{DD}	V
	"L" Level	V_{IL}	Fref	0	~	0.3×V_{DD}	
Output Current	"H" Level	I_{OH}	RV,LD terminal, V_{OH}=4V	-	-1.0	-0.5	mA
	"L" Level	I_{OL}	V_{OL}=1V	0.5	1.0	-	
Nch OPEN DRAIN CURRENT							
Nch ON Current	I_{OLD}	RH terminal	V_G=5V	1.5	2.5	-	mA
Nch OFF Current	I_{OID}		V_G=0V	-	-	±1.0	μA

* : Guaranted within the range of V_{DD}=4.5V~5.5V, Ta=-30~75°C.

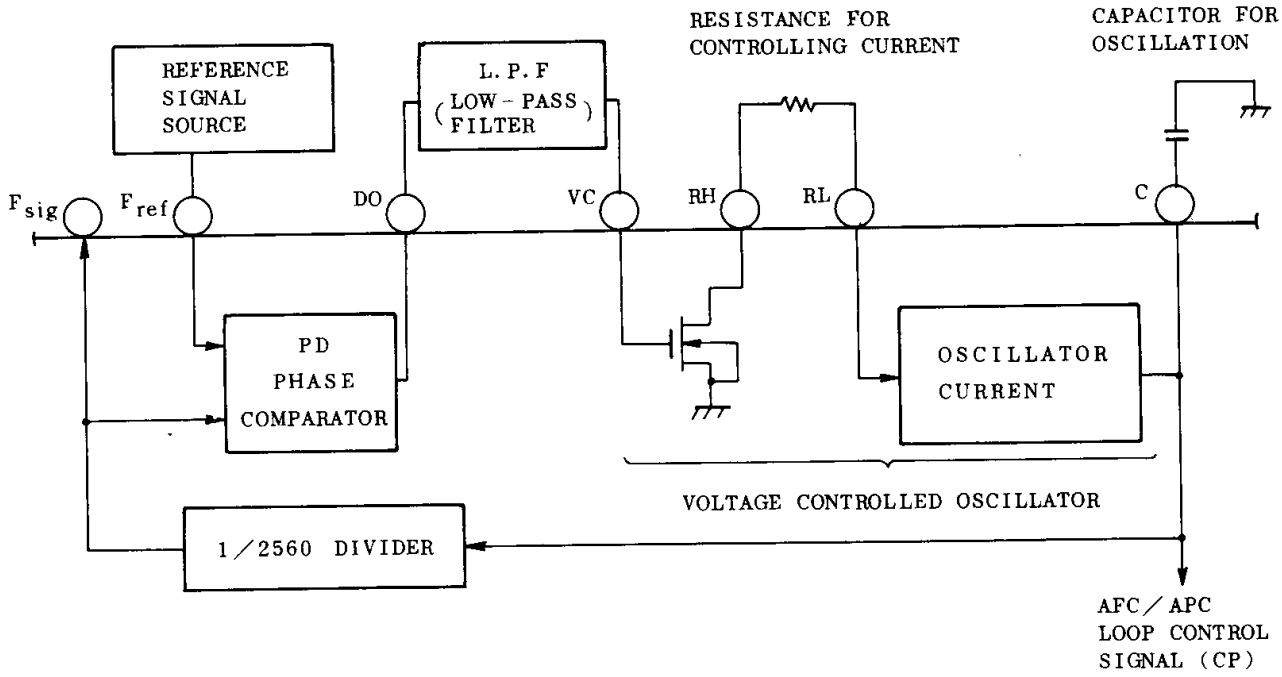
FUNCTIONAL DISCRIPTION OF EACH PIN

PIN No. P	PIN No. F	SYMBOL	FUNCTION, OPERATION	REMARKS
18	20	V_{DD}	Power supply voltage terminal and grounding terminal.	
1	1	GND		
2	2	F_{ref}	Reference frequency input terminal for phase comparator.	C-MOS input
3	3	F_{sig}	1/2560 dividing output terminal of VCO frequency, internally comparison signal is made.	C-MOS output
5	5	LW	Switching terminal of lock range. at LW="H", normal range. at LW="L", double range.	Built-in pull-up resistance speed
6	7	FG_{IN}	Pulse input terminal for indicating the rotation speed of motor.	Built-in amp.
7	8	APC	Output terminal of APC 8-bit D/A converter output.	Built-in bipolar transistor
8	9	AFC	Output terminal of AFC 8-bit D/A converter output.	Built-in bipolar transistor
9	10	V_{ro}	Output terminal for reference voltage.	Built-in bipolar transistor
10	11	RV	Reverse rotation signal for output driver.	C-MOS output
11	12	R/S	RUN/STOP switching terminal of motor at R/S="L", RUN. at R/S="H", STOP	Built-in pull-up resistance
12	13	LD	Lock detecting terminal. When the rotation frequency is within lock range, "H" level, and in other cases, "L" level.	C-MOS output
13	14	C	Terminal attached with capacitor for adjusting frequency. Internal control signal is made.	
14	15	RL	Current control terminal for controlling VCO frequency.	
15	17	RH	Current control output terminal for VCO	
16	18	VC	Voltage control input terminal for VCO	
17	19	DO	Output terminal of phase comparator	C-MOS input
4	4	Tset	Input terminal of internal test. Generally ground.	C-MOS input
-	6,16	NC	No connect	

EXPLANATION OF OPERATION

TC9192P/F has double PLL which is consist of AFC/APC loop for motor-controlling and phase feedback loop for reference signal. In the following operation of respective block is explained.

1. Phase Feedback Loop



(1) Voltage controlled oscillator terminal (C,RL,RH,VC)

. Voltage controlled oscillator (VCO) is consist of the Nch open drain FET (VC,RH, terminal) and current controlled oscillator (RL,C terminal) combinated.

VCO is an oscillator of which oscillation frequency is controlled by given control voltage. The control voltage and oscillation frequency are proportional.

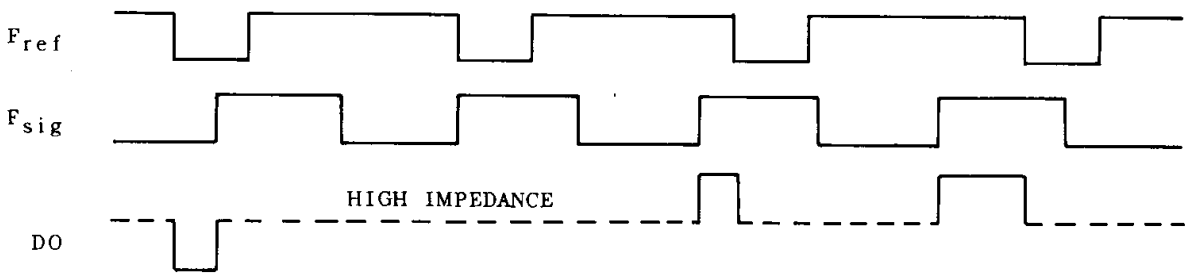
. The operation frequency range of VCO is 0.5~4MHz.

. Frequency which is obtained by VCO becomes control signal (CP) of AFC, APC loop in next step.

(2) Phase comparator output terminal (F_{sig}, F_{ref}, DO)

. Phase comparator detects the input pulse difference, and outputs at DO the positive and the negative pulses proportioned with the phase difference.

PHASE COMPARATOR TIMING CHART



. F_{ref} terminal is reference signal input terminal of APC/AFC loop control signal (CP), the motor speed (the number of FG pulses of motor) is decided by it.
The relations between FG, F_{ref} and FG is as follows;

$f_x(CP)=2560 \times F_{ref}[Hz]$: Relation between Fref and control signal (CP)

$f_x(CP)=20 \times 128 \times FG[Hz]$: Relation between FG and control signal (CP)

$\therefore$ This relation becomes "$FG=F_{ref}[Hz]$"

. F_{ref} input terminal is a C-MOS structure.

. F_{sig} output terminal is output comparison signal of phase comparator.

2. APC/AFC Loop

(1) FG pulse input terminal (FG_{IN})

. This is the input terminal of FG pulse for indicating the motor speed, and this signal becomes the comparison frequency of internal PLL.

. Since the amplifier and the Schmitt circuit are incorporated, operation is made with the small amplitude through the coupling capacitor.

(2) Output terminals (APC, AFC) of phase control system (APC) and speed control system.

. AFC is F-V converter against FG_{IN} frequency and is fabricated with 8-bit D/A converter.

. APC is the phase comparator (ϕ-V converter) for comparing the phase difference ϕ between $\frac{1}{2}$FG signal and the reference signal FS', and is also fabricated with 8-bit D/A converter.
(Note) $FS' = \frac{1}{2} FS$

. Both APC and AFC perform three kinds of operations described below.

a) When FG_{IN} frequency is within the lock range, both APC and AFC perform the normal operation against FG_{IN}.
Against the reference synchronization FS, the lock range is
at LW="L", +9.3%, -10.6% (about ±10%)
at LW="H", +4.6%, -5.3% (about ±5%)
(Note) Reference frequency $FS = \frac{f_{x(CP)}}{20 \times 128}$ [Hz]

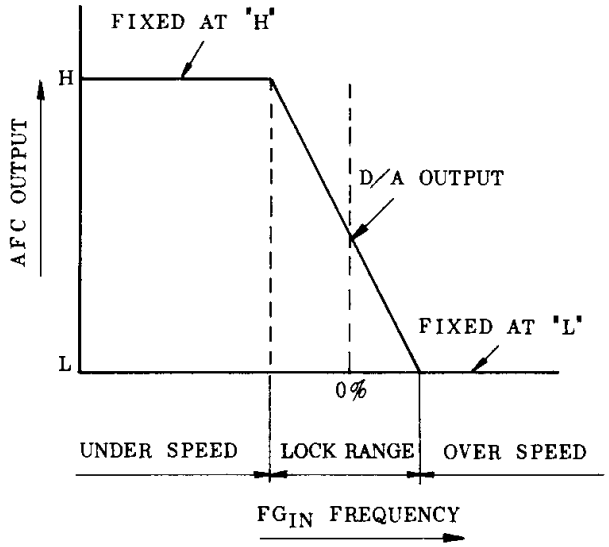
b) When FG_{IN} frequency is under the lock range (under speed), the outputs of APC and AFC are fixed at "H" level.

c) When FG_{IN} frequency is over the lock range (over speed), the outputs of APC and AFC are fixed at "L" level.

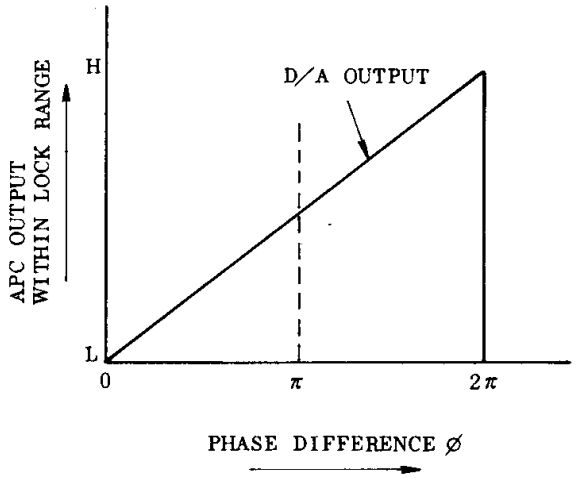
. When the motor is in STOP state (R/S=H or Open), both the outputs of AFC and APC are fixed at "L" level.

. Bipolar transformer is incorporated at the output stage of both APC and AFC.

CHANGE OF APC OUTPUT
AGAINST FG_{IN} FREQUENCY

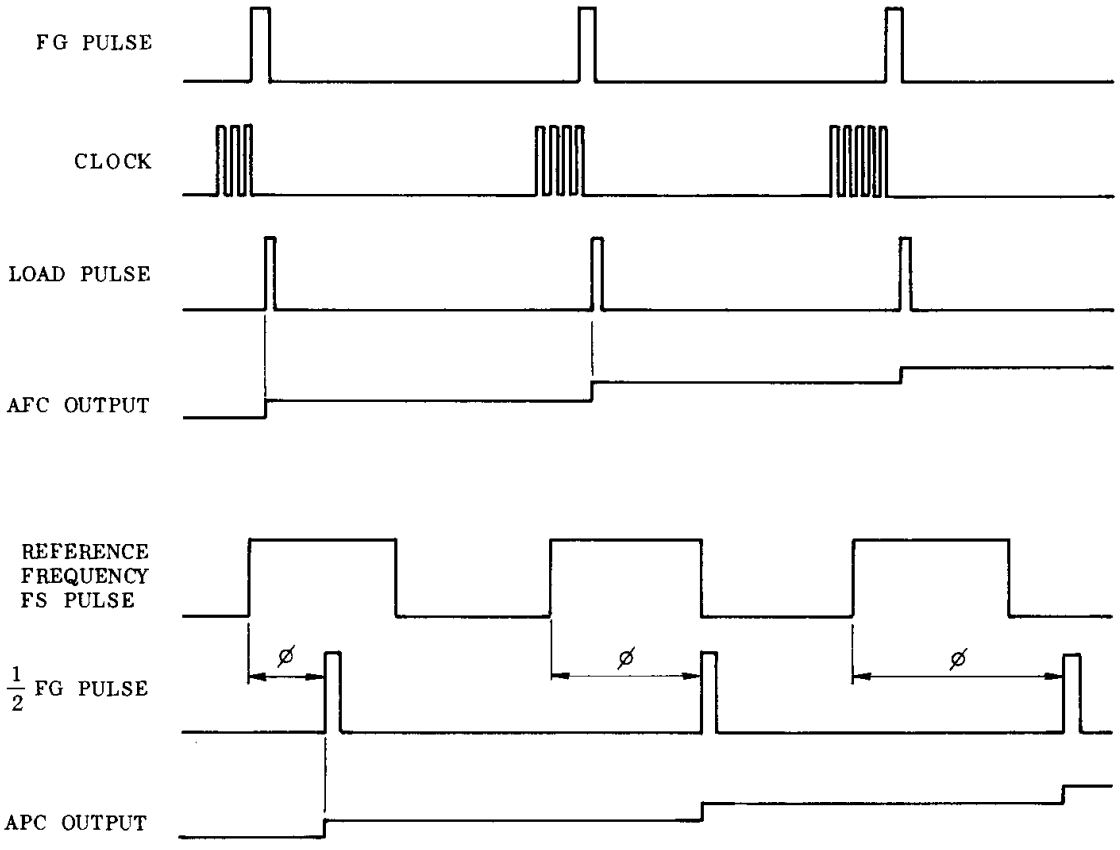


CHANGE OF APC OUTPUT
AGAINST PHASE DIFFERENCE ϕ



. Timing charts of AFC and APC within lock range

a. AFC (speed control system)



(3) Output terminal for reference voltage generation (V_{RO})

. V_{RO} is the transistor output terminal for the reference voltage of the operational amplifier which controls the motor by means of synthesizing the outputs of APC and AFC.

. V_{RO} is fixed at $\frac{1}{2} V_{DD} - V_F$ internally through dividing the resistance, and the output is fabricated into bipolar transistor construction.

(4) Lock range switching input terminal (LW)

. This is the terminal for switching the lock range of APC and AFC, and two kinds of lock ranges can be selected through operating this terminal.

at LW="H", normal lock range (±5%)

at LW="L", double lock range (±10%)

(5) RUN/STOP input terminal (R/S)

. RUN/STOP signals of motor are input. RUN="L", STOP="H" or open

. During RUN(R/S=L), APC, AFC and LD perform the normal operation against FG_{IN} frequency. During STOP(R/S=H or Open), APC, AFC and LD are all fixed at "L" level.

. Pull-up resistance and chattering prevention circuit are incorporated.

(6) Lock detection terminal (LD)

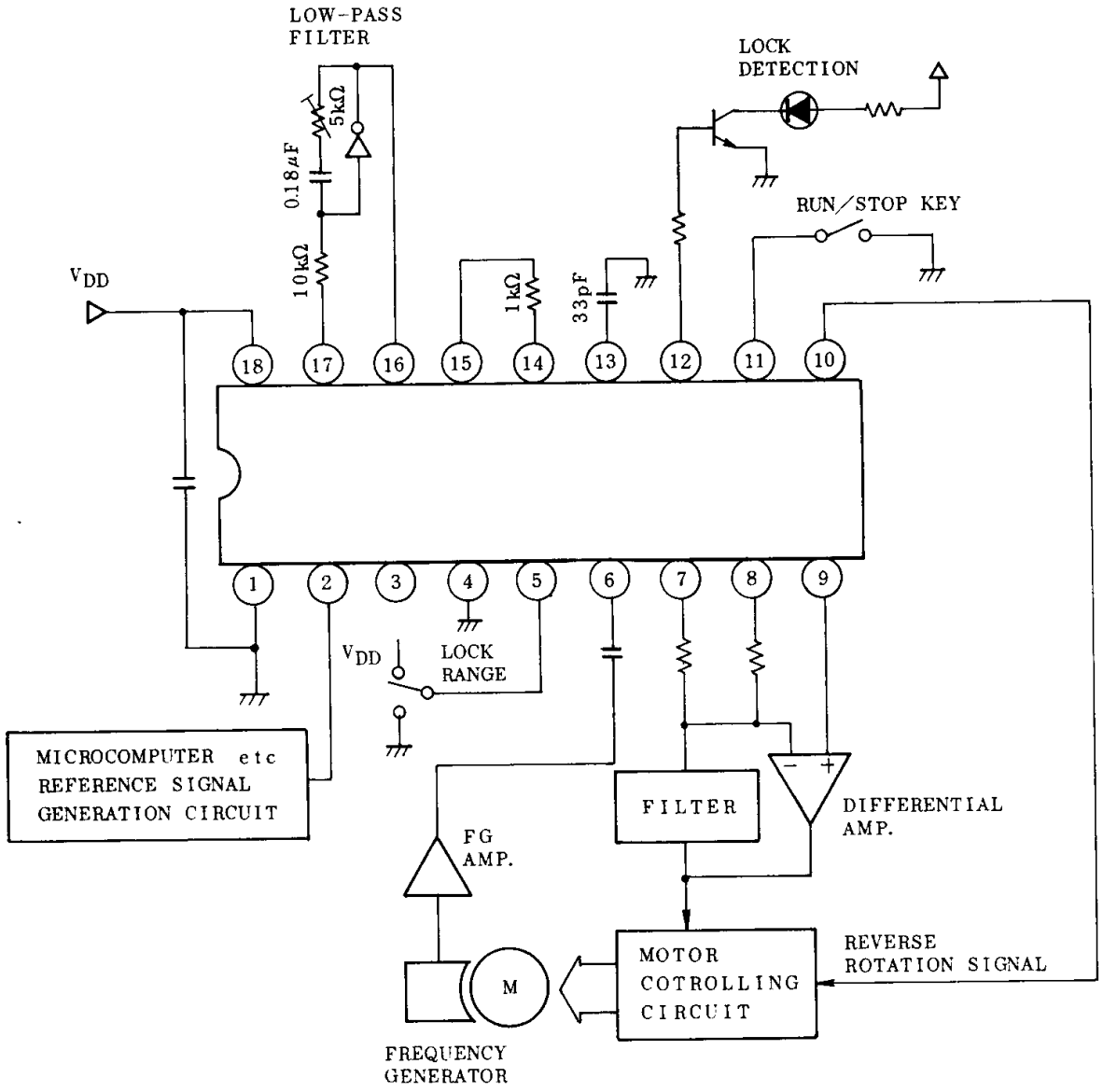
This is the output terminal for lock detection. When FG_{IN} frequency is within lock range, the terminal is at "H" level, and in other cases, at "L" level.

(7) Reverse rotation signal output terminal (RV)

. RV is the reverse rotation signal output for applying the brake to the motor when the motor is changed to STOP state.

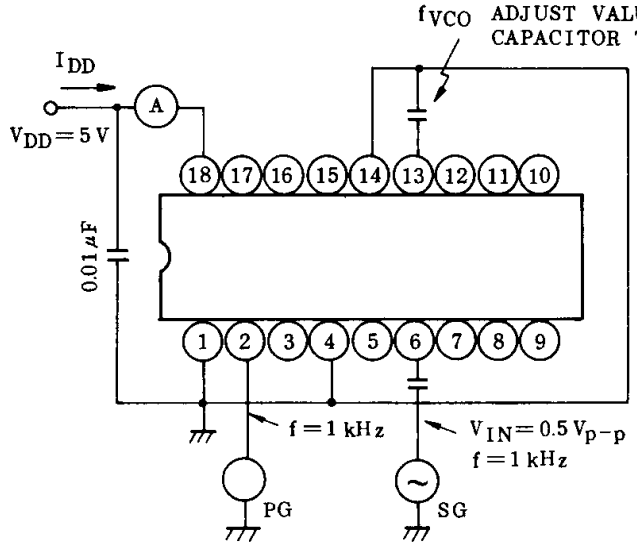
. When STOP state is turned out, RV becomes "H" level, and when the frequency of FG_{IN} becomes below $\frac{1}{8}$ FS, "L" level. In other cases, RV is fixed at "L" level.

EXAMPLE OF APPLICATION CIRCUIT (Pin connect is TC9192P)

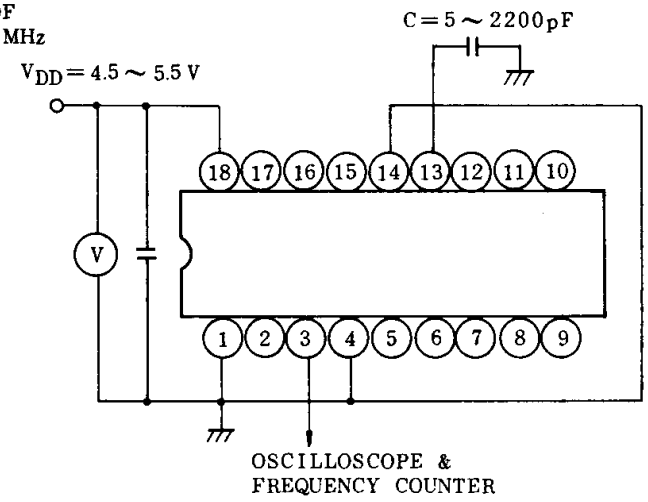


CHARACTERISTIC TEST CIRCUIT (Pin connect is TC9192P)

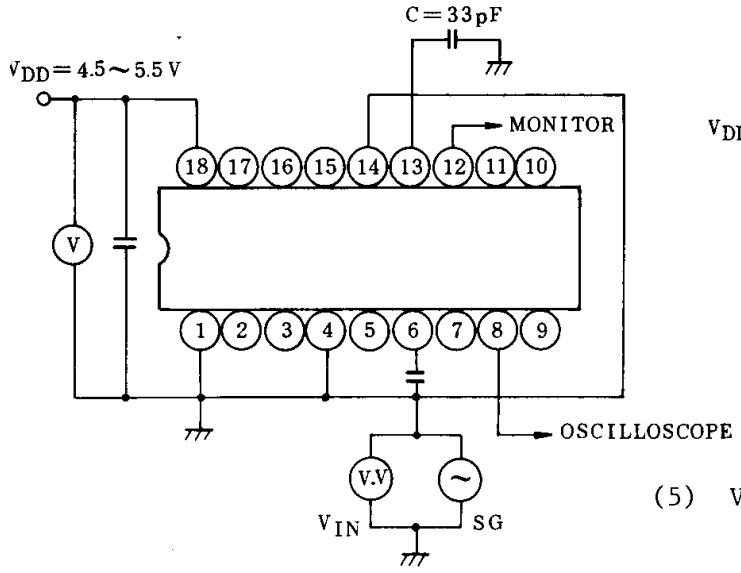
(1) Operating Supply Current (I_{DD})



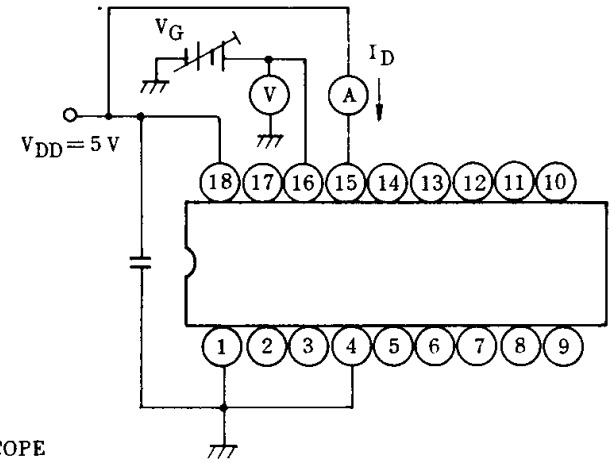
(2) VCO Operating Frequency Range (f_{VCO})



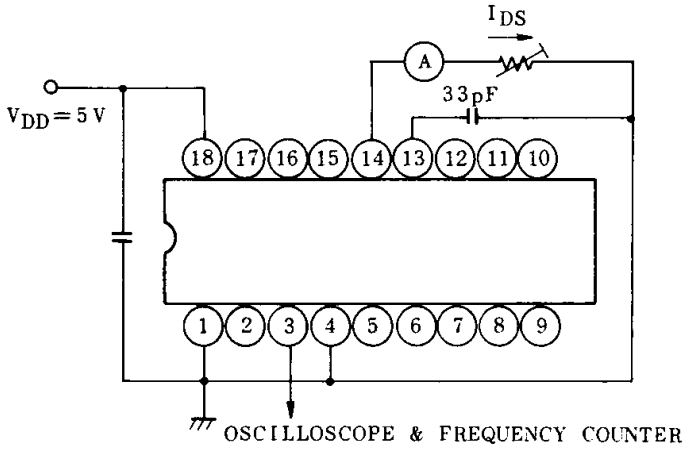
(3) FG_{IN} Input Sensitivity



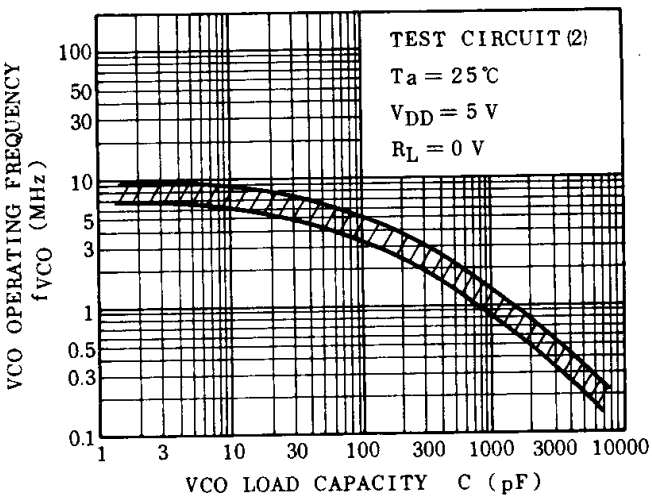
(4) Nch Open Drain Current (I_D)



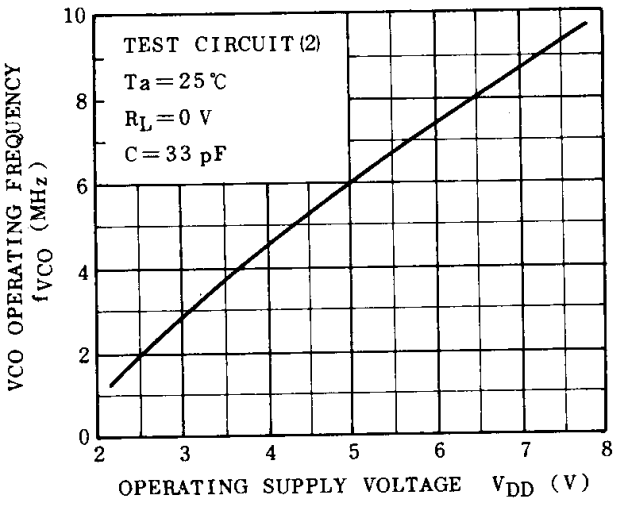
(5) VCO Operating Frequency Range (2) (f_{VCO})



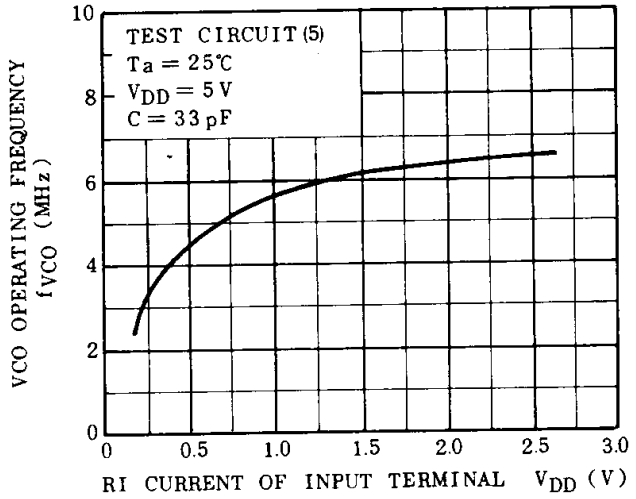
C – f_{VCO}



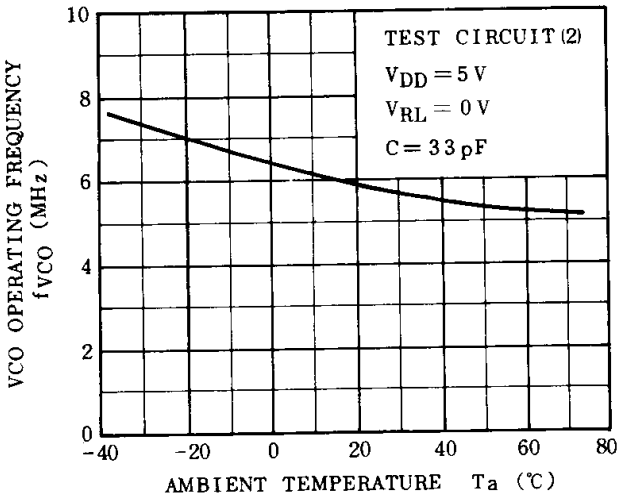
V_{DD} – f_{VCO}



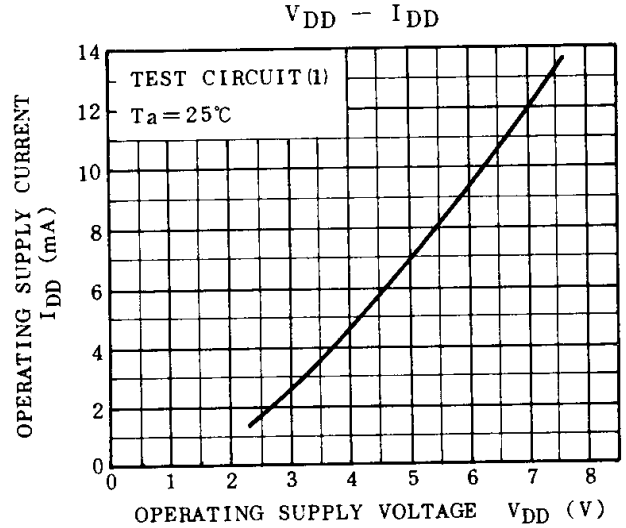
I_{DS} – f_{VCO}



Ta – f_{VCO}



V_{DD} – I_{DD}



V_G – I_D