TC9134P

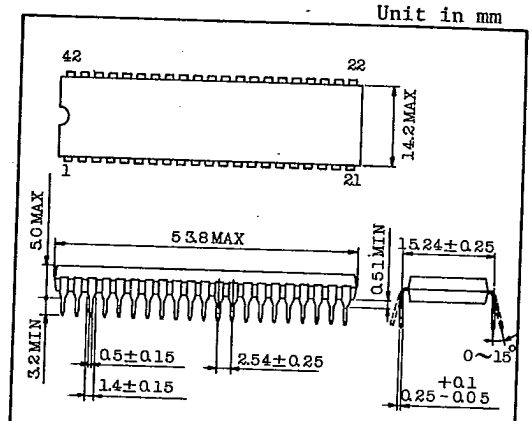
TC9134P 32-FUNCTION REMOTE CONTROL RECEIVING LSI

TC9134P is an LSI designed for use in a receiver of an infrared ray remote control system, and a multifunction remote control system can be composed in combination with TC9132P and LSI for a transmitter.

It is possible to control 32 functional instructions through the remote control and 3 functional instructions directly by the key.

- As decorder is built in and 30 functional instruction are transmitted in parallel, external parts are minimized.
- D/A converter is built in.
- Code detection circuit provided for code check with the transmitter prevents interferences from various types of machines and apparatus.
- LC (or ceramic) oscillation circuit is built in.
- Operating voltage: 4.0 ∿ 6.0V.

Unit in mm



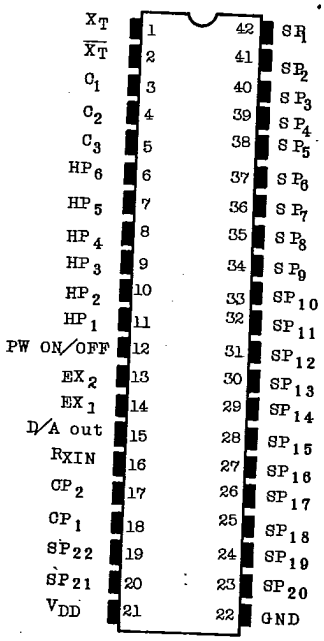
Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No. 42 leads.

JEDEC	—
TOSHIBA	6D42A-P

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	0 ∿ 7	V
Input Voltage	V_{IN}	-0.3 ∿ V_{DD}+0.3	V
Output Voltage	V_{OUT}	0 ∿ V_{DD}	V
Power Dissipation	P_D	600	mW
Operating Temperature	T_{opr}	-30 ∿ 70	°C
Storage Temperature	T_{stg}	-55 ∿ 125	°C

PIN CONNECTIONS



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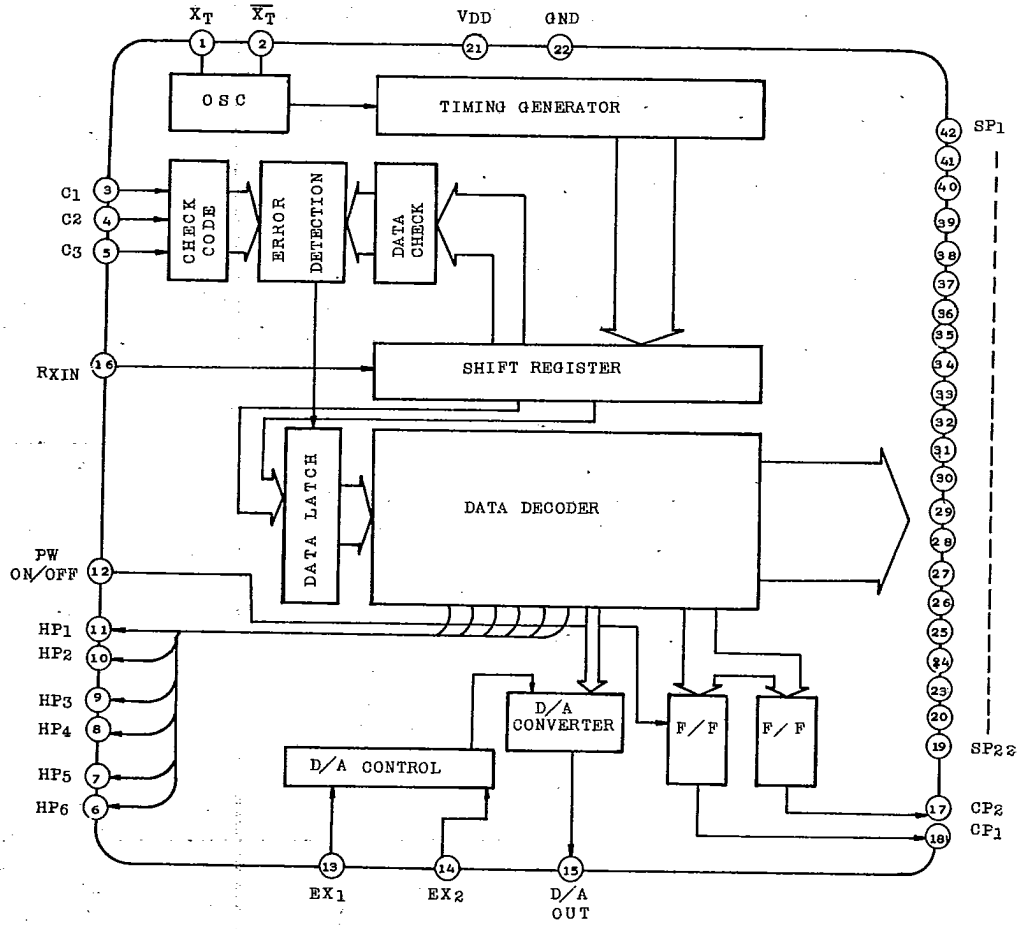
BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V_{DD} = 5.0 V and Ta = 25°C.)

CHARACTERISTIC				SYMBOL	TEST CIRCUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage				V_{DD}	-	-		4.0	-	6.0	V
Supply Current				I_{DD}	-	V_{DD} =6.0V		-	-	8.0	mA
Inputs	$C_1 \sim C_3$ EX_1 ~ EX_2 PW	Input Voltage	"H" Level	V_{IH}	-	-		3.5	-	-	V
			"L" Level	V_{IL}	-	-		-	-	1.5	V
	C_1 ~ C_3	Input Current	"H" Level	I_{IH}(C)	-	V_{DD}=6.0V	V_{IH}=6.0V	-	-	1.0	µA
			"L" Level	I_{IL}(C)	-		V_{IL}=0V	1.0	-	-	µA
	EX_1 ~ EX_2 PW	Input Current	"H" Level	I_{IH}	-		V_{IH}=6.0V	-	-	1.0	µA
			"L" Level	I_{IL}	-		V_{IL}=0V	-1000	-	-100	µA
SP, CP Outputs	SP_1 ~ SP_{22} HP_1 ~ HP_6	Output Current	"H" Level	I_{OH}	-	V_{OH}=4.0V		-	-	-0.5	mA
			"L" Level	I_{OL}	-	V_{OL}=1.0V		0.5	-	-	mA
	CP_1 ~ CP3	Output Current	"H" Level	I_{OH}	-	V_{OH}=4.0V		-	-	-0.5	mA
			"L" Level	I_{OL}	-	V_{OL}=1.0V		5.0	-	-	mA
D/A Error				-	-	-		-	-	1	LBS
Oscillator Frequency				f_{osc}	-	-		400	-	600	kHz

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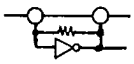
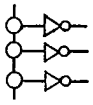
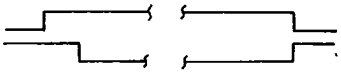
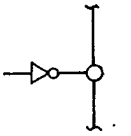
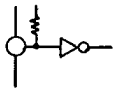
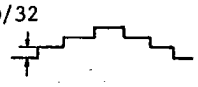
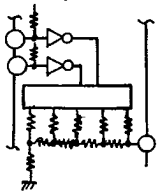
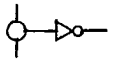
PIN DESCRIPTION

PIN NO.	SYMBOL	FUNCTIONAL DESCRIPTION	INPUT/OUTPUT CONFIGURATION
1,2	X_T, $\overline{X}_T$	Timing oscillator terminal 455 kHz ceramic oscillator or L, C oscillation circuit is connected.	
3 ∿ 5	C_1, C_2, C_3	Code designation input If the transmitter code and a code set at this pin are identical when compared, input is accepted.	
6 ∿ 11	HP_6 ∿ HP_1	Continuous signal output While receiving signal is being input, this output is kept at "L" level. In transmission HP_1 ∿ 6 	
12	PW on/off	External control input for cyclic output CP_1 CP_1 can be controlled not only from the transmitter but also from the receiver. CP_1 is reversed at "L" level.	
13 ∿ 15	EX_1 EX_2 D/A out	External control input for D/A converter Operation is started at "L" level when EX_1 is turned up and when EX_2 is turned down. D/A converter output $V_{DD}/32$  V_{DD} is divided into 32 portions and is output.	
16	R_X IN	Receiving signal input An instruction signal with a carrier signal eliminated is input.	

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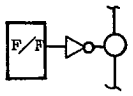
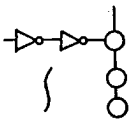
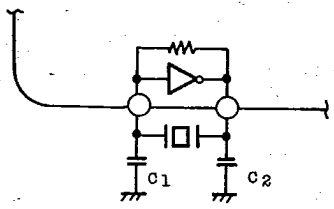
PIN NO.	SYMBOL	FUNCTIONAL DESCRIPTION	INPUT/OUTPUT CONFIGURATION
17 18	CP_2 CP_1	Cyclic signal output When a signal is received, output is reversed. CP_1 can also be controlled from a receiving IC.	
19 20 23∿42	SP_{22}∿SP_1	Single-shot signal (single pulse) output When an instruction signal is received, designated output of "L" level pulse only is transmitted. About 140 ms	
21,22	V_{DD},GND	Supply voltage applying terminal	

OPERATIONAL DESCRIPTION

1. OSCILLATION CIRCUIT

All timings, such as timing with the transmitter, D/A converter clock, interval operating clock, are decided by frequencies generated by this oscillator. 455 kHz is used as the standard frequency.

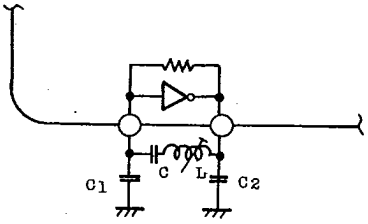
The oscillation circuit has the built-in linear amplifier with a C-MOS inverter, and an oscillator can be easily constructed by connecting a 455 kHz ceramic oscillator to X_T and $\overline{X}_T$ pins. In addition, an oscillation circuit using L, C circuit also can be composed.



Example using ceramic oscillator

Ceramic KBR-455B (Kyoto Ceramics)

C_1, C_2 50 ∿ 150pF



Example using L, C circuit

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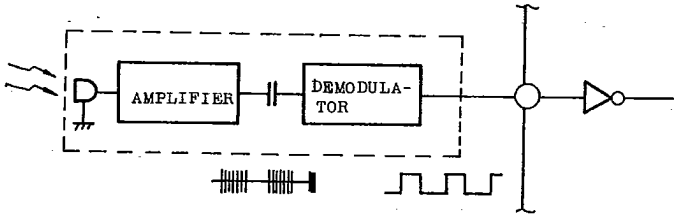
2. RECEIVED SIGNAL INPUT CIRCUIT

A signal received by the light receiving element is amplifierd by the linear amplifier and input after a carrier signal has been eliminated. In this case, care should be taken not to create change in duty and non-linear waveform due to the demodulation circuit.

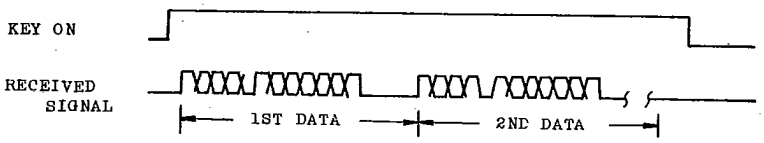


3. CHECKING OF RECEIVED SIGNAL

Received signal is strictly checked to ascertain if it is a normal signal or a code is correct.
There are some differences in the methods of checking single pulse and continuous signal.

3-1) Checking of single-shot signal

Transmission of single-shot signal will end after the same signal has been transmitted in two cycles as illustrated below.



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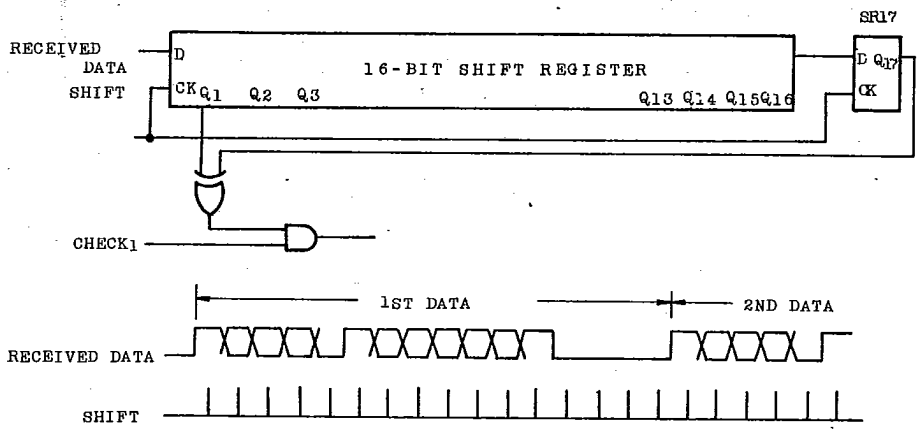
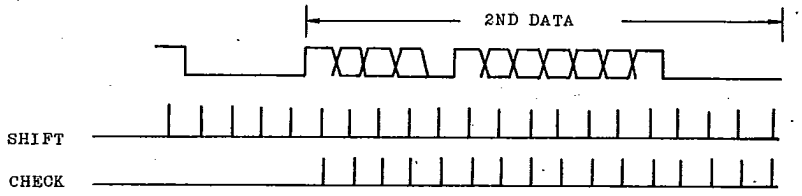


First, the 1st data is stored in the 16-bit shift register by the shift signal. When the 2nd data is transferred to the shift register by the shift signal, the 1st bit data of the 1st data is forced out to SR_{17}. Whenever the 1st data and the 2nd data are the normal data, the 1st bit output Q_1 of the shift register and the output from SR_{17} would be the same data at all times.



Accordingly, Q_1 of the 16-bit shift register and output Q_{17} from SR_{17} are compared by $check_1$ signal.

Since this check signal is transmitted 16 times, all the data (16 bits) of the 1st and the 2nd data are thoroughly checked.

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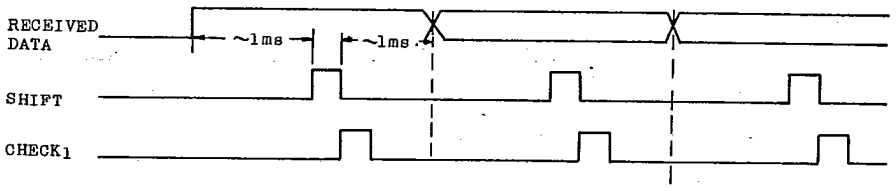
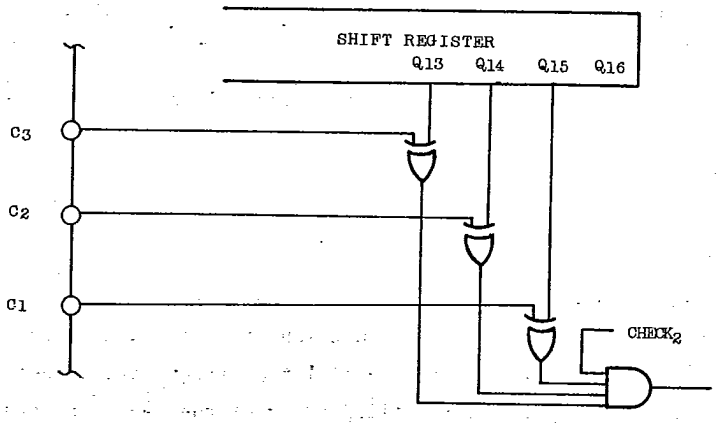
With due consideration of frequency margins of the transmitter and receiver oscillators, the shift signal is in such a timing as shown below.



Code Comparison

When the comparison of all 16-bit data is completed, the code comparison is executed. At the time when the comparison of all 16-bit data is completed, the 2nd data is kept stored in the shift register and the code data are available at $Q_{13} \sim Q_{15}$.



Thus, the codes at C_1, C_2 and C_3 terminals and the outputs from $Q_{13} \sim Q_{14}$ are compared by Check 2 (16th Check 1) signal.

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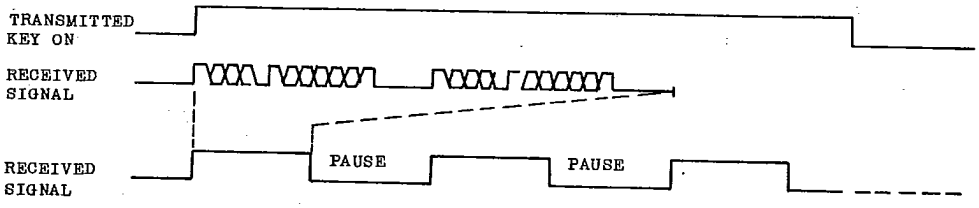
Error Signal and End Signal

When error is detected by either the 16-bit data check or code chek, an error signal is generated at that point of time and the system is reset.

On the contrary, when everything is OK, an end signal is generated. Data receiving is validated by this end signal, and output from the data decoder begins to operate.

3-2) Checking of continuous signal

Continuous signal is transmitted at intervals of 2-cycle output and 2-cycle pause as illustrated below.



Continuous signal is checked as in single-shot signal. During the period of pause, the check is also stopped and resumed when data is again transferred.

3-3) Timing reset

Received signal is checked by a signal generated in the timing circuit by frequency of the oscillation circuit, Shift Check$_1$ and Shift Check$_2$, etc. However, to give a margin to oscillation frequency, a reset signal is generated at the rising and falling edges of the received data to reset the timing circuit, thus constantly synchronizing with the received signal.

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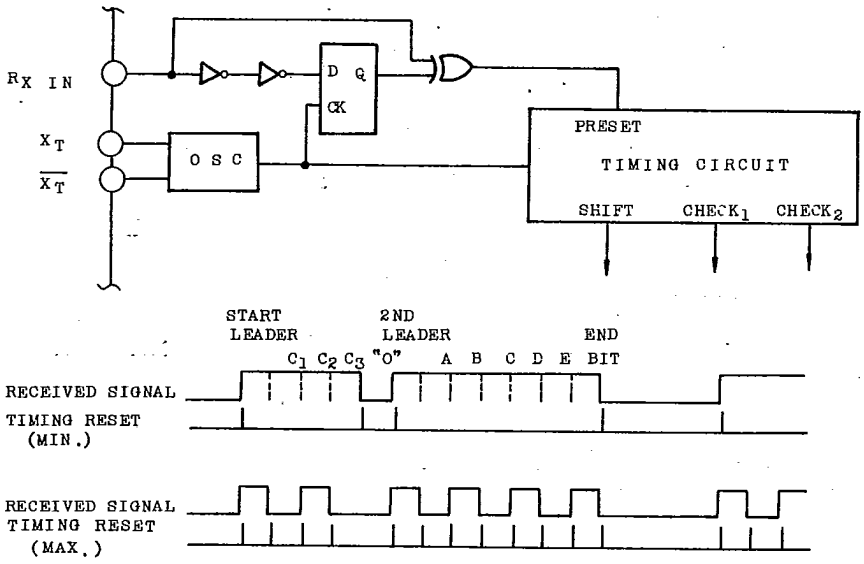

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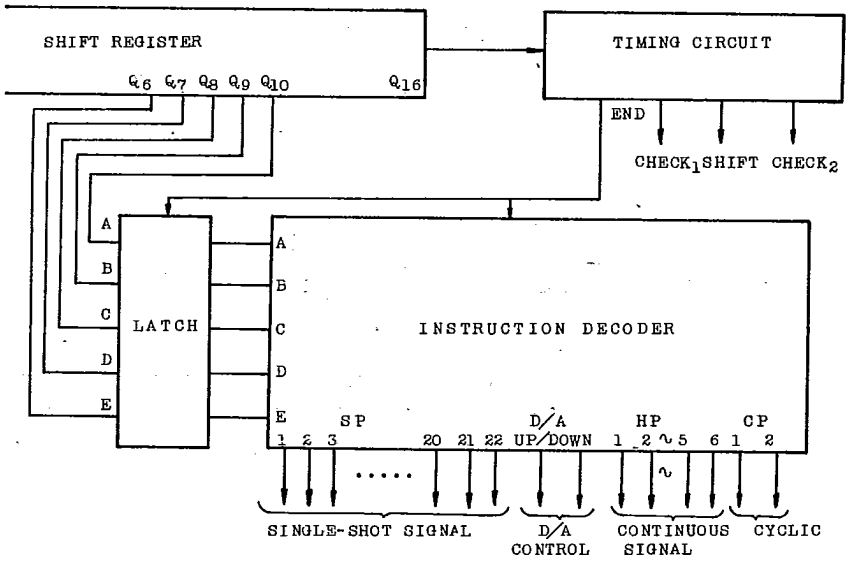
4. INSTRUCTION DECODER

If no error is detected in the above checking of recieved signal, an end signal is generated to actuate the decoder for execution of instructions.



The instruction decoder decodes data bits A ∿ E into.

- o For single-shot signal — 32 instructions
- o For continuous signal — 6 instructions
- o For D/A control (up/down) — 2 instructions
- o For cyclic signal — 2 instructions

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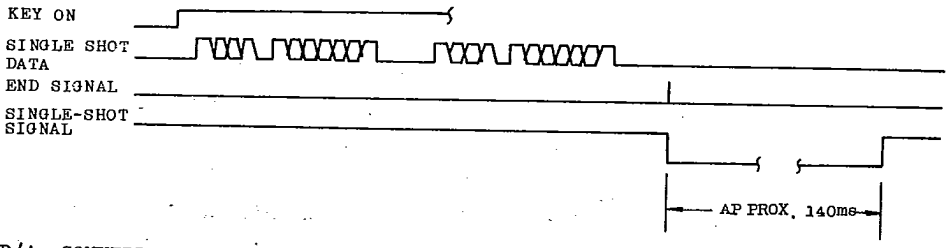
DATA BIT A	B	C	D	E	INSTRUCTION FUNCTION	DATA BIT A	B	C	D	E	INSTRUCTION FUNCTION	DATA BIT A	B	C	D	E	INSTRUCTION FUNCTION
0	0	0	0	0	Single-shot signal SP 1	1	1	0	1	0	Single-shot signal SP 12	0	0	1	0	1	D/A up
1	0	0	0	0	" 2	0	0	1	1	0	" 13	1	0	1	0	1	D/A down
0	1	0	0	0	" 3	1	0	1	1	0	" 14	0	1	1	0	1	Continuous signal HP 1
1	1	0	0	0	" 4	0	1	1	1	0	" 15	1	1	1	0	1	" 2
0	0	1	0	0	" 5	1	1	1	1	0	" 16	0	0	0	1	1	" 3
1	0	1	0	0	" 6	0	0	0	0	1	" 17	1	0	0	1	1	" 4
0	1	1	0	0	" 7	1	0	0	0	1	" 18	0	1	0	1	1	" 5
1	1	1	0	0	" 8	0	1	0	0	1	" 19	1	1	0	1	1	" 6
0	0	0	1	0	" 9	1	1	0	0	1	" 20	0	0	1	1	1	Cyclic signal CP 1
1	0	0	1	0	" 10	0	1	1	1	1	" 21	1	0	1	1	1	" 2
0	1	0	1	0	" 11	1	1	1	1	1	" 22						

5. SINGLE-SHOT SIGNALS $SP_1 \sim SP_{22}$

Single-shot signal is a single pulse output, falls at the end signal and rises after approx. 140ms.



6. D/A CONVERTER CIRCUIT

6-1) TC9134P has a built-in 3-circuit, 5-bit, D/A converter.

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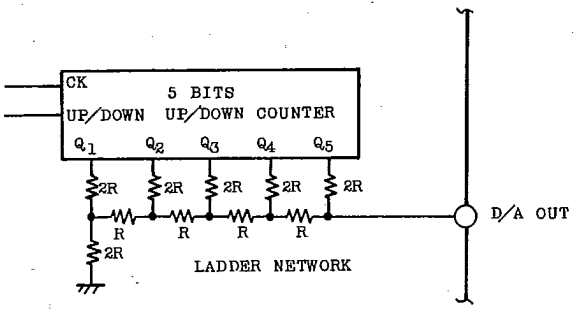
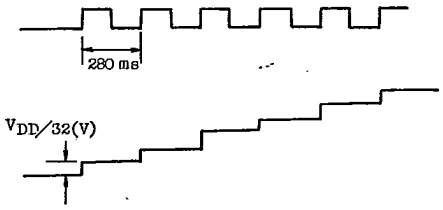


6-2) The clock from the up/down counter is approx. 280 msec when the frequency generated from the oscillator is 455 kHz,



6-3) The up/down control of this D/A converter is as shown below according to the above-mentioned instruction decoder output:

A	B	C	D	E	
0	0	1	0	1	D/A UP
1	0	1	0	1	D/A DOWN

6-4) The D/A converter is capable of controlling up/down directly by the key. The external input pins EX_1 and EX_2 are the up/down controllers of the D/A converter.

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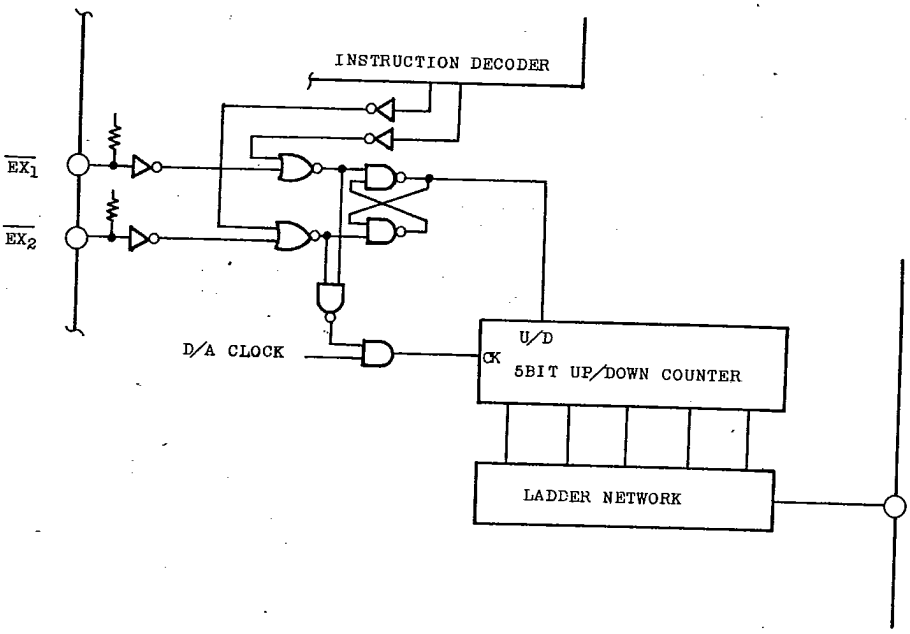
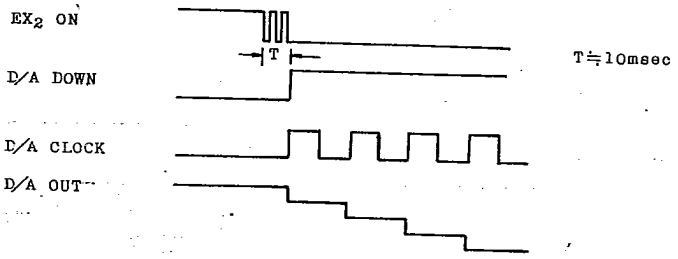


The chattering prevention circuit is provided in the EX input unit to prevent malfunction due to noise and switch chattering.



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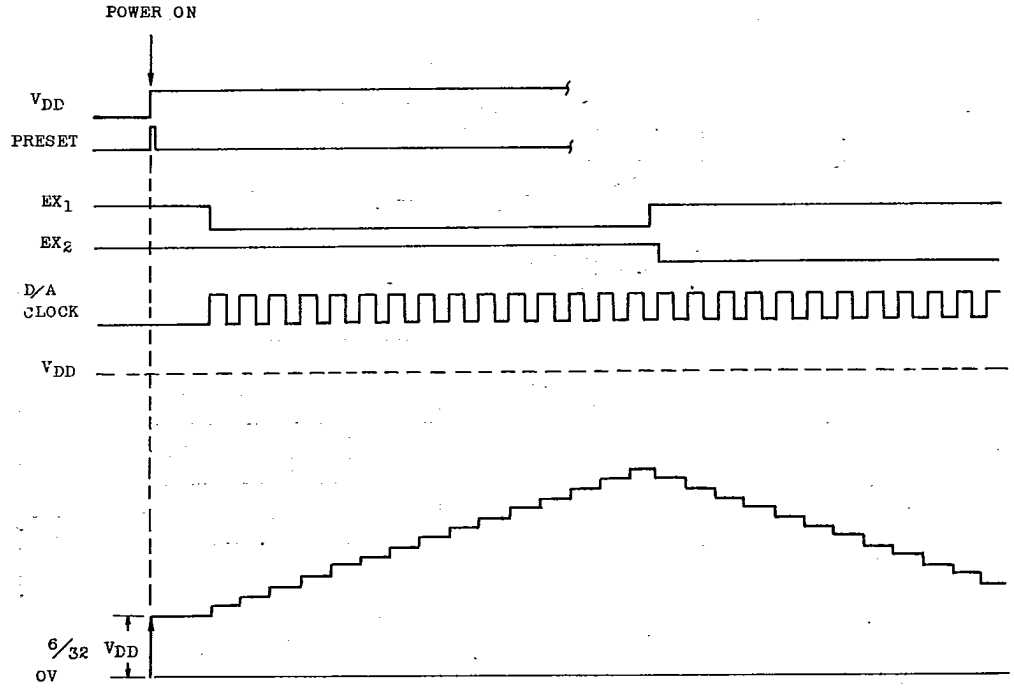
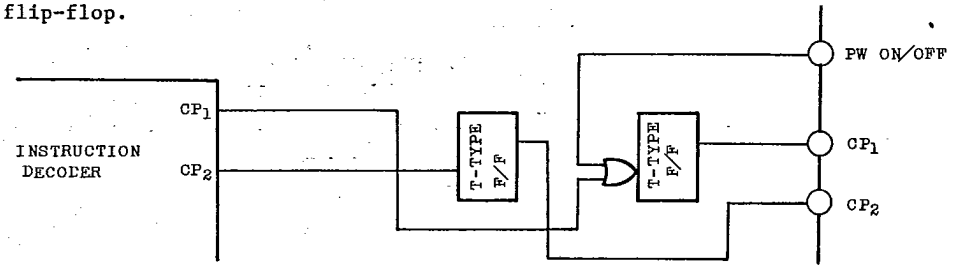


7. CYCLIC SIGNALS (CP_1, CP_2)

Cyclic signal is a signal by which output is inverted when it is received. Data from the instruction decoder is inverted by the T-type flip-flop.



Further, CP_1 can be inverted through the external input key PW ON/OFF, and is used for the power ON/OFF.

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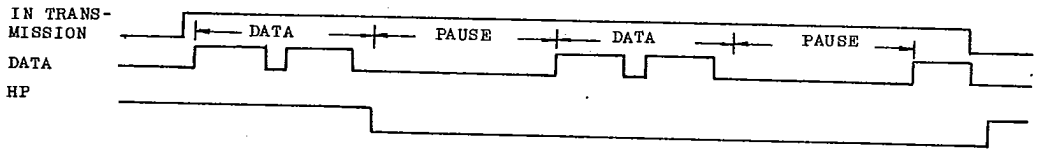
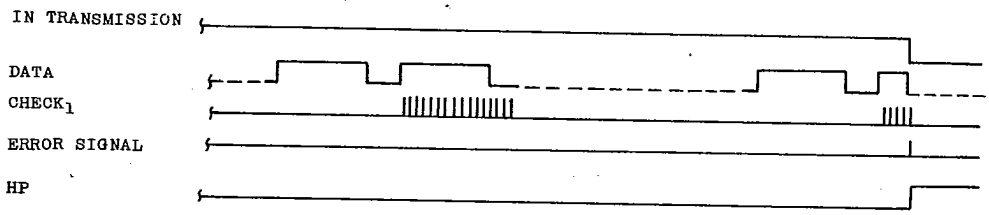
8. CONTINUOUS SIGNAL

Continuous signal is kept at "L" level during the period when it is being transmitted from the transmitter.



Similar to the single-shot signal, output timing of the continuous signal is such that it is inverted to "L" level when an end signal is generated after the checking of 16 bits of the 2nd data of the 1st data has been completed, and it becomes error when the first $Check_1$ signal for the second data of next data is generated after the transmission has stopped, and then, it is inverted to "H" level.



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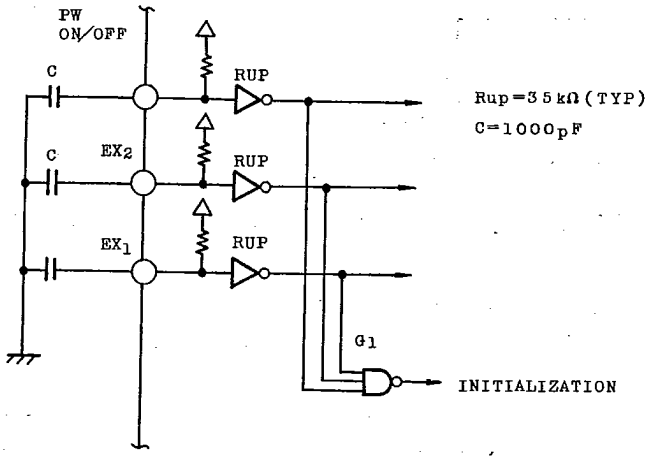
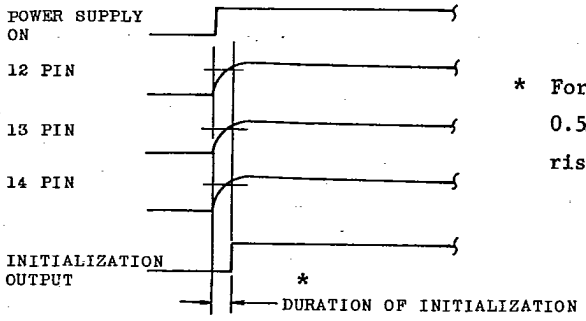
INITIALIZATION AT TIMER OF POWER ON

When power is turned on, it is necessary to initialize the system for initialization of the internal state and presetting of the D/A converter.

This initialization can be executed by simultaneously setting 3 terminals of 12 Pin, 13 Pin and 14 Pin at time of the power ON.
That is, the initialization is executed when capacitors are connected to 12 Pin, 13 Pin and 14 Pin.



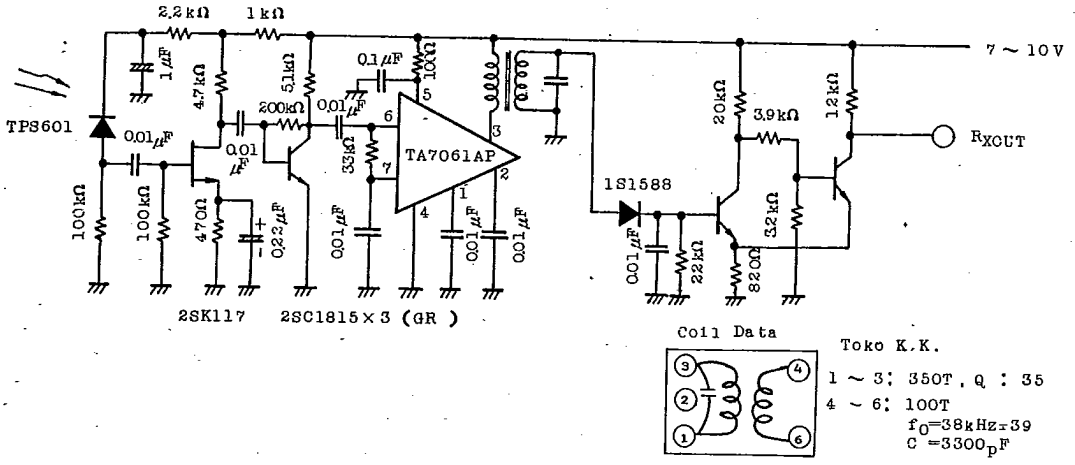


* For the duration of initialization, 0.5 msec or above is required after rising of the supply voltage (V_{DD}).

TC9134P

T-77-11

EXAMPLE IF APPLIED CIRCUIT AT RECEIVING UNIT



Coil Data

Toko K.K.

1 ~ 3: 350T, Q : 35
4 ~ 6: 100T
f_0=38kHz±3%
C =3300pF