SC473
Single-Phase Single Chip Graphics Core Power Supply

POWER MANAGEMENT

Description

The SC473 is a single-phase chip, high-performance PWM controller designed to power advanced graphic cores. On-chip support is provided that includes slew-rate controlled VID transitions.

The SC473 implements hysteretic control technology which provides the fastest possible transient response while avoiding the stability issues inherent to classical PWM controllers. Eliminating the sense resistors reduces costs and PCB area, plus increases system efficiency. Integrated SmartDriver™ technology initially turns on the high-side driver with 'soft' drive to reduce ringing, EMI, and capacitive turn-on of the low side MOSFET, while also increasing overall efficiency.

Hysteretic operation adaptively reduces the SC473 switching frequency at light loads. Combined with an automatic "powersave" mode which prevents negative current flow in the low-side FET, system efficiency is significantly enhanced during light loading conditions.

A 5-bit DAC, accurate to 0.85%, sets the output voltage reference, and implements the voltage range required by the processor. The DAC slew rate is externally programmed to minimize transient currents and audible noise. True differential remote sensing provides accurate point-of-load regulation at the processor die. Other features include programmable soft-start, an open-drain PWRGD output, dual-level over-voltage and programmable over-current protection. The SC473 is available in a space-saving 4x4mm, 24-pin MLP package.

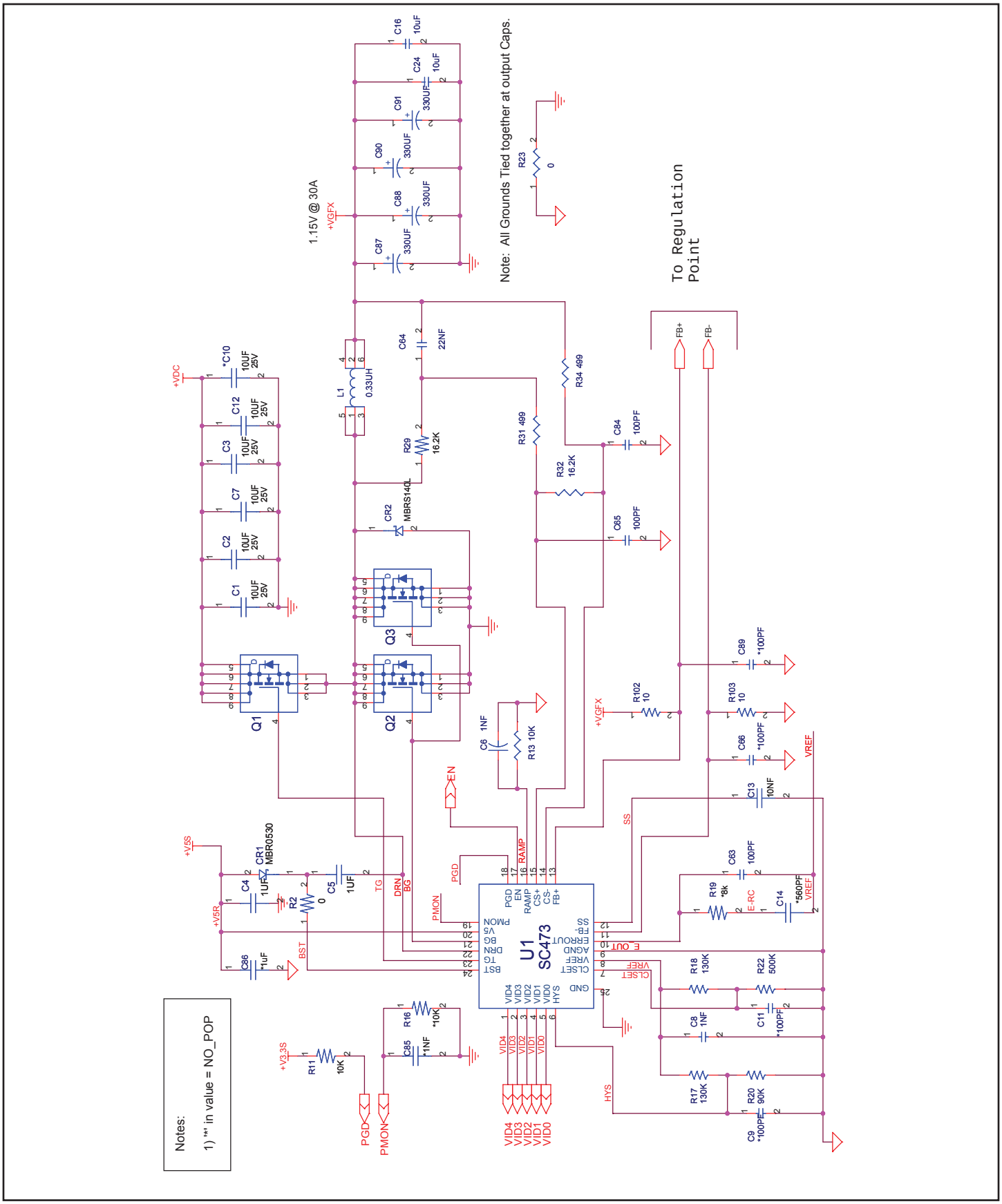
Features

- Single-Phase Solution with Integrated Drivers
- Hysteretic Control for Fast Transient Response
- SmartDriver™ for reduced EMI
- True Differential Remote (die) Sensing
- VID Programmed Voltage
- Delayed Power Good Signal with Blanking
- Programmable Soft-Start and DAC Slew Control
- Programmable OCP Threshold
- Supports all Ceramic Decoupling Solutions
- 24-Pin MLP (4x4)
- Lead-Free Package
- RoHS and WEEE compliant

Applications

- High Performance Graphics
- Embedded Applications

Typical Application Circuit SC473



Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Condition	Min	Max	Units
Supply Voltage (V5)		-0.3	6.5	V
BST to PGND	Static	-0.3	30	V
	Transient <100ns	-0.3	34	V
BST to DRN		-0.3	6	V
DRN to PGND	Static	-2	25	V
	Transient <100ns	-5	29	V
TG to PGND		DRN, -0.3	BST, +0.3	V
BG to PGND		-0.3	V5, +0.3	V
All Other Pins to PGND		-0.3	VCCA +0.3	V
Thermal Resistance Junction to Ambient JESD51 Standard Method*	θ_{JA}		28	°C/W
Operating Junction Temperature Range	T_J	-40	125	°C
Storage Temperature Range	T_{STG}	-65	150	°C
Peak IR Reflow (10-40sec)	$T_{IRreflow}$		260	°C

*Calculated from package in still air, mounted to 3" x 4.5", 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

Electrical Characteristics

Unless otherwise specified, VccA = V5 = 5V, -40° < T_J < +125°C.

Parameter	Condition	Min	Typ	Max	Units
Control / Driver Supply (V5)					
V5 Operating Range		4.5	5.0	5.5	V
V5 UVLO	Rising	4.25	4.4	4.5	V
	Hysteresis Falling	50	150	250	mV
V5 Current	EN = L0			10	µA
	In UVLO		0.8	1.3	mA
	Operating (Static)		10	12	mA

Electrical Characteristics (Cont.)

Parameter	Condition	Min	Typ	Max	Units
Logic Inputs (EN, VID [4:0])					
Enable Threshold		0.8		2.0	V
VID [4:0] Threshold		0.45		0.55	V
Input Impedance			40		kΩ
Reference (DAC, SS, VREF), (0 < T_J <85°C)					
DAC Error + Internal Offset	1.15 - 0.85V	-0.85		+0.85	%
	0.825V - 0.5V	-7		7	mV
	0.475 - 0.375V	-14		14	mV
DAC Sink/Source Ability	0.3V < DAC < 1.5V	|50|			µA
SS Slew Current	Start-up and Operating	102	120	138	µA
	Discharge (SS = 0.5V)	15			mA
SS Discharge Threshold			50	400	mV
VREF Accuracy		1.97	2.00	2.03	V
VREF Sink/Source Ability		|1.5|			mA
Remote Sense (FB+, FB-)					
Bandwidth(1)		2			MHz
Error Amplifier (ERROUT)					
Gain			19		
Bandwidth(1)		2			MHz
Current Sensing (CS+, CS-)					
CS+, CS- Input Bias Current	CS+ = CS- = 1.5V			1	µA
Maximum Input Signal		50			mV
Zero-Crosssing Detector Threshold Powersave		-6		6	mV

Electrical Characteristics (Cont.)

Parameter	Condition		Min	Typ	Max	Units
Current Sensing (CS+, CS-) (Cont.)						
Low-Pass Filter Corner Frequency(1)			50	80	125	kHz
Current Limit Combined System (CLSET)						
CL System Accuracy	CLSET = 1.2V, TG Low		28		52	mV
	CLSET = 1.2V, TG High		16		32	
CLSET Input Bias Current					|1|	µA
Hysteresis Setting (HYS)						
HYS Input Bias Current					|1|	µA
HYS Gain (internal hysteresis setting relative to voltage applied at HYS pin)	HYS = 1V		4	7	10	%
OVP and Internal Powergood						
Fixed Over-Voltage Protection Threshold			1.65	1.7	1.75	V
Power Good Window Upper Threshold	FB Rising Relative DAC		+160	+200	+240	mV
Power Good Window Lower Threshold	FB Falling Relative DAC		-360	-300	-240	mV
Power Good Window Lower Hysteresis	FB Rising Relative DAC		30	50	70	mV
Powergood (PWRGD)						
Leakage	PWRGD High Impedance V_{PG} = 5V				1	µA
On-Resistance	PWRGD = 0.1V			20	100	Ω
Power Monitor						
PMON Output Voltage	VOUT = 1.2875 T_J = 25 °C	CS+, CS- = 4mV	74	148	222	mV
		CS+, CS- = 16mV	530	590	650	

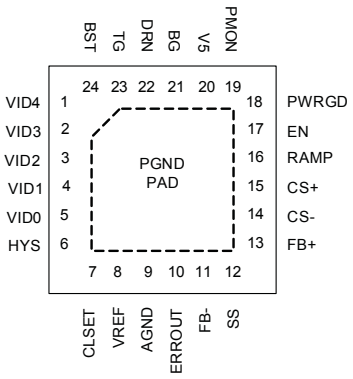
Electrical Characteristics (Cont.)

Parameter	Condition	Min	Typ	Max	Units
High-Side Driver (TG, BST, DRN)					
Peak Current(1)(2)		1.75	2.0	2.25	A
On-Resistance	R_{TG_UP}, DRN < 0.5V, 25°C	4.1	5.8	7.5	Ω
	R_{TG_UP}, DRN < 0.5V, -40 to 125°C	3.48	5.8	9.24	Ω
	R_{TG_UP}, DRN > 0.5V, 25°C	0.9	1.3	1.7	Ω
	R_{TG_UP}, DRN > 0.5V, -40 to 125°C	0.76	1.3	1.7	Ω
	R_{TG_DN}, at 25°C	0.42	0.6	0.78	Ω
	R_{TG_DN}, -40 to 125°C	0.34	0.6	1.01	Ω
Rise Time(1, 2)	C_{TG} = 3nF	17	22	27	ns
Fall Time(1, 2)	C_{TG} = 3nF	9	12	15	ns
Propagation Delay(1, 2)	From Hysteretic Comparator Inputs to Driver Output	30	45	60	ns
Shoot-thru Protection Delay(1)		10	20	30	ns
Lower-Side Driver (BG, V5, PGND)					
Peak Current(1, 2)		3.5	4.0	4.5	A
On-Resistance	R_{BG_UP} at 25°C	0.9	1.3	1.7	Ω
	R_{BG_UP} at -40° to 125°C	0.76	1.3	2.1	Ω
	R_{BG_DN} at 25°C	0.35	0.5	0.65	Ω
	R_{BG_DN} at -40° to 125°C	0.28	0.5	0.86	Ω
Rise Time(1, 2)	C_{BG} = 3nF	5	7	9	ns
Fall Time(1, 2)	C_{BG} = 3nF	2.5	3.5	4.5	ns

Notes:
(1) Guaranteed by design.
(2) T_J = 25 °C

POWER MANAGEMENT

Pin Configuration



SC473 Pin Out Diagram
Top View

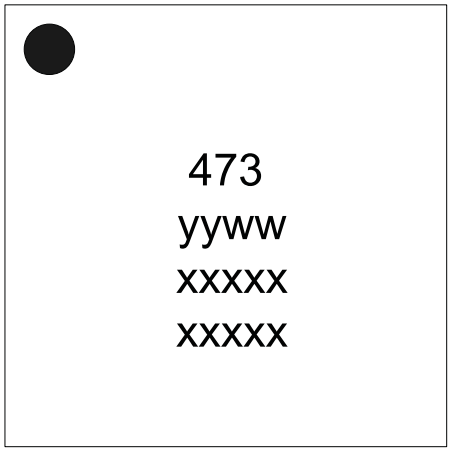
Ordering Information

Device[2]	Package	Temp Range (T_J)
SC473MLTRT [1][3]	MLP-4x4-24	-40°C to +85°C
SC473EVB	EVALUATION BOARD	

Notes:
1) Only available in tape and reel packaging. A reel contains 3000 devices.
2) This device is ESD sensitive. Use of standard ESD handling precautions is required.
3) Lead-free package compliant with J-STD-020B. Qualified to support maximum IR Reflow temperature of 260°C for 30 seconds. This product is fully WEEE and RoHS compliant.

Marking Information

TOP MARKING

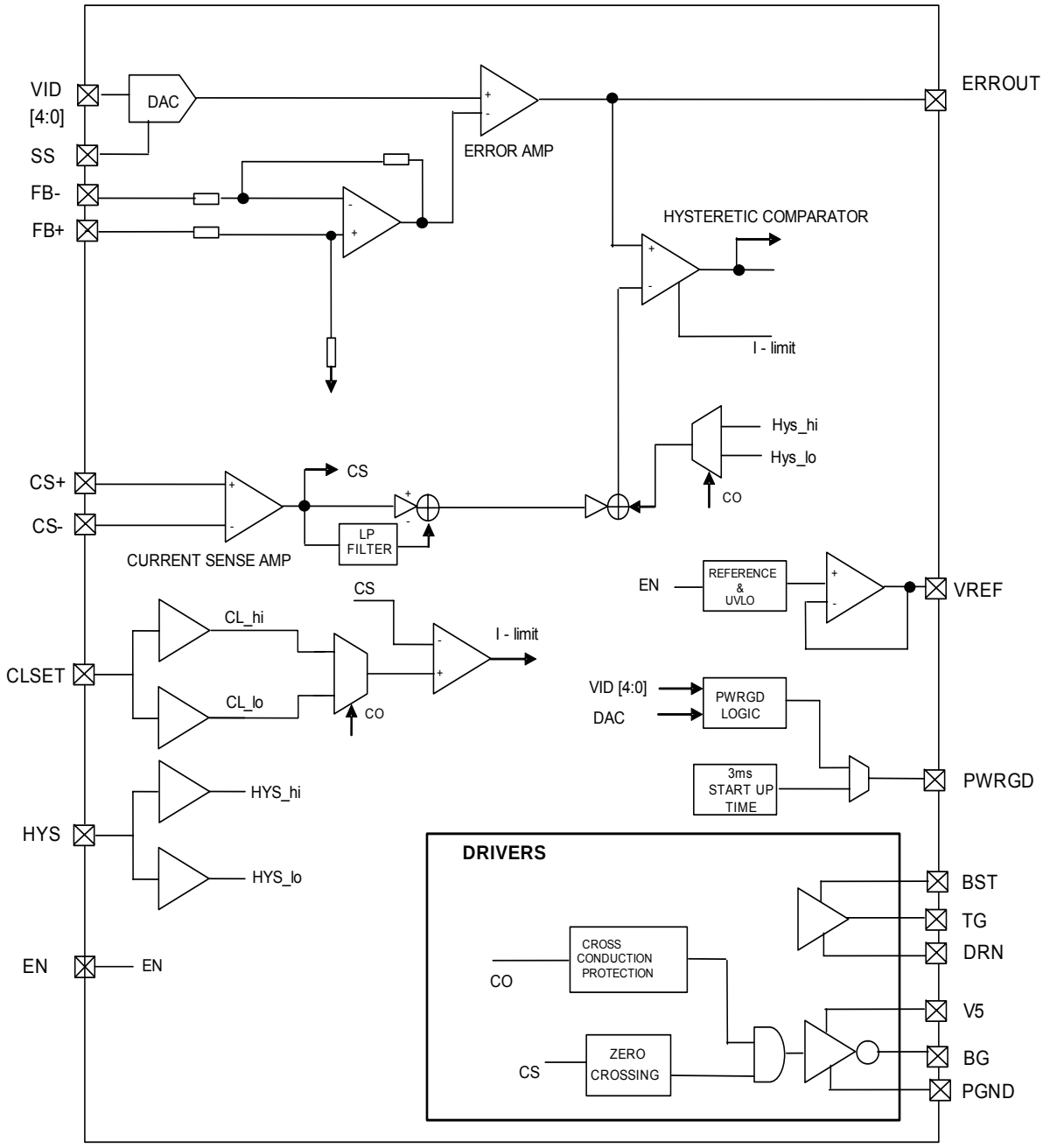


yyww = Date Code (Example: 0550)
xxxxx = Semtech Lot Number (Example: E9000)
xxxxx = (Example: 1–100)

Pin Descriptions

SC473 Pin Configuration		Pin Description
Pin #	Pin Name	
1	VID4	VID most significant bit
2	VID3	
3	VID2	
4	VID1	
5	VID0	VID least significant bit
6	HYS	Core comparator hysteresis - a resistor divider from VREF to AGND on this pin sets the hysteresis voltage
7	CLSET	Current limit set - a resistor divider from VREF to AGND on this pin sets the OCP threshold
8	VREF	Internal reference voltage (2V) - bypass to AGND with a 1000pF NPO ceramic capacitor
9	AGND	Quiet ground for analog control circuits
10	ERROUT	Error amplifier compensation pin
11	FB-	Remote GND sense - connect to VSS_Sense at the CPU socket
12	SS	Soft-start. The external NPO ceramic capacitor at this pin defines the soft-start ramp
13	FB+	Remote die sense of core voltage - connect to VCC_Sense at the CPU socket
14	CS-	Inverting input to Current-Sense amplifier
15	CS+	Non-inverting input to Current-Sense amplifier
16	RAMP	An external R-C defines the internal slope ramp
17	EN	Enable control pin - active high
18	PWRGD	Power good indicator, active high, open drain output
19	PMON	Power Monitor output
20	V5	Input supply for both control circuits and gate drive. Connect to 5V and decouple with at least 1µF ox X5R ceramic capacitance
21	BG	Output drive for the synchronous MOSFET
22	DRN	Inductor switching node - connect to the junction of the switching and synchronous MOSEFETs
23	TG	Output drive for the switching MOSFET
24	BST	Bootstrap pin - a capacitor is connected between BST and DRN to develop the floating voltage for the switching MOSFET
Thermal Pad		Power ground for driver - connect with at least two vias to the system GND plane

Block Diagram



SC473

Applications Information

Introduction

The SC473 is a new generation of hysteretic converters which combines the best features of Semtech's hysteretic converter technology with the benefit of an error amplifier. The SC473 provides a complete solution to high performance graphics core requirements.

In the SC473, the ripple for the hysteretic switching control is provided by DCR sensing. This provides several advantages over plain voltage-mode hysteretic converters, which switch on voltage ripple.

- No current sense resistors are required resulting in higher converter efficiency
- Full differential feedback of the output voltage from the CPU die is enabled
- Stable with all-ceramic output

Because the basic control is hysteretic, the SC473 provides the fastest possible transient response without switching at very high frequencies. This results in higher efficiency with less expensive parts because switching losses are reduced.

The SC473 also provides a full range of features:

- Graphics functions are implemented on-chip:
    - EN
    - PWRGD
    - VID programmable Output
    - Slew Rate Control
    - Power Monitor
- A 2.00V voltage reference is provided
- Separate hysteresis and current limit settings
- A full suite of protection features is provided:
    - Over-current protection (OCP)
    - Fixed and DAC-referenced over-voltage protection (OVP)
    - Over-temperature protection (OTP)
    - Under-voltage detection via PWRGD

All protection features are latching, and are reset either by recycling power or toggling the EN signal.

Theory of Operation

Voltage Regulation:

Referring to the block diagram on the preceding page, the hysteretic comparator is the heart of the converter. The "FB+" input corresponds roughly to the CMPREF node of our older generations of IC; the "FB-" input is similar to CMP.

To regulate, the comparator needs this information:

- DAC (reference) voltage
- Feedback voltage
- Hysteresis voltage

CMPREF receives the reference, voltage feedback and current information via current sense amplifier. The reference source is the DAC. The feedback voltage is received by the differential amplifier. A third amplifier, labeled the "Error Amplifier", multiplies the difference between the "ideal" voltage (DAC) and the actual voltage (FB+ minus FB-) for faster response. This signal is the reference for the hysteretic comparator.

CMP has the ripple signal derived from the current sense inputs plus the hysteresis signal. The DC is stripped from the ripple signals by the combination of low-pass filter and summing amplifier.

Current Limit Regulation:

In Current Limit, the voltage hysteretic converter is overridden by the current limit hysteretic comparator, and the TG pulse is terminated when the output of the current sense amplifier reaches the CL_hi threshold and BG is terminated at the CL_lo threshold. These thresholds are set from the CLSET resistor divider:

CL_hi = 0.33 * V(clset)
CL_lo = 0.20 * V(clset)

Current limit pulses continue until 32 pulses after the voltage droops to the PWRGD low threshold; then the controller latches off. This current limit algorithm is used in several generations of V_{CORE} controllers and is extremely robust.

Applications Information (Cont.)

Start-Up and Soft-Off Sequences:

For the SC473 cold start-up, V5 must rise above its under-voltage lockout (UVLO) threshold (4.4V typ.) The EN signal may go high either before UVLO or after (preferred). The DAC drives 120µA (typical) into the soft-start capacitor on the SS pin. The SS pin and DAC rise slowly until the VID(4:0) When the voltage hits the lower PWRGD threshold, PWRGD goes high, and start-up is complete.

In a normal shutdown, the EN signal is driven low, the TG and BG signals are driven low, tri-stating the power chains. An approximately 10Ω FET on the FB+ signal discharges Vcore slowly and prevents normal amounts of leakage from pulling Vcore high. The DAC is discharged to zero, but the power regulation circuitry is inactive, and PWRGD is low.

DAC Description:

A +/-0.85% 5-bit digital-to-analog converter (DAC) serves as the programmable reference source of the Core Comparator. Programming is accomplished by logic voltage levels applied to the DAC inputs. The VID code vs. the DAC output is shown in Table 1. The five voltage identification pins are used to support automatic selection of V_{OUT} voltages.

DAC Slew Rate Control:

The DAC also has integrated slew-rate control with to charge and discharge the soft-start capacitor. All operating voltage transitions including soft-start use the 120µA source to charge the soft-start capacitor.

Power Supply Protection:

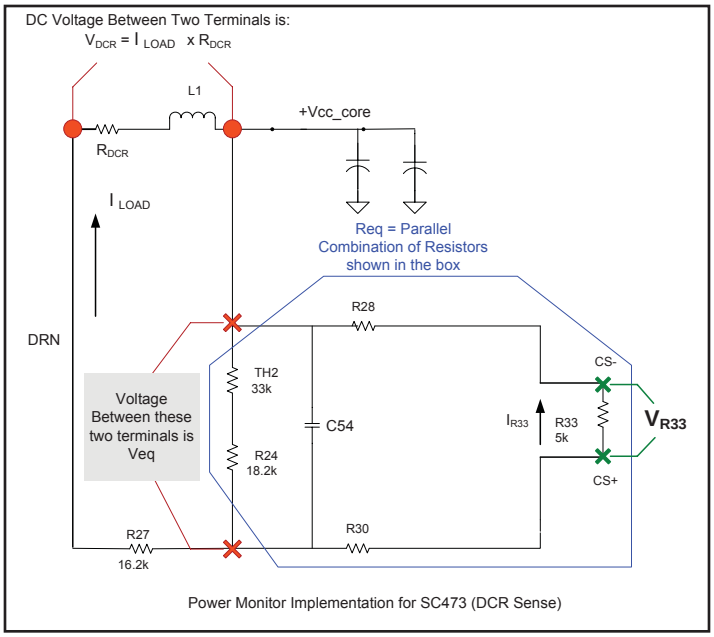
The UVLO circuit consists of a comparator that monitors the input supply voltage level, V5. The SC473 is in UVLO mode when its supply voltage has not ramped above the upper threshold or dropped below the lower threshold. The output of the UVLO comparator turns on or off the internal bias, enables or disables the SC473 output, and initiates or resets the soft-start timer.

The OVP circuit of SC473 monitors the processor core V_{OUT} voltage for an over-voltage condition. If the FB voltage is 200mV greater than the DAC voltage (i.e., out of the power-good window), the SC473 will latch off and hold the low-side driver on permanently. Either the power or EN must be recycled to clear the latch. The latch is disabled during soft-start and VID/DeeperSleep transitions. For safety, the latch is enabled if the FB voltage exceeds 1.7V even during VID transitions.

The device will be disabled and latched off when the internal junction temperature reaches approximately 160°C. Either the power or EN must be recycled to clear the latch.

Power Monitor:

The SC473 adds a power monitor feature to accurately predict the graphics CPU power consumption. The power monitor output depends on the current sensing methodology used. The following diagram and equation predict the ideal PMON output.



Power Monitor Implementation for SC473 (DCR Sense)

$$Req = (TH2 + R24)(R28 + R30 + R33) \div (TH2 + R24 + R28 + R30 + R33)$$

$$Veq = (VDCR \times Req) \div (Req + R27)$$

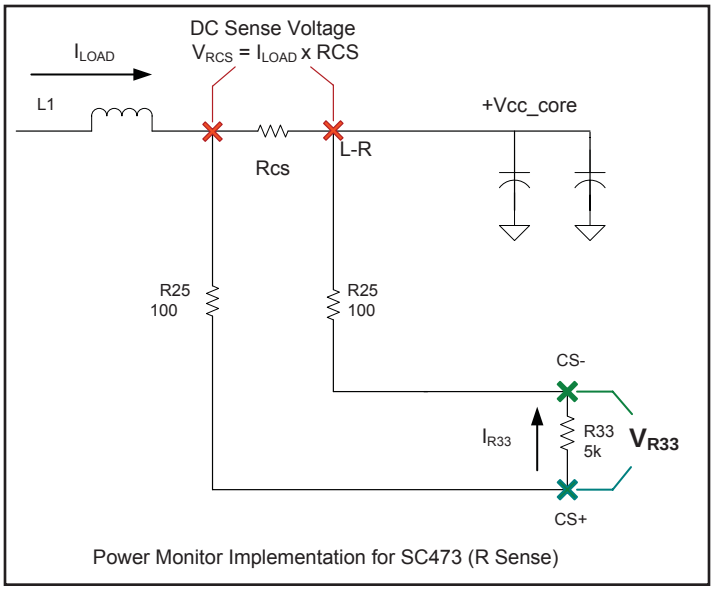
$$IR33 = Veq \div (R28 + R30 + R33)$$

$$VR33 = IR33 \times R33$$

$$PMON\_Ideal = V\,R33 \times Vcc\_core \times 28.5$$

Similar exercise can be done for R-SENSE configuration as shown below:

Applications Information (Cont.)



Power Monitor Implementation for SC473 (R Sense)

$$IR33 = VDCR \div (R25 + R25 + R33)$$

$$VR33 = IR33 \times R33$$

$$PMON\_Ideal = V\,R33 \times Vcc\_core \times 28.5$$

Applications Information (Cont.)

Component	Manufacturer	Series or Part Number
High Side MOSFET, HSFET	International Rectifier Fairchild Semiconductor Siliconix Infenion Technologies	IRF7821, IRF6602, SSC3002S, Si4860DY,Si4410BDY
Low Side MOSFET, LSFET	International Rectifier Fairchild Semiconductor Siliconix Infenion Technologies	Depends on Application
Boost Capacitor, Cbst	Various	X5R or better
Boost Diode, Dbst	Various	Schottky, 200mA or greater
Output Inductor, L	Vishay / Panasonic	0.2 µH - 0.5µH
Decoupling Capacitors	Various	X5R or better
Current Sense Resistor	IRC, Panasonic	ERJ-M1WTJ
Output Bulk Capacitors	Panasonic / NEC-TOKIN SPCAP	330µF, max ESR 6mΩ

Company	Contact
International Rectifier	Web: http://www.irf.com/product-info/ Phone: (310) 726-8000
Panasonic	Web: http://www.panasonic.com/pic/ecg/ Phone: (201) 348-7522
IRC	Web: http://www.irctt.com Phone: (888) 472-4376
NEC/TOKIN	Web: http://www.nec-tokinamerica.com/ Phone: (510) 324-4110
Sanyo	Web: http://www.sanyovideo.com/ Phone: (619) 661-6835
TDK	Web: http://www.component.tdk.com/components/components.html Phone: (847) 390-4373
Vishay/Dale	Web: http://www.vishay.com/brands/dale Phone: (402) 564-3131
Vishay/Siliconix	Web: http://www.vishay.com/brands/siliconix Phone: (800) 554-5565

Table 1.
VID vs. V_{OUT} Voltage

EN	VID4	VID3	VID2	VID1	VID0	V_{OUT}
1	1	0	0	0	0	1.1500V
1	1	0	0	0	1	1.1250V
1	1	0	0	1	0	1.1000V
1	1	0	0	1	1	1.0750V
1	1	0	1	0	0	1.0500V
1	1	0	1	0	1	1.0250V
1	1	0	1	1	0	1.0000V
1	1	0	1	1	1	0.9750V
1	1	1	0	0	0	0.9500V
1	1	1	0	0	1	0.9250V
1	1	1	0	1	0	0.9000V
1	1	1	0	1	1	0.8750V
1	1	1	1	0	0	0.8500V
1	1	1	1	0	1	0.8250V
1	1	1	1	1	0	0.8000V
1	1	1	1	1	1	0.7750V
1	0	0	0	0	0	0.7500V
1	0	0	0	0	1	0.7250V
1	0	0	0	1	0	0.7000V
1	0	0	0	1	1	0.6750V
1	0	0	1	0	0	0.6500V
1	0	0	1	0	1	0.6250V
1	0	0	1	1	0	0.6000V
1	0	0	1	1	1	0.5750V
1	0	1	0	0	0	0.5500V
1	0	1	0	0	1	0.5250V
1	0	1	0	1	0	0.5000V
1	0	1	0	1	1	0.4750V
1	0	1	1	0	0	0.4550V
1	0	1	1	0	1	0.4250V
1	0	1	1	1	0	0.4000V
1	0	1	1	1	1	0.3750V
0	X	X	X	X	X	0.0000V

Typical Characteristics

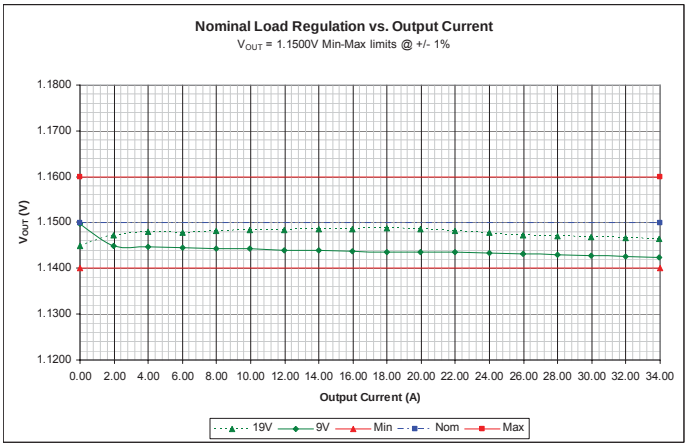


Figure 1 – Nominal Mode Line and Load Regulation

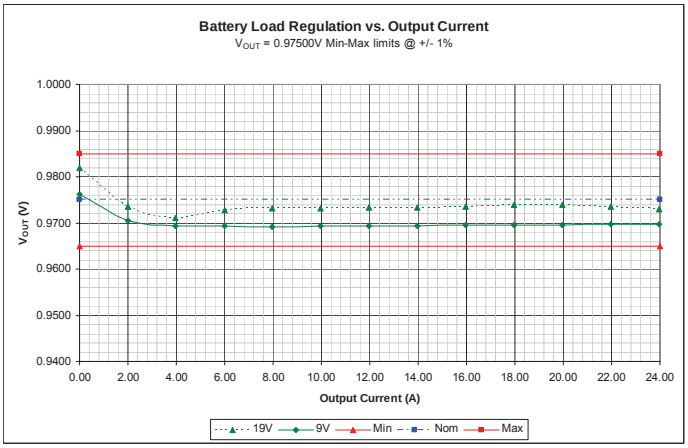


Figure 2 – Battery Mode Line and Load Regulation

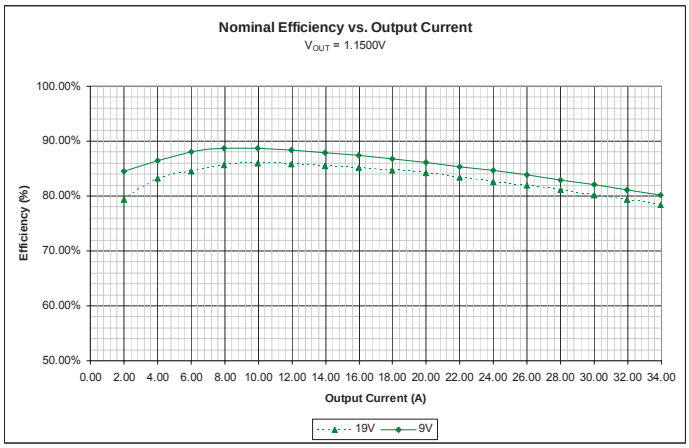


Figure 3 – Nominal Mode Efficiency v/s Output Current

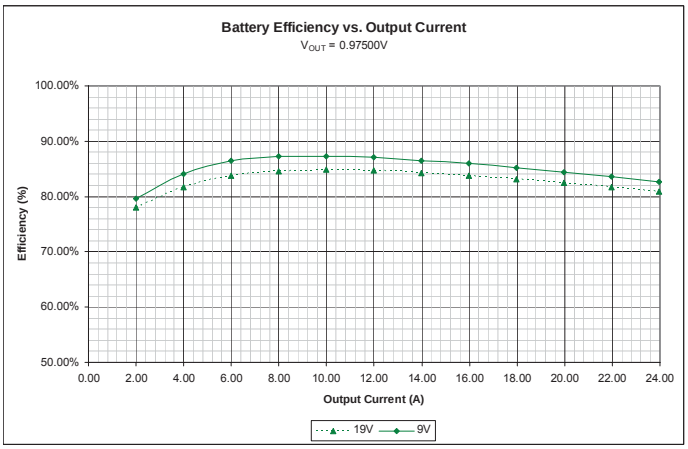


Figure 4 – Battery Mode Efficiency v/s Output Current

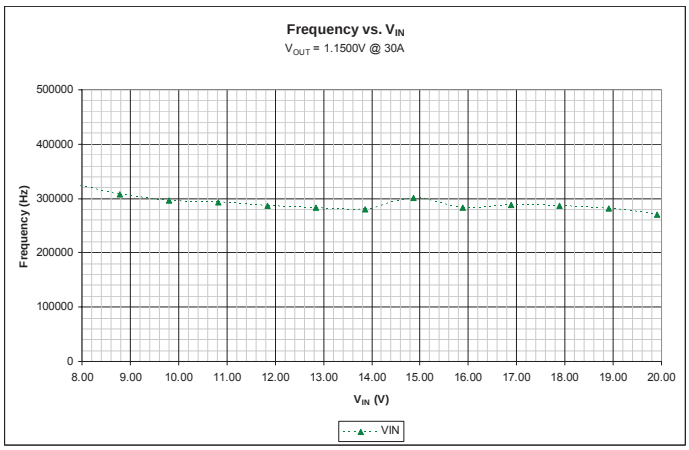


Figure 5 – Nominal Mode Frequency v/s Input Voltage

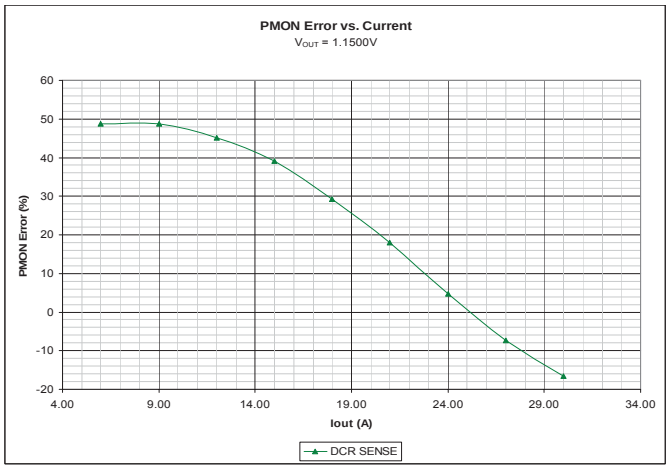


Figure 6 – Typical PMON Error v/s Output Current

*Above performance graphs correspond to Applications Schematic on page 2

Typical Characteristics

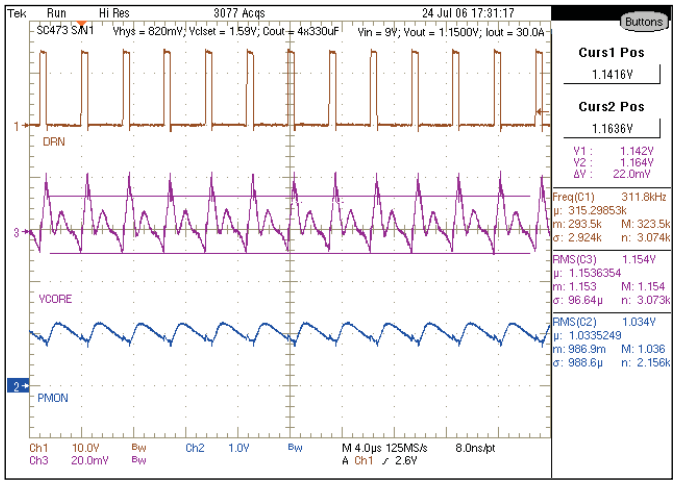


Figure 7 – Nominal Operation @ Iout = 30A

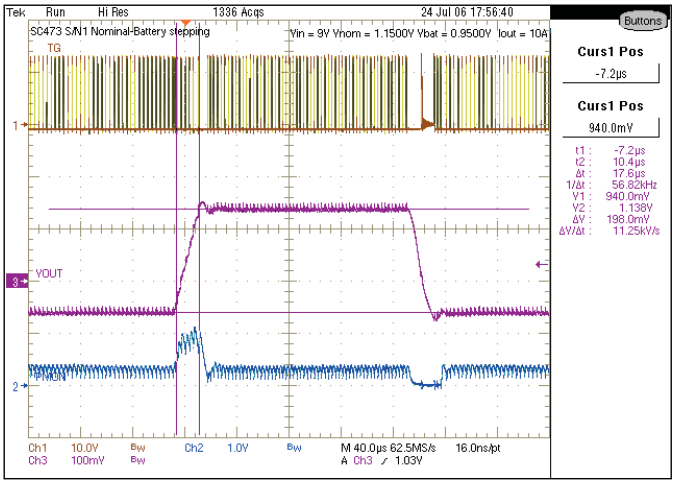


Figure 8 – Voltage Transition 0.95V to 1.15V

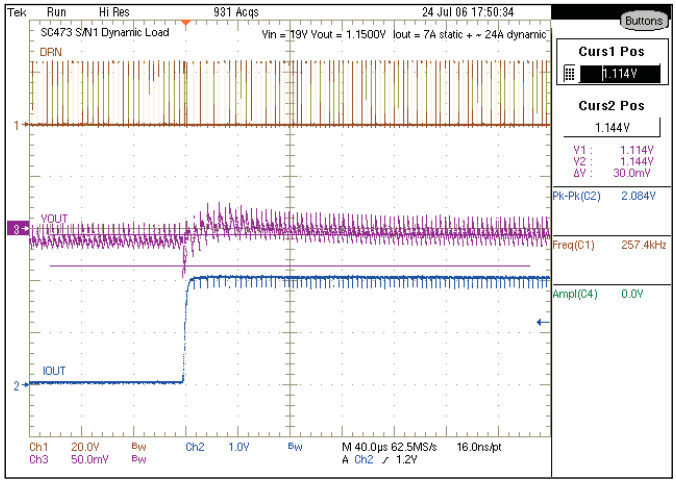


Figure 9 – Output Voltage with 24A load step

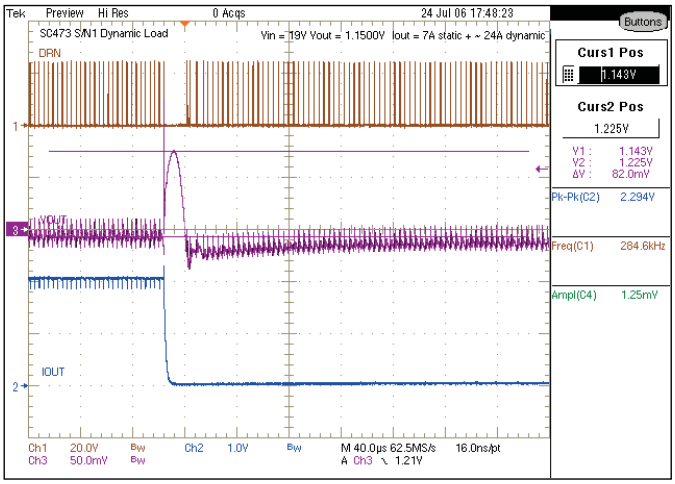
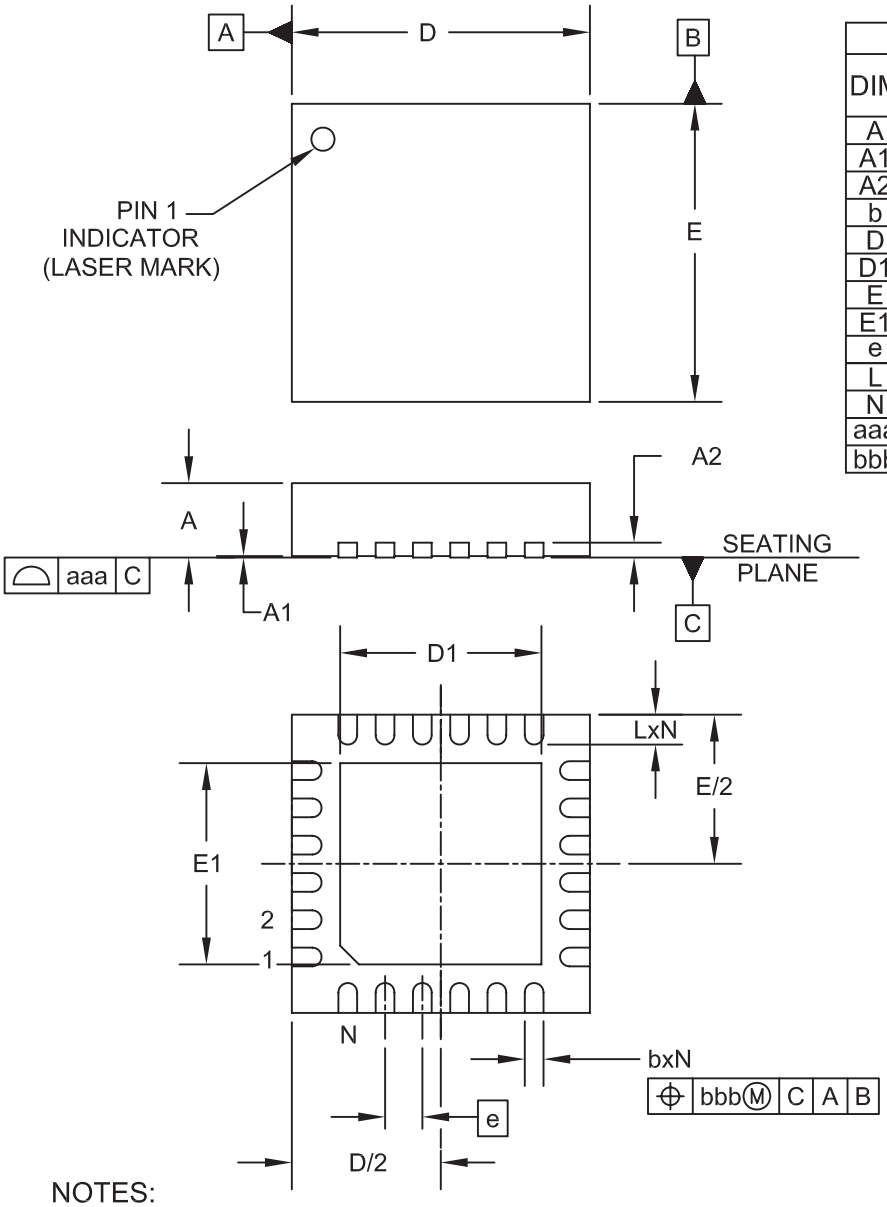


Figure 10 – Output Voltage with 24A dynamic load release

*Above performance graphs correspond to Applications Schematic on page 2

Outline Drawing - MLP 4x4-24

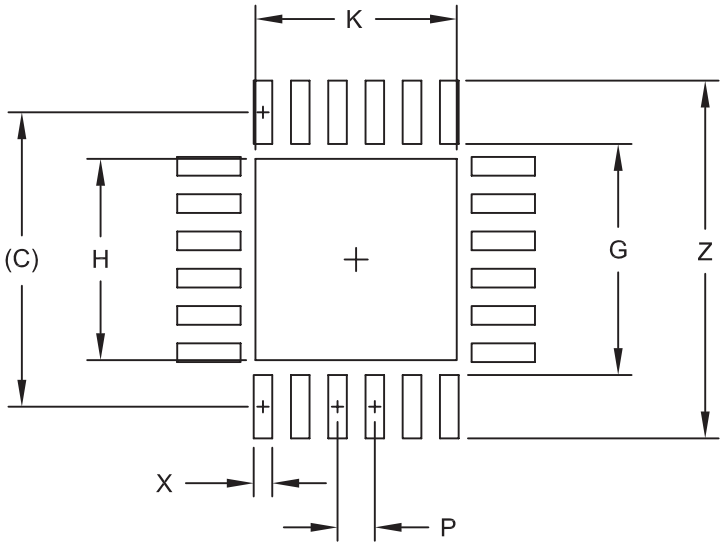


DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.031	.035	.039	0.80	0.90	1.00
A1	.000	.001	.002	0.00	0.02	0.05
A2	-	(.008)	-	-	(0.20)	-
b	.007	.010	.012	0.18	0.25	0.30
D	.152	.157	.163	3.85	4.00	4.15
D1	.100	.106	.110	2.55	2.70	2.80
E	.152	.157	.163	3.85	4.00	4.15
E1	.100	.106	.110	2.55	2.70	2.80
e	.020 BSC			0.50 BSC		
L	.012	.016	.020	0.30	0.40	0.50
N	24			24		
aaa	.004			0.10		
bbb	.004			0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Land Pattern - MLP 4x4-24



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.156)	(3.95)
G	.122	3.10
H	.106	2.70
K	.106	2.70
P	.020	0.50
X	.010	0.25
Y	.033	0.85
Z	.189	4.80

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

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