3A EcoSpeed™ Synchronous Step-Down Regulator with Automatic Power Save

Features

- V_{IN}: 3V to 5.5V
- V_{OUT}: 0.75V to 95% x V_{IN}
- I_{OUT}: Up to 3A
- Low $R_{DS(ON)}$ Switches
  - Up to 96% Peak Efficiency
- Enable High Threshold: 1V
  - Compatible with Low Voltage Logic
- High Output Accuracy
- Small Ceramic Capacitors
- Power Good Pin (Open-Drain)
- Patented Adaptive On-Time Control:
  - Excellent Transient Response
  - Programmable Pseudo-fixed Frequency
- Fault Protection Features:
  - Cycle-by-Cycle Current Limit
  - Short Circuit Protection
  - Over and Under Output Voltage Protection
  - Over-Temperature
- Internal Soft start
- Smart Power Save
- Ultra-Small Lead-Free 3x3mm, 10-Pin MLPD Package
- Fully WEEE and RoHS Compliant

Applications

- Networking Equipment, Embedded Systems
- Medical Equipment, Office Automation
- Instrumentation, Portable Systems
- Consumer Devices (DTV, Set-top Box, ...)
- 5V POL Converters

Description

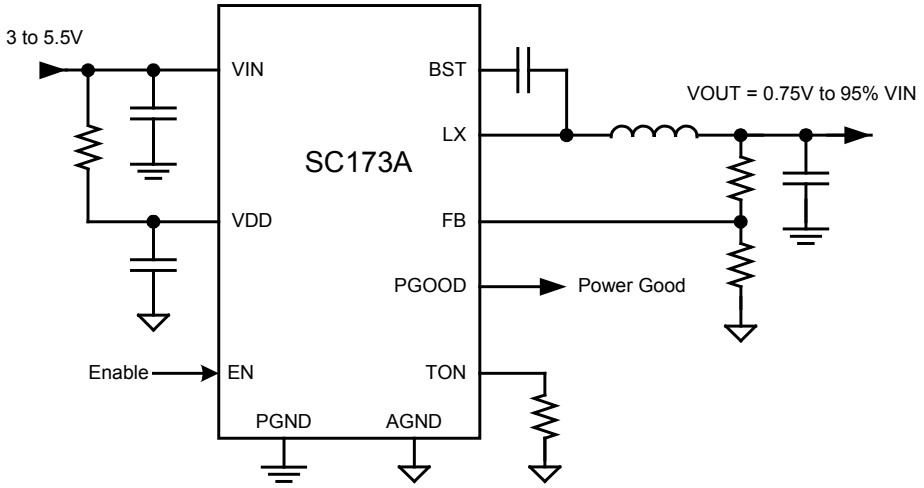
The SC173A is an integrated, synchronous 3A EcoSpeed™ step-down regulator, which incorporates Semtech's advanced, patented adaptive on-time architecture to achieve best-in-class performance in dynamic point-of-load applications. The input voltage range is 3V to 5.5V with a programmable output voltage from 0.75V up to 95% x V_{IN}. The device features low-$R_{DS(ON)}$ internal switches and automatic power save for high efficiency across the output load range.

Adaptive on-time control provides programmable pseudo-fixed frequency operation and excellent transient performance. The switching frequency can be set from 200kHz to 1MHz - allowing the designer to reduce external LC filtering and minimize light load (standby) losses.

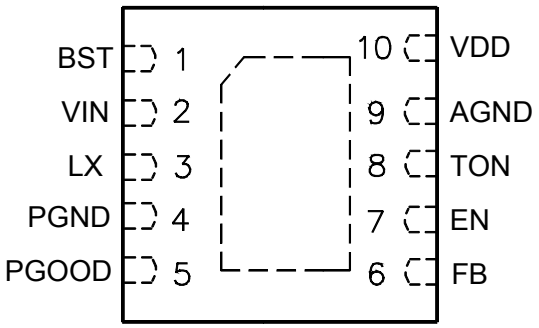
Additional features include cycle-by-cycle current limit, soft start, input UVLO and output OV protection, and over temperature protection. The open-drain PGOOD pin provides output status. Standby current is less than 10µA when disabled.

The device is available in a low profile, thermally enhanced MLPD-3x3mm 10-pin package.

Typical Application Circuit



Pin Configuration



10 Pin MLPD

θ_{JA} = 40 °C/W.

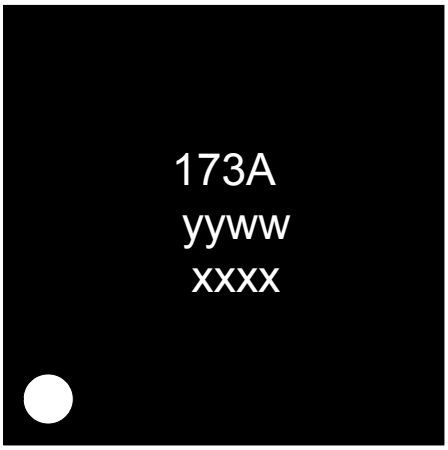
Ordering Information

Device	Top Mark	Package[2]
SC173AMLTRT[1]	173A	MLPD-10 3x3
SC173AEVB	Evaluation Board	

Notes:
1) Available in tape and reel packaging only. A reel contains 3000 devices.
2) Available in lead-free packaging only. WEEE compliant and Halogen free. This component and all homogenous sub-components are RoHS compliant.

Marking Information

TOP MARKING



yyww = Date Code (Example: 0952)
xxxx = Semtech Lot Number (Example: 3901)

SEMTECH

Absolute Maximum Ratings

LX to GND[3] ..... - 0.3(DC) to +6.0V(DC) Max
VIN to PGND, EN to AGND ..... -0.3 to +6.0V
BST to LX ..... -0.3 to +6.0V
BST to PGND ..... -0.3 to +12V
VDD to AGND, VOUT to AGND ..... -0.3V to +6.0V
FB, PGOOD, TON ..... -0.3 to VDD + 0.3V
AGND to PGND ..... -0.3 to +0.3V
Peak IR Reflow Temperature ..... 260°C
ESD Protection Level[2] 1kV

Recommended Operating Conditions

Supply Input Voltage ..... 3V to 5.5V
Maximum Continuous Output Current 3A

Thermal Information

Storage Temperature ..... -60 to +150°C
Maximum Junction Temperature ..... 150°C
Operating Junction Temperature ..... -40 to +125°C
Thermal Resistance, Junction to Ambient[1] ..... 40°C/W

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES-

(1) Calculated from package in still air, mounted to 3" x 4.5", 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

(2) Tested according to JEDEC standard JESD22-A114-B

(3) Due to parasitic board inductance, the transient LX pin voltage at the point of measurement may appear larger than that which exists on silicon. The device is designed to tolerate the short duration transient voltages that will appear on the LX pin due to the deadtime diode conduction, for inductor currents up to the current limit setting of the device. See application section for details.

Electrical Characteristics

Unless specified: V_{IN} =5V, T_A=+25°C for Typ, -40°C to +85°C for Min and Max, T_J < 125°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Supplies						
VIN, VDD Input Voltage			3		5.5	V
VDD UVLO Threshold		Rising UVLO V_{TH}	2.75	2.85	2.98	V
VDD UVLO Hysteresis			100	200		mV
VIN, VDD Supply Current		EN= 0V		5	15	µA
		I_{OUT}=0A[1]		500		
Controller						
FB On-Time Threshold			0.7425	0.75	0.7575	V
Frequency Programming Range		See R_{TON} Calculation	200		1000	kHz
FB Input Bias Current		FB=VDD or 0V	-1		+1	µA
Timing						
On-Time		In Continuous Conduction V_{IN}=5V, V_{OUT}=3V, R_{TON}=200kΩ	2.7	3	3.3	µs
Minimum On-Time[1]				80		ns
Minimum Off-Time[1]				250		ns

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Electrical Characteristics (continued)

Unless specified: V_{IN} =5V, T_A=+25°C for Typ, -40°C to +85°C for Min and Max, T_J < 125°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Power Good						
Power Good Threshold		Power Good Signal Threshold High	116	120	124	%V_{OUT}
		Power Good Signal Threshold Low	86	90	93	
PGOOD Delay Time(1)		VDD=3V		1		ms
		VDD=5V		2		
Noise Immunity Delay Time				5		µs
Leakage					1	µA
Power Good On-Resistance				10	20	Ω
Fault Protection						
Output Under-Voltage Fault		FB with Respect to REF, 8 Consecutive Clocks	-30	-25	-20	%
Output Over-Voltage Fault		FB with Respect to REF	+16	+20	+24	%
Smart PowerSave Protection Threshold		FB with Respect to REF	+7	+10	+13	%
OV, UV Fault Noise Immunity Delay				5		µs
Over-Temperature Shutdown		OT Latched		150		°C
Enable						
Output Enabled			1			V
Output Disabled					0.4	V
EN Input Bias Current		EN = VDD or 0V		0.5	8.0	µA
Enable Pin Floating Voltage		EN floating	39	41	44	%V_{DD}

Electrical Characteristics (continued)

Unless specified: V_{IN} =5V, T_A=+25°C for Typ, -40°C to +85°C for Min and Max, T_J < 125°C

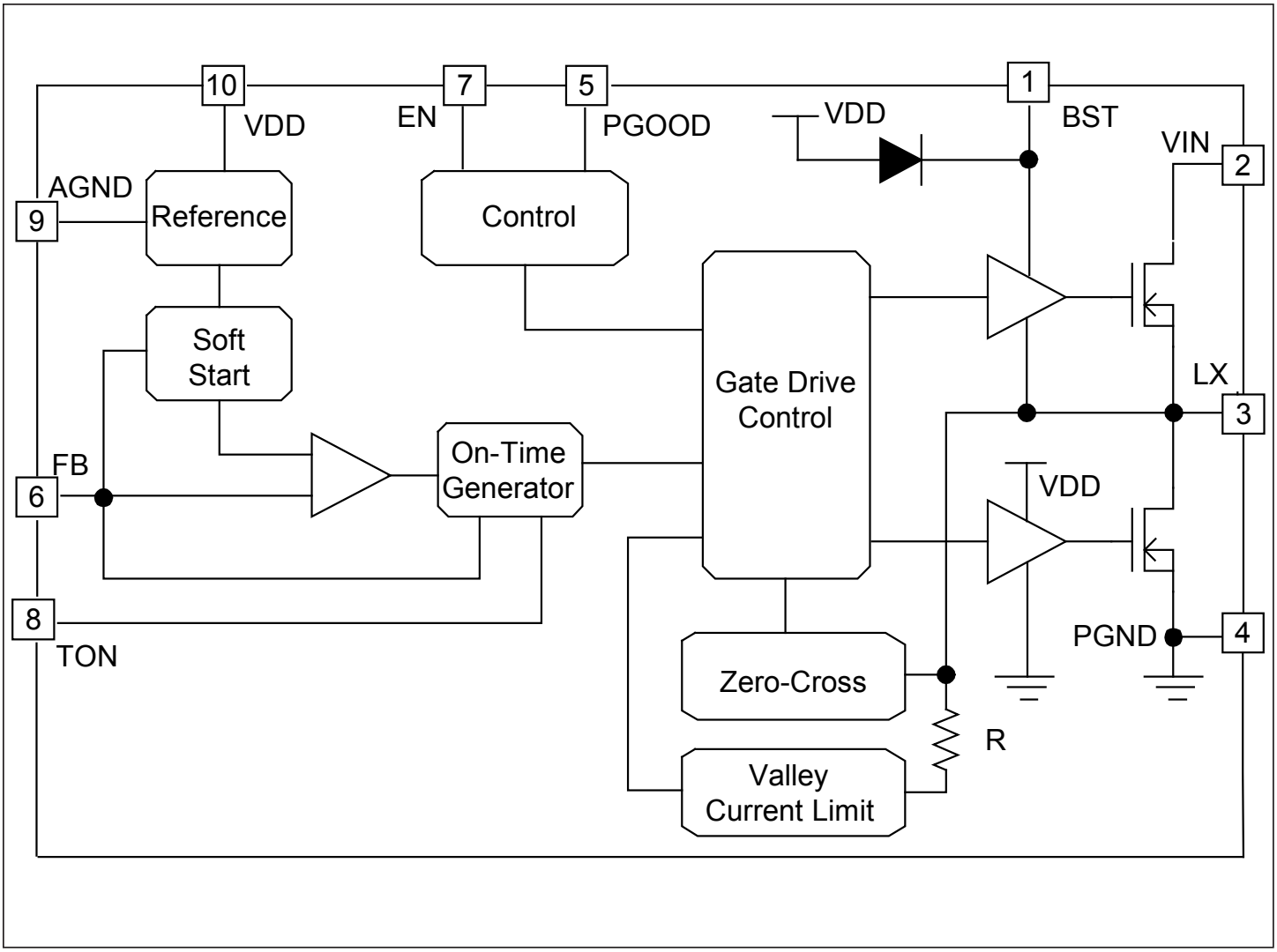
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Gate Drivers						
BST Switch On resistance				25	45	Ω
Internal Power MOSFETs						
Current Limit		Valley Current Limit, VDD=5V	3.5			A
		Valley Current Limit, VDD=3V	3	3.5		
LX Leakage Current		VIN=5.5V, LX=0V, High Side		1	10	µA
Switch Resistance		High Side		60	85	mΩ
		Low Side		50	75	
Non-overlap time (1)				30		ns

Note:
(1) Typical value from EVB, not ATE tested.

Pin Descriptions (MLPD-10)

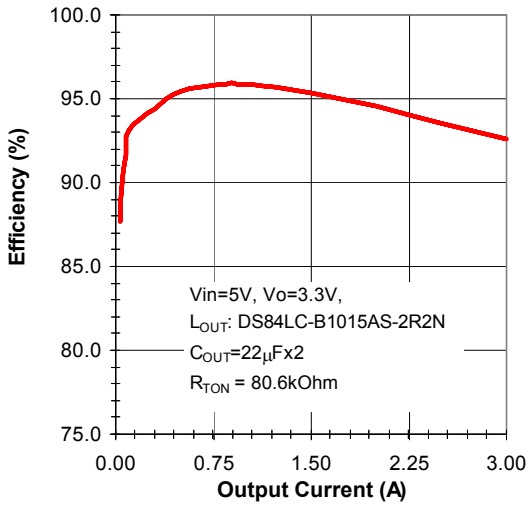
Pin #	Pin Name	Pin Function
1	BST	Bootstrap pin. A capacitor is connected between BST to LX to develop the floating voltage for the high-side gate drive.
2	VIN	Power input supply voltage.
3	LX	Switching (Phase) node.
4	PGND	Power ground.
5	PGOOD	Open-drain Power Good indicator. High impedance indicates power is good. An external pull-up resistor is required.
6	FB	Feedback input for switching regulator. Connect to an external resistor divider from the output to program the output voltage.
7	EN	Enable input for the switching regulator. Pull EN above 1V or float it to enable the part with automatic power save mode enabled. Connect EN to AGND to disable the switching regulator.
8	TON	On-time set input. Set the on-time by a series resistor to AGND.
9	AGND	Analog Ground.
10	VDD	Input power for internal control circuit. Needs at least 2.2µF decoupling capacitor from this pin to AGND.
	PAD	Thermal pad for heatsinking purposes. Connect to ground plane using multiple vias. Not connected internally.

Block Diagram

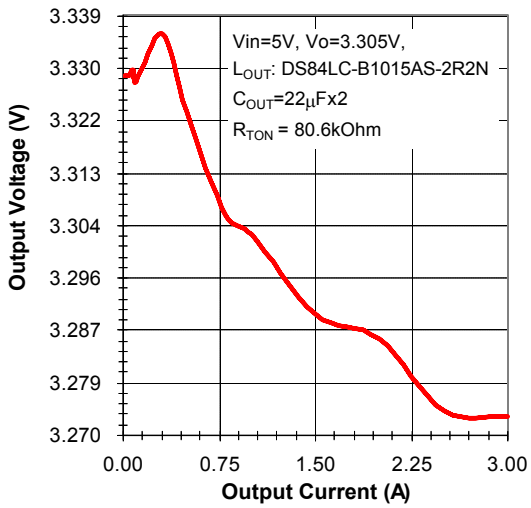


Typical Characteristics

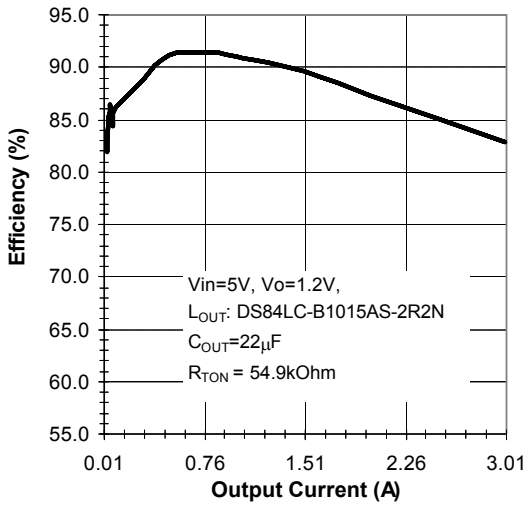
Efficiency vs Output Current



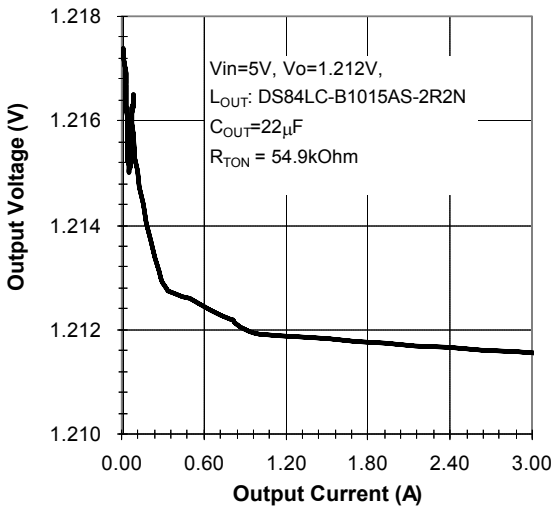
Output Voltage vs Output Current



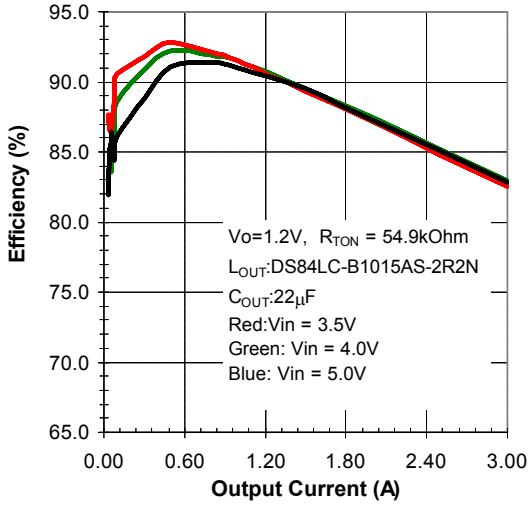
Efficiency vs Output Current



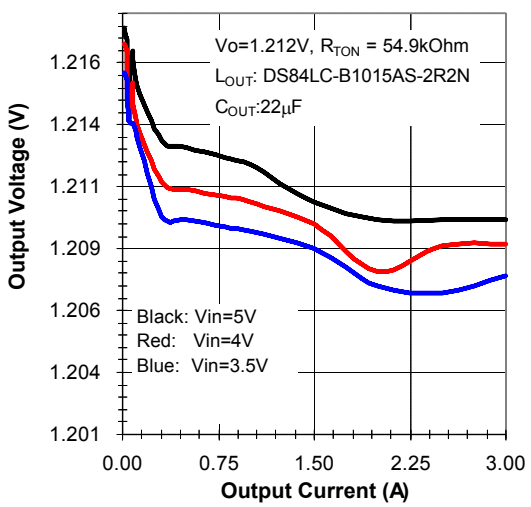
Output Voltage vs Output Current



Efficiency vs Output Current

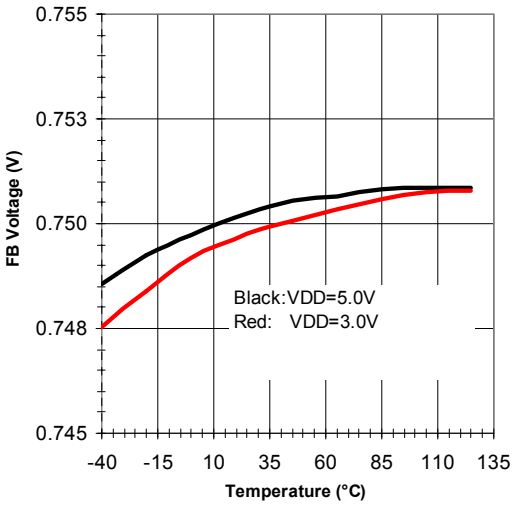


Output Voltage vs Output Current

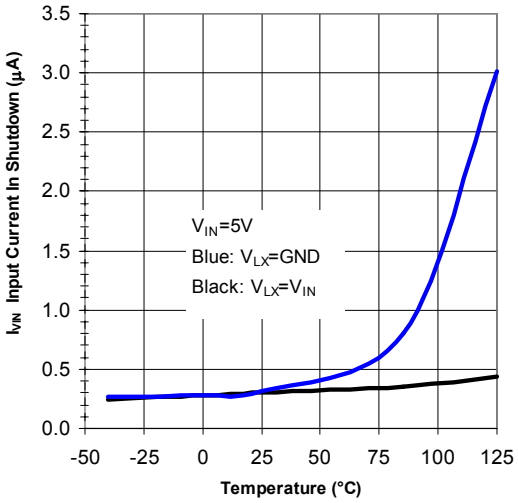


Typical Characteristics

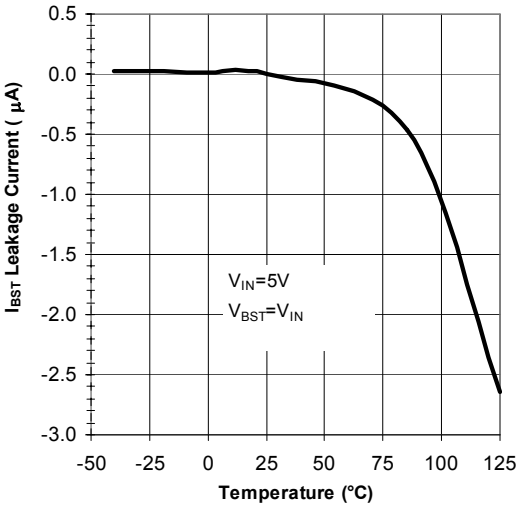
FB Voltage vs Temperature



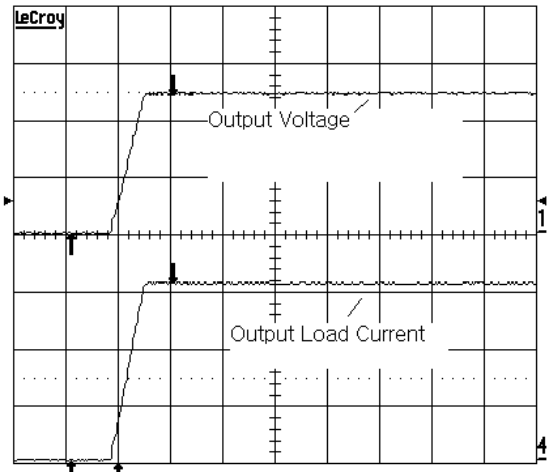
I_{VIN} Input Current In Shutdown vs Temperature



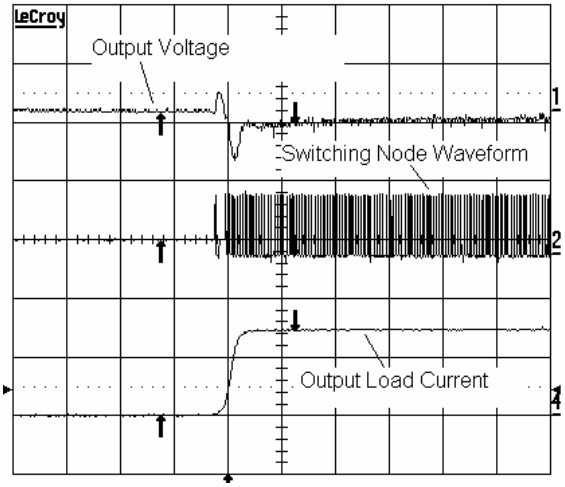
I_{BST} Leakage Current vs Temperature



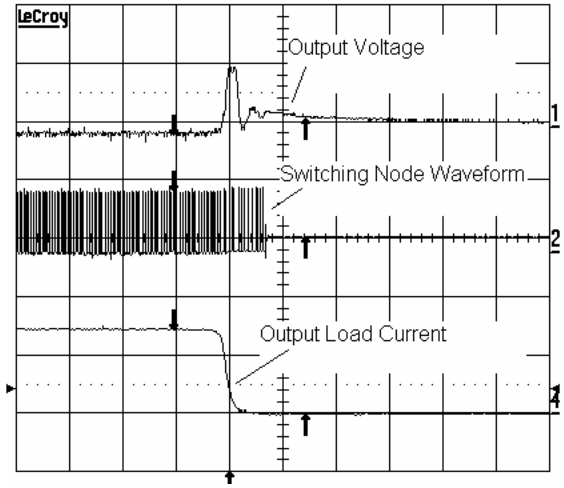
Start up waveform (V_{IN}=5V, V_{OUT}=1.2V, I_{OUT}=3A, Channel 1: 500mV/Div, Channel 4: 1A/Div, Time: 1ms/Div)



Load Transient Test (V_{IN}=5V, V_{OUT}=1.2V, I_{OUT}= 0A to 3A, L_{OUT}=1.0µH,C_{OUT}=2x22µF,Channel 1: 50mV/Div, Channel 2:5V/Div,Channel 4:2A/Div,Time:20µs/Div)

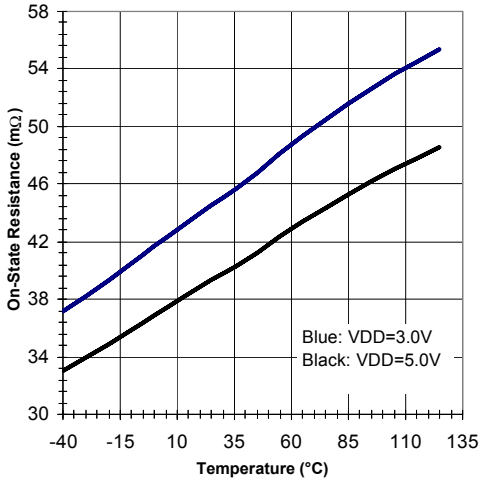


Load Transient Test (V_{IN}=5V, V_{OUT}=1.2V, I_{OUT}= 3A to 0A, L_{OUT}=1.0µH, C_{OUT}=2x22µF, Channel 1: 50mV/Div,Channel 2:5V/Div,Channel 4:2A/Div, Time:20µs/Div)

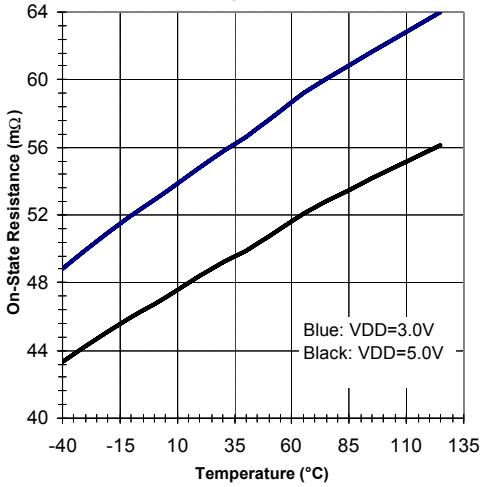


Typical Characteristics

Low Side Switch On-State Resistance vs Temperature



High Side Switch On-State Resistance vs Temperature



Applications Information

SC173A Synchronous Buck Converter

The SC173A is a step down synchronous buck dc-dc regulator. The SC173A is capable of 3A operation at very high efficiency in a tiny 3x3-10 pin package. The programmable operating frequency range of 200kHz – 1MHz (continuous conduction mode) enables the user to optimize the solution for minimum board space and optimum efficiency.

The buck regulator employs pseudo-fixed frequency adaptive on-time control. This control scheme allows fast transient response thereby lowering the size of the power components used in the system.

Input Voltage Range

The SC173A can operate with an input voltage ranging from 3V to 5.5V.

Psuedo-fixed Frequency Adaptive On-time Control

The PWM control method used by the SC173A is pseudo-fixed frequency, adaptive on-time, as shown in Figure 1. The ripple voltage generated at the output capacitor ESR is used as a PWM ramp signal. This ripple is used to trigger the on-time of the controller.

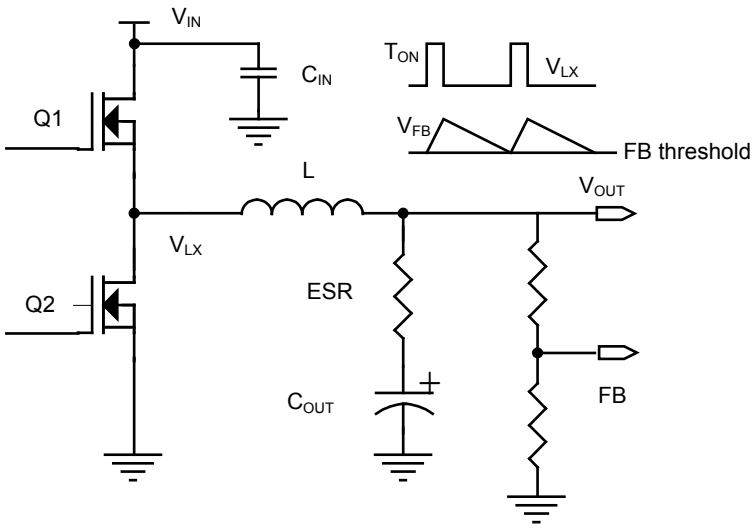


Figure 1 — PWM Control Method, V_{OUT} Ripple

The adaptive on-time is determined by an internal one-shot timer. When the one-shot is triggered by the output ripple, the device sends a single on-time pulse to the high-side MOSFET. The pulse period is determined by V_{OUT} and V_{IN}; the period is proportional to output voltage and inversely proportional to input voltage. With this adaptive on-time arrangement, the device automatically anticipates the on-time needed to regulate V_{OUT} for the present V_{IN} condition and at the selected frequency.

The advantages of adaptive on-time control are:

- Predictable operating frequency compared to other variable frequency methods.
- Reduced component count by eliminating the error amplifier and compensation components.
- Reduced component count by removing the need to sense and control inductor current.
- Fast transient response — the response time is controlled by a fast comparator instead of a typically slow error amplifier.
- Reduced output capacitance due to fast transient response

One-Shot Timer and Operating Frequency

The one-shot timer operates as shown in Figure 2. The FB Comparator output goes high when V_{FB} is less than the internal 750mV reference. This feeds into the gate drive and turns on the high-side MOSFET, and also starts the one-shot timer. The one-shot timer uses an internal comparator, timing capacitor, and a low pass filter (LPF) which regenerates V_{OUT} from LX. One comparator input is connected to the filtered LX voltage, the other input is connected to the capacitor. When the on-time begins, the internal capacitor charges from zero volts through a current which is proportional to V_{IN}. When the capacitor voltage reaches V_{OUT}, the on-time is completed and the high-side MOSFET turns off.

This method automatically produces an on-time that is proportional to V_{OUT} and inversely proportional to V_{IN}. Under steady-state operation conditions, the switching frequency can be determined from the on-time by the following equation.

$$f_{SW} = \frac{V_{OUT}}{T_{ON} \times V_{IN}}$$

Applications Information (continued)

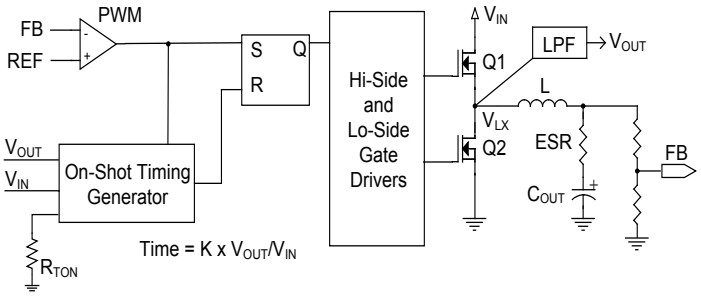


Figure 2 — On-Time Generation

The SC173A uses an external resistor to set the on-time which indirectly sets the frequency. The on-time can be programmed to provide operating frequency from 200kHz to 1MHz using a resistor between the TON pin and ground. The resistor value is selected by the following equation.

$$R_{TON} = \frac{1}{25pF \cdot f_{SW}}$$

V_{OUT} Voltage Selection

The switcher output voltage is regulated by comparing V_{OUT} as seen through a resistor divider at the FB pin to the internal 750mV reference voltage, see Figure 3.

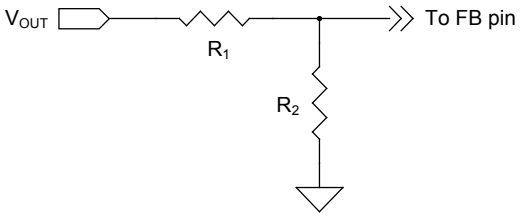


Figure 3 — Output Voltage Selection

Note that this control method regulates the valley of the output ripple voltage, not the DC value. The DC output voltage V_{OUT} is offset by the output ripple according to the following equation.

$$V_{OUT} = 0.75V \cdot \left(1 + \frac{R_1}{R_2}\right) + \frac{V_{RIPPLE}}{2}$$

Enable Input

The EN input is used to enable or disable the switching regulator. When EN is low (grounded), the switching regulator is off and in its lowest power state. When off, the output power switches are tri-stated.

When EN is pulled high (above 1V), or permitted to float, the switching regulator turns on with automatic power save enabled.

Smart Power Save Protection

Active loads may leak current from a higher voltage into the switcher output. Under light load conditions with power save enabled, this can force V_{OUT} to slowly rise and reach the over-voltage threshold, resulting in a hard shutdown. Smart power save prevents this condition. When the FB voltage exceeds 10% above nominal (exceeds 825mV), the device immediately disables powe save, and DL drives high to turn on the low-side MOSFET. This draws current from V_{OUT} through the inductor and causes V_{OUT} to fall. When V_{FB} drops back to the 750mV trip point, a normal T_{ON} switching cycle begins. This method prevents a hard OVP shutdown and also cycles energy from V_{OUT} back to V_{IN}. Figure 4 shows typical waveforms for the Smart Power Save feature.

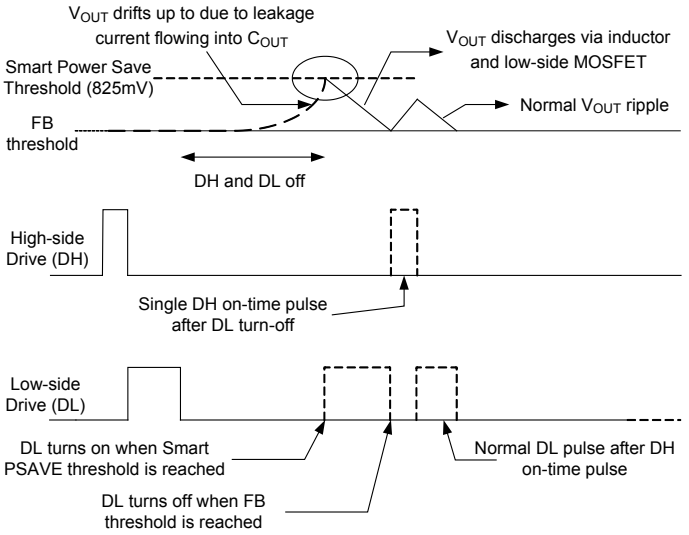


Figure 4 — Smart Power Save

Current Limit Protection

The device features fixed current limiting, which is accomplished by using the $R_{DS(ON)}$ of the lower MOSFET for current sensing. While the low-side MOSFET is on, the

inductor current flows through it and creates a voltage across the $R_{DS(ON)}$. During this time, the voltage across the MOSFET is negative with respect to ground. During this time, If this MOSFET voltage drop exceeds the internal reference voltage, the current limit will activate. The current limit then keeps the low-side MOSFET on and will not allow another high side on-time, until the current in the low-side MOSFET reduces enough to drop below the internal reference voltage once more. This method regulates the inductor valley current at the level shown by I_{LIM} in Figure 5.

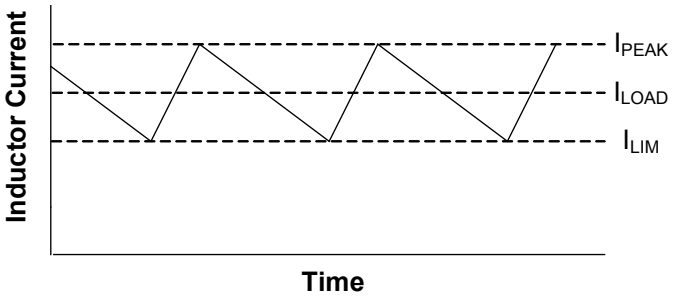


Figure 5 — Valley Current Limit

Setting the valley current limit to a value of I_{LIM} results in a peak inductor current of ILIM plus the peak-to-peak ripple current. In this situation, the average (load) current through the inductor will be I_{LIM} plus one half the peak-to-peak ripple current.

Soft start of PWM Regulator

Soft start is achieved in the PWM regulator by using an internal voltage ramp as the reference for the FB comparator. The voltage ramp is generated using an internal charge pump which drives the reference from zero to 750mV in ~1.8mV increments, using an internal ~500kHz oscillator. When the ramp voltage reaches 750mV, the ramp is ignored and the FB comparator switches over to a fixed 750mV threshold. During soft start the output voltage tracks the internal ramp, which limits the start-up inrush current and provides a controlled soft start profile for a wide range of applications. Typical soft start ramp time is 0.85ms.

During soft start the regulator turns off the low-side MOSFET on any cycle if the inductor current falls to zero. This prevents negative inductor current, allowing the device to start into a pre-biased output.

Power Good Output

The power good (PGOOD) output is an open-drain output which requires a pull-up resistor. When the output voltage is 10% below the nominal voltage, PGOOD is pulled low. It is held low until the output voltage returns to the nominal voltage. PGOOD is held low during soft start and activated approximately 1ms after V_{OUT} reaches regulation. The total PGOOD delay is typically 2ms.

PGOOD will transition low if the V_{FB} pin exceeds +20% of nominal, which is also the over-voltage shutdown threshold (900mV). PGOOD also pulls low if the EN pin is low when VDD is present.

Output Over-Voltage Protection

Over-Voltage Protection (OVP) becomes active as soon as the device is enabled. The threshold is set at 750mV + 20% (900mV). When V_{FB} exceeds the OVP threshold, DL latches high and the low-side MOSFET is turned on. DL remains high and the controller remains off, until the EN input is toggled or VDD is cycled. There is a 5µs delay built into the OVP detector to prevent false transitions. PGOOD is also low after an OVP event.

Output Under-Voltage Protection

When V_{FB} falls to 75% of its nominal voltage (falls to 562.5mV) for eight consecutive clock cycles, the switcher is shut off and the DH and DL drives are pulled low to turn off the MOSFETs. The controller stays off until EN is toggled or VDD is cycled.

VDD UVLO, and POR

Under-Voltage Lock-Out (UVLO) circuitry inhibits switching and tri-states the power FETs until VDD rises above 2.9V. An internal Power-On Reset (POR) occurs when VDD exceeds 2.9V, which resets the fault latch and soft start counter to begin the soft start cycle. The SC173A then begins a soft start cycle. The PWM will shut off if VDD falls below 2.7V.

Applications Information (continued)

Design Procedure

When designing a switch mode supply the input voltage range, load current, switching frequency, and inductor ripple current must be specified.

The maximum input voltage (V_{INMAX}) is the highest specified input voltage. The minimum input voltage (V_{INMIN}) is determined by the lowest input voltage after evaluating the voltage drops due to connectors, fuses, switches, and PCB traces.

The following parameters define the design.

- Nominal output voltage (V_{OUT})
- Static or DC output tolerance
- Transient response
- Maximum load current (I_{OUT})

There are two values of load current to evaluate — continuous load current and peak load current. Continuous load current relates to thermal stresses which drive the selection of the inductor and input capacitors. Peak load current determines instantaneous component stresses and filtering requirements such as inductor saturation, output capacitors, and design of the current limit circuit.

The following values are used in this design.

- V_{IN} = 5V ± 10%
- V_{OUT} = 1.0V ± 4%
- f_{SW} = 800kHz
- Load = 3A maximum

Frequency Selection

Selection of the switching frequency requires making a trade-off between the size and cost of the external filter components (inductor and output capacitor) and the power conversion efficiency.

The desired switching frequency is 800kHz which results from using components selected for optimum size and cost .

A resistor (R_{TON}) is used to program the on-time (indirectly setting the frequency) using the following equation.

$$R_{TON} = \frac{1}{25pF \cdot f_{SW}}$$

Calculating R_{TON} results in the following solution.

R_{TON}=50kΩ, we use R_{TON}=49.9kΩ in real application.

Inductor Selection

In order to determine the inductance, the ripple current must first be defined. Low inductor values result in smaller size but create higher ripple current which can reduce efficiency. Higher inductor values will reduce the ripple current/voltage and for a given DC resistance are more efficient. However, larger inductance translates directly into larger packages and higher cost. Cost, size, output ripple, and efficiency are all used in the selection process.

The ripple current will also set the boundary for power save operation. The switching will typically enter power save mode when the load current decreases to 1/2 of the ripple current. For example, if ripple current is 3A then power save operation will typically start for loads less than 1.5A. If ripple current is set at 40% of maximum load current, then power save will start for loads less than 20% of maximum current.

The inductor value is typically selected to provide a ripple current that is between 25% to 50% of the maximum load current. This provides an optimal trade-off between cost, efficiency, and transient performance.

During the DH on-time, voltage across the inductor is (V_{IN} - V_{OUT}). The equation for determining inductance is shown next.

$$T_{ON} = \frac{V_{OUT}}{V_{INMAX} \cdot f_{SW}}$$

$$L = \frac{(V_{IN} - V_{OUT}) \times T_{ON}}{I_{RIPPLE}}$$

Applications Information (continued)

Example

In this example, the inductor ripple current is set equal to 30% of the maximum load current. Therefore ripple current will be 30% x 3A or 0.9A. To find the minimum inductance needed, use the V_{IN} and T_{ON} values that correspond to V_{INMAX}.

$$T_{ON\_VINMAX} = \frac{1V}{5.5V \cdot 800kHz} = 227ns$$

$$L = \frac{(5.5V - 1V) \bullet 227ns}{0.9A} = 1.14\mu H$$

A larger value of 2µH is selected. This will decrease the maximum I_{RIPPLE} to 0.511A.

Note that the inductor must be rated for the maximum DC load current plus 1/2 of the ripple current.

The ripple current under minimum V_{IN} conditions is also checked using the following equations.

$$T_{ON\_VINMIN} = \frac{1V}{4.5V \times 800kHz} = 277ns$$

$$I_{RIPPLE} = \frac{(V_{IN} - V_{OUT}) \times T_{ON}}{L}$$

$$I_{RIPPLE\_VINMIN} = \frac{(4.5V - 1V) \times 277ns}{2\mu H} = 0.485A$$

Capacitor Selection

The output capacitors are chosen based on required ESR and capacitance. The maximum ESR requirement is controlled by the output ripple requirement and the DC tolerance. The output voltage has a DC value that is equal to the valley of the output ripple plus 1/2 of the peak-to-peak ripple. Change in the output ripple voltage will lead to a change in DC voltage at the output.

The design goal is for the output voltage regulation to be ±4% under static conditions. The internal 750mV reference tolerance is 1%. Assuming a 1% tolerance from the FB resistor divider, this allows 2% tolerance due to V_{OUT} ripple. Since this 2% error comes from 1/2 of the ripple voltage, the allowable ripple is 4%, or 40mV for a 1V output.

The maximum ripple current of 0.511A creates a ripple voltage across the ESR. The maximum ESR value allowed is shown by the following equations.

$$ESR_{MAX} = \frac{V_{RIPPLE}}{I_{RIPPLEMAX}} = \frac{40mV}{0.51A}$$

$$ESR_{MAX} = 78.3\ m\Omega$$

The output capacitance is chosen to meet transient requirements. A worst-case load release, from maximum load to no load at the exact moment when inductor current is at the peak, determines the required capacitance. If the load release is instantaneous (load changes from maximum to zero in < 1µs), the output capacitor must absorb all the inductor's stored energy. This will cause a peak voltage on the capacitor according to the following equation.

$$COUT_{MIN} = \frac{L \times (I_{OUT} + \frac{1}{2} \times I_{RIPPLEMAX})^2}{(V_{PEAK})^2 - (V_{OUT})^2}$$

Assuming a peak voltage V_{PEAK} of 1.050V (50mV rise upon load release), and a 3A load release, the required capacitance is shown by the next equation.

$$COUT_{MIN} = \frac{2\mu H \times (3A + \frac{1}{2} \times 0.511A)^2}{(1.05V)^2 - (1.0V)^2} = 207\ \mu F$$

If the load release is relatively slow, the output capacitance can be reduced. At heavy loads during normal switching, when the FB pin is above the 750mV reference, the DL output is high and the low-side MOSFET is on. During this time, the voltage across the inductor is approximately $-V_{OUT}$. This causes a down-slope or falling di/dt in the inductor. If the load di/dt is not much faster than the -di/dt in the inductor, then the inductor current will tend to track the falling load current. This will reduce the excess inductive energy that must be absorbed by the output capacitor, therefore a smaller capacitance can be used.

The following can be used to calculate the needed capacitance for a given dI_{LOAD}/dt. Peak inductor current is shown by the next equation.

Applications Information (continued)

$$I_{LPK} = 3A + \frac{1}{2} \times 0.511A = 3.26A$$

Rate of change of load current is

$$\frac{dI_{LOAD}}{dt} = \frac{0.6A}{1\mu s}$$

I_{MAX} = maximum load release = 3A

$$C_{OUT} = I_{LPK} \times \frac{L \times \frac{I_{LPK}}{V_{OUT}} - \frac{I_{MAX}}{dI_{LOAD}} \times dt}{2 \times (V_{PK} - V_{OUT})}$$

$$C_{OUT} = 3.26A \times \frac{2\mu H \times \frac{3.26A}{1V} - \frac{3A}{0.6A} \times 1\mu s}{2 \times (1.05V - 1V)}$$

$$C_{OUT} = 50\mu F$$

Note that C_{OUT} is much smaller in this example, 50µF compared to 207µF based upon a worst-case load release. To meet the two design criteria of minimum 50µF and maximum 78mΩ ESR, select two capacitors rated at 33µF and 15mΩ ESR or less.

It is recommended that an additional small capacitor be placed in parallel with C_{OUT} in order to filter high frequency switching noise.

Stability Considerations

Unstable operation is possible with adaptive on-time controllers, and usually takes the form of double-pulsing or ESR loop instability.

Double-pulsing occurs due to switching noise seen at the FB input or because the FB ripple voltage is too low. This causes the FB comparator to trigger prematurely after the minimum off-time has expired. In extreme cases the noise can cause three or more successive on-times. Double-pulsing will result in higher ripple voltage at the output, but in most applications it will not affect operation. This form of instability can usually be avoided by providing the FB pin with a smooth, clean ripple signal that is at least 10mVp-p, which may dictate the need to increase the ESR of the output capacitors. It is also imperative to provide a proper PCB layout as discussed in the Layout Guidelines section.

Another way to eliminate doubling-pulsing is to add a small (~ 10pF) capacitor across the upper feedback resistor, as shown in Figure 6. This capacitor should be left unpopulated unless it can be confirmed that double-pulsing exists. Adding the C_{TOP} capacitor will couple more ripple into FB to help eliminate the problem. An optional connection on the PCB should be available for this capacitor.

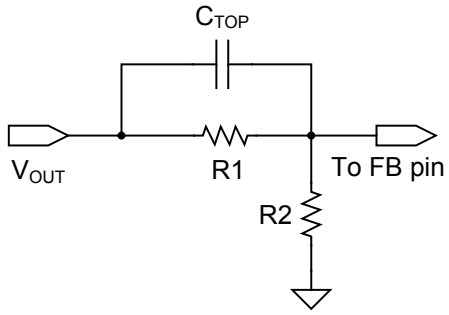


Figure 6 — Capacitor Coupling to FB Pin

ESR loop instability is caused by insufficient ESR. The details of this stability issue are discussed in the ESR Requirements section. The best method for checking stability is to apply a zero-to-full load transient and observe the output voltage ripple envelope for overshoot and ringing. Ringing for more than one cycle after the initial step is an indication that the ESR should be increased.

One simple way to solve this problem is to add trace resistance in the high current output path. A side effect of adding trace resistance is a decrease in load regulation.

ESR Requirements

A minimum ESR is required for two reasons. One reason is to generate enough output ripple voltage to provide 10mVp-p at the FB pin (after the resistor divider) to avoid double-pulsing.

The second reason is to prevent instability due to insufficient ESR. The on-time control regulates the valley of the output ripple voltage. This ripple voltage is the sum of the two voltages. One is the ripple generated by the ESR, the other is the ripple due to capacitive charging

Applications Information (continued)

and discharging during the switching cycle. For most applications, the total output ripple voltage is dominated by the output capacitors, typically SP or POSCAP devices. For stability the ESR zero of the output capacitor should be lower than approximately one-third the switching frequency. The formula for minimum ESR is shown by the following equation.

$$ESR_{MIN} = \frac{3}{2 \times \pi \times C_{OUT} \times f_{SW}}$$

Using Ceramic Output Capacitors

When applications use ceramic output capacitors, the ESR is normally too small to meet the previously stated ESR criteria. In these applications it is necessary to add a small signal injection network as shown in Figure 7. In this network R_L and C_L filter the LX switching waveform to generate an in-phase ripple voltage comparable to the ripple seen on higher ESR capacitors. C_C is a coupling capacitor used to AC couple the generated ripple onto the FB pin. Capacitor C_{FF} is required for min C_{OUT} applications. This capacitor introduces a lead/lag into the control with the maximum phase placed at 1/2 f_{SW} for added stability.

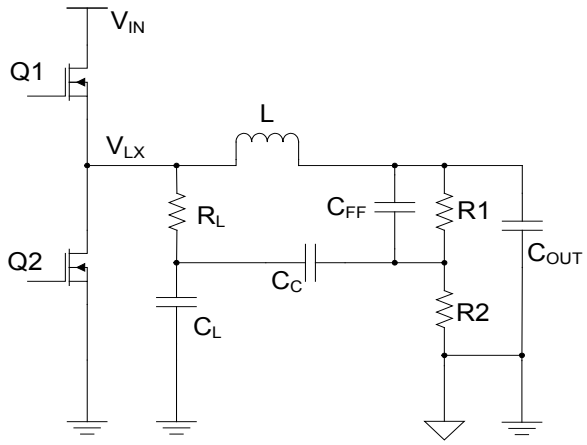


Figure 7 — Signal Injection Circuit

The values of R_L, C_L, C_C and C_{FF} are dependent on the conditions of the specific application such as V_{IN}, V_{OUT}, f_{SW} and I_{OUT}. For switching frequencies ranging from 600kHz to 800kHz, calculations plus experimental test results show that the following combination of R_L=2.5kΩ, C_L=10nF, C_C=68pF and C_{FF}=39pF can be used for many output voltages and loads.

Output Voltage Dropout

The output voltage adjustable range for continuous-conduction operation is limited by the fixed 320ns (typical) minimum off-time. When working with low input voltages, the duty-factor limit must be calculated using worst-case values for on and off times. The duty-factor limitation is shown by the next equation.

$$DUTY = \frac{T_{ON(MIN)}}{T_{ON(MIN)} + T_{OFF(MAX)}}$$

The inductor resistance and MOSFET on-state voltage drops must be included when performing worst-case dropout duty-factor calculations.

System DC Accuracy — V_{OUT} Controller

Three factors affect V_{OUT} accuracy: the trip point of the FB error comparator, the ripple voltage variation with line and load, and the external resistor tolerance. The error comparator offset is trimmed so that under static conditions it trips when the feedback pin is 750mV, ±1%.

The on-time pulse from the SC173A in the design example is calculated to give a pseudo-fixed frequency of 800kHz. Some frequency variation with line and load is expected. This variation changes the output ripple voltage. Because adaptive on-time converters regulate to the valley of the output ripple, ½ of the output ripple appears as a DC regulation error. For example, if the output ripple is 50mV with V_{IN} = 5 volts, then the measured DC output will be 25mV above the comparator trip point. If the ripple increases to 30mV with V_{IN} = 5.5V, then the measured DC output will be 15mV above the comparator trip. The best way to minimize this effect is to minimize the output ripple.

To compensate for valley regulation, it may be desirable to use passive droop. Take the feedback directly from the output side of the inductor and place a small amount of trace resistance between the inductor and output capacitor. This trace resistance should be optimized so that at full load the output droops to near the lower regulation limit. Passive droop minimizes the required output capacitance because the voltage excursions due to load steps are reduced as seen at the load.

Applications Information (continued)

The use of 1% feedback resistors may result in up to an additional 1% error. If tighter DC accuracy is required, resistors with lower tolerances should be used.

The output inductor value may change with current. This will change the output ripple and therefore will have a minor effect on the DC output voltage. The output ESR also affects the output ripple and thus has a minor effect on the DC output voltage.

Switching Frequency Variation

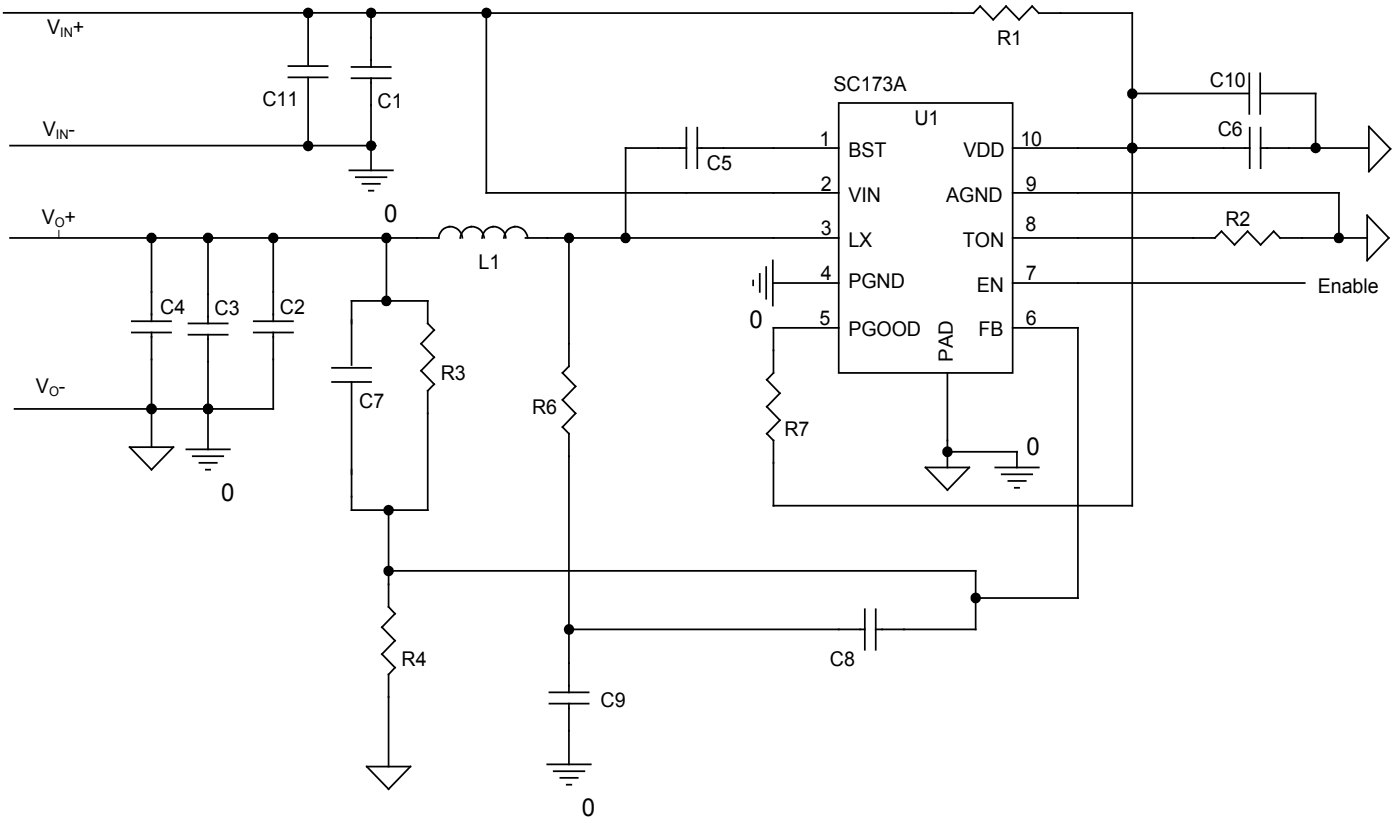
The switching frequency will vary depending on line and load conditions. The line variations are a result of fixed propagation delays in the on-time one-shot, as well as unavoidable delays in the power FET switching. As V_{IN} increases, these factors make the actual DH on-time slightly longer than the ideal on-time. The net effect is that frequency tends to fall slightly with increasing input voltage.

The switching frequency also varies with load current as a result of the power losses in the MOSFETs and the inductor. For a conventional PWM constant-frequency converter, as load increases the duty cycle also increases slightly to compensate for IR and switching losses in the MOSFETs and inductor. A adaptive on-time converter must also compensate for the same losses by increasing the effective duty cycle (more time is spent drawing energy from V_{IN} as losses increase). The on-time is essentially constant for a given V_{OUT} and V_{IN} combination, to offset the losses the off-time will tend to reduce slightly as load increases. The net effect is that switching frequency increases slightly with increasing load.

Switching Node Voltage Spike

Due to parasitic board inductance, the transient LX pin voltage at the point of measurement may appear larger than that which exists on silicon. With an input multilayer ceramic capacitor of 10uF placed less than 3mm away from the PVIN pin, the device is designed and guaranteed to tolerate the short transient voltages, of maximum 20ns duration, that will appear on the LX pin due to the deadtime diode conduction, as long as the transient voltage on PVIN is less than 6.0V. The time duration of the transient LX pin voltage is measured on the voltage portion which is either over 6.0V for positive voltage spike or under -1V for negative voltage spike. The LX voltage is measured from the LX pin to the PGND pin by using a probing loop which is as short as possible to minimize or eliminate the switching noise pick up.

Layout Guideline



Schematic for layout illustration

Since the SC173A has integrated switches, special consideration should be given to board layout. Let us use the schematic shown above as an example. The board level layout is illustrated in the following four layers.

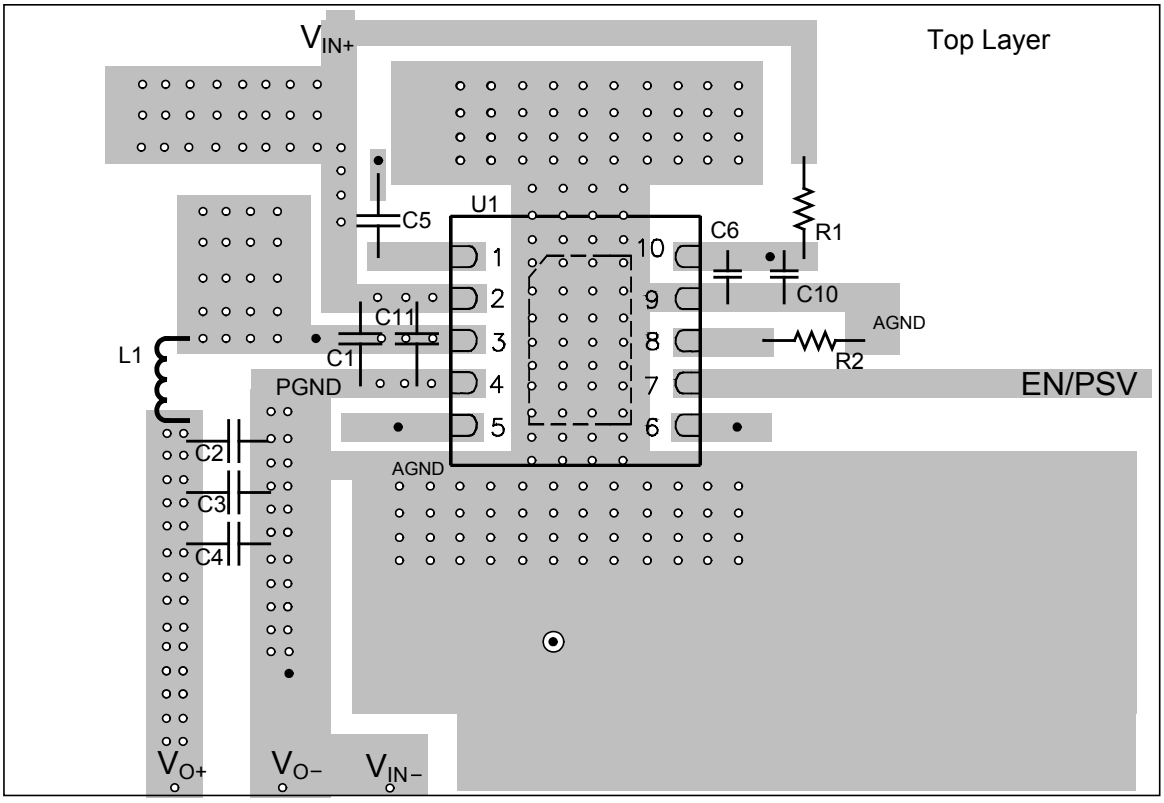
As shown on the top layer layout, U1 is the switching regulator SC173A. C1 and C11 serve as the decoupling capacitor for the buck converter power train. C11, with a value between 1nF and 10nF, is the high frequency filtering capacitor. It is recommended to put C1 and C11 as close as possible to the SC173A to get the best decoupling performance, with C11 closest. C1, with a value of 10uF, should be placed no more than 3mm away from the VIN pin. L1 is the output filtering inductor. C2, C3 and C4 are the output filtering capacitors. C5 is the boostrap capacitor. Pin 10 (VDD) is the input bias power for the internal circuits. It is recommended to get the power from VIN through an RC filtering network consisted of R1, C6 and C10. The value of R1 can be between 3.01Ω and 10Ω and the capacitance of C10 should be above 1μF. C6, with a value of 1nF, is the high frequency filtering capacitor. The locations of C6 and C10 should be as close as possible to pins 9 and 10, with C6 closest, to get the best possible filtering result. R2 is the on-time programming resistor. R2 should be located as close as possible to pin 8 and it should return to analog ground. Pull EN high (above 1V) or permit it to float to enable the part with automatic power save enabled. Connect EN to AGND to disable the switching regulator.

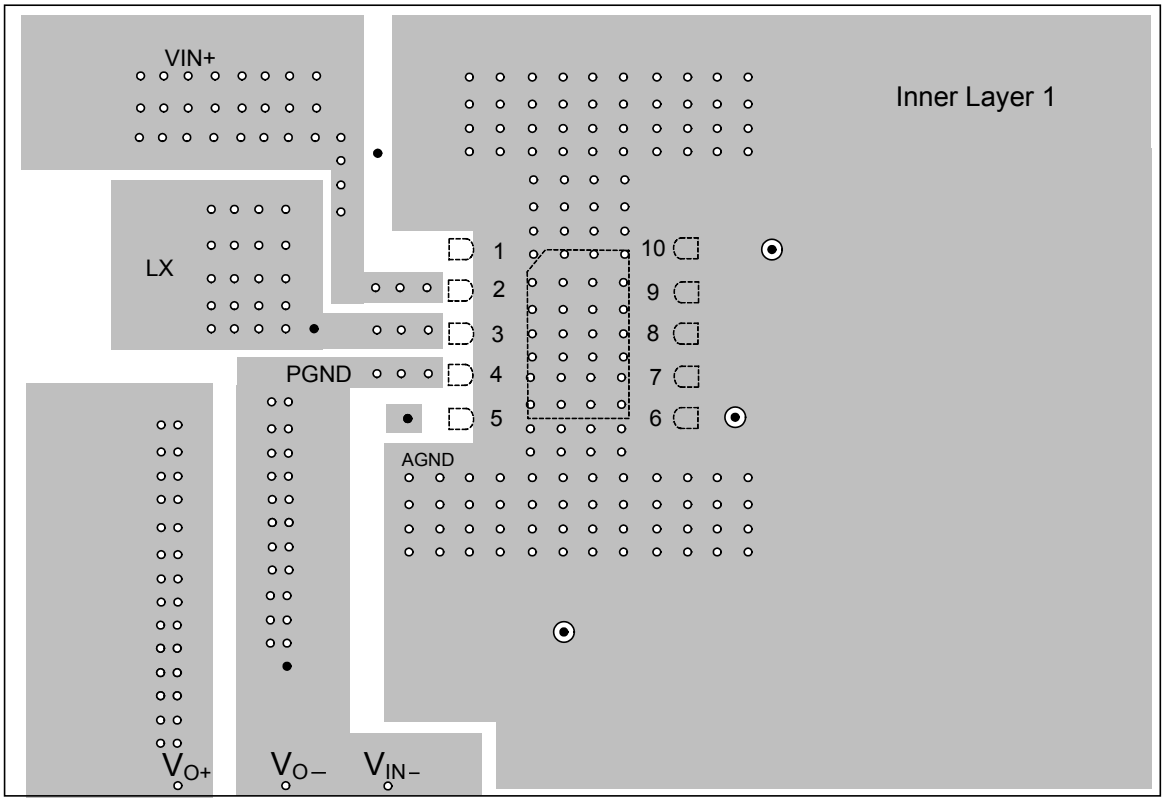
Since there are two integrated MOSFETs inside the SC173A that will dissipate a lot of power, to help spread the heat out of the IC more efficiently, there is a thermal pad underneath the SC173A serving as a heat sink. To enlarge the heat sinking area, a large copper plane under the thermal pad as shown on the top layer is recommended.

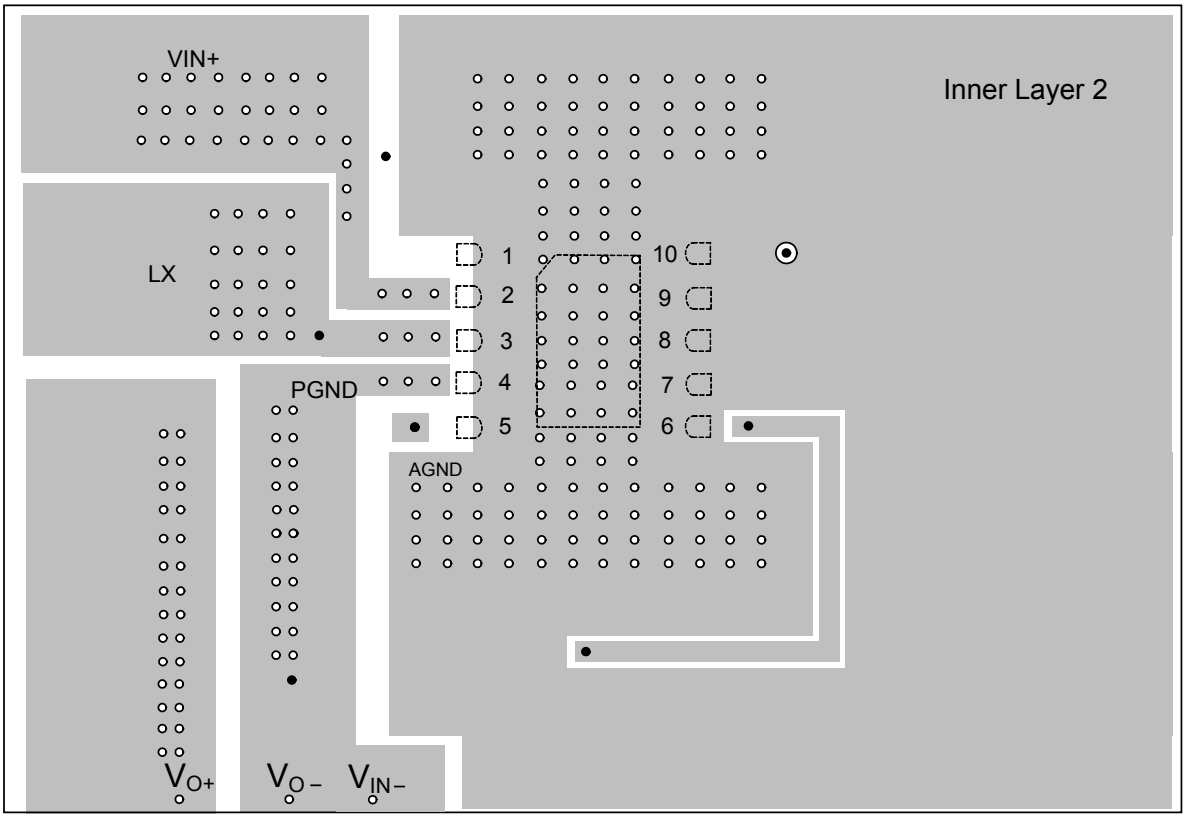
On inner layer 2, a large analog ground plane (AGND) on the right hand side is connected to the thermal pad underneath the SC173A using vias. Thus the heat generated inside the SC173A can be spread through the vias to the

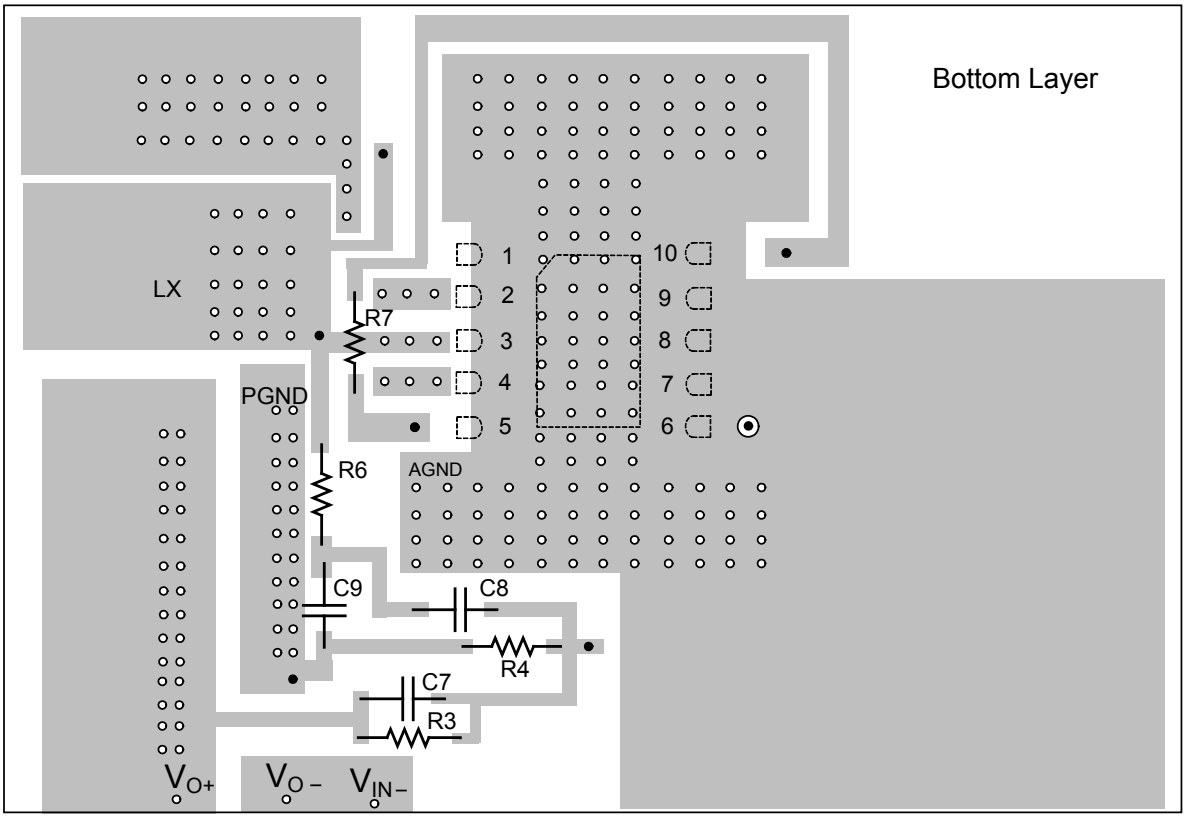
inner layers to expand the heat sinking area.

On the bottom layer, the resistor network composed of R3 and R4 determines the output voltage. C7 is the feed forward capacitor which helps to stabilize the circuit. R6 in series with C9 is connected to the LX pin (through the via) to the power ground. C8 is the coupling capacitor which injects the ramp signal generated on C9 to the FB pin of the SC173A. R7 is the pull up resistor for the PGOOD pin.

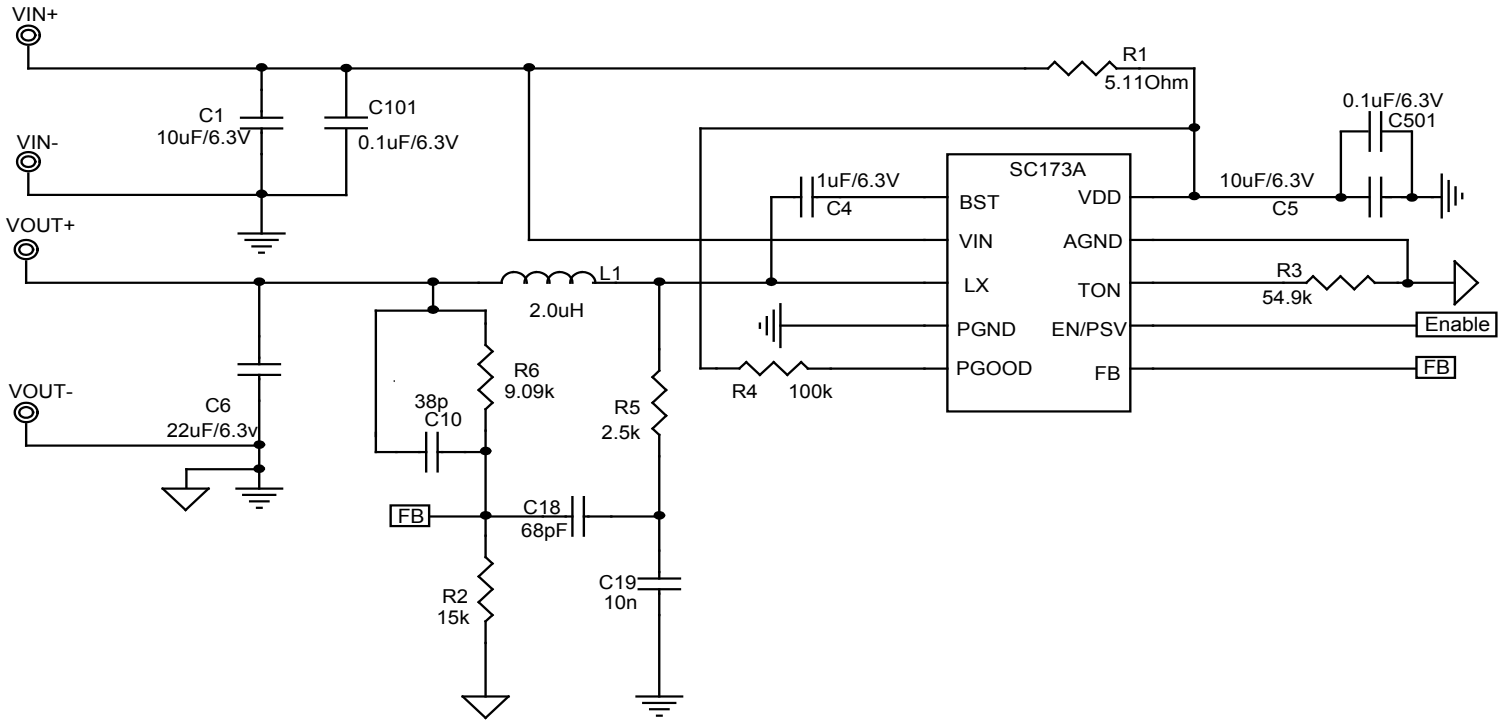




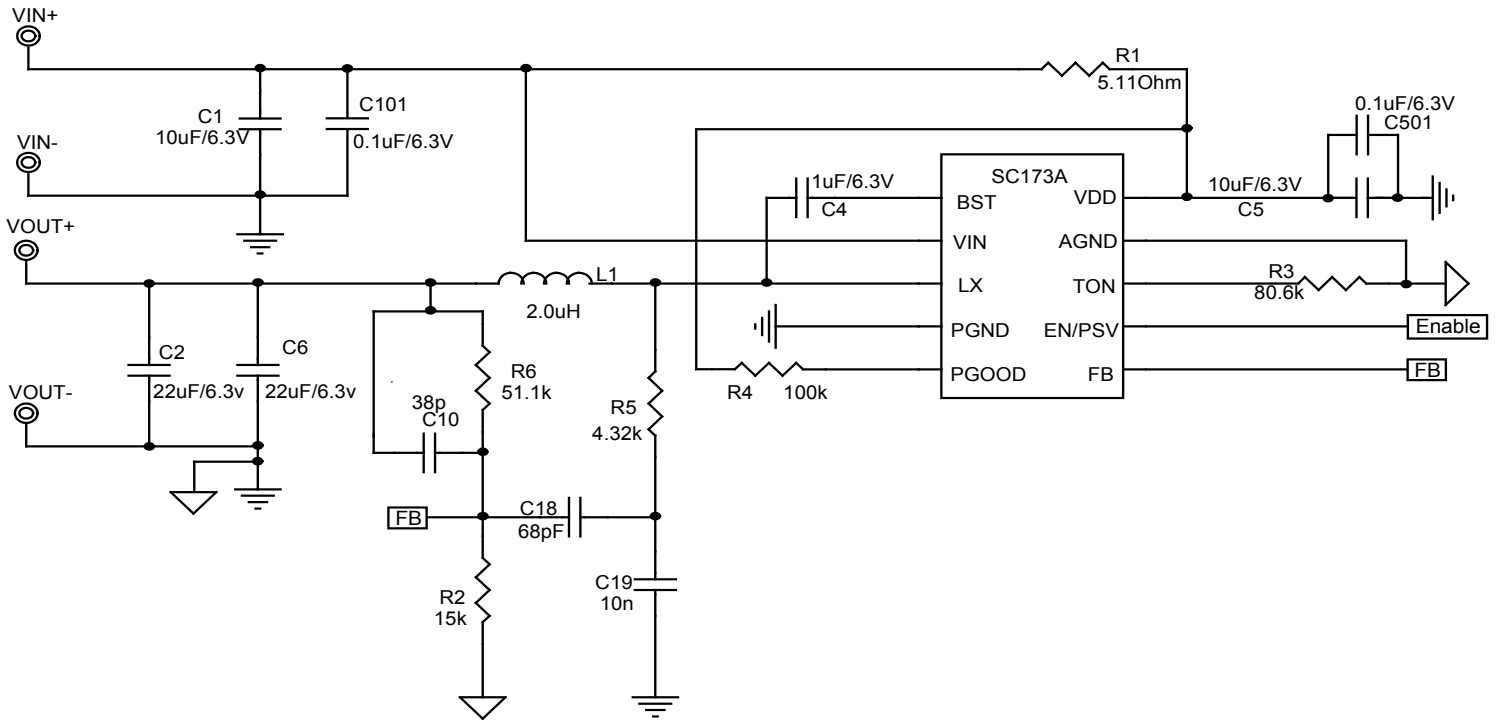




Typical Application Circuits



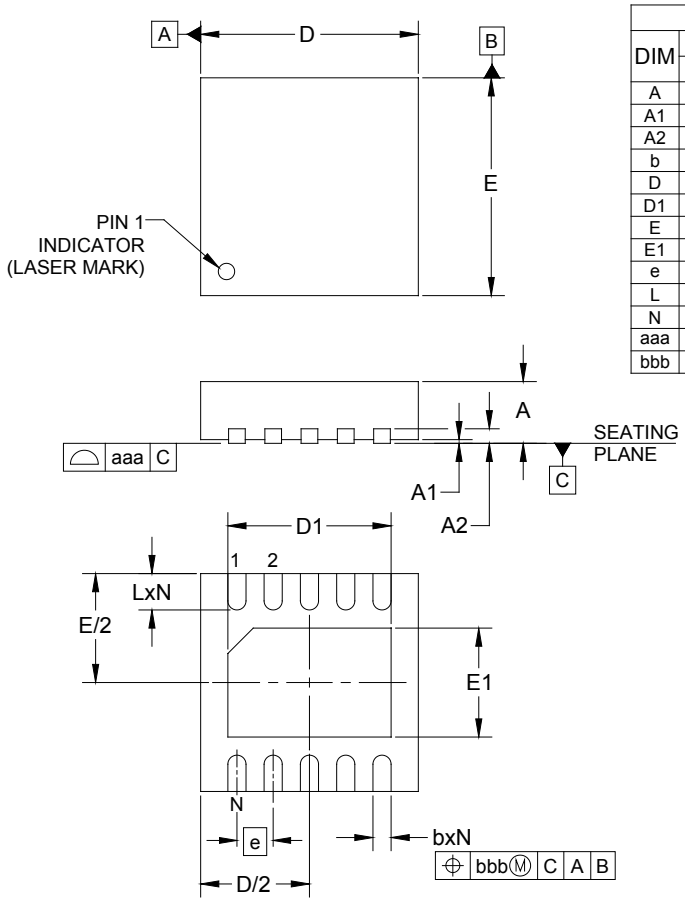
Application Circuit: Buck Converter with 1.2V out and 0 to 3A load current (Vin=5V)



Application Circuit: Buck Converter with 3.3V out and 0 to 3A load current (Vin=5V)

SEMTECH

Outline Drawing - MLPD-10 3x3

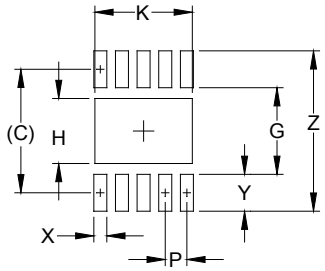


DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.031	-	.039	0.80	-	1.00
A1	.000	-	.002	0.00	-	0.05
A2	-	(.008)	-	-	(0.20)	-
b	.008	.010	.012	0.20	0.25	0.30
D	.114	.118	.122	2.90	3.00	3.10
D1	.087	.089	.091	2.20	2.25	2.30
E	.114	.118	.122	2.90	3.00	3.10
E1	.057	.059	.061	1.45	1.50	1.55
e	.020 BSC			0.50 BSC		
L	.018	.020	.022	0.45	0.50	0.55
N	10			10		
aaa	.003			0.08		
bbb	.004			0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS TERMINALS.

Land Pattern - MLPD-10 3x3



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.112)	(2.85)
G	.079	2.00
H	.059	1.50
K	.089	2.25
P	.020	0.50
X	.012	0.30
Y	.033	0.85
Z	.146	3.70

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

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