STRUCTURE Silicon Monolithic Integrated Circuit
TYPE Step down 1ch DC/DC converter Controller for Lap top PC
PRODUCT SERIES **BD95513MUV**
FEATURES
- Built in H^3REG DC/DC controller
- Switching Frequency Variable (f=200kHz～600kHz)
- Built in N-MOS FET (typ:120mΩ)

○ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

Parameter	Symbol	Limit	Unit
Input Voltage 1	Vcc	7 *1	V
Input Voltage 2	VDD	7 *1	V
Input Voltage 3	AVIN	30 *1	V
Input Voltage 4	VIN	30 *1	V
EXTVCC Voltage	EXTVcc	7 *1	V
BOOT Voltage	BOOT	35	V
BOOT-SW Voltage	BOOT-SW	7 *1	V
Output Feedback Voltage	FB	VCC	V
SS / FS / MODE Voltage	SS/FS/MODE	VCC	V
VREG Voltage	VREG	VCC	V
EN/CTL Input Voltage	EN/CTL	7 *1	V
PGOOD Voltage	PGOOD	7 *1	V
Output Current (Average)	Isw	3 *1	A
Power Dissipation 1	Pd1	0.38*2	W
Power Dissipation 2	Pd2	0.88*3*6	W
Power Dissipation 3	Pd3	2.06*4*6	W
Power Dissipation 4	Pd4	4.56*5*6	W
Operating Temperature Range	Topr	-10～+100	℃
Storage Temperature Range	Tstg	-55～+150	℃
Maximum Junction Temperature	Tjmax	+150	℃

*1 Not to exceed Pd, ASO, and Tjmax=150℃.
*2 Reduced by 3.0mW for each increase in Ta of 1℃ over 25℃ (when don't mounted on a heat radiation board)
*3 Reduced by 7.0mW for increase in Ta of 1℃ over 25℃. (when mounted on a board 70.0mm×70mm×1.6mm Glass-epoxy PCB which has 1 layer. (Copper foil area : 0mm^2))
*4 Reduced by 16.5mW for increase in Ta of 1℃ over 25℃. (when mounted on a board 70.0mm×70mm×1.6mm Glass-epoxy PCB which has 4 layers. (1st and 4th copper foil area : 20.2mm^2, 2nd and 3rd copper foil area : 5505mm^2))
*5 Reduced by 36.5mW for increase in Ta of 1℃ over 25℃. (when mounted on a board 70.0mm×70mm×1.6mm Glass-epoxy PCB which has 4 layers. (All copper foil area : 5505mm^2))
*6 It is the value when reverse side is soldered. Incase not soldered, power dissipation is decreased.

○OPERATING CONDITIONS (Ta=25℃)

Parameter	Symbol	MIN	MAX	Unit
Input Voltage 1	Vcc	4.5	5.5	V
Input Voltage 2	VDD	4.5	5.5	V
Input Voltage 3	AVIN	4.5	28	V
Input Voltage 4	VIN	4.5	28	V
EXTVCC Voltage	EXTVcc	4.5	5.5	V
BOOT Voltage	BOOT	4.5	33	V
SW Voltage	SW	-0.7	28	V
BOOT-SW Voltage	BOOT-SW	4.5	5.5	V
MODE Input Voltage	MODE	0	5.5	V
EN/CTL Input Voltage	EN/CTL	0	5.5	V
PGOOD Voltage	PGOOD	0	5.5	V
Minimum ON Time	tonmin	-	100	nsec

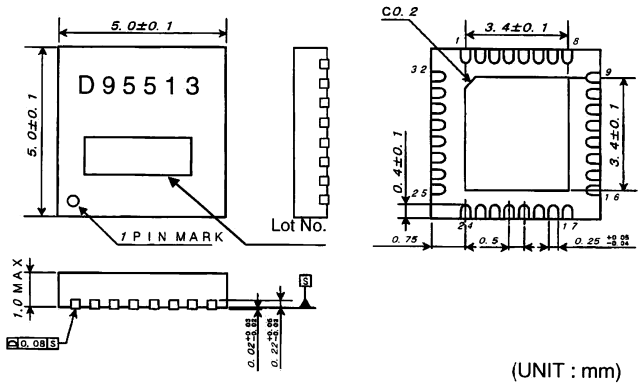
★ This product is not designed for protection against radioactive rays.

Status of this document
The Japanese version of this document is the official specification.
This translated version is intended only as a reference, to aid in understanding the official version.
If there are any differences between the original and translated versions of this document, the official Japanese language version takes priority.

○ELECTRICAL CHARACTERISTICS (unless otherwise noted, Ta=25℃ AVIN=12V, VCC=VDD=VREG, EN/CTL=5V, MODE=0V, RFS=180kΩ)

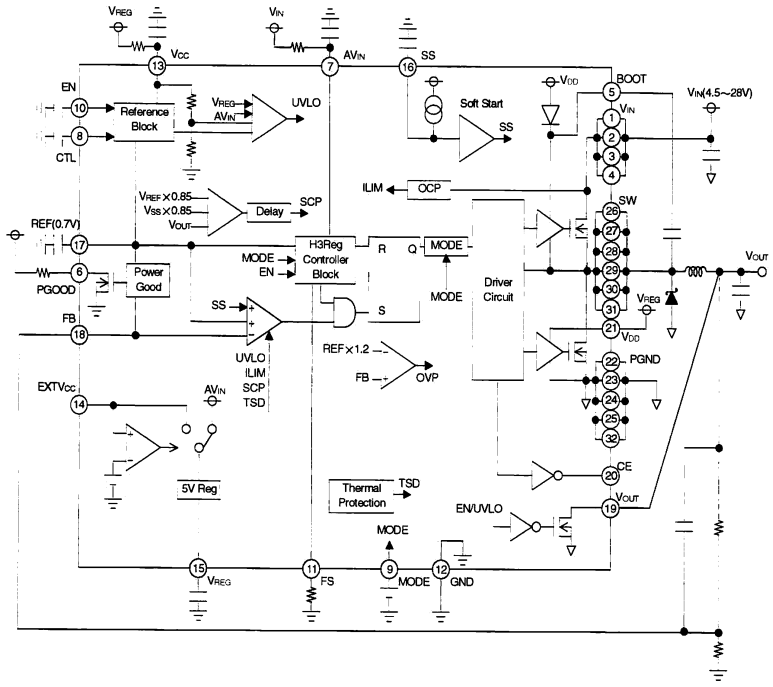
Parameter	Symbol	Standard Value			Unit	Condition
		MIN	TYP	MAX		
[Whole Device block]						
AVIN bias current 1	IIN1	-	1200	1800	μA	
AVIN bias current 2	IIN2	-	150	250	μA	EXTVCC=5V
AVIN standby current	IINstb	-	0	10	μA	CTL=EN=0V
EN Low voltage	ENlow	GND	-	0.8	V	
EN High voltage	ENhigh	2.3	-	5.5	V	
EN bias current	IEN	-	12	20	μA	
CTL Low voltage	CTLlow	GND	-	0.8	V	
CTL High voltage	CTLhigh	2.3	-	5.5	V	
CTL bias current	ICTL	-	1	6	μA	
[5V Linear regulator block]						
VREG output voltage	VREG	4.90	5.00	5.10	V	AVIN=6.0 to 25V
Maximum current	IREG	200	-	-	mA	
[5V switch block]						
EXTVCC input threshold voltage	EVCC_UVLO	4.2	4.4	4.6	V	EXTVCC:Sweep up
Switch resistance	REVCC	-	1.0	2.0	Ω	
[Under Voltage Locked Out block]						
AVIN threshold voltage	AVIN_UVLO	4.1	4.3	4.5	V	VCC:Sweep up
AVIN hysteresis voltage	dAVIN_UVLO	100	160	220	mV	VCC:Sweep down
VREG threshold voltage	VREG_UVLO	4.1	4.3	4.5	V	VREG:Sweep up
VREG hysteresis voltage	dVREG_UVLO	100	160	220	mV	VREG:Sweep down
[H^3REG^{TM} block]						
ON Time	ton	400	500	600	nsec	
MAX ON Time	tonmax	10.0	22.0	35.0	μsec	
MIN OFF Time	toffmin	-	450	550	nsec	
[FET Driver block]						
High side ON resistance	Ron_high	-	120	200	mΩ	
Low side ON resistance	Ron_low	-	120	200	mΩ	
[SCP block]						
SCP startup voltage	VSCP	0.420	0.490	0.560	V	@VFB:30%down
Delay time	tSCP	0.5	1	2	ms	
[OVP block]						
OVP setting voltage	VOVP	0.800	0.840	0.880	V	@VFB:20%up
[Soft start block]						
Charge current	Iss	1.4	2.2	3.0	μA	
Standby voltage	Vss_stb	-	-	100	mV	
[Current Limit block]						
Output current control	IOCP	3	-	-	A	
[Output Voltage Sense block]						
Feedback pin voltage 1	VFB1	0.693	0.700	0.707	V	
Feedback pin voltage 2	VFB2	0.690	0.700	0.710	V	Ta=-10℃ to 100℃ Iout=0A to 2A
Feedback pin bias current	IFB	-100	0	100	nA	
[Mode block]						
SLLM	VthSLLM	VCC-0.5	-	VCC	V	SLLM (Maximum LG offtime:∞)
Forced continuous mode	VthCONT	GND	-	0.5	V	Continuos mode
Open voltage	VMODE	1.5	-	3.0	V	
[Power Good block]						
VFB Power Good Low voltage	VFB PL	0.605	0.630	0.655	V	@VFB:10%down
VFB Power Good High voltage	VFB PH	0.745	0.770	0.795	V	@VFB:10%up

○PHYSICAL DIMENSIONS



(UNIT : mm)

○Block diagram

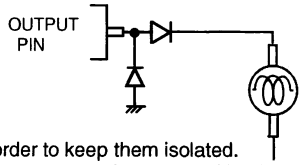


○Pin No. Pin name

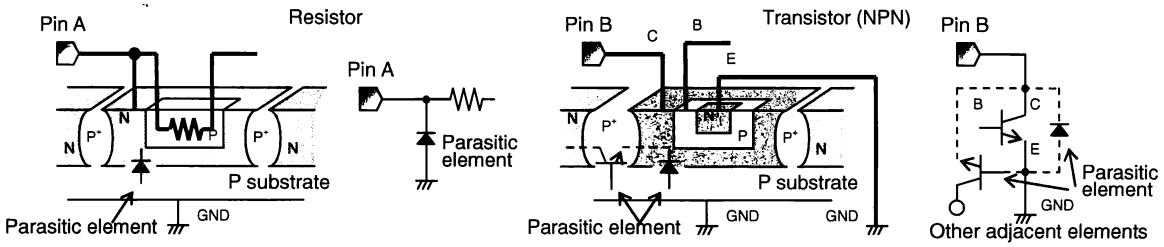
PIN No.	PIN name
1	VIN
2	VIN
3	VIN
4	VIN
5	BOOT
6	PGOOD
7	AVIN
8	CTL
9	MODE
10	EN
11	FS
12	GND
13	VCC
14	EXTVCC
15	VREG
16	SS
17	REF
18	FB
19	VOUT
20	CE
21	VDD
22	PGND
23	PGND
24	PGND
25	PGND
26	SW
27	SW
28	SW
29	SW
30	SW
31	SW
32	PGND

○NOTES FOR USE

1. Absolute maximum ratings
   An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.
2. GND voltage
   The potential of GND, PGND1, PGND2 pin must be minimum potential in all operating conditions.
3. Thermal design
   Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.
4. Inter-pin shorts and mounting errors
   Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if pins are shorted together.
5. Actions in strong electromagnetic field
   Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.
6. ASO
   When using the IC, set the output transistor so that it does not exceed absolute maximum ratings or ASO.
7. Testing on application boards
   When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting or storing the IC.
8. Electrical characteristics
   The electrical characteristics in the Specifications may vary depending on ambient temperature, power supply voltage, circuit(s) externally applied, and/or other conditions. It is therefore requested to carefully check them including transient characteristics.
9. Not of a radiation-resistant design.
10. In the event that load containing a large inductance component is connected to the output terminal, and generation of back-EMF at the start-up and when output is turned OFF is assumed, it is requested to insert a protection diode.



11. Regarding input pin of the IC
    This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:
    When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
    When GND > Pin B, the P-N junction operates as a parasitic transistor.
    Parasitic diodes can occur inevitable in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.



12. Ground Wiring Pattern
    When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the ground potential of application so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.
13. Operating ranges
    If it is within the operating ranges, certain circuit functions and operations are warranted in the working ambient temperature range. With respect to characteristic values, it is unable to warrant standard values of electric characteristics but there are no sudden variations in characteristic values within these ranges.
14. Thermal shutdown circuit
    This IC is provided with a built-in thermal shutdown (TSD) circuit, which is activated when the chip temperature reaches the threshold value listed below. When TSD is on, the device goes to high impedance mode. Note that the TSD circuit is provided for the exclusive purpose shutting down the IC in the presence of extreme heat, and is not designed to protect the IC per se or guarantee performance when or after extreme heat conditions occur. Therefore, do not operate the IC with the expectation of continued use or subsequent operation once the TSD is activated.

TSD ON temperature [℃] (typ.)	Hysteresis temperature[℃] (typ.)
175	15

15. Heat sink (FIN)
    Since the heat sink (FIN) is connected with the Sub, short it to the GND.

Notes

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