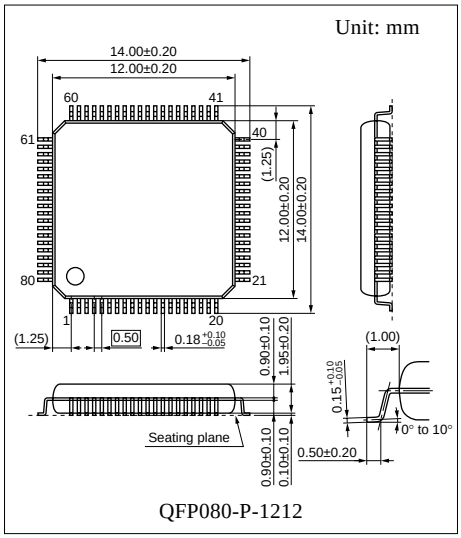
AN8725FH

Semiconductor laser power control IC

■ Overview

The AN8725FH is a laser driver IC that can set a laser emitting level to a maximum precision in recording and playback of an optical recording equipment such as PD, and can modulate a laser light in tune with the external signal.



QFP080-P-1212

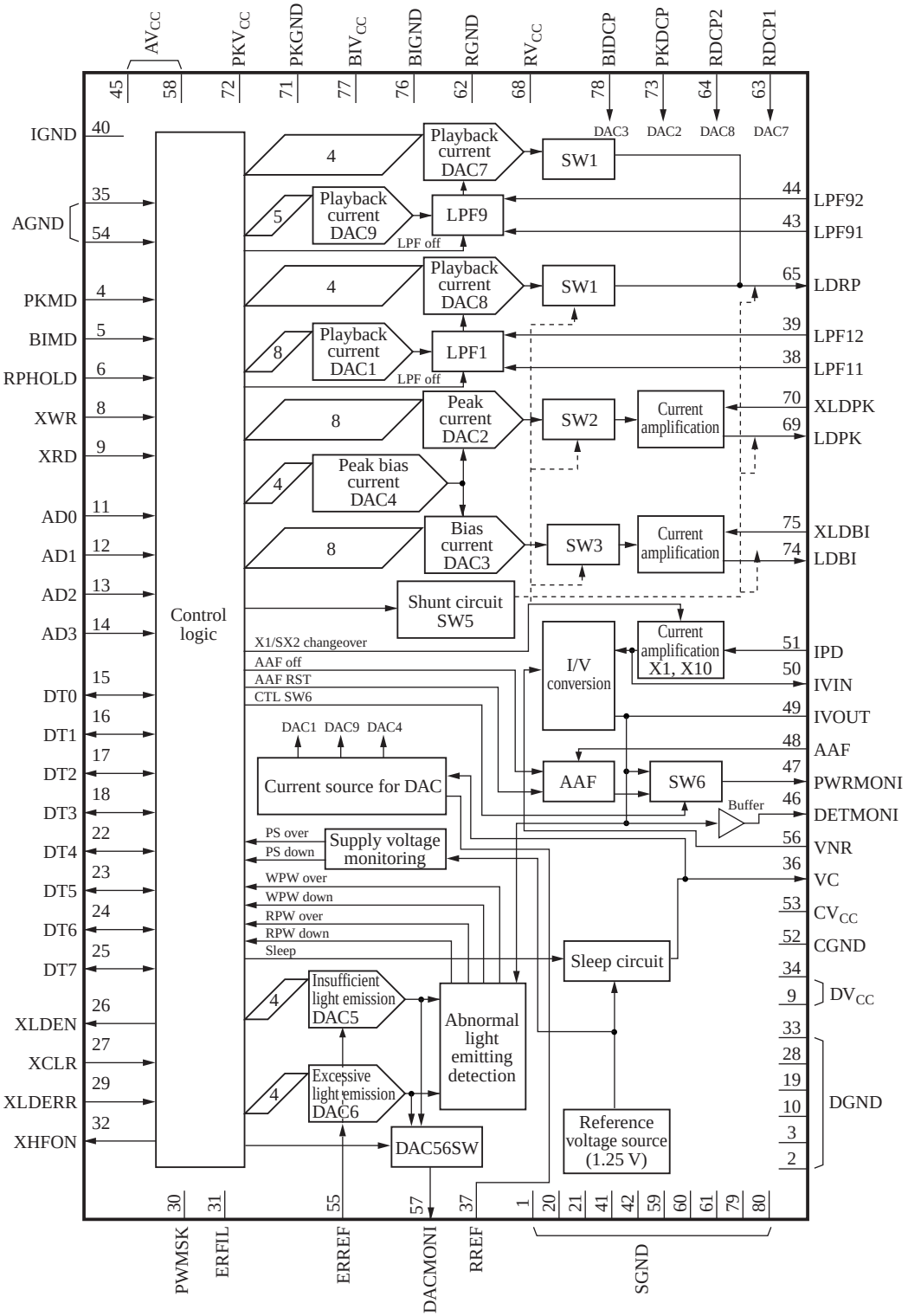
■ Features

- Digital setting of playback current, peak current, bias current and abnormal light emitting level
- Peak current and bias current can be modulated by the external signal.
- Driving current set-up (digital set-up)
  For playback: 8-bit + 4-bit (0 mA to 80 mA)
  5-bit + 4-bit (0 mA to 150 mA)
  For peak: 4-bit + 8-bit (0 mA to 150 mA)
  For bias: 4-bit + 8-bit (0 mA to 150 mA)
- Laser output light monitoring circuit built-in
- Abnormal light emitting detecting function built-in:
  Possible to set up excessive and insufficient light emitting levels with 4-bit DAC for playback and recording, respectively.
- Supply voltage abnormality detection:
  Voltage down (3.9 V or less), voltage up (6.1 V or more)

■ Applications

- Optical disk drive

■ Block Diagram



■ Pin Descriptions

Note) Description on notations of "Category" in the following list:

IN : Input pin
IND : Input pin (pull-down with 100 kΩ)
INU : Input pin (pull-up with 100 kΩ)
OUT: Output pin
I/O : Input/output pin (pull-down with 100 kΩ)
PS : Power supply/GND pin
MSC : Parts connecting pin, etc.
A: Analog function
D: Digital function

Pin No.	Symbol	Category		Description
1	SGND	PS	D	Pin connected to the chip substrate. Must be used in the same potential as other GND pins.
2	DGND	PS	D	GND pin exclusive for a logic circuit. Must be used in the same potential as other GND pins.
3	DGND	PS	D	
4	PKMD	IND	D	Peak current modulation signal input pin. In high-level, the current set up with DAC2 is superimposed on LD.
5	BIMD	IND	D	Bias current modulation signal input pin. In high-level, the current set up with DAC3 is superimposed on LD.
6	RPHOLD	IND	D	Record gate signal input pin. Inputs a low-level in playback and a high-level in recording. Switches an amp. of light monitoring signal, abnormally emitted light detection level and on/off of HF module.
7	XWR	INU	D	Register writing signal pin. Selects a register specified by address in a fall edge and writes a bus data on the register of the address specified in the rise edge.
8	XRD	INU	D	Register read-out signal pin. Register data of the address specified in low appears on the bus.
9	DV_{CC}	PS	D	Power supply pin exclusive for a logic circuit. Must be used in the same potential as other power supply pins.
10	DGND	PS	D	GND pin exclusive for a logic circuit. Must be used in the same potential as other GND pins.
11	AD0	IND	D	4-bit address pin for registers. Selects the register to be accessed.
12	AD1	IND	D	
13	AD2	IND	D	
14	AD3	IND	D	
15	DT0	I/O	D	Data I/O 8-bit bus pin. The bus to set the data to be written on a register and to read out the data of a register.
16	DT1	I/O	D	
17	DT2	I/O	D	
18	DT3	I/O	D	
19	DGND	PS	D	GND pin exclusive for a logic circuit. Must be used in the same potential as other GND pins.

■ Pin Descriptions (continued)

Pin No.	Symbol	Category		Description
20	SGND	PS	D	Pin connected to the chip substrate.
21	SGND	PS	D	Must be used in the same potential as other GND pins.
22	DT 4	I/O	D	Data I/O 8-bit bus pin.
23	DT 5	I/O	D	The bus to set the data to be written on a register and to read out the data
24	DT 6	I/O	D	of a register.
25	DT 7	I/O	D	
26	XLDEN	INU	D	LD enable input pin. In a high-level or open mode, LD becomes off and open. This state is suited to check the LD characteristics in keeping a connection to the IC. At the time power off, both ends of LD are short-circuited by the IC for protection. In the low-level, it returns to a normal operation.
27	XCLR	IND	D	Clear signal input pin. Sets an LDDENB register to "0" in the low-level and presets the status of each DAC and each switch to an initial state as defined separately. But six registers for an abnormal detection are not cleared. In this state, each output of a current amplification 1, 2, 3 are in the off state and a shunt circuit becomes on to continue to protect LD. Setting this pin to the high-level and the LDDENB register to "1", it returns to a normal operation.
28	DGND	PS	D	GND pin exclusive for a logic circuit. Must be used in the same potential as other GND pins.
29	XLDERR	OUT	D	Laser abnormality detection output pin. When a supply voltage or a laser light emission exceeds a fixed range, it goes to low-level. A supply voltage abnormality is detected for the voltage drop (3.9 V or less) or voltage rise (6.1 V or more). And an abnormal light emission is detected for an excessive or weaker light emission set up by 4-bit DAC5 and DAC6. This abnormality detection is latched so as to prevent it from being reset until ERRCLR register is set to "1". Further, each DAC output of a playback current, a peak current and a bias current can be set to off, a shunt circuit be set to on and LD between anode and GND be short-circuited by 100 Ω so that LD can be protected. This protection function is latched to keep it from being reset until ERRCLR is set to "1". Selection of either operation or non-operation for this operation can be made by an STPMSK register.
30	PWMSK	MSC	D	The pin to set up the mask time for a transitional response output that comes out at switching a detection level of excessive or insufficient light emission by RPHOLD. Set a mask time by an external capacitor between PWMSK and DGND and the resistor (10 kΩ) inside the IC. This pin is for a schmitt-trigger input.

■ Pin Descriptions (continued)

Pin No.	Symbol	Category		Description
31	ERFIL	MSC	D	Filter setting pin to avoid a detection error of laser abnormality caused by noise. Connect an external capacitor between ERFIL and DGND, and set a filter together with a resistor (10 kΩ) inside the IC. This pin is for schmitt-trigger input.
32	XHFON	OUT	D	HF module on/off control signal output pin. High corresponds to off and low to on.
33	DGND	PS	D	GND pin exclusive to a logic circuit. Must be used in the same potential as other GND pins.
34	DV_{CC}	PS	D	Power supply pin exclusive to a logic circuit. Must be used in the same potential as other power supply pins.
35	AGND	PS	A	GND pin exclusive to a analog circuit. Must be used in the same potential as other GND pins.
36	VC	MSC	A	Output pin for reference voltage (1.25 V). Connects a capacitor C between this pin and AGND for de-coupling.
37	RREF	MSC	A	Reference resistor connecting pin to determine an output current for each DAC. Connect a resistor of 10 kΩ between RREF and AGND.
38	LPF11	MSC	A	LPF characteristic setting pin for DAC1 and DAC8.
39	LPF12	MSC	A	Connect an external resistor between LPF11 and LPF12, and then capacitor between LPF12 and IGND to set up a cutoff frequency.
40	IGND	PS	A	GND pin for playback power supply setting DAC1, DAC9 and disturbance reduction LPF. Must be used in the same potential as other GND pins.
41	SGND	PS	D	Pin connected to the chip substrate.
42	SGND	PS	D	Must be used in the same potential as other GND pins.
43	LPF91	MSC	A	LPF characteristic setting pin for DAC9 and DAC7.
44	LPF92	MSC	A	Connect an external resistor between LPF91 and LPF92 and then capacitor between LPF92 and IGND to set a cutoff frequency.
45	AV_{CC}	PS	A	Power supply pin for an analog circuit, a reference supply voltage circuit, etc. Must be used in the same potential as other power supply pins.
46	DETMONI	OUT	A	Pin to monitor a signal for detecting abnormally emitted light. In a playback mode, the signal output is five times that in recording (ten times is posisible by a register setting). Has offset to VNR due to being outputted through a buffer of transistors.
47	PWRMONI	OUT	A	Laser emitting light monitor signal. In a low-level of RPHOLD, the amplifier output has 10 times gain compared with recording, and is equipped with AFF.

■ Pin Descriptions (continued)

Pin No.	Symbol	Category		Description
48	AAF	MSC	A	AAF characteristic setting pin for optical monitor circuit. Connect an external resistor, capacitor between AAF and IVOUT and set up a cutoff frequency.
49	IVOUT	OUT	A	I to V conversion signal output pin. Connect an external variable resistor between IVIN and IVOUT.
50	IVIN	MSC	A	I to V conversion resistor connection pin. Connect an external variable resistor between IVIN and IVOUT.
51	IPD	MSC	A	Pin photo diode (PD) connection pin. Connect a pin photo diode for detecting a semiconductor laser emitting light. Connect anode to this pin. Applicable to a source-type PD which has a typical value of 40 µA to 160 µA output in object lens output power of 1 mW.
52	CGND	PS	A	GND pin in an optical monitor circuit. Must be used in the same potential as other GND pins.
53	CV_{CC}	PS	A	Power supply pin in an optical monitor circuit. Must be used in the same potential as other power supply pins.
54	AGND	PS	A	GND pin exclusive to a analog circuit. Must be used in the same potential as other GND pins.
55	ERREF	IN	A	Abnormally emitting light detecting range setting pin. Sets a full scale voltage of DAC5 and DAC6. A setting range is VNR or more and input range of an external ADC or less.
56	VNR	IN	A	Reference level input pin for PWRMONI output. Input a reference voltage of 1.25 V of an external ADC.
57	DACMONI	OUT	A	DAC5, DAC6 monitor pin. DAC5 voltage is outputted when DAC56 SW register is low, DAC6 voltage is outputted when DAC6 voltage is high.
58	AV_{CC}	PS	A	Power supply pin for an analog circuit, a reference supply voltage circuit, etc. Must be used in the same potential as other power supply pins.
59	SGND	PS	D	Pin connected to the chip substrate. Must be used in the same potential as other GND pins.
60	SGND	PS	D	
61	SGND	PS	D	
62	RGND	PS	A	GND pin for the lead current setting DAC7 and DAC8. Must be used in the same potential as other GND pins.
63	RDCP1	MSC	A	Pin to connect a de-coupling capacitor to protect the output current of DAC7, the read current setting circuit, from disturbance by a switching noise such as peak current. (Connects a capacitor between RDCP1 and RGND.)

■ Pin Descriptions (continued)

Pin No.	Symbol	Category		Description
64	RDCP2	MSC	A	Pin to connect a de-coupling capacitor to protect the output current of DAC7, the read current setting circuit, from disturbance by a switching noise such as peak current. (Connects a capacitor between RDCP2 and RGND.)
65	LDRP	OUT	A	Source type read current (DAC1, DAC7, DAC8, DAC9) output pin. Possible to set up the range of 0 mA to 150 mA in the precision of 8-bit + 4-bit + 5-bit + 4-bit. Output voltage range is 1.0 V to 3.5 V.
66	N.C.	—	—	N.C. pin.
67	N.C.	—	—	Open the pin or connect to GND.
68	RV_{CC}	PS	A	Power supply pin for read current setting DAC7, DAC8. Consumes approximately a quarter of the necessary read current. Must be used in the same potential as other power supply pins.
69	LDPK	OUT	A	Source-type peak current (DAC2) output pin. Possible to set the range of 0 mA to 150 mA in the accuracy of 8-bit. The output voltage range is 1.0 V to 3.2 V.
70	XLDPK	IN	A	Sink-type peak current output pin. Approximately three fourths of LDRK output current are outputted from this pin.
71	PKGND	PS	A	GND pin of DAC2 in the peak current setting circuit. Must be used in the same potential as other GND pins.
72	PKV_{CC}	PS	A	DAC2 power supply pin in the peak current setting circuit. Consumes approximately a quarter of the setting current. Must be used in the same potential as other power supply pins.
73	PKDCP	MSC	A	Pin to connect a de-coupling capacitor to avoid the output current disturbance, which is caused by a switching noise such as peak current, in peak current setting circuit DAC2. (Connects a capacitor between PKDCP and PKGND.)
74	LDBI	OUT	A	Source-type bias current (DAC3) output pin. Possible to set the range of 0 mA to 150 mA in the accuracy of 8-bit. Output voltage range is 1.0 V to 3.2 V.
75	XLDBI	IN	A	Sink-type peak current output pin. Approximately three fourths of LDBI output current are outputted from this pin.
76	BIGND	PS	A	GND pin of a bias current setting circuit DAC3. Must be used in the same potential as other GND pins.
77	BIV_{CC}	PS	A	Power supply pin of a bias current setting circuit DAC3. Consumes approximately one fourth of a setting current. Must be used in the same potential as other power supply pins.

■ Pin Descriptions (continued)

Pin No.	Symbol	Category		Description
78	BIDCP	MSC	A	Pin to connect a de-coupling capacitor to avoid the output current disturbance, which is caused by a switching noise such as bias current, of a bias current setting circuit DAC3. (Connects a capacitor between BIDCP and BIGND.)
79	SGND	PS	D	Pin connected to the chip substrate.
80	SGND	PS	D	Must be used in the same potential as other GND pins.

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	7.0	V
Input voltage	V_{IN}	− 0.4 to V_{CC} +0.4	V
Outoput voltage	V_{OUT}	− 0.4 to V_{CC} +0.4	V
Parts connecting pin voltage	V_{MSC}	− 0.4 to V_{CC} +0.4	V
Supply current	I_{CC}	80	mA
Pin current	I_{PIN}	−100 to +100	mA
Power dissipation *2	P_D	600	mW
Operating ambient temperature *1	T_{opr}	−20 to +75	°C
Storage temperature *1	T_{stg}	−55 to +150	°C

Note) *1: Except for the operating ambient temperature and storage temperature, all ratings are for T_a = 25°C.
*2: The power dissipation shown is for the IC package in single unit at T_a = 75°C.
Refer to "■ Application Notes, 1. P_D — T_a curves of QFP080-P-1212".

■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Supply voltage	V_{CC}	4.50 to 5.50	V

■ Electrical Characteristics at V_{CC} = 5.0 V, T_a = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply current						
Supply current	I_{CC}	XCLR = low, digital I/O pin = open, I_{PD} = 0 µA	—	20	30	mA
Sleep mode supply current	I_{SLP}	Sleep = 1, I_{PD} = 0 µA	—	3	4	mA
Reference voltage block						
Reference voltage output	V_{REF}		1.20	1.25	1.30	V
Reference voltage variation	ΔV_{REF}	V_{CC} = 4.5 V to 5.5 V, I_{REF} = 0 mA	—	—	± 15	mV
		V_{CC} = 4.5 V to 5.5 V, I_{REF} = −1 mA to + 1 mA	—	—	± 20	
Maximum output current	ΔV_{OM}	I_{REF} = −1.5 mA, difference from I_{REF} = 0 mA	—	—	± 50	mV

■ Electrical Characteristics at V_{CC} = 5.0 V, T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Digital block						
High-level input voltage	V_{IH}	To be applied to a digital input pin	0.8 × V_{CC}	—	—	V
Low-level input voltage	V_{IL}	To be applied to a digital input pin	—	—	0.2 × V_{CC}	V
High-level input voltage (Schmitt-trigger input)	V_{IHSHC}	To be applied to PWMSK, ERFIL pin	0.8 × V_{CC}	—	—	V
Low-level input voltage (Schmitt-trigger input)	V_{ILSHC}	To be applied to PWMSK, ERFIL pin	—	—	0.2 × V_{CC}	V
High-level output voltage	V_{OH}	I_{OH} = –2 mA	0.8 × V_{CC}	—	—	V
Low-level output voltage	V_{OL1}	I_{OL} = +2 mA	—	—	0.2 × V_{CC}	V
	V_{OL2}	I_{OL} = +0.5 mA	—	—	0.4	
Input pull-up, pull-down resistance	R_{PD}	Pull-up: V_{IL} = 0 V Pull-down: V_{IH} = 5.0 V	75	100	125	kΩ
Input leak	I_{LKH}	To be applied to a digital input pin, V_{OH} = 5.25 V	—	—	80	µA
	I_{LKL}	To be applied to a digital input pin, V_{OL} = 0 V	—	—	10	
Entire optical monitor						
Offset voltage at playback	V_{PMOFR}	VR1 = 1 kΩ, I_{PD} = 0 mA	–15	—	15	mV
		VR1 = 1 kΩ, difference from an ideal value at I_{PD} = 100 µA to 200 µA	–40	0	40	
Offset voltage at recording	V_{PMOFW}	VR1 = 1 kΩ, I_{PD} = 0 mA	–15	—	15	mV
		VR1 = 1 kΩ, difference from an ideal value at I_{PD} = 100 µA to 2 000 µA	–20	0	20	
Gain ratio	GR	G_{PMR} /G_{PMW} , output = VNR +0.6 V to 2.0 V	9.0	10.0	11.0	times
Maximum output voltage	$V_{PM\ max}$		V_{CC} × 0.73	V_{CC} × 0.78	—	V
Minimum output voltage	$V_{PM\ min}$		—	—	VNR– 0.015	V
f characteristics at playback	$f_{PMR\ AAF\ OFF}$	AAF-off VR1 = 1 kΩ, –3 dB, I_{PD} = 100 µA to 200 µA	4	6	—	MHz
f characteristics at recording	f_{PMW}	VR1 = 1 kΩ, –3 dB, I_{PD} = 100 µA to 2 000 µA	6	7.5	—	MHz
Settling time at playback	t_{PMSETR}	VR1 = 1 kΩ, error ±0.5%, output variation: Range of 0 V to 2 V	—	200	400	ns
Settling time at recording	t_{PMSETW}	VR1 = 1 kΩ, error ±0.5%, output variation: Range of 0 V to 2 V	—	200	400	ns

■ Electrical Characteristics at V_{CC} = 5.0 V, T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Current amplification changeover						
Gain at playback	G_{IPDR}	Reg7 = "80h", I_{PD} = 40 µA to 240 µA	9.0	10.0	11.0	times
Gain at recording	G_{IPDW}	Reg7 = "C0h", I_{PD} = 200 µA to 3 200 µA	0.9	1.0	1.1	times
Gain ratio	GR_{IPD}	G_{IPDR} /G_{IPDW}	9.0	10.0	11.0	times
I to V conversion block						
Offset voltage	V_{IVOF}	VR1 = 0 Ω, I_{PD} = 0 mA	–15	—	15	mV
DAC1 block						
Resolution	RES1		—	8	—	bit
Integral linearity error	EL1		–1.0	—	10.0	LSB
Differential linearity error	ED1		–1.0	—	1.5	LSB
Maximum output current	I_{1max}	DAC1 = "FFh", DAC8 [Fh], DAC7 [0h], DAC9 [00h]	70	80	90	mA
Offset current	I_{1OF1}	"00h" LPF-on, DAC8 [Fh], DAC7 [0h], DAC9 [00h], DAC7, DAC8 characteristics included	–1	—	1	mA
	I_{1OF2}	"00h" LPF-off, DAC8 [Fh], DAC7 [0h], DAC9 [00h]	–250	—	250	µA
LPF on/off gain ratio	GR_{DAL}	G_{LPFON} /G_{LPFOFF} , input amplitude 0 V to 2 V	0.95	1	1.05	times
Settling time	t_{SDA1}	XWR ↑ to DAC1 [10h to 8Fh], ±2 LSB range, DAC7 [0h], DAC8 [Fh], DAC9 [00h] LPF-off, LPF11 pin open, RDCP2 pin open	—	400	800	ns
DAC7 block						
Resolution	RES7		—	4	—	bit
Integral linearity error	EL7		–1.0	—	1.0	LSB
Differential linearity error	ED7		– 0.5	—	0.5	LSB
Maximum output current	I_{7max}	Set to DAC7 = "Fh", DAC9 [1Fh], DAC1 [00h], DAC8 [0h]	133	150	170	mA
Minimum output current	I_{7min}	Set to DAC7 = "0h", DAC9 [1Fh], DAC1 [00h], DAC8 [0h]	– 0.1	0	0.1	mA
Settling time	t_{SDA7}	XWR ↑ to DAC7 [0h to Fh], DAC9 [1Fh], ±0.5 LSB, DAC1 [00h], DAC8 [0h]	—	50	500	ns
DAC8 block						
Resolution	RES8		—	4	—	bit
Integral linearity error	EL8		–1.0	—	1.0	LSB
Differential linearity error	ED8		– 0.5	—	0.5	LSB

■ Electrical Characteristics at V_{CC} = 5.0 V, T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DAC8 block (continued)						
Maximum output current	I_{8max}	Set to DAC8 = "Fh", DAC1 [FFh], DAC9 [1Fh], DAC7 [0h]	70	80	90	mA
Minimum output current	I_{8min}	Set to DAC8 = "0h", DAC1 [FFh], DAC9 [1Fh], DAC7 [0h]	4	5	6	mA
Settling time	t_{SDA8}	XWR ↑ to DAC8 [0h to Fh], DAC1 [80h], ±0.5 LSB, DAC9 [00h], DAC7 [0h]	—	50	250	ns
DAC2 block						
Resolution	RES2		—	8	—	bit
Integral linearity error	EL2		–1.0	—	5.0	LSB
Differential linearity error	ED2		–1.0	—	1.0	LSB
Maximum output current	I_{2max}	DAC2 = "FFh", DAC4 [Fh]	133	150	170	mA
Offset current	I_{2OF}	DAC2 = "00h", DAC4 [Fh]	– 0.1	—	0.1	mA
Settling time	t_{SDA2}	XWR ↑ to DAC2 [10h to FFh], ±2.0 LSB, DAC4 [Fh]	—	100	250	ns
DAC3 block						
Resolution	RES3		—	8	—	bit
Integral linearity error	EL3		–1.0	—	5.0	LSB
Differential linearity error	ED3		–1.0	—	1.0	LSB
Maximum output current	I_{3max}	DAC3 = "FFh", DAC4 [Fh]	133	150	170	mA
Offset current	I_{3OF}	DAC3 = "00h", DAC4 [Fh]	– 0.1	—	0.1	mA
Settling time	t_{SDA3}	XWR ↑ to DAC3 [10h to FFh], ±2.0 LSB, DAC4 [Fh]	—	200	450	ns
DAC4 block						
Resolution	RES4		—	4	—	bit
Integral linearity error	EL4		–1.0	—	1.0	LSB
Differential linearity error	ED4		–1.0	—	1.0	LSB
Maximum output current	I_{4max}	DAC2 = "FFh", DAC4 [Fh]	133	150	170	mA
Offset current	I_{4OF}	DAC2 = "00h", DAC4 [Fh]	– 0.1	—	0.1	mA
Settling time	t_{SDA4}	XWR ↑ to DAC4 [0h to Fh], ±0.5 LSB, DAC2 [FFh]	—	300	600	ns
DAC9 block						
Resolution	RES9		—	5	—	bit
Integral linearity error	EL9		–1.0	—	1.0	LSB
Differential linearity error	ED9		–1.0	—	1.0	LSB
Maximum output current	I_{9max}	DAC9 = "1Fh", DAC7 [Fh], DAC1 [00h], DAC8 [0h]	133	150	170	mA

■ Electrical Characteristics at V_{CC} = 5.0 V, T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DAC9 block (continued)						
Offset current	I_{9OF1}	"00h" LPF-on, DAC7 [Fh], DAC8 [0h], DAC1 [00h], DAC7, DAC8 characteristics included	–2.0	—	2.0	mA
	I_{9OF2}	"00h" LPF-off, DAC7 [Fh], DAC8 [0h], DAC9 [00h], DAC7, DAC8 characteristics included	– 0.85	—	0.85	
LPF on/off gain ratio	GR_{DA9}	G_{LPFON} /G_{LPFOFF} , input amplitude 0 V to 2 V	0.95	1	1.05	times
Settling time	t_{SDA9}	XWR ↑ to DAC9 [00h to 1Fh] ±2 LSB range, DAC7[Fh], DAC8 [0h], LPF9-off, LPF91 pin open, RDCP1 pin open	—	400	800	ns
Supply voltage monitoring block						
Abnormality release supply voltage	V_{PSDL}	Sweep V_{CC} from low to high	3.9	4.2	4.5	V
	V_{PSOL}	Sweep V_{CC} from high to low	5.5	5.8	6.1	
Abnormality supply voltage	V_{PSDH}	Sweep V_{CC} from high to low	3.6	3.9	4.2	V
	V_{PSOH}	Sweep V_{CC} from low to high	5.8	6.1	6.4	
Abnormally emitted light detection DAC5						
Resolution	RES5		—	4	—	bit
Integral linearity error	EL5		– 0.5	—	0.5	LSB
Differential linearity error	ED5		– 0.5	—	0.5	LSB
Offset voltage	V_{5OF1}	DAC5 = set to "Fh" and difference to ERREF pin	–20	—	20	mV
	V_{5OF2}	DAC5 = set to "0h" and difference to VNR pin, at ERREF – VNR = 2.0 V	105	125	145	
Settling time	t_{SDA5}	XWR ↑ to DAC5 [0h to Fh], ±0.5 LSB	—	0.5	1.5	µs
Abnormally emitted light detection DAC6						
Resolution	RES6		—	4	—	bit
Integral linearity error	EL6		– 0.5	—	0.5	LSB
Differential linearity error	ED6		– 0.5	—	0.5	LSB
Offset voltage	V_{6OF1}	DAC6 = set to "Fh" and difference to ERREF pin	–20	—	20	mV
	V_{6OF2}	DAC6 = set to "0h" and difference to VNR pin, at ERREF – VNR = 2.0 V	105	125	145	
Settling time	t_{SDA6}	XWR ↑ to DAC6 [0h to Fh] ±0.5 LSB	—	0.5	1.5	µs

■ Electrical Characteristics at V_{CC} = 5.0 V, T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Abnormally emitted light detection optical monitor block						
Offset voltage	V_{EROFR}	In playback, DETMONI pin, I_{PD} = 0 µA	–40	—	60	mV
	V_{EROFW}	In recording, DETMONI pin, I_{PD} = 0 µA	–50	—	50	
Gain	G_{ERR1}	In playback, addr. "9": D4 = "0", I_{PD} = 100 µA to 200 µA	9.0	10.0	11.0	times
	G_{ERR2}	In playback, addr. "9": D4 = "1", I_{PD} = 100 µA to 200 µA	4.5	5.0	5.5	
	G_{ERW}	In recording, DETMONI pin, I_{PD} = 100 µA to 2 000 µA	0.9	1.0	1.1	
Gain ratio	$\frac{G_{ERR1}}{G_{ERW}}$		9.0	10.0	11.0	times
	$\frac{G_{ERR2}}{G_{ERW}}$		4.5	5.0	5.5	
f characteristics at playback	f_{ERR}	VR1 = 1 kΩ, –3 dB, I_{PD} = 100 µA to 200 µA	2.5	—	—	MHz
f characteristics at recording	f_{ERW}	VR1 = 1 kΩ, –3 dB, I_{PD} = 100 µA to 2 000 µA	5.0	—	—	MHz
Control operation response						
Data write to XLDERR ↓	t_{203}	XWR ↑ to XLDERR ↓	—	20	60	ns
Data write to XLDERR ↑	t_{204}	XWR ↑ to XLDERR ↑	—	25	60	ns
Data write to sleep mode	t_{205}	XWR ↑ to sleep mode	—	4	9	µs
Data write to normal mode	t_{206}	XWR ↑ to normal mode	—	3	8	µs
RPHOLD ↑ to DAC5 R → W	t_{39}	RPHOLD ↑ to DAC5 W, at having reached ±0.5 LSB	—	0.40	2.5	µs
RPHOLD ↓ to DAC5 W → R	t_{40}	RPHOLD ↓ to DAC5 R, at having reached ±0.5 LSB	—	0.40	2.5	µs
RPHOLD ↑ to DAC6 R → W	t_{41}	RPHOLD ↑ to DAC6 W, at having reached ±0.5 LSB	—	0.40	2.5	µs
RPHOLD ↓ to DAC6 W → R	t_{42}	RPHOLD ↓ to DAC6 R, at having reached ±0.5 LSB	—	0.40	2.5	µs
RPHOLD ↑ to HF module signal	t_{43}	RPHOLD ↑ to XHFON ↑	—	18	30	ns
RPHOLD ↓ to HF module signal	t_{44}	RPHOLD ↓ to XHFON ↓	—	17	30	ns

■ Electrical Characteristics at V_{CC} = 5.0 V, T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Recording Modulation						
Peak modulation signal response *1	t_{113}	PKMD ↑ to LDPK ↑ 50% delay	—	18	30	ns
	t_{114}	PKMD ↓ to LDPK ↓ 50% delay	—	17	30	
	t_{115}	LDPK ↑ 50% to LDPK ↓ 50%	t_{112} −3	t_{112} −1	t_{112} +1	
	t_{116}	LDPK ↑ 10% to LDPK ↑ 90%	—	6	9	
	t_{117}	LDPK ↓ 90% to LDPK ↓ 10%	—	4	6	
Bias modulation signal response *1	t_{123}	BIMD ↑ to LDBI ↑ 50% delay	—	18	30	ns
	t_{124}	BIMD ↓ to LDBI ↓ 50% delay	—	17	30	
	t_{125}	LDBI ↑ 50% to LDBI ↓ 50%	t_{122} −3	t_{122} −1	t_{122} +1	
	t_{126}	LDBI ↑ 10% to LDBI ↑ 90%	—	6	9	
	t_{127}	LDBI ↓ 90% to LDBI ↓ 10%	—	5	8	

Note) ∗1: Resistive load (at 15 Ω)
Conditions of t_{113} to t_{117}
Measure at approximately 1.75 V of LDPK pin voltage.
DAC1 [FFh], DAC8 [7h]
DAC9 [1Fh], DAC7 [7h], DAC4 [Fh]
DAC2 [00h to 80f]
Conditions of t_{123} to t_{127}
Measure at approximately 1.75 V of LDPK pin voltage.
DAC1 [FFh], DAC8 [7h]
DAC9 [1Fh], DAC7 [7h], DAC4 [Fh]
DAC3 [00h to 80f]

• Design reference data

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reference voltage block						
Reference voltage temperature characteristics *2	ΔV_{TEM}	V_{REF} = 0 V, T_a = −20°C to +75°C	—	—	±30	mV
Digital block						
Low → high input hysteresis (Schmidt trigger input)	V_{LHHYS}	To be applied to PWMSK, ERFIL pin	—	1.0	—	V
High → low input hysteresis (Schmidt trigger input)	V_{HLHYS}	To be applied to PWMSK, ERFIL pin	—	1.0	—	V
Entire optical monitor						
Offset voltage temperature variation	$\frac{\Delta V_{PMOFR}}{\Delta T}$	In playback, VR1 = 1 kΩ I_{PD} = 10 µA to 200 µA T_a = −20°C to +75°C	—	55	200	$\frac{\mu V}{°C}$
	$\frac{\Delta V_{PMOFW}}{\Delta T}$	In recording, VR1 = 1 kΩ I_{PD} = 100 µA to 2 000 µA T_a = −20°C to +75°C	—	30	150	

Note) ∗2: Difference between V_{REF} min. and V_{REF} max. within the range of T_a = −20°C to +75°C.

■ Electrical Characteristics at V_{CC} = 5.0 V, T_a = 25°C (continued)

• Design reference data (continued)

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Entire optical monitor (continued)						
Gain ratio variation to temperature	$d\frac{G_{PMR}}{G_{PMW}}$	T_a = –20°C to +75°C	–3	—	3	%
Slew rate	$S1_{PMR}$	In playback, AAF-off rise	13	18	—	V/µs
	$S1_{PMW}$	In recording, rise	35	45	—	
Signal changeover response	t_{PMSW1}	× 10 → × 1, at having reached ±0.5%	—	100	300	ns
	t_{PMSW2}	× 1 → × 10, at having reached ±0.5%	—	200	500	
f characteristics	f_{PMROF}	In playback, –3 dB, VR1 = 1 kΩ, AAF filter on, I_{PD} 100 µA to 200 µA	—	40.8	—	kHz
Current amplification block						
Gain variation to temperature	dG_{IPDR}	In playback, I_{PD} = 60 µA to 240 µA, T_a = –20°C to +75°C	–3	—	3	%
	dG_{IPDW}	In recording, I_{PD} = 0.2 mA to 3.2 mA, T_a = –20°C to +75°C	–3	—	3	
Gain ratio variation to temperature	$d\frac{G_{IPDR}}{G_{PMW}}$	In playback, I_{PD} = 60 µA to 240 µA, In recording, I_{PD} = 0.2 mA to 3.2 mA, T_a = –20°C to +75°C	–3	—	3	%
Signal changeover response	t_{IPDSW1}	× 10 → × 1, at having reached ±0.5%	—	100	300	ns
	t_{IPDSW2}	× 1 → × 10, at having reached ±0.5%	—	200	500	
I to V conversion						
Offset voltage variation to temperature	$\frac{dV_{IVOF}}{dT}$	VR1 = 0 Ω, I_{PD} = 0 µA, T_a = –20°C to +75°C	—	10	50	$\frac{\mu V}{°C}$
Slew rate	Sl_{IV}		20	34	—	V/µs
Open loop gain	G_{IV}		—	50	—	dB
Zero-cross frequency	f_{0IV}	Output amplitude at 1 V[p-p]	—	8	—	MHz
Settling time	t_{IVSET}	Error ±0.5%, output variation: within the range of 0 V to 2 V	—	100	200	ns
AAF analog SW						
On resistance at playback	R_{AFR}	0 Ω between I_{VOUT} and I_{VIN}	—	175	250	Ω
On resistance at recording	R_{AFW}		—	200	300	Ω
DAC1						
f characteristics	f_{DAC1}	Sine wave signal equivalent to 40 mA[p-p] of current amplitude at LPF12 pin, DAC7 [0h], DAC8 [Fh], DAC9 [00h], RDCP2 pin = 1 000 pF	—	1	—	MHz

■ Electrical Characteristics at V_{CC} = 5.0 V, T_a = 25°C (continued)

• Design reference data (continued)

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DAC1 (continued)						
Driving current temperature characteristics	Err_{DA1}	Including DAC8 when setting at "FFh", DAC7 [0h], DAC8 [Fh], T_a = 0°C to +75°C	—	7	10	%
Offset current variation to temperature	$\frac{dI_{1ON}}{dT}$	"00h", LPF-on, including DAC7, DAC8, DAC7 [0h], DAC8 [Fh], T_a = −25°C to +75°C	—	2	10	$\frac{\mu A}{°C}$
	$\frac{dI_{1OF}}{dT}$	"00h", LPF-off, including DAC7, DAC8, DAC7 [0h], DAC8 [Fh], T_a = −25°C to +75°C	—	0.5	10	
DAC9						
f characteristics	f_{DAC9}	Sine wave signal equivalent to 40 mA[p-p] of current amplitude at LPF22 pin, DAC7 [Fh], DAC8 [0h], DAC1 [00h], RDCP1 pin = 1 000 pF	—	1	—	MHz
Driving current temperature characteristics	Err_{DA9}	Including DAC8 at setting at "1Fh", DAC7 [Fh], DAC8 [0h], T_a = 0°C ~ +75°C	—	7	10	%
Offset current variation to temperature	$\frac{dI_{9ON}}{dT}$	"00h", LPF-on, including DAC7, DAC8, DAC7 [Fh], DAC8 [0h], T_a = −25°C ~ +75°C	—	2	10	$\frac{\mu A}{°C}$
	$\frac{dI_{9OF}}{dT}$	"00h", LPF-off, including DAC7, DAC8, DAC7 [Fh], DAC8 [0h], T_a = −25°C to +75°C	—	0.5	10	
DAC7						
Driving current temperature characteristics	Err_{DA7}	DAC7 [Fh], DAC8 [0h], DAC9 [1Fh], DAC1 [00h], T_a = −20°C to +75°C	0	8	15	%
Offset current temperature characteristics	$\frac{dI_{DA7OF}}{dT}$	DAC7 [0h], DAC8 [0h], DAC9 [1Fh], DAC1 [00h], T_a = −20°C to +75°C	—	0.2	10	$\frac{\mu A}{°C}$
DAC8						
Driving current temperature characteristics	Err_{DA8}	DAC8 [Fh], DAC7 [0h], DAC1 [FFh], DAC9 [00h], T_a = −20°C to +75°C	0	8	15	%
Offset current temperature characteristics	$\frac{dI_{DA8OF}}{dT}$	DAC8 [0h], DAC7 [0h], DAC1 [FFh], DAC9 [00h], T_a = −20°C to +75°C	—	0.2	10	$\frac{\mu A}{°C}$

■ Electrical Characteristics at V_{CC} = 5.0 V, T_a = 25°C (continued)

• Design reference data (continued)

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DAC2						
Offset current temperature characteristics	$\frac{dI_{DA2OF}}{dT}$		—	—	10	$\frac{\mu A}{°C}$
Driving current temperature characteristics	Err_{DA2}	DAC3 = "FFh", set to DAC4 = "Fh", T_a = –20°C to +75°C	—	6	10	%
Settling time	t_{SDA2A}	XWR ↑ to DAC2 [Δ4: 10 h to 14h], ±0.5 LSB DAC4 [Fh]	—	40	100	ns
	t_{SDA2B}	XWR ↑ to DAC2 [Δ7F: 10 h to 8 Fh], ±1.0 LSB DAC4 [Fh]	—	80	200	
DAC3						
Offset current temperature characteristics	$\frac{dI_{DA3OF}}{dT}$		—	—	10	$\frac{\mu A}{°C}$
Driving current temperature characteristics	Err_{DA3}	DAC3 = "FFh", set to DAC4 = "Fh", T_a = –20°C to +75°C	—	6	10	%
Settling time	t_{SDA3A}	XWR ↑ to DAC3 [Δ4: 10 h to 14h], ±0.5 LSB DAC4 [Fh]	—	40	100	ns
	t_{SDA3B}	XWR ↑ to DAC3 [Δ7F: 10 h to 8Fh], ±1.0 LSB DAC4 [Fh]	—	80	200	
DAC4						
Offset current temperature characteristics	$\frac{dI_{DA4OF}}{dT}$		—	—	10	$\frac{\mu A}{°C}$
Driving current temperature characteristics	Err_{DA4}	DAC4 = "Fh", set to DAC2 = "FFh", T_a = –20°C to +75°C	—	6	10	%
Supply voltage monitoring block						
Abnormal supply voltage detection hysteresis	V_{PSDHYS}	Voltage difference between abnormality detection and release of supply voltage drop, $V_{PSD1} - V_{PSDH}$	—	300	—	mV
	V_{PSOHYS}	Voltage difference between abnormality detection and release of supply voltage drop, $V_{PSOH} - V_{PSOL}$	—	300	—	
Comparator in abnormally emitted light detection block						
Input offset voltage	V_{PDCOF}	Insufficiently emitted light detection	–5	—	5	mV
	V_{POCOF}	Excessively emitted light detection	–5	—	5	

■ Electrical Characteristics at V_{CC} = 5.0 V, T_a = 25°C (continued)

• Design reference data (continued)

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Comparator in abnormally emitted light detection block (continued)						
Input offset voltage variation to temperature	$\frac{dV_{PDCOF}}{dT}$	Insufficiently emitted light detection	—	—	20	$\frac{\mu V}{°C}$
	$\frac{dV_{POCOF}}{dT}$	Excessively emitted light detection	—	—	20	
Abnormally emitted light detection response	t_{PWDNF}	Insufficiently emitted light detection	—	150	300	ns
	t_{PWOVF}	Excessively emitted light detection	—	150	300	
Abnormally emitted light release response	t_{PWDR}	Insufficiently emitted light detection	—	150	300	ns
	t_{PWOVF}	Excessively emitted light detection	—	150	300	
DAC5 block						
Offset voltage variation to temperature	$\frac{dV_{DA5OF}}{dT}$	Set to "Fh"	—	−10	80	$\frac{\mu V}{°C}$
DAC6 block						
Offset voltage variation to temperature	$\frac{dV_{DA5OF}}{dT}$	Set to "Fh"	—	−10	80	$\frac{\mu V}{°C}$
Optical monitor for abnormally emitted light detection						
Offset voltage variation to temperature	$\frac{dV_{EROFR}}{dT}$	In playback, I_{PD} = 0 µA	—	−20	210	$\frac{\mu V}{°C}$
	$\frac{dV_{EROFW}}{dT}$	In recording, I_{PD} = 0 µA	—	−20	200	
Gain variation to temperature	dG_{ERR1}	In playback, I_{PD} = 100 µA to 200 µA, T_a = −20°C to +75°C	−3	0.5	3	%
	dG_{ERR2}	In playback, I_{PD} = 100 µA to 200 µA, T_a = −20°C to +75°C	−3	0.5	3	
	dG_{ERW}	In recording, I_{PD} = 100 µA to 2 000 µA, T_a = −20°C to +75°C	−3	0.5	3	
Gain ratio variation to temperature	$d\frac{G_{ERR}}{G_{ERW}}$	T_a = −20°C to +75°C	−3	0.5	3	%
Settling time	t_{ERR}	In playback, error: ±0.5%, current variation 100 µA to 200 µA	—	250	400	ns
	t_{ERW}	In playback, error: ±0.5%, current variation 100 µA to 2 000 µA	—	100	200	
Signal changeover response (× 10 mode)	t_{ERSW1A}	Playback → recording ±0.5% addr "9": D4 = "0" × 10	—	170	400	ns
	t_{ERSW2A}	Recording → playback ±0.5% addr "9": D4 = "0" × 10	—	550	1 000	

■ Electrical Characteristics at V_{CC} = 5.0 V, T_a = 25°C (continued)

• Design reference data (continued)

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Optical monitor for abnormally emitted light detection (continued)						
Signal changeover response × 5 mode	t_{ERSW1B}	Playback → recording ±0.5%, addr "9": D4 = "1" × 5	—	200	400	ns
	t_{ERSW2B}	Recording → playback ±0.5%, addr "9": D4 = "1" × 5	—	250	500	
Control operation response	Register setting → output					
Data writing to LPF-off	t_{87}	XWR ↑ to LPF "off"	—	0.8	2.0	µs
Data writing to LPF-on	t_{88}	XWR ↑ to LPF "on"	—	250	600	ns
Data writing to AAF-off	t_{85}	XWR ↑ to AAF "off"	—	60	200	ns
Data writing to AAF-on	t_{86}	XWR ↑ to AAF "on"	—	20	200	ns
Data writing to DAC6 changeover *3	t_{207}	XWR ↑ to DAC6 ±0.5%	—	0.9	2.5	µs
Data writing to DAC5 changeover *3	t_{208}	XWR ↑ to DAC5 ±0.5%	—	0.9	2.5	µs
Data writing to shunt on *4	t_{89}	XWR ↑ to shunt circuit "on", LDERR register "1"	—	—	430	ns
Data writing to shunt off *4	t_{90}	XWR ↑ to shunt circuit "off", LDERR register "0"	—	—	230	ns
Control operation response	Input → output					
RPHOLD ↑ to PWRMONI changeover	t_{37}	RPHOLD ↑ to × 1, at having reached ±0.5%	—	0.4	0.9	µs
RPHOLD ↓ to PWRMONI changeover	t_{38}	RPHOLD ↓ to × 10, AAF, at having reached ±0.5%	—	0.4	0.9	µs
RPHOLD ↑ to mask signal *5	t_{45}	RPHOLD ↑ to mask signal ↓	—	15	30	ns
Mask signal width at RPHOLD ↑ *5	t_{46}	Mask signal ↓ to mask signal ↑ at RPHOLD high	—	1	1.1	µs
RPHOLD ↓ to mask signal *5	t_{47}	RPHOLD ↓ to mask signal ↓	—	15	30	ns
Mask signal width at RPHOLD ↑ *5	t_{48}	Mask signal ↓ to mask signal ↑ at RPHOLD low	—	1	1.1	µs
RPHOLD ↓ to AAFRST signal ↑ *5	t_{211}	RPHOLD ↓ to AAFRST ↑	—	15	30	ns
AAFRST signal width *5	t_{212}	AAFRST ↑ to AAFRST ↓	—	2	2.2	µs
Shunt circuit "on" *6	t_{49}	XCLR ↓ to shunt circuit "on"	—	—	430	ns
Shunt circuit "off" *6	t_{50}	XCLR ↑ to shunt circuit "off"	—	—	230	ns

Note) ∗3: Measure at DACMONI pin.

∗4: Measuring is impossible outside the IC.

∗5: Measuring is impossible outside the IC.
The values of t_{46}, t_{48} and t_{212} are determined by the built-in resistor Rin1 (10 kΩ, allowance: 10%) and the external C1.

∗6: Measuring is impossible outside the IC. The built-in resistor Rin2 (10 kΩ, allowance: 10%) and the external C2.

■ Electrical Characteristics at V_{CC} = 5.0 V, T_a = 25°C (continued)

• Design reference data (continued)

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Control operation response	Input → output (continued)					
AAF reset "reset" *6	t_{213}	AAFRST ↑ to AAF "reset"	—	—	200	ns
AAF reset "normal" *6	t_{214}	AAFRST ↓ to AAF "normal"	—	—	200	ns
Mask signal (wrt. ERFIL) *7	t_{215}	ERFIL ↑ to XLDERR1 ↓	—	1.2	2.0	µs
	t_{216}	ERFIL ↓ to XLDERR1 ↑	—	15	—	ns
Register → output						
Mode changeover	t_{55}	XWR ↑ to AAFRST test mode	—	25	60	ns
AAFRST	t_{56}	XWR ↑ to AAFRST normal mode	—	200	400	
Mode changeover	t_{57}	XWR ↑ to SW6 test mode	—	90	200	ns
SW6	t_{58}	XWR ↑ to SW6 normal mode	—	60	150	
Mode changeover	t_{59}	XWR ↑ to XHFON test mode	—	20	60	ns
XFHON	t_{60}	XWR ↑ to XHFON normal mode	—	25	70	
Mode changeover	t_{61}	XWR ↑ to SW2 test mode	—	30	80	ns
SW2	t_{62}	XWR ↑ to SW2 normal mode	—	20	50	
Mode changeover	t_{63}	XWR ↑ to SW3 test mode	—	30	70	ns
SW3	t_{64}	XWR ↑ to SW3 normal mode	—	20	50	
Mode changeover	t_{67}	XWR ↑ to SW1 test mode	—	20	50	ns
SW1	t_{68}	XWR ↑ to SW1 normal mode	—	35	100	
Mode changeover	t_{69}	XWR ↑ to LEVSW test mode	—	0.55	2.0	µs
LEVSW	t_{70}	XWR ↑ to LEVSW normal mode	—	0.35	1.0	
Test mode operation	t_{75}	XWR ↑ to AAF filter reset	—	25	100	ns
AAF filter *8	t_{76}	XWR ↑ to AAF filter normal	—	200	400	
Test mode operation	t_{77}	XWR ↑ to × 1, when reaching ±0.5%	—	0.4	0.9	µs
Current amplification changeover	t_{78}	XWR ↑ to × 10, when reaching AAF ±0.5%	—	0.4	0.9	
Test mode operation	t_{79}	XWR ↑ to XHFON ↑	—	20	60	ns
XHFON	t_{80}	XWR ↑ to XHFON ↓	—	25	70	
Test mode operation	t_{81}	XWR ↑ to SW2 "on" DAC2 ±2.0 LSB	—	90	200	ns
SW2 *9	t_{81A}	XWR ↑ to SW2 "on" DAC2 × 50%	—	30	80	
	t_{82}	XWR ↑ to SW2 "off" 0 mA ±2.0 LSB	—	50	150	
	t_{82A}	XWR ↑ to SW2 "on" DAC2 × 50%	—	20	60	

Note) *6: Measuring is impossible outside the IC. The built-in resistor Rin2 (10 kΩ, allowance: 10%) and the external C2.

*7: Measuring is impossible outside the IC.

*8: No external fitting until on/off of switch.

*9: Set the data to "7Fh".

■ Electrical Characteristics at V_{CC} = 5.0 V, T_a = 25°C (continued)

• Design reference data (continued)

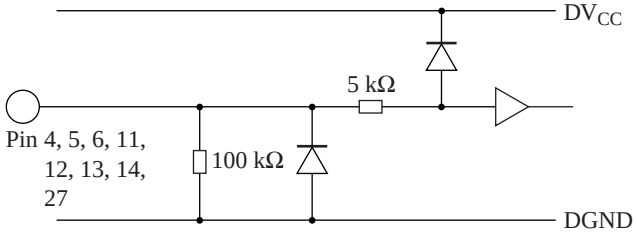
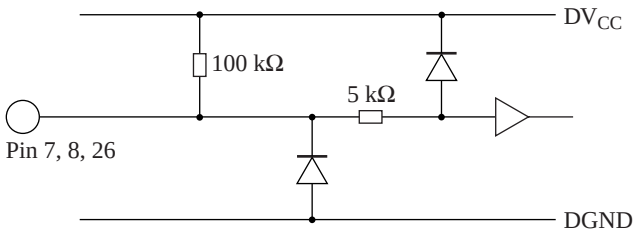
Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Register → output (continued)						
Test mode operation SW3 *9	t_{83}	XWR ↑ to SW3 "on" DAC3 ±2.0 LSB	—	330	600	ns
	t_{83A}	XWR ↑ to SW3 "on" DAC3 × 50%	—	30	80	
	t_{84}	XWR ↑ to SW3 "off" 0 mA ±2.0 LSB	—	50	150	
	t_{84A}	XWR ↑ to SW3 "on" DAC3 × 50%	—	20	60	
Test mode operation SW1 *10	t_{91}	XWR ↑ to SW1 "off"	—	20	100	ns
	t_{92}	XWR ↑ to SW1 "on"	—	35	150	
Test mode operation DAC5	t_{93}	XWR ↑ to DAC5 W, at having reached ±0.5 LSB	—	1.0	2.5	µs
	t_{94}	XWR ↑ to DAC5 R, at having reached ±0.5 LSB	—	0.7	2.5	
Test mode operation DAC6	t_{95}	XWR ↑ to DAC6 W, at having reached ±0.5 LSB	—	1.0	2.5	µs
	t_{96}	XWR ↑ to DAC6 R, at having reached ±0.5 LSB	—	0.7	2.5	

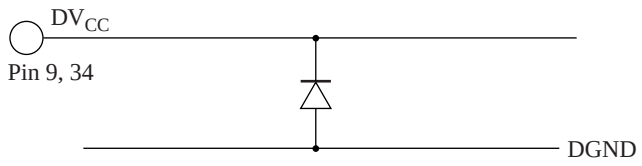
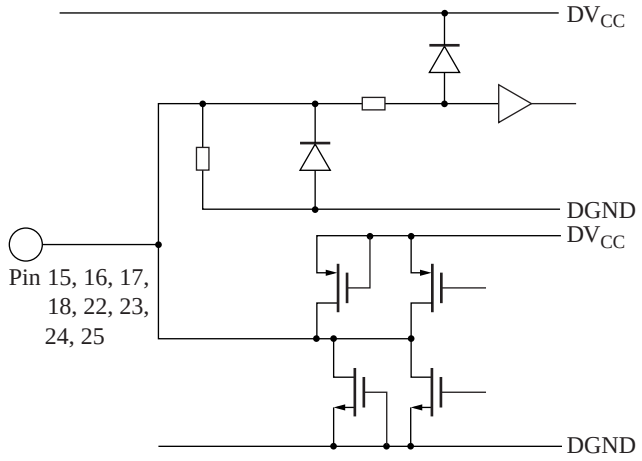
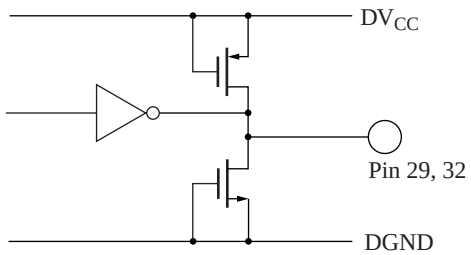
Note) *9 : Data sets up "7Fh".

*10: DAC1 = 7 Fh, DAC9 = 00 h, DAC7 = 0h, DAC8 = Fh

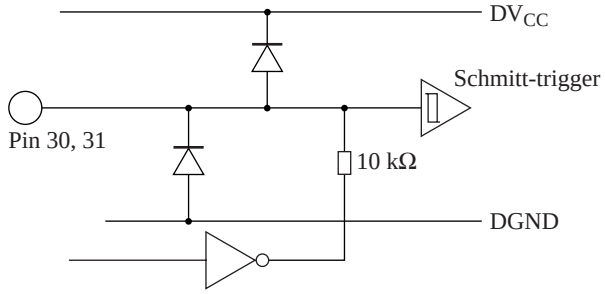
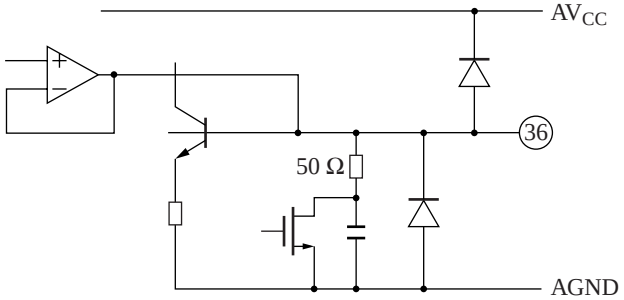
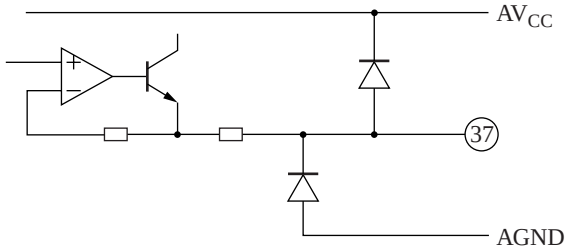
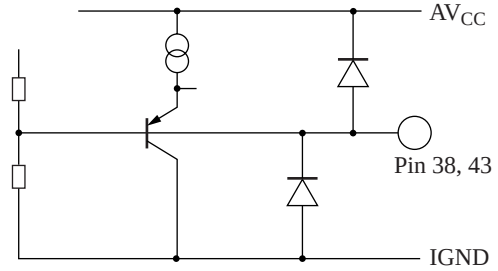
■ Terminal Equivalent Circuits

Pin No.	Symbol	Equivalent circuit
1 2 3	Pin 1: SGND Pin 2: DGND Pin 3: DGND	—
4 5 6	Pin 4: PKMD Pin 5: BIMD Pin 6: RPHOLD	
7 8	Pin 7: XWR Pin 8: XRD	

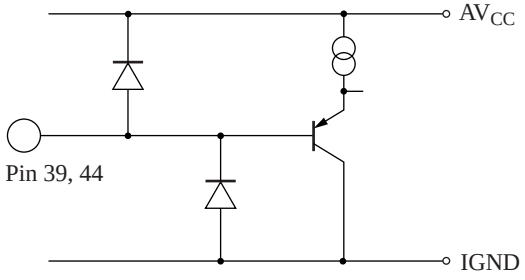
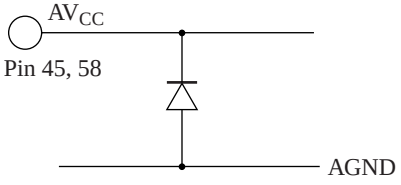
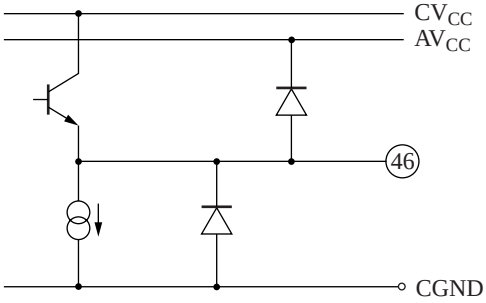
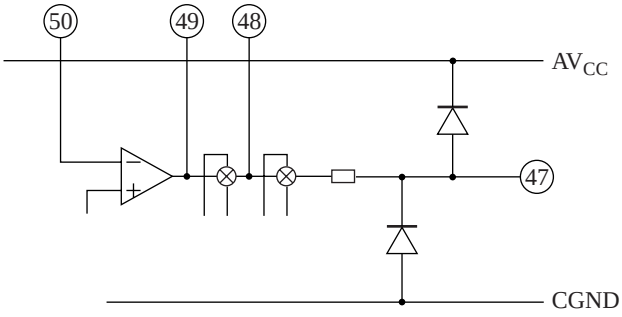
■ Terminal Equivalent Circuits (continued)

Pin No.	Symbol	Equivalent circuit
9	DV_{CC}	
10	DGND	—
11 12 13 14	Pin 11: AD0 Pin 12: AD1 Pin 13: AD2 Pin 14: AD3	Refer to pin 4
15 16 17 18	Pin 15: DT0 Pin 16: DT1 Pin 17: DT2 Pin 18: DT3	
19 20 21	Pin 19: DGND Pin 20: SGND Pin 21: SGND	—
22 23 24 25	Pin 22: DT4 Pin 23: DT5 Pin 24: DT6 Pin 25: DT7	Refer to pin 15
26	XLDEN	Refer to pin 7
27	XCLR	Refer to pin 4
28	DGND	—
29	XLDERR	

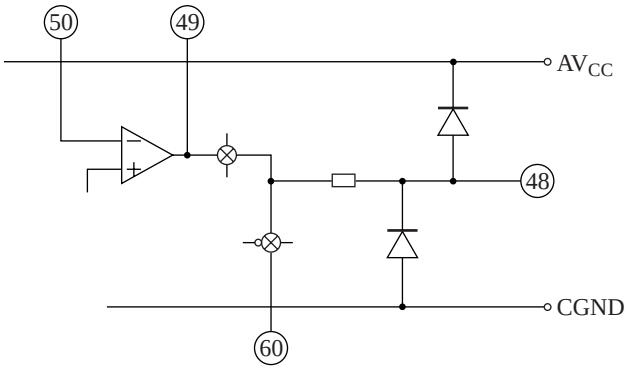
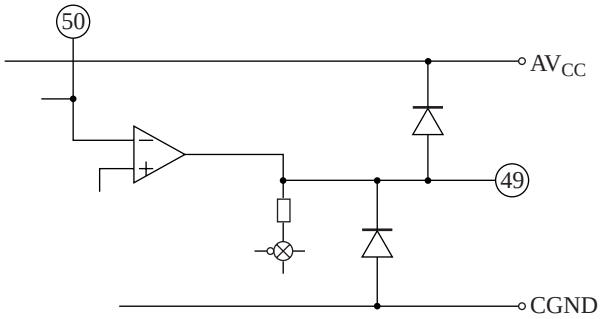
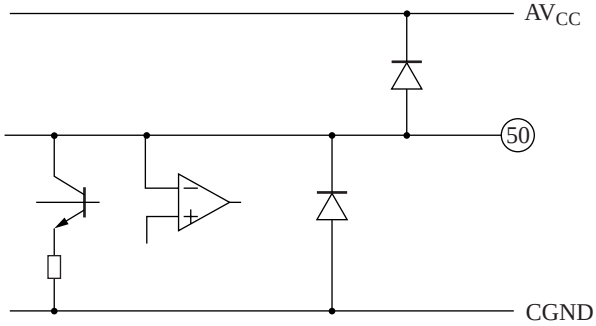
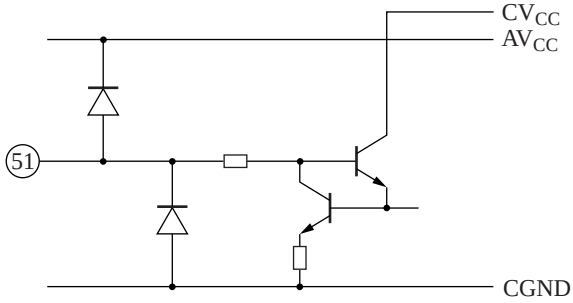
■ Terminal Equivalent Circuits (continued)

Pin No.	Symbol	Equivalent circuit
30 31	Pin 30: PWMSK Pin 31: ERFIL	
32	XHFON	Refer to pin 29
33	DGND	—
34	DV_{CC}	Refer to pin 9
35	AGND	—
36	VC	
37	RREF	
38	LPF11	

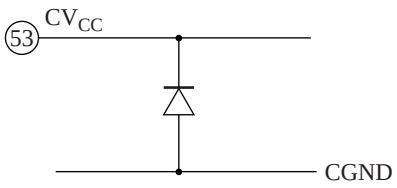
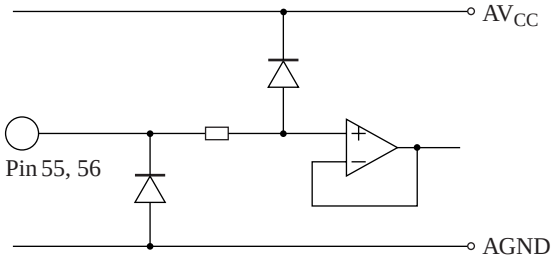
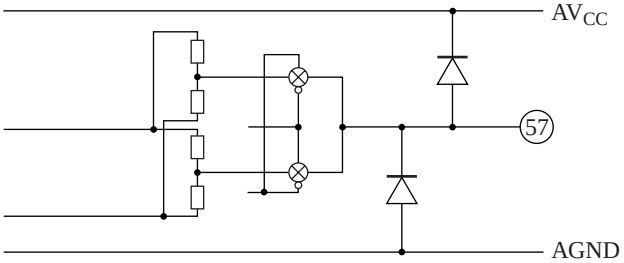
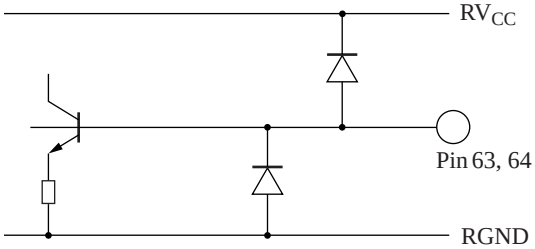
■ Terminal Equivalent Circuits (continued)

Pin No.	Symbol	Equivalent circuit
39	LPF12	
40 41 42	Pim 40 : IGND Pim 41 : SGND Pim 42 : SGND	—
43	LPF91	Refer to pin 38
44	LPF92	Refer to pin 39
45	AV_{CC}	
46	DETMONI	
47	PWRMONI	

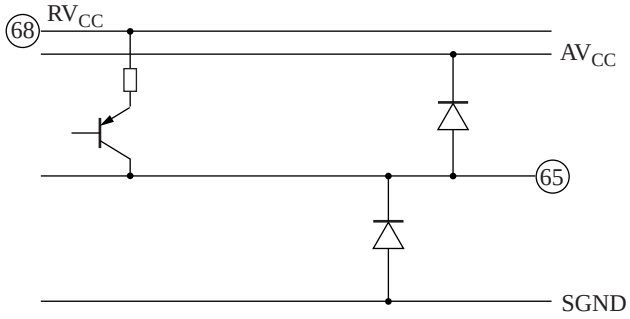
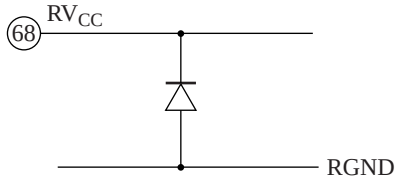
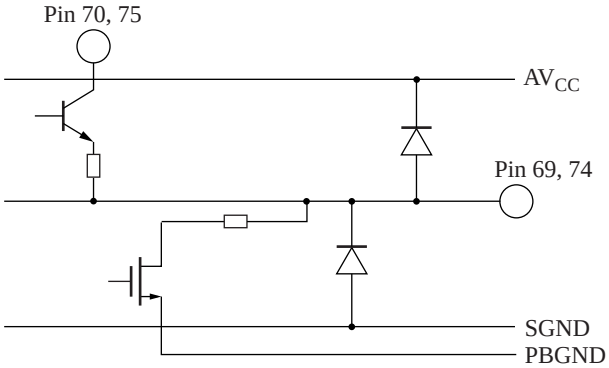
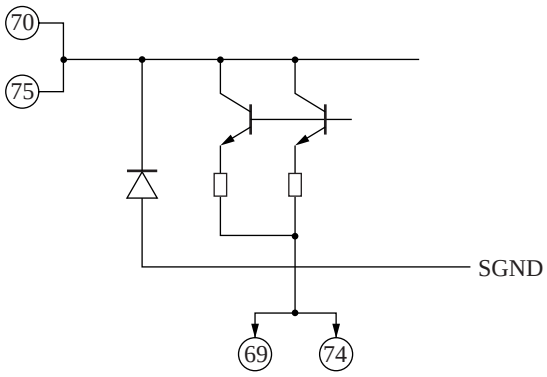
■ Terminal Equivalent Circuits (continued)

Pin No.	Symbol	Equivalent circuit
48	AAF	
49	IVOUT	
50	IVIN	
51	IPD	
52	CGND	—

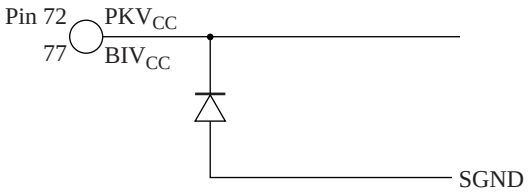
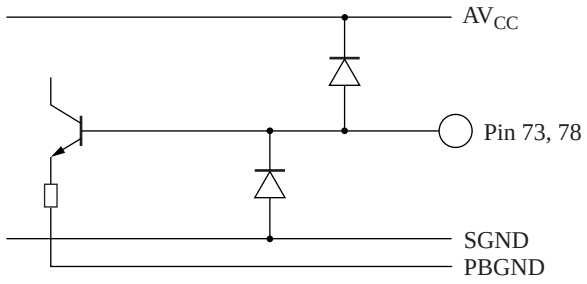
■ Terminal Equivalent Circuits (continued)

Pin No.	Symbol	Equivalent circuit
53	CV_{CC}	
54	AGND	—
55 56	Pim 55 : ERREF Pim 56 : VNR	
57	DACMONI	
58	AV_{CC}	Refer to pin 45
59 60 61 62	Pim 59 : SGND Pim 60 : SGND Pim 61 : SGND Pim 62 : RGND	—
63 64	Pim 63 : RDCP1 Pim 64 : RDCP2	

■ Terminal Equivalent Circuits (continued)

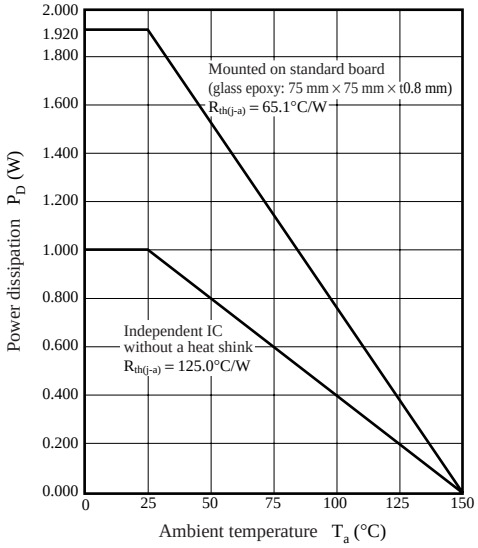
Pin No.	Symbol	Equivalent circuit
65	LDRP	
66	N.C.	—
67	N.C.	—
68	RV_{CC}	
69	LDPK	
70	XLDPK	

■ Terminal Equivalent Circuits (continued)

Pin No.	Symbol	Equivalent circuit
71	PKGND	—
72	PKV_{CC}	
73	PKDCP	
74	LDBI	Refer to pin 69
75	XLDBI	Refer to pin 70
76	BIGND	—
77	BIV_{CC}	Refer to pin 72
78	BIDCP	Refer to pin 73
79	SGND	—
80	SGND	—

■ Application Notes

1. P_D — T_a curves of QFP080-P-1212

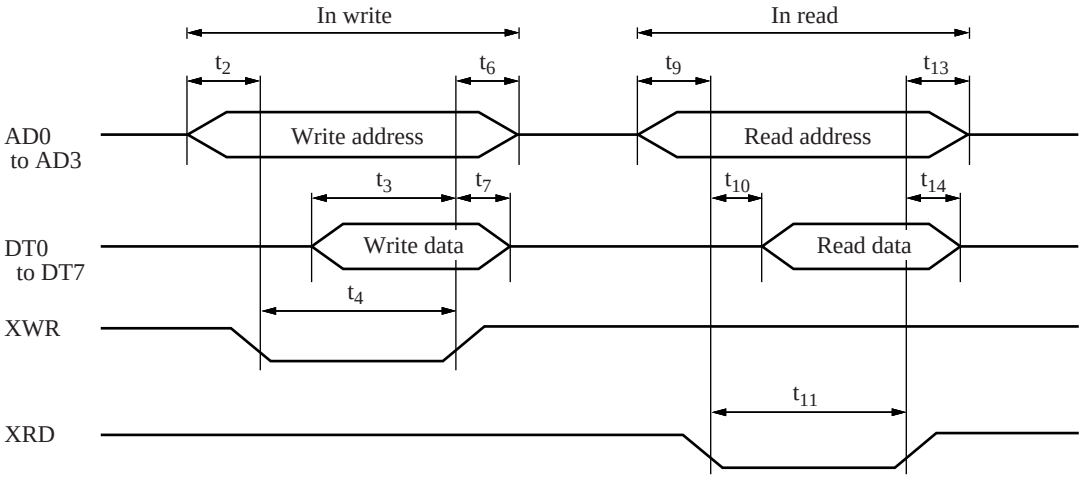


■ Application Notes (continued)

2. Timing chart

1) Definition of rising and falling

2) Interface



Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Switching characteristics	t_{LH}	10% to 90%	—	—	10	ns
	t_{HL}	90% to 10%	—	—	10	
Pulse width	t_4	XWR ↓ to XWR ↑	50	—	—	ns
	t_{11}	XRD ↓ to XRD ↑	70	—	—	
Setup time	t_2	AD defined to XWR ↓	10	—	—	ns
	t_3	DT defined to XWR ↑	35	—	—	
	t_9	AD defined to XRD ↓	10	—	—	
	t_{10}	XRD ↓ to DT defined	—	—	50	
Hold time	t_6	XWR ↑ to AD released	0	—	—	ns
	t_7	XWR ↑ to DT released	0	—	—	
	t_{13}	XRD ↑ to AD released	0	—	—	
	t_{14}	XRD ↑ to DT released	0	—	30	

■ Application Notes (continued)

3. I/O specifications

- Parallel interface

1) I/O level is CMOS.

2) Transfers a digital signal to DAC and each mode setting register with 4 addresses, 8 data and 2 control signals.

Address signal	AD0 to AD3
Data signal	DT0 to DT7
Control signal	XWR, XRD

3) Write can be done at the rise of XWR.

However, selection of a write register can be done at the fall of XWR.

DAC and register data are stored at D-FF.

4) Read appears on DT0 to DT7 at XRD = low.

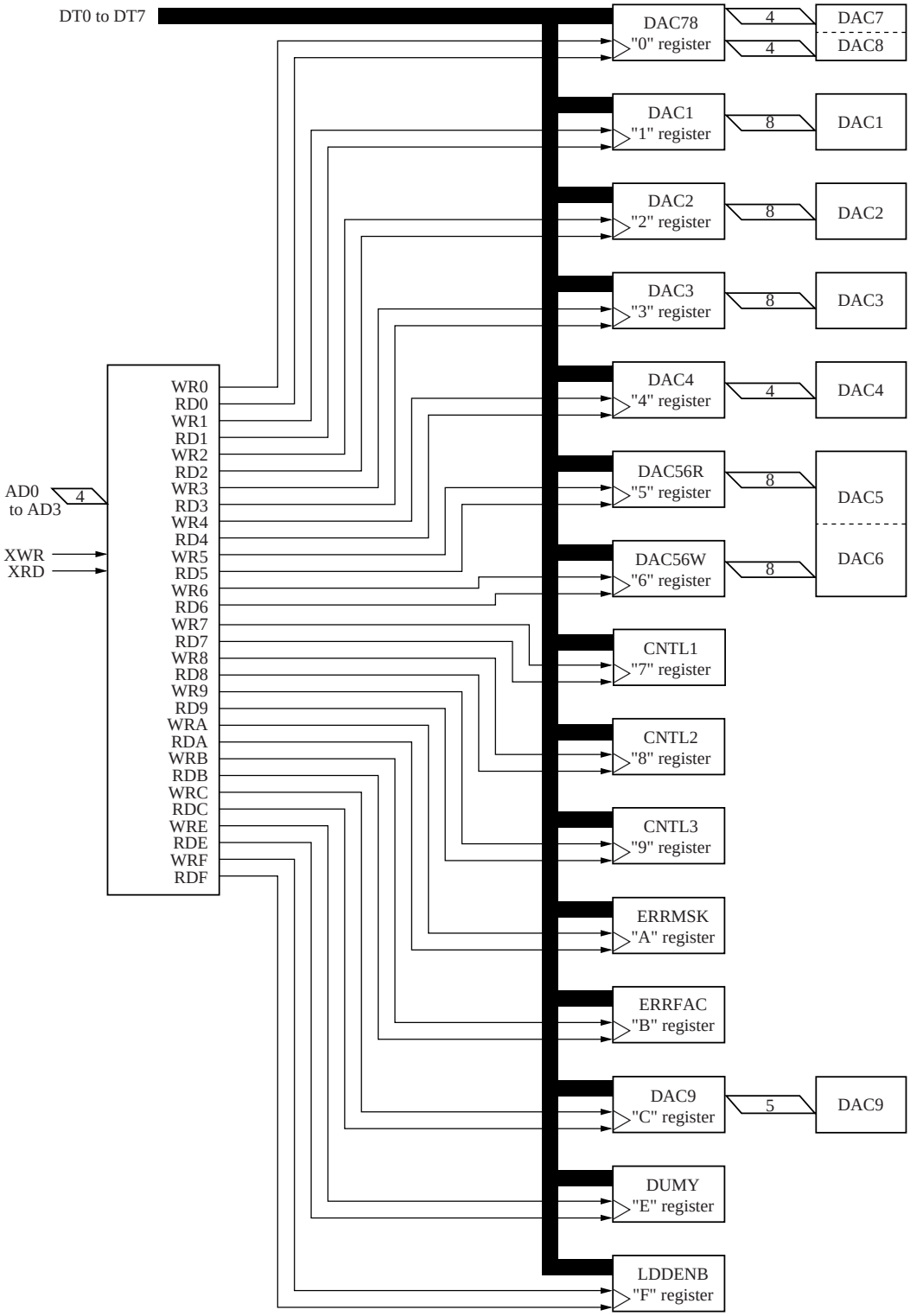
5) Refer to "■ Application Notes, 2. Timing chart" for the timing chart.

6) Each signal line is pulled up and down as below:

Pull-down to GND with 100 kΩ	AD0 to AD3
	DT0 to DT7
Pull-up to V_{CC} with 100 kΩ	XWR
	WRD

■ Application Notes (continued)

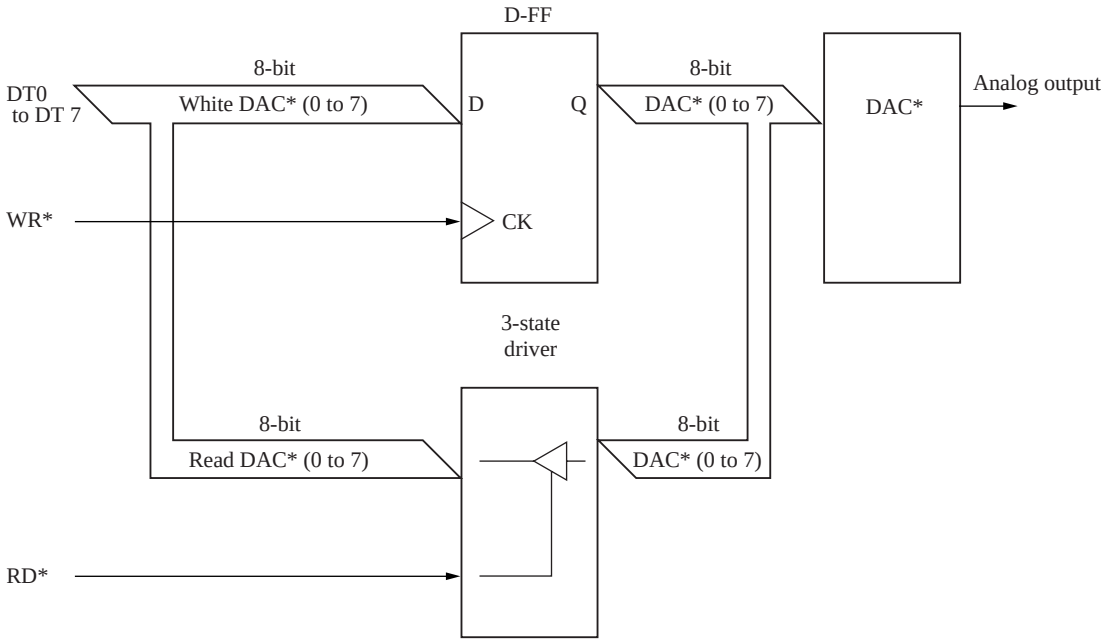
4. Signal flow



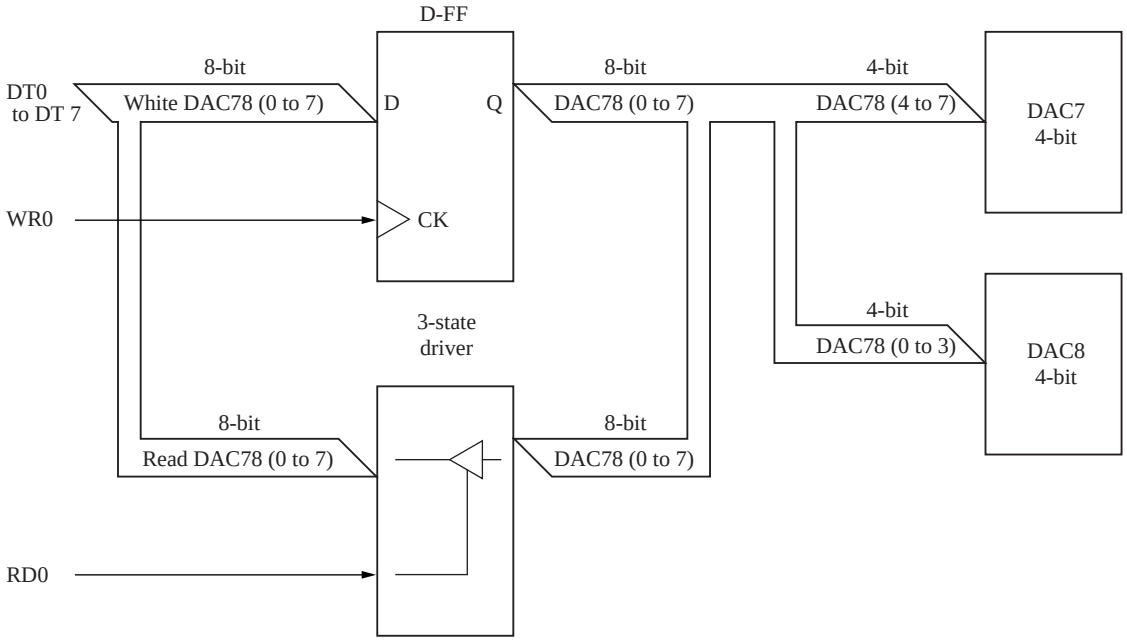
■ Application Notes (continued)

5. Register circuit configuration

1) DAC1, DAC2, DAC3, DAC4, DAC9



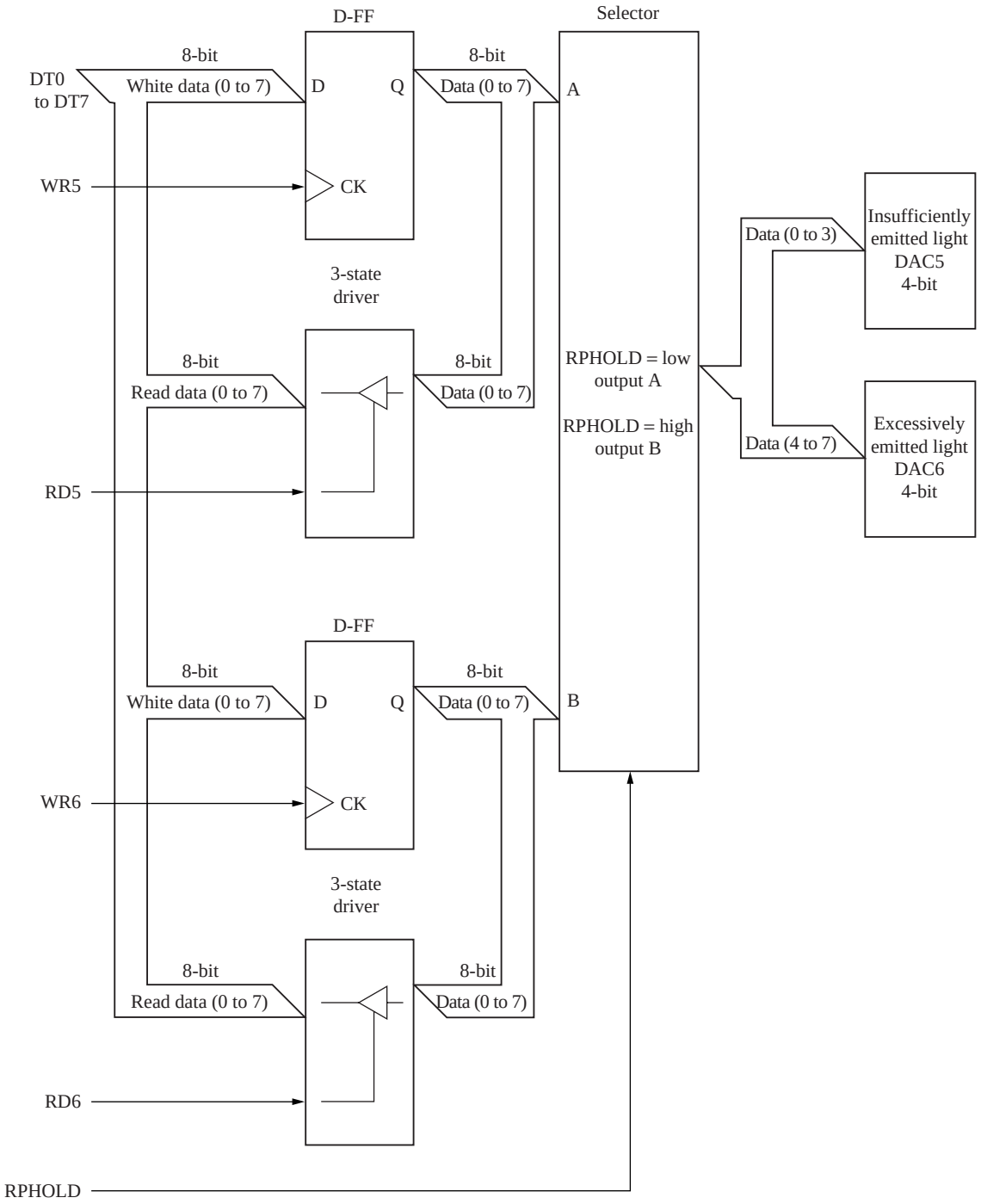
2) DAC7, DAC8



■ Application Notes (continued)

5. Register circuit configuration (continued)

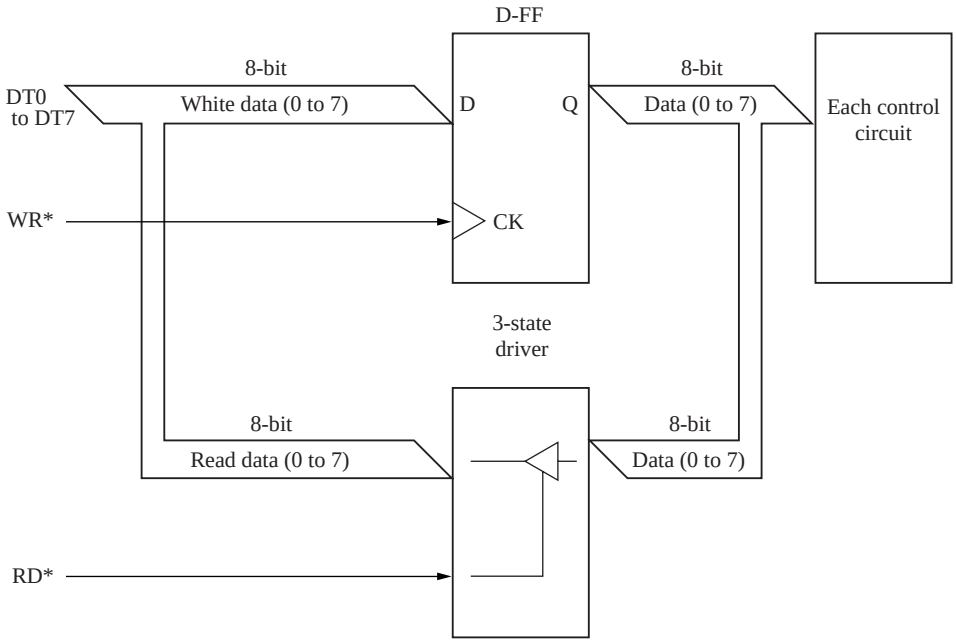
3) DAC56R, DAC56W



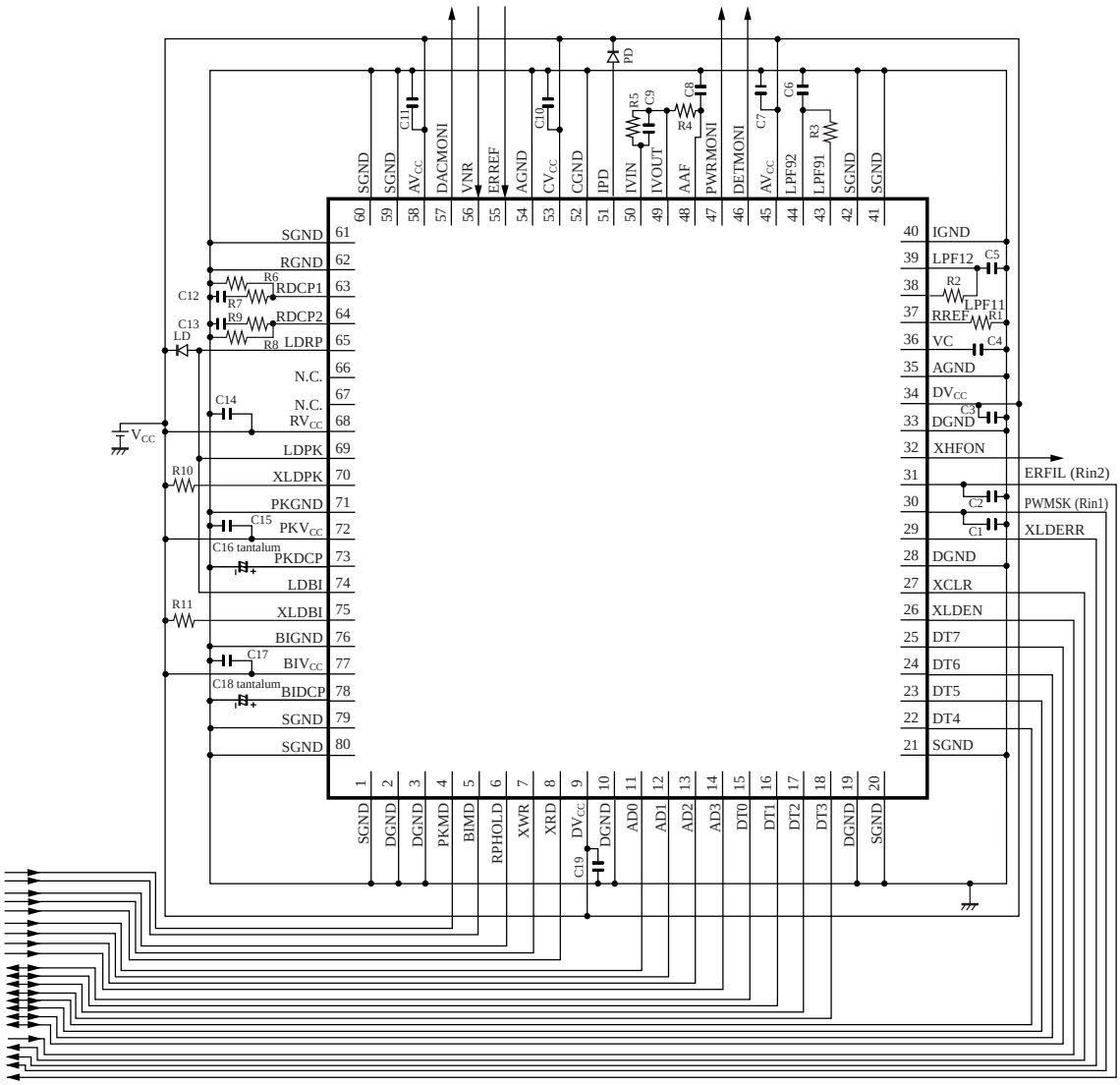
■ Application Notes (continued)

5. Register circuit configuration (continued)

4) CNTL1, CNTL2, CNTL3, ERRMSK, ERRFAC, DUMY, LDDENB



■ Application Circuit Example



■ Application Circuit Example (continued)

• Resistance and capacitance

Symbol	Resistor value	Unit
R1	10	kΩ
R2	—	—
R3	—	—
R4	—	—
R5	1	kΩ
R6	10	kΩ
R7	82	Ω
R8	10	kΩ
R9	82	Ω
R10	3	Ω
R11	3	Ω
(Rin1)	10	kΩ
(Rin2)	10	kΩ

Symbol	Resistor value	Unit
C1	220	pF
C2	100	pF
C3	0.1	µF
C4	0.01	µF
C5	—	—
C6	—	—
C7	0.1	µF
C8	—	—
C9	18	pF
C10	0.1	µF
C11	0.1	µF
C12	5 600	pF
C13	5 600	pF
C14	0.1	µF
C15	0.1	µF
C16	1	µF
C17	0.1	µF
C18	1	µF
C19	0.1	µF