FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-16314-2E

32-Bit Microcontroller

CMOS

FR60 MB91307 Series

MB91306R/MB91307R

■ DESCRIPTION

The FUJITSU FR family of single-chip microcontrollers using a 32-bit high-performance RISC CPU, with a variety of built-in I/O resources and bus control mechanisms for built-in control applications requiring high-capability, high-speed CPU processing. External bus access is assumed in order to support the expanded address space accessible by the 32-bit CPU, and a 1K bytes cache memory plus large RAM are provided for high-speed execution of CPU instructions.

This microcontroller is ideal for built-in applications such as DVD players, navigation systems, high-capability FAX and printer control that demand high-capability CPU processing power.

The MB91307 series is a FR60 family product based on the FR30/40 family CPU with enhanced bus access for higher speed operation.

■ FEATURES

FR CPU

- 32-bit RISC, load/store architecture, 5-stage pipeline
- Operating frequency 66MHz [with PLL: base frequency 16.5 MHz]
- 16-bit fixed length instructions (basic instructions), 1 instruction per cycle
- Instructions for built-in applications: memory-to-memory transfer, bit processing, barrel shift etc.
- Instructions adapted for high-level languages: function input/output instructions, register contents multi-load/store instructions

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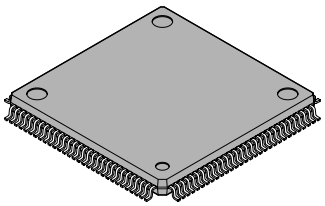
■ PACKAGE

120-pin, plastic LQFP



(FPT-120P-M21)

FUJITSU

- Easier assembler notation: register interlock function
- Built-in multiplier/instruction level support
  Signed 32-bit multiplication: 5 cycles
  Signed 16-bit multiplication: 3 cycles
- Interrupt (PC, PS removal): 6 cycles, 16 priority levels
- Harvard architecture for simultaneous execution of program access and data access
- CPU hold 4-word queue allows advanced instruction fetch function
- 4G bytes expanded memory space enables linear access
- Instruction compatible with FR30/40 family

Bus Interface

- Operating frequency: Max 33 MHz
- 8- or 16-bit data output
- Built-in pre-fetch buffer
- Unused data/address pins can be used as general-0purpose input/output ports
- Fully independent 8-area chip select outputs, can be set in minimum 64K bytes units
- Interface support for many memory types
  SRAM, ROM/Flash
  Page mode flash ROM, page mode ROM interface
  Burst mode flash ROM (select burst length 1, 2, 4, 8)
- Basic bus cycle: 2 cycles
- Programmable by area with automatic wait cycle generation to enable wait insert
- RDY input for external wait cycles
- DMA supports fly-by transfer with independent I/O wait control

Built-in RAM

- 128K bytes (MB91307R), 64K bytes (MB91306R)
- Accepts writing of data and instruction codes, enabling use as instruction RAM

Instruction cache

- 1K bytes capacity
- 2-way set associative
- 4-words (16 bytes) per set
- Lock function enables permanent program storage
- Areas not used for instruction cache can be used for RAM

DMAC (DMA controller)

- 5-channel (3-channel external-to-external)
- 3 transfer sources (external pin, internal peripheral, software)
- Addressing mode with 32-bit full address indication (increment, decrement, fixed)
- Transfer mode (demand transfer / burst transfer / step transfer / block transfer)
- Fly-by transfer support (3 channels between external I/O and external memory)
- Transfer data size selection 8/16/32-bit

Bit search module (using REALOS)

- Searches words from MSB for first bit position of a 1/0 change

Reload timer (includes 1 channel for REALOS)

- 16-bit timer: 3 channels
- Internal clock multiplier choice of x2, x8, x32

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UART

- Full duplex double buffer
- 3-channel
- Parity/no parity selection
- Asynchronous (start-stop synchronized), CLK-synchronized communications selection
- Built-in exclusive baud rate timer
- External clock can be used as transfer clock
- Variety of error detection functions (parity, frame, overrun)

I²C* interface

- Master/slave sending and receiving
- Clock synchronization function
- Transfer direction detection function
- Bus error detection function
- Arbitration function
- Slave address/general call address detection function
- Start condition repeat generator and detection function
- 10-bit/7-bit slave address
- Operates in standard mode (Max 100 Kbps) or high speed mode (Max 400 Kbps)

Interrupt controller

- Total of 9 external interrupts: 1 non-maskable interrupt pin ($\overline{\text{NMI}}$) and 8 normal interrupt pins INT7-INT0
- Interrupt from internal peripheral devices
- Programmable priority settings (16 levels) enabled, except for non-maskable interrupt
- Can be used for wake-up from stop mode

A/D converter

- 10-bit resolution, 4-channel
- Sequential comparator type, conversion time approx. 5.4 µs
- Conversion modes: single conversion mode, continuous conversion mode
- Startup source: software / external trigger / timer output signal

Other interval timers

- 16-bit timer with 3 channels (U-timer)
- Watchdog timer

I/O port

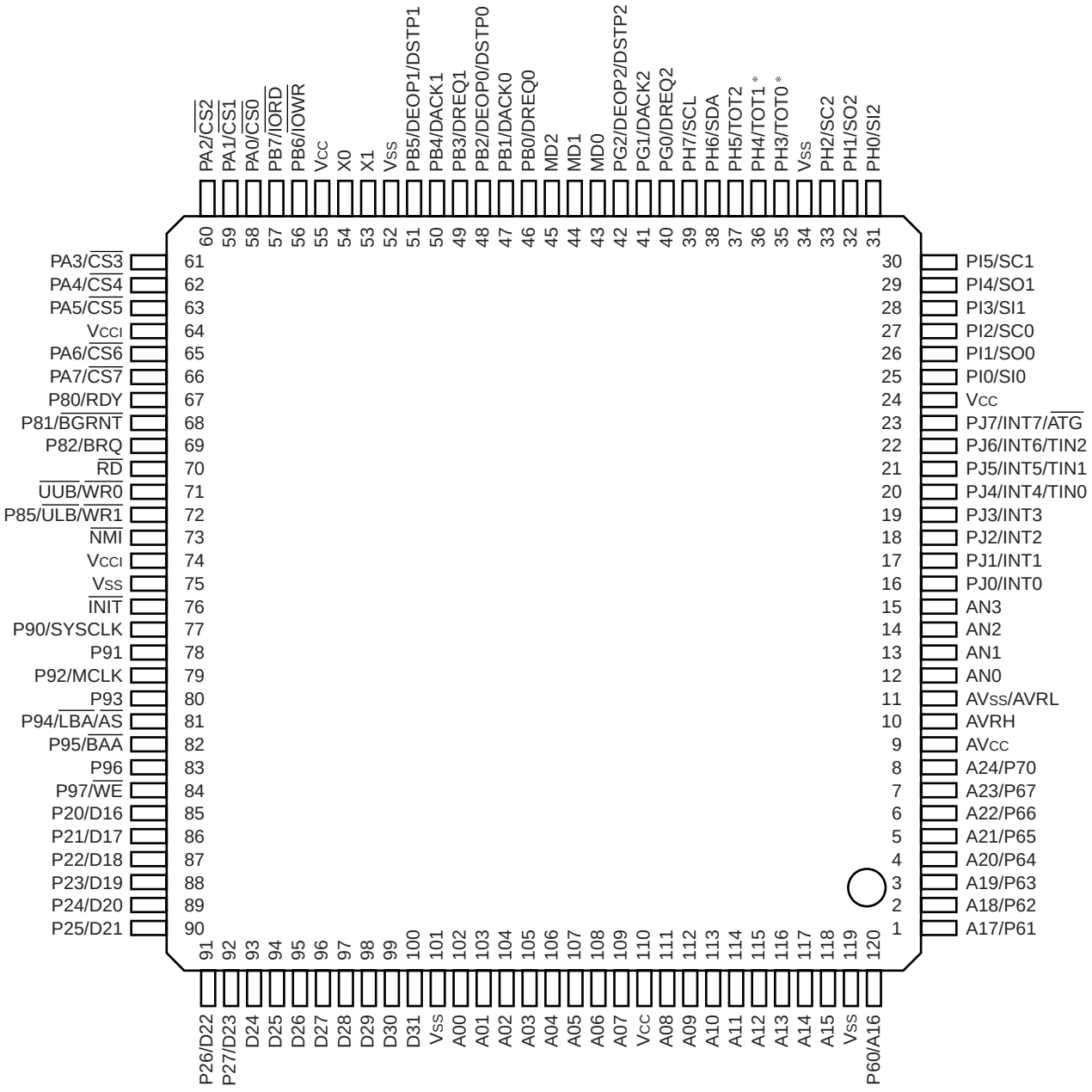
- Maximum 69 ports

Other features

- Built-in oscillator circuit for clock source, PLL multiplier selection enabled
- $\overline{\text{INIT}}$ reset pin
- Also included: watchdog timer reset, software reset
- Power-saving modes: stop mode, sleep mode supported
- Gear functions
- Built-in time base timer
- Packages: LQFP-120 (FPT-120P-M21) : MB91306R, MB91307R
  : MB91V307R (Evaluation products)
- CMOS technology : 0.25 µm : MB91V307R, 0.18 µm : MB91306R, MB91307R
- Supply voltage : MB91V307R : 3.3 V ± 0.3 V (built-in regulator 3.3 V → 2.5 V)
  : MB91306R, MB91307R : 3.3 V ± 0.3 V, 1.8V ± 0.15 V dual power supplies

* : Purchase of Fujitsu I²C components conveys a license under the Philips I²C Patent rights to use, these components in an I²C system provided that the system conforms to the I²C Standard Specification as defined by Philips.

■ PIN ASSIGNMENT



FPT-120P-M21

* : “L” level output after initialization and reset

■ PIN DESCRIPTIONS

Pin no.	Pin name	I/O circuit type	Description
85 to 92	D16 to D23	C	External data bus bit 16 to bit 23 Valid only in external bus 16-bit mode.
	P20 to P27		These pins can be used as ports in external bus 8-bit mode
93 to 100	D24 to D31	C	External data bus bit 24 to bit 31
102 to 109	A00 to A07	F	External address output bit0 to bit7
111 to 118	A08 to A15	F	External address output bit8 to bit15
120, 1 to 7	A16 to A23	F	External address output bit16 to bit23
	P60 to P67		These pins can be used as ports according to setting
8	A24	F	External data bus output bit24
	P70		This pin can be used as a port according to setting
9	AV_{CC}	—	Power supply pin. Analog power supply for A/D converter
10	AVRH	—	A/D converter reference voltage supply
11	AV_{SS}/AVRL	—	Power supply pin. Analog power supply for A/D converter
12 to 15	AN0 to AN3	D	A/D converter reference voltage supply. Analog input pin.
16 to 19	INT0 to INT3	I	External interrupt input. When the corresponding external interrupt is enabled, this input is in use at all times, so that output from other functions must be stopped unless used intentionally
	PJ0 to PJ3		General purpose input/output port
20 to 22	TIN0 to TIN2	I	Reload timer input. When the corresponding timer input is enabled, this input is in use at all times, so that output from other functions must be stopped unless used intentionally.
	INT4 to INT6		External interrupt input. When the corresponding external interrupt is enabled, this input is in use at all times, so that output from other functions must be stopped unless used intentionally.
	PJ4 to PJ6		General purpose input/output port
23	$\overline{ATG}$	I	A/D converter external trigger input. When selected as an A/D start source, this input is in use at all times, so that output from other functions must be stopped unless used intentionally.
	INT7		External interrupt input. When the corresponding external interrupt is enabled, this input is in use at all times, so that output from other functions must be stopped unless used intentionally.
	PJ7		General purpose input/output port
25	SI0	F	UART0 data input. When the UART0 channel is in input operation, this input is in use at all times, so that output from other functions must be stopped unless used intentionally.
	PI0		General purpose input/output port.
26	SO0	F	UART0 data output. This function is valid when the UART0 data output function setting is disabled.
	PI1		General purpose input/output port. This function is valid when the UART0 data output function setting is disabled.

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Pin no.	Pin name	I/O circuit type	Description
27	SC0	F	UART0 clock output. The clock output is valid when the UART0 clock output function setting is enabled.
	PI2		General purpose input/output port. This function is valid when the UART0 clock output function is disabled.
28	SI1	F	UART1 data input. When UART1 is set for input operation, this input is in use at all times, so that output from other functions must be stopped unless used intentionally.
	PI3		General purpose input/output port.
29	SO1	F	UART1 data output. This function is enabled when the UART1 data output function setting is enabled.
	PI4		General purpose input/output port. This function is valid when the UART1 data output function setting is disabled.
30	SC1	F	UART1 clock input/output. The clock output is enabled when the UART1 clock output function setting is enabled.
	PI5		General purpose input/output port. This function is valid when the UART1 clock output function setting is disabled.
31	SI2	F	UART2 data input. When UART2 is set for input operation, this input is in use at all times, so that output from other functions must be stopped unless used intentionally.
	PH0		General purpose input/output port.
32	SO2	F	UART2 data output. This function is enabled when the UART2 data output function setting is enabled.
	PH1		General purpose input/output port This function is enabled when the UART2 data output function setting is disabled.
33	SC2	F	UART2 clock input/output. The clock output is enabled when the UART2 clock output function setting is enabled.
	PH2		General purpose input/output port This function is enabled when the UART2 clock output function is disabled.
35	TOT0	C	Timer output port. This function is valid when the timer output setting is enabled.
	PH3		General purpose input/output port.This pin outputs an “L” level signal at reset.
36	TOT1	C	Timer output port. This function is valid when the timer output setting is enabled.
	PH4		General purpose input/output port.This pin outputs an “L” level signal at reset.
37	TOT2	C	Timer output port. This function is valid when the timer output is enabled.
	PH5		General purpose input/output port.

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Pin no.	Pin name	I/O circuit type	Description
38	SDA	Q	I^2C bus input/output port. This function is valid when I^2C operation is enabled. When the I^2C bus is in use, the port output must be set to Hi-Z level. When the I^2C bus is in use, this is an open drain pin.
	PH6		General purpose input/output port.
39	SCL	Q	I^2C bus input/output port. This function is valid when I^2C operation is enabled. When the I^2C bus is in use, the port output must be set to Hi-Z level. When the I^2C bus is in use, this is an open drain pin.
	PH7		General purpose input/output port.
40	DREQ2	F	DMA external transfer request input. When selected as a DMA startup source, this input is in use at all times, so that output from other functions must be stopped unless used intentionally.
	PG0		General purpose input/output port.
41	DACK2	F	DMA external transfer request acknowledge output. This function is valid when the DMA transfer request acknowledge output setting is enabled.
	PG1		General purpose input/output port. This function is valid when the DMA transfer request acknowledge output setting is enabled.
42	DEOP2	F	DMA external transfer end output. This function is valid when the DMA external transfer end output setting is enabled.
	DSTP2		DMA external transfer stop input. This function is valid when the DMA external transfer stop input setting is enabled.
	PG2		General purpose input/output port. This function is valid when the DMA external transfer end output selection and the DMA external transfer stop input selection are disabled.
43 to 45	MD2 to MD0	G	Mode pins 2 to 0. The setting of these two pins determines the basic operating mode. They should be connected to V_{CC} or V_{SS}.
46	DREQ0	F	DMA external transfer request input. When selected as a DMA startup source, this input is in use at all times, so that output from other functions must be stopped unless used intentionally.
	PB0		General purpose input/output port.
47	DACK0	F	DMA external transfer request acknowledge output. This function is valid when the DMA transfer request acknowledge output setting is enabled.
	PB1		General purpose input/output port. This function is enabled when the DMA transfer request acknowledge output setting is disabled.
48	DEOP0	F	DMA external transfer end output. This function is valid when the DMA external transfer end output setting is enabled.
	DSTP0		DMA external transfer stop input. This function is valid when the DMA external transfer stop input setting is enabled.
	PB2		General purpose input/output port. This function is valid when the DMA external transfer end output selection and the DMA external transfer stop input selection are disabled.

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Pin no.	Pin name	I/O circuit type	Description
49	DREQ1	F	DMA external transfer request input. When selected as a DMA startup source, this input is in use at all times, so that output from other functions must be stopped unless used intentionally.
	PB3		General purpose input/output port.
50	DACK1	F	DMA external transfer request acknowledge output. This function is valid when the DMA transfer request acknowledge output setting is enabled.
	PB4		General purpose input/output port. This function is enabled when the DNA transfer request acknowledge output setting is disabled.
51	DEOP1	F	DMA external transfer end output. This function is valid when the DMA external transfer end output setting is enabled.
	DSTP1		DMA external transfer stop input. This function is valid when the DMA external transfer stop input setting is enabled.
	PB5		General purpose input/output port. This function is valid when the DMA external transfer end output selection and the DMA external transfer stop input selection are disabled.
53	X1	A	Clock (oscillator) output
54	X0		Clock (oscillator) input
56	$\overline{\text{IOWR}}$	F	Write strobe output for DMA fly-by transfer. This function is valid when the DMA fly-by transfer write strobe output setting is enabled.
	PB6		General purpose input/output port. This function is valid when the DMA fly-by transfer write strobe output setting is disabled.
57	$\overline{\text{IORD}}$	F	Read strobe output for DMA fly-by transfer. This function is valid when the DMA fly-by transfer read strobe output setting is enabled.
	PB7		General purpose input/output port. This function is valid when the DMA fly-by transfer read strobe output setting is disabled.
58	CS0	F	Chip select output. This function is valid when the chip select 0 output setting is enabled.
	PA1		General purpose input/output port. This function is valid when the chip select 0 output setting is disabled.
59	CS1	F	Chip select output. This function is valid when the chip select 1 output setting is enabled.
	PA1		General purpose input/output port. This function is valid when the chip select 1 output setting is disabled.
60	CS2	F	Chip select output. This function is valid when the chip select 2 output setting is enabled.
	PA2		General purpose input/output port. This function is valid when the chip select 2 output setting is disabled.
61	CS3	F	Chip select output. This function is valid when the chip select 3 output setting is enabled.
	PA3		General purpose input/output port. This function is valid when the chip select 3 output setting is disabled.

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Pin no.	Pin name	I/O circuit type	Description
62	CS4	F	Chip select output. This function is valid when the chip select 4 output setting is enabled.
	PA4		General purpose input/output port. This function is valid when the chip select 4 output setting is disabled.
63	CS5	F	Chip select output. This function is valid when the chip select 5 output setting is enabled.
	PA5		General purpose input/output port. This function is valid when the chip select 5 output setting is disabled.
64	V_{CCI}	—	Internal Power supply pin (1.8 V power supply) .
65	CS6	F	Chip select output. This function is valid when the chip select 6 output setting is enabled.
	PA6		General purpose input/output port. This function is valid when the chip select 6 output setting is disabled.
66	CS7	F	Chip select output. This function is valid when the chip select 7 output setting is enabled.
	PA7		General purpose input/output port. This function is valid when the chip select 7 output setting is disabled.
67	RDY	C	External ready signal input. This function is valid when the external ready input setting is enabled.
	P80		General purpose input/output port. This function is valid when the external ready input setting is disabled.
68	$\overline{BGRNT}$	F	External bus open acknowledge output. This pin outputs an L level signal when the external bus is open. This function is valid when the output setting is enabled.
	P81		General purpose input/output port. This function is valid when the output setting is disabled.
69	BRQ	P	External bus open request input. The input value is “1” when the external bus is open. This function is valid when the input setting is enabled.
	P82		General purpose input/output port. This function is valid when the input setting is disabled.
70	$\overline{RD}$	M	External bus read strobe output.
71	$\overline{WR0}$ $\overline{UUB}$	F	External bus write strobe output. Upper side of the 16-bit SRAM input/output mask enable signal. It is valid when the external bus is set to SRAM use. ($\overline{WE}$/P97 function as the write strobe.)
72	$\overline{WR1}$ $\overline{ULB}$	F	External bus write strobe output. Lower side of the 16-bit SRAM input/output mask enable signal. It is valid when the external bus is set to SRAM use. ($\overline{WE}$/P97 function as the write strobe.)
	P85		General purpose input/output port. This function is valid when the enable output setting is disabled.

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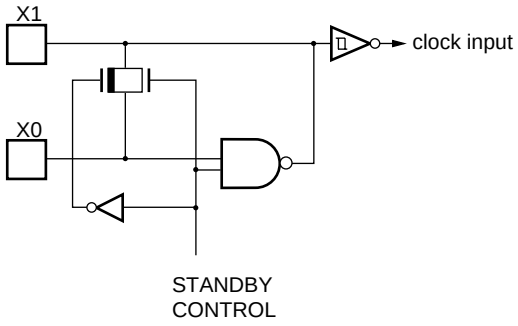
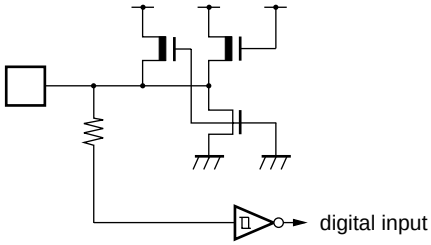
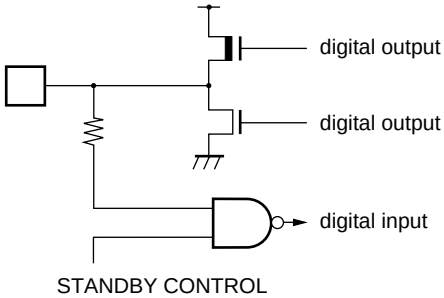
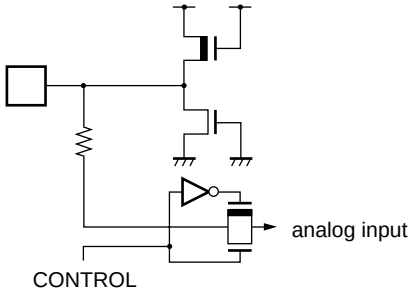
Pin no.	Pin name	I/O circuit type	Description
73	$\overline{\text{NMI}}$	H	$\overline{\text{NMI}}$ request input
74	V_{CCI}	H	Internal Power supply pin(1.8 V power supply)
76	$\overline{\text{INIT}}$	B	External reset input
77	SYSCLK	F	System clock output. This function is valid when the system clock output setting is enabled. The clock signal output is at the same frequency as the external bus operating frequency. Clock output halts in the stop mode or the hardware standby mode.
	P90		General purpose input/output port. This function is enabled when the system clock output setting is disabled.
78	P91	F	General purpose input/output port. This function is enabled when the SDRAM clock enable output setting is disabled.
79	MCLK	F	Memory clock output. Clock output halts in the sleep mode, the stop mode or the hardware standby mode.
	P92		General purpose input/output port. This function is enabled when the clock output setting is disabled.
80	P93	F	General purpose input/output port. This function is enabled when the SDRAM clock re-input setting is disabled.
81	$\overline{\text{AS}}$	F	Address strobe output. This function is valid when the address strobe output setting is disabled.
	$\overline{\text{LBA}}$		Burst flash ROM address load output. This function is valid when the address load output setting is enabled.
	P94		General purpose input/output port. This function is valid when the address load output and address strobe output settings are disabled.
82	$\overline{\text{BAA}}$		Burst flash ROM address advance output. This function is valid when the address advance output setting is enabled.
	P95		General purpose input/output port. This function is valid when the address advance output and column address strobe output settings are disabled.
83	P96	F	General purpose input/output port. This function is enabled when the column address strobe output setting is disabled.
84	$\overline{\text{WE}}$		Write strobe output for 16-bit SRAM. This function is enabled when the write strobe output setting is enabled.
	P97		General purpose input/output port. This function is enabled when the write strobe output setting is prohibited.
9	AV_{CC}	—	A/D converter power supply
10	AVRH	—	A/D converter power supply
11	AV_{SS}/AVRL	—	A/D converter power supply (GND)
24, 55, 110	V_{CC}	—	Power supply pins
34, 52, 75, 101	V_{SS}	—	Power supply pins (GND)

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• Oscillator feedback resistance approx. 1 MΩ
B		• CMOS hysteresis input with pull-up resistance (25 kΩ)
C		• CMOS level input/output with standby control
D		• Analog input with switch

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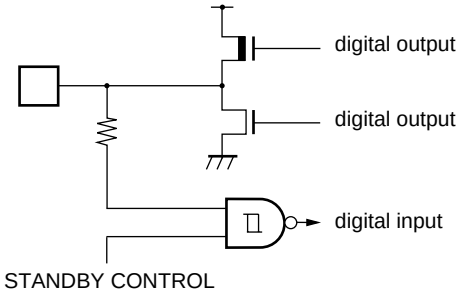
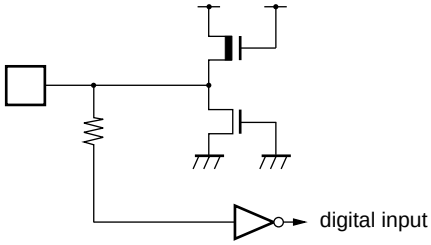
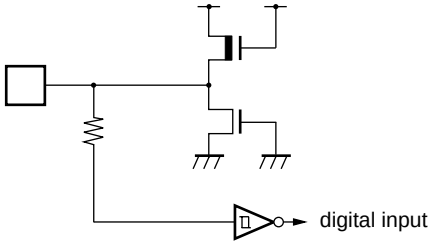
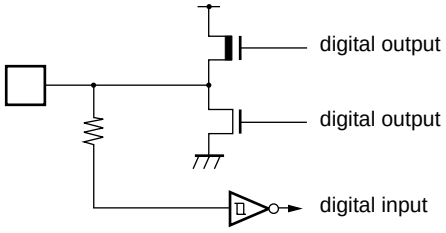
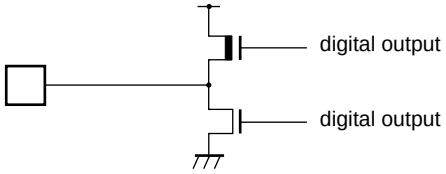
Type	Circuit	Remarks
F		• CMOS level output • CMOS level hysteresis input with standby control
G		• CMOS level input without standby control
H		• CMOS level hysteresis input without standby control
I		• CMOS level input • CMOS level hysteresis input without standby control
M		• CMOS level input

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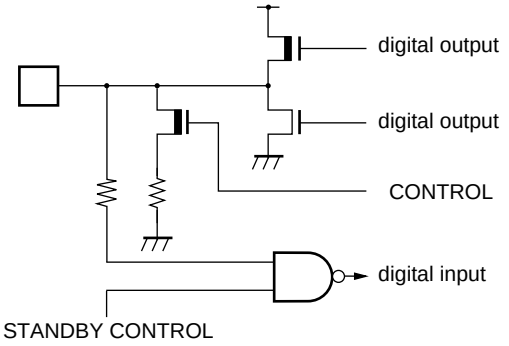
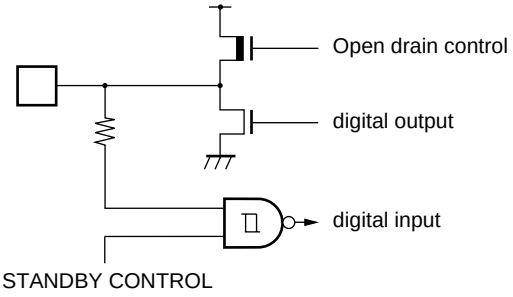
Type	Circuit	Remarks
P		• CMOS level input/output with standby control with pull-down resistance (25 kΩ)
Q		• Open drain output CMOS level hysteresis input with standby control

■ HANDLING DEVICES

❍MB91307 Series

• Preventing Latchup

When CMOS integrated circuit devices are subjected to applied voltages higher than V_{CC} at input and output pins (other than medium- and high-withstand voltage pins), or to voltages lower than V_{SS}, as well as when voltages in excess of rated levels are applied between V_{CC} and V_{SS}, a phenomenon known as latchup can occur. When a latchup condition occurs, supply current can increase dramatically and may destroy semiconductor elements. In using semiconductor devices, always take sufficient care to avoid exceeding maximum ratings.

• Treatment of unused pins

Do not leave an unused input pin open, since it may cause a malfunction. Handle by, using a pull-up or pull-down resistor.

• About power supply pins

In products with multiple V_{CC} or V_{SS} pins, the pins of the same potential are internally connected in the device to avoid abnormal operations including latch-up. However, you must connect the pins to external power supply and a ground line to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with the V_{CC} and V_{SS} pins of this device at the low impedance.

It is also advisable to connect a ceramic bypass capacitor of approximately 0.1 mF between V_{CC} and V_{SS} near this device.

• Notes on Power-ON/shut-down

Cautions to take when turning on/off V_{CCI} (1.8-V internal power supply) and V_{SS} (3.3-V external-pin power supply)

Do not apply V_{SS} (external) alone continuously (for over an indication of one minute) with V_{CCI} (internal) disconnected not to cause a reliability problem with the LSI.

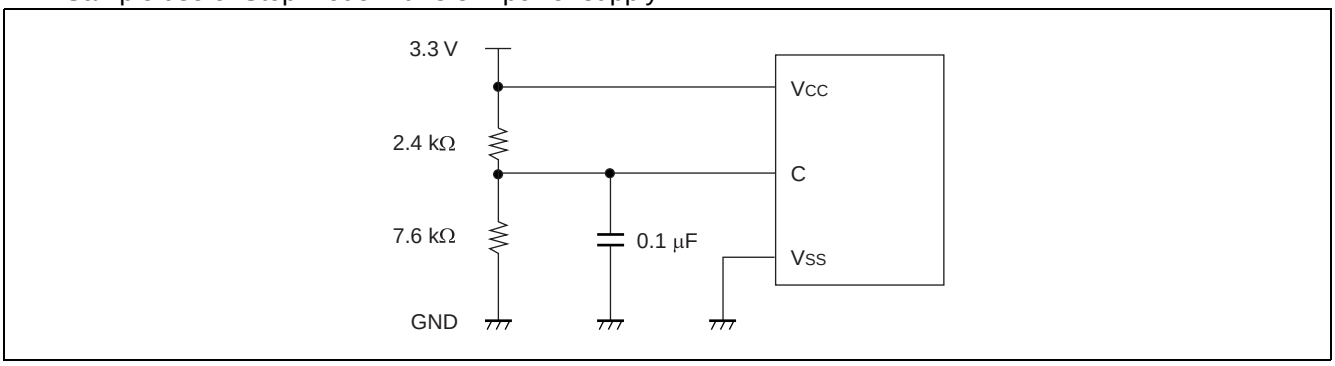
When V_{SS} (external) returns from the OFF state to the ON state, the circuit may fail to hold its internal state, for example, due to power supply noise.

When the power is turned on	V_{CCI} (internal) → V_{SS} (external) → Signal
When the power is turned off	Signal → V_{SS} (external) → V_{CCI} (internal)

• Precautions for use of stop mode

The built-in regulator in this device stops operating when the device is in stop mode. In such cases as when increased leak current (I_{CCH}) in stop mode, or abnormal operation or power fluctuation due to noise while in operating mode cause the regulator to stop, the internal 2.5 V power supply can ball below the voltage at which operation is assured. Therefore it is necessary when using the internal regulator and stop mode to assure that the external power supply does not fall below 3.3 V. And even if this should occur, the internal regulator can be set to restart when a reset is applied. (In this case the oscillator stabilization wait period should also be set to “L” level.)

- Sample use of Stop Mode with 3.3 V power supply



- About crystal oscillator circuit

  Noise near the X0 and X1 pins may cause the device to malfunction. Design the printed circuit board so that X0, X1, the crystal oscillator (or ceramic oscillator) , and the bypass capacitor to ground are located as close to the device as possible.

  It is strongly recommended to design the PC board artwork with the X0 and X1 pins surrounded by ground plane because stable operation can be expected with such a layout.

- Treatment of NC pins

  Any pins marked “NC” (not connected) must be left open.

- About mode pins (MD0 to MD2)

  Mode pins (MD0 to MD2) should be connected directly to V_{CC} or V_{SS} .

  To prevent the device erroneously switching to test mode due to noise, design the printed circuit board such that the distance between the mode pins and V_{CC} or V_{SS} is as short as possible and the connection impedance is low.

- Operation at startup

  Immediately after a power-on startup, always apply a reset initialization (INIT) at the $\overline{\text{INIT}}$ pin. Also, in order to assure a wait period for the oscillator circuits to stabilize immediately after startup, be sure that the “L” level input to the $\overline{\text{INIT}}$ pin continues for the required stabilization wait interval. (The INIT cycle for the $\overline{\text{INIT}}$ pin includes only the minimum setting for the stabilization wait period.)

- Base oscillator input at startup

  At power-on startup, always input a clock signal until the oscillator stabilization wait period is ended.

- Caution on Operations during PLL Clock Mode

  If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

- Precaution on using ports 6 and 7

  If one of P60/A15 to P70/A24, which are shared for output of external bus interface addresses, is used as a port, a grid voltage is applied to the port instantaneously when the status of another address output pin is changed. Therefore, add resistors or capacitors to those ports to prevent application of the grid voltage.

- Clock control block

  For L-level input to the $\overline{\text{INIT}}$ pin, allow for the regulator settling time or oscillation settling time.

- Bit search module

  The 0-detection, 1-detection, and transition-detection data registers (BSD0, BSD1, and BSDC) are only word-accessible.

- Prefetch

  When accessing a prefetch-enabled little endian area, use word access only (access in 32 bits).

  Byte or halfword access results in wrong data read.

- Setting of external bus

  The MB91307 series is guaranteed at an external bus frequency of 33 MHz. As the external bus is capable of supporting 66 MHz for future enhancements, the initial value is the same rate as the base clock (determined by the PLL setting) . The external bus is set to 66 MHz if you set the base clock to 66 MHz with the external-bus base clock division setting register (DIVR1) containing the initial value. To change the base clock frequency, set the external bus frequency not exceeding 33 MHz and set the new base clock frequency.

- MCLK and SYSCLK

  MCLK causes a stop in SLEEP/STOP mode while SYSCLK causes a stop only in STOP mode. Use either depending on each application.

- I^2C input/output pin

  The SDA and SCL pins of the MB91307 series are pseudo open-drain pins with the P-ch transistor turned off to prevent the “H” level from being output. As the circuit configuration has a diode added to the V_{CC} side, therefore, the communication voltage must be adjusted to the 3.3-V power supply of this model (pulled up to a voltage of 3.3 V) .

- Shared port function switching

  To switch a pin that also serves as a port, use the port function register (PFR). Note, however, that bus pins are switched depending on external bus settings.

- Pull-up control

  Connecting a pull-up resistor to the pin serving as an external bus pin cannot a guarantee the AC standard.

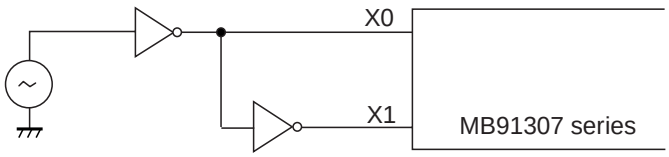
  Even the port for which a pull-up resistor has been set is invalid in stop mode with HIZ = 1 or in hardware standby mode.

- I/O port access

  Byte access only for access to port

- Remarks for the external clock operation

  When selecting the external clock, active X0 pin generally. Also simultaneously the opposite phase clock to X0 must be supplied to X1 pin. When using the clock along with STOP (oscillation stopped) mode, the X1 pin stops when “H” is input in STOP mode. To prevent one output from competing against another, in this case, the stop mode must not be used.



Using external clock (normal)

Note : Stop mode (oscillation stop mode) cannot be used.

- Low-power consumption modes
  - To enter the standby mode, use the synchronous standby mode (set with the SYNCS bit as bit 8 in the TBCR, or time-base counter control register) and be sure to use the following sequence:

```
(LDI     #value_of_standby, R0)
(LDI     #_STCR, R12)
STB      R0, @R12          ; Write to standby control register (STCR)
LDUB     @R12, R0          ; Read STCR for synchronous standby
LDUB     @R12, R0          ; Read STCR again for dummy read
NOP                        ; NOP x 5 for timing adjustment
NOP
NOP
NOP
NOP
```

    Set the I-flag and the ILM and ICR registers to branch to an interrupt handler when the interrupt handler triggers the microcontroller to return from the standby mode.

  - If you use the monitor debugger, follow the precautions below:

    Do not set a breakpoint within the above array of instructions.
    Do not single-step the above array of instructions.

- Current at power-on (only for MB91V307R)

  About 300 mA of power supply current flows when the power is turned on with $\overline{\text{INIT}}$ set to 0.

  Set $\overline{\text{INIT}}$ to 1 to stop the overcurrent flowing. After that, the overcurrent will not flow even if $\overline{\text{INIT}}$ is set to 0.

- Watchdog timer

  The watchdog timer function of this model monitors that a program delays a reset within a certain period of time and resets the CPU if the program fails to delay it, for example, because the program runs out of control. Once the watchdog timer function is enabled, therefore, the watchdog timer countinues to operate until a reset takes place.

  An exception, for example during stop, sleep and DMA transfer modes, is the automatic delaying of a reset under a condition in which the CPU stops program execution.

  Note, however, that a watchdog reset may not occur in the above state caused when the system runs out of control. If this is the case, use the external $\overline{\text{INIT}}$ pin to cause a reset (INIT).

- Terminal and timing control register (TCR) (0x00000683)

  The terminal and timing control register (TCR) is a write-only register. Therefore, do not access TCR with a bit manipulation instruction.

  If you intend to disable sharing of the bus by writing “0” to Bit 7 (BREN bit) of TCR when the bit is “1”, be sure to follow the procedure below. If the procedure is not followed, the device may hang up.

  1. Write “0” to Bit 2 (BRQE bit) of the port 8 function register (PFR8).
  2. Write “0” to Bit 7 (BREN bit) of TCR.

- $\overline{RD}/\overline{WR} \rightarrow \overline{CS}$ hold extension cycle

  Assume that use of the $\overline{RD}/\overline{WR} \rightarrow \overline{CS}$ hold extension cycle is specified (Bit 0 of AWR is 1) for an area for which the normal memory/IO access type is set (the TYPE3 to TYPE0 bits of ACR are 0xxx). Even in this case, the hold extension cycle might not be inserted when the operation and settings are specified in a specific combination.

  The hold extension cycle will not be inserted when the following conditions are met:
  - Use of the $\overline{RD}/\overline{WR} \rightarrow \overline{CS}$ hold extension cycle is specified.
    (Bit 0 [W00 bit] of AWR is 1.)
  - A normal memory/IO access type is set for the area.
    (Bits 3 to 0 [TYPE3 to TYPE0 bits] of ACR are 0xxx.)
    Note: The MB91307 series allows only this type to be set.
  - Disuse of the address $\rightarrow \overline{CS}$ delay cycle is specified.
    (Bit 2 [W02 bit] of AWR is 0.)
  - A setting (recovery enabled) other than 0 cycle is made for the write recovery cycle.
    (Bits 5 and 4 [W05 and W04 bits] of AWR are other than 00.)
    (Example: First word writing to an external bus 16-bit area)
  - If an access is made to write data larger than the bus width to the relevant area under the above conditions, the $\overline{RD}/\overline{WR}$-$\overline{CS}$ hold extension cycle is not inserted in any cycle other than the last cycle to write divisions of the data. Therefore, the hold time becomes insufficient.
    Note : This problem does not occur in the read cycle.

  To use this function, make either of the following settings:
  - Specify the use of the address $\rightarrow \overline{CS}$ delay cycle.
    (Set 1 for Bit 2 [W02 bit] of AWR.)
  - Specify 0 cycle for the write recovery cycle.
    (Set 00 for Bits 5 and 4 [W05 and W04 bits] of AWR.)

- Signed DIVIDE statement (DIVOS)

  When the instruction immediately before the instruction of DIVOS is an instruction by which the memory access is done, a correct calculation result might not be obtained.

  This is generated under the following conditions.

  - When the instruction performs memory accesses just before a DIVOS instruction.

    Note : Instructions that performs relevant memory accesses (a total of 58 instructions)

ST Ri, @- R15	ST Rs, @- R15	ST PS, @- R15
STB Ri, @Rj	STB Ri, @ (R13, Rj)	DMOVB R13, @dir8
STB Ri, @ (R14, disp8)	LDUB @Rj, Ri	LD @ (R13, Rj), Ri
LDUH @ (R13, Rj), Ri	LDUB @ (R13, Rj), Ri	DMOV @dir10, R13
DMOVH @dir9, R13	DMOVB @dir8, R13	LD @ (R14, disp10), Ri

LDUH @ (R14, disp9), Ri	LDUB @ (R14, disp8), Ri	AND Rj, @Ri
ANDH Rj, @Ri	ANDB Rj, @Ri	ORB Rj, @Ri
EORB Rj, @Ri	DMOV @R13+, @dir10	DMOVH @R13+, @dir9
DMOVB @R13+, @dir8	DMOV @dir10, @R13+	DMOVH @dir9, @R13+
DMOVB @dir8, @R13+	DMOV @R15+, @dir10	DMOV @dir10, @- R15

- When full trace mode is specified as trace mode and the DIVOS and DIV1 instructions are not 4-byte aligned.
- Even if the DIVOS and DIV1 instructions are 4-byte aligned, perform a D-bus DMA transfer or specify the full trace mode as trace mode if a breakpoint is set in the DIV1 instruction.

Avoid this notes as follows:

(1) Do not place an instruction that performs memory access before a DIVOS instruction.
(2) Do not perform a DMA transfer to the D-bus or set full trace mode as trace made when a DIVOS instruction is specified.

To output the code for avoiding above (1) condition, specify "-@div0s 1" as the compiler option.

SOFTUNE compiler:

- In case of using the SOFTUNE V3: after the SOFTUNE compiler V30L07R07
- In case of using the SOFTUNE V5: after the SOFTUNE compiler V50L04
- In case of using the SOFTUNE V6: after the SOFTUNE compiler V60L01

- DMA demand transfer

In sleep mode, demand transfer is executed only once and processing does not go further. During normal operation, the efficiency of demand transfers may seem to be lowered.

This action occurs only in demand transfers (it does not occur in DREQ edge detection mode or the like).

This is occurred in the following cases:

- A demand transfer by DMAC is performed in sleep mode.
  - After a demand transfer is performed once, processing does not go further although DREQ is input successively.
  - A subsequent transfer is started if the device is released from sleep mode and an external bus operation other than a DMA transfer occurs.
- A demand transfer by DMAC is performed during normal operation.
  - After a demand transfer is performed once, a subsequent transfer is not performed until an external bus access other than a DMA transfer occurs.
  - A demand transfer does not progress while there is no external bus access because cache hitting is performed continuously or internal ROM operation continues.
- A subsequent demand transfer is not started even if an external bus access for prefetching occurs.

Avoid this notes as follows:

- Do not perform a demand transfer by DMAC in sleep mode.
- Do not use sleep mode during a demand transfer by DMAC.

- RMW instructions using R15

  If one of the instructions listed below is executed, the value of SSP or USP* is not used as the value of R15 and, as a result, an incorrect value is written to memory. Therefore, the compiler does not generate the following instructions:

AND	R15,@Rj	ANDH	R15,@Rj	ANDB	R15,@Rj
OR	R15,@Rj	ORH	R15,@Rj	ORB	R15,@Rj
EOR	R15,@Rj	EORH	R15,@Rj	EORB	R15,@Rj
XCHB	@Rj,R15				

  * : R15 is an insubstantial register. If R15 is accessed by a program, SSP or USP is accessed according to the state of the S flag of the PS register.

  Avoid this notes as follows:
  - When programming any of the above 10 instructions by an assembler, specify a general-purpose register in place of R15.

- Executing instructions on RAM
  - If instruction codes are placed in RAM, they should not be placed in the last 8 address bytes 0005 FFF8$_H$ to 0005 FFFF$_H$. (Instruction code prohibited area)

- Notes on the PS register

  Since some instructions manipulate the PS register earlier, the following exceptions may cause the interrupt handler to break or the PS flag to update its display setting when the debugger is being used. As the microcontroller is designed to carry out reprocessing correctly upon returning from such an EIT event, it performs operations before and after the EIT as specified in either case.

  - The following operations may be performed when the instruction immediately followed by a DIVOU/DIVOS instruction is (a) halted by a user interrupt or NMI, (b) single-stepped, or (c) breaks in response to a data event or emulator menu:
    (1) D0 and D1 flags are updated earlier.
    (2) The EIT handler (user interrupt/NMI or emulator) is executed.
    (3) Upon returning from the EIT, the DIVOU/DIVOS instruction is executed and the D0 and D1 flags are updated to the same values as those in (1) above.
  - The following operations are performed when the ORCCR/STILM/MOV Ri and PS instructions are executed to enable interruptions when a user interrupt or NMI trigger event has occurred.
    (1) The PS register is updated earlier.
    (2) The EIT handler (user interrupt/NMI or emulator) is executed.
    (3) Upon returning from the EIT, the above instructions are executed and the PS register is updated to the same value as that in (1) above.

- Notes on I-bus Memory

  Do not access data in the instruction cache control register or the instruction cache RAM immediately before the RETI instruction.

❍Unique to the evaluation chip MB91V307R

• Simultaneous occurrences of a software break and a user interrupt/NMI

When a software break and a user interrupt /NMI take place at the same time, the emulator debugger can cause the following phenomena:

• The debugger stops pointing to a location other than the programmed breakpoints.
• The halted program is not re-executed correctly.

If these phenomena occur, use a hardware break instead of the software break. If the monitor debugger has been used, avoid setting any break at the relevant location.

• Single-stepping the RETI instruction

If an interrupt occurs frequently during single stepping, execute only the relevant processing routine repeatedly after single-stepping RETI. This will prevent the main routine and low-interrupt-level programs from being executed. Do not single-step the RETI instruction for avoidance purposes. When the debugging of the relevant interrupt routine becomes unnecessary, perform debugging with that interrupt disabled.

• Break function

- If the address of a current system stack pointer or an area that includes a stack pointer is specified as an object address of a hardware break (including an event break), a break occurs after one instruction is executed. The break occurs although the relevant user program does not include an actual data access instruction. To avoid this problem, do not set the (word) access to an area that includes the address of a system stack pointer as a target of a hardware break (including an event break).
- If an instruction that causes a wait is executed between an instruction to read a branch destination address from memory and a branch instruction, an instruction alignment error occurs at a point where an instruction alignment error cannot occur originally. Then, an ICE break (CPU error break) occurs, and execution of instructions stops. Furthermore, even if an instruction break is set for the branch destination address at the point where the above error occurs, a break might not occur.

```
Example:  LD     @R1,R0  ; read F-bus RAM
          LD     @R2,R3  ; read F-bus RAM
          CALL   @R0     ; An incorrect alignment error may occur or a break might not occur.
```

To avoid the incorrect alignment error as described above, turn off the alignment error function in debugger function setup.

To perform the instruction break correctly, do not specify use of a hardware break, but specify use of a software break in debugger function setup.

• Trace mode

If the trace mode for debugging is set to full trace mode, which uses internal FIFO memory as the output buffer, the current may increase or DMA access to the D-bus may be lost.

This is occurred if:

- A DMA transfer to the D-bus or standby mode occurs in full trace mode.

Use internal trace mode to avoid this notes.

- Alignment error (emulator debugger)

  Assume that instruction alignment error break is enabled and an instruction that causes a wait is executed between an instruction to read a branch destination address from memory and a branch instruction. Under these conditions, an instruction alignment error occurs at a point where an instruction alignment error cannot occur originally, an ICE break occurs, and execution of instructions stops. Then, a message indicating an unknown break factor or a CPU error break is output.

  Furthermore, even if an instruction break is set for the branch destination address at the point where the above error occurs, a break might not occur.

  This problem occurs if the following three types of instructions are executed successively:

  (1) LD or DMOV instructions causing a wait (reading a branch destination address)

LD	@Rj,Ri	LDUH @Rj,RI	
LD	@(R13,Rj)Ri	LDUH @(R13,Rj),Ri	LDUB @(R13,Rj),Ri
LD	@(R14,disp10),Ri	LDUH @(R14,disp9),Ri	LDUB @(R14,disp8),Ri
LD	@R15+,Ri	LD @R15+,Rs	LD @R15+,PS
DMOV	@dir10,R13	DMOVH @dir9,R13	DMOVB @dir8,R13

  (2) Instructions causing a wait (reading F-bus RAM or external memory)

  (3) Branch instructions such as JMP @Ri, JMP: D @Ri, CALL @Ri, CALL: D @Ri, RET, and RET: D

```
Example:    LD@R1,R0    ;read F-bus RAM
            LD@R2,R3    ;read F-bus RAM
            CALL @R0
```

  Avoid this notes as follows:

  Assume that instruction alignment error break is enabled and an instruction that causes a wait is executed between an instruction to read a branch destination address from memory and a branch instruction. Under these conditions, an instruction alignment error occurs at a point where an instruction alignment error cannot occur originally, an ICE break occurs, and execution of instructions stops. Then, a message indicating an unknown break factor or a CPU error break is output.

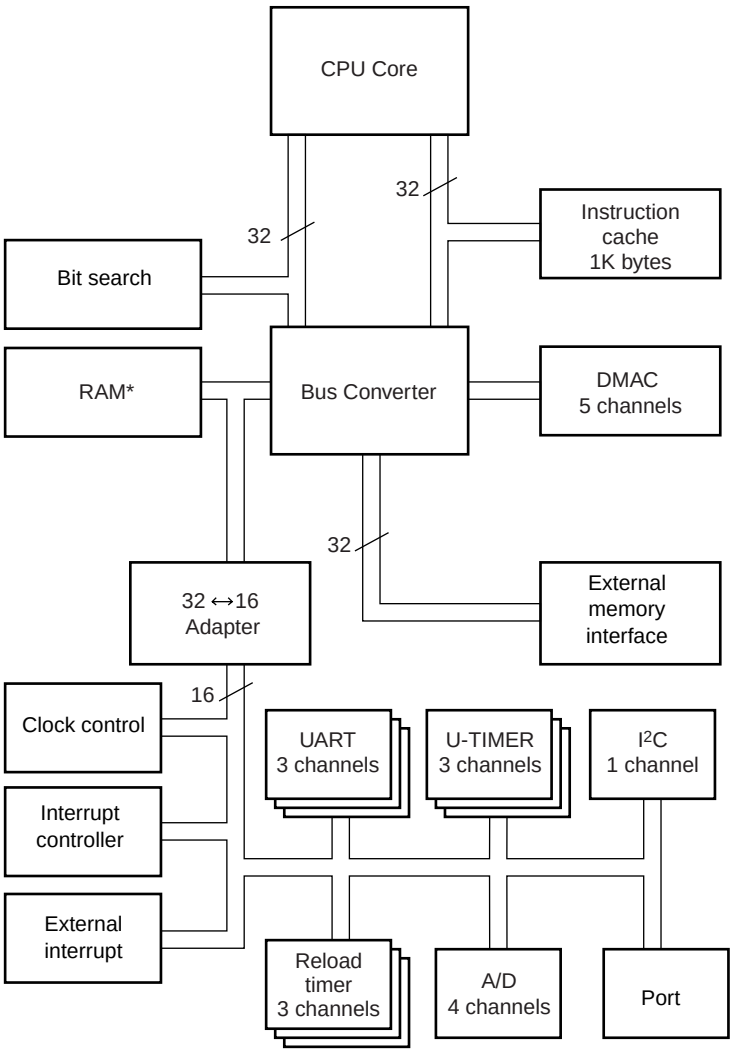
  Furthermore, even if an instruction break is set for the branch destination address at the point where the above error occurs, a break might not occur.

  Avoid this problem as follows:
  - To avoid the incorrect alignment error as described above, turn off the alignment error function in debugger function setup.
  - To perform the instruction break correctly, set the break point in an address other than the branch destination address.

- Operand break

  A stack pointer placed in an area set for a DSU operand break can cause a malfunction. Do not apply a data event break to access to the area containing the address of a system stack pointer.

■ BLOCK DIAGRAM



* : Internal RAM 128K bytes for MB91307R
64K bytes for MB91306R

■ CPU AND CONTROL BLOCK

Internal Architecture

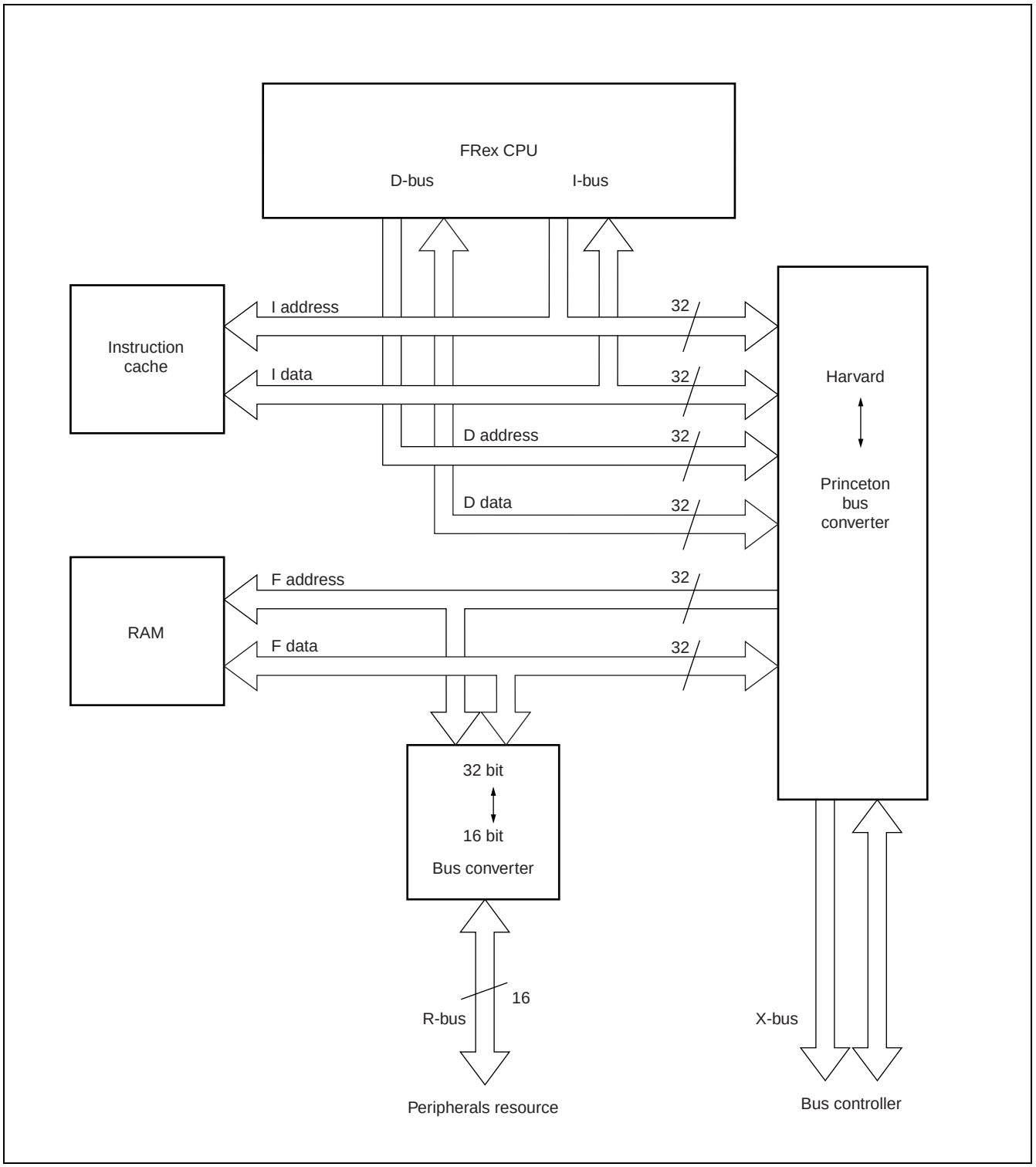
The FR series CPU is a high-performance core using RISC architecture with a high-capability instruction set intended for built-in applications.

1. Features

- Uses of RISC Architecture
  Basic instruction set: 1 instruction to 1 cycle.
- 32-bit architecture
  General-purpose registers: 32-bits × 16 registers
- 4G bytes linear memory space
- Built-in multipliers
  32-bit × 32-bit multiplication: 5 cycles
  16-bit × 16-bit multiplication: 3 cycles
- Enhanced interrupt processing
  High-speed response (6 cycles)
  Multiple interrupt support
  Level masking functions (16 levels)
- Enhanced I/O operating instructions
  Memory-to-memory transfer instructions
  Bit processing instructions
- High code efficiency
  Basic instruction length: 16 bits
- Low power consumption
  Sleep mode, stop mode
- Gear function

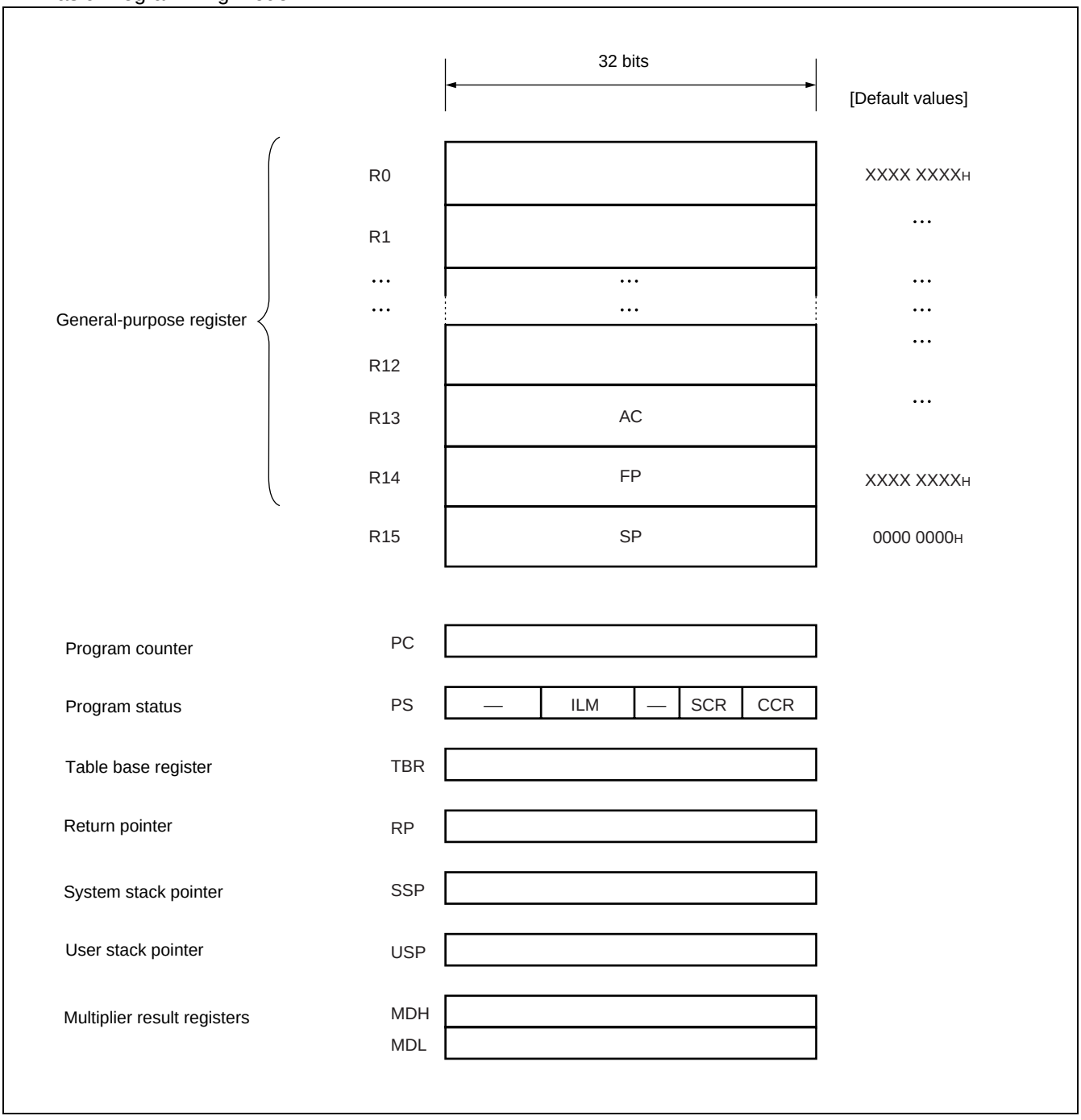
2. Internal Architecture

The FR series CPU uses a Harvard architecture with independent instruction bus and data bus. The instruction bus (I-bus) is connected to an on-chip instruction cache. a 32-bit ←→16-bit bus converter is connected to the bus (F-bus) to provide an interface between the CPU and peripheral resources. The Harvard ←→ Princeton bus converter is connected to the both the I-bus and D-bus as an interface between the CPU and bus controller.



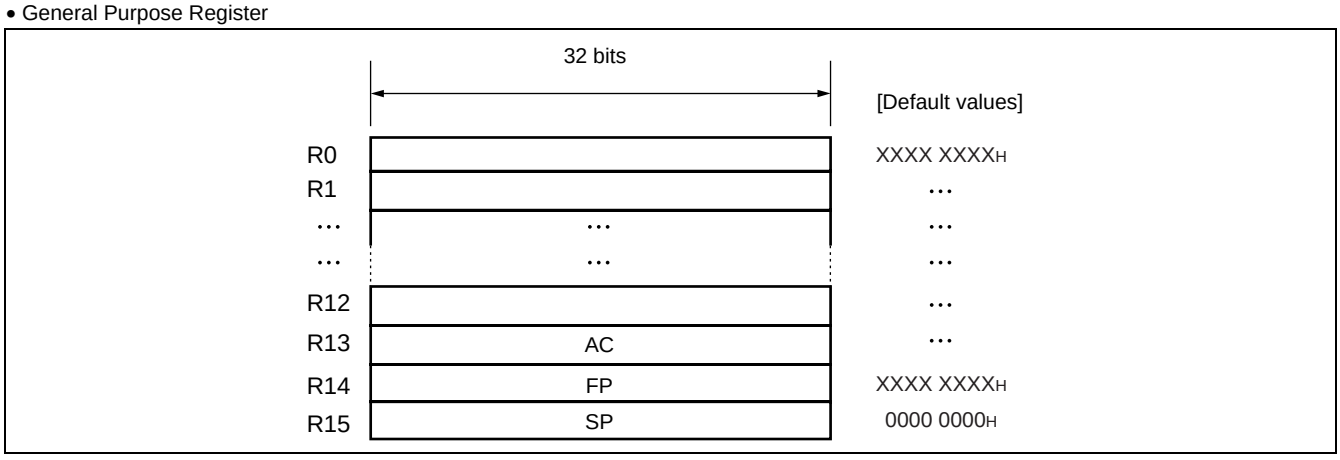
3. Programming Model

- Basic Programming Model



4. Registers

• General Purpose Register



Registers R 0 to R 15 are general-purpose registers. These registers can be used as accumulators for computation operations, or as pointers for memory access.

Of the 16 registers, enhanced commands are provided for the following registers to enable their use for particular applications.

R13: Virtual accumulator

R14: Frame pointer

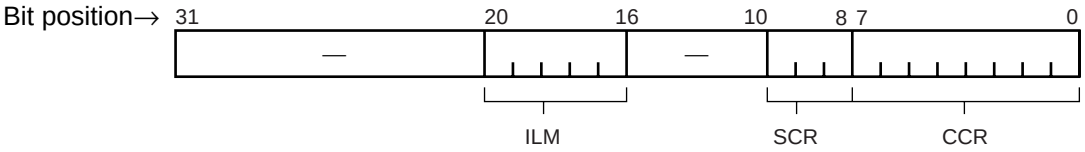
R15: Stack pointer

Default values at reset are undefined for R0 to R14. The value for R15 is 00000000H (SSP value).

• PS (Program Status Register)

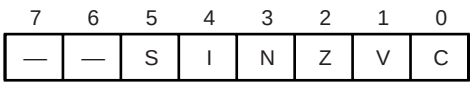
This register holds the program status, and is divided into three parts, ILM, SCR, and CCR.

All bits not defined in the diagram are reserved bits with read value “0” at all times. Write access to these bits is not enabled.



PS Register

• CCR (Condition Code Register)



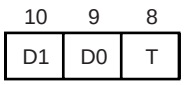
[Default value]

- - 00XXXXB

CCR Register

S : Stack flag, cleared to “0” at reset.
I : Interrupt flag, cleared to “0” at reset.
N : Negative flag, default value at reset undefined.
Z : Zero flag, default value at reset undefined.
V : Overflow flag, default value at reset undefined.
C : Carry flag, default value at reset undefined.

- SCR (System Condition code Register)



[Default value]
$XX0_B$

SCR Register

Stepwise division flags

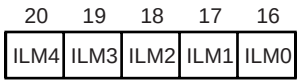
These flags store interim data during execution of stepwise division.

Step trace trap flag

Indicates whether the step trace trap is enabled or disabled.

The step trace trap function is used by emulators. When an emulator is in use, it cannot be used in execution of user programs.

- ILM(Interrupt Level Mask Register)



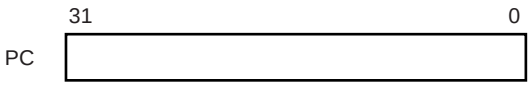
[Default value]
01111_B

ILM Register

This register stores interrupt level mask values, for use in level masking.

The register is initialized to value 15 (01111_B) at reset.

- PC (Program Counte Registerr)



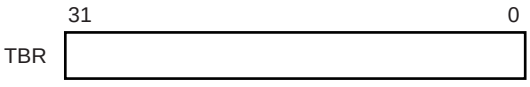
[Default value]
$XXXXXXXX_H$

PC Register

The program counter indicates the address of the instruction that is executing.

The default value at reset is undefined.

- TBR (Table Base Register)



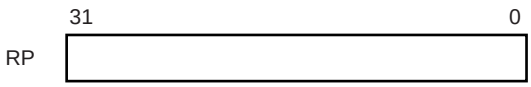
[Default value]
$000FFC00_H$

TBR Register

The table base register stores the starting address of the vector table used in EIT processing.

The default value at reset is $000FFC00_H$.

- RP (Return Pointer)



[Default value]
$XXXXXXXX_H$

RP Register

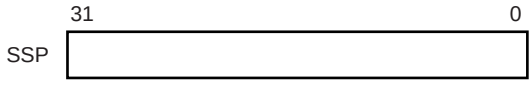
The return register stores the address for return from subroutines.

During execution of a CALL instruction, the PC value is transferred to this RP register.

During execution of a RET instruction, the contents of the RP register are transferred to this PC register.

The default value at reset is undefined.

- SSP (System Stack Pointer)



[Default value]
00000000_H

SSP Register

The SSP register is the system stack pointer.

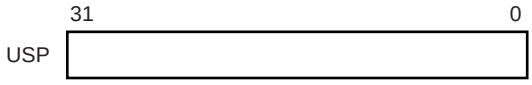
When the S flag is “0,” this register functions as the R15 register.

The SSP register can also be explicitly specified.

This register is also used as a stack pointer to indicate the stack to which the PS and PC are removed when an EIT occurs.

The default value at reset is 00000000_H.

- USP (User Stack Pointer)



[Default value]
$XXXXXXXX_H$

USP Register

The USP register is the user stack pointer.

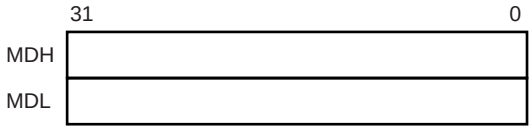
When the S flag is “1,” this register functions as the R15 register.

The USP register can also be explicitly specified.

The default value at reset is undefined.

This register cannot be used with RETI instructions.

- Multiply & Divide registers



Multiply & Divide Registers

The multiply and divide registers are each 32 bits in length.

The default value at reset is undefined.

■ SETTING MODE

In the FR family, the mode pins (MD2, MD1, MD0) and the mode register (MODR) are used to set the operating mode.

1. Mode Pins

The three pins MD2, MD1, MD0 are used in mode vector fetch instructions, and also to make settings in test mode.

Mode pin			Mode name	Reset vector access area	Remarks
MD2	MD1	MD0			
0	0	1	External ROM mode vector	Outside	Bus width is set by mode register.

2. Mode Register (MODR)

The mode data fetch instruction writes data to the address “0000 07FD$_H$” called the mode data.

The area “0000 07FD$_H$” is the mode register (MODR). When a setting is made to this register, the device will operate the mode corresponding to that setting.

The mode register can only be set by a reset source at the INIT level. It is not possible to write to this register from a user program.

Note : No data exists at the FR family mode register address (0000 07FF$_H$).

< Detailed register description >

MODR Address 0000 07FD$_H$

7	6	5	4	3	2	1	0
0	0	0	0	0	ROMA	WTH1	WTH0
					← Operating mode setting bits →		

Default: XXXXXXXX$_B$

[bit7 to bit3] Reserved bits

These bits should always be set to “00000.” If set to any other value, stable operation is not assured.

[bit2] ROMA (Internal RAM enable bit)

This bit indicates whether internal RAM is enabled.

ROMA	Function	Remarks
0	External ROM mode	The built-in RAM area functions as external area.
1	Internal RAM mode	The built-in RAM area is enabled. The 128K bytes built-in RAM can be used.

[bit1, 0] WTH1, WTH0 (Bus width indicator bits)

In external bus mode, these bits determine the bus width setting.

In external bus mode, the value of these bits sets the BW1, 0 bits in the AMD0 register (CS0 area).

WTH1	WTH0	Bus width
0	0	8-bit
0	1	16-bit
1	0	Setting prohibited
1	1	Setting prohibited

■ MEMORY SPACE

1. Memory Space

The FR family has 4G bytes (2^{32} addresses) of logical address space with linear access from the CPU.

•Direct Addressing Areas

The following areas of address space are used for I/O operations.

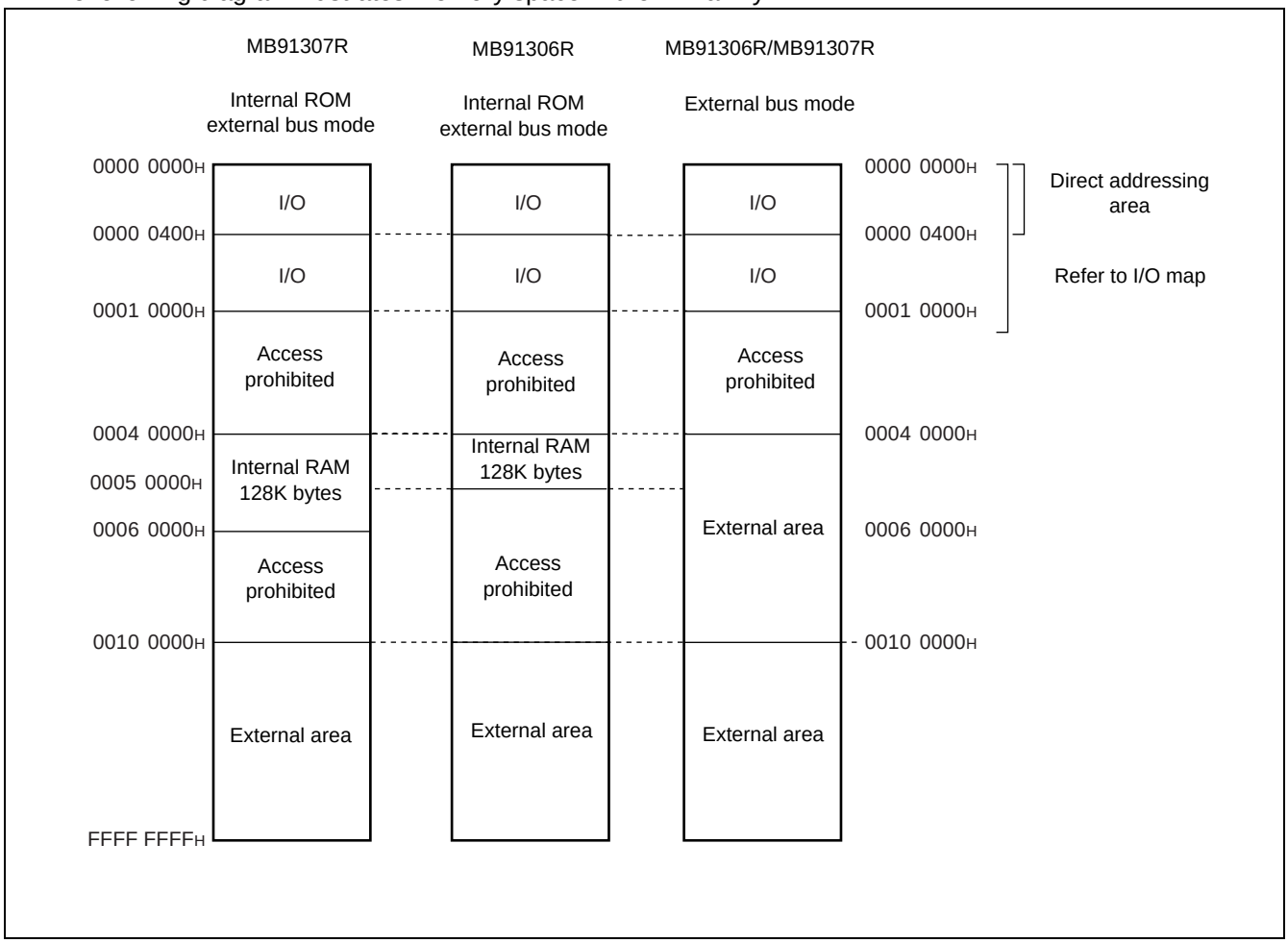
These areas are called direct addressing areas, in which the address of an operand can be specified directly during an instruction.

The direct areas differ according to the size of the data accessed, as follows.

→ byte data access : 000_H to $0FF_H$
→ half word data access : 000_H to $1FF_H$
→ word data access : 000_H to $3FF_H$

2. Memory Map

The following diagram illustrates memory space in the FR family.

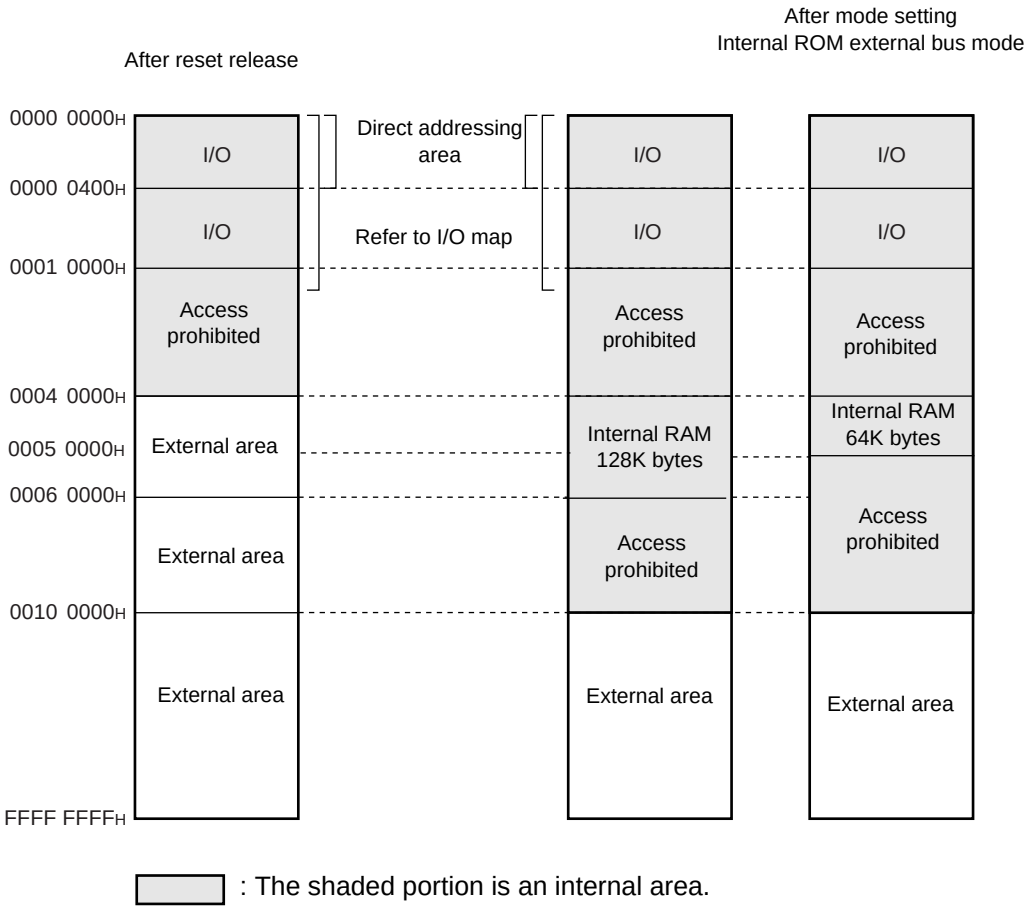


•Use of Built-in RAM

The MB91307R contains 128K bytes of internal RAM, and MB91306R contains 64K bytes of internal RAM. To enable use of this RAM, the mode register must be set to internal ROM external bus mode (ROMA=1).

Precautions for use of this model

- The reset vector is fixed at 000F FFFC$_H$.
- For the MB91307R, the 128K bytes RAM area is from 0004 0000$_H$ to 0005 FFFF$_H$ and for the MB91306R, the 64K bytes RAM area is from 0004 0000$_H$ to 0004 FFFF$_H$. The area from 0006 0000$_H$ to 000F FFFF$_H$ is access prohibited.
- In order to use RAM the mode register must be set to internal ROM external bus mode.
- In internal ROM external bus mode the built-in RAM area can be used, but the vector area 000F FFXX$_H$ is an internal area and cannot be accessed externally. Please refer to the following explanation.
- When placing instruction code in RAM, nothing should be placed in the last 8 bytes of the area 0005 FFF8$_H$ to 0005 FFFF$_H$. (This is an instruction code prohibited area.)

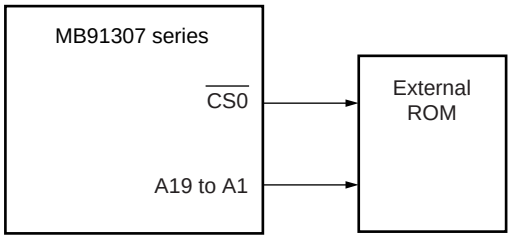


After mode register setting the vector area is an internal area. Therefore before writing to the mode register it is necessary to rewrite the TBR register so that the vector area is changed to an external area.

■ USER PROGRAM INITIALIZATION

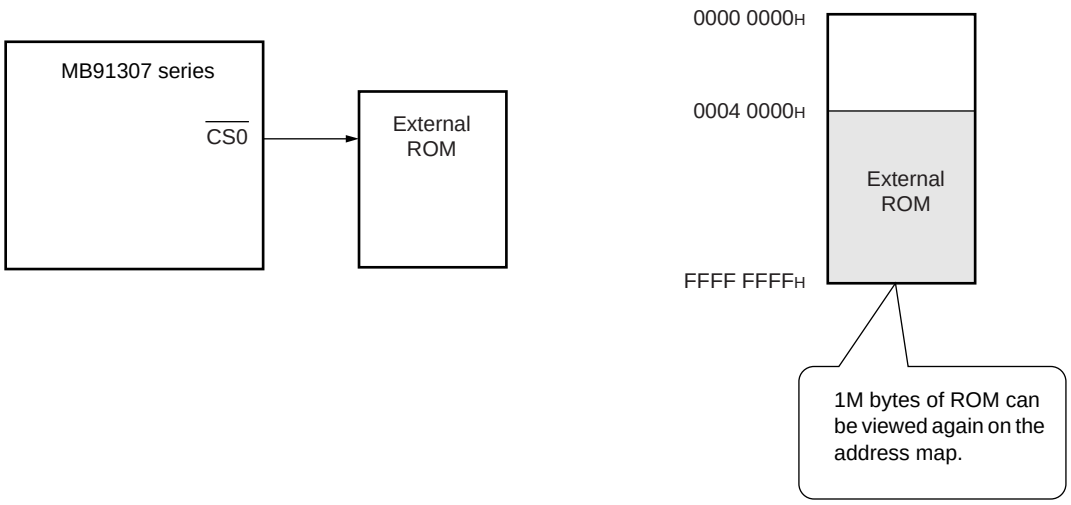
The following sequence describes an example using built-in RAM.
For the MB91306R, only the internal RAM area is different but the setting is same.

1. Hardware Setting Conditions



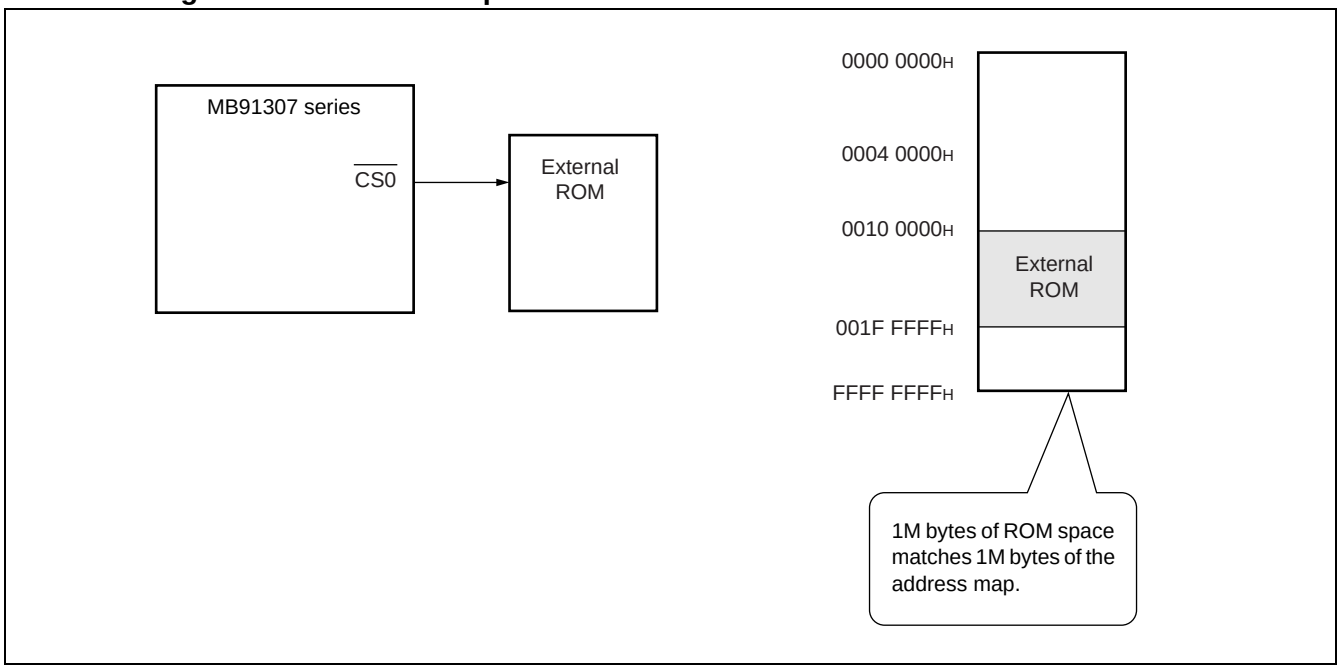
1) Assume that 1M bytes of external ROM is placed beginning at 0010 0000H. Place the program at this location in the linker. (The following description can apply to other addresses than this one as well.)
2) Connect addresses A19 to A1 (1M bytes) to ROM, other addresses will use $\overline{CS0}$.
3) Set the mode pins (MD2, MD1, MD0) to external vectors.
4) Write the reset vector to 001F FFFCH. Likewise write the mode vector to 001F FFF8H.

2. Immediately After Reset Release



1) After reset release, the CPU will attempt to load a mode vector from 000F FFF8H, a reset vector from 000F FFFCH, however because this will be an external vector, the CPU will have to go externally. However the $\overline{CS0}$ default value causes 1M bytes of external ROM to be repeated in external space, so that the mode vector and the reset vector itself will load the contents written at 001F FFF8H and 001F FFFCH in external ROM.
2) The branch destination is set in the linker to an address in the area 001X XXXXH, so that subsequent program execution will be in this area.

3. User Program Initialization Steps



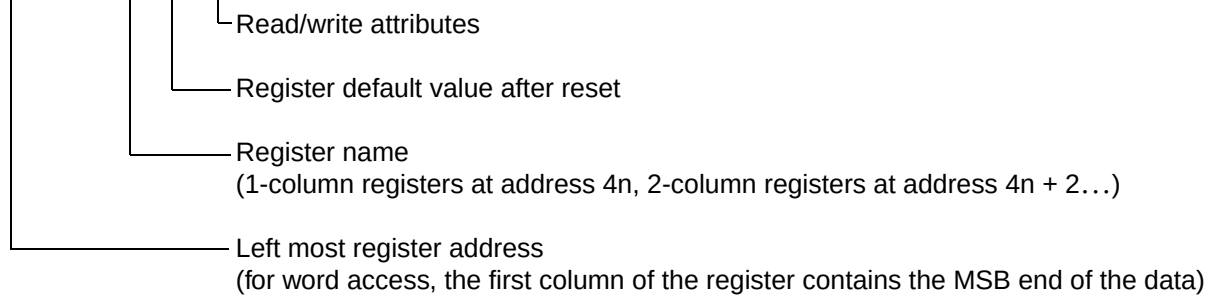
1) Set the TBR register so that the interrupt table is 001F FFXXH, then perform initialization. This process also includes a chip select setting, and at the same time the $\overline{CS0}$ address is set to be valid at 001X XXXXH. The $\overline{CS0}$ decoding result is the same before and after the setting, so that the CPU can continue to run programs on external ROM.
2) If necessary, initialize the contents of RAM.
3) Now initialization is complete, and the application program can be executed.

■ I/O MAP

This map shows the correlation between areas of memory space and individual registers in peripheral resources.

[How to read the map]

Address	Register				Block
	+0	+1	+2	+3	
000000_H	PDR0 [R/W] XXXXXXXX	PDR1 [R/W] XXXXXXXX	PDR2 [R/W] XXXXXXXX	PDR3 [R/W] XXXXXXXX	T-unit Port Data Register



Note: Default register bit values are indicated as follows:

- “1” : Default value “1”
- “0” : Default value “0”
- “X” : Default value “X”
- “-“ : No physical register at this location

Address	Register				Block
	+0	+1	+2	+3	
000000H	—	—	PDR2 [R/W] XXXXXXXX	—	T-unit Port Data Register
000004H	—	—	PDR6 [R/W] XXXXXXXX	PDR7 [R/W] -------X	
000008H	PDR8 [R/W] --X--XXX	PDR9 [R/W] XXXXXXX-	PDRA [R/W] XXXXXXXX	PDRB [R/W] XXXXXXXX	
00000CH	—				
000010H	PDRG [R/W] -----XXX	PDRH [R/W] XXX00XXX	PDRI [R/W] ---XXXXX	PDRJ [R/W] XXXXXXXX	R-bus Port Data Register
000018H to 00001CH	—				
000020H to 00003CH	—				Reserved
000040H	EIRR [R/W] 00000000	ENIR [R/W] 00000000	ELVR [R/W] 00000000		Ext int
000044H	DICR [R/W] -------0	HRCL [R/W] 0--11111	—		DLYI/I-unit
000048H	TMRLR [W] XXXXXXXX XXXXXXXX		TMR [R] XXXXXXXX XXXXXXXX		Reload Timer 0
00004CH	—		TMCSR [R/W] ----0000 00000000		
000050H	TMRLR [W] XXXXXXXX XXXXXXXX		TMR [R] XXXXXXXX XXXXXXXX		Reload Timer 1
000054H	—		TMCSR [R/W] ----0000 00000000		
000058H	TMRLR [W] XXXXXXXX XXXXXXXX		TMR [R] XXXXXXXX XXXXXXXX		Reload Timer 2
00005CH	—		TMCSR [R/W] ----0000 00000000		
000060H	SSR [R/W] 00001-00	SIDR [R/W] XXXXXXXX	SCR [R/W] 00000100	SMR [R/W] 00--0-0-	UART0
000064H	UTIM [R] 00000000	(UTIMR [W]) 00000000	DRCL [W] --------	UTIMC [R/W] 0--00001	U-TIMER 0
000068H	SSR [R/W] 00001-00	SIDR [R/W] XXXXXXXX	SCR [R/W] 00000100	SMR [R/W] 00--0-0-	UART1

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
00006CH	UTIM [R] 00000000	(UTIMR [W]) 00000000	DRCL [W] --------	UTIMC [R/W] 0--00001	U-TIMER 1
000070H	SSR [R/W] 00001-00	SIDR [R/W] XXXXXXXX	SCR [R/W] 00000100	SMR [R/W] 00--0-0-	UART2
000074H	UTIM [R] 00000000	(UTIMR [W]) 00000000	DRCL [W] --------	UTIMC [R/W] 0--00001	U-TIMER 2
000078H	ADCR [R] ------XX	XXXXXXXX	ADCS [R/W] 00000000	00000000	A/D Converter sequential comparator
00007CH	—				Reserved
000080H	—				Reserved
000084H	—				Reserved
000088H	—				Reserved
00008CH	—				Reserved
000090H	—				Reserved
000094H	IBCR [R/W] 00000000	IBSR [R/W] 00000000	ITBA [R/W] ------00	00000000	I²C interface
000098H	ITMK [R/W] 00----11	11111111	ISMK [R/W] 01111111	ISBA [R/W] 00000000	
00009CH	—	IDAR [R/W] 00000000	ICCR [R/W] 0-011111	IDBL [R/W] -------0	
0000A0H	—				Reserved
0000A4H	—				Reserved
0000A8H	—				Reserved
0000ACH	—				Reserved
0000B0H	—				Reserved

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000200H	DMACA0 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000204H	DMACB4 [R/W] 00000000 00000000 00000000 00000000				
000208H	DMACA1 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00020CH	DMACB4 [R/W] 00000000 00000000 00000000 00000000				
000210H	DMACA2 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000214H	DMACB4 [R/W] 00000000 00000000 00000000 00000000				
000218H	DMACA3 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00021CH	DMACB4 [R/W] 00000000 00000000 00000000 00000000				
000220H	DMACA4 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000224H	DMACB4 [R/W] 00000000 00000000 00000000 00000000				
000228H	—				
00022CH to 00023CH	—				Reserved
000240H	DMACR [R/W] 0XX00000 XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
000244H to 000274H	—				Reserved
000278H	—				Reserved
00027CH	—				Reserved
000280H to 0002FCH	—				Reserved

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000300H	—				Reserved
000304H	—			ISIZE [R/W] ------00	Instruction Cache
000308H to 0003E0H	—				Reserved
0003E4H	—			ICHRC [R/W] 0 - 000000	Instruction Cache
0003E8H to 0003ECH	—				Reserved
0003F0H	BSD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit Search Module
0003F4H	BSD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003F8H	BSDC [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003FCH	BSRR [R] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000400H	DDRG [R/W] ----000	DDRH [R/W] 00011000	DDRI [R/W] --000000	DDRJ [R/W] 00000000	R-bus Port Direction Register
000404H	—				
000408H	—				
00040CH	—				
000410H	PFRG [R/W] ----0000	PFRH [R/W] 0000000-	PFRI [R/W] --00-00-	—	R-bus Port Function Register
000414H	—				
000418H	—				
00041CH	—				
000420H to 00043CH	—				Reserved

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000440H	ICR00 [R/W] ---11111	ICR01 [R/W] ---11111	ICR02 [R/W] ---11111	ICR03 [R/W] ---11111	Interrupt Control unit
000444H	ICR04 [R/W] ---11111	ICR05 [R/W] ---11111	ICR06 [R/W] ---11111	ICR07 [R/W] ---11111	
000448H	ICR08 [R/W] ---11111	ICR09 [R/W] ---11111	ICR10 [R/W] ---11111	ICR11 [R/W] ---11111	
00044CH	ICR12 [R/W] ---11111	ICR13 [R/W] ---11111	ICR14 [R/W] ---11111	ICR15 [R/W] ---11111	
000450H	ICR16 [R/W] ---11111	ICR17 [R/W] ---11111	ICR18 [R/W] ---11111	ICR19 [R/W] ---11111	Interrupt Control unit
000454H	ICR20 [R/W] ---11111	ICR21 [R/W] ---11111	ICR22 [R/W] ---11111	ICR23 [R/W] ---11111	
000458H	ICR24 [R/W] ---11111	ICR25 [R/W] ---11111	ICR26 [R/W] ---11111	ICR27 [R/W] ---11111	
00045CH	ICR28 [R/W] ---11111	ICR29 [R/W] ---11111	ICR30 [R/W] ---11111	ICR31 [R/W] ---11111	
000460H	ICR32 [R/W] ---11111	ICR33 [R/W] ---11111	ICR34 [R/W] ---11111	ICR35 [R/W] ---11111	
000464H	ICR36 [R/W] ---11111	ICR37 [R/W] ---11111	ICR38 [R/W] ---11111	ICR39 [R/W] ---11111	
000468H	ICR40 [R/W] ---11111	ICR41 [R/W] ---11111	ICR42 [R/W] ---11111	ICR43 [R/W] ---11111	
00046CH	ICR44 [R/W] ---11111	ICR45 [R/W] ---11111	ICR46 [R/W] ---11111	ICR47 [R/W] ---11111	
000470H to 00047CH	—				—
000480H	RSRR [R/W] 10000000 *2	STCR [R/W] 00110011 *2	TBCR [R/W] 00XXXX00 *1	CTBR [W] XXXXXXXX	Clock Control unit
000484H	CLKR [R/W] 00000000 *1	WPR [W] XXXXXXXX	DIVR0 [R/W] 00000011 *1	DIVR1 [R/W] 00000000 *1	
000488H to 0005FCH	—				Reserved

*1: These registers have different default values at reset level. The value shown is the INIT level value.

*2: These registers have different default values at reset level. The value shown is the INIT level value from the $\overline{\text{INIT}}$ pin.

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000600H	—	—	DDR2 [R/W] 00000000	—	T-unit Port Direction Register
000604H	—	—	DDR6 [R/W] 00000000	DDR7 [R/W] 00000000	
000608H	DDR8 [R/W] --0--000	DDR9 [R/W] 00000000	DDRA [R/W] 00000000	DDRB [R/W] 00000000	
00060CH	—				
000610H	—	—	—	—	T-unit Port Function Register
000614H	—	—	PFR6 [R/W] 11111111	PFR7 [R/W] -------1	
000618H	PFR8 [R/W] --1--0--	PFR9 [R/W] 1111111-	PFRA [R/W] 0-001101	PFRB1 [R/W] 00000000	
00061CH	PFRB2 [R/W] 00------	—			
000620H	—				
000624H	—				
000628H to 00063FH	—				Reserved
000640H	ASR0 [R/W] 00000000 00000000		ACR0 [R/W] 1111XX00 00000000		T-unit
000644H	ASR1 [R/W] XXXXXXXX XXXXXXXX		ACR1 [R/W] XXXXXXXX XXXXXXXX		
000648H	ASR2 [R/W] XXXXXXXX XXXXXXXX		ACR2 [R/W] XXXXXXXX XXXXXXXX		
00064CH	ASR3 [R/W] XXXXXXXX XXXXXXXX		ACR3 [R/W] XXXXXXXX XXXXXXXX		
000650H	ASR4 [R/W] XXXXXXXX XXXXXXXX		ACR4 [R/W] XXXXXXXX XXXXXXXX		
000654H	ASR5 [R/W] XXXXXXXX XXXXXXXX		ACR5 [R/W] XXXXXXXX XXXXXXXX		

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000658H	ASR6 [R/W] XXXXXXXX XXXXXXXX		ACR6 [R/W] XXXXXXXX XXXXXXXX		T-unit
00065CH	ASR7 [R/W] XXXXXXXX XXXXXXXX		ACR7 [R/W] XXXXXXXX XXXXXXXX		
000660H	AWR0 [R/W] 011111111 11111111		AWR1 [R/W] XXXXXXXX XXXXXXXX		
000664H	AWR2 [R/W] XXXXXXXX XXXXXXXX		AWR3 [R/W] XXXXXXXX XXXXXXXX		
000668H	AWR4 [R/W] XXXXXXXX XXXXXXXX		AWR5 [R/W] XXXXXXXX XXXXXXXX		
00066CH	AWR6 [R/W] XXXXXXXX XXXXXXXX		AWR7 [R/W] XXXXXXXX XXXXXXXX		
000670H	—				
000674H	—				
000678H	IOWR0 [R/W] XXXXXXXX	IOWR1 [R/W] XXXXXXXX	IOWR2 [R/W] XXXXXXXX	—	
00067CH	—				
000680H	CSER [R/W] 000000001	CHER [R/W] 11111111	—	TCR [R/W] 00000000	
000684H	—				
000684H to 0007F8H	—				Reserved
0007FCH	—				—
000800H to 000AFCH	—				Reserved
000B00H	ESTS0 [R/W] X0000000	ESTS1 [R/W] XXXXXXXX	ESTS2 [R] 1XXXXXXX	—	DSU
000B04H	ECTL0 [R/W] 0X000000	ECTL1 [R/W] 00000000	ECTL2 [W] 000X0000	ECTL3 [R/W] 00X00X11	

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000B08H	ECNT0 [W] XXXXXXXX	ECNT1 [W] XXXXXXXX	EUSA [W] XXX00000	EDTC [W] 0000XXXX	DSU
000B0CH	EWPT [R] 00000000 00000000		—		
000B10H	EDTR0 [W] XXXXXXXX XXXXXXXX		EDTR1 [W] XXXXXXXX XXXXXXXX		
000B14H to 000B1CH	—				
000B20H	EIA0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B24H	EIA1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B28H	EIA2 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B2CH	EIA3 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B30H	EIA4 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B34H	EIA5 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B38H	EIA6 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B3CH	EIA7 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B40H	EDTA [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B44H	EDTM [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B48H	EOA0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B4CH	EOA1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B50H	EPCR [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

(Continued)

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000B54H	EPSR [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DSU
000B58H	EIAM0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B5CH	EIAM1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B60H	EOAM0/EODM0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B64H	EOAM1/EODM1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B68H	EOD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B6CH	EOD1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B70H to 000FFCH	—				Reserved
001000H	DMASA0 [R/W] XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				DMAC
001004H	DMADA0 [R/W] XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
001008H	DMASA1 [R/W] XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
00100CH	DMADA1 [R/W] XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
001010H	DMASA2 [R/W] XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
001014H	DMADA2 [R/W] XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
001018H	DMASA3 [R/W] XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
00101CH	DMADA3 [R/W] XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
001020H	DMASA4 [R/W] XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
001024H	DMADA4 [R/W] XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				DMAC

■ INTERRUPT SOURCES AND INTERRUPT VECTORS

Interrupt source	Interrupt number		Interrupt level	Offset	TBR default address
	Decimal	Hex			
Reset	0	00	—	3FC$_H$	000FFFFC$_H$
Mode vector	1	01	—	3F8$_H$	000FFFF8$_H$
System reserved	2	02	—	3F4$_H$	000FFFF4$_H$
System reserved	3	03	—	3F0$_H$	000FFFF0$_H$
System reserved	4	04	—	3EC$_H$	000FFFEC$_H$
System reserved	5	05	—	3E8$_H$	000FFFE8$_H$
System reserved	6	06	—	3E4$_H$	000FFFE4$_H$
Coprocessor absent trap	7	07	—	3E0$_H$	000FFFE0$_H$
Coprocessor error trap	8	08	—	3DC$_H$	000FFFDC$_H$
INTE instruction	9	09	—	3D8$_H$	000FFFD8$_H$
Instruction break exception	10	0A	—	3D4$_H$	000FFFD4$_H$
Operand break trap	11	0B	—	3D0$_H$	000FFFD0$_H$
Step trace trap	12	0C	—	3CC$_H$	000FFFCC$_H$
NMI request (tool)	13	0D	—	3C8$_H$	000FFFC8$_H$
Undefined instruction exception	14	0E	—	3C4$_H$	000FFFC4$_H$
NMI requ	15	0F	15 (F$_H$)	3C0$_H$	000FFFC0$_H$
External interrupt 0	16	10	ICR00	3BC$_H$	000FFFBC$_H$
External interrupt 1	17	11	ICR01	3B8$_H$	000FFFB8$_H$
External interrupt 2	18	12	ICR02	3B4$_H$	000FFFB4$_H$
External interrupt 3	19	13	ICR03	3B0$_H$	000FFFB0$_H$
External interrupt 4	20	14	ICR04	3AC$_H$	000FFFAC$_H$
External interrupt 5	21	15	ICR05	3A8$_H$	000FFFA8$_H$
External interrupt 6	22	16	ICR06	3A4$_H$	000FFFA4$_H$
External interrupt 7	23	17	ICR07	3A0$_H$	000FFFA0$_H$
Reload timer 0	24	18	ICR08	39C$_H$	000FFF9C$_H$
Reload timer 1	25	19	ICR09	398$_H$	000FFF98$_H$
Reload timer 2	26	1A	ICR10	394$_H$	000FFF94$_H$
UART0(RX completed)	27	1B	ICR11	390$_H$	000FFF90$_H$
UART1(RX completed)	28	1C	ICR12	38C$_H$	000FFF8C$_H$
UART2(RX completed)	29	1D	ICR13	388$_H$	000FFF88$_H$
UART0(TX completed)	30	1E	ICR14	384$_H$	000FFF84$_H$
UART1(TX completed)	31	1F	ICR15	380$_H$	000FFF80$_H$
UART2(TX completed)	32	20	ICR16	37C$_H$	000FFF7C$_H$
DMAC0(end, error)	33	21	ICR17	378$_H$	000FFF78$_H$

(Continued)

Interrupt source	Interrupt number		Interrupt level	Offset	TBR default address
	Decimal	Hex			
DMAC1(end, error)	34	22	ICR18	374H	000FFF74H
DMAC2(end, error)	35	23	ICR19	370H	000FFF70H
DMAC3(end, error)	36	24	ICR20	36CH	000FFF6CH
DMAC4(end, error)	37	25	ICR21	368H	000FFF68H
A/D	38	26	ICR22	364H	000FFF64H
I^2C	39	27	ICR23	360H	000FFF60H
System reserved	40	28	ICR24	35CH	000FFF5CH
System reserved	41	29	ICR25	358H	000FFF58H
System reserved	42	2A	ICR26	354H	000FFF54H
System reserved	43	2B	ICR27	350H	000FFF50H
U-TIMER0	44	2C	ICR28	34CH	000FFF4CH
U-TIMER1	45	2D	ICR29	348H	000FFF48H
U-TIMER2	46	2E	ICR30	344H	000FFF44H
Time base timer overflow	47	2F	ICR31	340H	000FFF40H
System reserved	48	30	ICR32	33CH	000FFF3CH
System reserved	49	31	ICR33	338H	000FFF38H
System reserved	50	32	ICR34	334H	000FFF34H
System reserved	51	33	ICR35	330H	000FFF30H
System reserved	52	34	ICR36	32CH	000FFF2CH
System reserved	53	35	ICR37	328H	000FFF28H
System reserved	54	36	ICR38	324H	000FFF24H
System reserved	55	37	ICR39	320H	000FFF20H
System reserved	56	38	ICR40	31CH	000FFF1CH
System reserved	57	39	ICR41	318H	000FFF18H
System reserved	58	3A	ICR42	314H	000FFF14H
System reserved	59	3B	ICR43	310H	000FFF10H
System reserved	60	3C	ICR44	30CH	000FFF0CH
System reserved	61	3D	ICR45	308H	000FFF08H
System reserved	62	3E	ICR46	304H	000FFF04H
Delay interrupt source bit	63	3F	ICR47	300H	000FFF00H
System reserved (REALOS use)	64	40	—	2FCH	000FFEFCH
System reserved (REALOS use)	65	41	—	2F8H	000FFEF8H
System reserved	66	42	—	2F4H	000FFEF4H
System reserved	67	43	—	2F0H	000FFEF0H
System reserved	68	44	—	2ECH	000FFEECH

(Continued)

(Continued)

Interrupt source	Interrupt number		Interrupt level	Offset	TBR default address
	Decimal	Hex			
System reserved	69	45	—	$2E8_H$	$000FFEE8_H$
System reserved	70	46	—	$2E4_H$	$000FFEE4_H$
System reserved	71	47	—	$2E0_H$	$000FFEE0_H$
System reserved	72	48	—	$2DC_H$	$000FFEDC_H$
System reserved	73	49	—	$2D8_H$	$000FFED8_H$
System reserved	74	4A	—	$2D4_H$	$000FFED4_H$
System reserved	75	4B	—	$2D0_H$	$000FFED0_H$
System reserved	76	4C	—	$2CC_H$	$000FFECC_H$
System reserved	77	4D	—	$2C8_H$	$000FFEC8_H$
System reserved	78	4E	—	$2C4_H$	$000FFEC4_H$
System reserved	79	4F	—	$2C0_H$	$000FFEC0_H$
Used by INT instructions	80 to 255	50 to FF	—	$2BC_H$ to 000_H	$000FFEBC_H$ to $000FFC00_H$

■ PERIPHERAL RESOURCES

1. Interrupt Controller

(1) Overview

The interrupt controller receives and processes arbitration of interrupts.

•Hardware Configuration

This module is configured from the following elements.

- ICR register
- Interrupt priority determination circuit
- Interrupt level and interrupt number (vector) generator
- Hold request removal request generator

•Principal Functions

This module primarily provides the following functions.

- NMI request / interrupt request detection
- Order of priority determination (according to level and number)
- Notification (to CPU) of interrupt level of source according to determination
- Notification (to CPU) of interrupt number of source according to determination
- Instruction (to CPU) to recover from stop mode when an interrupt other than NMI/interrupt level “11111” is generated
- Generation of hold request removal requests to the bus master

(2) Register List

	bit 7	6	5	4	3	2	1	0	
Address : 00000440H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR00
Address : 00000441H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR01
Address : 00000442H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR02
Address : 00000443H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR03
Address : 00000444H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR04
Address : 00000445H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR05
Address : 00000446H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR06
Address : 00000447H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR07
Address : 00000448H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR08
Address : 00000449H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR09
Address : 0000044AH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR10
Address : 0000044BH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR11
Address : 0000044CH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR12
Address : 0000044DH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR13
Address : 0000044EH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR14
Address : 0000044FH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR15
Address : 00000450H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR16
Address : 00000451H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR17
Address : 00000452H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR18
Address : 00000453H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR19
Address : 00000454H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR20
Address : 00000455H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR21
Address : 00000456H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR22
Address : 00000457H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR23
Address : 00000458H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR24
Address : 00000459H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR25
Address : 0000045AH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR26
Address : 0000045BH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR27
Address : 0000045CH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR28
Address : 0000045DH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR29
Address : 0000045EH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR30
Address : 0000045FH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR31
				R	R/W	R/W	R/W	R/W	

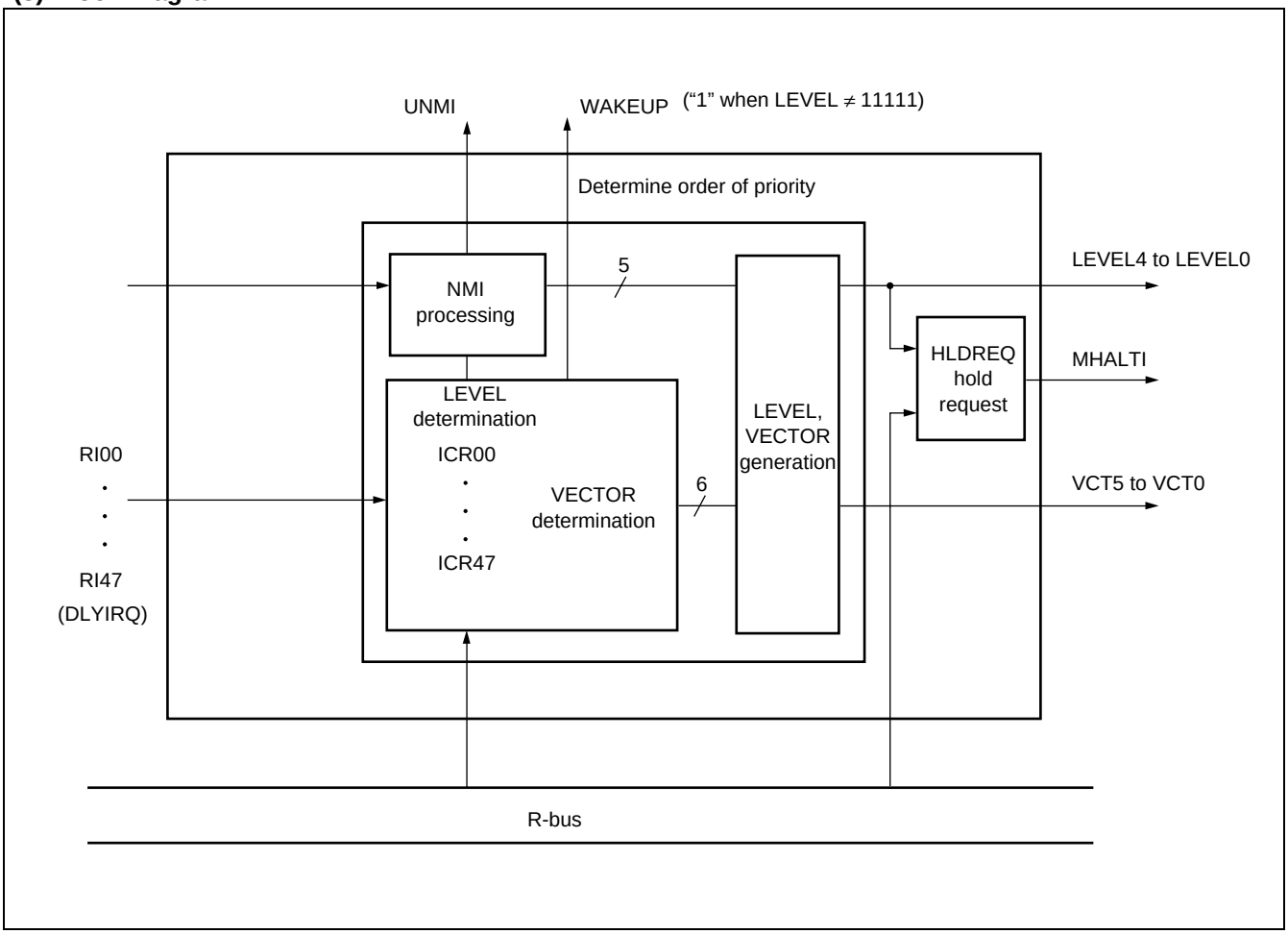
(Continued)

(Continued)

	bit 7	6	5	4	3	2	1	0	
Address : 00000460H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR32
Address : 00000461H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR33
Address : 00000462H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR34
Address : 00000463H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR35
Address : 00000464H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR36
Address : 00000465H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR37
Address : 00000466H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR38
Address : 00000467H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR39
Address : 00000468H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR40
Address : 00000469H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR41
Address : 0000046AH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR42
Address : 0000046BH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR43
Address : 0000046CH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR44
Address : 0000046DH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR45
Address : 0000046EH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR46
Address : 0000046FH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR47
				R	R/W	R/W	R/W	R/W	

Address : 00000045H	MHALTI	—	—	LVL4	LVL3	LVL2	LVL1	LVL0	HRCL
	R/W			R	R/W	R/W	R/W	R/W	

(3) Block Diagram



2. External Interrupt - NMI Control Block

(1) Overview

The External Interrupt-control block controls external interrupt requests input at the $\overline{\text{NMI}}$ and INT0 to INT7 pins.

The request level can be selected from “H,” “L,” “rising edge,” or “falling edge” detection (except for NMI).

(2) Register List

• External interrupt enable register (ENIR)

bit	7	6	5	4	3	2	1	0
	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0

• External interrupt source register (EIRR)

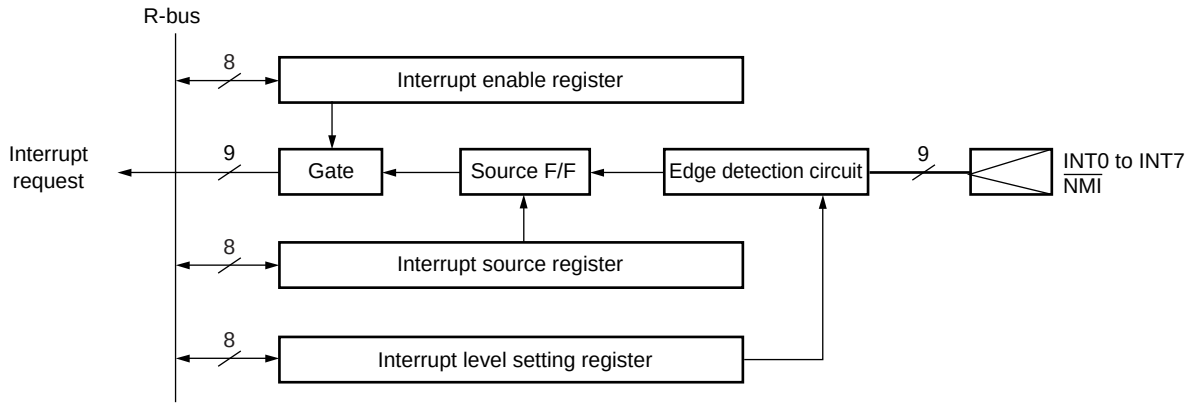
bit	15	14	13	12	11	10	9	8
	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0

• Request level setting register (ELVR)

bit	15	14	13	12	11	10	9	8
	LB7	LA7	LB6	LA6	LB5	LA5	LB4	LA4

bit	7	6	5	4	3	2	1	0
	LB3	LA3	LB2	LA2	LB1	LA1	LB0	LA0

(3) Block Diagram



3. REALOS Related Hardware

REALOS related hardware is used by the REALOS operating system. Therefore, when REALOS is in use, these resources cannot be used by user programs.

• Delay Interrupt Module

(1) Overview

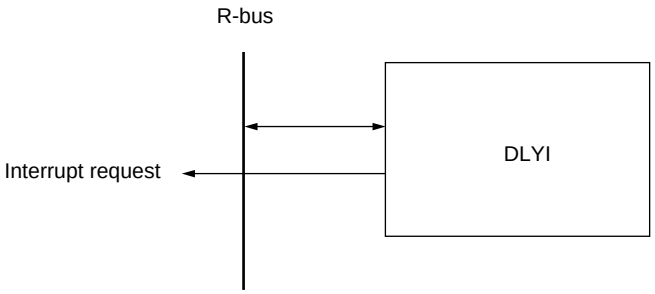
The delay interrupt module is a module that generates interrupts for task switching. This module can be used with software instructions to generate and cancel interrupts to the CPU.

(2) Register List

Address : 00000044H

bit	7	6	5	4	3	2	1	0	
	—	—	—	—	—	—	—	DLYI	DICR
								[R/W]	

(3) Block Diagram



• Bit Search Module

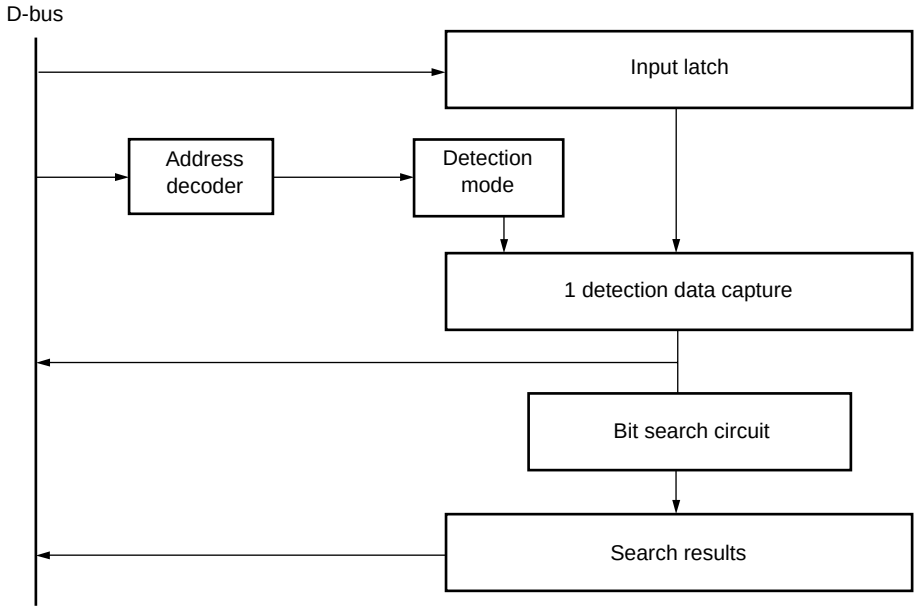
(1) Overview

Searches data written to input registers for “0” or “1” or change points, and outputs the value of the detected bits.

(2) Register List

		31 … 0	
Address :	000003F0H	BSD0	0 detection data register
Address :	000003F4H	BSD1	1 detection data register
Address :	000003F8H	BSDC	Change point detection register
Address :	000003FCH	BSRR	Detection results register

(3) Block Diagram



4. 16-bit Reload Timer

(1) Overview

The 16-bit timer is configured from a 16-bit down-counter, 16-bit reload register, prescaler for internal count clock generation, and a control register.

For the input clock signal, a selection of three internal clock signals (machine clock multiplied by 2, 8, or 32) or external clock is provided.

The output pin (TOUT) produces a toggle output waveform at every underflow in reload mode, and a square wave indicating counting in progress in one-shot mode.

The input pin (TIN) can be used for event input in external event count mode, and trigger input or gate input in internal clock mode.

The external event count function can be used in reload mode or as a frequency multiplier in external clock mode.

The MB91306R/MB91307R contain 3 channels (0 to 2) of this timer.

(2) Register List

• Control status register (TMCSR)

15	14	13	12	11	10	9	8
—	—	—	—	CSL1	CSL0	MOD2	MOD1

7	6	5	4	3	2	1	0
MOD0	—	OUTL	RELD	INTE	UF	CNTE	TRG

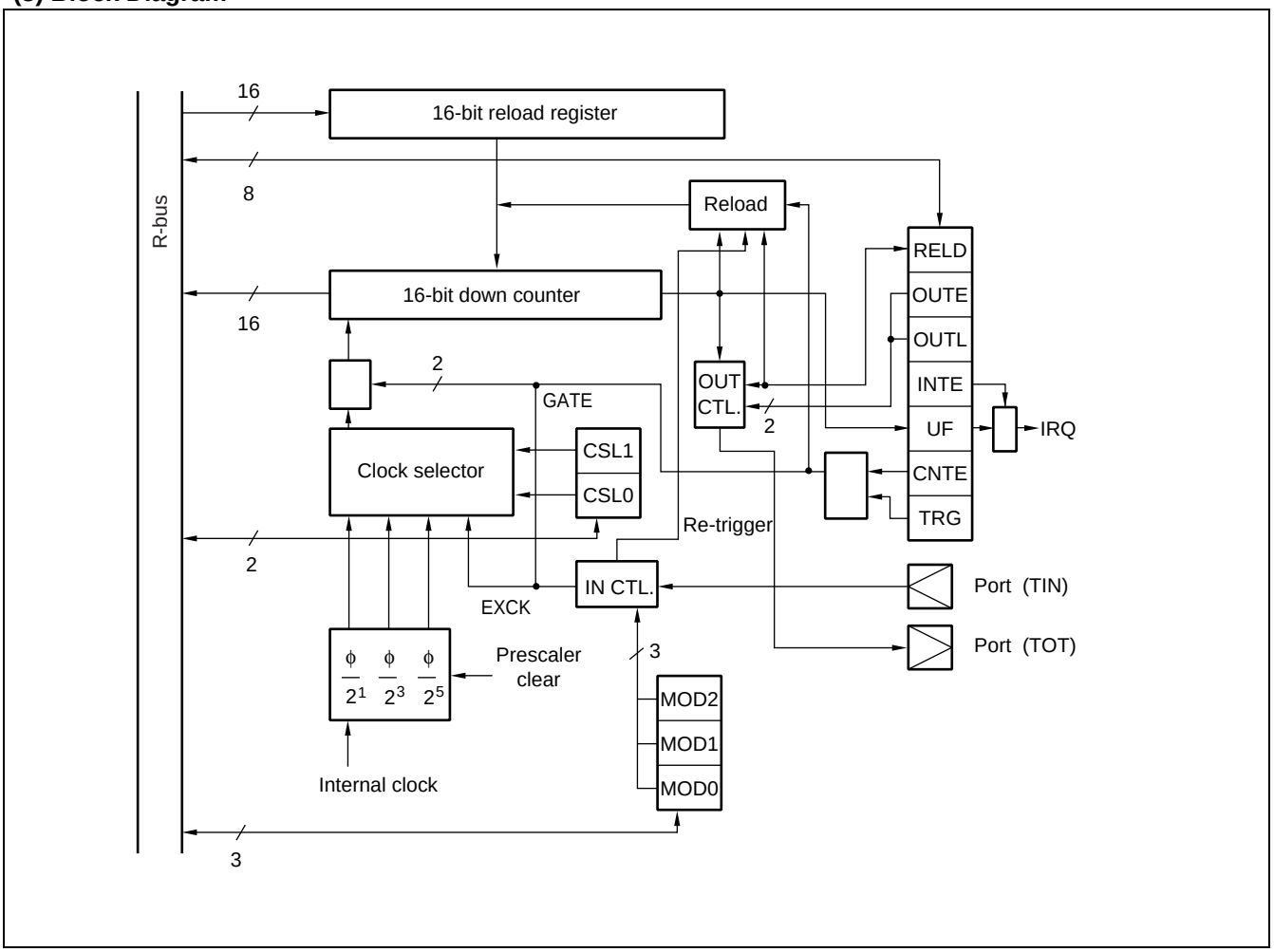
• 16-bit timer register (TMR)

15	0

• 16-bit reload register (TMRLR)

15	0

(3) Block Diagram



5. U-TIMER (16 bit timer for UART baud rate generation)

(1) Overview

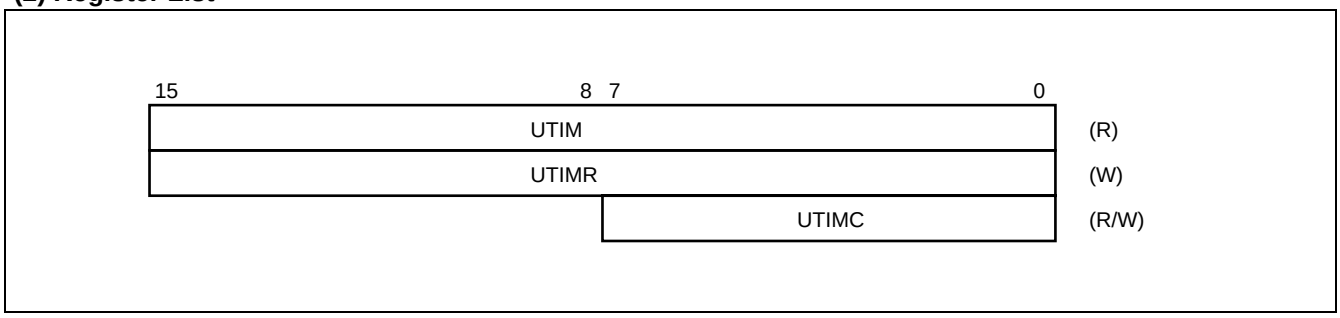
The U-TIMER is a 16-bit timer used to generate the baud rate for the UART. Any desired baud rate can be set using the combination of chip operating frequency and U-TIMER reload value.

The U-TIMER can also be used as an interval timer by generating an interrupt from a count underflow event.

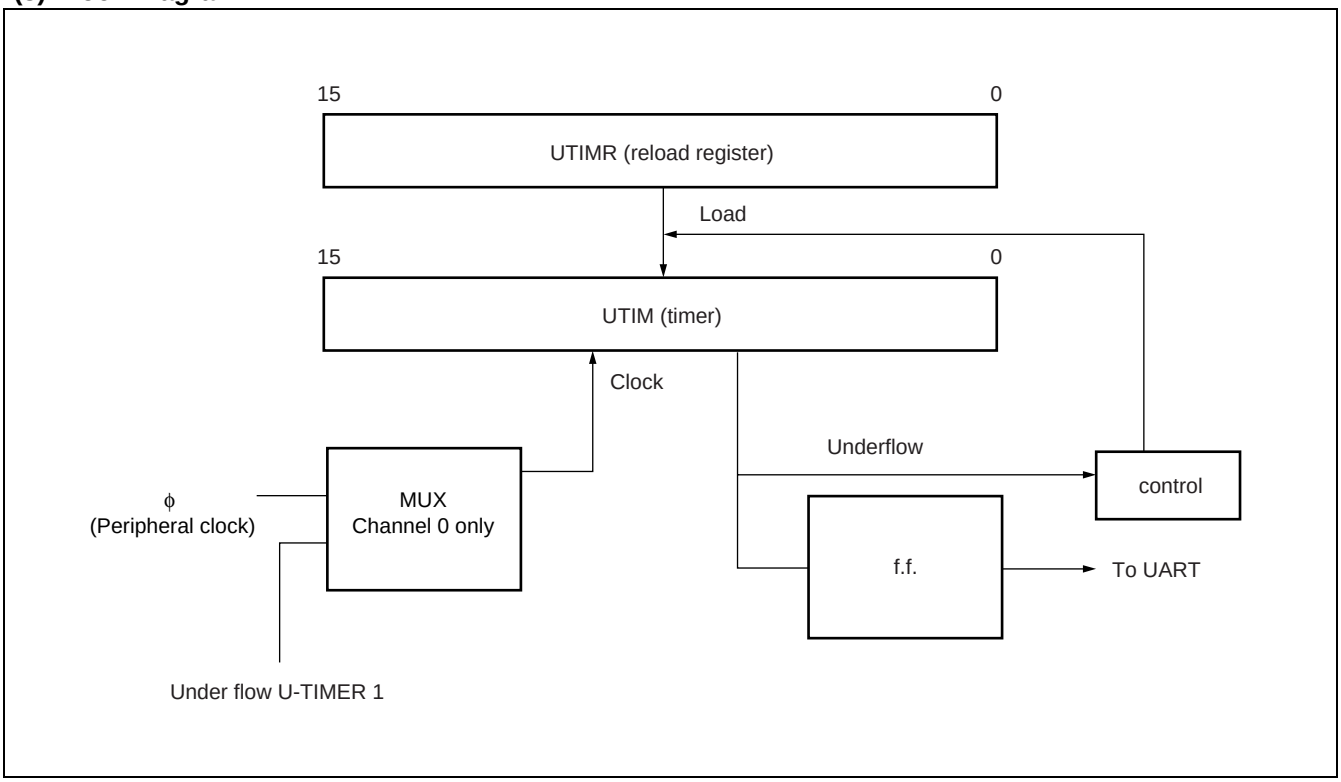
This device features a 3-channel built-in U-TIMER. By connecting two U-TIMER channels used as interval timers in a cascade connection, it is possible to count intervals up to a maximum of $2^{32} \times \phi$.

The available case connections are channel 0 to channel 1, and channel 1 to channel 2.

(2) Register List



(3) Block Diagram



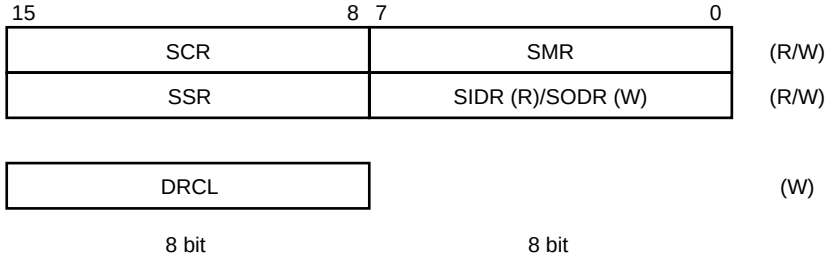
6. UART

(1) Overview

The UART is an I/O port for asynchronous (start-stop synchronized) or CLK synchronized transmission, providing the following features. This device features a 3-channel built-in UART.

- Full duplex double buffer
- Asynchronous (start-stop synchronized) or CLK synchronized transmission enabled
- Supports multi-processor mode
- Fully programmable baud rate
  Built-in timer can be set to any desired baud rate (see U-TIMER description)
- Independent baud rate setting from external clock enabled.
- Error detection functions (parity, framing, overrun)
- Transfer signal NRZ encoded
- DMA transfer start from interrupt enabled
- DMAC interrupt source cleared by write operation to DRCL register.

(2) Register List



• Serial input register/Serial output registe (SIDR/SODR)

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

• Serial status register (SSR)

7	6	5	4	3	2	1	0
PE	ORE	FRE	RDRF	TDRE	—	RIE	TIE

• Serial mode register (SMR)

7	6	5	4	3	2	1	0
MD1	MD0	—	—	CS0	—	SCKE	—

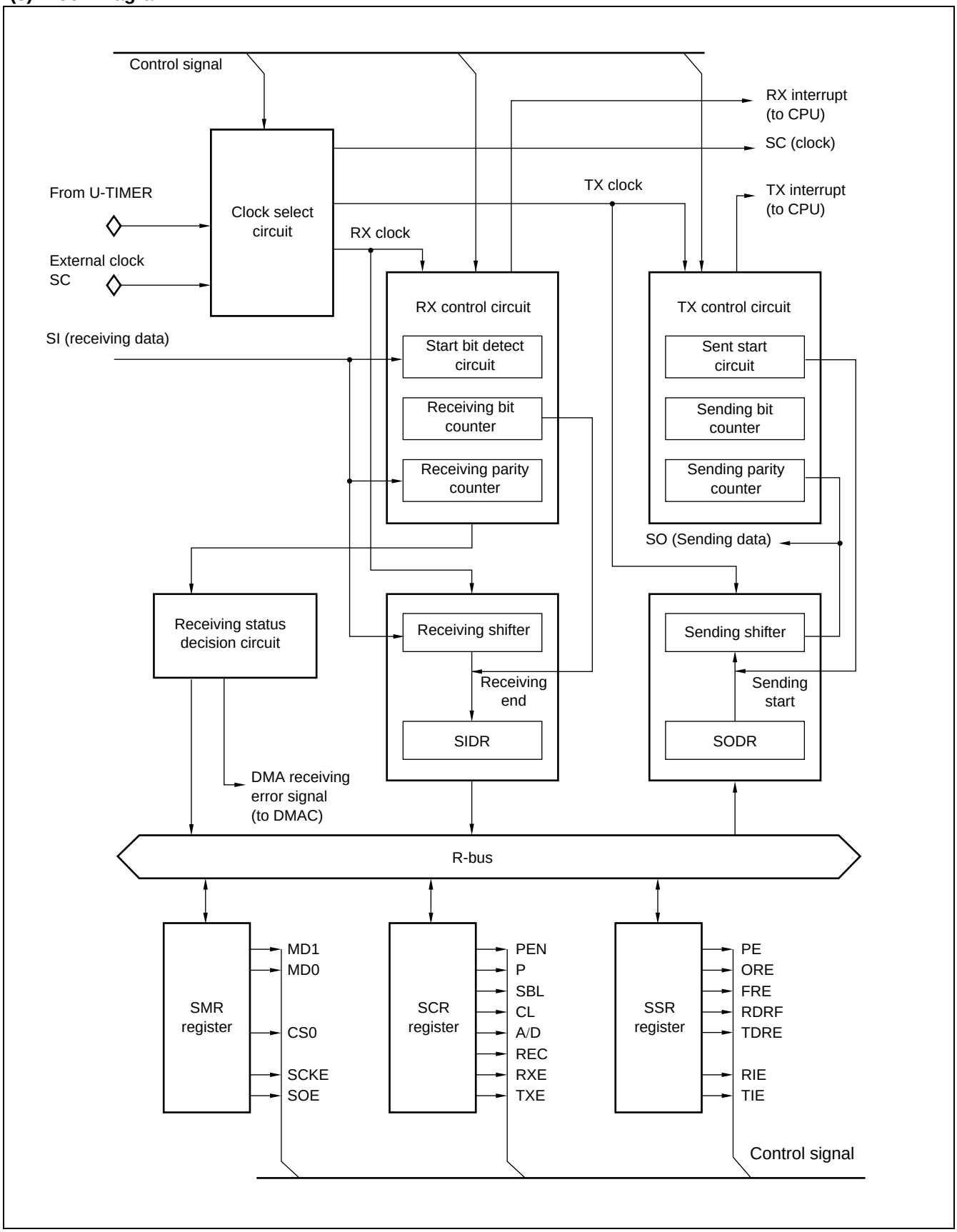
• Serial control register (SCR)

7	6	5	4	3	2	1	0
PEN	P	SBL	CL	A/D	REC	RXE	TXE

• DRCL register (DRCL)

7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	—

(3) Block Diagram



7. A/D Converter (Sequential comparison type)

(1) Overview

This A/D converter is a module that coverts analog input voltages to digital values, and provides the following features.

- Minimum conversion time 5.4 µs/ch (at machine clock 33 MHz-CKLP)
- Built-in sample & hold circuit
- Resolution 10 bits (8-bit accuracy)
- Analog input: 4 channels by program selection
  Single conversion mode: Conversion on 1 select channel
  Scan conversion mode: Select continuous multiple channels. Up to 4 channels can be selected by program.
  Continuous conversion mode: Continuous conversion on selected channel
  Stop conversion mode: 1-channel conversion then pause and wait until the next start is applied (enables synchronized conversion start)
- DMA transfer start from interrupt enabled
- Start sources can be selected from software, external trigger (falling edge), reload timer (rising edge).

(2) Register List

• Control status register (ADCS)

bit	15	14	13	12	11	10	9	8
	BUSY	INT	INTE	PAUS	STS1	STS0	STRT	—

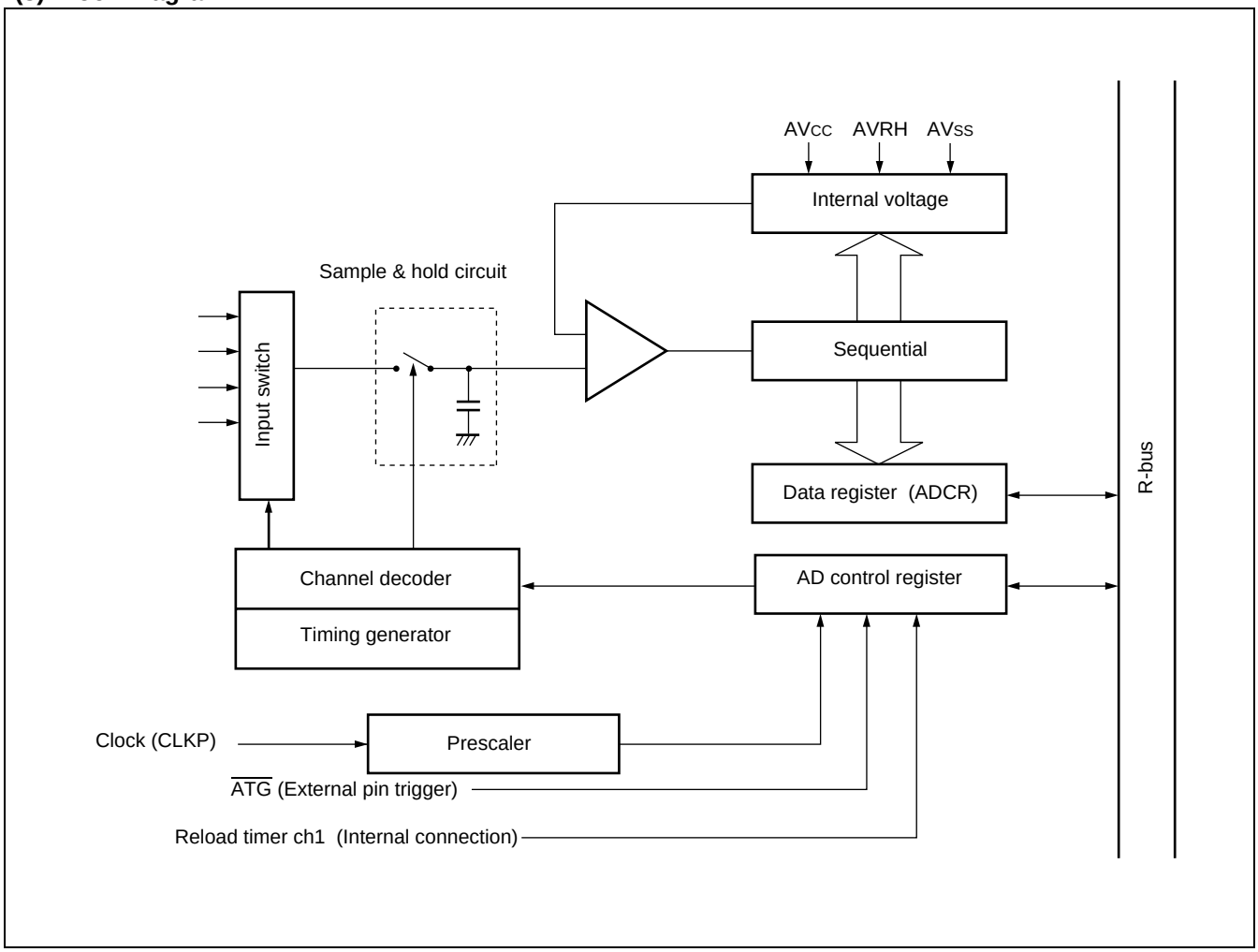
bit	7	6	5	4	3	2	1	0
	MD1	MD0	ANS2	ANS1	ANS0	ANE2	ANE1	ANE0

• Data register (ADCR)

bit	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	9	8

bit	7	6	5	4	3	2	1	0
	7	6	5	4	3	2	1	0

(3) Block Diagram



(4) Precautions for Use:

When the A/D converter is started from an external trigger or internal timer, the ADCS register A/D start source bits STS1, STS0 are set, and at this time the input values for the external trigger and internal timer should be set to the inactive side. If these values are set to the active side, abnormal operation may result.

When setting the STS1, STS0 bits, set $\overline{ATG}$ = “1” input, reload timer (channel 2) = “0” output.

Note : If internal impedance is higher than the specified value, it may not be possible to obtain analog input value sampling within the specified sampling time, so that proper results will not be obtained.

8. I²C Interface

(1) Overview

The I²C interface operates as a master/slave device on the I²C bus at serial I/O ports with IC bus support. The following features are provided.

- Master/slave sending and receiving
- Arbitration function
- Clock synchronization function
- Slave address/general call address detection function
- Transfer direction detection function
- Start condition repeat generation and detection function
- Bus error detection function
- 10-bit/7-bit master/slave addressing
- Compatible with standard mode (Max 100 Kbps) or high speed mode (Max 400 Kbps)
- Transfer end interrupt/bus error interrupt generation

(2) Register List

- Bus Control Register (IBCR)

Address : 000094H

15	14	13	12	11	10	9	8
BER	BEIE	SCC	MSS	ACK	GCAA	INTE	INT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Default value →

- Bus Status Register (IBSR)

Address : 000095H

7	6	5	4	3	2	1	0
BB	RSC	AL	LRB	TRX	AAS	GCA	ADT
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0

Default value →

- 10-Bit Slave Address Register

Address : 000096H

15	14	13	12	11	10	9	8
—	—	—	—	—	—	TA9	TA8
—	—	—	—	—	—	R/W	R/W
						0	0

Default value →

Address : 000097H

7	6	5	4	3	2	1	0
TA7	TA6	TA5	TA4	TA3	TA2	TA1	TA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Default value →

(Continued)

(Continued)

• 10-Bit Slave Address Mask Register (ITMK)

Address : 000098H

15	14	13	12	11	10	9	8
ENTB	RAL	—	—	—	—	TM9	TM8
R/W	R					R/W	R/W
0	0	—	—	—	—	1	1

Address : 000099H

7	6	5	4	3	2	1	0
TM7	TM6	TM5	TM4	TM3	TM2	TM1	TM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

• 7-Bit Slave Address Register (ISBA)

Address : 00009BH

7	6	5	4	3	2	1	0
—	SA6	SA5	SA4	SA3	SA2	SA1	SA0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W
—	0	0	0	0	0	0	0

• 7-Bit Slave Address Mask Register (ISMK)

Address : 00009AH

15	14	13	12	11	10	9	8
ENSB	SM6	SM5	SM4	SM3	SM2	SM1	SM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	1	1	1	1	1	1	1

• Data Register (IDAR)

Address : 00009DH

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

• Clock Control Register (ICCR)

Address : 00009EH

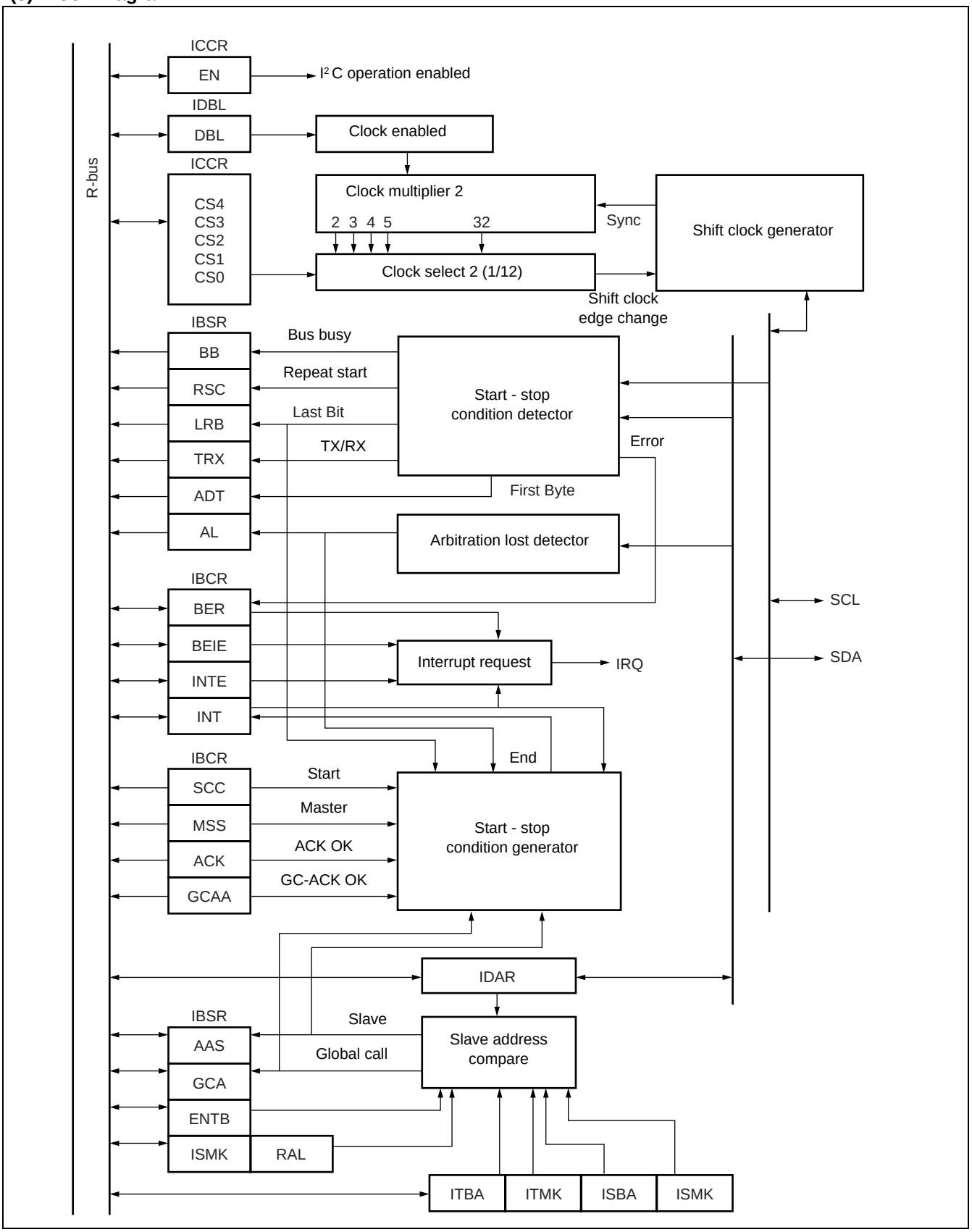
15	14	13	12	11	10	9	8
TEST	—	EN	CS4	CS3	CS2	CS1	CS0
W		R/W	R/W	R/W	R/W	R/W	R/W
0	—	0	1	1	1	1	1

• Clock Disable Register (IDBL)

Address : 00009FH

7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	DBL
							R/W
—	—	—	—	—	—	—	0

(3) Block Diagram



9. DMAC (DMA Controller)

(1) Overview

This module is used to accomplish DMA (Direct Memory Access) transfer on FR family devices.

DMA transfer controlled by this module increases system performance by enabling high speed transfer of many types of data without going through the CPU.

•Hardware Configuration

This module is principally configured from the following units:

- Five independent DMA channels
- 5 channels independent access control circuit
- 32-bit address registers (reload enabled: 2 per channel)
- 16-bit transfer count registers (reload enabled: 2 per channel)
- 4-bit block count registers (1 per channel)
- External transfer request input pins: DREQ0,DREQ1,DREQ2 (ch0, ch1, ch2 only)
- External transfer request acknowledge output pins: DACK0,DACK1,DACK2 (ch0, ch1, ch2 only)
- DMA output completed pins: DEOP0,DEOP1,DEOP2 (ch0, ch1, ch2 only)
- Fly-by transfer (memory to I/O, memory to memory) (ch0, ch1, ch2 only)
- Two-cycle transfer

•Principal Functions

Data transfer using the DMAC module primarily involves the following functions:

- Supports independent data transfer on multiple channels (5 channels)

(1) Order of priority (ch0 > ch1 > ch2 > ch3 > ch4)

(2) The order can be reversed between ch0 and ch1.

(3) DMAC startup sources

- Input from an external-only pin (edge detection/level detection, ch0, ch1, ch2 only)
- Request from a built-in peripheral (shared interrupt request, including external interrupts)
- Software request (register write)

(4) Transfer modes

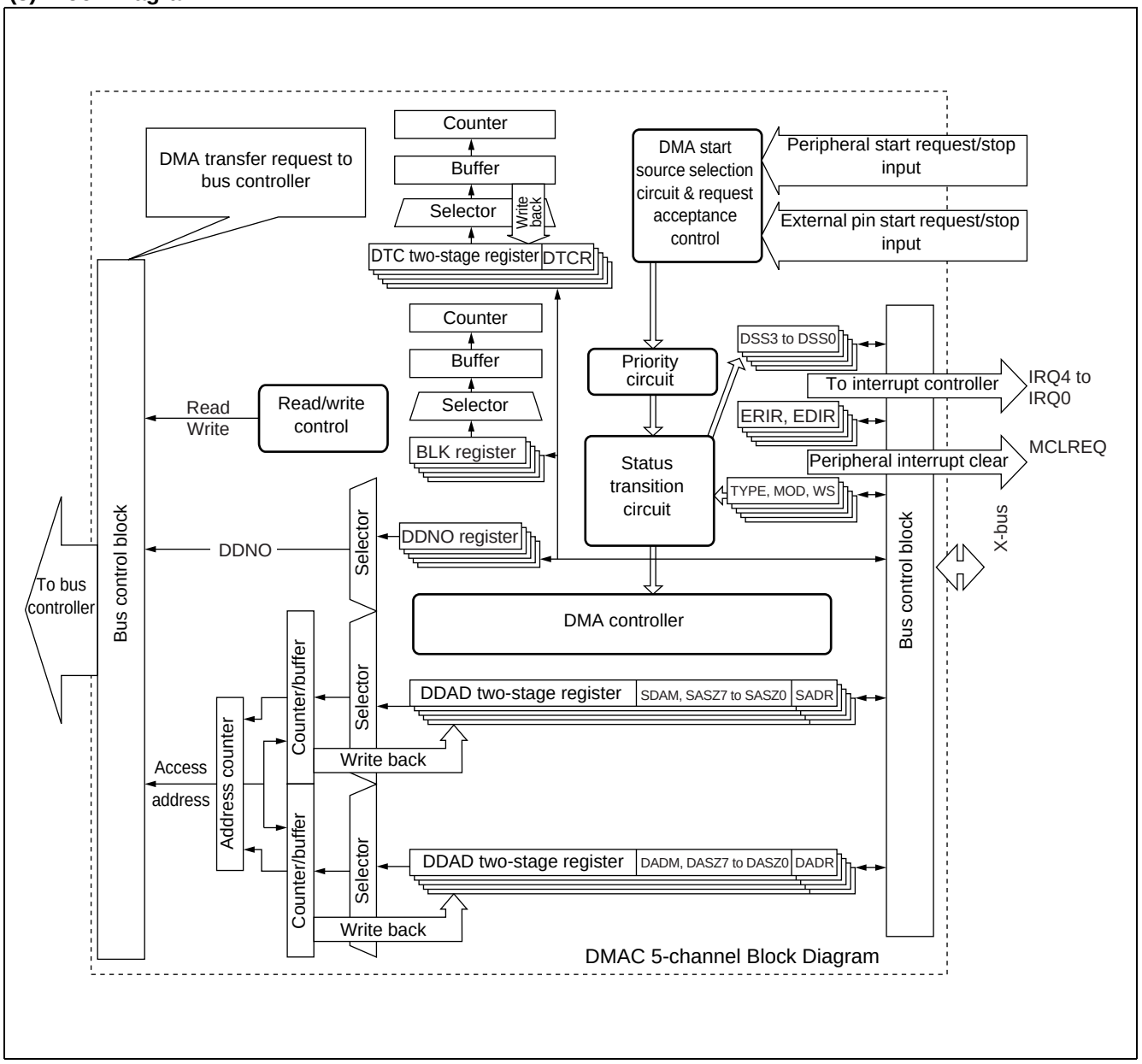
- Demand transfer / burst transfer / step transfer / block transfer
- Addressing mode 32-bit full address designation (increment/decrement/fixed)

  (address increment can be specified up to -255 to +255)
- Data type, byte / half-word / word length
- Single-shot / reload selection available

(2) Register Descriptions

		(bit) 31 24 23 16 15 08 07 00
ch0 Control/status register A	DMACA0 0000200H	
ch0 Control/status register B	DMACB0 0000204H	
ch1 Control/status register A	DMACA1 0000208H	
ch1 Control/status register B	DMACB1 000020CH	
ch2 Control/status register A	DMACA2 0000210H	
ch2 Control/status register B	DMACB2 0000214H	
ch3 Control/status register A	DMACA3 0000218H	
ch3 Control/status register B	DMACB3 000021CH	
ch4 Control/status register A	DMACA4 0000220H	
ch4 Control/status register B	DMACB4 0000224H	
Overall control register	DMACR 0000240H	
ch0 Transfer source address register	DMASA0 0001000H	
ch0 Transfer source address register	DMADA0 0001004H	
ch1 Transfer source address register	DMASA1 0001008H	
ch1 Transfer source address register	DMADA1 000100CH	
ch2 Transfer source address register	DMASA2 0001010H	
ch2 Transfer source address register	DMADA2 0001014H	
ch3 Transfer source address register	DMASA3 0001018H	
ch3 Transfer source address register	DMADA3 000101CH	
ch4 Transfer source address register	DMASA4 0001020H	
ch4 Transfer source address register	DMADA4 0001024H	

(3) Block Diagram



10. External Interface

(1) Overview

The external interface controller controls the interface between the LSI's internal bus and external memory or I/O devices.

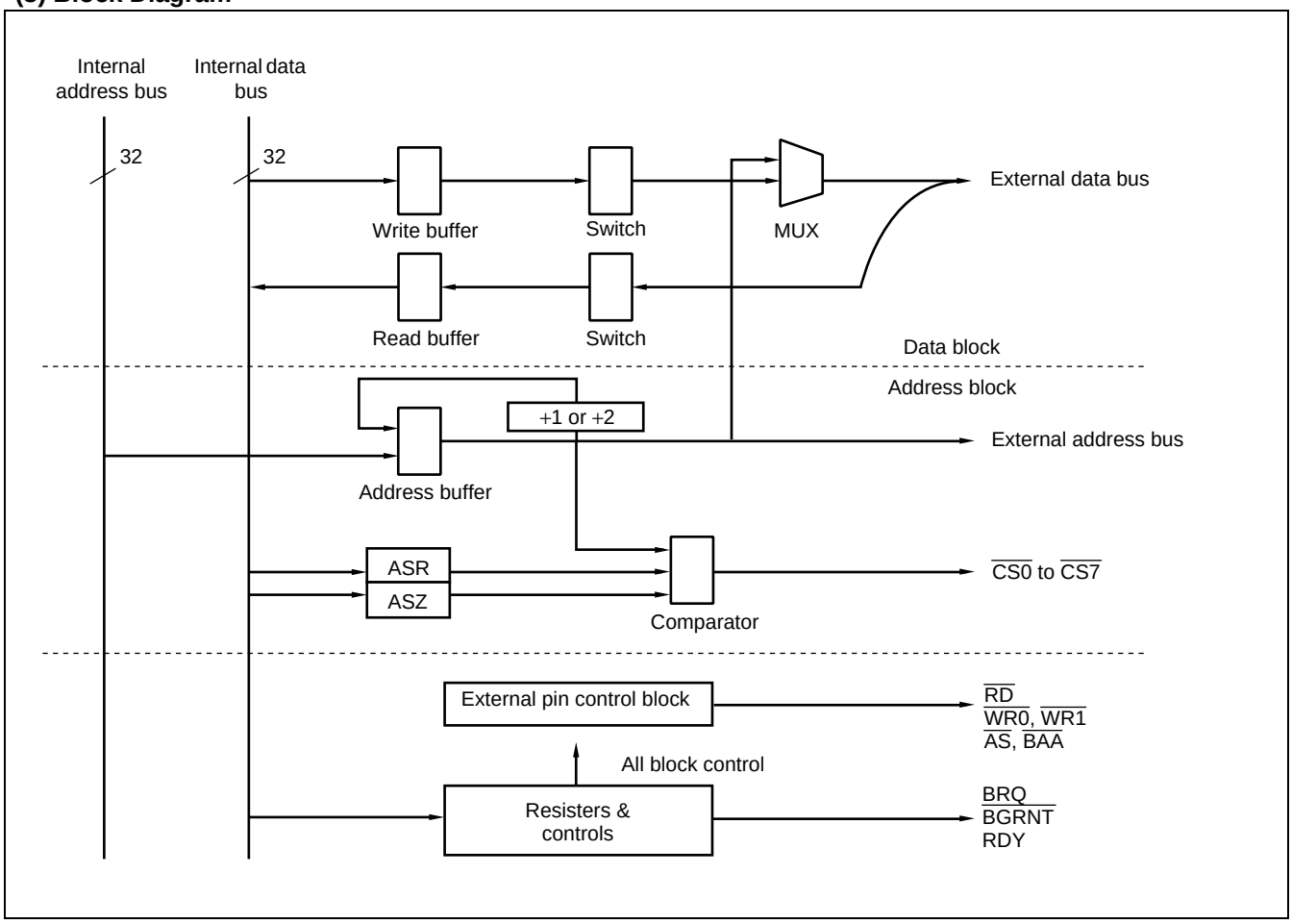
This section describes the functions of the external interface.

(2) Features

- Up to 32 bit-length (4G bytes space) address output.
- Connects directly to many external memory (8 bit/16 bit) devices, allows control of multiple access timings.
  Asynchronous SRAM, asynchronous ROM/Flash memory (multiple write strobe type or byte enable type)
  Page mode ROM/flash memory (2/4/8 page size enabled)
  Burst ROM/Flash memory (MBM29BL160D/161D/162D etc.)
  Address/data multiplexed bus (8 bit/16 bit width only)
  Synchronous memory* (ASIC built-in memory etc.)
  *: Does not connect to synchronous SRAM.
- 8 independent bank (chip select area) settings, each with corresponding chip select output available
  Each area size can be set in multiples of 64K bytes (from 64K bytes to 2G bytes per chip select area).
  Each area can be set in any desired area of logic address space (boundaries limited by area size).
- The following functions can be independently set for each chip select area.
  Chip select area enable/disable (no access to prohibited areas)
  Access timing type for each area, etc.
  Detailed access timing settings (individual access type settings for wait cycle, etc.)
  Data bus width setting (8 bit/16 bit)
  Byte ordering endian setting* (big or little).
  *: $\overline{CS0}$ area available with big endian only.

  Write prohibited setting (read-only areas)
  Internal cache loading enable/disable settings
  Pre-fetch function enable/disable settings
  Maximum burst length setting (1,2,4,8)
- Different detailed timing settings for each access timing type
  Different settings can be used for each chip select area even for the same access timing type.
  Auto wait setting up to 15 cycles (asynchronous SRAM, ROM, Flash, I/O areas)
  Bus cycle extension with external RDY input enabled (asynchronous SRAM, ROM, Flash, I/O areas)
  First access wait and page wait settings enabled (burst, page mode ROM/FLASH areas)
  Different idle, recovery cycles setup delay insertion etc. enabled
- Fly-by transfer with DMA enabled
  Transfer between memory and I/O with 1 access
  Memory wait cycle can be synchronized with I/O wait cycle during fly-by
  Hold time can be obtained by delaying transfer access only
  Specific idle/recovery cycles can be set for fly-by transfer
- External bus arbitration using BRQ and $\overline{BGRNT}$ enabled
- Pins not used in external interface can be set for use as general purpose I/O ports

(3) Block Diagram



(4) I/O Pins

These are the external interface pins. (Some pins have dual functions.)

< Normal bus interface >

A24 to A0, D31 to D16

$\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$, $\overline{CS4}$, $\overline{CS5}$, $\overline{CS6}$, $\overline{CS7}$

$\overline{AS}$, SYSCLK, MCLK

$\overline{RD}$

$\overline{WE}$, $\overline{WR0}$ ($\overline{UUB}$) , $\overline{WR1}$ ($\overline{ULB}$)

RDY, BRQ, $\overline{BGRNT}$

< Memory interface >

MCLK

$\overline{LBA}$ (= $\overline{AS}$) , $\overline{BAA}$*

*: For burst ROM, Flash use

< DMA interface >

$\overline{IOWR}$, $\overline{IORD}$

DACK0, DACK1, DACK2

DREQ0, DREQ1, DREQ2

DEOP0/DSTP0, DEOP1/DSTP1, DEOP2/DSTP2

(5) Register List

Address	31 24	23 16	15 08	07 00
00000640H	ASR0		ACR0	
00000644H	ASR1		ACR1	
00000648H	ASR2		ASR2	
0000064CH	ASR3		ACR3	
00000650H	ASR4		ACR4	
00000654H	ASR5		ACR5	
00000658H	ASR6		ACR6	
0000065CH	ASR7		ACR7	
00000660H	AWR0		AWR1	
00000664H	AWR2		AWR3	
00000668H	AWR4		AWR5	
0000066CH	AWR6		AWR7	
00000670H	Reserved	Reserved	Reserved	Reserved
00000674H	Reserved	Reserved	Reserved	Reserved
00000678H	IOWR0	IOWR1	IOWR2	Reserved
0000067CH	Reserved	Reserved	Reserved	Reserved
00000680H	CSER	CHER	Reserved	TCR
00000684H	Reserved	Reserved	Reserved	Reserved
00000688H	Reserved	Reserved	Reserved	Reserved
0000068CH	Reserved	Reserved	Reserved	Reserved
• • •	• • •	• • •	• • •	• • •
000007F8H	Reserved	Reserved	Reserved	Reserved
000007FCH	Reserved	(MODR)	Reserved	Reserved

Reserved: This address is reserved, and should always be set to “0.”

MODR: Cannot be accessed from user programs.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Supply voltage*1	V_{CC}	V_{SS} – 0.5	V_{SS} + 4.0	V	*2
Internal supply voltage	V_{CCI}	V_{SS} – 0.5	V_{SS} + 2.2	V	*2
Analog supply voltage	AV_{CC}	V_{SS} – 0.5	V_{SS} + 4.0	V	*3
Analog reference voltage	AVRH	V_{SS} – 0.5	V_{SS} + 4.0	V	*3
Input voltage*1	V_I	V_{SS} – 0.3	V_{CC} + 0.3	V	*8
Analog pin input voltage	V_{IA}	V_{SS} – 0.3	AV_{CC} + 0.3	V	
Output voltage*1	V_O	V_{SS} – 0.3	V_{CC} + 0.3	V	*8
Maximum clamp current	I_{CLAMP}	– 2.0	2.0	mA	*7
Total maximum clamp current	$\Sigma \lvert I_{CLAMP} \rvert$	—	20	mA	*7
L level maximum output current	I_{OL}	—	10	mA	*4
L level average output current	I_{OLAV}	—	8	mA	*5
L level maximum total output current	ΣI_{OL}	—	100	mA	
L level average total output current	ΣI_{OLAV}	—	50	mA	*6
H level maximum output current	I_{OH}	—	–10	mA	*4
H level average output current	I_{OHAV}	—	–4	mA	*5
H level maximum total output current	ΣI_{OH}	—	–50	mA	
H level average total output current	ΣI_{OHAV}	—	–20	mA	*6
Power consumption	P_D	—	750	mW	
Operating temperature	T_A	0	+70	°C	
Storage temperature	T_{STG}	—	+150	°C	

*1 : The parameter is based on $V_{SS} = AV_{SS} = 0$ V.

*2 : V_{CC} must not be lower than V_{SS} – 0.3 V.

*3 : AV_{CC} and AVRH shall never exceed V_{CC} + 0.3 V. Also AVRH shall never exceed AV_{CC}.

*4 : Maximum output current determines the peak value of any one of the corresponding pins.

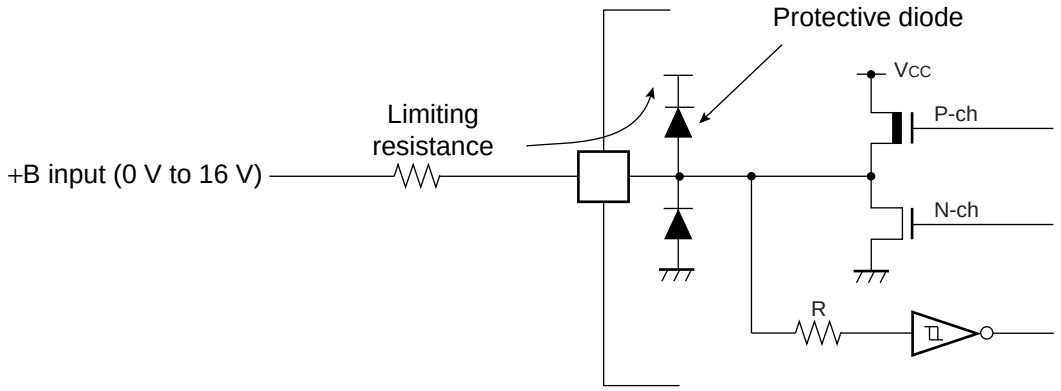
*5 : Average output current is defined as the value of the average current flowing over 100 ms at any one of the corresponding pins.

*6 : Average total output current is defined as the value of the average current flowing over 100 ms at all of the corresponding pins.

*7 :
- Applicable to pins : P20 to P27, P60 to P67, P70, PJ0 to PJ7, PI0 to PI5, PH0 to PH7, PB0 to PB5, PA0 to PA7, P80 to P82, P85, P90 to P97, AN0 to AN3
- Use within recommended operating conditions.
- Use at DC voltage (current) .
- The +B signal should always be applied with a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.

- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the VCC pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller current is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal input.
- Sample recommended circuits :

•Input/Output Equivalent circuits



*8 : V_I and V_O must never exceed V_{CC} + 0.3 V. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Supply voltage	V_{CC}	3.0	3.6	V	
	V_{CCI}	1.65	1.95	V	
Analog supply voltage	AV_{CC}	V_{SS} – 0.3	V_{SS} + 3.6	V	
Analog reference voltage	AVRH	AV_{SS}	AV_{CC}	V	
Operating temperature	T_A	0	+70	°C	

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

(V_{CCI} = 1.65 V to 1.95 V, V_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, T_A = 0 °C to +70 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH}	See note *	—	0.7 × V_{CC}	—	V_{CC} + 0.3	V	
	V_{HIS}	Input pins other than *	—	0.8 × V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
"L" level input voltage	V_{IL}	See note *	—	V_{SS}	—	0.25 × V_{CC}	V	
	V_{ILS}	Input pins other than *	—	V_{SS}	—	0.2 × V_{CC}	V	Hysteresis input
"H" level output voltage	V_{OH}	D16 to D31 A00 to A25 P6 to PH	V_{CC} = 3.0 V I_{OH} = – 4.0 mA	V_{CC} – 0.5	—	V_{CC}	V	
"L" level output voltage	V_{OL}	D16 to D31 A00 to A25 P6 to PH	V_{CC} = 3.0 V I_{OL} = 8.0 mA	V_{SS}	—	0.4	V	
Input leak current (Hi-Z output leak current)	I_{LI}	D16 to D31 A00 to A25 P8 to PH	V_{CC} = 3.6 V 0.45 V<V_I<V_{CC}	–5	—	+5	µA	
Pull-up resistance	R_{UP}	$\overline{INIT}$	V_{CC} = 3.6 V V_I = 0.45 V	12	25	100	kΩ	
Pull-down resistance	R_{DOWN}	P82/BRQ	V_{CC} = 3.6 V V_I = 3.3 V	12	25	100	kΩ	
Supply current	I_{CC}	V_{CC}+V_{CCI}(	f_C = 16.5 MHz V_{CC} = 3.3 V V_{CCI} = 1.8 V	—	150	—	mA	(4x multiplied) 66 MHz operation
	I_{CCS}		f_C = 16.5 MHz V_{CC} = 3.3 V V_{CCI} = 1.8 V	—	50	—	mA	Sleep mode
	I_{CCH}		T_A = 25 °C V_{CC} = 3.3 V V_{CCI} = 1.8 V	—	150	—	µA	Stop mode
Input capacitance	C_{IN}	Other than: V_{CC} V_{SS} AV_{CC} AV_{SS}	—	—	5	15	pF	

* : Pins without hysteresis input pins: D16 to D31, RDY, BRQ, $\overline{INIT}$

4. AC Characteristics

(1) Clock Timing Standards

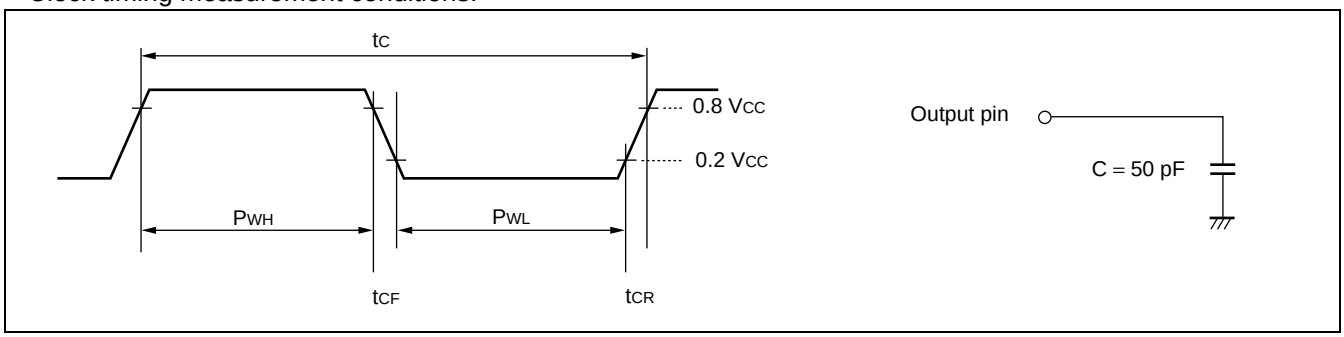
(V_{CCI} = 1.65 V to 1.95 V, V_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, T_A = 0 °C to +70 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Clock frequency (1)	f_C	X0 X1	—	12.5	16.5	MHz	PLL system*1 (self oscillation 16.5MHz,multiplied x4,maximum internal operation 66MHz)
Clock cycle time	t_C	X0 X1		—	60.6	ns	
Clock frequency (2)	f_C	X0 X1	—	10	33	MHz	Self oscillation (x1/2 frequency input)
Clock frequency (3)	f_C	X0 X1		10	33	MHz	External clock
Clock cycle time	t_C	X0 X1		40	100	ns	
Input clock pulse width	P_{WH} P_{WL}	X0 X1		16	—	ns	
Input clock rise, fall time	t_{CR} t_{CF}	X0 X1		—	8	ns	(t_{CR} + t_{CF})
Internal operating clock frequency	f_{CP}	—	—	0.78*2	66	MHz	CPU system
	f_{CPP}			0.78*2	33	MHz	Peripheral system
	f_{CPT}			0.78*2	66	MHz	External bus system
Internal operating clock cycle time	t_{CP}			15.2	1280*2	ns	CPU system
	t_{CPP}			30.3	1280*2	ns	Peripheral system
	t_{CPT}			15.2	1280*2	ns	External bus system

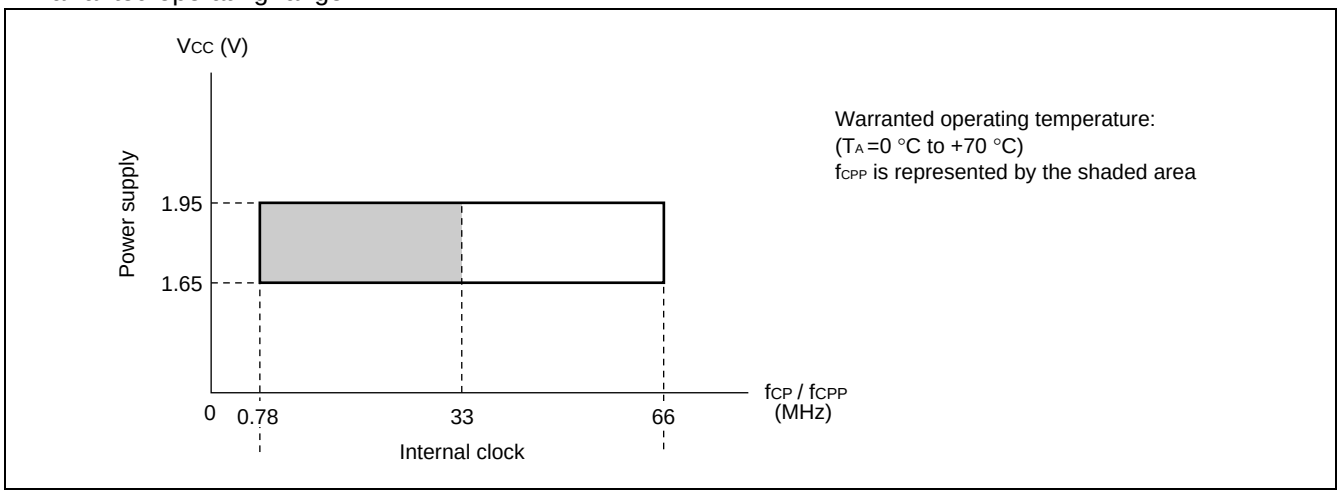
*1 : When using the PLL, the clock frequency should be around 12.5 to 16.5 MHz.

*2 : The values shown represent a minimum clock frequency of 12.5 MHz input at the X0 pin, using the oscillator circuit PLL and a gear ratio of 1/16.

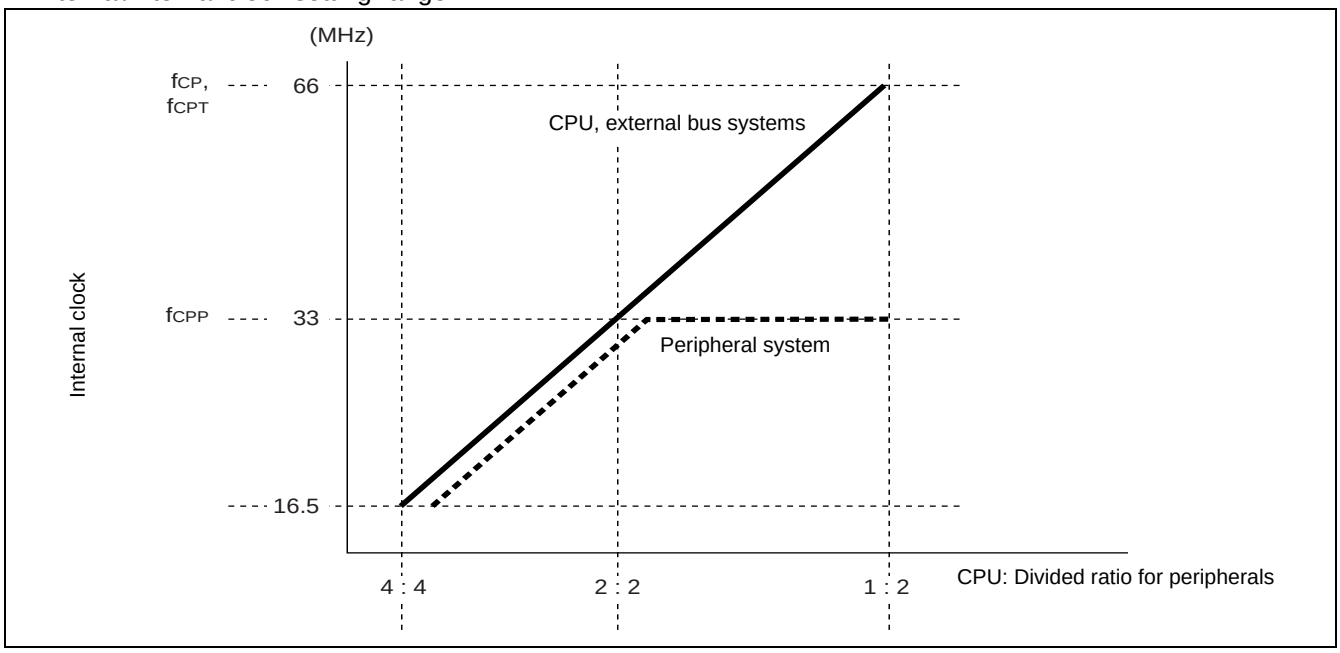
• Clock timing measurement conditions:



• Warranted operating range



• External/internal clock setting range

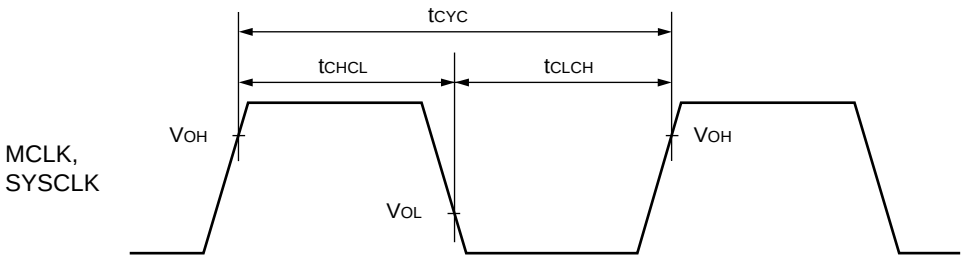


Notes : • When using the PLL, the external clock input should be around 16.5 MHz.
• Set PLL oscillator stabilization time > 300 µs.
• The internal clock gear setting should be within the values shown in (1) clock timing standards.

(2) Clock Output Timing

(V_{CCI} = 1.65 V to 1.95 V, V_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, T_A = 0 °C to +70 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	MCLK, SYSCLK	—	t_{CPT}	—	ns	*1
MCLK↑→MCLK↓ SYSCLK↑→SYSCLK↓	t_{CHCL}	MCLK, SYSCLK		1/2 × t_{CYC} – 3	1/2 × t_{CYC} + 3	ns	*2
MCLK↓→MCLK↑ SYSCLK↓→SYSCLK↑	t_{CLCL}	MCLK, SYSCLK		1/2 × t_{CYC} – 3	1/2 × t_{CYC} + 3	ns	*3



*1 : t_{CYC} represents the frequency of one clock cycle including the gear period.

*2 : The values shown represent standards for × 1 gear period.
For gear period settings of 1/2, 1/4, 1/8, use the following formula replacing n with the value 1/2, 1/4, 1/8 respectively.

$(1/2 \times 1/n) \times t_{CYC} - 10$

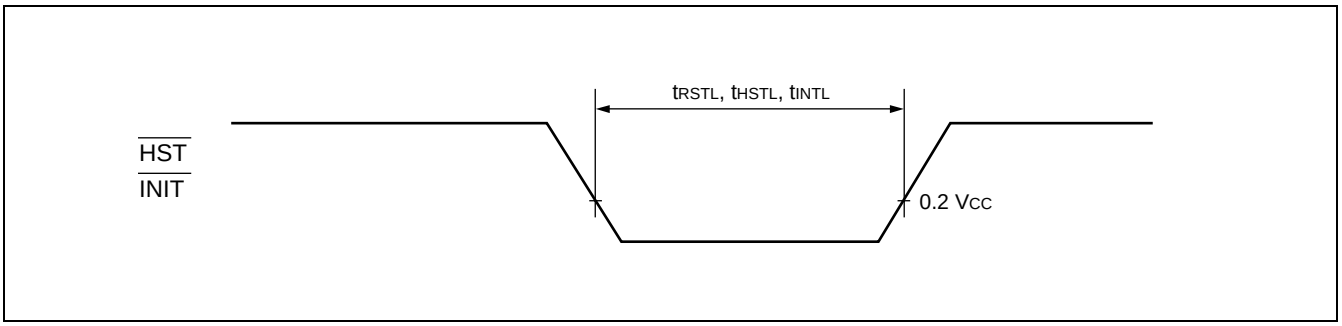
*3 : The values shown represent standards for × 1 gear period.

Note : t_{CPT} indicates the internal operating clock time. See “ (1) Clock Timing Standards”.

(3) Reset and Hardware Standby Input Standards

(V_{CCI} = 1.65 V to 1.95 V, V_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, T_A = 0 °C to +70 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Hardware standby input time	t_{HSTL}	V_{CCI}	—	$t_{CP} \times 5$	—	ns	
INIT input time (power-on)	t_{INTL}	$\overline{INIT}$		*	—	ns	
INIT input time (other than power-on)				$t_{CP} \times 5$	—	ns	



* : INIT input time (at power-on)
FAR, Ceralock : $\phi \times 2^{15}$ or greater recommended
Crystal : $\phi \times 2^{21}$ or greater recommended
ϕ : Power on $\rightarrow$ X0/X1 period $\times$ 2

Note : t_{CP} indicates the clock cycle time. See “ (1) Clock Timing Standards”.

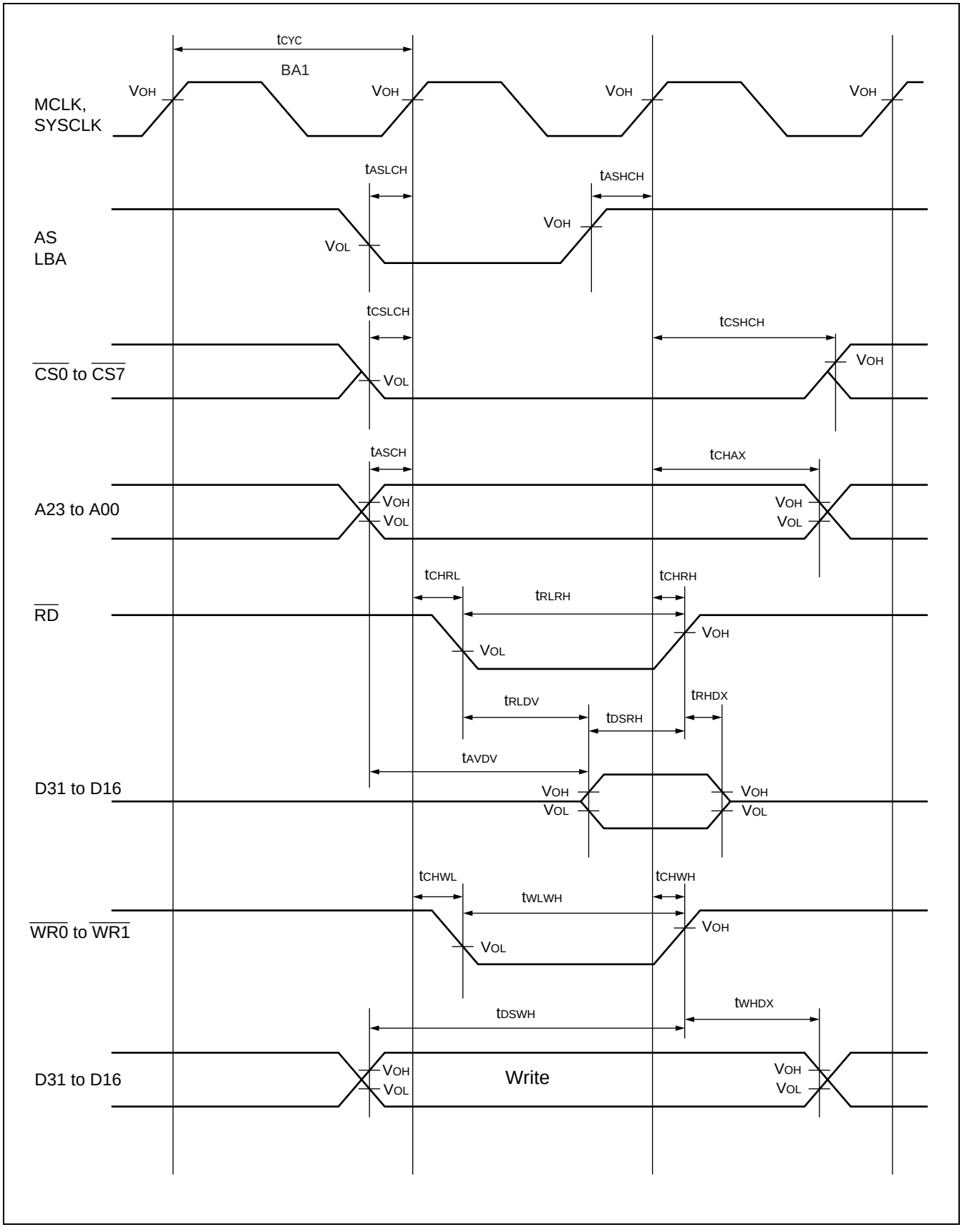
(4) Normal Bus Access Read/Write Operation

(V_{CCI} = 1.65 V to 1.95 V, V_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, T_A = 0 °C to +70 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
$\overline{CS0}$ to $\overline{CS7}$ setup	t_{CSLCH}	MCLK, SYSCLK, $\overline{CS0}$ to $\overline{CS7}$	—	3	—	ns	
$\overline{CS0}$ to $\overline{CS7}$ hold	t_{CSHCH}			3	$t_{CYC}/2 + 6$	ns	
Address setup	t_{ASCH}	MCLK, SYSCLK, A23 to A00	—	3	—	ns	
Address hold	t_{CHAX}	MCLK, SYSCLK, A23 to A00		3	$t_{CYC}/2 + 6$	ns	
Valid address → valid data input time	t_{AVDV}	A23 to A00, D31 to D16		—	$3/2 \times t_{CYC} - 11$	ns	*
$\overline{WR0}$ to $\overline{WR1}$ delay time	t_{CHWL}	MCLK, SYSCLK, $\overline{WR0}$ to $\overline{WR1}$		—	6	ns	
	t_{CHWH}			—	6	ns	
$\overline{WR0}$ to $\overline{WR1}$ minimum pulse width	t_{WLWH}	$\overline{WR0}$ to $\overline{WR1}$		$t_{CYC} - 3$	—	ns	
Data setup → $\overline{WRx}$↑	t_{DSWH}	$\overline{WR0}$ to $\overline{WR1}$, D31 to D16		t_{CYC}	—	ns	
$\overline{WRx}$↑ → data hold time	t_{WHDX}			5	—	ns	
$\overline{RD}$ delay time	t_{CHRL}	MCLK, SYSCLK, $\overline{RD}$		—	6	ns	
	t_{CHRH}			—	6	ns	
$\overline{RD}$↓ → valid data input time	t_{RLDV}	$\overline{RD}$, D31 to D16		—	$t_{CYC} - 10$	ns	*
Data setup → $\overline{RD}$↑time	t_{DSRH}			10	—	ns	
$\overline{RD}$↑ → data hold time	t_{RHDX}			0	—	ns	
$\overline{RD}$ minimum pulse width	t_{RLRH}	$\overline{RD}$		$t_{CYC} - 3$	—	ns	
$\overline{AS}$ setup	t_{ASLCH}	MCLK, SYSCLK, $\overline{AS}$		3	—	ns	
$\overline{AS}$ hold	t_{ASHCH}			3	—	ns	

* : To extend bus time by automatic wait insertion or RDY input, add to this value (t_{CYC} × number of extended cycles).

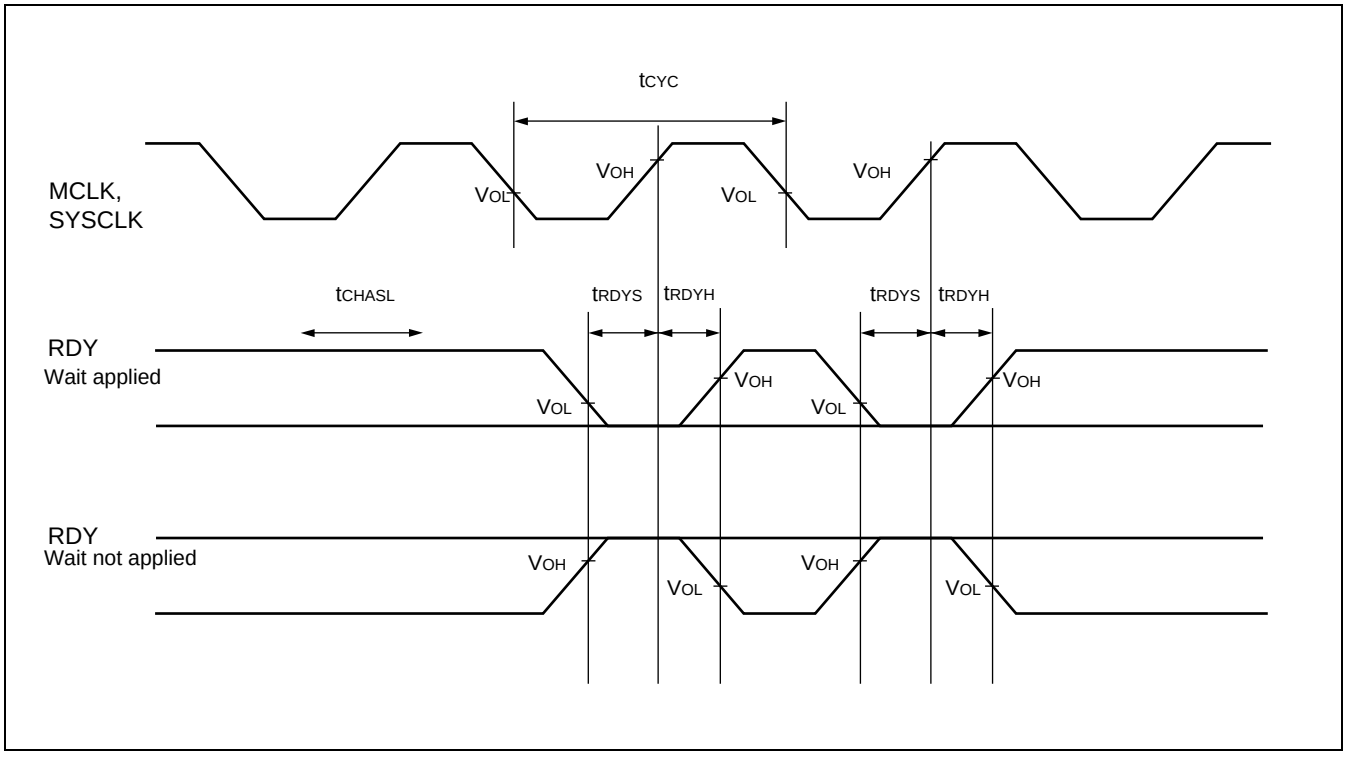
Note : t_{CYC} indicates the cycle time. See “ (2) Clock Output Timing”.



(5) Ready Input Timing

(V_{CCI} = 1.65 V to 1.95 V, V_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, T_A = 0 °C to +70 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
RDY setup time → MCLK↑, SYSCLK↑	t_{RDYS}	MCLK, SYSCLK, RDY	—	10	—	ns	
MCLK↑, SYSCLK↑ RDY hold time	t_{RDYH}	MCLK, SYSCLK, RDY	—	0	—	ns	

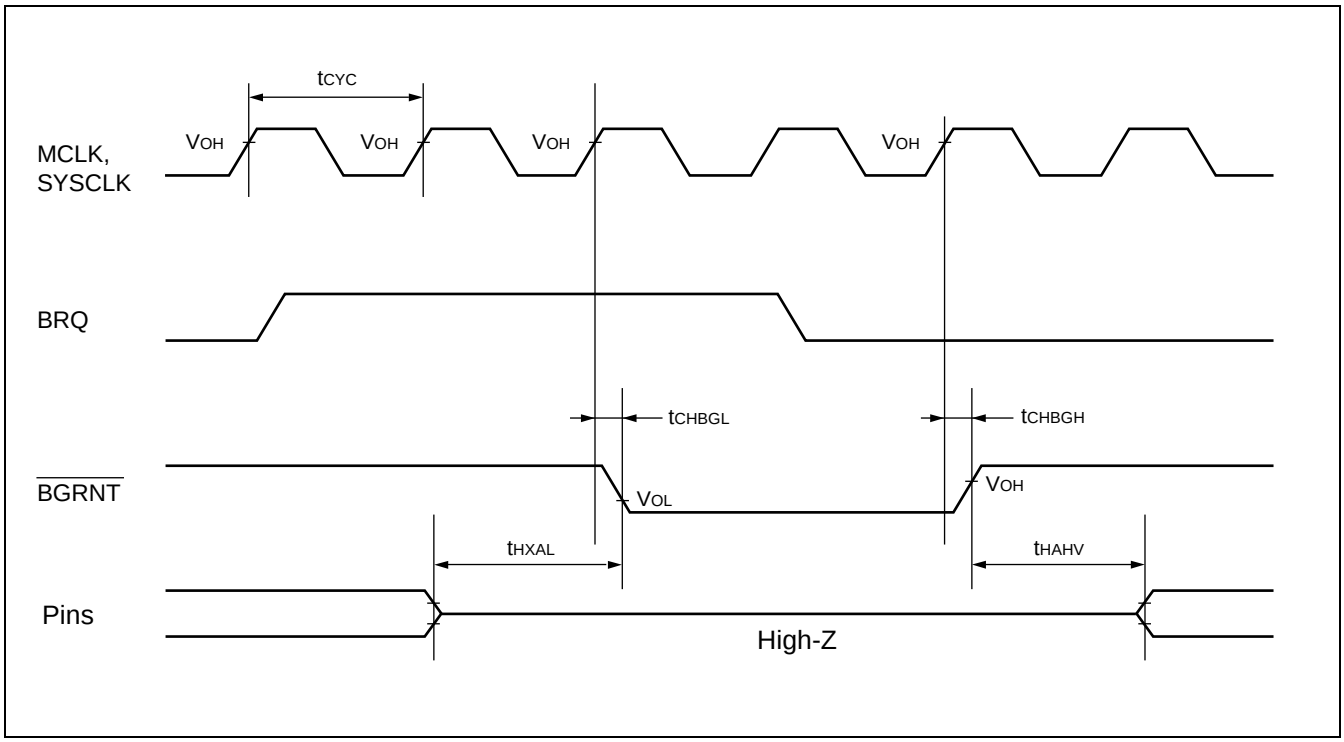


(6) Hold Timing

(V_{CCI} = 1.65 V to 1.95 V, V_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, T_A = 0 °C to +70 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
$\overline{BGRNT}$ delay time	t_{CHBGL}	MCLK, SYSCLK, $\overline{BGRNT}$	—	3	13.5	ns	
	t_{CHBGH}			3	13.5	ns	
Pin floating → $\overline{BGRNT}$↓time	t_{XHAL}	$\overline{BGRNT}$		t_{CYC} – 10	t_{CYC} + 10	ns	
$\overline{BGRNT}$↑ → valid time	t_{HAHV}			t_{CYC} – 10	t_{CYC} + 10	ns	

Note: After a BRQ is accepted, a minimum of 1 cycle is required before $\overline{BGRNT}$ changes.



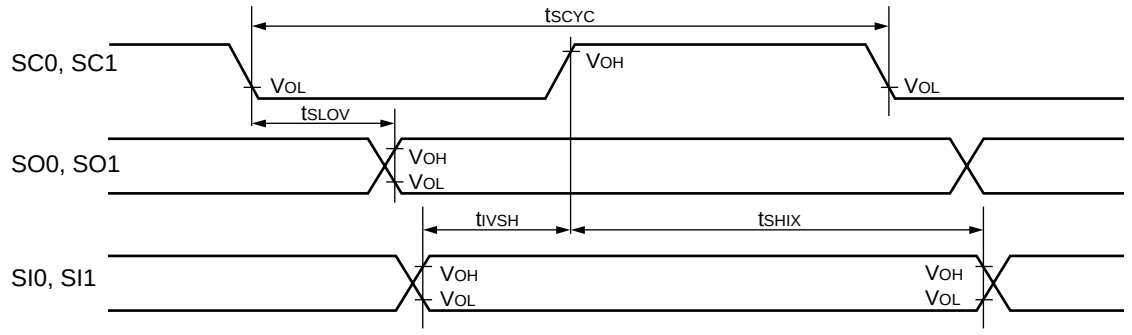
(7) UART Timing

(V_{CCI} = 1.65 V to 1.95 V, V_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, T_A = 0 °C to +70 °C)

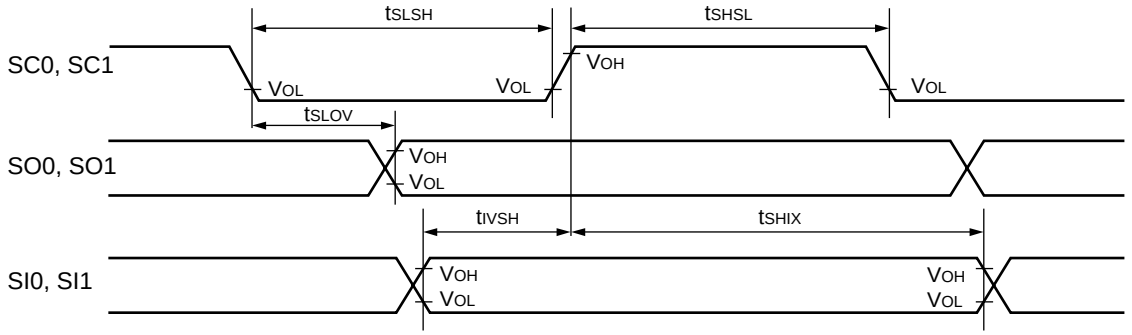
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SC0 to SC2	Internal shift lock mode	8 t_{CPP}	—	ns	
SCLK↓ → SOUT delay time	t_{SLOV}	SC0 to SC2, SO0 to SO2		–80	80	ns	
Valid SIN → SCLK↑	t_{IVSH}	SC0 to SC2, SI0 to SI2		100	—	ns	
SCLK↑ → valid SIN hold time	t_{SHIX}	SC0 to SC2, SI0 to SI2		60	—	ns	
Serial clock “H” pulse width	t_{SHSL}	SC0 to SC2	External shift lock mode	4 t_{CPP}	—	ns	
Serial clock “L” pulse width	t_{SLSH}	SC0 to SC2		4 t_{CPP}	—	ns	
SCLK↓ → SOUT delay time	t_{SLOV}	SC0 to SC2, SO0 to SO2		—	150	ns	
Valid SIN → SCLK↑	t_{IVSH}	SC0 to SC2, SI0 to SI2		60	—	ns	
SCLK↑ → valid SIN hold time	t_{SHIX}	SC0 to SC2, SI0 to SI2		60	—	ns	

Notes: • Above ratings are for operation in CLK synchronized mode.
• t_{CPP} is the cycle time of the peripheral system clock.

• Internal Shift Clock Mode



• External Shift Clock Mode

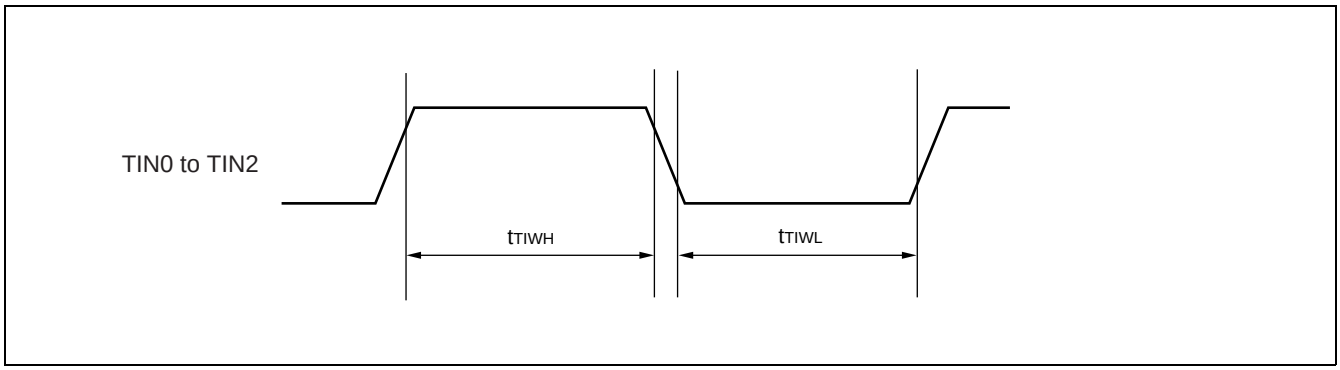


(8) Timer Clock Input Timing

(V_{CCI} = 1.65 V to 1.95 V, V_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, T_A = 0 °C to +70 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH} t_{TIWL}	TIN0 to TIN2	—	2 t_{CYCP}	—	ns	

Note: t_{CYCP} is the cycle time of the peripheral system clock.

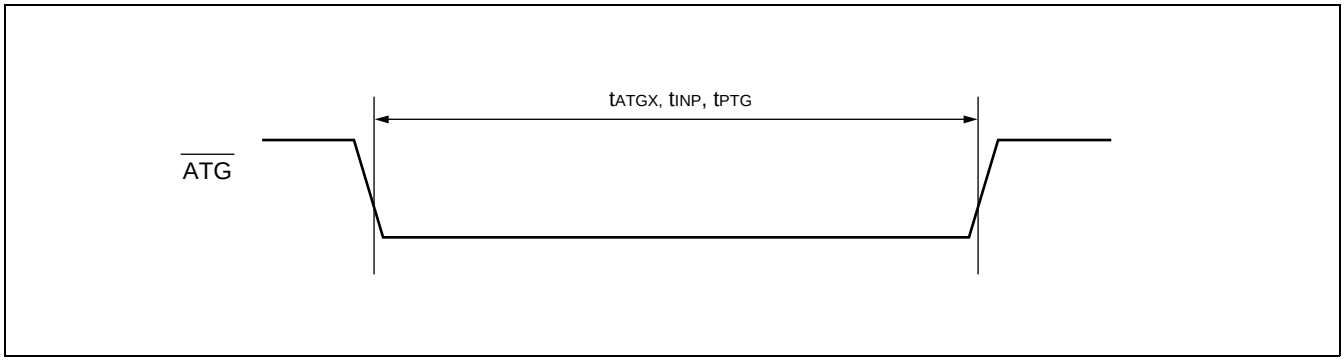


(9) Trigger Input Timing

(V_{CCI} = 1.65 V to 1.95 V, V_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, T_A = 0 °C to +70 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
A/D startup trigger input time	t_{ATGX}	$\overline{ATG}$	—	5 t_{CYCP}	—	ns	

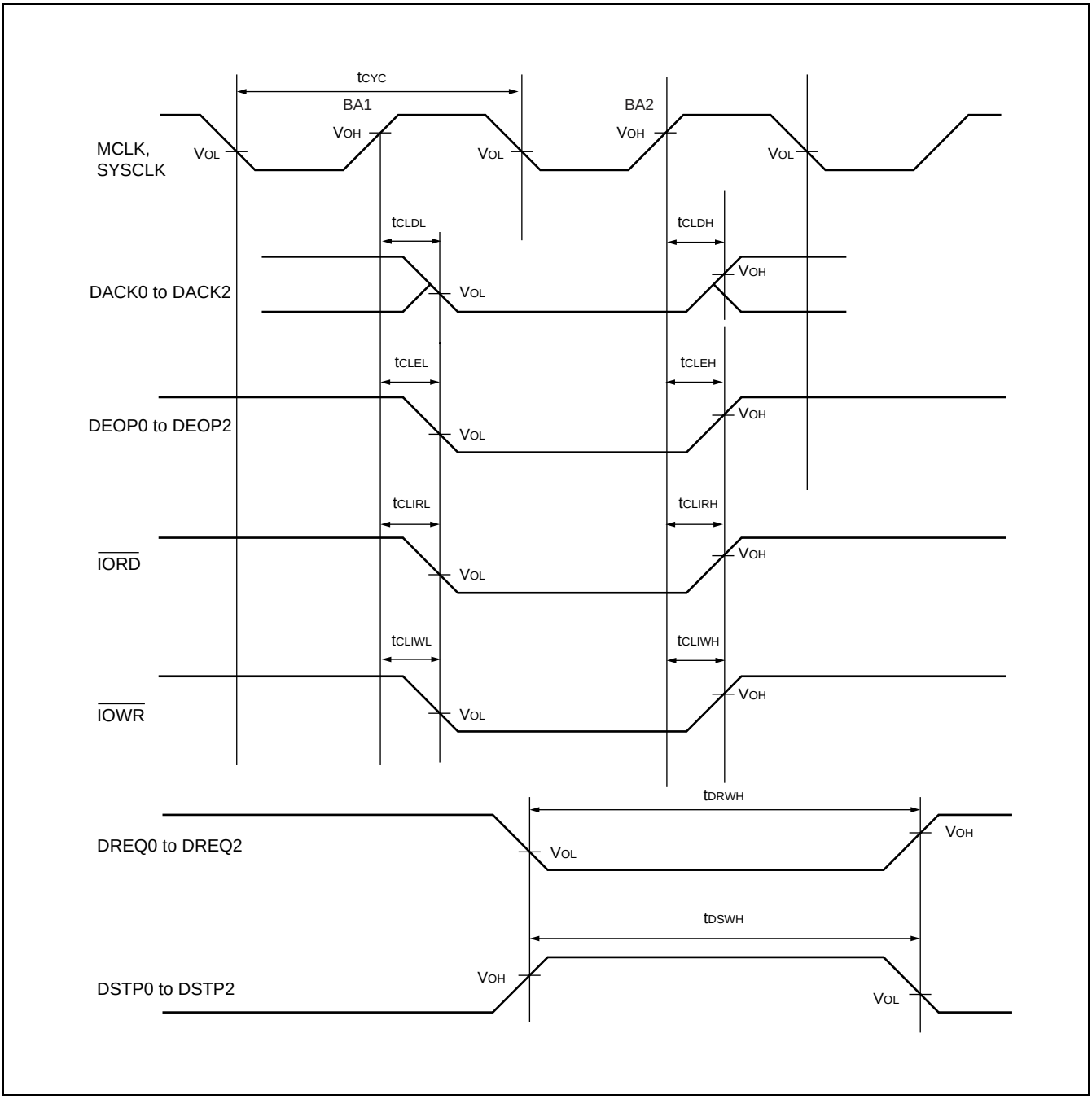
Note: t_{CYCP} is the cycle time of the peripheral system clock.



(10) DMA Controller Timing

(V_{CCI} = 1.65 V to 1.95 V, V_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, T_A = 0 °C to +70 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
DREQ input pulse width	t_{DRWH}	DREQ 0 to DREQ2	—	5 t_{CYC}	—	ns	
DSTP input pulse width	t_{DSWH}	DSTP 0 to DSTP2		5 t_{CYC}	—	ns	
DACK delay time	t_{CLDL}	MCLK, SYSCLK, DACK0 to DACK2		—	6	ns	
	t_{CLDH}			—	6		
DEOP delay time	t_{CLEL}	MCLK, SYSCLK, DEOP 0 to DEOP2		—	6	ns	
	t_{CLEH}			—	6		
$\overline{IORD}$ delay time	t_{CLIRL}	MCLK, SYSCLK		—	6	ns	
	t_{CLIRH}			—	6		
$\overline{IOWR}$ delay time	t_{CLIWL}	MCLK, SYSCLK		—	6	ns	
	t_{CLIWH}			—	6		



(11) I²C Timing

(V_{CCI} = 1.65 V to 1.95 V, V_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, T_A = 0 °C to +70 °C)

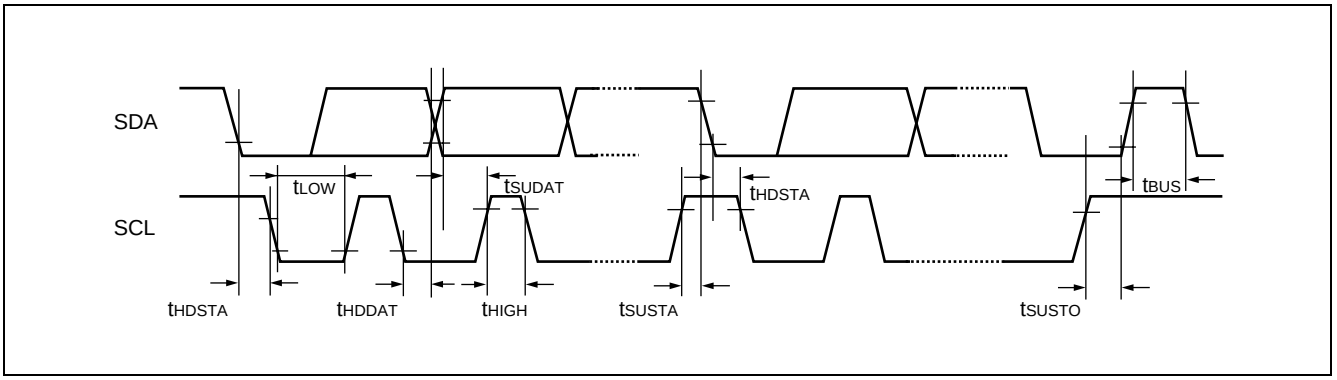
Parameter	Symbol	Condition	Standard mode		High-speed mode*4		Unit
			Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	R = 1.0 kΩ, C = 50 pF*1	0	100	0	400	kHz
(Repeat) “start” condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		4.0	—	0.6	—	µs
SCL clock “L” width	t_{LOW}		4.7	—	1.3	—	µs
SCL clock “H” width	t_{HIGH}		4.0	—	0.6	—	µs
Repeat “start” condition setup time SCL ↑ → SDA ↓	t_{SUSTA}		4.7	—	0.6	—	µs
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45*2	0	0.9*3	µs
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250	—	100	—	ns
“Stop” condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		4.0	—	0.6	—	µs
Bus free time between “stop” and “start” conditions	t_{BUS}		4.7	—	1.3	—	µs

*1 : R, C : Pull-up resistor and load capacitor of the SCL and SDA lines.

*2 : The maximum t_{HDDAT} only has to be met if the device does not stretch the “L” width (t_{LOW}) of the SCL signal.

*3 : A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement $t_{SUDAT} \geq 250$ ns must then be met.

*4 : For use at over 100 kHz, set the resource clock to at least 6 MHz.



5. A/D Converter Electrical Characteristics

(V_{CCI} = 1.65 V to 1.95 V, V_{CC} = +3.0 V to +3.6 V, V_{SS} = AV_{SS} = 0 V, T_A = 0 °C to +70 °C)

Parameter	Symbol	Pin name	Value			Unit
			Min	Typ	Max	
Resolution	—	—	—	10	10	BIT
Total error	—	—	—	—	± 4.5	LSB
Linear error	—	—	—	—	± 3.0	LSB
Differential linear error	—	—	—	—	± 2.5	LSB
Zero transition error	V_{OT}	AN0 to AN3	– 1.5	+ 0.5	+ 4.5	LSB
Full scale transition error	V_{FST}	AN0 to AN3	AVRH – 4.5	AVRH – 1.5	AVRH + 4.5	LSB
Conversion time	—	—	5.4 *1	—	—	µs
Analog port input current	I_{AIN}	AN0 to AN3	—	0.1	10	µA
Analog input voltage	V_{AIN}	AN0 to AN3	AVss	—	AVRH	V
Reference voltage	—	AVRH	AVss	—	AV_{CC}	V
Supply current	I_A	AV_{CC}	—	600	—	µA
	I_{AH}		—	—	10 *2	µA
Reference voltage supply current	I_R	AVRH	—	600	—	µA
	I_{RH}		—	—	10 *2	µA
Inter-channel variation	—	AN0 to AN3	—	—	5	LSB

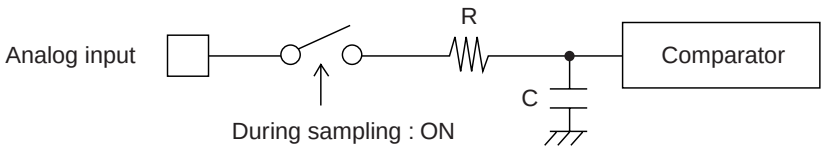
*1 : At V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{CCI} = 1.65 V to 1.95 V machine clock 33 MHz.

*2 : Current in CPU stop mode with A/D converter not operating (at V_{CC} = AV_{CC} = AVRH = 3.6 V, V_{CCI} = 1.95 V)

• About the external impedance of the analog input and its sampling time

- A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision.

- Analog input circuit model



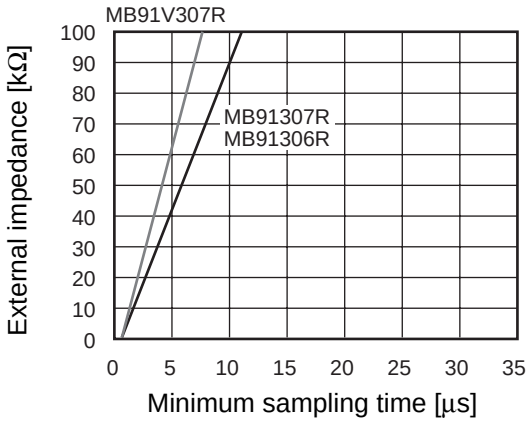
Note : The values are reference values.

	R	C
MB91307R/306R	5.0 kΩ (Max)	15 pF (Max)
MB91V307R	8.1 kΩ (Max)	10 pF (Max)

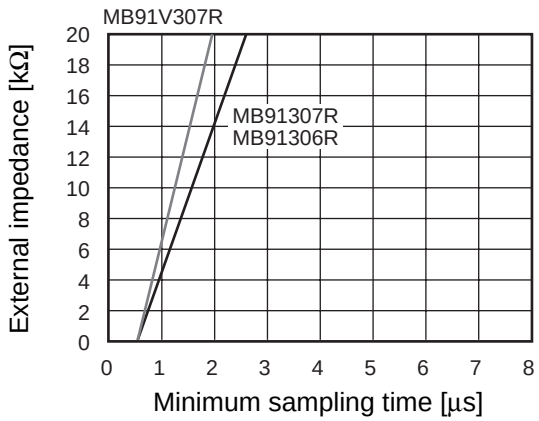
- To satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value.

- The relationship between external impedance and minimum sampling time

External impedance = 0 kΩ to 100 kΩ



External impedance = 0 kΩ to 20 kΩ



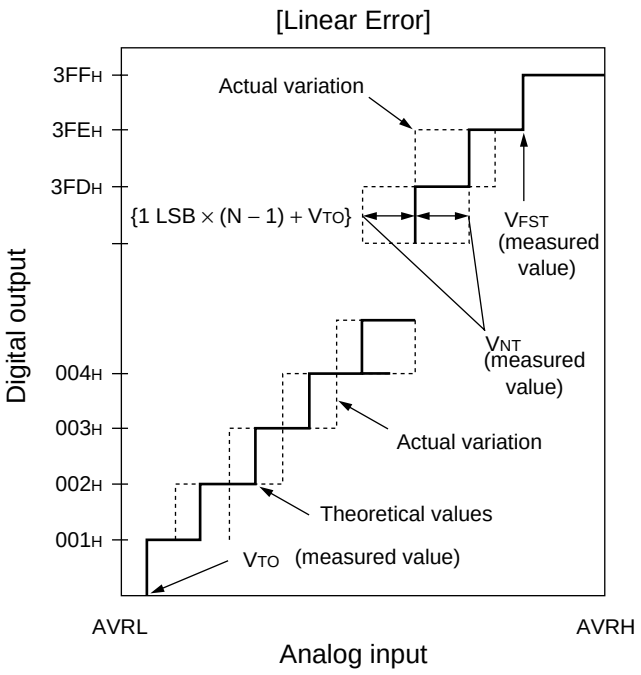
- If the sampling time cannot be sufficient, connect a capacitor of about 0.1 mF to the analog input pin.

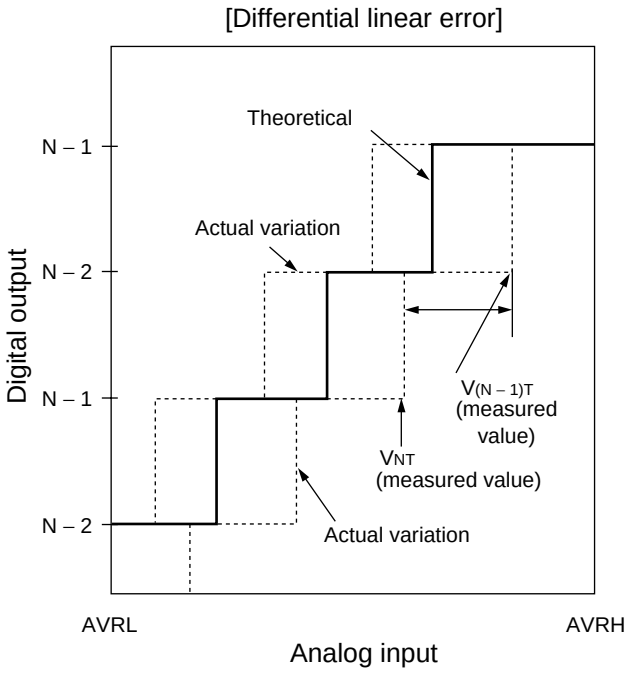
- **About errors**

As | AVRH | becomes smaller, values of relative errorsgrow larger.

Definition of A/D Converter Terms

- Resolution
  Indicates the ability of the A/D converter to discriminate analog variation
- Linear error
  Expresses the deviation between actual conversion characteristics and a straight line connecting the device's zero transition point (00 0000 0000←→00 0000 0001) and full scale transition point (11 1111 1110←→11 1111 1111)
- Differential linear error
  Expresses the deviation of the logical value of input voltage required to create a variation of 1 LSB in output code.





$$\text{Linear error in digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ \text{[LSB]}$$

$$\text{Differential linear error in digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{[LSB]}$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ \text{[V]}$$

$$1\ \text{LSB"} = \frac{\text{AVRH} - \text{AVRL}}{1024}\ \text{[V]}\quad \text{(theoretical value)}$$

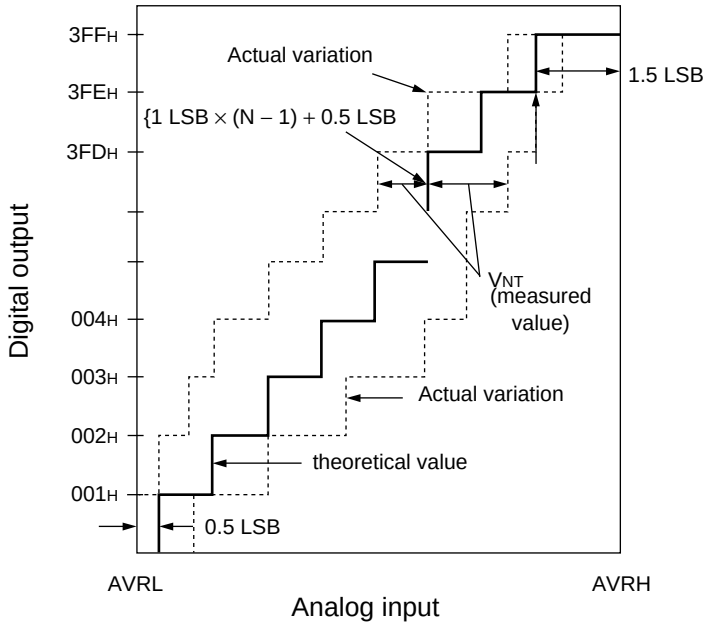
V_{OT} : Voltage at which the digital output transitions from "000"$_H$ to "001"$_H$.

V_{FST} : Voltage at which the digital output transitions from "3FE"$_H$ to "3FF"$_H$.

V_{NT} : Voltage at which the digital output transitions from (N-1) to N.

- Total error
  Expresses the difference between actual and theoretical values as error, including zero transition error, full-scale error, and linearity error.

[Total error]



$$\text{Total error in digital output N} = \frac{V_{NT} - \{1\ \text{LSB}'' \times (N-1) + 0.5\ \text{LSB}''\}}{1\ \text{LSB}''}\ [\text{LSB}]$$

V_{OT}" (theoretical value) = AVRL + 0.5 LSB" [V]

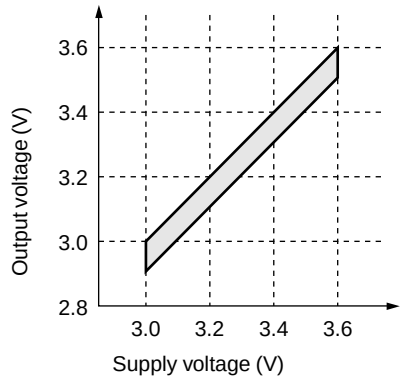
V_{FST}" (theoretical value) = AVRH – 1.5 LSB" [V]

V_{NT} : Voltage at which digital output transitions from (N-1) to N.

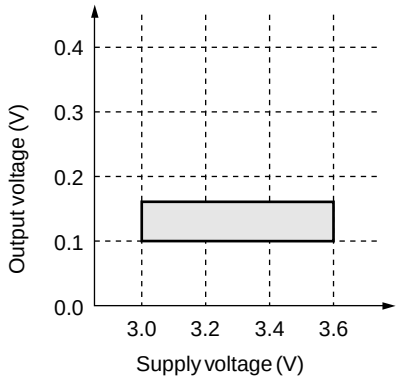
■ EXAMPLE CHARACTERISTICS

(1) Sample output voltage characteristics (T_A = +25 °C)

Sample output H voltage (V_{OH}) characteristics

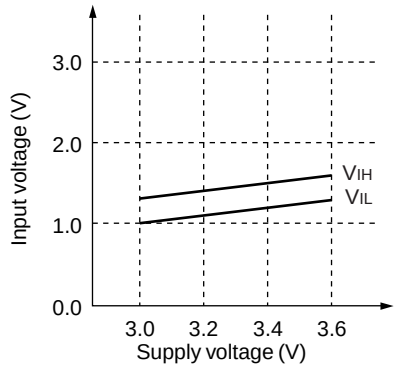


Sample output L voltage (V_{OL}) characteristics

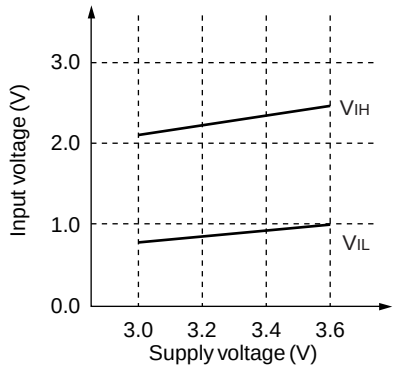


(2) Sample input voltage characteristics (T_A = +25 °C)

Sample input H/L level characteristics (CMOS)

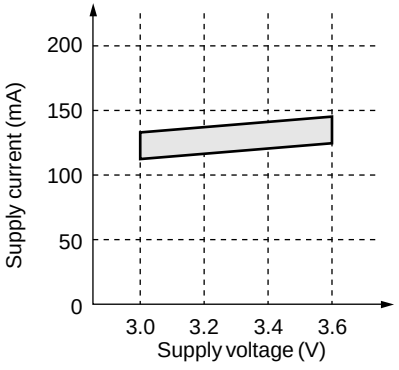


Sample input H/L level characteristics (hysteresis)

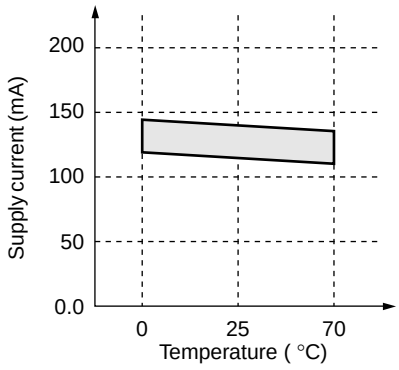


(3) Sample supply current characteristics

Sample supply current (I_{CC}) characteristics
(T_A = +25 °C, 66 MHz)



Sample supply current (I_{CC}) characteristics
(V_{CC} = 3.3 V, 66 MHz)



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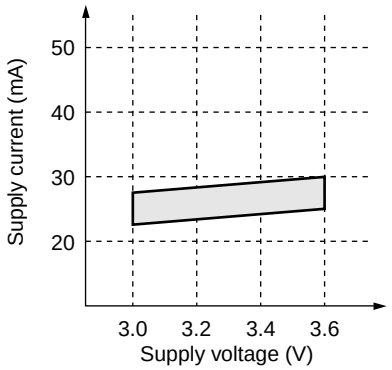
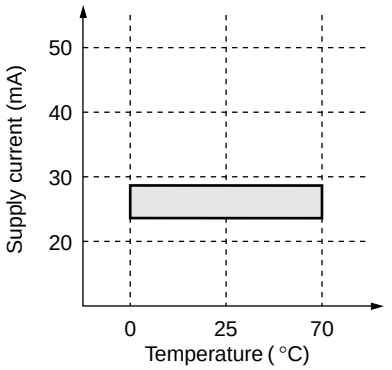
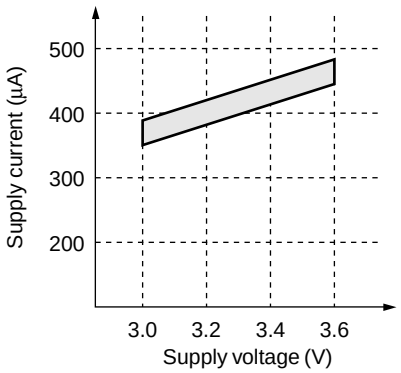
Sample sleep current (I_{CCS}) characteristics
(T_A = +25 °C, 33 MHz)



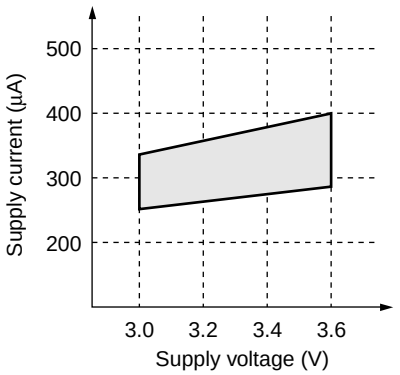
Sample sleep current (I_{CCS}) characteristics
(V_{CC} = 3.3 V, 33 MHz)



Sample A/D supply current (I_A) characteristics
(T_A = +25 °C, 33 MHz)

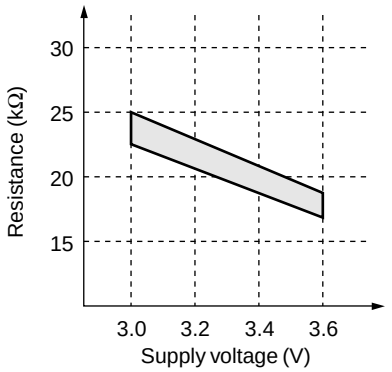


Sample A/D reference current (I_R) characteristics
(T_A = +25 °C, 33 MHz)

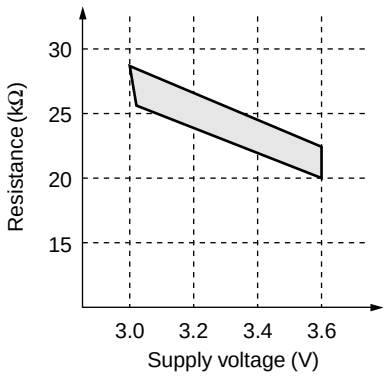


(4) Port resistance characteristics

Sample pull-up resistance characteristics
(T_A = +25 °C)



Sample pull-down resistance characteristics
(T_A = +25 °C)



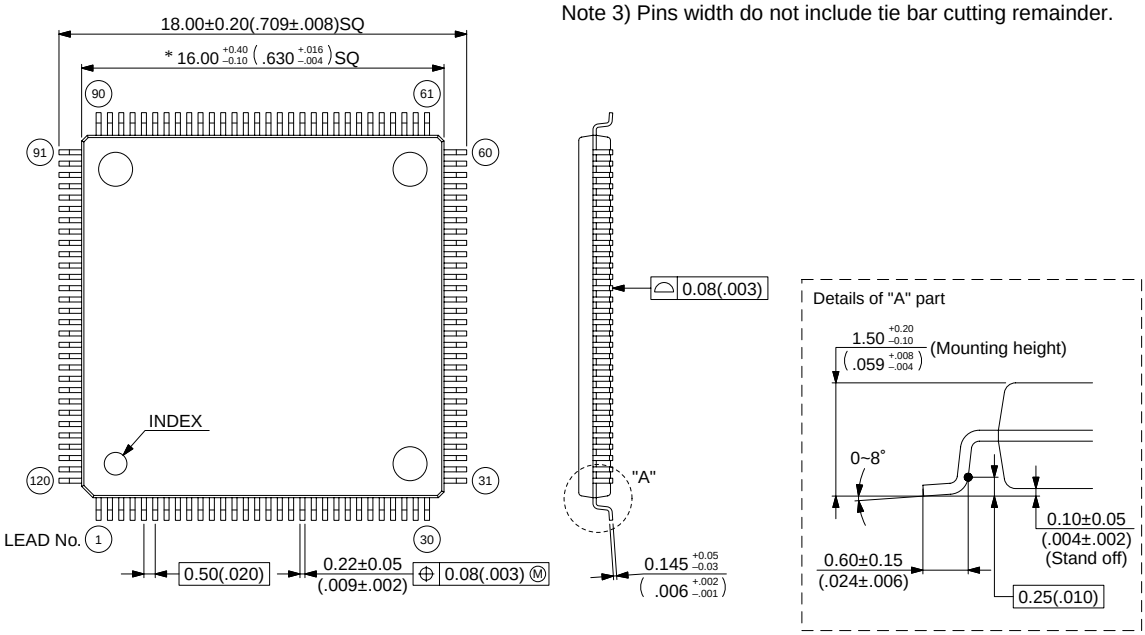
■ ORDERING INFORMATION

Part number	Package	Remarks
MB91306RPFV MB91307RPFV	120-pin, Plastic LQFP (FPT-120P-M21)	Lead-free package
MB91V307RCR	135-pin, Ceramic PGA (PGA-135C-A02)	For development tool use

■ PACKAGE DIMENSION

120-pin, Plastic LQFP
(FPT-120P-M21)

Note 1) * : These dimensions do not include resin protrusion.
Resin protrusion is +0.25(.010) MAX(each side).
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches)
Note : The values in parentheses are reference values.

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