

16/32

M32C/83 Group (M32C/83, M32C/83T) Hardware Manual

RENESAS 16/32-BIT SINGLE-CHIP MICROCOMPUTER
M16C FAMILY / M32C/80 SERIES

Hardware Manual

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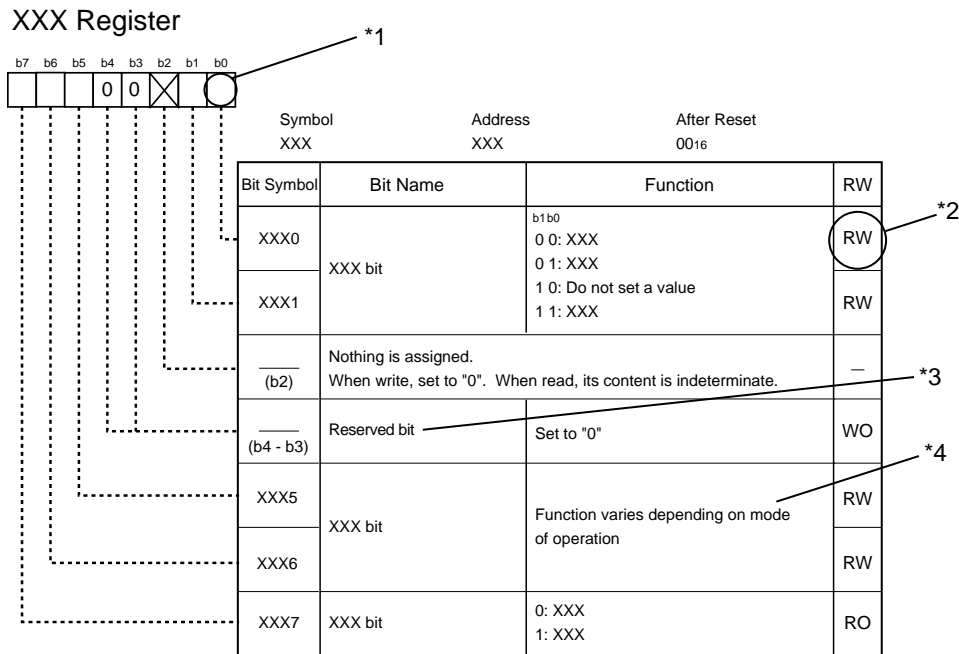
How to Use This Manual

1. Introduction

This hardware manual provides detailed information on the M32C/83 Group (M32C/83, M32C/83T) microcomputers. Users are expected to have basic knowledge of electric circuits, logical circuits and microcomputers.

2. Register Diagram

The symbols, and descriptions, used for bit function in each register are shown below.



*1

Blank: Set to "0" or "1" according to the application

0: Set to "0"

1: Set to "1"

X: Nothing is assigned

*2

RW: Read and write

RO: Read only

WO: Write only

—: Nothing is assigned

*3

- Reserved bit

Reserved bit. Set to specified value.

*4

- Nothing is assigned

Nothing is assigned to the bit concerned. As the bit may be use for future functions, set to "0" when writing to this bit.

- Do not set a value

The operation is not guaranteed when a value is set.

- Function varies depending on mode of operation

Bit function varies depending on peripheral function mode.

Refer to respective register for each mode.

3. M16C Family Documents

The following documents were prepared for the M16C family. ⁽¹⁾

Document	Contents
Short Sheet	Hardware overview
Data Sheet	Hardware overview and electrical characteristics
Hardware Manual	Hardware specifications (pin assignments, memory maps, peripheral specifications, electrical characteristics, timing charts)
Software Manual	Detailed description of assembly instructions and microcomputer performance of each instruction
Application Note	<ul style="list-style-type: none">• Application examples of peripheral functions• Sample programs• Introduction to the basic functions in the M16C family• Programming method with Assembly and C languages
RENESAS TECHNICAL UPDATE	Preliminary report about the specification of a product, a document, etc.

NOTES :

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023F ₁₆	CAN0 Message Slot 15 Control Register (COMCTL15)		02C6 ₁₆	X3 Register Y3 Register (X3R,Y3R)	
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0241 ₁₆	CAN0 Control Register 1 (C0CTLR1)	329	02C8 ₁₆	X4 Register Y4 Register (X4R,Y4R)	
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			02CD ₁₆		
			02CE ₁₆	X7 Register Y7 Register (X7R,Y7R)	
			02CF ₁₆		
			02D0 ₁₆	X8 Register Y8 Register (X8R,Y8R)	
			02D1 ₁₆		
			02D2 ₁₆	X9 Register Y9 Register (X9R,Y9R)	
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			02D5 ₁₆		
			02D6 ₁₆	X11 Register Y11 Register (X11R,Y11R)	
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			02D8 ₁₆	X12 Register Y12 Register (X12R,Y12R)	
			02D9 ₁₆		
			02DA ₁₆	X13 Register Y13 Register (X13R,Y13R)	
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			02E9 ₁₆	UART1 Baud Rate Register (U1BRG)	
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0352 ₁₆	Timer B1 Register (TB1)	152	0382 ₁₆	A/D0 Register1 (AD01)	230	
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03AF ₁₆	Function Select Register C (PSC)	380	03DF ₁₆		
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03B2 ₁₆	Function Select Register B0 (PSL0)	378	03E1 ₁₆	Port P14 Register (P1)	371
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03B4 ₁₆	Function Select Register A2 (PS2)	374	03E2 ₁₆	Port P14 Direction Register (PD0)	372
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03BF ₁₆			03EB ₁₆	Port P14 Direction Register (PD5)	
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03C2 ₁₆	Port P6 Direction Register (PD6)	371	03ED ₁₆		
03C3 ₁₆	Port P7 Direction Register (PD7)				
03C4 ₁₆	Port P8 Register (P8)	372	03EE ₁₆		
03C5 ₁₆	Port P9 Register (P9)				
03C6 ₁₆	Port P8 Direction Register (PD8)	371	03EF ₁₆		
03C7 ₁₆	Port P9 Direction Register (PD9)				
03C8 ₁₆	Port P10 Register (P10)	372	03F0 ₁₆	Pull-Up Control Register 0 (PUR0)	
03C9 ₁₆	Port P11 Register (P11)				
03CA ₁₆	Port P10 Direction Register (PD10)	371	03F1 ₁₆	Pull-Up Control Register 1 (PUR1)	
03CB ₁₆	Port P11 Direction Register (PD11)				
03CC ₁₆	Port P12 Register (P12)	372	03F2 ₁₆		
03CD ₁₆	Port P13 rRegister (P13)				
03CE ₁₆	Port P12 Direction Register (PD12)	371	03F3 ₁₆		
03CF ₁₆	Port P13 Direction Register (PD13)				
			03F4 ₁₆		383
			03F5 ₁₆		
			03F6 ₁₆		
			03F7 ₁₆		
			03F8 ₁₆		
			03F9 ₁₆		
			03FA ₁₆		
			03FB ₁₆		
			03FC ₁₆		
			03FD ₁₆		
			03FE ₁₆		
			03FF ₁₆	Port Control Register (PCR)	

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M32C/83 Group (M32C/83, M32C/83T)

SINGLE-CHIP 16/32-BIT CMOS MICROCOMPUTER

1. Overview

The M32C/83 Group (M32C/83, M32C/83T) microcomputer is a single-chip control unit that utilizes high-performance silicon gate CMOS technology with the M32C/80 Series CPU core. The M32C/83 Group (M32C/83, M32C/83T) is available in 144-pin and 100-pin plastic molded LQFP/QFP packages.

With a 16-Mbyte address space, this microcomputer combines advanced instruction manipulation capabilities to process complex instructions by less bytes and execute instructions at higher speed.

It includes a multiplier and DMAC adequate for office automation, communication devices and industrial equipments, and other high-speed processing applications.

1.1 Applications

Automobiles, audio, cameras, office equipment, communications equipment, portable equipment, etc.

1.2 Performance Overview

Tables 1.1 and 1.2 list performance overview of the M32C/83 Group (M32C/83, M32C/83T).

Table 1.1 M32C/83 Group (M32C/83, M32C/83T) Performance (144-Pin Package)

Characteristic		Performance	
		M32C/83	M32C/83T
CPU	Basic Instructions	108 instructions	
	Minimum Instruction Execution Time	31.3 ns (f(BCLK)=32 MHz, Vcc=4.2 to 5.5 V) ⁽³⁾ 50 ns (f(BCLK)=20 MHz, Vcc=3.0 to 5.5 V)	31.3 ns (f(BCLK)=32 MHz, Vcc=4.2 to 5.5 V) ⁽³⁾
	Operating Mode	Single-chip mode, Memory expansion mode and Microprocessor mode	Single-chip mode
	Address Space	16 Mbytes	
	Memory Capacity	See Table 1.3	
Peripheral Function	I/O Port	123 I/O pins and 1 input pin	
	Multifunction Timer	Timer A: 16 bits x 5 channels, Timer B: 16 bits x 6 channels Three-phase motor control circuit	
	Intelligent I/O	Time measurement function: 16 bits x 12 channels Waveform generating function: 16 bits x 28 channels Communication function (Clock synchronous serial I/O, Clock asynchronous serial I/O, HDLC data processing, Clock synchronous variable length serial I/O, IEBus ⁽¹⁾ , 8-bit or 16-bit Clock synchronous serial I/O)	
	Serial I/O	5 Channels Clock synchronous serial I/O, Clock asynchronous serial I/O, IEBus ⁽¹⁾ , I ² C bus ⁽²⁾	
	CAN Module	1 channel Supporting CAN 2.0B specification	
	A/D Converter	10-bit A/D converter: 2 circuit, 34 channels	
	D/A Converter	8 bits x 2 channels	
	DMAC	4 channels	
	DMAC II	Can be activated by all peripheral function interrupt sources Immediate transfer, Calculation transfer and Chain transfer functions	
	DRAM	CAS before RAS refresh, Self-refresh, EDO, EP	
	CRC Calculation Circuit	CRC-CCITT	
	X/Y Converter	16 bits x 16 bits	
	Watchdog Timer	15 bits x 1 channel (with prescaler)	
	Interrupt	42 internal and 8 external sources, 5 software sources, Interrupt priority level: 7	
	Clock Generation Circuit	4 circuits Main clock oscillation circuit(*), Sub clock oscillation circuit(*), On-chip oscillator, PLL frequency synthesizer (*)Equipped with a built-in feedback resistor. Ceramic resonator or crystal oscillator must be connected externally	
	Oscillation Stop Detect Function	Main clock oscillation stop detect function	
	Electrical Characteristics	Supply Voltage	4.2 to 5.5 V (f(BCLK)=32 MHz) 3.0 to 5.5 V (f(BCLK)=20 MHz, through VDC) 3.0 to 3.6 V (f(BCLK)=20 MHz, not through VDC)
Power Consumption		41 mA (Vcc=5 V, f(BCLK)=32 MHz) 38 mA (Vcc=5 V, f(BCLK)=30 MHz) 26 mA (Vcc=3.3 V, f(BCLK)=20 MHz) 470 μA (Vcc=5 V, f(XCIN)=32 kHz, in wait mode) 340 μA (Vcc=3.3 V, f(XCIN)=32 kHz, through VDC, in wait mode) 5.0 μA (Vcc=3.3 V, f(XCIN)=32 kHz, not through VDC, in wait mode) 0.4 μA (Vcc=5 V, stop mode) 0.4 μA (Vcc=3.3 V, stop mode)	41 mA (Vcc=5 V, f(BCLK)=32 MHz) 38 mA (Vcc=5 V, f(BCLK)=30 MHz) 470 μA (Vcc=5 V, f(XCIN)=32 kHz, in wait mode) 0.4 μA (Vcc=5 V, stop mode)
Flash Memory	Program/Erase Supply Voltage	3.3 ± 0.3 V or 5.0 ± 0.5 V	
	Program and Erase Endurance	100 times	
Operating Ambient Temperature	-20 to 85°C, -40 to 85°C (optional)		-40 to 85°C (T version)
Package	144-pin plastic molded LQFP		

NOTES:

1. IEBus is a trademark of NEC Electronics Corporation.
2. I²C bus is a trademark of Koninklijke Philips Electronics N. V.
3. Contact our sales office if 30-MHz or higher frequency is required.

All options are on a request basis.

Table 1.2 M32C/83 Group (M32C/83, M32C/83T) Performance (100-Pin Package)

Characteristic		Performance	
		M32C/83	M32C/83T
CPU	Basic Instructions	108 instructions	
	Minimum Instruction Execution Time	31.3 ns (f(BCLK) = 32 MHz, V _{CC} = 4.2 to 5.5 V) 50 ns (f(BCLK) = 20 MHz, V _{CC} = 3.0 to 5.5 V)	31.3 ns (f(BCLK) = 32 MHz, V _{CC} = 4.2 to 5.5 V)
	Operating Mode	Single-chip mode, Memory expansion mode and Microprocessor mode	Single-chip mode
	Address Space	16 Mbytes	
	Memory Capacity	See Table 1.3	
Peripheral Function	I/O Port	87 I/O pins and 1 input pin	
	Multifunction Timer	Timer A: 16 bits x 5 channels, Timer B: 16 bits x 6 channels Three-phase motor control circuit	
	Intelligent I/O	Time measurement function: 16 bits x 5 channels Waveform generating function: 16 bits x 10 channels Communication function (Clock synchronous serial I/O, Clock asynchronous serial I/O, HDLC data processing, Clock synchronous variable length serial I/O, IEBus ⁽¹⁾)	
	Serial I/O	5 Channels Clock synchronous serial I/O, Clock asynchronous serial I/O, IEBus ⁽¹⁾ , I ² C bus ⁽²⁾	
	CAN Module	1 channel Supporting CAN 2.0B specification	
	A/D Converter	10-bit A/D converter: 2 circuits, 26 channels	
	D/A Converter	8 bits x 2 channels	
	DMAC	4 channels	
	DMAC II	Can be activated by all peripheral function interrupt sources Immediate transfer, Calculation transfer and Chain transfer functions	
	CRC Calculation Circuit	CRC-CCITT	
	X/Y Converter	16 bits x 16 bits	
	Watchdog Timer	15 bits x 1 channel (with prescaler)	
	Interrupt	42 internal and 8 external sources, 5 software sources Interrupt priority level: 7	
	Clock Generation Circuit	4 circuits Main clock oscillation circuit(*), Sub clock oscillation circuit(*), On-chip oscillator, PLL frequency synthesizer (*)Equipped with a built-in feedback resistor. Ceramic resonator or crystal oscillator must be connected externally	
	Oscillation Stop Detect Function	Main clock oscillation stop detect function	
Electrical Characteristics	Supply Voltage	4.2 to 5.5 V (f(BCLK)=32 MHz) 3.0 to 5.5 V (f(BCLK)=20 MHz, through VDC) 3.0 to 3.6 V (f(BCLK)=20 MHz, not through VDC)	4.2 to 5.5 V (f(BCLK)=32 MHz)
	Power Consumption	41 mA (V _{CC} =5 V, f(BCLK)=32 MHz) 38 mA (V _{CC} =5 V, f(BCLK)=30 MHz) 26 mA (V _{CC} =3.3 V, f(BCLK)=20 MHz) 470 μA (V _{CC} =5 V, f(XCIN)=32 kHz, in wait mode) 340 μA (V _{CC} =3.3 V, f(XCIN)=32 kHz, through VDC, in wait mode) 5.0 μA (V _{CC} =3.3 V, f(XCIN)=32 kHz, not through VDC, in wait mode) 0.4 μA (V _{CC} =5 V, stop mode) 0.4 μA (V _{CC} =3.3 V, stop mode)	41 mA (V _{CC} =5 V, f(BCLK)=32 MHz) 38 mA (V _{CC} =5 V, V _f (BCLK)=30 MHz) 470 μA (V _{CC} =5 V, f(XCIN)=32 kHz, in wait mode) 0.4 μA (V _{CC} =5 V, stop mode)
Flash Memory	Program/Erase Supply Voltage	3.3 ± 0.3 V or 5.0 ± 0.5 V	5.0 ± 0.5 V
	Program and Erase Endurance	100 times	
	Operating Ambient Temperature	-20 to 85°C, -40 to 85°C (optional)	-40 to 85°C (T version)
	Package	100-pin plastic molded LQFP/QFP	

NOTES:

- IEBus is a trademark of NEC Electronics Corporation.
- I²C bus is a trademark of Koninklijke Philips Electronics N. V.
- Contact our sales office if 30-MHz or higher frequency is required.

All options are on a request basis.

1.3 Block Diagram

Figure 1.1 shows a block diagram of the M32C/83 Group (M32C/83, M32C/83T) microcomputer.

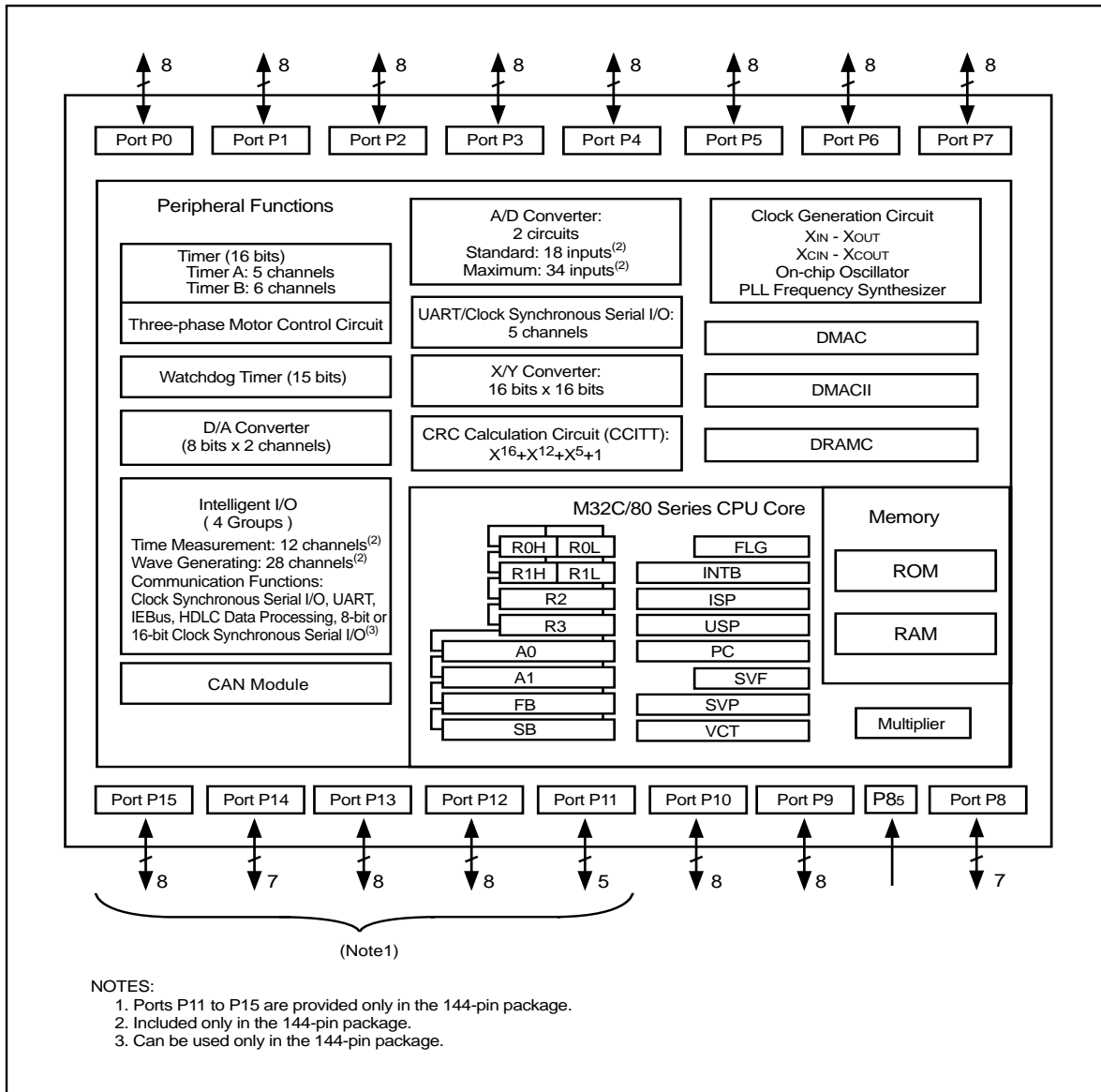


Figure 1.1 M32C/83 Group (M32C/83, M32C/83T) Block Diagram

1.4 Product Information

Table 1.3 lists the product information. Figure 1.2 shows the product numbering system.

Table 1.3 M32C/83 Group (1) (M32C/83) As of January, 2006

Type Number	Package Type	ROM Capacity	RAM Capacity	Remarks
M30835FJGP	PLQP0144KA-A (144P6Q-A)	512K	31K	Flash Memory
M30833FJGP	PLQP0100KB-A (100P6Q-A)			
M30833FJFP	PRQP0100JB-A (100P6S-A)			

Table 1.3 M32C/83 Group (2) (T Version, M32C/83T) As of January, 2006

Type Number	Package Type	ROM Capacity	RAM Capacity	Remarks
M30833FJTGP	PLQP0100KB-A (100P6Q-A)	512K	31K	Flash Memory T Version (High-reliability 85°C Version)

Please contact our sales office for V version information.

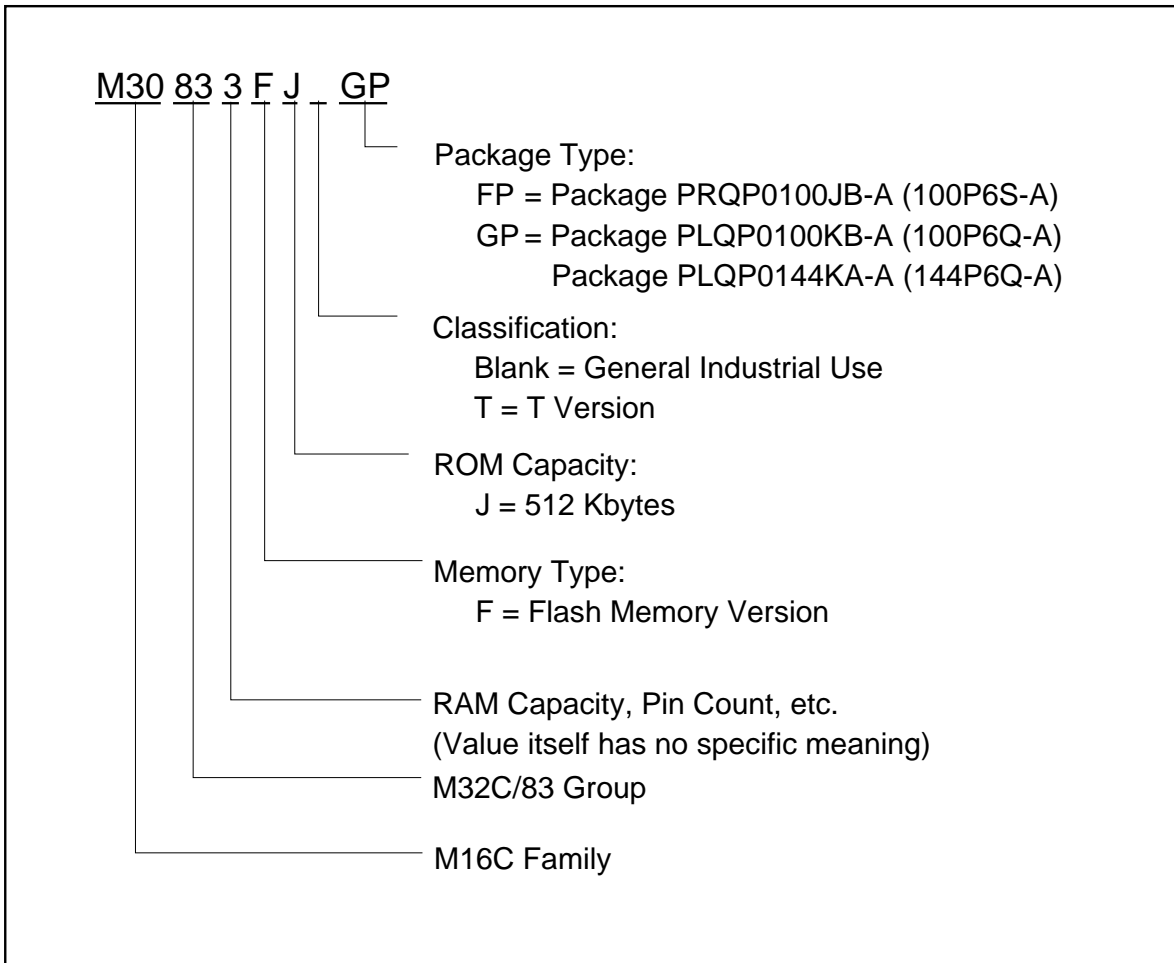


Figure 1.2 Product Numbering System

1.5 Pin Assignment

Figures 1.3 to 1.5 show pin assignments (top view).

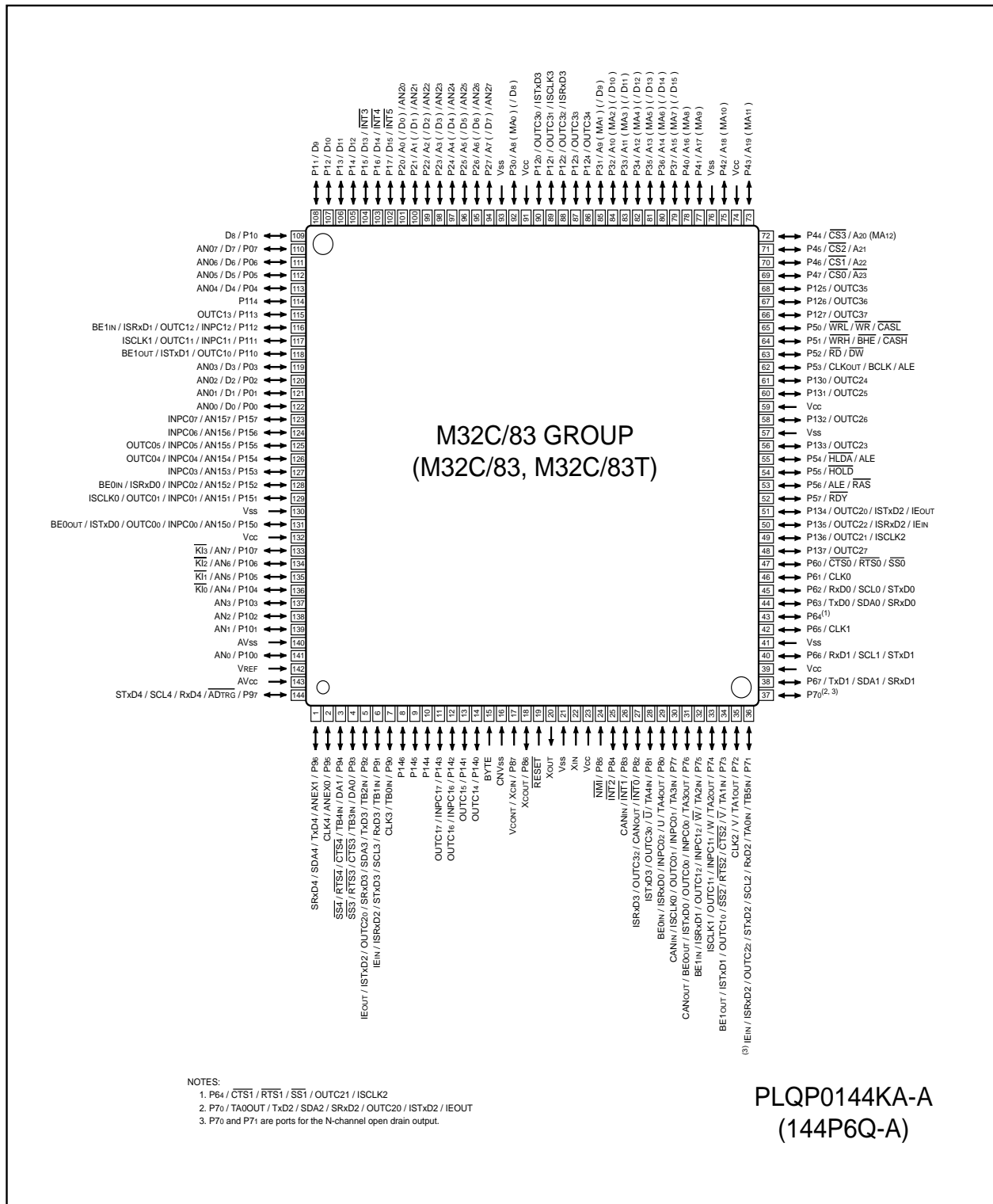


Table 1.4 Pin Characteristics for 144-Pin Package

Pin No	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin ⁽¹⁾
1		P96			TxD4/SDA4/SRxD4		ANEX1	
2		P95			CLK4		ANEX0	
3		P94		TB4IN	CTS4/RTS4/SS4			
4		P93		TB3IN	CTS3/RTS3/SS3		DA0	
5		P92		TB2IN	TxD3/SDA3/SRxD3	OUTC20/IEOUT/ISTxD2		
6		P91		TB1IN	RxD3/SCL3/STxD3	IEIN/ISRxD2		
7		P90		TB0IN	CLK3			
8		P146						
9		P145						
10		P144						
11		P143				INPC17/OUTC17		
12		P142				INPC16/OUTC16		
13		P141				OUTC15		
14		P140				OUTC14		
15	BYTE							
16	CNVSS							
17	XCIN/VCONT	P87						
18	XCOUT	P86						
19	RESET							
20	XOUT							
21	VSS							
22	XIN							
23	VCC							
24		P85	NMI					
25		P84	INT2					
26		P83	INT1		CANIN			
27		P82	INT0		CANOUT	OUTC32/ISRxD3		
28		P81		TA4IN/U		OUTC30/ISTxD3		
29		P80		TA4OUT/U		INPC02/ISRxD0/BE0IN		
30		P77		TA3IN	CANIN	INPC01/OUTC01/ISCLK0		
31		P76		TA3OUT	CANOUT	INPC00/OUTC00/ISTxD0/BE0OUT		
32		P75		TA2IN/W		INPC12/OUTC12/ISRxD1/BE1IN		
33		P74		TA2OUT/W		INPC11/OUTC11/ISCLK1		
34		P73		TA1IN/V	CTS2/RTS2/SS2	OUTC10/ISTxD1/BE1OUT		
35		P72		TA1OUT/V	CLK2			
36		P71		TB5IN/TA0IN	RxD2/SCL2/STxD2	OUTC22/ISRxD2/IEIN		
37		P70		TA0OUT	TxD2/SDA2/SRxD2	OUTC20/ISTxD2/IEOUT		
38		P67			TxD1/SDA1/SRxD1			
39	VCC							
40		P66			RxD1/SCL1/STxD1			
41	VSS							
42		P65			CLK1			
43		P64			CTS1/RTS1/SS1	OUTC21/ISCLK2		
44		P63			TxD0/SDA0/SRxD0			
45		P62			RxD0/SCL0/STxD0			
46		P61			CLK0			
47		P60			CTS0/RTS0/SS0			
48		P137				OUTC27		

NOTES:

1. Bus control pins in M32C/83T cannot be used.

Table 1.4 Pin Characteristics for 144-Pin Package (Continued)

Pin No	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin ⁽¹⁾
49		P136				OUTC21/ISCLK2		
50		P135				OUTC22/ISRxD2/IEiN		
51		P134				OUTC20/ISTxD2/IEoUT		
52		P57						$\overline{\text{RDY}}$
53		P56						$\overline{\text{ALE/RAS}}$
54		P55						$\overline{\text{HOLD}}$
55		P54						$\overline{\text{HLDA/ALE}}$
56		P133				OUTC23		
57	V _{SS}							
58		P132				OUTC26		
59	V _{CC}							
60		P131				OUTC25		
61		P130				OUTC24		
62		P53						$\overline{\text{CLKout/BCLK/ALE}}$
63		P52						$\overline{\text{RD/DW}}$
64		P51						$\overline{\text{WRH/BHE/CASH}}$
65		P50						$\overline{\text{WRL/WR/CASL}}$
66		P127				OUTC37		
67		P126				OUTC36		
68		P125				OUTC35		
69		P47						$\overline{\text{CS0/A23}}$
70		P46						$\overline{\text{CS1/A22}}$
71		P45						$\overline{\text{CS2/A21}}$
72		P44						$\overline{\text{CS3/A20(MA12)}}$
73		P43						A _{19(MA11)}
74	V _{CC}							
75		P42						A _{18(MA10)}
76	V _{SS}							
77		P41						A _{17(MA9)}
78		P40						A _{16(MA8)}
79		P37						A _{15(MA7)/(D15)}
80		P36						A _{14(MA6)/(D14)}
81		P35						A _{13(MA5)/(D13)}
82		P34						A _{12(MA4)/(D12)}
83		P33						A _{11(MA3)/(D11)}
84		P32						A _{10(MA2)/(D10)}
85		P31						A _{9(MA1)/(D9)}
86		P124				OUTC34		
87		P123				OUTC33		
88		P122				OUTC32/ISRxD3		
89		P121				OUTC31/ISCLK3		
90		P120				OUTC30/ISTxD3		
91	V _{CC}							
92		P30						A _{8(MA0)/(D8)}
93	V _{SS}							
94		P27					AN27	A _{7(D7)}
95		P26					AN26	A _{6(D6)}
96		P25					AN25	A _{5(D5)}

NOTES:

1. Bus control pins in M32C/83T cannot be used.

Table 1.4 Pin Characteristics for 144-Pin Package (Continued)

Pin No	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin ⁽¹⁾
97		P24					AN24	A4(/D4)
98		P23					AN23	A3(/D3)
99		P22					AN22	A2(/D2)
100		P21					AN21	A1(/D1)
101		P20					AN20	A0(/D0)
102		P17	$\overline{\text{INT5}}$					D15
103		P16	$\overline{\text{INT4}}$					D14
104		P15	$\overline{\text{INT3}}$					D13
105		P14						D12
106		P13						D11
107		P12						D10
108		P11						D9
109		P10						D8
110		P07					AN07	D7
111		P06					AN06	D6
112		P05					AN05	D5
113		P04					AN04	D4
114		P114						
115		P113				OUTC13		
116		P112				INPC12/OUTC12/ISRxD1/BE1IN		
117		P111				INPC11/OUTC11/ISCLK1		
118		P110				OUTC10/ISTxD1/BE1OUT		
119		P03					AN03	D3
120		P02					AN02	D2
121		P01					AN01	D1
122		P00					AN00	D0
123		P157				INPC07	AN157	
124		P156				INPC06	AN156	
125		P155				INPC05/OUTC05	AN155	
126		P154				INPC04/OUTC04	AN154	
127		P153				INPC03	AN153	
128		P152				INPC02/ISRxD0/BE0IN	AN152	
129		P151				INPC01/OUTC01/ISCLK0	AN151	
130	Vss							
131		P150				INPC00/OUTC00/ISTxD0/BE0OUT	AN150	
132	Vcc							
133		P107	$\overline{\text{KI3}}$				AN7	
134		P106	$\overline{\text{KI2}}$				AN6	
135		P105	$\overline{\text{KI1}}$				AN5	
136		P104	$\overline{\text{KI0}}$				AN4	
137		P103					AN3	
138		P102					AN2	
139		P101					AN1	
140	AVss							
141		P100					AN0	
142	VREF							
143	AVCC							
144		P97			RxD4/SCL4/STxD4		$\overline{\text{ADTRG}}$	

NOTES:

1. Bus control pins in M32C/83T cannot be used.

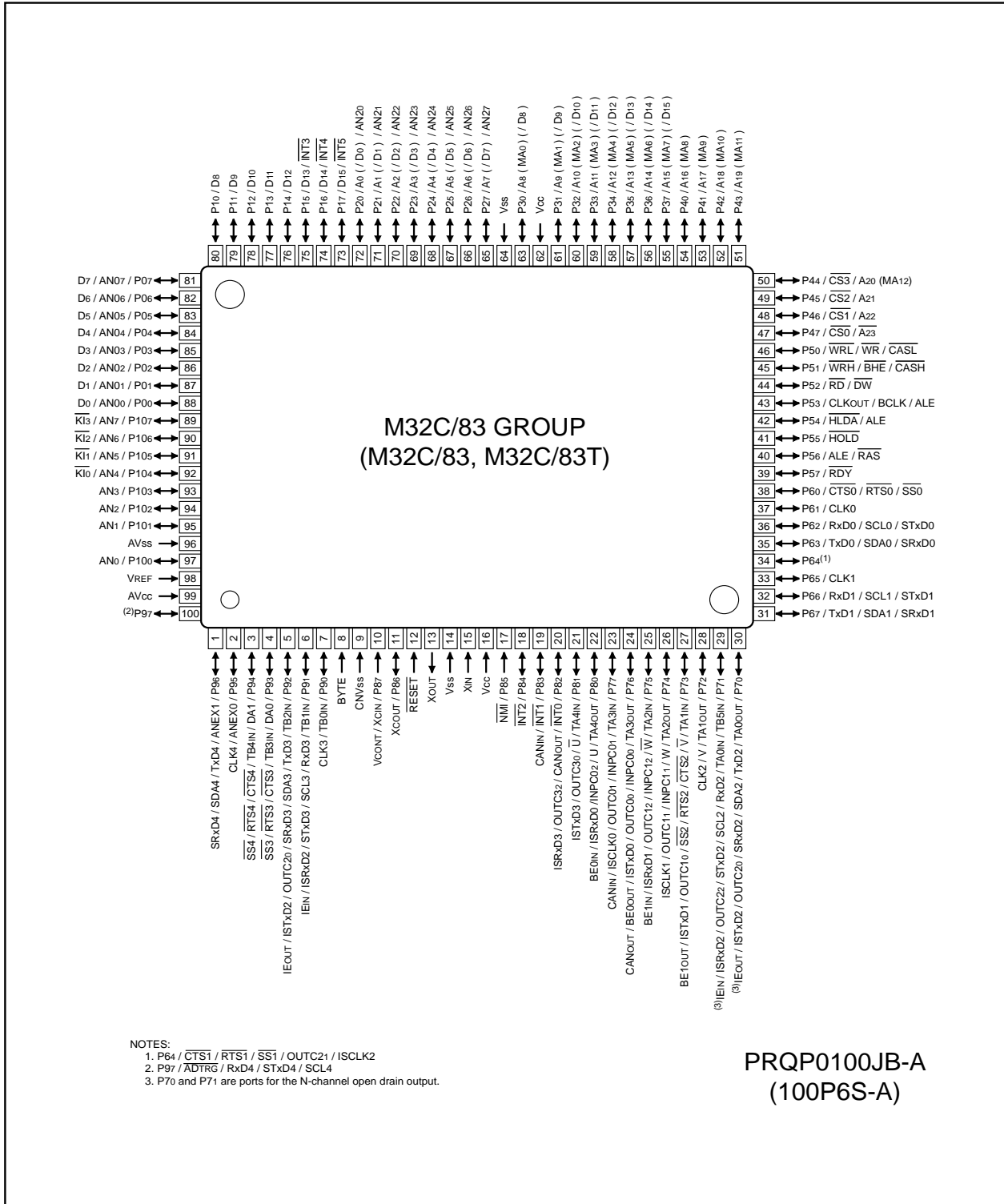


Figure 1.4 Pin Assignment for 100-Pin Package

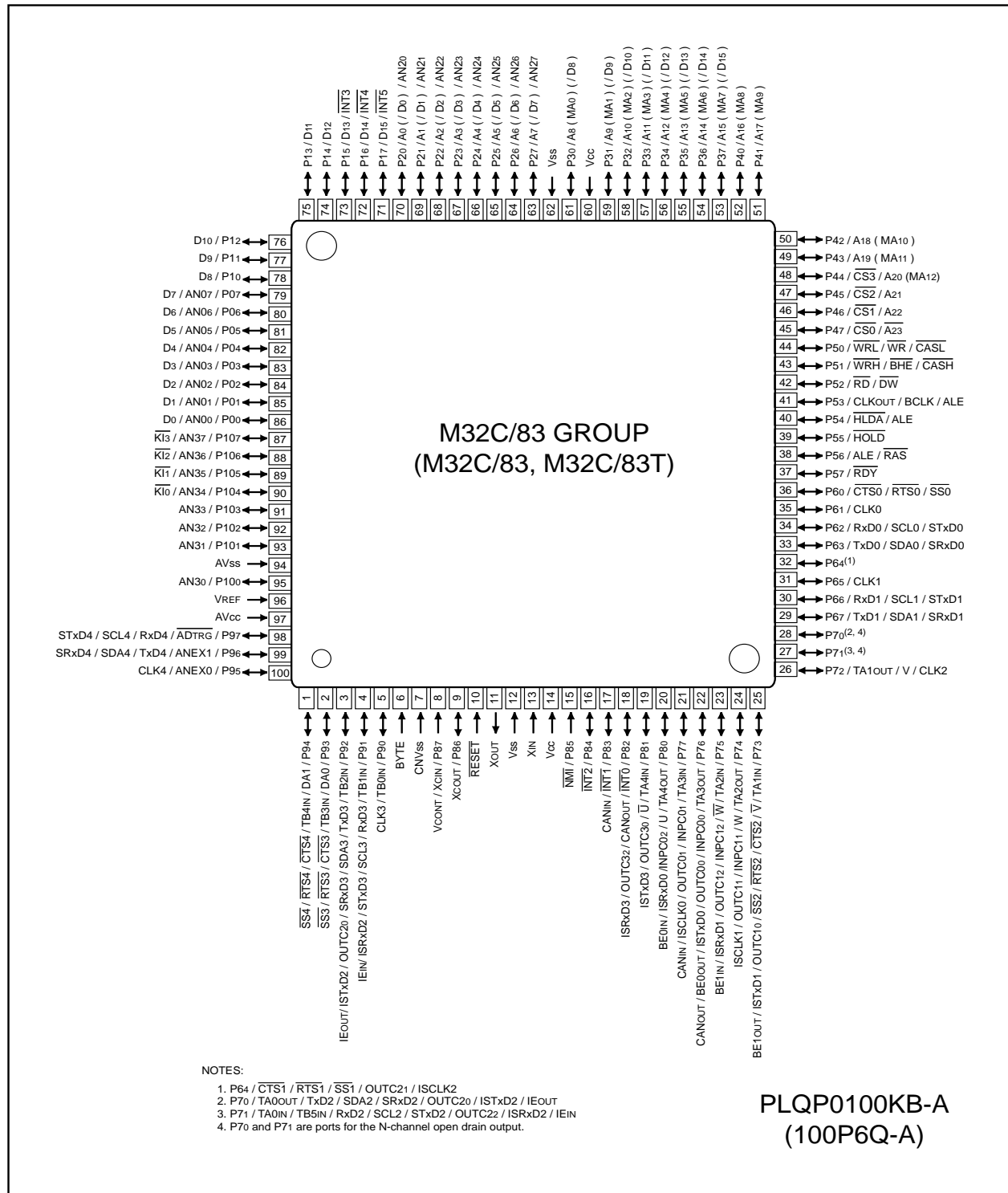


Figure 1.5 Pin Assignment for 100-Pin Package

Table 1.5 Pin Characteristics for 100-Pin Package

Package Pin No		Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin ⁽¹⁾
FP	GP								
1	99		P96			TxD4/SDA4/SRx4		ANEX1	
2	100		P95			CLK4		ANEX0	
3	1		P94		TB4IN	CTS4/RTS4/SS4		DA1	
4	2		P93		TB3IN	CTS3/RTS3/SS3		DA0	
5	3		P92		TB2IN	TxD3/SDA3/SRx3	OUTC2 ₀ /IE _{OUT} /ISTxD2		
6	4		P91		TB1IN	RxD3/SCL3/STxD3	IE _{IN} /ISRx2		
7	5		P90		TB0IN	CLK3			
8	6	BYTE							
9	7	CNV _{SS}							
10	8	X _{CIN} /V _{CONT}	P87						
11	9	X _{COU}	P86						
12	10	RESET							
13	11	X _{OU}							
14	12	V _{SS}							
15	13	X _{IN}							
16	14	V _{CC}							
17	15		P85	NMI					
18	16		P84	INT2					
19	17		P83	INT1		CAN _{IN}			
20	18		P82	INT0		CAN _{OUT}	OUTC3 ₂ /ISRx3		
21	19		P81		TA4 _{IN} /U		OUTC3 ₀ /ISTxD3		
22	20		P80		TA4 _{OUT} /U		INPC0 ₂ /ISRx0/BE0 _{IN}		
23	21		P77		TA3 _{IN}	CAN _{IN}	INPC0 ₁ /OUTC0 ₁ /ISCLK0		
24	22		P76		TA3 _{OUT}	CAN _{OUT}	INPC0 ₀ /OUTC0 ₀ /ISTxD0/BE0 _{OUT}		
25	23		P75		TA2 _{IN} /W		INPC1 ₂ /OUTC1 ₂ /ISRx1/BE1 _{IN}		
26	24		P74		TA2 _{OUT} /W		INPC1 ₁ /OUTC1 ₁ /ISCLK1		
27	25		P73		TA1 _{IN} /V	CTS2/RTS2/SS2	OUTC1 ₀ /ISTxD1/BE1 _{OUT}		
28	26		P72		TA1 _{OUT} /V	CLK2			
29	27		P71		TB5 _{IN} /TA0 _{IN}	RxD2/SCL2/STxD2	OUTC2 ₂ /ISRx2/IE _{IN}		
30	28		P70		TA0 _{OUT}	TxD2/SDA2/SRx2	OUTC2 ₀ /ISTxD2/IE _{OUT}		
31	29		P67			TxD1/SDA1/SRx1			
32	30		P66			RxD1/SCL1/STxD1			
33	31		P65			CLK1			
34	32		P64			CTS1/RTS1/SS1	OUTC2 ₁ /ISCLK2		
35	33		P63			TxD0/SDA0/SRx0			
36	34		P62			RxD0/SCL0/STxD0			
37	35		P61			CLK0			
38	36		P60			CTS0/RTS0/SS0			
39	37		P57						RDY
40	38		P56						ALE/RAS
41	39		P55						HOLD
42	40		P54						HLDA/ALE
43	41		P53						CLK _{OUT} /BCLK/ALE
44	42		P52						RD/DW
45	43		P51						WRH/BHE/CASH
46	44		P50						WRL/WR/CASL
47	45		P47						CS0/A23
48	46		P46						CS1/A22
49	47		P45						CS2/A21
50	48		P44						CS3/A20(MA12)

NOTES:

1. Bus control pins in M32C/83T cannot be used.

Table 1.5 Pin Characteristics for 100-Pin Package (Continued)

Package Pin No		Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin ⁽¹⁾
FP	GP								
51	49		P43					A19(MA11)	
52	50		P42					A18(MA10)	
53	51		P41					A17(MA9)	
54	52		P40					A16(MA8)	
55	53		P37					A15(MA7)/(D15)	
56	54		P36					A14(MA6)/(D14)	
57	55		P35					A13(MA5)/(D13)	
58	56		P34					A12(MA4)/(D12)	
59	57		P33					A11(MA3)/(D11)	
60	58		P32					A10(MA2)/(D10)	
61	59		P31					A9(MA1)/(D9)	
62	60	Vcc							
63	61		P30					A8(MA0)/(D8)	
64	62	Vss							
65	63		P27				AN27	A7(/D7)	
66	64		P26				AN26	A6(/D6)	
67	65		P25				AN25	A5(/D5)	
68	66		P24				AN24	A4(/D4)	
69	67		P23				AN23	A3(/D3)	
70	68		P22				AN22	A2(/D2)	
71	69		P21				AN21	A1(/D1)	
72	70		P20				AN20	A0(/D0)	
73	71		P17	INT5				D15	
74	72		P16	INT4				D14	
75	73		P15	INT3				D13	
76	74		P14					D12	
77	75		P13					D11	
78	76		P12					D10	
79	77		P11					D9	
80	78		P10					D8	
81	79		P07				AN07	D7	
82	80		P06				AN06	D6	
83	81		P05				AN05	D5	
84	82		P04				AN04	D4	
85	83		P03				AN03	D3	
86	84		P02				AN02	D2	
87	85		P01				AN01	D1	
88	86		P00				AN00	D0	
89	87		P107	K13			AN7		
90	88		P106	K12			AN6		
91	89		P105	K11			AN5		
92	90		P104	K10			AN4		
93	91		P103				AN3		
94	92		P102				AN2		
95	93		P101				AN1		
96	94	AVss							
97	95		P100				AN0		
98	96	VREF							
99	97	AVcc							
100	98		P97			RxD4/SCL4/STxD4	ADTRG		

NOTES:

1. Bus control pins in M32C/83T cannot be used.

1.6 Pin Description

Table 1.6 Pin Description (100-Pin and 144-Pin Packages)

Classification	Symbol	I/O Type	Function
Power Supply	Vcc Vss	I	Apply 3.0 to 5.5V to both Vcc pin. Apply 0V to the Vss pin. ⁽¹⁾
Analog Power Supply	AVcc AVss	I	Supplies power to the A/D converter. Connect the AVcc pin to Vcc and the AVss pin to Vss
Reset Input	RESET	I	The microcomputer is in a reset state when "L" is applied to the RESET pin
CNVss	CNVss	I	Switches processor mode. Connect the CNVss pin to Vss to start up in single-chip mode or to Vcc to start up in microprocessor mode
Input to Switch External Data Bus Width ⁽²⁾	BYTE	I	Switches data bus width in external memory space 3. The data bus is 16 bits wide when the BYTE pin is held "L" and 8 bits wide when it is held "H". Set to either. Connect the BYTE pin to Vss to use the microcomputer in single-chip mode
Bus Control Pins ⁽²⁾	D0 to D7	I/O	Inputs and outputs data (D0 to D7) while accessing an external memory space with separate bus
	D8 to D15	I/O	Inputs and outputs data (D8 to D15) while accessing an external memory space with 16-bit separate bus
	A0 to A22	O	Outputs address bits A0 to A22
	A ₂₃	O	Outputs inversed address bit A23
	A0/D0 to A7/D7	I/O	Inputs and outputs data (D0 to D7) and outputs 8 low-order address bits (A0 to A7) by time-sharing while accessing an external memory space with multiplexed bus
	A8/D8 to A15/D15	I/O	Inputs and outputs data (D8 to D15) and outputs 8 middle-order address bits (A8 to A15) by time-sharing while accessing an external memory space with 16-bit multiplexed bus
	CS0 to CS3	O	Outputs CS0 to CS3 that are chip-select signals specifying an external space
	WRL / WR WRH / BHE RD	O	Outputs WRL, WRH, (WR, BHE) and RD signals. WRL and WRH can be switched with WR and BHE by program <ul style="list-style-type: none"> ■ WRL, WRH and RD selected: If external data bus is 16 bits wide, data is written to an even address in external memory space when \overline{WRL} is held "L". Data is written to an odd address when \overline{WRH} is held "L". Data is read when \overline{RD} is held "L". ■ WR, BHE and RD selected: Data is written to external memory space when \overline{WR} is held "L". Data in an external memory space is read when RD is held "L". An odd address is accessed when BHE is held "L". Select \overline{WR}, BHE and RD for external 8-bit data bus.
	ALE	O	ALE is a signal latching the address
	HOLD	I	The microcomputer is placed in a hold state while the HOLD pin is held "L"
HLDA	O	Outputs an "L" signal while the microcomputer is placed in a hold state	
RDY	I	Bus is placed in a wait state while the \overline{RDY} pin is held "L"	
DRAM Bus Control Pin ⁽²⁾	MA0 to MA12	O	When DRAM area is accessed, outputs column and row addresses by time-sharing.
	DW	O	The DW signal becomes "L" when data is written to the DRAM area. CASL and CASH are signals indicating the timing to latch column addresses. The CASL signal becomes "L" when an even address is accessed. The CASH signal becomes "L" when an odd address is accessed. RAS is a signal latching row addresses.
	CASL		
	CASH		
	RAS		

I : Input O : Output I/O : Input and output

NOTES:

1. Apply 4.2 to 5.5V to the Vcc pin when using M32C/83T.
2. Bus control pins in M32C/83T cannot be used.

Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)

Classification	Symbol	I/O Type	Function
Main Clock Input	XIN	I	I/O pins for the main clock oscillation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT. To apply external clock, apply it to XIN and leave XOUT open
Main Clock Output	XOUT	O	
Sub Clock Input	XCIN	I	I/O pins for the sub clock oscillation circuit. Connect a crystal oscillator between XCIN and Xcout. To apply external clock, apply it to XCIN and leave Xcout open
Sub Clock Output	Xcout	O	
Low-Pass Filter Connect Pin for PLL Frequency Synthesizer Pin	VCONT		Connects the low-pass filter to the VCONT pin when using the PLL frequency synthesizer. Connect P86 to VSS to stabilize the PLL frequency.
BCLK Output ⁽¹⁾	BCLK	O	Outputs BCLK signal
Clock Output	CLKOUT	O	Outputs the clock having the same frequency as fc, f8 or f32
INT Interrupt Input	INT0 to INT5	I	Input pins for the INT interrupt
NMI Interrupt Input	NMI	I	Input pin for the NMI interrupt
Key Input Interrupt	KI0 to KI3	I	Input pins for the key input interrupt
Timer A	TA0OUT to TA4OUT	I/O	I/O pins for the timer A0 to A4 (TA0OUT is a pin for the N-channel open drain output.)
	TA0IN to TA4IN	I	Input pins for the timer A0 to A4
Timer B	TB0IN to TB5IN	I	Input pins for the timer B0 to B5
Three-phase Motor Control Timer Output	U, \bar{U} , V, \bar{V} , W, \bar{W}	O	Output pins for the three-phase motor control timer
Serial I/O	CTS0 to CTS4	I	Input pins for data transmission control
	RTS0 to RTS4	O	Output pins for data reception control
	CLK0 to CLK4	I/O	Inputs and outputs the transfer clock
	RxD0 to RxD4	I	Inputs serial data
	TxD0 to TxD4	O	Outputs serial data (TxD2 is a pin for the N-channel open drain output.)
I ² C Mode	SDA0 to SDA4	I/O	Inputs and outputs serial data (SDA2 is a pin for the N-channel open drain output.)
	SCL0 to SCL4		Inputs and outputs the transfer clock (SCL2 is a pin for the N-channel open drain output.)

I : Input O : Output I/O : Input and output

NOTE:

1. Bus control pins in M32C/83T cannot be used.

Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)

Classification	Symbol	I/O Type	Function	
Serial I/O Special Function	STxD0 to STxD4	O	Outputs serial data when slave mode is selected	
	SRxD0 to SRxD4	I	Inputs serial data when slave mode is selected	
	SS0 to SS4	I	Input pins to control serial I/O special function	
Reference Voltage Input	VREF	I	Applies reference voltage to the A/D converter and D/A converter	
A/D Converter	AN0 to AN7 AN00 to AN07 AN20 to AN27 AN150 to AN157	I	Analog input pins for the A/D converter	
	ADTRG	I	Input pin for an external A/D trigger	
	ANEX0	I/O	Extended analog input pin for the A/D converter and output pin in external op-amp connection mode	
	ANEX1	I	Extended analog input pin for the A/D converter	
D/A Converter	DA0, DA1	O	Output pin for the D/A converter	
Intelligent I/O	INPC00 to INPC02 INPC03 to INPC07 ⁽¹⁾ INPC11 to INPC12 INPC16 to INPC17 ⁽¹⁾	I	Input pins for the time measurement function	
	OUTC00 to OUTC02 OUTC04 to OUTC05 ⁽¹⁾ OUTC10 to OUTC12 OUTC13 to OUTC17 ⁽¹⁾ OUTC20 to OUTC22 OUTC23 to OUTC27 ⁽¹⁾ OUTC30 to OUTC32 OUTC31, OUTC33 to OUTC37 ⁽¹⁾	O	Output pins for the waveform generating function (OUTC20 and OUTC22 assigned to P70 and P71 are pins for the N-channel open drain output.)	
	ISCLK0 to ISCLK2 ISCLK3 ⁽¹⁾	I/O	Inputs and outputs the clock for the intelligent I/O communication function	
	ISRXD0 to ISRXD3	I	Inputs data for the intelligent I/O communication function	
	ISTXD0 to ISTXD3	O	Outputs data for the intelligent I/O communication function	
	BE0IN, BE1IN	I	Inputs data for the intelligent I/O communication function	
	BE0OUT, BE1OUT	O	Outputs data for the intelligent I/O communication function	
	IEIN	I	Inputs data for the intelligent I/O communication function	
	IEOUT	O	Outputs data for the intelligent I/O communication function	
	CAN	CANIN	I	Input pin for the CAN communication function
		CANOUT	O	Output pin for the CAN communication function

I : Input O : Output I/O : Input and output

NOTE:

1. Available in the 144-pin package only.

Table 1.6 Pin Description (144-Pin Package only) (Continued)

Classification	Symbol	I/O Type	Function
I/O Ports	P00 to P07 P10 to P17 P20 to P27 P30 to P37 P40 to P47 P50 to P57 P60 to P67 P70 to P77 P90 to P97 P100 to P107	I/O	8-bit I/O ports for CMOS. Each port can be programmed for input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resistor available in 4-bit units (P70 and P71 are ports for the N-channel open drain output.)
	P110 to P114 P120 to P127 P130 to P137 P140 to P146 P150 to P157 (1)	I/O	I/O ports having equivalent functions to P0
	P80 to P84 P86, P87	I/O	I/O ports having equivalent functions to P0
Input Port	P85	I	Shares a pin with NMI. NMI input state can be got by reading P85

I : Input O : Output I/O : Input and output

NOTE:

1. Available in the 144-pin package only.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers.

A register bank comprises 8 registers (R0, R1, R2, R3, A0, A1, SB and FB) out of 28 CPU registers. Two sets of register banks are provided.

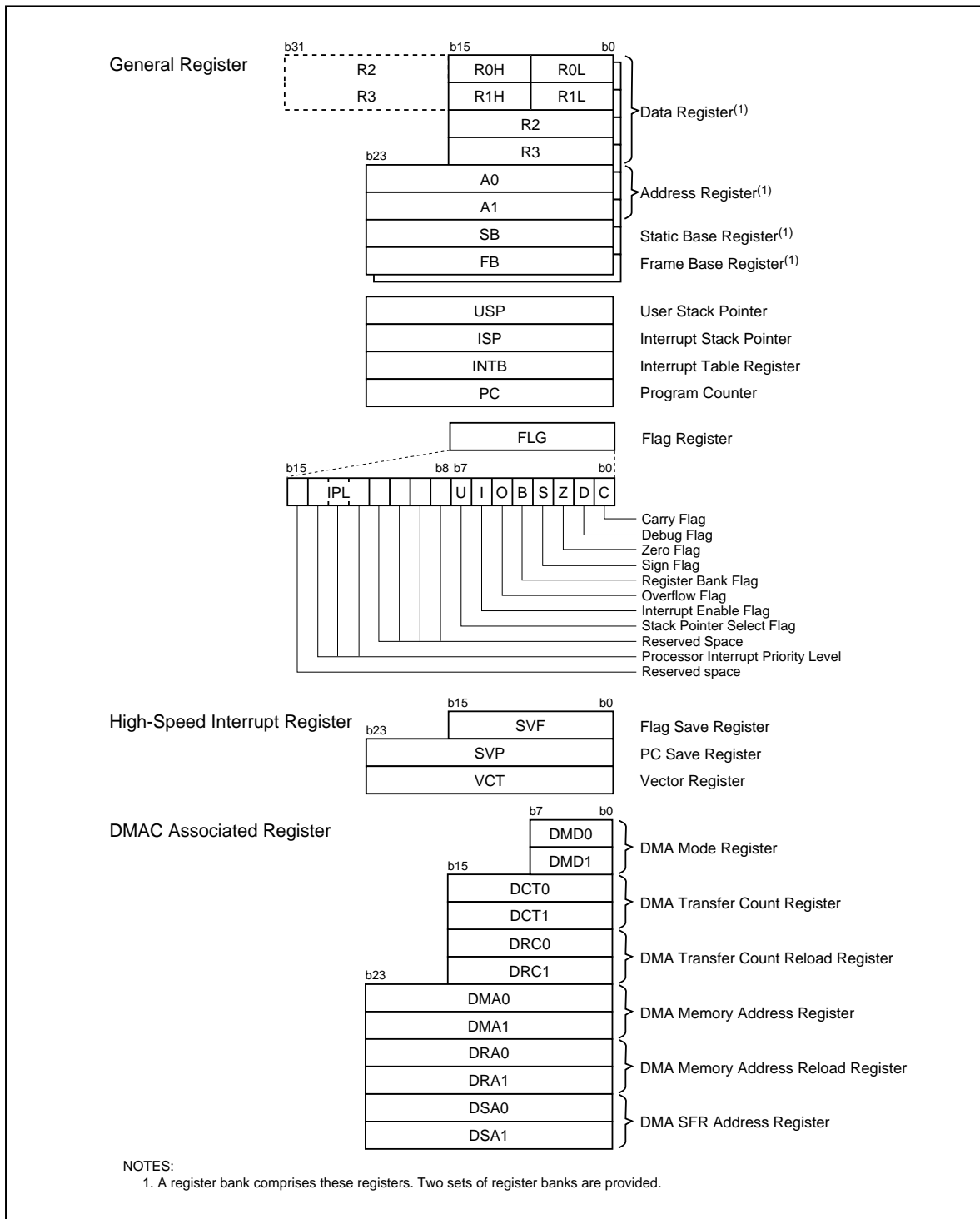


Figure 2.1 CPU Register

2.1 General Registers

2.1.1 Data Registers (R0, R1, R2 and R3)

R0, R1, R2 and R3 are 16-bit registers for transfer, arithmetic and logic operations. R0 and R1 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R0 can be combined with R2 to be used as a 32-bit data register (R2R0). The same applies to R1 and R3.

2.1.2 Address Registers (A0 and A1)

A0 and A1 are 24-bit registers for A0-/A1-indirect addressing, A0-/A1-relative addressing, transfer, arithmetic and logic operations.

2.1.3 Static Base Register (SB)

SB is a 24-bit register for SB-relative addressing.

2.1.4 Frame Base Register (FB)

FB is a 24-bit register for FB-relative addressing.

2.1.5 Program Counter (PC)

PC, 24 bits wide, indicates the address of an instruction to be executed.

2.1.6 Interrupt Table Register (INTB)

INTB is a 24-bit register indicating the starting address of an interrupt vector table.

2.1.7 User Stack Pointer (USP), Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are 24 bits wide each. The U flag is used to switch between USP and ISP. Refer to "2.1.8 Flag Register (FLG)" for details on the U flag. Set USP and ISP to even addresses to execute an interrupt sequence efficiently.

2.1.8 Flag Register (FLG)

FLG is a 16-bit register indicating a CPU state.

2.1.8.1 Carry Flag (C)

The C flag indicates whether carry or borrow has occurred after executing an instruction.

2.1.8.2 Debug Flag (D)

The D flag is for debug only. Set to "0".

2.1.8.3 Zero Flag (Z)

The Z flag is set to "1" when the value of zero is obtained from an arithmetic calculation; otherwise "0".

2.1.8.4 Sign Flag (S)

The S flag is set to "1" when a negative value is obtained from an arithmetic calculation; otherwise "0".

2.1.8.5 Register Bank Select Flag (B)

The register bank 0 is selected when the B flag is set to "0". The register bank 1 is selected when this flag is set to "1".

2.1.8.6 Overflow Flag (O)

The O flag is set to "1" when the result of an arithmetic operation overflows; otherwise "0".

2.1.8.7 Interrupt Enable Flag (I)

The I flag enables a maskable interrupt.

An interrupt is disabled when the I flag is set to "0" and enabled when the I flag is set to "1". The I flag is set to "0" when an interrupt is acknowledged.

2.1.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to "0". USP is selected when this flag is set to "1".

The U flag is set to "0" when a hardware interrupt is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.1.8.9 Processor Interrupt Priority Level (IPL)

IPL, 3 bits wide, assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has greater priority than IPL, the interrupt is enabled.

2.1.8.10 Reserved Space

When writing to a reserved space, set to "0". When read, its content is indeterminate.

2.2 High-Speed Interrupt Registers

Registers associated with the high-speed interrupt are as follows. Refer to **10.4 High-Speed Interrupt** for details.

- Flag save register (SVF)
- PC save register (SVP)
- Vector register (VCT)

2.3 DMAC-Associated Registers

Registers associated with DMAC are as follows. Refer to **12. DMAC** for details.

- DMA mode register (DMD0, DMD1)
- DMA transfer count register (DCT0, DCT1)
- DMA transfer count reload register (DRC0, DRC1)
- DMA memory address register (DMA0, DMA1)
- DMA SFR address register (DSA0, DSA1)
- DMA memory address reload register (DRA0, DRA1)

3. Memory

Figure 3.1 shows a memory map of the M32C/83 group (M32C/83, M32C/83T).

M32C/83 group (M32C/83, M32C/83T) provides 16-Mbyte address space from addresses 000000_{16} to $FFFFFF_{16}$.

The internal ROM is allocated lower addresses beginning with address $FFFFFF_{16}$. For example, a 64-Kbyte internal ROM is allocated addresses $FF0000_{16}$ to $FFFFFF_{16}$.

The fixed interrupt vectors are allocated addresses $FFFDC_{16}$ to $FFFFFF_{16}$. It stores the starting address of each interrupt routine. Refer to **10. Interrupts** for details.

The internal RAM is allocated higher addresses beginning with address 000400_{16} . For example, a 10-Kbyte internal RAM is allocated addresses 000400_{16} to $002BFF_{16}$. Besides storing data, it becomes stacks when the subroutine is called or an interrupt is acknowledged.

SFR, consisting of control registers for peripheral functions such as I/O port, A/D conversion, serial I/O, and timers, is allocated addresses 000000_{16} to $0003FF_{16}$. All addresses, which have nothing allocated within SFR, are reserved space and cannot be accessed by users.

The special page vectors are allocated addresses $FFFE00_{16}$ to $FFFDB_{16}$. It is used for the JMPS instruction and JSRS instruction. Refer to the Renesas publication **Software Manual** for details.

In memory expansion mode and microprocessor mode, some space are reserved and cannot be accessed by users.

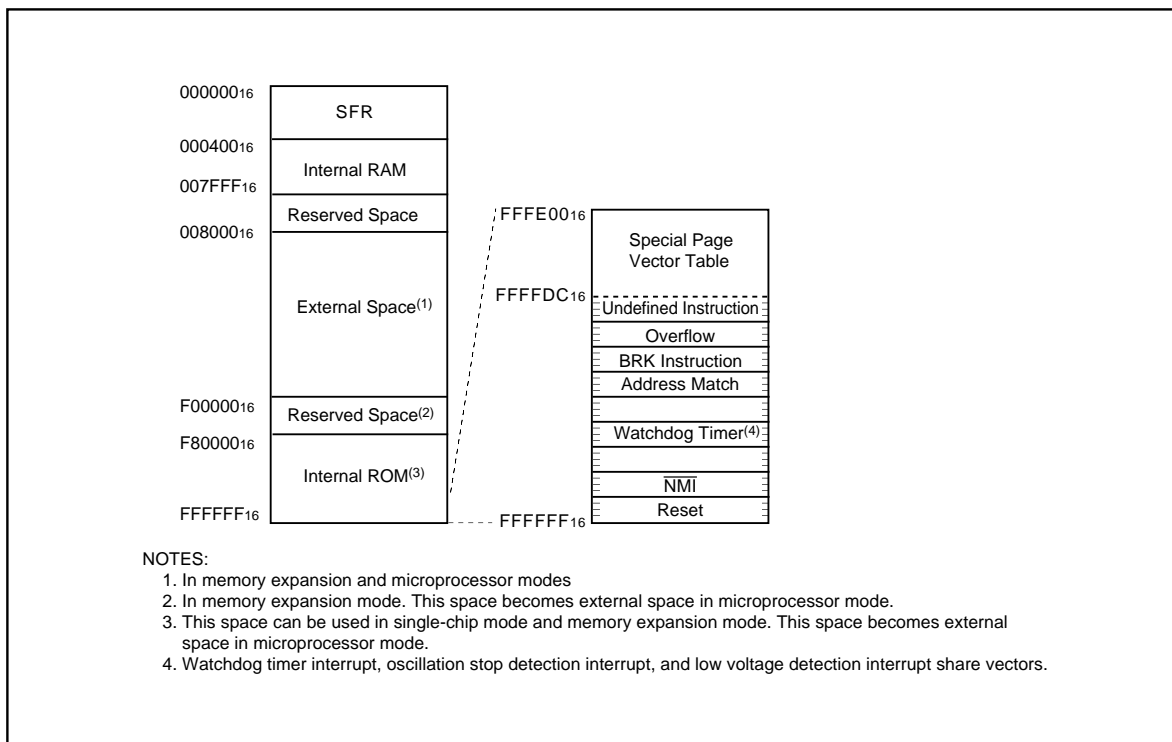


Figure 3.1 Memory Map

4. Special Function Registers (SFR)

Address	Register	Symbol	Value after RESET
0000 ₁₆			
0001 ₁₆			
0002 ₁₆			
0003 ₁₆			
0004 ₁₆	Processor Mode Register 0 ⁽¹⁾	PM0	1000 0000 ₂ (CNVss pin ="L") 0000 0011 ₂ (CNVss pin ="H")
0005 ₁₆	Processor Mode Register 1	PM1	0X00 0000 ₂
0006 ₁₆	System Clock Control Register 0	CM0	0000 X000 ₂
0007 ₁₆	System Clock Control Register 1	CM1	0010 0000 ₂
0008 ₁₆	Wait Control Register ⁽²⁾	WCR	1111 1111 ₂
0009 ₁₆	Address Match Interrupt Enable Register	AIER	XXXX 0000 ₂
000A ₁₆	Protect Register	PRCR	XXXX 0000 ₂
000B ₁₆	External Data Bus Width Control Register ⁽²⁾	DS	XXXX 1000 ₂ (BYTE pin ="L") XXXX 0000 ₂ (BYTE pin ="H")
000C ₁₆	Main Clock Division Register	MCD	XXXX0 1000 ₂
000D ₁₆	Oscillation Stop Detection Register	CM2	00 ₁₆
000E ₁₆	Watchdog Timer Start Register	WDTS	XX ₁₆
000F ₁₆	Watchdog Timer Control Register	WDC	000X XXXX ₂
0010 ₁₆			
0011 ₁₆	Address Match Interrupt Register 0	RMAD0	00 00 00 ₁₆
0012 ₁₆			
0013 ₁₆			
0014 ₁₆			
0015 ₁₆	Address Match Interrupt Register 1	RMAD1	00 00 00 ₁₆
0016 ₁₆			
0017 ₁₆	VDC Control Register for PLL	PLV	XXXX XX01 ₂
0018 ₁₆			
0019 ₁₆	Address Match Interrupt Register 2	RMAD2	00 00 00 ₁₆
001A ₁₆			
001B ₁₆	VDC Control Register 0	VDC0	00 ₁₆
001C ₁₆			
001D ₁₆	Address Match Interrupt Register 3	RMAD3	00 00 00 ₁₆
001E ₁₆			
001F ₁₆			
0020 ₁₆			
0021 ₁₆			
0022 ₁₆			
0023 ₁₆			
0024 ₁₆			
0025 ₁₆			
0026 ₁₆			
0027 ₁₆			
0028 ₁₆			
0029 ₁₆			
002A ₁₆			
002B ₁₆			
002C ₁₆			
002D ₁₆			
002E ₁₆			
002F ₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The PM00 and PM01 bits in the PM1 register maintain values set before reset even if software reset or watchdog timer reset is performed.
2. These registers in M32C/83T cannot be used.

Address	Register	Symbol	Value after RESET
0030 ₁₆			
0031 ₁₆			
0032 ₁₆			
0033 ₁₆			
0034 ₁₆			
0035 ₁₆			
0036 ₁₆			
0037 ₁₆			
0038 ₁₆			
0039 ₁₆			
003A ₁₆			
003B ₁₆			
003C ₁₆			
003D ₁₆			
003E ₁₆			
003F ₁₆			
0040 ₁₆	DRAM Control Register ⁽¹⁾	DRAMCONT	XX ₁₆
0041 ₁₆	DRAM Refresh Interval Set Register ⁽¹⁾	REFCNT	XX ₁₆
0042 ₁₆			
0043 ₁₆			
0044 ₁₆			
0045 ₁₆			
0046 ₁₆			
0047 ₁₆			
0048 ₁₆			
0049 ₁₆			
004A ₁₆			
004B ₁₆			
004C ₁₆			
004D ₁₆			
004E ₁₆			
004F ₁₆			
0050 ₁₆			
0051 ₁₆			
0052 ₁₆			
0053 ₁₆			
0054 ₁₆			
0055 ₁₆			
0056 ₁₆			
0057 ₁₆	Flash Memory Control Register 0	FMR0	XX00 0001 ₂
0058 ₁₆			
0059 ₁₆			
005A ₁₆			
005B ₁₆			
005C ₁₆			
005D ₁₆			
005E ₁₆			
005F ₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. These registers in M32C/83T cannot be used.

Address	Register	Symbol	Value after RESET
0060 ₁₆			
0061 ₁₆			
0062 ₁₆			
0063 ₁₆			
0064 ₁₆			
0065 ₁₆			
0066 ₁₆			
0067 ₁₆			
0068 ₁₆	DMA0 Interrupt Control Register	DM0IC	XXXX X000 ₂
0069 ₁₆	Timer B5 Interrupt Control Register	TB5IC	XXXX X000 ₂
006A ₁₆	DMA2 Interrupt Control Register	DM2IC	XXXX X000 ₂
006B ₁₆	UART2 Receive /ACK Interrupt Control Register	S2RIC	XXXX X000 ₂
006C ₁₆	Timer A0 Interrupt Control Register	TA0IC	XXXX X000 ₂
006D ₁₆	UART3 Receive /ACK Interrupt Control Register	S3RIC	XXXX X000 ₂
006E ₁₆	Timer A2 Interrupt Control Register	TA2IC	XXXX X000 ₂
006F ₁₆	UART4 Receive /ACK Interrupt Control Register	S4RIC	XXXX X000 ₂
0070 ₁₆	Timer A4 Interrupt Control Register	TA4IC	XXXX X000 ₂
0071 ₁₆	UART0/UART3 Bus Conflict Detect Interrupt Control Register	BCN0IC/BCN3IC	XXXX X000 ₂
0072 ₁₆	UART0 Receive/ACK Interrupt Control Register	S0RIC	XXXX X000 ₂
0073 ₁₆	A/D0 Conversion Interrupt Control Register	AD0IC	XXXX X000 ₂
0074 ₁₆	UART1 Receive/ACK Interrupt Control Register	S1RIC	XXXX X000 ₂
0075 ₁₆	Intelligent I/O Interrupt Control Register 0	IIO0IC	XXXX X000 ₂
0076 ₁₆	Timer B1 Interrupt Control Register	TB1IC	XXXX X000 ₂
0077 ₁₆	Intelligent I/O Interrupt Control Register 2	IIO2IC	XXXX X000 ₂
0078 ₁₆	Timer B3 Interrupt Control Register	TB3IC	XXXX X000 ₂
0079 ₁₆	Intelligent I/O Interrupt Control Register 4	IIO4IC	XXXX X000 ₂
007A ₁₆	INT5 Interrupt Control Register	INT5IC	XX00 X000 ₂
007B ₁₆	Intelligent I/O Interrupt Control Register 6	IIO6IC	XXXX X000 ₂
007C ₁₆	INT3 Interrupt Control Register	INT3IC	XX00 X000 ₂
007D ₁₆	Intelligent I/O Interrupt Control Register 8	IIO8IC	XXXX X000 ₂
007E ₁₆	INT1 Interrupt Control Register	INT1IC	XX00 X000 ₂
007F ₁₆	Intelligent I/O Interrupt Control Register 10/ CAN Interrupt 1 Control Register	IIO10IC CAN1IC	XXXX X000 ₂
0080 ₁₆			
0081 ₁₆	Intelligent I/O Interrupt Control Register 11/ CAN Interrupt 2 Control Register	IIO11IC CAN2IC	XXXX X000 ₂
0082 ₁₆			
0083 ₁₆			
0084 ₁₆			
0085 ₁₆			
0086 ₁₆	A/D1 Conversion Interrupt Control Register	AD1IC	XXXX X000 ₂
0087 ₁₆			
0088 ₁₆	DMA1 Interrupt Control Register	DM1IC	XXXX X000 ₂
0089 ₁₆	UART2 Transmit /NACK Interrupt Control Register	S2TIC	XXXX X000 ₂
008A ₁₆	DMA3 Interrupt Control Register	DM3IC	XXXX X000 ₂
008B ₁₆	UART3 Transmit /NACK Interrupt Control Register	S3TIC	XXXX X000 ₂
008C ₁₆	Timer A1 Interrupt Control Register	TA1IC	XXXX X000 ₂
008D ₁₆	UART4 Transmit /NACK Interrupt Control Register	S4TIC	XXXX X000 ₂
008E ₁₆	Timer A3 Interrupt Control Register	TA3IC	XXXX X000 ₂
008F ₁₆	UART2 Bus Conflict Detect Interrupt Control Register	BCN2IC	XXXX X000 ₂

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0090 ₁₆	UART0 Transmit /NACK Interrupt Control Register	S0TIC	XXXX X000 ₂
0091 ₁₆	UART1/UART4 Bus Conflict Detect Interrupt Control Register	BCN11C/BCN41C	XXXX X000 ₂
0092 ₁₆	UART1 Transmit/NACK Interrupt Control Register	S1TIC	XXXX X000 ₂
0093 ₁₆	Key Input Interrupt Control Register	KUPIC	XXXX X000 ₂
0094 ₁₆	Timer B0 Interrupt Control Register	TB0IC	XXXX X000 ₂
0095 ₁₆	Intelligent I/O Interrupt Control Register 1	IIO1IC	XXXX X000 ₂
0096 ₁₆	Timer B2 Interrupt Control Register	TB2IC	XXXX X000 ₂
0097 ₁₆	Intelligent I/O Interrupt Control Register 3	IIO3IC	XXXX X000 ₂
0098 ₁₆	Timer B4 Interrupt Control Register	TB4IC	XXXX X000 ₂
0099 ₁₆	Intelligent I/O Interrupt Control Register 5	IIO5IC	XXXX X000 ₂
009A ₁₆	INT4 Interrupt Control Register	INT4IC	XX00 X000 ₂
009B ₁₆	Intelligent I/O Interrupt Control Register 7	IIO7IC	XXXX X000 ₂
009C ₁₆	INT2 Interrupt Control Register	INT2IC	XX00 X000 ₂
009D ₁₆	Intelligent I/O Interrupt Control Register 9/ CAN Interrupt 0 Control Register	IIO9IC CAN0IC	XXXX X000 ₂
009E ₁₆	INT0 Interrupt Control Register	INT0IC	XX00 X000 ₂
009F ₁₆	Exit Priority Control Register	RLVL	XXXX 0000 ₂
00A0 ₁₆	Interrupt Request Register 0	IIO0IR	0000 000X ₂
00A1 ₁₆	Interrupt Request Register 1	IIO1IR	0000 000X ₂
00A2 ₁₆	Interrupt Request Register 2	IIO2IR	0000 000X ₂
00A3 ₁₆	Interrupt Request Register 3	IIO3IR	0000 000X ₂
00A4 ₁₆	Interrupt Request Register 4	IIO4IR	0000 000X ₂
00A5 ₁₆	Interrupt Request Register 5	IIO5IR	0000 000X ₂
00A6 ₁₆	Interrupt Request Register 6	IIO6IR	0000 000X ₂
00A7 ₁₆	Interrupt Request Register 7	IIO7IR	0000 000X ₂
00A8 ₁₆	Interrupt Request Register 8	IIO8IR	0000 000X ₂
00A9 ₁₆	Interrupt Request Register 9	IIO9IR	0000 000X ₂
00AA ₁₆	Interrupt Request Register 10	IIO10IR	0000 000X ₂
00AB ₁₆	Interrupt Request Register 11	IIO11IR	0000 000X ₂
00AC ₁₆			
00AD ₁₆			
00AE ₁₆			
00AF ₁₆			
00B0 ₁₆	Interrupt Enable Register 0	IIO0IE	00 ₁₆
00B1 ₁₆	Interrupt Enable Register 1	IIO1IE	00 ₁₆
00B2 ₁₆	Interrupt Enable Register 2	IIO2IE	00 ₁₆
00B3 ₁₆	Interrupt Enable Register 3	IIO3IE	00 ₁₆
00B4 ₁₆	Interrupt Enable Register 4	IIO4IE	00 ₁₆
00B5 ₁₆	Interrupt Enable Register 5	IIO5IE	00 ₁₆
00B6 ₁₆	Interrupt Enable Register 6	IIO6IE	00 ₁₆
00B7 ₁₆	Interrupt Enable Register 7	IIO7IE	00 ₁₆
00B8 ₁₆	Interrupt Enable Register 8	IIO8IE	00 ₁₆
00B9 ₁₆	Interrupt Enable Register 9	IIO9IE	00 ₁₆
00BA ₁₆	Interrupt Enable Register 10	IIO10IE	00 ₁₆
00BB ₁₆	Interrupt Enable Register 11	IIO11IE	00 ₁₆
00BC ₁₆			
00BD ₁₆			
00BE ₁₆			
00BF ₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
00C0 ₁₆ 00C1 ₁₆	Group 0 Time Measurement/Waveform Generating Register 0	G0TM0/G0PO0	XX ₁₆ XX ₁₆
00C2 ₁₆ 00C3 ₁₆	Group 0 Time Measurement/Waveform Generating Register 1	G0TM1/G0PO1	XX ₁₆ XX ₁₆
00C4 ₁₆ 00C5 ₁₆	Group 0 Time Measurement/Waveform Generating Register 2	G0TM2/G0PO2	XX ₁₆ XX ₁₆
00C6 ₁₆ 00C7 ₁₆	Group 0 Time Measurement/Waveform Generating Register 3	G0TM3/G0PO3	XX ₁₆ XX ₁₆
00C8 ₁₆ 00C9 ₁₆	Group 0 Time Measurement/Waveform Generating Register 4	G0TM4/G0PO4	XX ₁₆ XX ₁₆
00CA ₁₆ 00CB ₁₆	Group 0 Time Measurement/Waveform Generating Register 5	G0TM5/G0PO5	XX ₁₆ XX ₁₆
00CC ₁₆ 00CD ₁₆	Group 0 Time Measurement/Waveform Generating Register 6	G0TM6/G0PO6	XX ₁₆ XX ₁₆
00CE ₁₆ 00CF ₁₆	Group 0 Time Measurement/Waveform Generating Register 7	G0TM7/G0PO7	XX ₁₆ XX ₁₆
00D0 ₁₆	Group 0 Waveform Generating Control Register 0	G0POCR0	0X00 X0002
00D1 ₁₆	Group 0 Waveform Generating Control Register 1	G0POCR1	0X00 X0002
00D2 ₁₆	Group 0 Waveform Generating Control Register 2	G0POCR2	0X00 X0002
00D3 ₁₆	Group 0 Waveform Generating Control Register 3	G0POCR3	0X00 X0002
00D4 ₁₆	Group 0 Waveform Generating Control Register 4	G0POCR4	0X00 X0002
00D5 ₁₆	Group 0 Waveform Generating Control Register 5	G0POCR5	0X00 X0002
00D6 ₁₆	Group 0 Waveform Generating Control Register 6	G0POCR6	0X00 X0002
00D7 ₁₆	Group 0 Waveform Generating Control Register 7	G0POCR7	0X00 X0002
00D8 ₁₆	Group 0 Time Measurement Control Register 0	G0TMCR0	00 ₁₆
00D9 ₁₆	Group 0 Time Measurement Control Register 1	G0TMCR1	00 ₁₆
00DA ₁₆	Group 0 Time Measurement Control Register 2	G0TMCR2	00 ₁₆
00DB ₁₆	Group 0 Time Measurement Control Register 3	G0TMCR3	00 ₁₆
00DC ₁₆	Group 0 Time Measurement Control Register 4	G0TMCR4	00 ₁₆
00DD ₁₆	Group 0 Time Measurement Control Register 5	G0TMCR5	00 ₁₆
00DE ₁₆	Group 0 Time Measurement Control Register 6	G0TMCR6	00 ₁₆
00DF ₁₆	Group 0 Time Measurement Control Register 7	G0TMCR7	00 ₁₆
00E0 ₁₆ 00E1 ₁₆	Group 0 Base Timer Register	G0BT	XX ₁₆ XX ₁₆
00E2 ₁₆	Group 0 Base Timer Control Register 0	G0BCR0	00 ₁₆
00E3 ₁₆	Group 0 Base Timer Control Register 1	G0BCR1	00 ₁₆
00E4 ₁₆	Group 0 Time Measurement Prescaler Register 6	G0TPR6	00 ₁₆
00E5 ₁₆	Group 0 Time Measurement Prescaler Register 7	G0TPR7	00 ₁₆
00E6 ₁₆	Group 0 Function Enable Register	G0FE	00 ₁₆
00E7 ₁₆	Group 0 Function Select Register	G0FS	00 ₁₆
00E8 ₁₆ 00E9 ₁₆	Group 0 SI/O Receive Buffer Register	G0RB	XXXX XXXX ₂ XX00 XXXX ₂
00EA ₁₆ 00EB ₁₆	Group 0 Transmit Buffer/Receive Data Register	G0TB/G0DR	XX ₁₆
00EC ₁₆	Group 0 Receive Input Register	G0RI	XX ₁₆
00ED ₁₆	Group 0 SI/O Communication Mode Register	G0MR	00 ₁₆
00EE ₁₆	Group 0 Transmit Output Register	G0TO	XX ₁₆
00EF ₁₆	Group 0 SI/O Communication Control Register	G0CR	0000 X0002

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
00F0 ₁₆	Group 0 Data Compare Register 0	G0CMP0	XX ₁₆
00F1 ₁₆	Group 0 Data Compare Register 1	G0CMP1	XX ₁₆
00F2 ₁₆	Group 0 Data Compare Register 2	G0CMP2	XX ₁₆
00F3 ₁₆	Group 0 Data Compare Register 3	G0CMP3	XX ₁₆
00F4 ₁₆	Group 0 Data Mask Register 0	G0MSK0	XX ₁₆
00F5 ₁₆	Group 0 Data Mask Register 1	G0MSK1	XX ₁₆
00F6 ₁₆			
00F7 ₁₆			
00F8 ₁₆ 00F9 ₁₆	Group 0 Receive CRC Code Register	G0RCRC	XX ₁₆ XX ₁₆
00FA ₁₆ 00FB ₁₆	Group 0 Transmit CRC Code Register	G0TCRC	00 ₁₆ 00 ₁₆
00FC ₁₆	Group 0 SI/O Extended Mode Register	G0EMR	00 ₁₆
00FD ₁₆	Group 0 SI/O Extended Receive Control Register	G0ERC	00 ₁₆
00FE ₁₆	Group 0 SI/O Special Communication Interrupt Detect Register	G0IRF	0000 00XX ₂
00FF ₁₆	Group 0 SI/O Extended Transmit Control Register	G0ETC	0000 0XXX ₂
0100 ₁₆ 0101 ₁₆	Group 1 Time Measurement/Waveform Generating Register 0	G1TM0/G1PO0	XX ₁₆ XX ₁₆
0102 ₁₆ 0103 ₁₆	Group 1 Time Measurement/Waveform Generating Register 1	G1TM1/G1PO1	XX ₁₆ XX ₁₆
0104 ₁₆ 0105 ₁₆	Group 1 Time Measurement/Waveform Generating Register 2	G1TM2/G1PO2	XX ₁₆ XX ₁₆
0106 ₁₆ 0107 ₁₆	Group 1 Time Measurement/Waveform Generating Register 3	G1TM3/G1PO3	XX ₁₆ XX ₁₆
0108 ₁₆ 0109 ₁₆	Group 1 Time Measurement/Waveform Generating Register 4	G1TM4/G1PO4	XX ₁₆ XX ₁₆
010A ₁₆ 010B ₁₆	Group 1 Time Measurement/Waveform Generating Register 5	G1TM5/G1PO5	XX ₁₆ XX ₁₆
010C ₁₆ 010D ₁₆	Group 1 Time Measurement/Waveform Generating Register 6	G1TM6/G1PO6	XX ₁₆ XX ₁₆
010E ₁₆ 010F ₁₆	Group 1 Time Measurement/Waveform Generating Register 7	G1TM7/G1PO7	XX ₁₆ XX ₁₆
0110 ₁₆	Group 1 Waveform Generating Control Register 0	G1POCR0	0X00 X000 ₂
0111 ₁₆	Group 1 Waveform Generating Control Register 1	G1POCR1	0X00 X000 ₂
0112 ₁₆	Group 1 Waveform Generating Control Register 2	G1POCR2	0X00 X000 ₂
0113 ₁₆	Group 1 Waveform Generating Control Register 3	G1POCR3	0X00 X000 ₂
0114 ₁₆	Group 1 Waveform Generating Control Register 4	G1POCR4	0X00 X000 ₂
0115 ₁₆	Group 1 Waveform Generating Control Register 5	G1POCR5	0X00 X000 ₂
0116 ₁₆	Group 1 Waveform Generating Control Register 6	G1POCR6	0X00 X000 ₂
0117 ₁₆	Group 1 Waveform Generating Control Register 7	G1POCR7	0X00 X000 ₂
0118 ₁₆	Group 1 Time Measurement Control Register 0	G1TMCR0	00 ₁₆
0119 ₁₆	Group 1 Time Measurement Control Register 1	G1TMCR1	00 ₁₆
011A ₁₆	Group 1 Time Measurement Control Register 2	G1TMCR2	00 ₁₆
011B ₁₆	Group 1 Time Measurement Control Register 3	G1TMCR3	00 ₁₆
011C ₁₆	Group 1 Time Measurement Control Register 4	G1TMCR4	00 ₁₆
011D ₁₆	Group 1 Time Measurement Control Register 5	G1TMCR5	00 ₁₆
011E ₁₆	Group 1 Time Measurement Control Register 6	G1TMCR6	00 ₁₆
011F ₁₆	Group 1 Time Measurement Control Register 7	G1TMCR7	00 ₁₆

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0120 ₁₆ 0121 ₁₆	Group 1 Base Timer Register	G1BT	XX ₁₆ XX ₁₆
0122 ₁₆	Group 1 Base Timer Control Register 0	G1BCR0	00 ₁₆
0123 ₁₆	Group 1 Base Timer Control Register 1	G1BCR1	00 ₁₆
0124 ₁₆	Group 1 Time Measurement Prescaler Register 6	G1TPR6	00 ₁₆
0125 ₁₆	Group 1 Time Measurement Prescaler Register 7	G1TPR7	00 ₁₆
0126 ₁₆	Group 1 Function Enable Register	G1FE	00 ₁₆
0127 ₁₆	Group 1 Function Select Register	G1FS	00 ₁₆
0128 ₁₆ 0129 ₁₆	Group 1 SI/O Receive Buffer Register	G1RB	XXXX XXXX ₂ XX00 XXXX ₂
012A ₁₆ 012B ₁₆	Group 1 Transmit Buffer/Receive Data Register	G1TB/G1DR	XX ₁₆
012C ₁₆	Group 1 Receive Input Register	G1RI	XX ₁₆
012D ₁₆	Group 1 SI/O Communication Mode Register	G1MR	00 ₁₆
012E ₁₆	Group 1 Transmit Output Register	G1TO	XX ₁₆
012F ₁₆	Group 1 SI/O Communication Control Register	G1CR	0000 X000 ₂
0130 ₁₆	Group 1 Data Compare Register 0	G1CMP0	XX ₁₆
0131 ₁₆	Group 1 Data Compare Register 1	G1CMP1	XX ₁₆
0132 ₁₆	Group 1 Data Compare Register 2	G1CMP2	XX ₁₆
0133 ₁₆	Group 1 Data Compare Register 3	G1CMP3	XX ₁₆
0134 ₁₆	Group 1 Data Mask Register 0	G1MSK0	XX ₁₆
0135 ₁₆	Group 1 Data Mask Register 1	G1MSK1	XX ₁₆
0136 ₁₆			
0137 ₁₆			
0138 ₁₆ 0139 ₁₆	Group 1 Receive CRC Code Register	G1RCRC	XX ₁₆ XX ₁₆
013A ₁₆ 013B ₁₆	Group 1 Transmit CRC Code Register	G1TCRC	00 ₁₆ 00 ₁₆
013C ₁₆	Group 1 SI/O Extended Mode Register	G1EMR	00 ₁₆
013D ₁₆	Group 1 SI/O Extended Receive Control Register	G1ERC	00 ₁₆
013E ₁₆	Group 1 SI/O Special Communication Interrupt Detect Register	G1IRF	0000 00XX ₂
013F ₁₆	Group 1 SI/O Extended Transmit Control Register	G1ETC	0000 0XXX ₂
0140 ₁₆ 0141 ₁₆	Group 2 Waveform Generating Register 0	G2PO0	XX ₁₆ XX ₁₆
0142 ₁₆ 0143 ₁₆	Group 2 Waveform Generating Register 1	G2PO1	XX ₁₆ XX ₁₆
0144 ₁₆ 0145 ₁₆	Group 2 Waveform Generating Register 2	G2PO2	XX ₁₆ XX ₁₆
0146 ₁₆ 0147 ₁₆	Group 2 Waveform Generating Register 3	G2PO3	XX ₁₆ XX ₁₆
0148 ₁₆ 0149 ₁₆	Group 2 Waveform Generating Register 4	G2PO4	XX ₁₆ XX ₁₆
014A ₁₆ 014B ₁₆	Group 2 Waveform Generating Register 5	G2PO5	XX ₁₆ XX ₁₆
014C ₁₆ 014D ₁₆	Group 2 Waveform Generating Register 6	G2PO6	XX ₁₆ XX ₁₆
014E ₁₆ 014F ₁₆	Group 2 Waveform Generating Register 7	G2PO7	XX ₁₆ XX ₁₆

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Address	Register	Symbol	Value after RESET
0150 ₁₆	Group 2 Waveform Generating Control Register 0	G2POCR0	00 ₁₆
0151 ₁₆	Group 2 Waveform Generating Control Register 1	G2POCR1	00 ₁₆
0152 ₁₆	Group 2 Waveform Generating Control Register 2	G2POCR2	00 ₁₆
0153 ₁₆	Group 2 Waveform Generating Control Register 3	G2POCR3	00 ₁₆
0154 ₁₆	Group 2 Waveform Generating Control Register 4	G2POCR4	00 ₁₆
0155 ₁₆	Group 2 Waveform Generating Control Register 5	G2POCR5	00 ₁₆
0156 ₁₆	Group 2 Waveform Generating Control Register 6	G2POCR6	00 ₁₆
0157 ₁₆	Group 2 Waveform Generating Control Register 7	G2POCR7	00 ₁₆
0158 ₁₆			
0159 ₁₆			
015A ₁₆			
015B ₁₆			
015C ₁₆			
015D ₁₆			
015E ₁₆			
015F ₁₆			
0160 ₁₆	Group 2 Base Timer Register	G2BT	XX ₁₆
0161 ₁₆			XX ₁₆
0162 ₁₆	Group 2 Base Timer Control Register 0	G2BCR0	00 ₁₆
0163 ₁₆	Group 2 Base Timer Control Register 1	G2BCR1	00 ₁₆
0164 ₁₆	Base Timer Start Register	BTSR	XXXX 0000 ₂
0165 ₁₆			
0166 ₁₆	Group 2 Function Enable Register	G2FE	00 ₁₆
0167 ₁₆	Group 2 RTP Output Buffer Register	G2RTP	00 ₁₆
0168 ₁₆			
0169 ₁₆			
016A ₁₆	Group 2 SI/O Communication Mode Register	G2MR	00XX X000 ₂
016B ₁₆	Group 2 SI/O Communication Control Register	G2CR	0000 X000 ₂
016C ₁₆	Group 2 SI/O Transmit Buffer Register	G2TB	XX ₁₆
016D ₁₆			XX ₁₆
016E ₁₆	Group 2 SI/O Receive Buffer Register	G2RB	XX ₁₆
016F ₁₆			XX ₁₆
0170 ₁₆	Group 2 IEBus Address Register	IEAR	XX ₁₆
0171 ₁₆			XX ₁₆
0172 ₁₆	Group 2 IEBus Control Register	IECR	00XX X000 ₂
0173 ₁₆	Group 2 IEBus Transmit Interrupt Cause Detect Register	IETIF	XXX0 0000 ₂
0174 ₁₆	Group 2 IEBus Receive Interrupt Cause Detect Register	IERIF	XXX0 0000 ₂
0175 ₁₆			
0176 ₁₆			
0177 ₁₆			
0178 ₁₆	Input Function Select Register	IPS	00 ₁₆
0179 ₁₆			
017A ₁₆	Group 3 SI/O Communication Mode Register	G3MR	00XX 0000 ₂
017B ₁₆	Group 3 SI/O Communication Control Register	G3CR	0000 X000 ₂
017C ₁₆	Group 3 SI/O Transmit Buffer Register	G3TB	XX ₁₆
017D ₁₆			XX ₁₆
017E ₁₆	Group 3 SI/O Receive Buffer Register	G3RB	XX ₁₆
017F ₁₆			XX ₁₆

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Address	Register	Symbol	Value after RESET
0180 ₁₆ 0181 ₁₆	Group 3 Waveform Generating Register 0	G3PO0	XX ₁₆ XX ₁₆
0182 ₁₆ 0183 ₁₆	Group 3 Waveform Generating Register 1	G3PO1	XX ₁₆ XX ₁₆
0184 ₁₆ 0185 ₁₆	Group 3 Waveform Generating Register 2	G3PO2	XX ₁₆ XX ₁₆
0186 ₁₆ 0187 ₁₆	Group 3 Waveform Generating Register 3	G3PO3	XX ₁₆ XX ₁₆
0188 ₁₆ 0189 ₁₆	Group 3 Waveform Generating Register 4	G3PO4	XX ₁₆ XX ₁₆
018A ₁₆ 018B ₁₆	Group 3 Waveform Generating Register 5	G3PO5	XX ₁₆ XX ₁₆
018C ₁₆ 018D ₁₆	Group 3 Waveform Generating Register 6	G3PO6	XX ₁₆ XX ₁₆
018E ₁₆ 018F ₁₆	Group 3 Waveform Generating Register 7	G3PO7	XX ₁₆ XX ₁₆
0190 ₁₆	Group 3 Waveform Generating Control Register 0	G3POCR0	00 ₁₆
0191 ₁₆	Group 3 Waveform Generating Control Register 1	G3POCR1	00 ₁₆
0192 ₁₆	Group 3 Waveform Generating Control Register 2	G3POCR2	00 ₁₆
0193 ₁₆	Group 3 Waveform Generating Control Register 3	G3POCR3	00 ₁₆
0194 ₁₆	Group 3 Waveform Generating Control Register 4	G3POCR4	00 ₁₆
0195 ₁₆	Group 3 Waveform Generating Control Register 5	G3POCR5	00 ₁₆
0196 ₁₆	Group 3 Waveform Generating Control Register 6	G3POCR6	00 ₁₆
0197 ₁₆	Group 3 Waveform Generating Control Register 7	G3POCR7	00 ₁₆
0198 ₁₆ 0199 ₁₆	Group 3 Waveform Generating Mask Register 4	G3MK4	XX ₁₆ XX ₁₆
019A ₁₆ 019B ₁₆	Group 3 Waveform Generating Mask Register 5	G3MK5	XX ₁₆ XX ₁₆
019C ₁₆ 019D ₁₆	Group 3 Waveform Generating Mask Register 6	G3MK6	XX ₁₆ XX ₁₆
019E ₁₆ 019F ₁₆	Group 3 Waveform Generating Mask Register 7	G3MK7	XX ₁₆ XX ₁₆
01A0 ₁₆ 01A1 ₁₆	Group 3 Base Timer Register	G3BT	XX ₁₆ XX ₁₆
01A2 ₁₆	Group 3 Base Timer Control Register 0	G3BCR0	00 ₁₆
01A3 ₁₆	Group 3 Base Timer Control Register 1	G3BCR1	00 ₁₆
01A4 ₁₆			
01A5 ₁₆			
01A6 ₁₆	Group 3 Function Enable Register	G3FE	00 ₁₆
01A7 ₁₆	Group 3 RTP Output Buffer Register	G3RTP	00 ₁₆
01A8 ₁₆			
01A9 ₁₆			
01AA ₁₆			
01AB ₁₆			
01AC ₁₆			
01AD ₁₆	Group 3 SI/O Communication Flag Register	G3FLG	XXXX XXX0 ₂
01AE ₁₆			
01AF ₁₆			

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Address	Register	Symbol	Value after RESET
01B0 ₁₆			
01B1 ₁₆			
01B2 ₁₆			
01B3 ₁₆			
01B4 ₁₆			
01B5 ₁₆			
01B6 ₁₆			
01B7 ₁₆			
01B8 ₁₆			
01B9 ₁₆			
01BA ₁₆			
01BB ₁₆			
01BC ₁₆			
01BD ₁₆			
01BE ₁₆			
01BF ₁₆			
01C0 ₁₆ 01C1 ₁₆	A/D1 Register 0	AD10	XX ₁₆ XX ₁₆
01C2 ₁₆ 01C3 ₁₆	A/D1 Register 1	AD11	XX ₁₆ XX ₁₆
01C4 ₁₆ 01C5 ₁₆	A/D1 Register 2	AD12	XX ₁₆ XX ₁₆
01C6 ₁₆ 01C7 ₁₆	A/D1 Register 3	AD13	XX ₁₆ XX ₁₆
01C8 ₁₆ 01C9 ₁₆	A/D1 Register 4	AD14	XX ₁₆ XX ₁₆
01CA ₁₆ 01CB ₁₆	A/D1 Register 5	AD15	XX ₁₆ XX ₁₆
01CC ₁₆ 01CD ₁₆	A/D1 Register 6	AD16	XX ₁₆ XX ₁₆
01CE ₁₆ 01CF ₁₆	A/D1 Register 7	AD17	XX ₁₆ XX ₁₆
01D0 ₁₆			
01D1 ₁₆			
01D2 ₁₆			
01D3 ₁₆			
01D4 ₁₆ 01D5 ₁₆	A/D1 Control Register 2	AD1CON2	X00X X000 ₂
01D6 ₁₆	A/D1 Control Register 0	AD1CON0	00 ₁₆
01D7 ₁₆	A/D1 Control Register 1	AD1CON1	XX00 0000 ₂
01D8 ₁₆			
01D9 ₁₆			
01DA ₁₆			
01DB ₁₆			
01DC ₁₆			
01DD ₁₆			
01DE ₁₆			
01DF ₁₆			

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Address	Register	Symbol	Value after RESET
01E0 ₁₆	CAN0 Message Slot Buffer 0 Standard ID0	C0SLOT0_0	XX ₁₆
01E1 ₁₆	CAN0 Message Slot Buffer 0 Standard ID1	C0SLOT0_1	XX ₁₆
01E2 ₁₆	CAN0 Message Slot Buffer 0 Extended ID0	C0SLOT0_2	XX ₁₆
01E3 ₁₆	CAN0 Message Slot Buffer 0 Extended ID1	C0SLOT0_3	XX ₁₆
01E4 ₁₆	CAN0 Message Slot Buffer 0 Extended ID2	C0SLOT0_4	XX ₁₆
01E5 ₁₆	CAN0 Message Slot Buffer 0 Data Length Code	C0SLOT0_5	XX ₁₆
01E6 ₁₆	CAN0 Message Slot Buffer 0 Data 0	C0SLOT0_6	XX ₁₆
01E7 ₁₆	CAN0 Message Slot Buffer 0 Data 1	C0SLOT0_7	XX ₁₆
01E8 ₁₆	CAN0 Message Slot Buffer 0 Data 2	C0SLOT0_8	XX ₁₆
01E9 ₁₆	CAN0 Message Slot Buffer 0 Data 3	C0SLOT0_9	XX ₁₆
01EA ₁₆	CAN0 Message Slot Buffer 0 Data 4	C0SLOT0_10	XX ₁₆
01EB ₁₆	CAN0 Message Slot Buffer 0 Data 5	C0SLOT0_11	XX ₁₆
01EC ₁₆	CAN0 Message Slot Buffer 0 Data 6	C0SLOT0_12	XX ₁₆
01ED ₁₆	CAN0 Message Slot Buffer 0 Data 7	C0SLOT0_13	XX ₁₆
01EE ₁₆	CAN0 Message Slot Buffer 0 Time Stamp High-Order	C0SLOT0_14	XX ₁₆
01EF ₁₆	CAN0 Message Slot Buffer 0 Time Stamp Low-Order	C0SLOT0_15	XX ₁₆
01F0 ₁₆	CAN0 Message Slot Buffer 1 Standard ID0	C0SLOT1_0	XX ₁₆
01F1 ₁₆	CAN0 Message Slot Buffer 1 Standard ID1	C0SLOT1_1	XX ₁₆
01F2 ₁₆	CAN0 Message Slot Buffer 1 Extended ID0	C0SLOT1_2	XX ₁₆
01F3 ₁₆	CAN0 Message Slot Buffer 1 Extended ID1	C0SLOT1_3	XX ₁₆
01F4 ₁₆	CAN0 Message Slot Buffer 1 Extended ID2	C0SLOT1_4	XX ₁₆
01F5 ₁₆	CAN0 Message Slot Buffer 1 Data Length Code	C0SLOT1_5	XX ₁₆
01F6 ₁₆	CAN0 Message Slot Buffer 1 Data 0	C0SLOT1_6	XX ₁₆
01F7 ₁₆	CAN0 Message Slot Buffer 1 Data 1	C0SLOT1_7	XX ₁₆
01F8 ₁₆	CAN0 Message Slot Buffer 1 Data 2	C0SLOT1_8	XX ₁₆
01F9 ₁₆	CAN0 Message Slot Buffer 1 Data 3	C0SLOT1_9	XX ₁₆
01FA ₁₆	CAN0 Message Slot Buffer 1 Data 4	C0SLOT1_10	XX ₁₆
01FB ₁₆	CAN0 Message Slot Buffer 1 Data 5	C0SLOT1_11	XX ₁₆
01FC ₁₆	CAN0 Message Slot Buffer 1 Data 6	C0SLOT1_12	XX ₁₆
01FD ₁₆	CAN0 Message Slot Buffer 1 Data 7	C0SLOT1_13	XX ₁₆
01FE ₁₆	CAN0 Message Slot Buffer 1 Time Stamp High-Order	C0SLOT1_14	XX ₁₆
01FF ₁₆	CAN0 Message Slot Buffer 1 Time Stamp Low-Order	C0SLOT1_15	XX ₁₆
0200 ₁₆ 0201 ₁₆	CAN0 Control Register 0	C0CTRL0	XX01 0X01 ₂ ⁽¹⁾ XXXX 0000 ₂ ⁽¹⁾
0202 ₁₆ 0203 ₁₆	CAN0 Status Register	C0STR	0000 0000 ₂ ⁽¹⁾ X000 0X01 ₂ ⁽¹⁾
0204 ₁₆ 0205 ₁₆	CAN0 Extended ID Register	C0IDR	00 ₁₆ ⁽¹⁾ 00 ₁₆ ⁽¹⁾
0206 ₁₆ 0207 ₁₆	CAN0 Configuration Register	C0CONR	0000 XXXX ₂ ⁽¹⁾ 0000 0000 ₂ ⁽¹⁾
0208 ₁₆ 0209 ₁₆	CAN0 Time Stamp Register	C0TSR	00 ₁₆ ⁽¹⁾ 00 ₁₆ ⁽¹⁾
020A ₁₆	CAN0 Transmit Error Count Register	C0TEC	00 ₁₆ ⁽¹⁾
020B ₁₆	CAN0 Receive Error Count Register	C0REC	00 ₁₆ ⁽¹⁾
020C ₁₆ 020D ₁₆	CAN0 Slot Interrupt Status Register	C0SISTR	00 ₁₆ ⁽¹⁾ 00 ₁₆ ⁽¹⁾
020E ₁₆			
020F ₁₆			

X: Indeterminate

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NOTES:

1. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Address	Register	Symbol	Value after RESET
0210 ₁₆	CAN0 Slot Interrupt Mask Register	C0SIMKR	00 ₁₆ ⁽²⁾
0211 ₁₆			00 ₁₆ ⁽²⁾
0212 ₁₆			
0213 ₁₆			
0214 ₁₆	CAN0 Error Interrupt Mask Register	C0EIMKR	XXXX X000 ₂ ⁽²⁾
0215 ₁₆	CAN0 Error Interrupt Status Register	C0EISTR	XXXX X000 ₂ ⁽²⁾
0216 ₁₆			
0217 ₁₆	CAN0 Baud Rate Prescaler	C0BRP	0000 0001 ₂ ⁽²⁾
0218 ₁₆			
0219 ₁₆			
021A ₁₆			
021B ₁₆			
021C ₁₆			
021D ₁₆			
021E ₁₆			
021F ₁₆			
0220 ₁₆			
0221 ₁₆			
0222 ₁₆			
0223 ₁₆			
0224 ₁₆			
0225 ₁₆			
0226 ₁₆			
0227 ₁₆			
0228 ₁₆	CAN0 Global Mask Register Standard ID0	C0GMR0	XXX0 0000 ₂ ⁽²⁾
0229 ₁₆	CAN0 Global Mask Register Standard ID1	C0GMR1	XX00 0000 ₂ ⁽²⁾
022A ₁₆	CAN0 Global Mask Register Extended ID0	C0GMR2	XXXX 0000 ₂ ⁽²⁾
022B ₁₆	CAN0 Global Mask Register Extended ID1	C0GMR3	00 ₁₆ ⁽²⁾
022C ₁₆	CAN0 Global Mask Register Extended ID2	C0GMR4	XX00 0000 ₂ ⁽²⁾
022D ₁₆			
022E ₁₆			
022F ₁₆			
0230 ₁₆	CAN0 Message Slot 0 Control Register / CAN0 Local Mask Register A Standard ID0	C0MCTL0/ C0LMAR0	0000 0000 ₂ ⁽²⁾ XXX0 0000 ₂ ⁽²⁾
0231 ₁₆	CAN0 Message Slot 1 Control Register / CAN0 Local Mask Register A Standard ID1	C0MCTL1/ C0LMAR1	0000 0000 ₂ ⁽²⁾ XX00 0000 ₂ ⁽²⁾
0232 ₁₆	CAN0 Message Slot 2 Control Register / CAN0 Local Mask Register A Extended ID0	C0MCTL2/ C0LMAR2	0000 0000 ₂ ⁽²⁾ XXXX 0000 ₂ ⁽²⁾
0233 ₁₆	CAN0 Message Slot 3 Control Register / CAN0 Local Mask Register A Extended ID1	C0MCTL3/ C0LMAR3	00 ₁₆ ⁽²⁾ 00 ₁₆ ⁽²⁾
0234 ₁₆	CAN0 Message Slot 4 Control Register / CAN0 Local Mask Register A Extended ID2	C0MCTL4/ C0LMAR4	0000 0000 ₂ ⁽²⁾ XX00 0000 ₂ ⁽²⁾
0235 ₁₆	CAN0 Message Slot 5 Control Register	C0MCTL5	00 ₁₆ ⁽²⁾
0236 ₁₆	CAN0 Message Slot 6 Control Register	C0MCTL6	00 ₁₆ ⁽²⁾
0237 ₁₆	CAN0 Message Slot 7 Control Register	C0MCTL7	00 ₁₆ ⁽²⁾
0238 ₁₆	CAN0 Message Slot 8 Control Register / CAN0 Local Mask Register B Standard ID0	C0MCTL8/ C0LMBR0	0000 0000 ₂ ⁽²⁾ XXX0 0000 ₂ ⁽²⁾

(Note 1)

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NOTES:

1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 0220₁₆ to 023F₁₆.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Address	Register	Symbol	Value after RESET
0239 ₁₆	CAN0 Message Slot 9 Control Register / CAN0 Local Mask Register B Standard ID1	C0MCTL9/ C0LMBR1	0000 0000 ₂ ⁽²⁾ XX00 0000 ₂ ⁽²⁾
023A ₁₆	CAN0 Message Slot 10 Control Register / CAN0 Local Mask Register B Extended ID0	C0MCTL10/ C0LMBR2	0000 0000 ₂ ⁽²⁾ XXXX 0000 ₂ ⁽²⁾
023B ₁₆	CAN0 Message Slot 11 Control Register / CAN0 Local Mask Register B Extended ID1	C0MCTL11/ C0LMBR3	00 ₁₆ ⁽²⁾ 00 ₁₆ ⁽²⁾
023C ₁₆	CAN0 Message Slot 12 Control Register / CAN0 Local Mask Register B Extended ID2	C0MCTL12/ C0LMBR4	0000 0000 ₂ ⁽²⁾ XX00 0000 ₂ ⁽²⁾
023D ₁₆	CAN0 Message Slot 13 Control Register	C0MCTL13	00 ₁₆ ⁽²⁾
023E ₁₆	CAN0 Message Slot 14 Control Register	C0MCTL14	00 ₁₆ ⁽²⁾
023F ₁₆	CAN0 Message Slot 15 Control Register	C0MCTL15	00 ₁₆ ⁽²⁾
0240 ₁₆	CAN0 Slot Buffer Select Register	C0SBS	00 ₁₆ ⁽²⁾
0241 ₁₆	CAN0 Control Register 1	C0CTLR1	XX00 00XX ₂ ⁽²⁾
0242 ₁₆	CAN0 Sleep Control Register	C0SLPR	XXXX XXX0 ₂
0243 ₁₆			
0244 ₁₆	CAN0 Acceptance Filter Support Register	C0AFS	00 ₁₆ ⁽²⁾
0245 ₁₆			01 ₁₆ ⁽²⁾
0246 ₁₆			
0247 ₁₆			
0248 ₁₆			
0249 ₁₆			
024A ₁₆			
024B ₁₆			
024C ₁₆			
024D ₁₆			
024E ₁₆			
024F ₁₆			
0250 ₁₆			
0251 ₁₆			
0252 ₁₆			
0253 ₁₆			
0254 ₁₆			
0255 ₁₆			
0256 ₁₆			
0257 ₁₆			
0258 ₁₆			
0259 ₁₆			
025A ₁₆			
025B ₁₆			
025C ₁₆			
025D ₁₆			
025E ₁₆			
025F ₁₆			
0260 ₁₆			
0261 ₁₆ to 02BF ₁₆			

(Note 1)

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NOTES:

1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 0220₁₆ to 023F₁₆.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Address	Register	Symbol	Value after RESET
02C0 ₁₆ 02C1 ₁₆	X0 Register Y0 Register	X0R,Y0R	XX ₁₆ XX ₁₆
02C2 ₁₆ 02C3 ₁₆	X1 Register Y1 Register	X1R,Y1R	XX ₁₆ XX ₁₆
02C4 ₁₆ 02C5 ₁₆	X2 Register Y2 Register	X2R,Y2R	XX ₁₆ XX ₁₆
02C6 ₁₆ 02C7 ₁₆	X3 Register Y3 Register	X3R,Y3R	XX ₁₆ XX ₁₆
02C8 ₁₆ 02C9 ₁₆	X4 Register Y4 Register	X4R,Y4R	XX ₁₆ XX ₁₆
02CA ₁₆ 02CB ₁₆	X5 Register Y5 Register	X5R,Y5R	XX ₁₆ XX ₁₆
02CC ₁₆ 02CD ₁₆	X6 Register Y6 Register	X6R,Y6R	XX ₁₆ XX ₁₆
02CE ₁₆ 02CF ₁₆	X7 Register Y7 Register	X7R,Y7R	XX ₁₆ XX ₁₆
02D0 ₁₆ 02D1 ₁₆	X8 Register Y8 Register	X8R,Y8R	XX ₁₆ XX ₁₆
02D2 ₁₆ 02D3 ₁₆	X9 Register Y9 Register	X9R,Y9R	XX ₁₆ XX ₁₆
02D4 ₁₆ 02D5 ₁₆	X10 Register Y10 Register	X10R,Y10R	XX ₁₆ XX ₁₆
02D6 ₁₆ 02D7 ₁₆	X11 Register Y11 Register	X11R,Y11R	XX ₁₆ XX ₁₆
02D8 ₁₆ 02D9 ₁₆	X12 Register Y12 Register	X12R,Y12R	XX ₁₆ XX ₁₆
02DA ₁₆ 02DB ₁₆	X13 Register Y13 Register	X13R,Y13R	XX ₁₆ XX ₁₆
02DC ₁₆ 02DD ₁₆	X14 Register Y14 Register	X14R,Y14R	XX ₁₆ XX ₁₆
02DE ₁₆ 02DF ₁₆	X15 Register Y15 Register	X15R,Y15R	XX ₁₆ XX ₁₆
02E0 ₁₆	XY Control Register	XYC	XXXX XX00 ₂
02E1 ₁₆			
02E2 ₁₆			
02E3 ₁₆			
02E4 ₁₆	UART1 Special Mode Register 4	U1SMR4	00 ₁₆
02E5 ₁₆	UART1 Special Mode Register 3	U1SMR3	00 ₁₆
02E6 ₁₆	UART1 Special Mode Register 2	U1SMR2	00 ₁₆
02E7 ₁₆	UART1 Special Mode Register	U1SMR	00 ₁₆
02E8 ₁₆	UART1 Transmit/Receive Mode Register	U1MR	00 ₁₆
02E9 ₁₆	UART1 Baud Rate Register	U1BRG	XX ₁₆
02EA ₁₆ 02EB ₁₆	UART1 Transmit Buffer Register	U1TB	XX ₁₆ XX ₁₆
02EC ₁₆	UART1 Transmit/Receive Control Register 0	U1C0	0000 1000 ₂
02ED ₁₆	UART1 Transmit/Receive Control Register 1	U1C1	0000 0010 ₂
02EE ₁₆ 02EF ₁₆	UART1 Receive Buffer Register	U1RB	XX ₁₆ XX ₁₆

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Address	Register	Symbol	Value after RESET
02F0 ₁₆			
02F1 ₁₆			
02F2 ₁₆			
02F3 ₁₆			
02F4 ₁₆	UART4 Special Mode Register 4	U4SMR4	00 ₁₆
02F5 ₁₆	UART4 Special Mode Register 3	U4SMR3	00 ₁₆
02F6 ₁₆	UART4 Special Mode Register 2	U4SMR2	00 ₁₆
02F7 ₁₆	UART4 Special Mode Register	U4SMR	00 ₁₆
02F8 ₁₆	UART4 Transmit/Receive Mode Register	U4MR	00 ₁₆
02F9 ₁₆	UART4 Baud Rate Register	U4BRG	XX ₁₆
02FA ₁₆	UART4 Transmit Buffer Register	U4TB	XX ₁₆
02FB ₁₆			XX ₁₆
02FC ₁₆	UART4 Transmit/Receive Control Register 0	U4C0	0000 1000 ₂
02FD ₁₆	UART4 Transmit/Receive Control Register 1	U4C1	0000 0010 ₂
02FE ₁₆	UART4 Receive Buffer Register	U4RB	XX ₁₆
02FF ₁₆			XX ₁₆
0300 ₁₆	Timer B3, B4, B5 Count Start Flag	TBSR	000X XXXX ₂
0301 ₁₆			
0302 ₁₆	Timer A1-1 Register	TA11	XX ₁₆
0303 ₁₆			XX ₁₆
0304 ₁₆	Timer A2-1 Register	TA21	XX ₁₆
0305 ₁₆			XX ₁₆
0306 ₁₆	Timer A4-1 Register	TA41	XX ₁₆
0307 ₁₆			XX ₁₆
0308 ₁₆	Three-Phase PWM Control Register 0	INVC0	00 ₁₆
0309 ₁₆	Three-Phase PWM Control Register 1	INVC1	00 ₁₆
030A ₁₆	Three-Phase output Buffer Register 0	IDB0	XX ₁₁ 1111 ₂
030B ₁₆	Three-Phase output Buffer Register 1	IDB1	XX ₁₁ 1111 ₂
030C ₁₆	Dead Time Timer	DTT	XX ₁₆
030D ₁₆	Timer B2 Interrupt Generating Frequency Set Counter	ICTB2	XX ₁₆
030E ₁₆			
030F ₁₆			
0310 ₁₆	Timer B3 Register	TB3	XX ₁₆
0311 ₁₆			XX ₁₆
0312 ₁₆	Timer B4 Register	TB4	XX ₁₆
0313 ₁₆			XX ₁₆
0314 ₁₆	Timer B5 Register	TB5	XX ₁₆
0315 ₁₆			XX ₁₆
0316 ₁₆			
0317 ₁₆			
0318 ₁₆			
0319 ₁₆			
031A ₁₆			
031B ₁₆	Timer B3 Mode Register	TB3MR	00XX 0000 ₂
031C ₁₆	Timer B4 Mode Register	TB4MR	00XX 0000 ₂
031D ₁₆	Timer B5 Mode Register	TB5MR	00XX 0000 ₂
031E ₁₆			
031F ₁₆	External Interrupt Cause Select Register	IFSR	00 ₁₆

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Address	Register	Symbol	Value after RESET
0320 ₁₆			
0321 ₁₆			
0322 ₁₆			
0323 ₁₆			
0324 ₁₆	UART3 Special Mode Register 4	U3SMR4	00 ₁₆
0325 ₁₆	UART3 Special Mode Register 3	U3SMR3	00 ₁₆
0326 ₁₆	UART3 Special Mode Register 2	U3SMR2	00 ₁₆
0327 ₁₆	UART3 Special Mode Register	U3SMR	00 ₁₆
0328 ₁₆	UART3 Transmit/Receive Mode Register	U3MR	00 ₁₆
0329 ₁₆	UART3 Baud Rate Register	U3BRG	XX ₁₆
032A ₁₆	UART3 Transmit Buffer Register	U3TB	XX ₁₆
032B ₁₆			XX ₁₆
032C ₁₆	UART3 Transmit/Receive Control Register 0	U3C0	0000 1000 ₂
032D ₁₆	UART3 Transmit/Receive Control Register 1	U3C1	0000 0010 ₂
032E ₁₆	UART3 Receive Buffer Register	U3RB	XX ₁₆
032F ₁₆			XX ₁₆
0330 ₁₆			
0331 ₁₆			
0332 ₁₆			
0333 ₁₆			
0334 ₁₆	UART2 Special Mode Register 4	U2SMR4	00 ₁₆
0335 ₁₆	UART2 Special Mode Register 3	U2SMR3	00 ₁₆
0336 ₁₆	UART2 Special Mode Register 2	U2SMR2	00 ₁₆
0337 ₁₆	UART2 Special Mode Register	U2SMR	00 ₁₆
0338 ₁₆	UART2 Transmit/Receive Mode Register	U2MR	00 ₁₆
0339 ₁₆	UART2 Baud Rate Register	U2BRG	XX ₁₆
033A ₁₆	UART2 Transmit Buffer Register	U2TB	XX ₁₆
033B ₁₆			XX ₁₆
033C ₁₆	UART2 Transmit/Receive Control Register 0	U2C0	0000 1000 ₂
033D ₁₆	UART2 Transmit/Receive Control Register 1	U2C1	0000 0010 ₂
033E ₁₆	UART2 Receive Buffer Register	U2RB	XX ₁₆
033F ₁₆			XX ₁₆
0340 ₁₆	Count Start Flag	TABSR	00 ₁₆
0341 ₁₆	Clock Prescaler Reset Flag	CPSRF	0XXX XXXX ₂
0342 ₁₆	One-Shot Start Flag	ONSF	00 ₁₆
0343 ₁₆	Trigger Select Register	TRGSR	00 ₁₆
0344 ₁₆	Up-Down Flag	UDF	00 ₁₆
0345 ₁₆			
0346 ₁₆	Timer A0 Register	TA0	XX ₁₆
0347 ₁₆			XX ₁₆
0348 ₁₆	Timer A1 Register	TA1	XX ₁₆
0349 ₁₆			XX ₁₆
034A ₁₆	Timer A2 Register	TA2	XX ₁₆
034B ₁₆			XX ₁₆
034C ₁₆	Timer A3 Register	TA3	XX ₁₆
034D ₁₆			XX ₁₆
034E ₁₆	Timer A4 Register	TA4	XX ₁₆
034F ₁₆			XX ₁₆

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Address	Register	Symbol	Value after RESET
0350 ₁₆ 0351 ₁₆	Timer B0 Register	TB0	XX ₁₆ XX ₁₆
0352 ₁₆ 0353 ₁₆	Timer B1 Register	TB1	XX ₁₆ XX ₁₆
0354 ₁₆ 0355 ₁₆	Timer B2 Register	TB2	XX ₁₆ XX ₁₆
0356 ₁₆	Timer A0 Mode Register	TA0MR	0000 0X002
0357 ₁₆	Timer A1 Mode Register	TA1MR	0000 0X002
0358 ₁₆	Timer A2 Mode Register	TA2MR	0000 0X002
0359 ₁₆	Timer A3 Mode Register	TA3MR	0000 0X002
035A ₁₆	Timer A4 Mode Register	TA4MR	0000 0X002
035B ₁₆	Timer B0 Mode Register	TB0MR	00XX 00002
035C ₁₆	Timer B1 Mode register	TB1MR	00XX 00002
035D ₁₆	Timer B2 Mode Register	TB2MR	00XX 00002
035E ₁₆	Timer B2 Special Mode Register	TB2SC	XXXX XXX02
035F ₁₆	Count Source Prescaler Register ⁽¹⁾	TCSPR	0XXX 00002
0360 ₁₆			
0361 ₁₆			
0362 ₁₆			
0363 ₁₆			
0364 ₁₆	UART0 Special Mode Register 4	U0SMR4	00 ₁₆
0365 ₁₆	UART0 Special Mode Register 3	U0SMR3	00 ₁₆
0366 ₁₆	UART0 Special Mode Register 2	U0SMR2	00 ₁₆
0367 ₁₆	UART0 Special Mode Register	U0SMR	00 ₁₆
0368 ₁₆	UART0 Transmit/Receive Mode Register	U0MR	00 ₁₆
0369 ₁₆	UART0 Baud Rate Register	U0BRG	XX ₁₆
036A ₁₆ 036B ₁₆	UART0 Transmit Buffer Register	U0TB	XX ₁₆ XX ₁₆
036C ₁₆	UART0 Transmit/Receive Control Register 0	U0C0	0000 10002
036D ₁₆	UART0 Transmit/Receive Control Register 1	U0C1	0000 00102
036E ₁₆ 036F ₁₆	UART0 Receive Buffer Register	U0RB	XX ₁₆ XX ₁₆
0370 ₁₆			
0371 ₁₆			
0372 ₁₆			
0373 ₁₆			
0374 ₁₆			
0375 ₁₆			
0376 ₁₆	PLL Control Register 0	PLC0	0011 X1002
0377 ₁₆	PLL Control Register 1	PLC1	XXXX 00002
0378 ₁₆	DMA0 Cause Select Register	DM0SL	0X00 00002
0379 ₁₆	DMA1 Cause Select Register	DM1SL	0X00 00002
037A ₁₆	DMA2 Cause Select Register	DM2SL	0X00 00002
037B ₁₆	DMA3 Cause Select Register	DM3SL	0X00 00002
037C ₁₆ 037D ₁₆	CRC Data Register	CRCD	XX ₁₆ XX ₁₆
037E ₁₆	CRC Input Register	CRCIN	XX ₁₆
037F ₁₆			

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NOTES:

1. The TCSPR register maintains the values set before reset even if software reset or watchdog timer reset is performed.

Address	Register	Symbol	Value after RESET
0380 ₁₆ 0381 ₁₆	A/D0 Register 0	AD00	XX ₁₆ XX ₁₆
0382 ₁₆ 0383 ₁₆	A/D0 Register 1	AD01	XX ₁₆ XX ₁₆
0384 ₁₆ 0385 ₁₆	A/D0 Register 2	AD02	XX ₁₆ XX ₁₆
0386 ₁₆ 0387 ₁₆	A/D0 Register 3	AD03	XX ₁₆ XX ₁₆
0388 ₁₆ 0389 ₁₆	A/D0 Register 4	AD04	XX ₁₆ XX ₁₆
038A ₁₆ 038B ₁₆	A/D0 Register 5	AD05	XX ₁₆ XX ₁₆
038C ₁₆ 038D ₁₆	A/D0 Register 6	AD06	XX ₁₆ XX ₁₆
038E ₁₆ 038F ₁₆	A/D0 Register 7	AD07	XX ₁₆ XX ₁₆
0390 ₁₆			
0391 ₁₆			
0392 ₁₆			
0393 ₁₆			
0394 ₁₆ 0395 ₁₆	A/D0 Control Register 2	AD0CON2	X000 0000 ₂
0396 ₁₆	A/D0 Control Register 0	AD0CON0	00 ₁₆
0397 ₁₆	A/D0 Control Register 1	AD0CON1	00 ₁₆
0398 ₁₆ 0399 ₁₆	D/A Register 0	DA0	XX ₁₆
039A ₁₆ 039B ₁₆	D/A Register 1	DA1	XX ₁₆
039C ₁₆ 039D ₁₆	D/A Control Register	DACON	XXXX XX00 ₂
039E ₁₆			
039F ₁₆			

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<144-pin package>

Address	Register	Symbol	Value after RESET
03A0 ₁₆	Function Select Register A8	PS8	X000 0000 ₂
03A1 ₁₆	Function Select Register A9	PS9	00 ₁₆
03A2 ₁₆			
03A3 ₁₆			
03A4 ₁₆			
03A5 ₁₆			
03A6 ₁₆			
03A7 ₁₆			
03A8 ₁₆			
03A9 ₁₆			
03AA ₁₆			
03AB ₁₆			
03AC ₁₆			
03AD ₁₆			
03AE ₁₆			
03AF ₁₆	Function Select Register C	PSC	00X0 0000 ₂
03B0 ₁₆	Function Select Register A0	PS0	00 ₁₆
03B1 ₁₆	Function Select Register A1	PS1	00 ₁₆
03B2 ₁₆	Function Select Register B0	PSL0	00 ₁₆
03B3 ₁₆	Function Select Register B1	PSL1	00 ₁₆
03B4 ₁₆	Function Select Register A2	PS2	00X0 0000 ₂
03B5 ₁₆	Function Select Register A3	PS3	00 ₁₆
03B6 ₁₆	Function Select Register B2	PSL2	00X0 0000 ₂
03B7 ₁₆	Function Select Register B3	PSL3	00 ₁₆
03B8 ₁₆			
03B9 ₁₆	Function Select Register A5	PS5	XXX0 0000 ₂
03BA ₁₆			
03BB ₁₆			
03BC ₁₆	Function Select Register A6	PS6	00 ₁₆
03BD ₁₆	Function Select Register A7	PS7	00 ₁₆
03BE ₁₆			
03BF ₁₆			
03C0 ₁₆	Port P6 Register	P6	XX ₁₆
03C1 ₁₆	Port P7 Register	P7	XX ₁₆
03C2 ₁₆	Port P6 Direction Register	PD6	00 ₁₆
03C3 ₁₆	Port P7 Direction Register	PD7	00 ₁₆
03C4 ₁₆	Port P8 Register	P8	XX ₁₆
03C5 ₁₆	Port P9 Register	P9	XX ₁₆
03C6 ₁₆	Port P8 Direction Register	PD8	00X0 0000 ₂
03C7 ₁₆	Port P9 Direction Register	PD9	00 ₁₆
03C8 ₁₆	Port P10 Register	P10	XX ₁₆
03C9 ₁₆	Port P11 Register	P11	XX ₁₆
03CA ₁₆	Port P10 Direction Register	PD10	00 ₁₆
03CB ₁₆	Port P11 Direction Register	PD11	XXX0 0000 ₂
03CC ₁₆	Port P12 Register	P12	XX ₁₆
03CD ₁₆	Port P13 Register	P13	XX ₁₆
03CE ₁₆	Port P12 Direction Register	PD12	00 ₁₆
03CF ₁₆	Port P13 Direction Register	PD13	00 ₁₆

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<144-pin package>

Address	Register	Symbol	Value after RESET
03D0 ₁₆	Port P14 Register	P14	XX ₁₆
03D1 ₁₆	Port P15 Register	P15	XX ₁₆
03D2 ₁₆	Port P14 Direction Register	PD14	X000 0000 ₂
03D3 ₁₆	Port P15 Direction Register	PD15	00 ₁₆
03D4 ₁₆			
03D5 ₁₆			
03D6 ₁₆			
03D7 ₁₆			
03D8 ₁₆			
03D9 ₁₆			
03DA ₁₆	Pull-Up Control Register 2	PUR2	00 ₁₆
03DB ₁₆	Pull-Up Control Register 3	PUR3	00 ₁₆
03DC ₁₆	Pull-Up Control Register 4	PUR4	XXXX 0000 ₂
03DD ₁₆			
03DE ₁₆			
03DF ₁₆			
03E0 ₁₆	Port P0 Register	P0	XX ₁₆
03E1 ₁₆	Port P1 Register	P1	XX ₁₆
03E2 ₁₆	Port P0 Direction Register	PD0	00 ₁₆
03E3 ₁₆	Port P1 Direction Register	PD1	00 ₁₆
03E4 ₁₆	Port P2 Register	P2	XX ₁₆
03E5 ₁₆	Port P3 Register	P3	XX ₁₆
03E6 ₁₆	Port P2 Direction Register	PD2	00 ₁₆
03E7 ₁₆	Port P3 Direction Register	PD3	00 ₁₆
03E8 ₁₆	Port P4 Register	P4	XX ₁₆
03E9 ₁₆	Port P5 Register	P5	XX ₁₆
03EA ₁₆	Port P4 Direction Register	PD4	00 ₁₆
03EB ₁₆	Port P5 Direction Register	PD5	00 ₁₆
03EC ₁₆			
03ED ₁₆			
03EE ₁₆			
03EF ₁₆			
03F0 ₁₆	Pull-Up Control Register 0	PUR0	00 ₁₆
03F1 ₁₆	Pull-Up Control Register 1	PUR1	XXXX 0000 ₂
03F2 ₁₆			
03F3 ₁₆			
03F4 ₁₆			
03F5 ₁₆			
03F6 ₁₆			
03F7 ₁₆			
03F8 ₁₆			
03F9 ₁₆			
03FA ₁₆			
03FB ₁₆			
03FC ₁₆			
03FD ₁₆			
03FE ₁₆			
03FF ₁₆	Port Control Register	PCR	XXXX XXX0 ₂

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
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Address	Register	Symbol	Value after RESET	
03A0 ₁₆				(Note 2)
03A1 ₁₆				
03A2 ₁₆				
03A3 ₁₆				
03A4 ₁₆				
03A5 ₁₆				
03A6 ₁₆				
03A7 ₁₆				
03A8 ₁₆				
03A9 ₁₆				
03AA ₁₆				
03AB ₁₆				
03AC ₁₆				
03AD ₁₆				
03AE ₁₆				
03AF ₁₆	Function Select Register C	PSC	0X00 0000 ₂	
03B0 ₁₆	Function Select Register A0	PS0	00 ₁₆	
03B1 ₁₆	Function Select Register A1	PS1	00 ₁₆	
03B2 ₁₆	Function Select Register B0	PSL0	00 ₁₆	
03B3 ₁₆	Function Select Register B1	PSL1	00 ₁₆	
03B4 ₁₆	Function Select Register A2	PS2	00X0 0000 ₂	
03B5 ₁₆	Function Select Register A3	PS3	00 ₁₆	
03B6 ₁₆	Function Select Register B2	PSL2	00X0 0000 ₂	
03B7 ₁₆	Function Select Register B3	PSL3	00 ₁₆	
03B8 ₁₆				
03B9 ₁₆				(Note 2)
03BA ₁₆				
03BB ₁₆				
03BC ₁₆				(Note 2)
03BD ₁₆				
03BE ₁₆				
03BF ₁₆				
03C0 ₁₆	Port P6 Register	P6	XX ₁₆	
03C1 ₁₆	Port P7 Register	P7	XX ₁₆	
03C2 ₁₆	Port P6 Direction Register	PD6	00 ₁₆	
03C3 ₁₆	Port P7 Direction Register	PD7	00 ₁₆	
03C4 ₁₆	Port P8 Register	P8	XX ₁₆	
03C5 ₁₆	Port P9 Register	P9	XX ₁₆	
03C6 ₁₆	Port P8 Direction Register	PD8	00X0 0000 ₂	
03C7 ₁₆	Port P9 Direction Register	PD9	00 ₁₆	
03C8 ₁₆	Port P10 Register	P10	XX ₁₆	
03C9 ₁₆				(Note 2)
03CA ₁₆	Port P10 Direction Register	PD10	00 ₁₆	
03CB ₁₆				(Note 1)
03CC ₁₆				(Note 2)
03CD ₁₆				
03CE ₁₆				(Note 1)
03CF ₁₆				

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

-  Set address spaces 03CB₁₆, 03CE₁₆ and 03CF₁₆ to "FF₁₆" in the 100-pin package.
-  Address spaces 03A0₁₆, 03A1₁₆, 03B9₁₆, 03BC₁₆, 03BD₁₆, 03C9₁₆, 03CC₁₆ and 03CD₁₆ are not provided in the 100-pin package.




<100-pin package>

Address	Register	Symbol	Value after RESET	
03D0 ₁₆				(Note 3)
03D1 ₁₆				
03D2 ₁₆				(Note 1)
03D3 ₁₆				
03D4 ₁₆				
03D5 ₁₆				
03D6 ₁₆				
03D7 ₁₆				
03D8 ₁₆				
03D9 ₁₆				
03DA ₁₆	Pull-up Control Register 2	PUR2	00 ₁₆	
03DB ₁₆	Pull-up Control Register 3	PUR3	00 ₁₆	
03DC ₁₆				(Note 2)
03DD ₁₆				
03DE ₁₆				
03DF ₁₆				
03E0 ₁₆	Port P0 Register	P0	XX ₁₆	
03E1 ₁₆	Port P1 Register	P1	XX ₁₆	
03E2 ₁₆	Port P0 Direction Register	PD0	00 ₁₆	
03E3 ₁₆	Port P1 Direction Register	PD1	00 ₁₆	
03E4 ₁₆	Port P2 Register	P2	XX ₁₆	
03E5 ₁₆	Port P3 Register	P3	XX ₁₆	
03E6 ₁₆	Port P2 Direction Register	PD2	00 ₁₆	
03E7 ₁₆	Port P3 Direction Register	PD3	00 ₁₆	
03E8 ₁₆	Port P4 Register	P4	XX ₁₆	
03E9 ₁₆	Port P5 Register	P5	XX ₁₆	
03EA ₁₆	Port P4 Direction Register	PD4	00 ₁₆	
03EB ₁₆	Port P5 Direction Register	PD5	00 ₁₆	
03EC ₁₆				
03ED ₁₆				
03EE ₁₆				
03EF ₁₆				
03F0 ₁₆	Pull-Up Control Register 0	PUR0	00 ₁₆	
03F1 ₁₆	Pull-Up Control Register 1	PUR1	XXXX 0000 ₂	
03F2 ₁₆				
03F3 ₁₆				
03F4 ₁₆				
03F5 ₁₆				
03F6 ₁₆				
03F7 ₁₆				
03F8 ₁₆				
03F9 ₁₆				
03FA ₁₆				
03FB ₁₆				
03FC ₁₆				
03FD ₁₆				
03FE ₁₆				
03FF ₁₆	Port Control Register	PCR	XXXX XXX0 ₂	

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1.  Set address spaces 03D2₁₆ and 03D3₁₆ to "FF₁₆" in the 100-pin package.
2.  Set address spaces 03DC₁₆ to "00₁₆" in the 100-pin package.
3.  Address spaces 03D0₁₆ and 03D1₁₆ are not provided in the 100-pin package.

5. Reset

Hardware reset, software reset, and watchdog timer reset are available to reset the microcomputer.

5.1 Hardware Reset

5.1.1 Reset on a Stable Supply Voltage

The microcomputer resets pins, the CPU and SFR when the supply voltage meets the recommended performance conditions while an "L" signal is applied to the $\overline{\text{RESET}}$ pin (see **Table 5.1**). Apply an "H" signal to the RESET pin again after 20 or more clock cycles are input to the XIN pin while applying an "L" to the $\overline{\text{RESET}}$ pin. The CPU and SFR are reset and programs run from the address indicated by the reset vector.

The internal RAM is not reset. When the $\overline{\text{RESET}}$ pin becomes "L" while writing data to the internal RAM, the internal RAM is in an indeterminate state.

5.1.2 Power-on Reset

The microcomputer resets pins, the CPU and SFR when the supply voltage applied to the VCC pin meets the recommended performance conditions while an "L" signal is applied to the $\overline{\text{RESET}}$ pin. (See **Table 5.1**.)

The CPU and SFR are reset when the signal applied to the $\overline{\text{RESET}}$ pin changes low ("L") to high ("H") after the main clock oscillation stabilizes and 20 or more clock cycles are applied to the XIN pin. Programs run from the address indicated by the reset vector. The internal RAM is in an indeterminate state

Figure 5.1 shows a reset circuit. Figure 5.2 shows a reset sequence. Figure 5.3 shows CPU register conditions after reset. Table 5.1 lists pin states while the $\overline{\text{RESET}}$ pin is held "L". Refer to **4. SFR** for SFR states after reset.

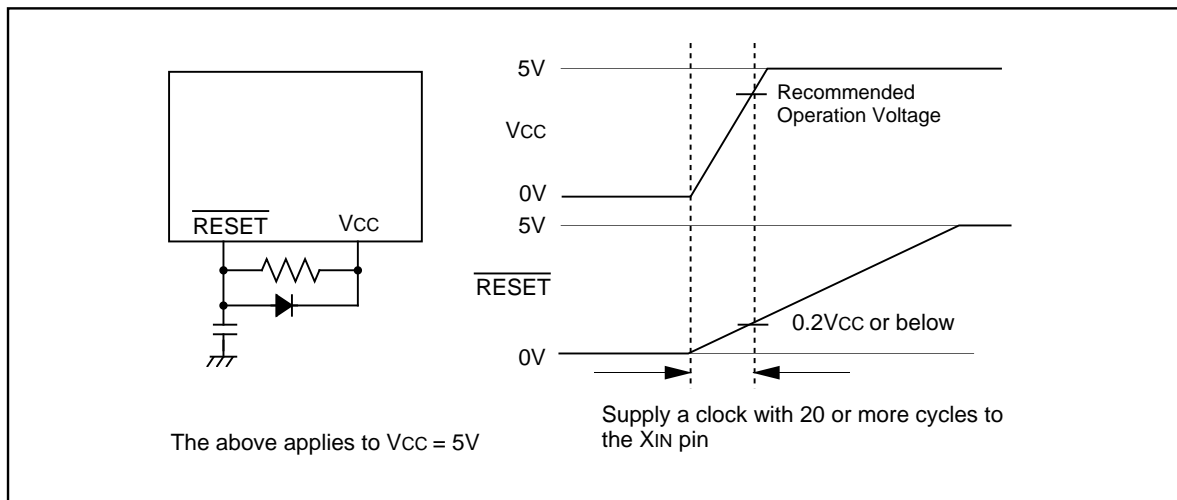


Figure 5.1 Reset Circuit

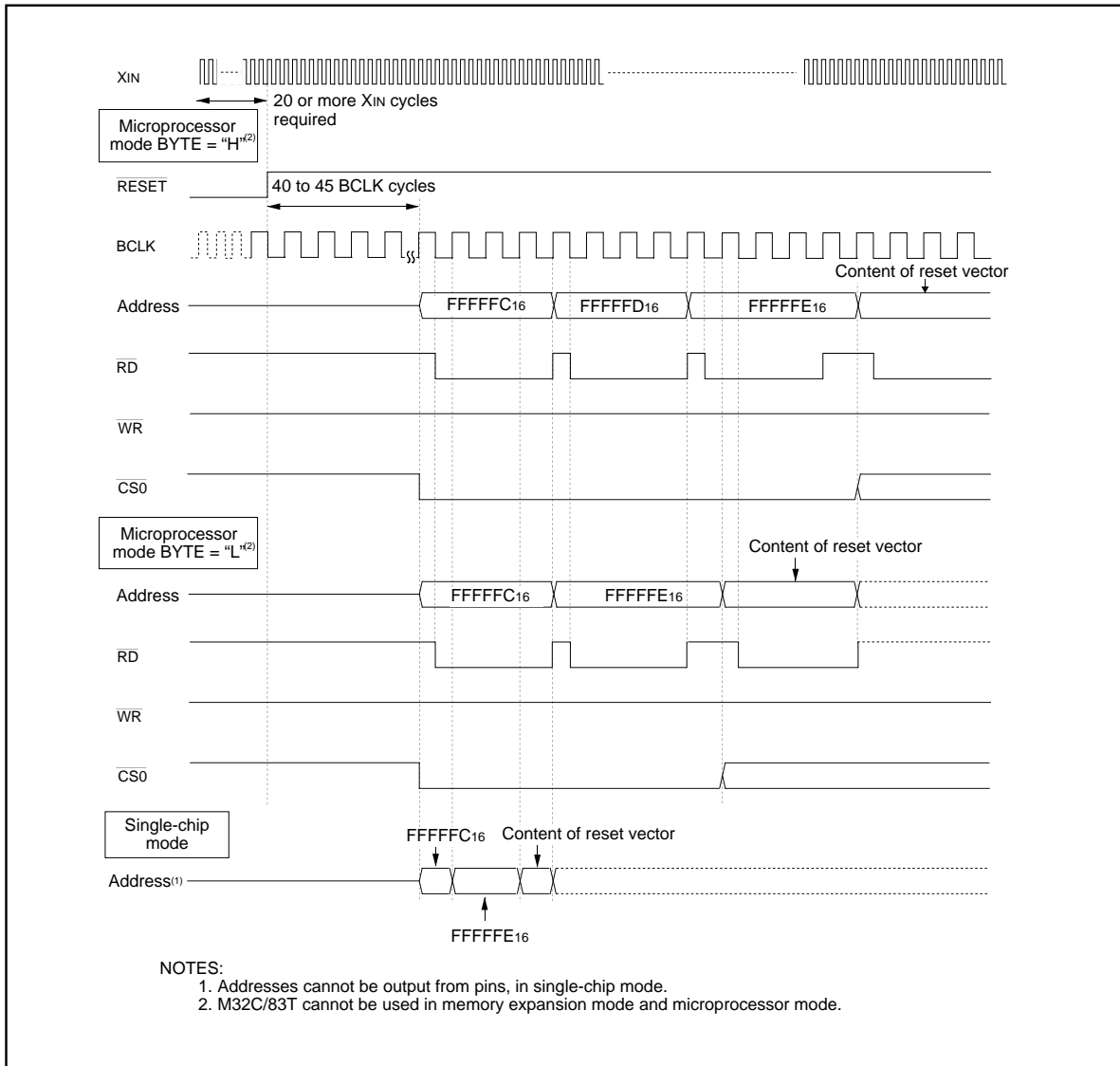


Figure 5.2 Reset Sequence

Table 5.1 Pin States while RESET Pin is Held "L"

Pin Name	Pin States		
	CNVss = Vss	CNVss = Vcc	
		BYTE = Vss	BYTE = Vcc
P0	Input port (high-impedance)	Data input (high-impedance)	
P1	Input port (high-impedance)	Data input (high-impedance)	Input port (high-impedance)
P2, P3, P4	Input port (high-impedance)	Address output (indeterminate)	
P50	Input port (high-impedance)	\overline{WR} output (output "H")	
P51	Input port (high-impedance)	\overline{BHE} output (indeterminate)	
P52	Input port (high-impedance)	\overline{RD} output (output "H")	
P53	Input port (high-impedance)	BCLK output	
P54	Input port (high-impedance)	HLDA output (output value depends on an input to \overline{HOLD} pin)	
P55	Input port (high-impedance)	\overline{HOLD} input (high-impedance)	
P56	Input port (high-impedance)	\overline{RAS} output	
P57	Input port (high-impedance)	\overline{RDY} input (high-impedance)	
P6 to P15 ⁽¹⁾	Input port (high-impedance)	Input port (high-impedance)	

NOTES:

1. Ports P11 to P15 are provided in the 144-pin package.

5.2 Software Reset

When the PM03 bit in the PM0 register is set to "1" (microcomputer reset), pins, the CPU and SFR are reset. Then the microcomputer executes the program from an address determined by the reset vector.

When software reset is performed, some registers in the SFR are not reset. Refer to **4. SFR** for details.

Set the PM03 bit to "1" while the main clock is selected as the CPU clock and the main clock oscillation is stable.

5.3 Watchdog Timer Reset

The microcomputer resets pins, the CPU and the SFR when the watchdog timer underflows while the CM06 bit in the CM0 register is set to "1" (reset). Then the microcomputer executes the program from an address indicated by the reset vector.

When watchdog timer reset is performed, some registers in the SFR are not reset. Refer to **4. SFR** for details. Because the PM01 to PM00 bits in the PM0 register are not reset, the processor mode remains unchanged.

5.4 Internal Space

Figure 5.3 shows CPU register states after reset. Refer to 4. SFR for SFR states after reset.

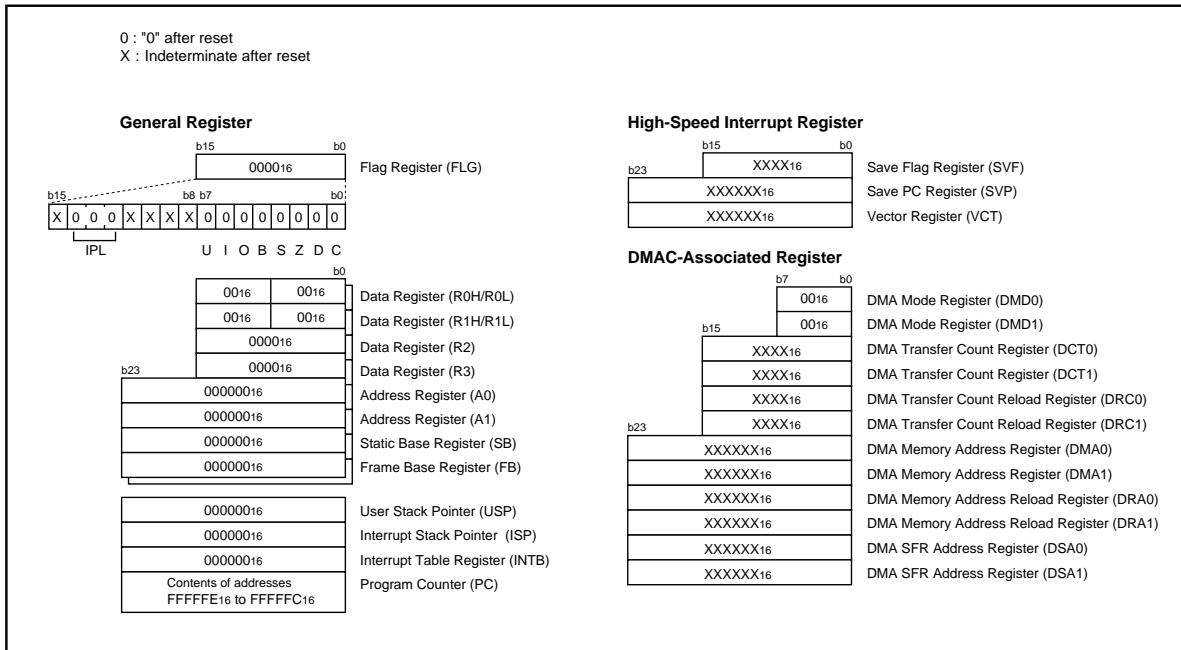


Figure 5.3 CPU Register after Reset

6. Processor Mode

NOTE

M32C/83T can be used in single-chip mode.

M32C/83T cannot be used in memory expansion mode and microprocessor mode.

6.1 Types of Processor Mode

Single-chip mode, memory expansion mode, or microprocessor mode can be selected as processor mode. Pin functions, memory map and accessible space vary depending on the selected processor mode.

6.1.1 Single-chip Mode

In single-chip mode, internal memory space (the SFR, internal RAM and internal ROM) can be accessed. All I/O ports can be used.

6.1.2 Memory Expansion Mode

In memory expansion mode, both external memory space and internal memory space can be accessed. Some pins function as pins for bus control signals. The BYTE pin and register settings determine how many pins are assigned for these pin functions. Refer to **7. Bus** for details.

6.1.3 Microprocessor Mode

In microprocessor mode, SFR, internal RAM and external memory space can be accessed. Internal ROM cannot be accessed.

Some pins function as pins for bus control signals. The BYTE pin and register settings determine how many pins are assigned for these pin functions. (Refer to **7. Bus** for details.)

6.2 Setting Processor Mode

The processor mode is set by the combination of CNVSS pin and the PM01 to PM00 bit settings in the PM0 register. Do not set the PM01 to PM00 bits to "102".

If the PM01 to PM00 bits are rewritten, the mode corresponding to the PM01 to PM00 bits is selected regardless of CNVSS pin level.

Do not change the PM01 to PM00 bits when the PM02 to PM07 bits in the PM0 register are being rewritten.

Do not enter microprocessor mode while the CPU is executing a program in the internal ROM. Do not enter single-chip mode while the CPU is executing a program in an external memory space.

Figures 6.1 and 6.2 show the PM0 register and PM1 register. Figure 6.3 shows a memory map in each processor mode.

6.2.1 Applying VSS to CNVSS Pin

The microcomputer enters single-chip mode after reset. Set the PM01 to PM00 bits to "012" (memory expansion mode) to switch to memory expansion mode after the microcomputer starts operating.

6.2.2 Applying VCC to CNVSS Pin

The microcomputer enters microprocessor mode after reset.

When using the flash memory version, apply VCC to P55 (HOLD) as well as to the CNVSS.

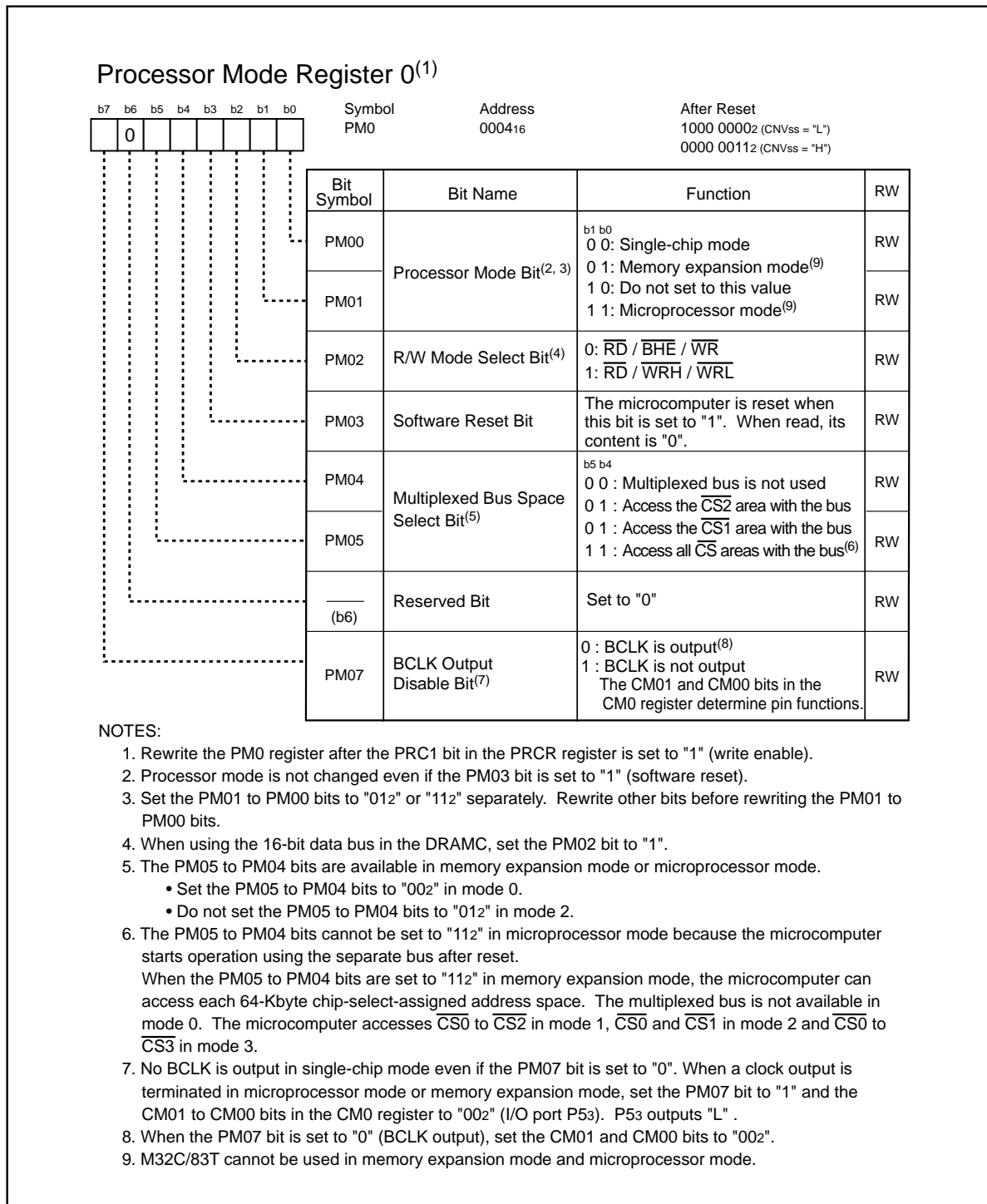
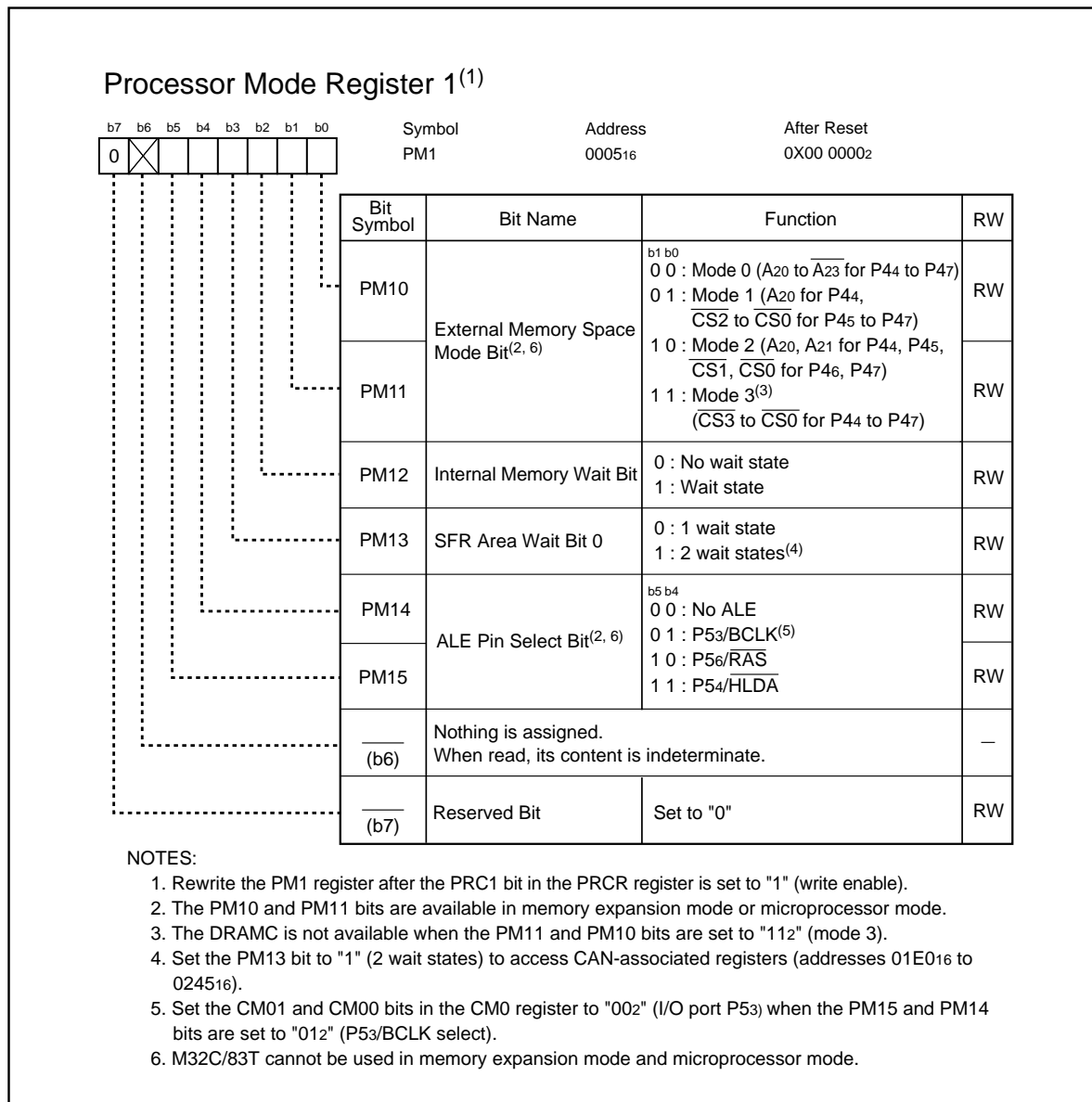


Figure 6.1 PM0 Register

**Figure 6.2 PM1 Register**

Address	Single-Chip Mode			Memory Expansion Mode			Microprocessor Mode		
	Mode 0	Mode 1	Mode 2	Mode 3	Mode 0	Mode 1	Mode 2	Mode 3	
00000016	SFR	SFR	SFR	SFR	SFR	SFR	SFR	SFR	
00040016	Internal RAM Reserved Space	Internal RAM Reserved Space	Internal RAM Reserved Space	Internal RAM Reserved Space	Internal RAM Reserved Space	Internal RAM Reserved Space	Internal RAM Reserved Space	Internal RAM Reserved Space	
00080016	External Space 0	External Space 0	External Space 0	External Space 0	External Space 0	External Space 0	External Space 0	External Space 0	
10000016	External Space 1	External Space 1	External Space 1	External Space 1	External Space 1	External Space 1	External Space 1	External Space 1	
20000016	External Space 2	External Space 2	External Space 2	External Space 2	External Space 2	External Space 2	External Space 2	External Space 2	
30000016	External Space 3	External Space 3	External Space 3	External Space 3	External Space 3	External Space 3	External Space 3	External Space 3	
40000016	Internal ROM	Internal ROM	Internal ROM	Internal ROM	Internal ROM	Internal ROM	Internal ROM	Internal ROM	
C0000016	External Space 0	External Space 0	External Space 0	External Space 0	External Space 0	External Space 0	External Space 0	External Space 0	
E0000016	External Space 1	External Space 1	External Space 1	External Space 1	External Space 1	External Space 1	External Space 1	External Space 1	
F0000016	External Space 2	External Space 2	External Space 2	External Space 2	External Space 2	External Space 2	External Space 2	External Space 2	
FFFFFF16	External Space 3	External Space 3	External Space 3	External Space 3	External Space 3	External Space 3	External Space 3	External Space 3	

NOTES:
 1. 20000016~00800016=2016K bytes. 32K bytes less than 2M bytes.
 2. 40000016~00800016=4064K bytes. 32K bytes less than 4M bytes.

The WCR register determines how many wait states are inserted for each space CS0 to CS3.

Figure 6.3 Memory Map in Each Processor Mode

7. Bus

In memory expansion mode or microprocessor mode, some pins function as bus control pins to input and output data from external devices. A0 to A22, $\overline{A23}$, D0 to D15, MA0 to MA12, $\overline{CS0}$ to $\overline{CS3}$, $\overline{WRL/WR/CASL}$, $\overline{WRH/BHE/CASH}$, $\overline{RD/DW}$, $\overline{BCLK/ALE}$, $\overline{HLDA/ALE}$, \overline{HOLD} , $\overline{ALE/RAS}$, and \overline{RDY} are used as bus control pins.

NOTE

Bus control pins in M32C/83T cannot be used.

7.1 Bus Settings

The BYTE pin, the DS register, the PM05 to PM04 bits in the PM0 register and the PM11 to PM10 bits in the PM1 register determine bus settings.

Table 7.1 lists how to change a bus setting. Figure 7.1 shows the DS register.

Table 7.1 Bus Settings

Bus Setting	Changed By
Selecting external address bus width	DS register
Setting bus width after reset	BYTE pin (external space 3 only)
Switching between separate bus or multiplexed bus	PM05 to PM04 bits in PM0 register
Number of chip-select	PM11 to PM10 bits in PM1 register

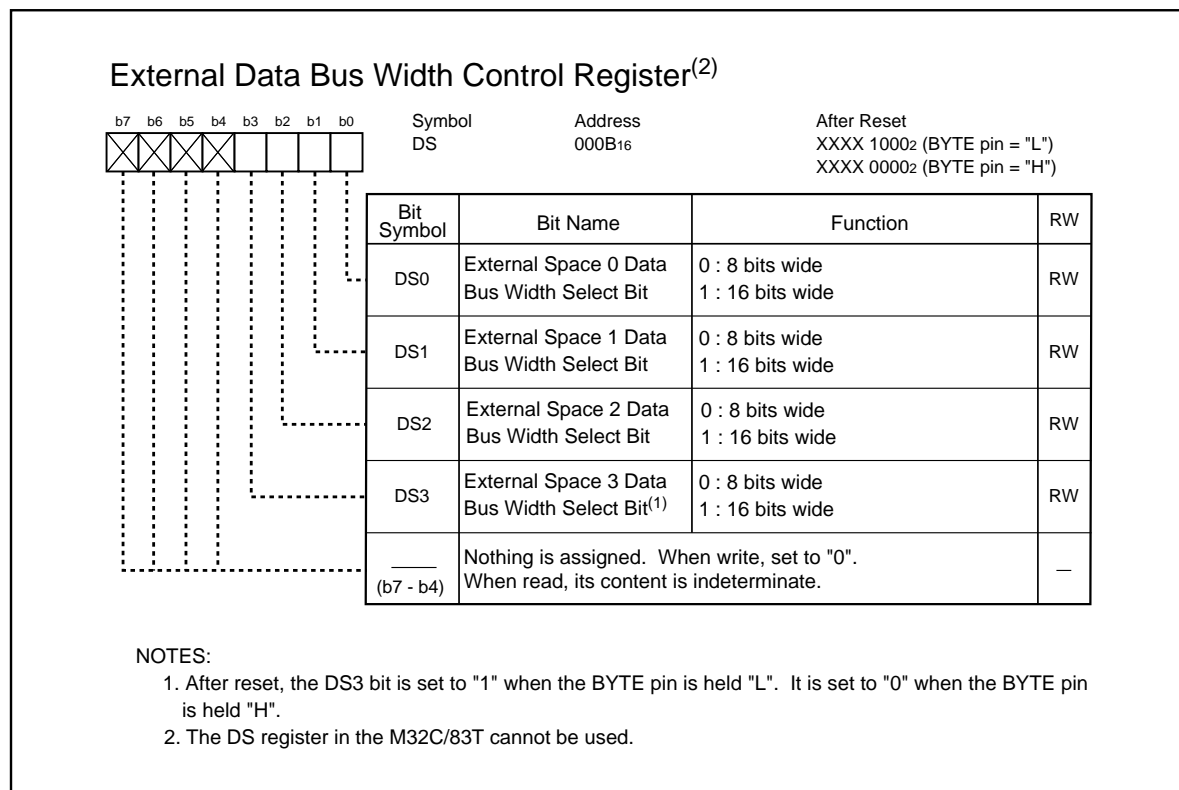


Figure 7.1 DS Register

7.1.1 Selecting External Address Bus

The number of externally-output address bus, chip-select signals and chip-select-assigned address space (\overline{CS} area) varies depending on each external space mode. The PM11 to PM10 bits in the PM1 register determine the external space mode.

When using the DRAMC, row addresses and column addresses are multiplexed to output in the DRAM area.

7.1.2 Selecting External Data Bus

The DS register selects either external 8-bit or 16-bit data bus per external space. The data bus in the external space 3, after reset, becomes 16 bits wide when an "L" signal is applied to the BYTE pin and 8 bits wide when an "H" signal is applied. Do not change the BYTE pin level while the microcomputer is operating. The internal bus is always 16 bits wide.

7.1.3 Selecting Separate/Multiplexed Bus

The PM05 to PM04 bits in the PM0 register determine either a separate or multiplexed bus as bus format .

7.1.3.1 Separate Bus

The separate bus is a bus format which allows the microcomputer to input and output data and address using separate buses. The DS register selects 8-bit or 16-bit data bus as the external data bus per external space. If all DS_i bits in the DS register (i=0 to 3) are set to "0" (8-bit data bus), port P0 becomes the data bus and port P1 becomes the programmable I/O port. If one of the DS_i bits is set to "1" (16-bit data bus), ports P0 and P1 become the data bus. When the microcomputer accesses a space while the DS_i bit set to "0", port P1 is indeterminate.

If the microcomputer accesses a space with the separate bus, the WCR register determines the number of software wait states inserted.

7.1.3.2 Multiplexed Bus

The multiplexed bus is a bus format which allows the microcomputer to input and output data and address via bus by timesharing. D0 to D7 are multiplexed with A0 to A7 in space accessed by the 8-bit data bus. D0 to D15 are multiplexed with A0 to A15 in space accessed by the 16-bit data bus. If the microcomputer accesses a space with the multiplexed bus, the WCR register can be set to either two wait states or three wait states. Two-wait-state access is automatically selected if the WCR register is set to no wait state or one wait state. Refer to **7.2.4 Bus Timing** for details.

The microcomputer starts operation using the separate bus after reset. Therefore, the multiplexed bus can be assigned to access the $\overline{CS1}$ area, the CS2 area, or all CS areas. However, the multiplexed bus cannot be assigned to access all \overline{CS} areas in microprocessor mode. When the PM05 and PM04 bits in the PM0 register are set to "112" (access all \overline{CS} areas with the bus), only 16 low-order bits, from A0 to A15, of an address are output. See Table 7.2 for details.

Table 7.2 Processor Mode and Port Function

Processor Mode	Single-Chip Mode	Memory Expansion Mode/ Microprocessor Mode				Memory Expansion Mode	
PM05 to PM04 Bits in PM0 Register		"012", "102" (Access CS ₁ or CS ₂ using the Multiplexed Bus Access All Other CS Areas using the Separate Bus)		"002" (Access all CS Areas using the Separate Bus)		"112" ⁽¹⁾ (Access all CS Areas using the Multiplexed Bus)	
		Access all external space with 8-bit data bus	Access one or more external space with 16-bit data bus	Access all external space with 8-bit data bus	Access one or more external space with 16-bit data bus	Access all external space with 8-bit data bus	Access one or more external space with 16-bit data bus
P00 to P07	I/O port	Data bus D ₀ to D ₇	Data bus D ₀ to D ₇	Data bus D ₀ to D ₇	Data bus D ₀ to D ₇	I/O port	I/O port
P10 to P17	I/O port	I/O port	Data bus D ₈ to D ₁₅	I/O port	Data bus D ₈ to D ₁₅	I/O port	I/O port
P20 to P27	I/O port	Address bus/ Data bus ⁽²⁾ A ₀ /D ₀ to A ₇ /D ₇	Address bus/ Data bus ⁽²⁾ A ₀ /D ₀ to A ₇ /D ₇	Address bus A ₀ to A ₇	Address bus A ₀ to A ₇	Address bus/ Data bus A ₀ /D ₀ to A ₇ /D ₇	Address bus/ Data bus A ₀ /D ₀ to A ₇ /D ₇
P30 to P37	I/O port	Address bus A ₈ to A ₁₅	Address bus/ Data bus ⁽²⁾ A ₈ /D ₈ to A ₁₅ /D ₁₅	Address bus A ₈ to A ₁₅	Address bus A ₈ to A ₁₅	Address bus A ₈ to A ₁₅	Address bus/ Data bus A ₈ /D ₈ to A ₁₅ /D ₁₅
P40 to P43	I/O port	Address bus A ₁₆ to A ₁₉	Address bus A ₁₆ to A ₁₉	Address bus A ₁₆ to A ₁₉	Address bus A ₁₆ to A ₁₉	I/O port	I/O port
P44 to P46	I/O port	CS (Chip-select signal) or Address bus (A ₂₀ to A ₂₂) (Refer to 7.2 Bus Control for details) ⁽⁴⁾					
P47	I/O port	CS (Chip-select signal) or Address bus (A ₂₃) (Refer to 7.2 Bus Control for details) ⁽⁴⁾					
P50 to P53	I/O port	Outputs RD, WRL, WRH and BCLK or outputs RD, BHE, WR and BCLK (Refer to 7.2 Bus Control for details) ⁽³⁾					
P54	I/O port	HLDA ⁽³⁾	HLDA ⁽³⁾	HLDA ⁽³⁾	HLDA ⁽³⁾	HLDA ⁽³⁾	HLDA ⁽³⁾
P55	I/O port	HOLD	HOLD	HOLD	HOLD	HOLD	HOLD
P56	I/O port	RAS ⁽³⁾	RAS ⁽³⁾	RAS ⁽³⁾	RAS ⁽³⁾	RAS ⁽³⁾	RAS ⁽³⁾
P57	I/O port	RDY	RDY	RDY	RDY	RDY	RDY

NOTES:

- The PM05 to PM04 bits cannot be set to "112" (access all CS areas using multiplexed bus) in microprocessor mode because the microcomputer starts operation using the separate bus after reset. When the PM05 to PM04 bits are set to "112" in memory expansion mode, the microcomputer accesses 64K-byte memory space per chip select using the address bus.
- These ports become address buses when accessing space using the separate bus.
- The PM15 to PM14 bits in the PM1 register determine which pin outputs the ALE signal. The PM02 bit in the PM0 register selects either "WRL,WRH" or "BHE,WR" combination. P56 provides an indeterminate output when the PM15 and PM14 bits to "002" (no ALE). It cannot be used as an I/O port.
- When DRAMC is selected to access DRAM area, CASL, CASH, DW, BCLK become output pins.
- The PM11 to PM10 bits in the PM1 register determine the CS signal and address bus.

7.2 Bus Control

Signals required to access external devices are provided and software wait states are inserted as follows. The signals are available in memory expansion mode and microprocessor mode only.

7.2.1 Address Bus and Data Bus

The address bus is a signal accessing 16M-byte space and uses 24 control pins; A₀ to A₂₂ and \overline{A}_{23} . \overline{A}_{23} is the inversed output signal of the highest-order address bit.

The data bus is a signal which inputs and outputs data. The DS register selects the 8-bit data bus from D₀ to D₇ or the 16-bit data bus from D₀ to D₁₅ for each external space. When applying an "H" signal to the BYTE pin, the data bus accessing the external memory space 3 becomes the 8-bit data bus after reset. When applying an "L" signal to the BYTE pin, the data bus accessing the external memory space 3 becomes the 16-bit data bus.

When changing single-chip mode to memory expansion mode, the address bus is in an indeterminate state until the microcomputer accesses an external memory space.

When using the DRAMC to access DRAM area, row addresses and column addresses are multiplexed and output via A₈ to A₂₀.

7.2.2 Chip-Select Signal

The chip-select signal shares ports with A₀ to A₂₂ and \overline{A}_{23} . The PM₁₁ to PM₁₀ bits in the PM1 register determine which \overline{CS} area is accessed and how many chip-select signals are output. A maximum of four chip-select signals can be output.

In microprocessor mode, the chip-select signal is not output after reset. \overline{A}_{23} , however, can perform as the chip-signal signal.

The chip-select signal becomes "L" while the microcomputer accesses the external \overline{CS}_i area (i=0 to 3). It becomes high ("H") when the microcomputer accesses another external memory space or an internal memory space. Figure 7.2 shows an example of the address bus and chip-select signal output.

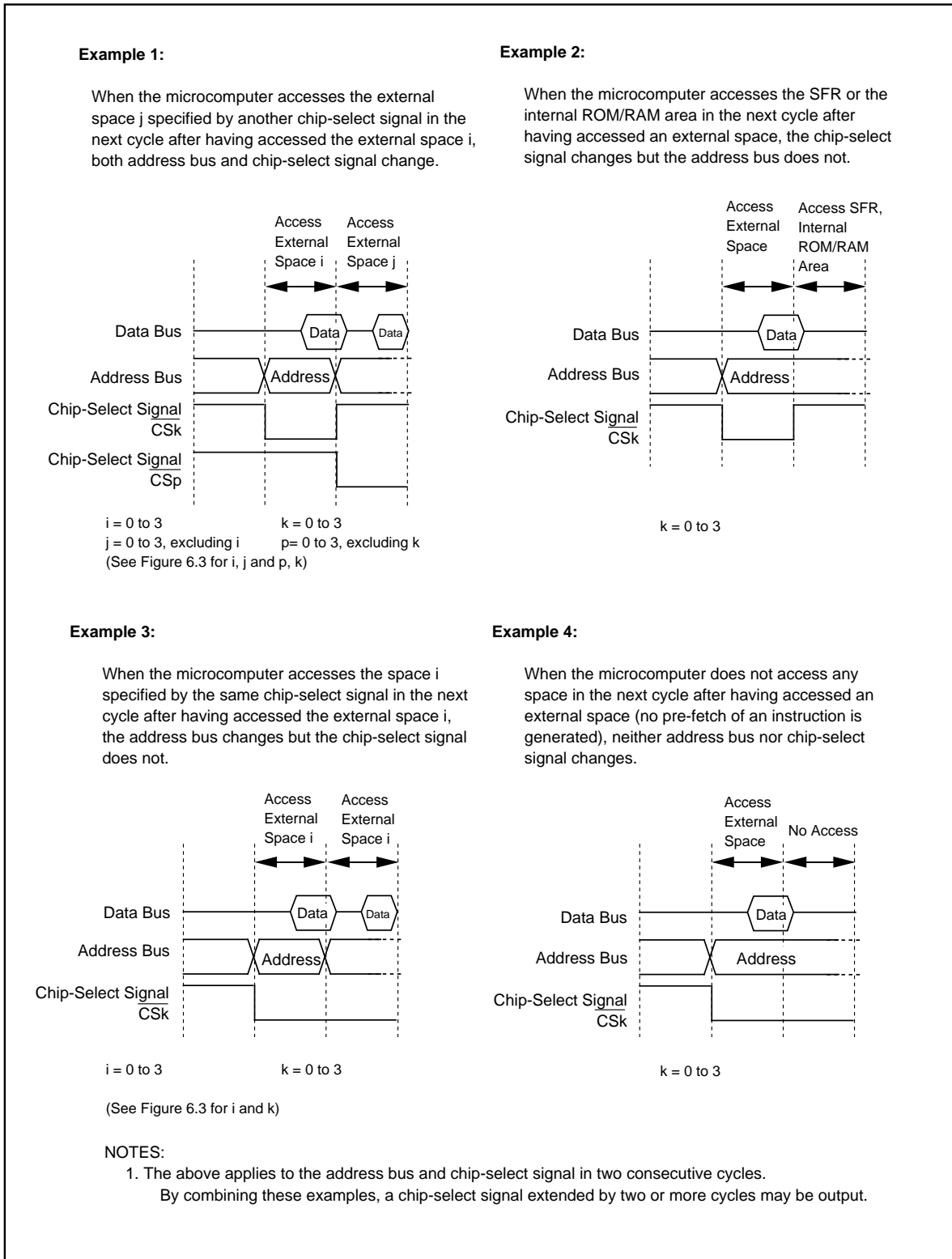


Figure 7.2 Address Bus and Chip-Select Signal Outputs (Separate bus)

7.2.3 Read and Write Signals

When set to the 16-bit data bus, the PM02 bit in the PM0 register selects a combination of the \overline{RD} , \overline{WR} and \overline{BHE} signals or the \overline{RD} , \overline{WRL} and \overline{WRH} signals to determine the read or write signal. When the DS3 to DS0 bits in the DS register are set to "0" (8-bit data bus), set the PM02 bit to "0" ($\overline{RD}/\overline{WR}/\overline{BHE}$). If any of the DS3 to DS0 bits are set to "1" (16-bit data bus) when accessing an 8-bit space, the combination of \overline{RD} , \overline{WR} and \overline{BHE} is automatically selected regardless of the PM02 bit setting. Tables 7.3 and 7.4 list each signal operations.

The \overline{RD} , \overline{WR} and \overline{BHE} signals are combined for the read or write signal after reset.

When changing the combination to \overline{RD} , \overline{WRL} and \overline{WRH} , set the PM02 bit before writing data to an external memory.

When using the DRAMC to access the DRAM with the 16-bit bus, set the PM02 bit to "1" ($\overline{RD}/\overline{WRL}/\overline{WRH}$).

Table 7.3 \overline{RD} , \overline{WRL} and \overline{WRH} Signals

Data Bus	\overline{RD}	\overline{WRL}	\overline{WRH}	Status of External Data Bus
16 Bits	L	H	H	Read data
	H	L	H	Write 1-byte data to even address
	H	H	L	Write 1-byte data to odd address
	H	L	L	Write data to both even and odd addresses
8 Bits	H	L ⁽¹⁾	Not used	Write 1-byte data
	L	H ⁽¹⁾	Not used	Read 1-byte data

NOTES:

1. The \overline{WR} signal is used instead of the \overline{WRL} signal.

Table 7.4 \overline{RD} , \overline{WR} and \overline{BHE} Signals

Data Bus	\overline{RD}	\overline{WR}	\overline{BHE}	A0	Status of External Data Bus
16 Bits	H	L	L	H	Write 1-byte data to odd address
	L	H	L	H	Read 1-byte data from odd address
	H	L	H	L	Write 1-byte data to even address
	L	H	H	L	Read 1-byte data from even address
	H	L	L	L	Write data to both even and odd addresses
	L	H	L	L	Read data from both even and odd addresses
8 Bits	H	L	Not used	H / L	Write 1-byte data
	L	H	Not used	H / L	Read 1-byte data

7.2.4 Bus Timing

Bus cycle for the internal ROM and internal RAM are basically one BCLK cycle. When the PM12 bit in the PM1 register is set to "1" (wait state), the bus cycles are two BCLK cycles.

Bus cycles for the SFR are basically two BCLK cycles. When the PM13 bit in the PM1 register is set to "1" (2 wait states), the bus cycles are three BCLK cycles. To access CAN-associated registers (addresses 01E0₁₆ to 0245₁₆), set the PM13 bit to "1".

Bus cycle for an external space is basically one BCLK cycle for a read operation and two BCLK cycles for a write operation. The WCR register inserts wait states equivalent to one to three BCLK cycles into an external space. Bus cycles are two BCLK cycles if selecting one wait state. Bus cycles are four BCLK cycles if selecting three wait states.

If applicable to the followings, bus cycles vary from those selected by the WCR register. Figure 7.5 shows each bit status and bus cycle.

- Write cycle with the separate bus and no wait state
- Read cycle and write cycle with the multiplexed bus and no wait state.
- Read cycle and write cycle with the multiplexed bus and one wait state.

Figure 7.3 shows the WCR register. Figures 7.4 and 7.5 show bus timing in an external space.

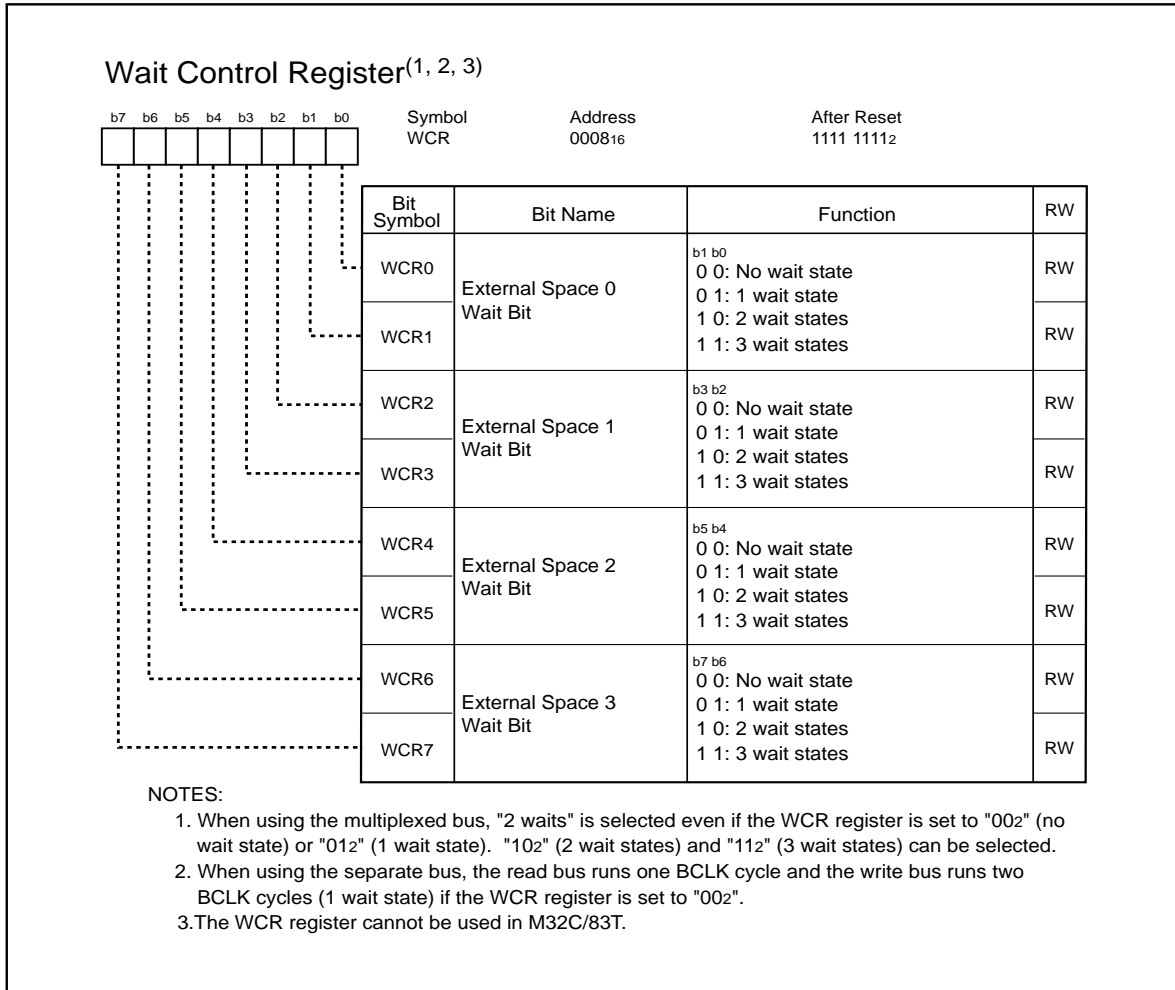


Figure 7.3 WCR Register

Table 7.5 Software Wait State and Bus Cycle

Space	External Bus Status	PM1 Register		WCR Register	Bus Cycle	
		PM13 Bit	PM12 Bit	WCRj to WCRi Bits		
SFR	_____	0	_____	_____	2 BCLK cycles	
		1			3 BCLK cycles	
Internal ROM/RAM	_____	_____	0	_____	1 BCLK cycle	
			1		2 BCLK cycles	
External Memory	Separate Bus	_____	_____	002	Read :1 BCLK cycle Write : 2 BCLK cycles	
				012	2 BCLK cycles	
				102	3 BCLK cycles	
				112	4 BCLK cycles	
	Multiplexed Bus	_____	_____	_____	002	3 BCLK cycle
					012	3 BCLK cycles
					102	3 BCLK cycles
					112	4 BCLK cycles

$i = 0, 2, 4, 6$ $j = i + 1$

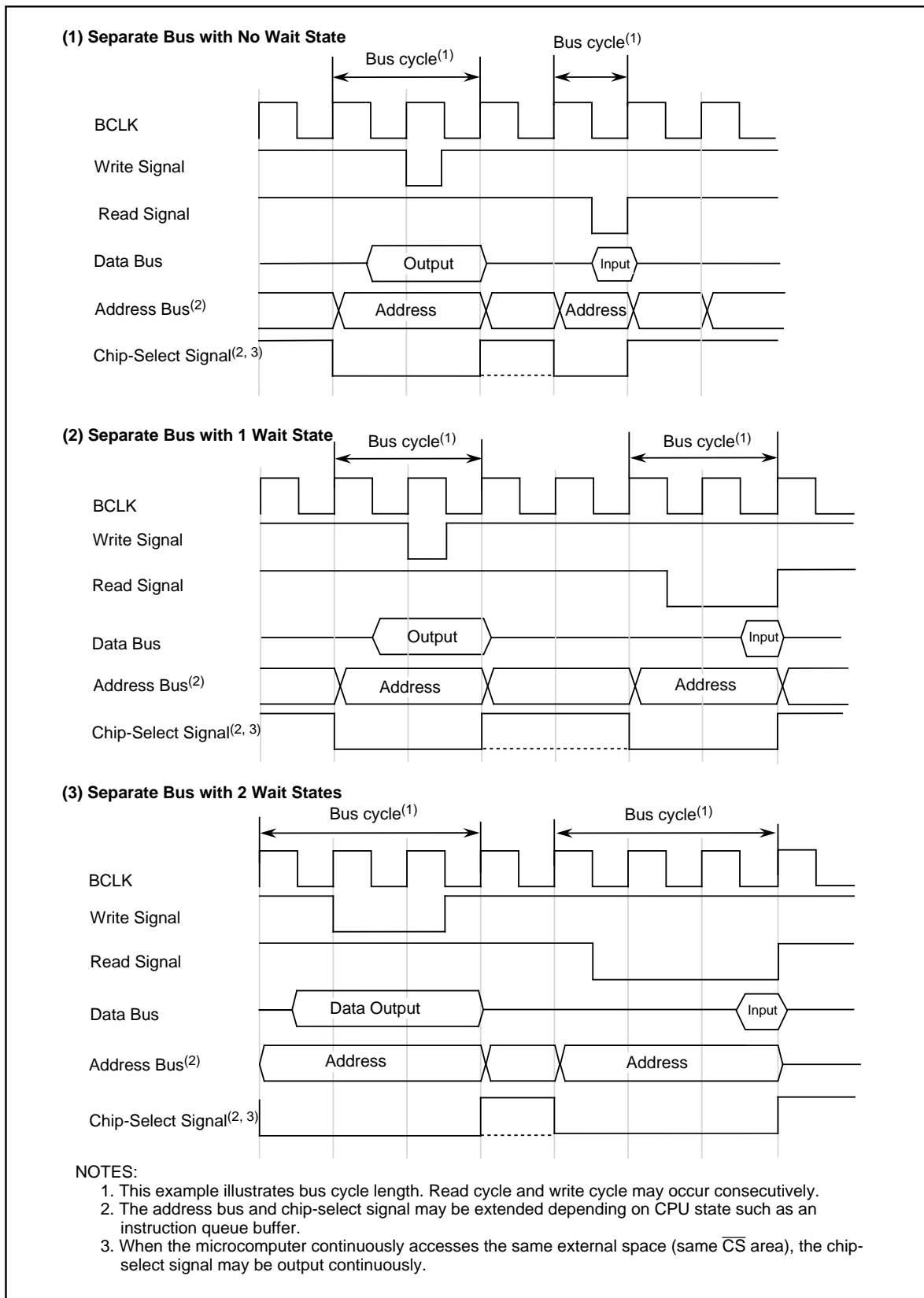


Figure 7.4 External Bus Operation with Software Wait State (1)

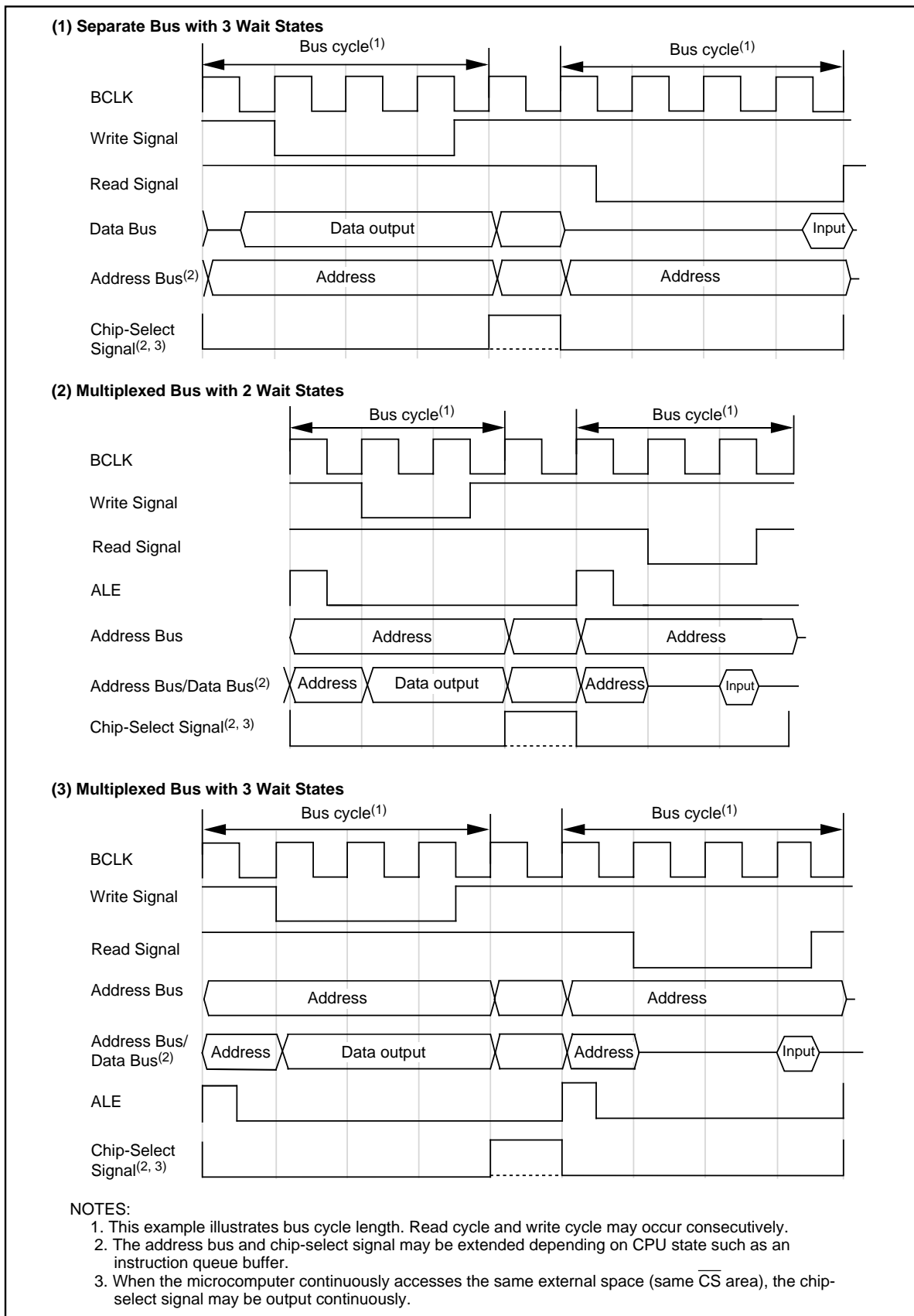


Figure 7.5 External Bus Operation with Software Wait State (2)

7.2.5 ALE Signal

The ALE signal latches an address of the multiplexed bus. Latch an address on the falling edge of the ALE signal. The PM15 to PM14 bits in the PM1 register determine the output pin for the ALE signal. The ALE signal is output to an internal space and external space.

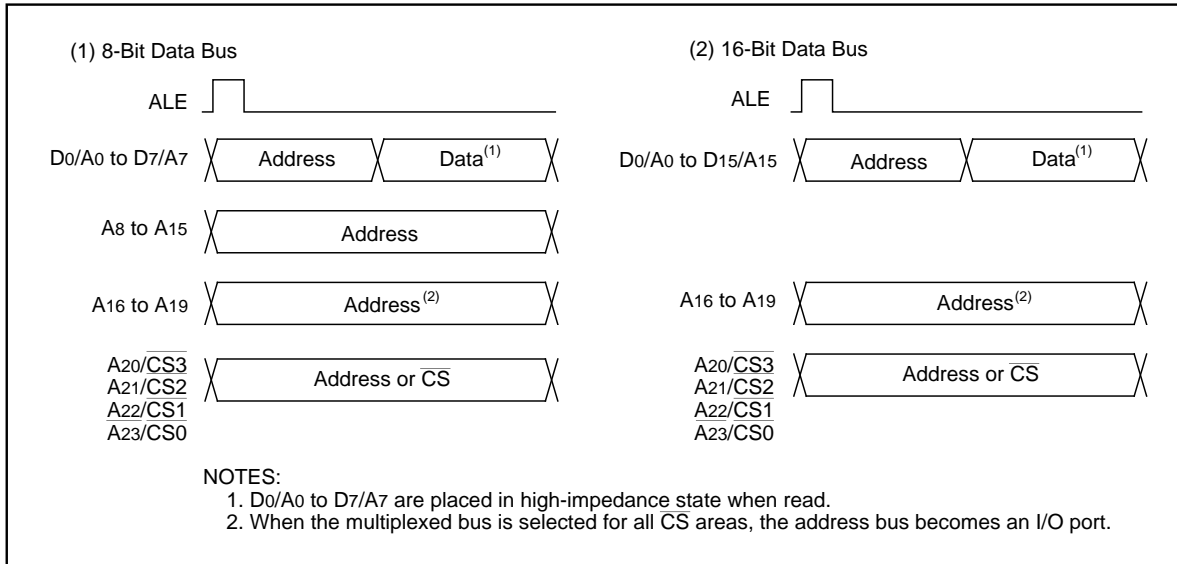


Figure 7.6 ALE Signal and Address/Data Bus

7.2.6 RDY Signal

The $\overline{\text{RDY}}$ signal facilitates access to external devices which need longer access time. When an "L" signal is applied to the $\overline{\text{RDY}}$ pin on the falling edge of last BCLK of the bus cycle, wait states are inserted into the bus cycle. When an "H" signal is applied to the $\overline{\text{RDY}}$ pin on the falling edge of the BCLK, the bus cycle starts running again.

Table 7.6 lists microcomputer states when the $\overline{\text{RDY}}$ signal inserts wait states into the bus cycle. Figure 7.7 shows an example of the $\overline{\text{RD}}$ signal extended by the $\overline{\text{RDY}}$ signal.

Table 7.6 Microcomputer States in a Wait State⁽¹⁾

Item	State
Oscillation	On
$\overline{\text{RD}}$ Signal, $\overline{\text{WR}}$ Signal, Address Bus, $\overline{\text{CS}}_i$ ($i=0$ to 3), Data Bus, ALE Signal, HLDA, Programmable I/O Ports	Maintains the same state as when $\overline{\text{RDY}}$ signal was received
Internal Peripheral Circuits	On

NOTES:

1. The $\overline{\text{RDY}}$ signal cannot be accepted immediately before software wait states are inserted.

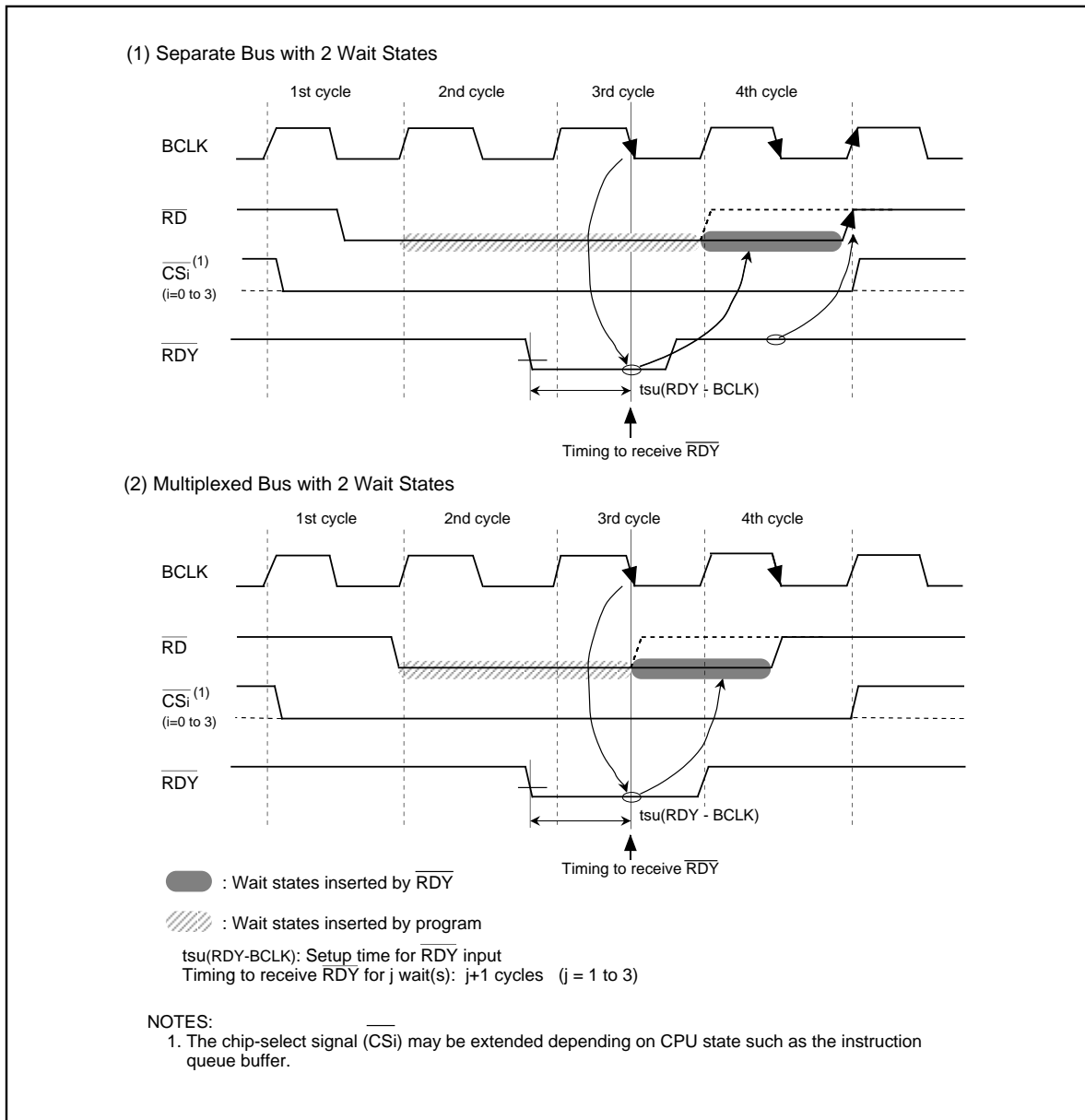


Figure 7.7 \overline{RD} Signal Output Extended by \overline{RDY} Signal

7.2.7 \overline{HOLD} Signal

The \overline{HOLD} signal transfers bus privileges from the CPU to external circuits. When an "L" signal is applied to the \overline{HOLD} pin, the microcomputer enters a hold state after bus access is completed. While the \overline{HOLD} pin is held "L", the microcomputer is in a hold state and the \overline{HLDA} pin outputs an "L" signal. Table 7.7 shows the microcomputer status in a hold state.

Bus is used in the following order of priority: \overline{HOLD} , DMAC, CPU.

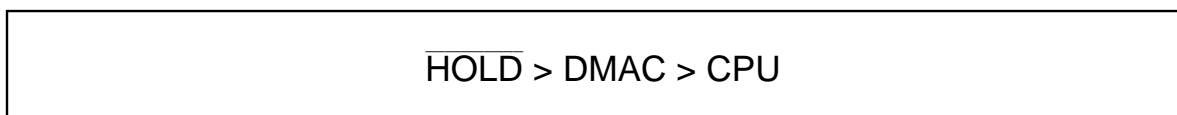


Figure 7.8 Order of Bus Priority

Table 7.7 Microcomputer Status in a Hold State

Item	Status
Oscillation	On
RD Signal, WR Signal, Address Bus, Data Bus, BHE, CS0 to CS3	High-impedance
Programmable I/O Ports: P0 to P15	Maintains the same state as when HOLD signal is received
HLDA	Output "L"
Internal Peripheral Circuits	On (excluding the watchdog timer)
ALE Signal	Output "L"

7.2.8 External Bus State when Accessing Internal Space

Table 7.8 shows external bus states when an internal space is accessed.

Table 7.8 External Bus State when Accessing Internal Space

Item	State when accessing SFR, internal ROM and internal RAM	
Address bus	Holds an address of an external space accessed just before	
Data Bus	When Read	High-impedance
	When Write	High-impedance
RD, WR, WRL, WRH	Output "H"	
BHE	Holds state of external space last accessed	
CS0 to CS3	Output "H"	
ALE	Output ALE	

7.2.9 BCLK Output

The CPU clock operates the CPU. When combining the PM07 bit in the PM0 register set to "0" (BCLK output) and the CM01 to CM00 bits in the CM0 register set to "002", the CPU clock signal is output from P53 as BCLK.

No BCLK is output in single-chip mode. Refer to **8. Clock Generating Circuit** for details.

7.2.10 DRAM Control Signals (RAS, CASL, CASH and DW)

The DRAM control signals control the DRAM. The DRAM control signals are output when the DRAM area, determined by the AR0 to AR2 bits in the DRAMCONT register, is output. Table 7.9 lists each signal operation.

Table 7.9 RAS, CASL, CASH and DW Signals

Data Bus Width	RAS	CASL	CASH	DW	Data Bus State
16 bits	L	L	L	H	Read data from both even and odd addresses
	L	L	H	H	Read 1-byte data from even address
	L	H	L	H	Read 1-byte data from odd address
	L	L	L	L	Write data to both even and odd addresses
	L	L	H	L	Write 1-byte data to even address
	L	H	L	L	Write 1-byte data to odd address
8 bits	L	L	Not used	H	Read 1-byte data
	L	L	Not used	L	Write 1-byte data

8. Clock Generation Circuit

8.1 Types of Clock Generation Circuits

Four circuits are incorporated to generate the system clock signal :

- Main clock oscillation circuit
- Sub clock oscillation circuit
- On-chip oscillator
- PLL frequency synthesizer

Table 8.1 lists specifications of the clock generation circuit. Figure 8.1 shows a block diagram of the clock generation circuit. Figures 8.2 to 8.8 show registers controlling the clock.

Table 8.1 Clock Generation Circuit Specifications

Item	Main Clock Oscillation Circuit	Sub Clock Oscillation Circuit	On-chip Oscillator	PLL Frequency Synthesizer
Use	<ul style="list-style-type: none"> • CPU clock source • Peripheral function clock source 	<ul style="list-style-type: none"> • CPU clock source • Timer A and B clock source 	<ul style="list-style-type: none"> • CPU clock source • Peripheral function clock source 	<ul style="list-style-type: none"> • CPU clock source • Peripheral function clock source
Clock Frequency	Up to 32 MHz	32.768 kHz	Approximately 1 MHz	20 MHz to 32 MHz (See Table 8.2)
Connectable Oscillator or Additional Circuit	<ul style="list-style-type: none"> • Ceramic resonator • Crystal oscillator 	<ul style="list-style-type: none"> • Crystal oscillator 	_____	<ul style="list-style-type: none"> • Low pass filter
Pins for Oscillator or for Additional Circuit	XIN, XOUT	XCIN, XCOU	_____	VCOUT (connect to low pass filter) P86 (connect to Vss)
Oscillation Stop/Restart Function	Available	Available	Available	Available
Oscillator State After Reset	Oscillating	Stopped	Stopped	Stopped
Other	External clock can be input	External clock can be input. The PLL frequency synthesizer cannot be used when using the sub clock oscillation circuit.	When the main clock stops oscillating, the on-chip oscillator starts oscillating automatically and becomes the clock source for the CPU and peripheral functions	The sub clock cannot be used when using the PLL frequency synthesizer

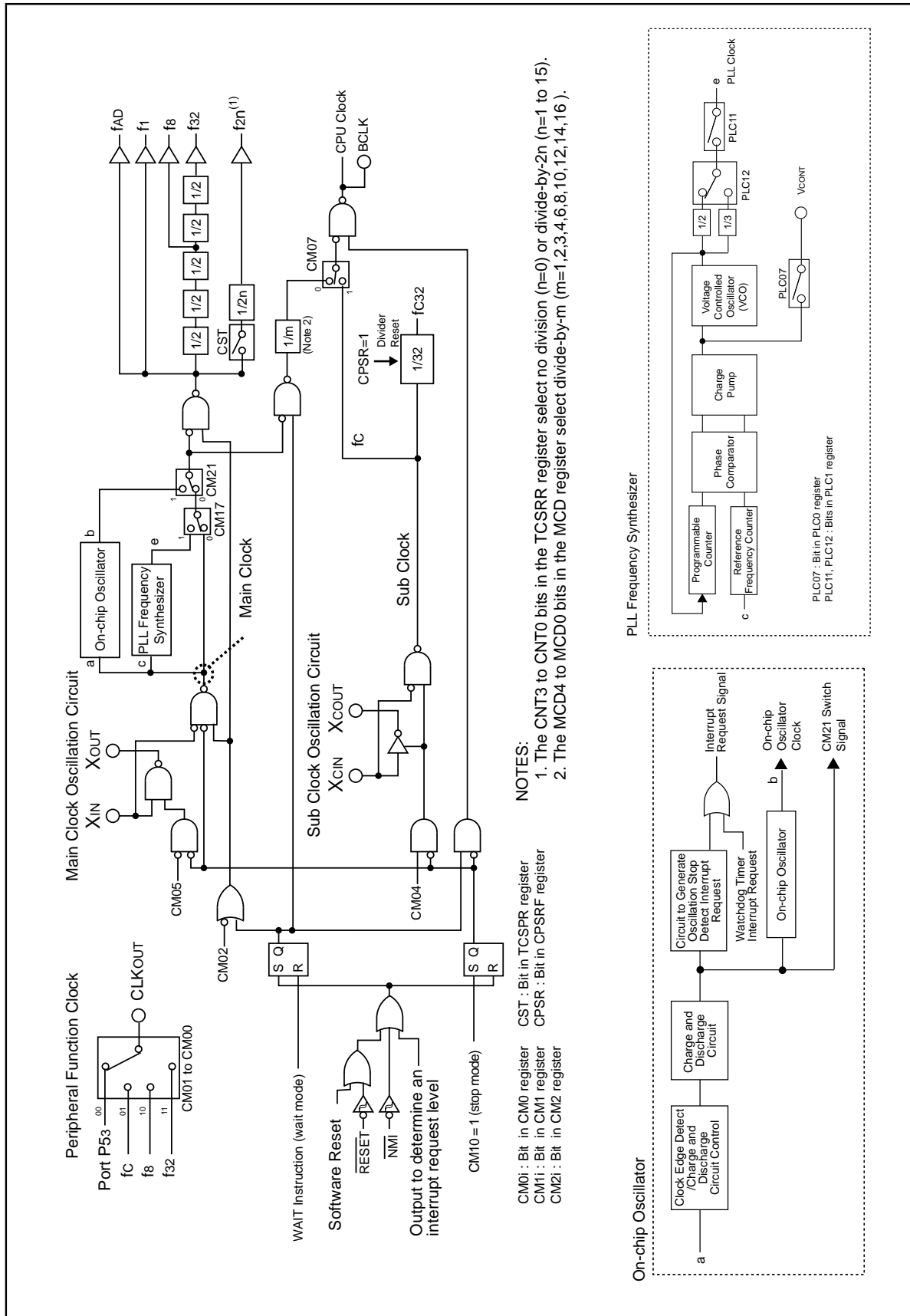


Figure 8.1 Clock Generation Circuit

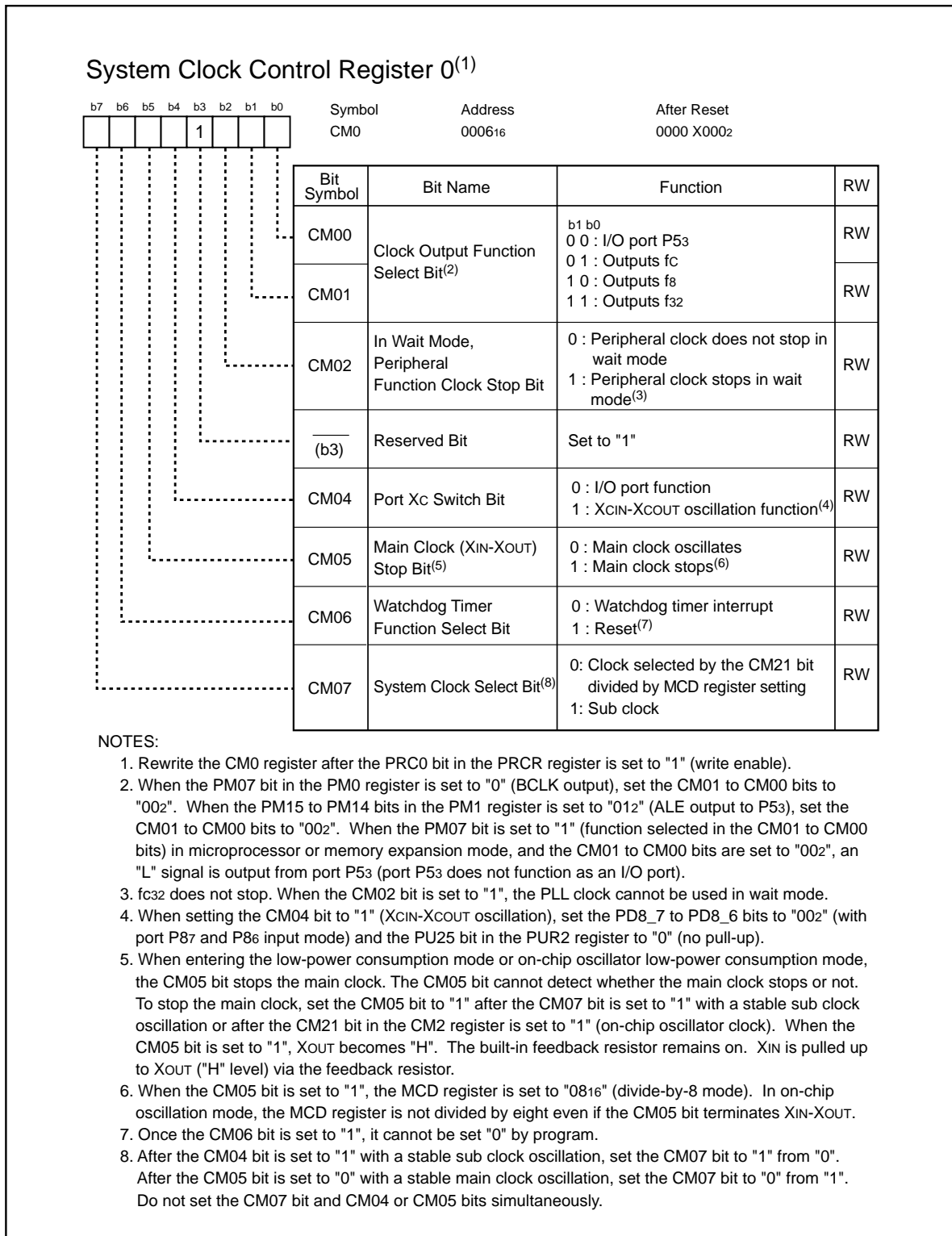
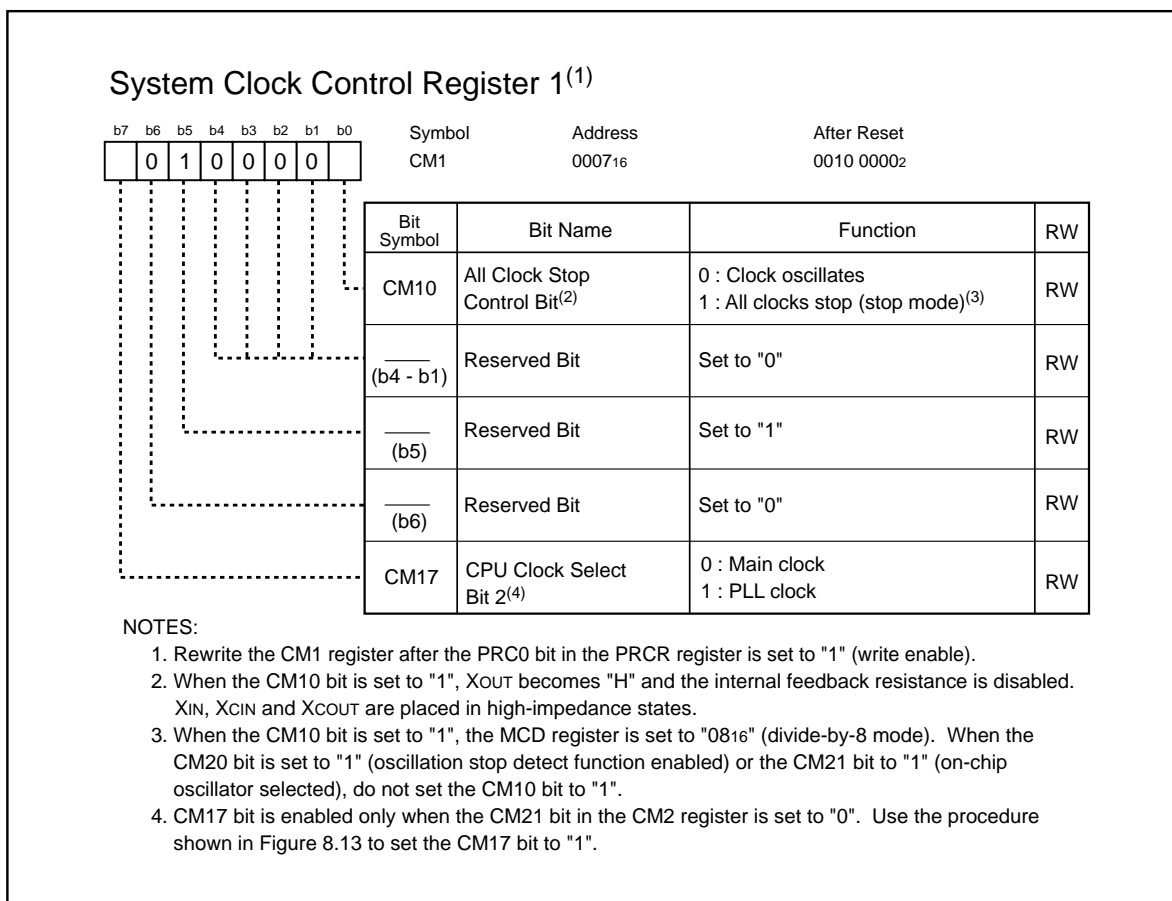
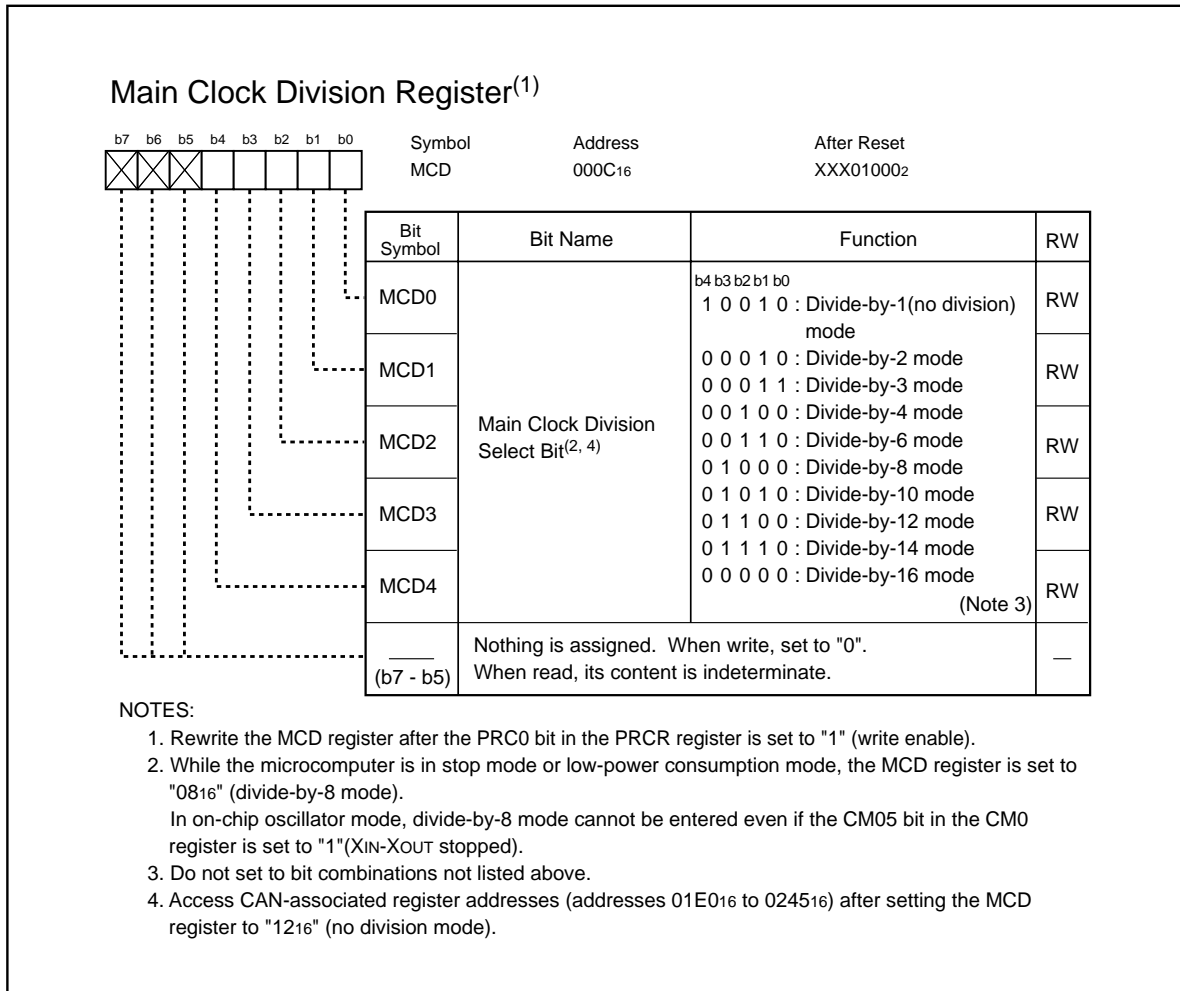
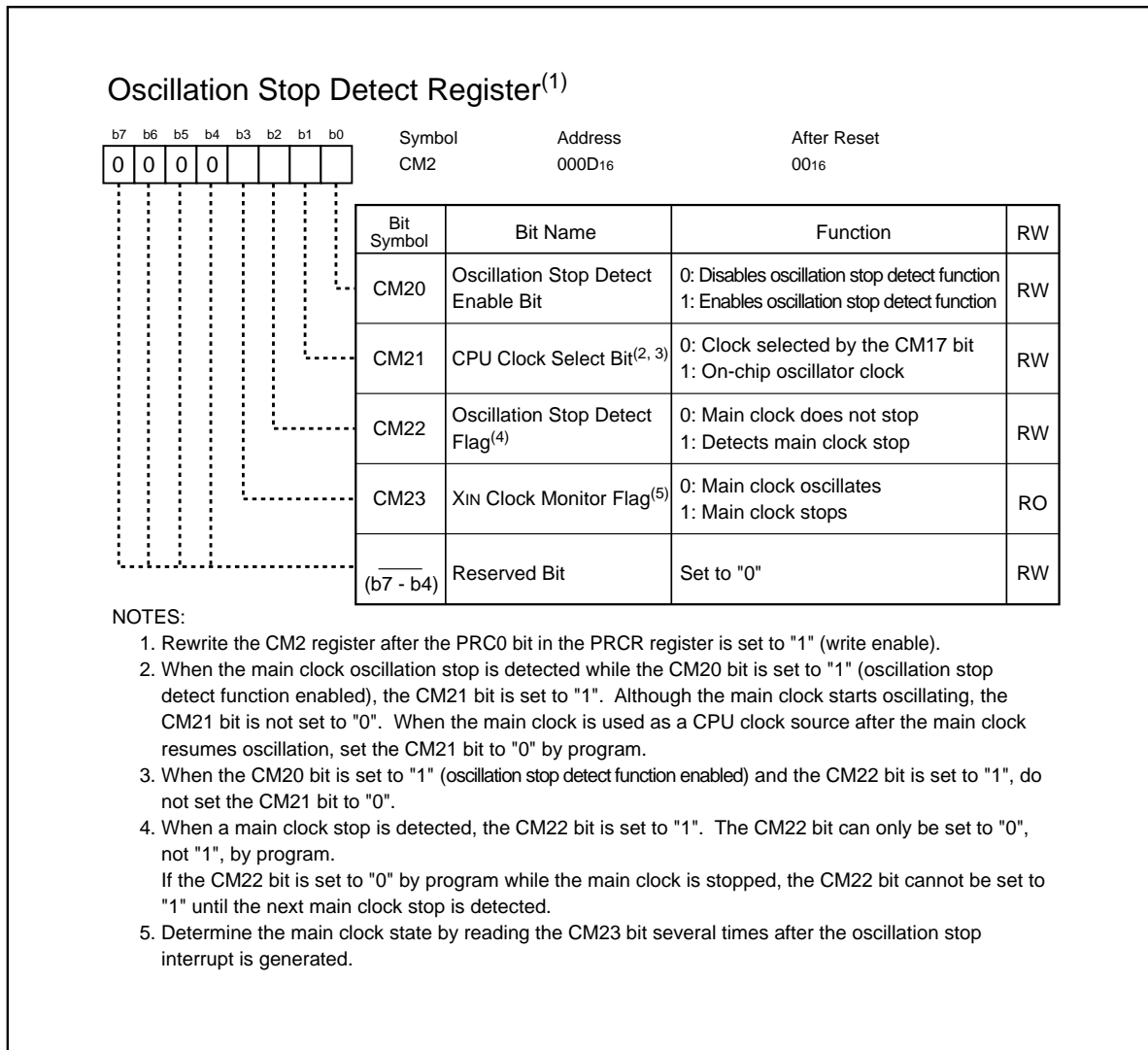


Figure 8.2 CM0 Register

**Figure 8.3 CM1 Register**

**Figure 8.4 MCD Register**

**Figure 8.5 CM2 Register**

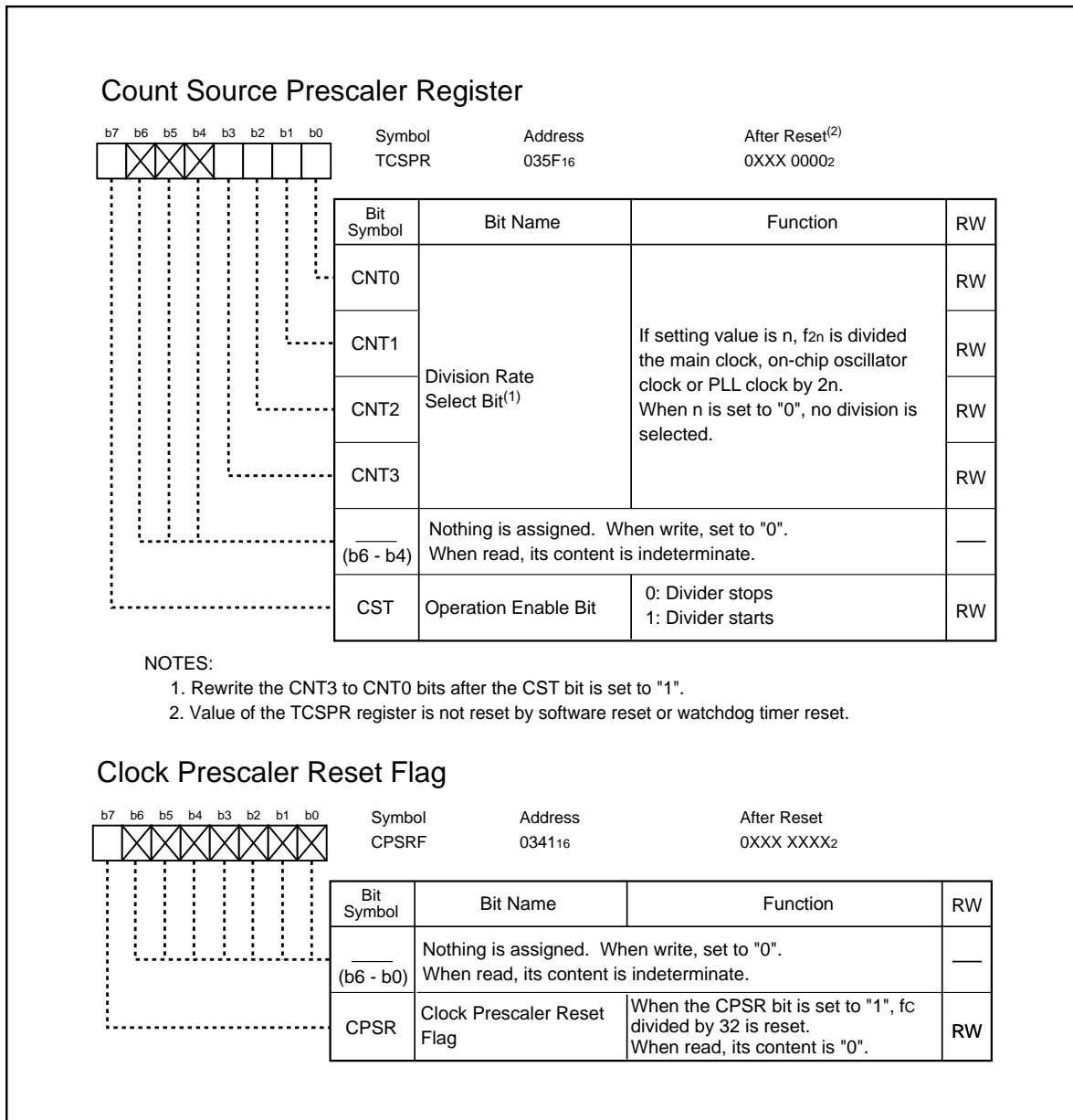


Figure 8.6 TCSR and CPSRF Registers

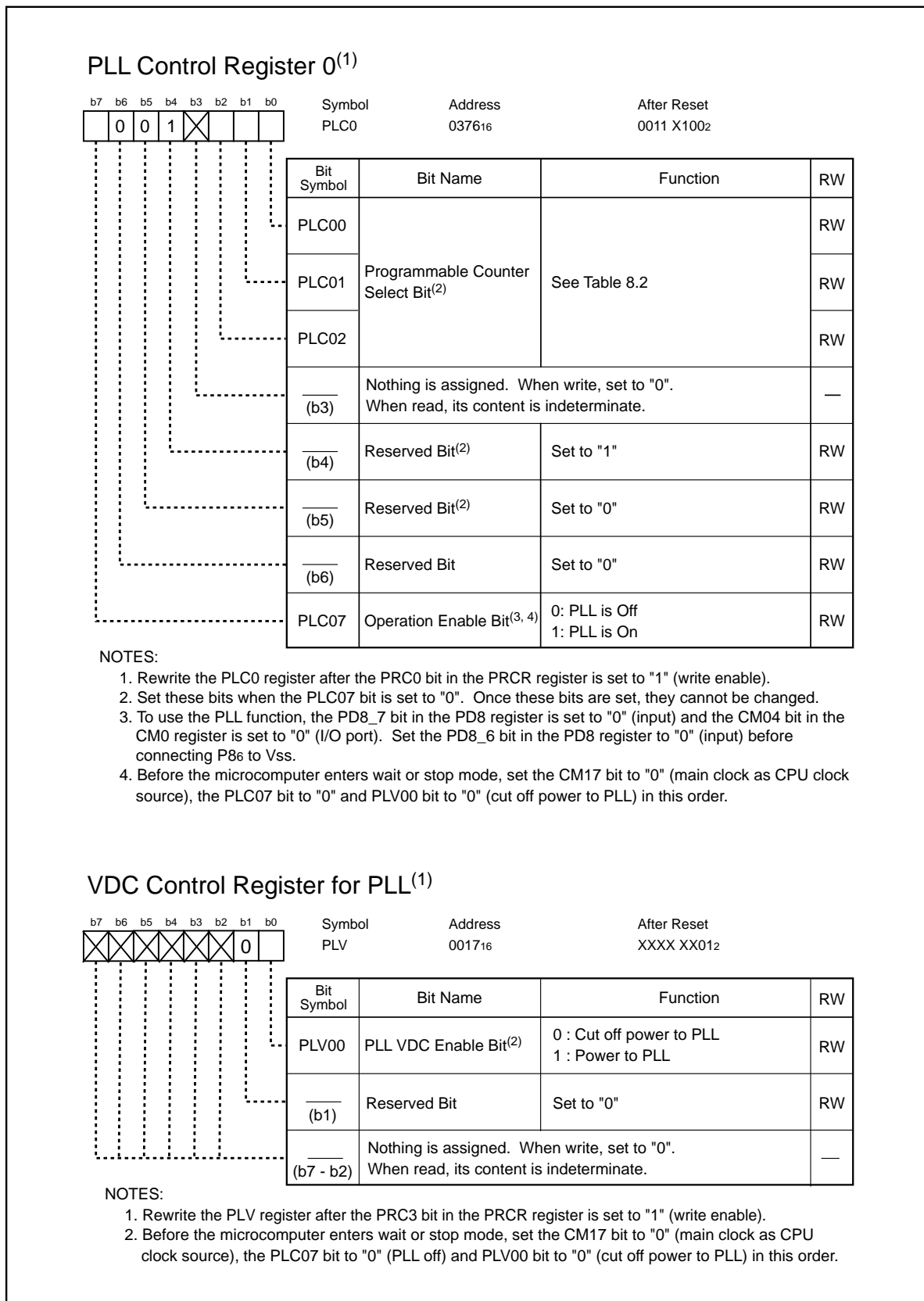


Figure 8.7 PLC0 and PLV Registers

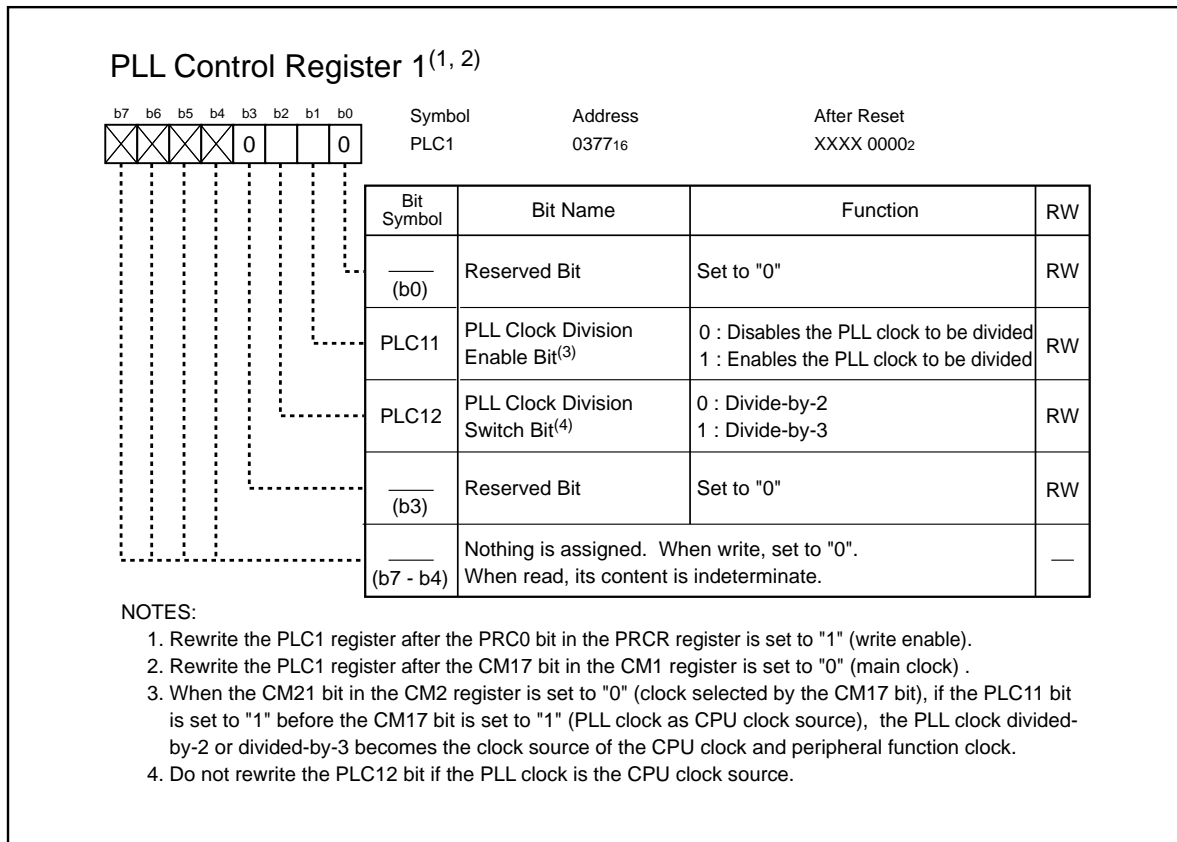


Figure 8.8 PLC1 Register

8.1.1 Main Clock

Main clock oscillation circuit generates the main clock. The main clock becomes a clock source for the CPU clock and peripheral function clock.

The main clock oscillation circuit is configured by connecting an oscillator or resonator between the XIN and XOUT pins. The circuit has a built-in feedback resistor. The feedback resistor is separated from the oscillation circuit in stop mode to reduce power consumption. The externally generated clock can be input to the XIN pin in the main clock oscillation circuit. Figure 8.9 shows an example of a main clock circuit connection. Circuit constants vary with each oscillator. Use the circuit constant recommended by each oscillator manufacturer.

The main clock divided-by-eight becomes the CPU clock after reset.

To reduce power consumption, set the CM05 bit in the CM0 register to "1" (main clock stopped) after switching the CPU clock source to the sub clock or on-chip oscillator clock. In this case, XOUT becomes "H". XIN is pulled up by XOUT via the feedback resistor which remains on. When an externally generated clock is input to the XIN pin, the main clock does not stop even if the CM05 bit is set to "1". Terminate main clock operation externally if necessary.

All clocks, including the main clock, stop in stop mode. Refer to **8.5 Power Consumption Control** for details.

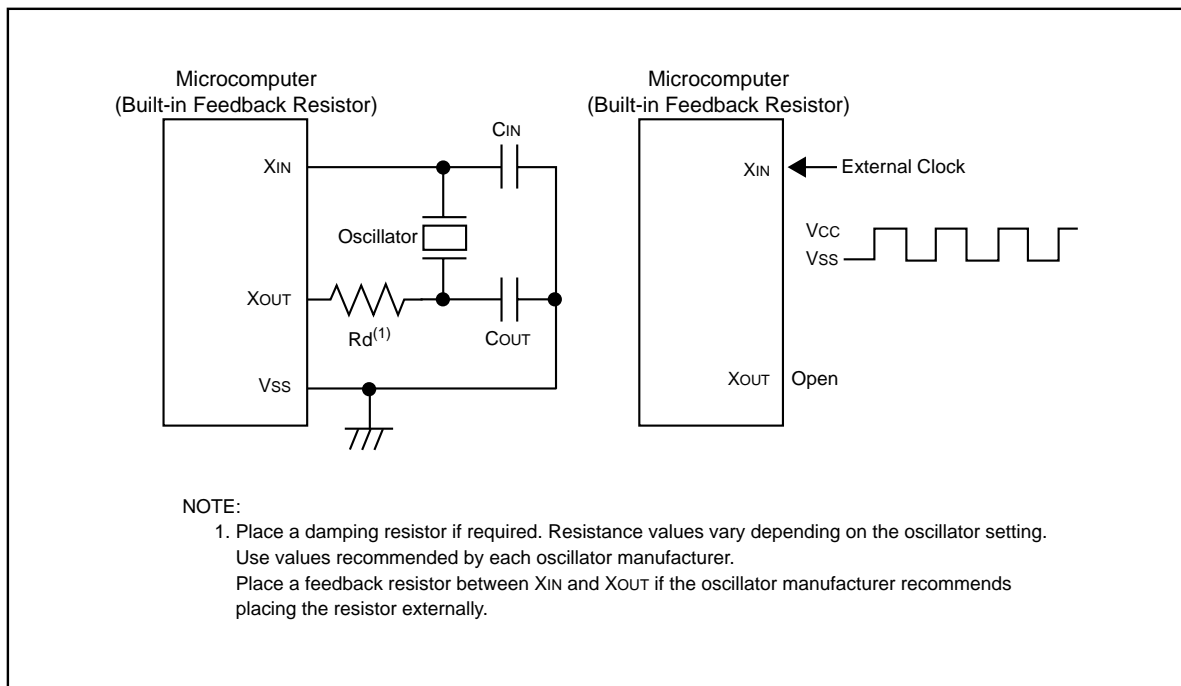


Figure 8.9 Main Clock Circuit Connection

8.1.2 Sub Clock

Sub clock oscillation circuit generates the sub clock. The sub clock becomes a clock source for the CPU clock and a count source for the timers A and B. The same frequency, f_c , as the sub clock can be output from the CLKOUT pin.

The sub clock oscillation circuit is configured by connecting a crystal oscillator between the XCIN and XCOUT pins. The circuit has a built-in feedback resistor. The feedback resistor is separated from the oscillation circuit in stop mode to reduce power consumption. The externally generated clock can be applied to the XCIN pin. Figure 8.10 shows an example of a sub clock circuit connection. Circuit constants vary with each oscillator. Use the circuit constant recommended by each oscillation manufacturer.

The sub clock stops after reset. The feedback resistor is separated from the oscillation circuit. When the PD8_6 and PD8_7 bits in the PD8 register are set to "0" (input mode) and the PU25 bit in the PUR2 register is set to "0" (no pull-up), set the CM04 bit in the CM0 register to "1" (XCIN-XCOUT oscillation function). The sub clock oscillation circuit starts oscillating. To apply the external clock to the XCIN pin, set the CM04 bit to "1" when the PD8_6 bit is set to "0" and the PU25 bit to "0". The clock applied to the XCIN pin becomes the clock source for the sub clock.

When the CM07 bit in the CM0 register is set to "1" (sub clock) after the sub clock oscillation has stabilized, the sub clock becomes the CPU clock.

All clocks, including the sub clock, stop in stop mode. Refer to **8.5 Power Consumption Control** for details.

XCIN shares pins with VCONT and XCOUT shares pins with P86. The sub clock and PLL frequency synthesizer cannot be used simultaneously.

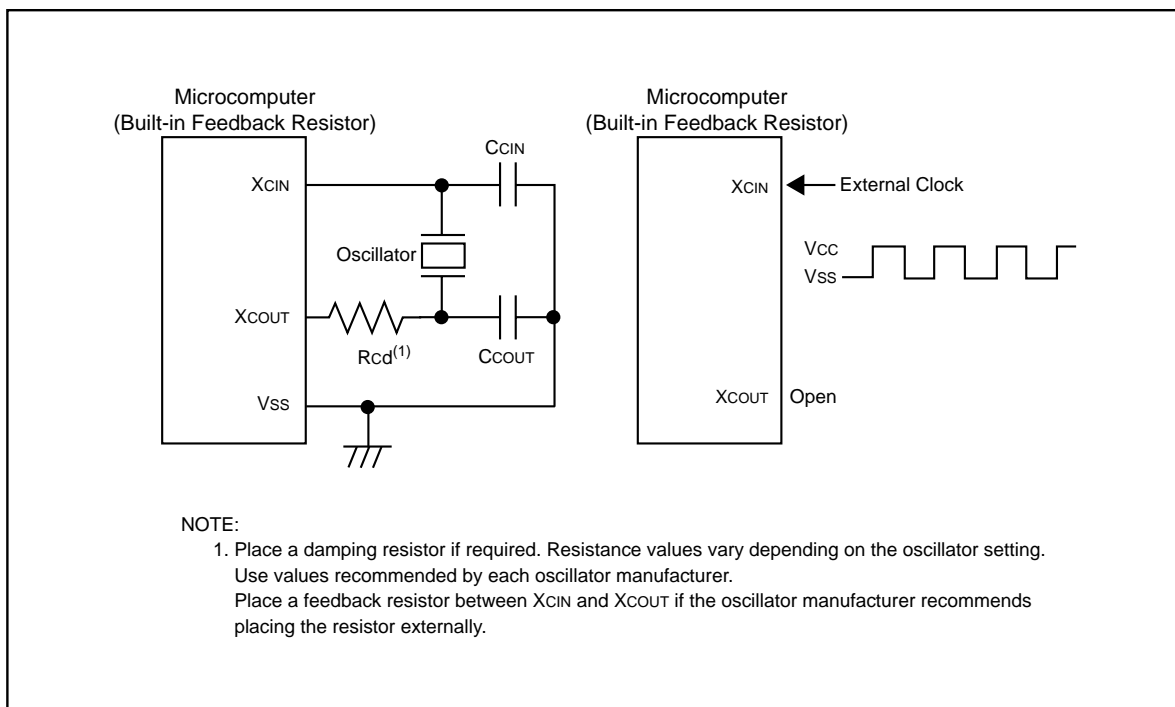


Figure 8.10 Sub Clock Connection Circuit

8.1.3 On-chip Oscillator Clock

On-chip oscillator generates the on-chip oscillator clock. The 1MHz on-chip oscillator clock becomes a clock source for the CPU clock and peripheral function clock.

The on-chip oscillator clock stops after reset. When the CM21 bit in the CM2 register is set to "1" (on-chip oscillator clock), the on-chip oscillator starts oscillating. Instead of the main clock, the on-chip oscillator clock becomes the clock source for the CPU clock and peripheral function clock.

8.1.3.1 Oscillation Stop Detect Function

When the main clock is terminated by external factors, the on-chip oscillator automatically starts oscillating to generate another clock.

When the CM 20 bit is set to "1" (oscillation stop detect function enabled), the oscillation stop detect interrupt request is generated as soon as the main clock stops. Simultaneously, the on-chip oscillator starts oscillating. The on-chip oscillator clock takes place of the main clock as the clock source for the CPU clock and peripheral function clock. Associated bits are set as follows:

- CM21 bit = 1 (on-chip oscillator clock becomes the clock source of the CPU clock.)
- CM22 bit = 1 (main clock stop is detected.)
- CM23 bit = 1 (main clock stops) (See **Figure 8.15**)

8.1.3.2 How to Use Oscillation Stop Detect Function

- The oscillation stop detect interrupt shares vectors with the watchdog timer interrupt. When both oscillation stop detect interrupt and watchdog timer interrupt are used, read the CM22 bit with an interrupt service routine to determine which interrupt request has been generated.
- When the main clock resumes running after an oscillation stop is detected, set the main clock as the clock source for the CPU clock and peripheral function clock. Figure 8.11 shows the procedure to switch the on-chip oscillator clock to the main clock.
- In low-speed mode, when the main clock is stopped by setting the CM20 bit to "1", the oscillation stop detect interrupt request is generated. Simultaneously, the on-chip oscillator starts oscillating. The sub clock remains the CPU clock. The on-chip oscillator clock becomes the clock source for the peripheral function clock.
- To enter wait mode while the oscillation stop detect interrupt function is in use, set the CM02 bit to "0" (peripheral function clock does not stop in wait mode).
- When the oscillation stop detect interrupt request is generated in wait mode, wait mode cannot be exited by the oscillation stop detect interrupt. After the microcomputer exits wait mode, the oscillation stop detect interrupt is acknowledged first, followed by the interrupt used to exit wait mode.
- The oscillation stop detect function is provided to handle main clock stop caused by external factors. Set the CM20 bit to "0" (oscillation stop detect function disabled) when the main clock is terminated by program, i.e., entering stop mode or setting the CM05 bit is set to "1" (main clock oscillation stop).
- When the main clock frequency is 2MHz or less, the oscillation stop detect function is not available. Set the CM20 bit to "0".

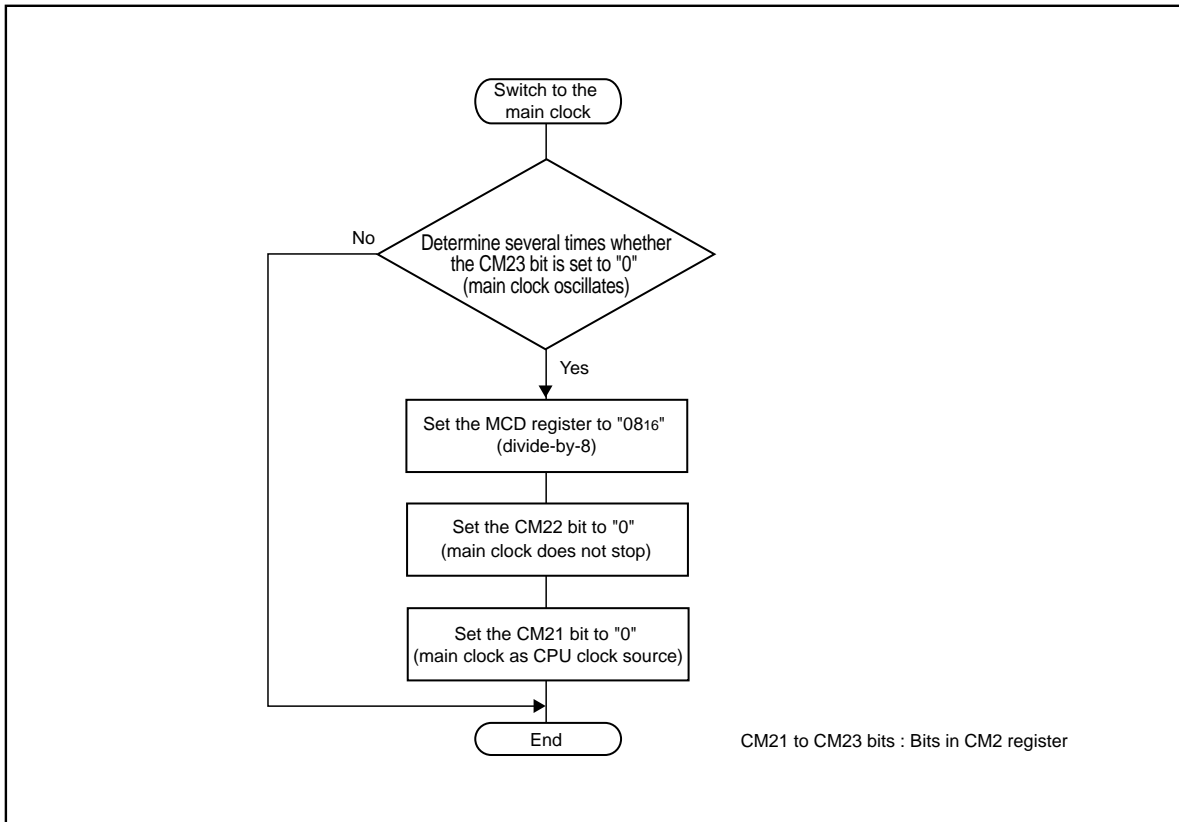


Figure 8.11 Switching Procedure from On-chip Oscillator Clock to Main Clock

8.1.4 PLL Clock

The PLL frequency synthesizer generates the PLL clock based on the main clock. The PLL clock can be used as a clock source for the CPU clock or peripheral function clock.

Connect a resistor and capacitor to the VCONT pin when using the PLL frequency synthesizer.

Set the PD8_6 and PD8_7 bits in the PD8 register to "0" (input mode) and the CM04 bit to "0" (the XCIN and XCOUT pins as ports). After that, connect the VCONT pin, the P86 pin, and the VSS pin to the circuit as is shown in Figure 8.12. Set the PLV00 bit in the PLV register to "1" (power to PLL).

The PLL frequency synthesizer stops after reset. When the PLC07 bit is set to "1" (PLL on), the PLL frequency synthesizer starts operating. Wait 20 ms (5 V operation) to 50 ms (3.3 V operation) for the PLL clock to stabilize.

The PLL clock can either be the clock output from the voltage controlled oscillator (VCO) divided-by-2 or divided-by-3.

When the PLL clock is used as a clock source for the CPU clock or peripheral function clock, set each bit as is shown in Table 8.2. Figure 8.13 shows the procedure for using the PLL clock as the CPU clock source.

To enter wait or stop mode, set the CM17 bit to "0" (main clock as CPU clock source). Set the PLC07 bit in the PLC0 register to "0" (PLL off) and the PLV00 bit to "0" (no power to PLL) before the microcomputer enters wait or stop mode.

The VCONT and P86 pins share pins with XCIN and XCOUT pins. When the PLL frequency synthesizer is being used, the sub clock cannot be used.

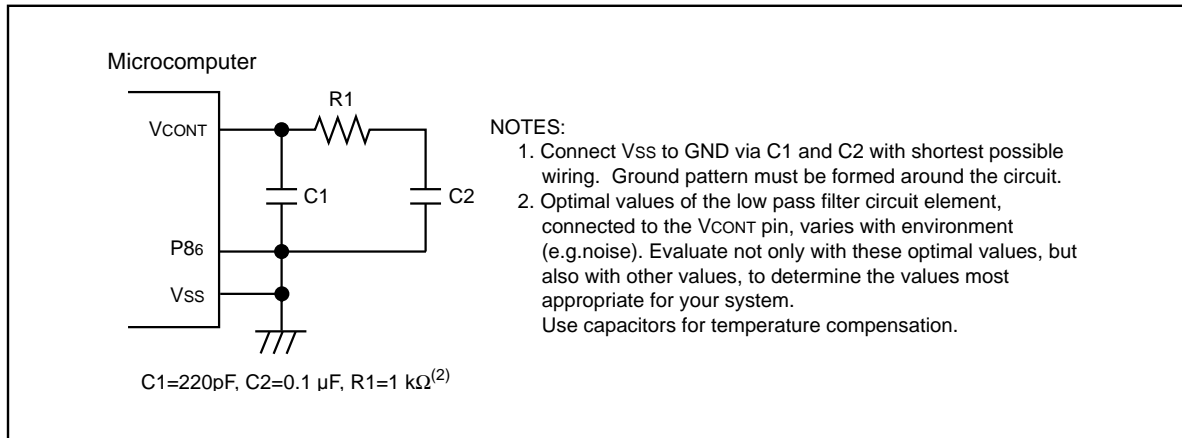


Figure 8.12 External Circuit with PLL Frequency Synthesizer

Table 8.2 Bit Settings to Use PLL Clock as CPU Clock Source

f(XIN)	PLC0 Register			PLC1 Register	PLL Clock
	PLC02	PLC01	PLC00	PLC12	
10MHz	0	1	1	0	30 MHz
				1	20 MHz
8MHz	1	0	0	0	32MHz
				1	21.3MHz

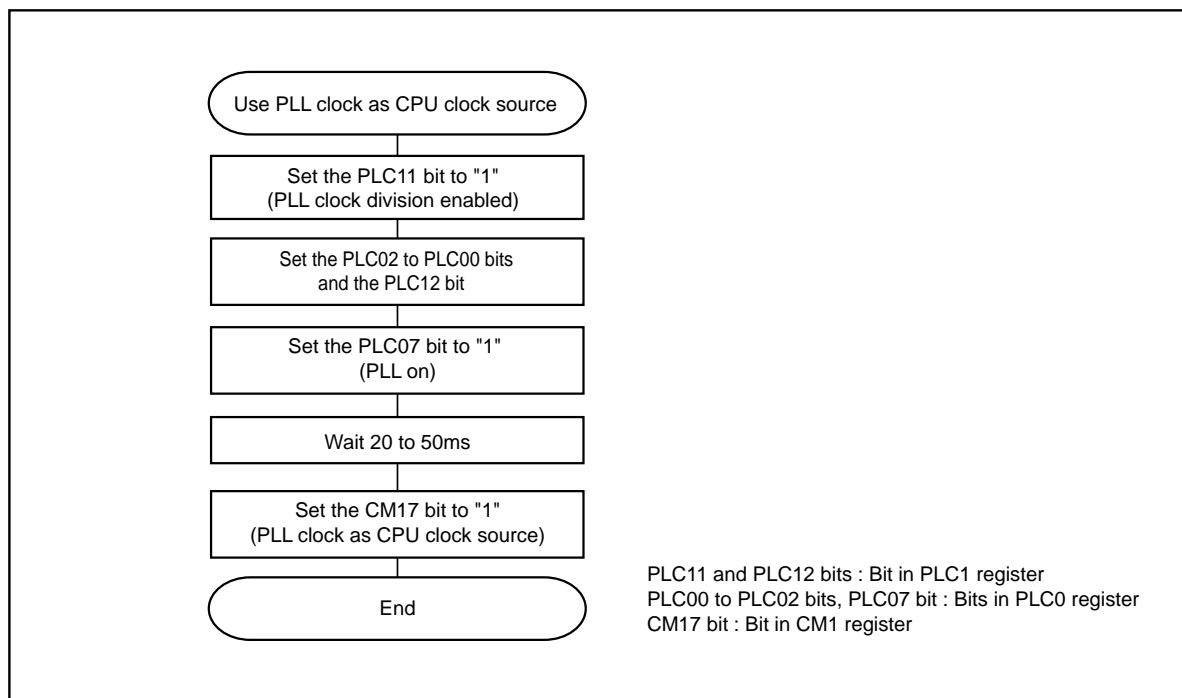


Figure 8.13 Procedure to Use PLL Clock as CPU Clock Source

8.2 CPU Clock and BCLK

The CPU operation clock is referred to as the CPU clock. The CPU clock is also the count source for the watchdog timer. After reset, the CPU clock is the main clock divided-by-8. In memory expansion or micro-processor mode, the clock having the same frequency as the CPU clock can be output from the BCLK pin as BCLK. Refer to **8.4 Clock Output Function** for details.

The main clock, sub clock, on-chip oscillator clock or PLL clock can be selected as a clock source for the CPU clock. Table 8.3 shows CPU clock source and bit settings.

When the main clock, on-chip oscillator clock or PLL clock is selected as a clock source of the CPU clock, the selected clock divided-by-1 (no division), -2, -3, -4, -6, -8, -10, -12, -14 or -16 becomes the CPU clock. The MCD register selects the clock division.

When the microcomputer enters stop mode or low-power consumption mode (except when the on-chip oscillator clock is the CPU clock), the MCD register is set to "0816" (divide-by-8 mode). Therefore, when the main clock starts running, the CPU clock enters middle-speed mode (divide-by-8).

Table 8.3 CPU Clock Source and Bit Settings

CPU Clock Source	CM0 Register	CM2 Register	CM1 Register
	CM07	CM21	CM17
Main Clock	0	0	0
Sub Clock	1	0	0
On-chip Oscillator Clock	0	1	0
PLL Clock	0	0	1

8.3 Peripheral Function Clock

The peripheral function clock becomes the operation clock or count source for peripheral functions excluding the watchdog timer.

8.3.1 f1, f8, f32 and f2n

f1, f8, f32 and f2n are the main clock⁽¹⁾ or on-chip oscillator clock divided-by-1, -8, -32, or -2n (n=1 to 15. No division when n=0). The CM21 bit determines which clock is selected.

When the CM02 bit is set to "1" (peripheral function stops in wait mode) when entering wait mode, f1, f8, f32 and f2n stop running. These clocks also stop in low-power consumption mode.

f1, f8 and f2n are used as the operation clock for the serial I/O and the count source for timers A and B. The CNT3 to CNT0 bits in the TCSPR register selects a f2n division. f1 is also used as the operation clock for the intelligent I/O.

The CLKOUT pin outputs f8 and f32. Refer to **8.4 Clock Output Function** for details.

8.3.2 fAD

fAD is the operation clock for the A/D convertor and has the same frequency as the main clock⁽¹⁾ and on-chip oscillator clock. The CM21 bit determines which clock is selected.

When the CM02 bit is set to "1" (peripheral function stop in wait mode) when entering wait mode, fAD stops. fAD also stops in low-power consumption mode.

NOTES:

1. When the CM17 bit is set to "1" (PLL clock as CPU clock source), the PLL clock is the main clock.

8.3.3 fc32

fc32 is the sub clock divided by 32. fc32 is used for as a count source for the timers A and B. fc32 is available when the sub clock is running.

8.4 Clock Output Function

The CLKOUT pin outputs fc, f8 or f32.

In memory expansion and microprocessor modes, a clock having the same frequency as the CPU clock can be output from the BCLK pin as BCLK.

Table 8.4 lists CLKOUT pin function in single-chip mode. Table 8.5 lists CLKOUT pin functions in memory expansion and microprocessor modes.

Table 8.4 CLKOUT Pin in Single-Chip Mode

PM0 Register (1)		CM0 Register (2)		CLKOUT Pin Function
PM07		CM01	CM00	
—		0	0	P53 I/O port
1		0	1	Outputs fc
1		1	0	Outputs f8
1		1	1	Outputs f32

- : Can be set to either "0" or "1"

NOTES:

1. Rewrite the PM0 register after the PRC1 bit in the PRCR register is set to "1" (write enable)
2. Rewrite the CM0 register after the PRC0 bit in the PRCR register is set to "1" (write enable)

Table 8.5 BCLK/CLKOUT Pin in Memory Expansion Mode and Microprocessor Mode⁽⁴⁾

PM1 Register(1)		PM0 Register(1)		CM0 Register(2)		CLKOUT Pin Function
PM15	PM14	PM07		CM01	CM00	
002, 102, 112,		0		0 (3)	0 (3)	Outputs BCLK
		1		0	0	Outputs "L" (not P53)
		1		0	1	Outputs fc
		1		1	0	Outputs f8
		1		1	1	Outputs f32
0	1	—		0 (3)	0 (3)	Outputs ALE

- : Can be set to either "0" or "1"

NOTES:

1. Rewrite the PM0 and PM1 register after the PRC1 bit in the PRCR register is set to "1" (write enable)
2. Rewrite the CM0 register after the PRC0 bit in the PRCR register is set to "1" (write enable)
3. When the PM07 bit is set to "0" (selected in the CM01 to CM00 bits) or the PM15 to PM14 bits are set to "012" (P53/BCLK), set the CM01 to CM00 bits to "002" (I/O port P53)
4. M32C/83T cannot be used in memory expansion mode and microprocessor mode.

8.5 Power Consumption Control

Normal operation mode, wait mode and stop mode are provided as the power consumption control.

All mode states, except wait mode and stop mode, are called normal operation mode in this document.

Figure 8.14 shows a block diagram of status transition in wait mode and stop mode. Figure 8.15 shows a block diagram of status transition in all modes.

8.5.1 Normal Operation Mode

The normal operation mode is further separated into six modes.

In normal operation mode, the CPU clock and peripheral function clock are supplied to operate the CPU and peripheral function. The power consumption control is enabled by controlling the CPU clock frequency. The higher the CPU clock frequency, the more processing power increases. The lower the CPU clock frequency, the more power consumption decreases. When unnecessary oscillation circuits stop, power consumption is further reduced.

8.5.1.1 High-Speed Mode

The main clock⁽¹⁾ becomes the CPU clock and the clock source for the peripheral function clock. When the sub clock runs, fc32 can be used as a count source for the timers A and B.

8.5.1.2 Medium-Speed Mode

The main clock divided-by-2, -3, -4, -6, -8, -10, -12, -14, or -16 becomes the CPU clock. The main clock is the clock source for the peripheral function clock. When the sub clock runs, fc32 can be used as the count source for the timers A and B.

8.5.1.3 Low-Speed Mode

The sub clock becomes the CPU clock. The main clock is the count source for the peripheral function clock. fc32 can be used as the count source for the timers A and B.

8.5.1.4 Low-Power Consumption Mode

The microcomputer enters low-power consumption mode when the main clock stops in low-speed mode. The sub clock becomes the CPU clock. fc32 can be used as the count source for timers A and B. Only fc32 can be used as the peripheral function clock. In low-power consumption mode, the MCD register is set to "0816" (divide-by-8 mode). Therefore, when the main clock resumes running, the microcomputer is in middle-speed mode (divide-by-8 mode).

8.5.1.5 On-chip Oscillator Mode

The on-chip oscillator clock divided-by-1(no division), -2, -3, -4, -6, -8, -10, -12, -14, or -16 becomes the CPU clock. The on-chip oscillator clock is the clock source for the peripheral function clock. When the sub clock runs, fc32 can be used as the count source for the timers A and B.

8.5.1.6 On-chip Oscillator Low-Power Consumption Mode

The microcomputer enters on-chip oscillator low-power consumption mode when the main clock stops in on-chip oscillator mode. The on-chip oscillator clock divided-by-1(no division), -2, -3, -4, -6, -8, -10, -12, -14, or -16 becomes the CPU clock. The on-chip oscillator clock is the clock source for the peripheral function clock. When the sub clock runs, fc32 can be used as the count source for the timers A and B.

Switch the CPU clock after the clock to be switched to stabilizes. Sub clock oscillation will take longer⁽²⁾ to stabilize. Wait, by program, until the clock stabilizes directly after running the microcomputer on or exiting stop mode.

To switch the on-chip oscillator to the main clock, enter medium-speed mode (divide-by-8) after the main clock is divided by eight in on-chip oscillator mode (MCD register=0816).

Do not enter on-chip oscillator mode or on-chip oscillator low-power consumption mode from low-speed mode or low-power consumption mode and vice versa.

NOTES:

1. When the CM17 bit is set to "1" (PLL clock as CPU clock source), the PLL clock is the main clock .
2. Contact your oscillator manufacturer for oscillation stabilization time.

8.5.2 Wait Mode

In wait mode, the CPU clock stops running. The CPU and watchdog timer, operated by the CPU clock, also stop. Because the main clock, sub clock and on-chip oscillator clock continue running, peripheral functions using these clocks also continue operating.

8.5.2.1 Peripheral Function Clock Stop Function

If the CM02 bit is set to "1" (peripheral function clock stops in wait mode), f1, f8, f32, f2n and fAD stop in wait mode. Power consumption can be reduced because the peripheral function that has f1, f8, f32, f2n, or fAD as a count source stops. fc32 does not stop running.

8.5.2.2 Entering Wait Mode

Follow the procedure below to enter wait mode.

- Initial Setting

Set each interrupt priority level after setting the exit priority level required to exit wait mode, controlled by the RLVL2 to RLVL0 bits in the RLVL register, to "7".

- Before Entering Wait Mode

- (1) Set the I flag to "0"
- (2) Set the interrupt priority level of the interrupt being used to exit wait mode
- (3) Set the interrupt priority levels of the interrupts, not being used to exit wait mode, to "0"
- (4) Set the IPL in the FLG register. Then set the exit priority level to the same level as IPL (Interrupt priority level of the interrupt used to exit wait mode > exit priority level ≥ interrupt priority level of the interrupts not used to exit wait mode)
- (5) Set the PRC0 bit in the PRCR register to "1" (write enable)
- (6) If the CPU clock source is the PLL clock, set the CM17 bit in the CM1 register to "0" (main clock), the PLC07 bit in the PLC0 register to "0" (PLL off), and the PLV00 bit in the PLV register to "0" (cut off power to PLL)
- (7) Set the I flag to "1"
- (8) Execute the WAIT instruction

- After Exiting Wait Mode

Set the interrupt priority level required to exit wait mode to "7" immediately after exiting wait mode.

8.5.2.3 Pin Status in Wait Mode

Table 8.6 lists pin states in wait mode.

Table 8.6 Pin Status in Wait Mode

Pin		Memory Expansion Mode Microprocessor Mode	Single-Chip Mode
Address Bus, Data Bus, CS ₀ to CS ₃ , BHE		Maintains state immediately before entering wait mode	/
RD, WR, WRL, WRH, DW, CASL, CASH		"H" (1)	
RAS		"H" (1)	
HLDA, BCLK		"H"	
ALE		"L"	
Port		Maintains state immediately before entering wait mode	
CLKOUT	When fc is selected	Outputs clock	
	When f8, f32 are selected	The clock is output when the CM02 bit in the CM0 register is set to "0" (peripheral function clock not stop in wait mode). Maintains state immediately before entering wait mode when the CM02 bit is set to "1" (peripheral function clock stopped in wait mode).	

NOTES:

1. When performing a self-refresh operation using the DRAMC, $\overline{\text{CAS}}$ and $\overline{\text{RAS}}$ become low ("L").
2. M32C/83T cannot be used in memory expansion mode and microprocessor mode.

8.5.2.4 Exiting Wait Mode

Wait mode is exited by the hardware reset, $\overline{\text{NMI}}$ interrupt or peripheral function interrupts.

When the hardware reset or $\overline{\text{NMI}}$ interrupt, but not the peripheral function interrupts, is used to exit wait mode, set the ILVL2 to ILVL0 bits for the peripheral function interrupts to "0002" (interrupt disabled) before executing the WAIT instruction.

The CM02 bit affects the peripheral function interrupts. When the CM02 bit is set to "0" (peripheral function clock does not stop in wait mode), all peripheral function interrupts can be used to exit wait mode. When the CM02 bit is set to "1" (peripheral function clock stops in wait mode), peripheral functions using the peripheral function clock stop. Therefore, the peripheral function interrupts cannot be used to exit wait mode. However, peripheral function interrupts caused by an external signal can be used to exit wait mode.

The CPU clock used when exiting wait mode by the peripheral function interrupts or $\overline{\text{NMI}}$ interrupt is the same CPU clock used when WAIT instructions are executed.

Table 8.7 shows interrupts to be used to exit wait mode and usage conditions.

Table 8.7 Interrupts to Exit Wait Mode

Interrupt	When CM02=0	When CM02=1
NMI Interrupt	Available	Available
Serial I/O Interrupt	Available when the internal and external clocks are used	Available only when the external clock is used
Key Input Interrupt	Available	Available
A/D Conversion Interrupt	Available in single or single-sweep mode	Do not use
Timer A Interrupt Timer B Interrupt	Available in all modes	Available in event counter mode or when the count source is fc32
$\overline{\text{INT}}$ Interrupt	Available	Available
CAN Interrupt	Available	Do not use
Intelligent I/O Interrupt	Available	Do not use

8.5.3 Stop Mode

In stop mode, all oscillators and resonators stop. The CPU clock and peripheral function clock, as well as the CPU and peripheral functions operated by these clocks, also stop. The least power required to operate the microcomputer is in stop mode. The internal RAM holds its data if the voltage applied to the Vcc pin is 2.5V or more.

Interrupts used to exit stop mode are $\overline{\text{NMI}}$ interrupt, key input interrupt, and $\overline{\text{INT}}$ interrupt.

8.5.3.1 Entering Stop Mode

Stop mode is entered when setting the CM10 bit in the CM1 register to "1" (all clocks stops). The MCD4 to MCD0 bits in the MCD register become set to "010002" (divide-by-8 mode).

Enter stop mode after setting the followings.

- Initial Setting
 - Set each interrupt priority level after setting the minimum interrupt priority level required to exit stop or wait mode, controlled by the RLVL2 to RLVL0 bits in the RLVL register, to "7".
- Before Entering Stop Mode
 - (1) Set the I flag to "0"
 - (2) Set the interrupt priority level of the interrupt being used to exit stop mode
 - (3) Set the interrupt priority levels of the interrupts, not being used to exit stop mode, to "0"
 - (4) Set IPL in the FLG register. Then set the exit priority level to the same level as IPL
 - (Interrupt priority level of the interrupt used to exit stop mode > interrupt priority level to exit stop mode \geq interrupt priority level of the interrupts not used to exit stop mode)
 - (5) Set the PRC0 bit in the PRCR register to "1" (write enabled)
 - (6) Select the main clock as the CPU clock
 - When the CPU clock source is the sub clock,
 - Set the CM05 bit in the CM0 register to "0" (main clock oscillates) and CM07 bit in the CM0 register to "0" (clock selected by the CM21 bit divided by MCD register setting)
 - When the CPU clock source is the PLL clock,
 - Set the CM17 bit in the CM1 register to "0" (main clock) and the PLC07 bit in the PLC0 register to "0" (PLL off)
 - When the CPU clock source is the on-chip oscillator clock,
 - Set the MCD4 to MCD0 bits to "010002" (divide-by-8 mode), the CM05 bit to "0" (main clock oscillates), and the CM21 bit in the CM2 register to "0" (clock selected by the CM17 bit)

- (7) The oscillation stop detect function is used, set the CM20 bit in the CM2 register to "0" (oscillation stop detect function disabled)
- (8) Set the I flag to "1"
- (9) Set the CM10 bit to "1" (all clocks stops)
- After Exiting Stop Mode
Set the interrupt priority level required to exit stop mode to "7" immediately after exiting stop mode.

8.5.3.2 Exiting Stop Mode

Stop mode is exited by the hardware reset, $\overline{\text{NMI}}$ interrupt, or peripheral function interrupts (key input interrupt and $\overline{\text{INT}}$ interrupt).

When the hardware reset or $\overline{\text{NMI}}$ interrupt, but not the peripheral function interrupts, is used to exit wait mode, set all ILVL2 to ILVL0 bits in the interrupt control registers for the peripheral function interrupt to "0002" (interrupt disabled) before setting the CM10 bit to "1" (all clocks stops).

8.5.3.3 Pin Status in Stop Mode

Table 8.8 lists pin status in stop mode.

Table 8.8 Pin Status in Stop Mode

Pin		Memory Expansion Mode Microprocessor Mode ⁽²⁾	Single-Chip Mode
Address Bus, Data Bus, $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$, BHE		Maintains state immediately before entering stop mode	/
RD, WR, $\overline{\text{WRL}}$, $\overline{\text{WRH}}$, DW, CASL, CASH		"H" (1)	
RAS		"H" (1)	
$\overline{\text{HLDA}}$, BCLK		"H"	
ALE		"H"	
Port		Maintains state immediately before entering stop mode	
CLKOUT	When f _c selected	"H"	
	When f ₈ , f ₃₂ selected	Maintains state immediately before entering stop mode	
XIN		High-impedance	
XOUT		"H"	
XCIN, XCOUT		High-impedance	

NOTES:

1. When performing a self-refresh operation using DRAMC, $\overline{\text{CAS}}$ and $\overline{\text{RAS}}$ become low ("L").
2. M32C/83T cannot be used in memory expansion mode and microprocessor mode.

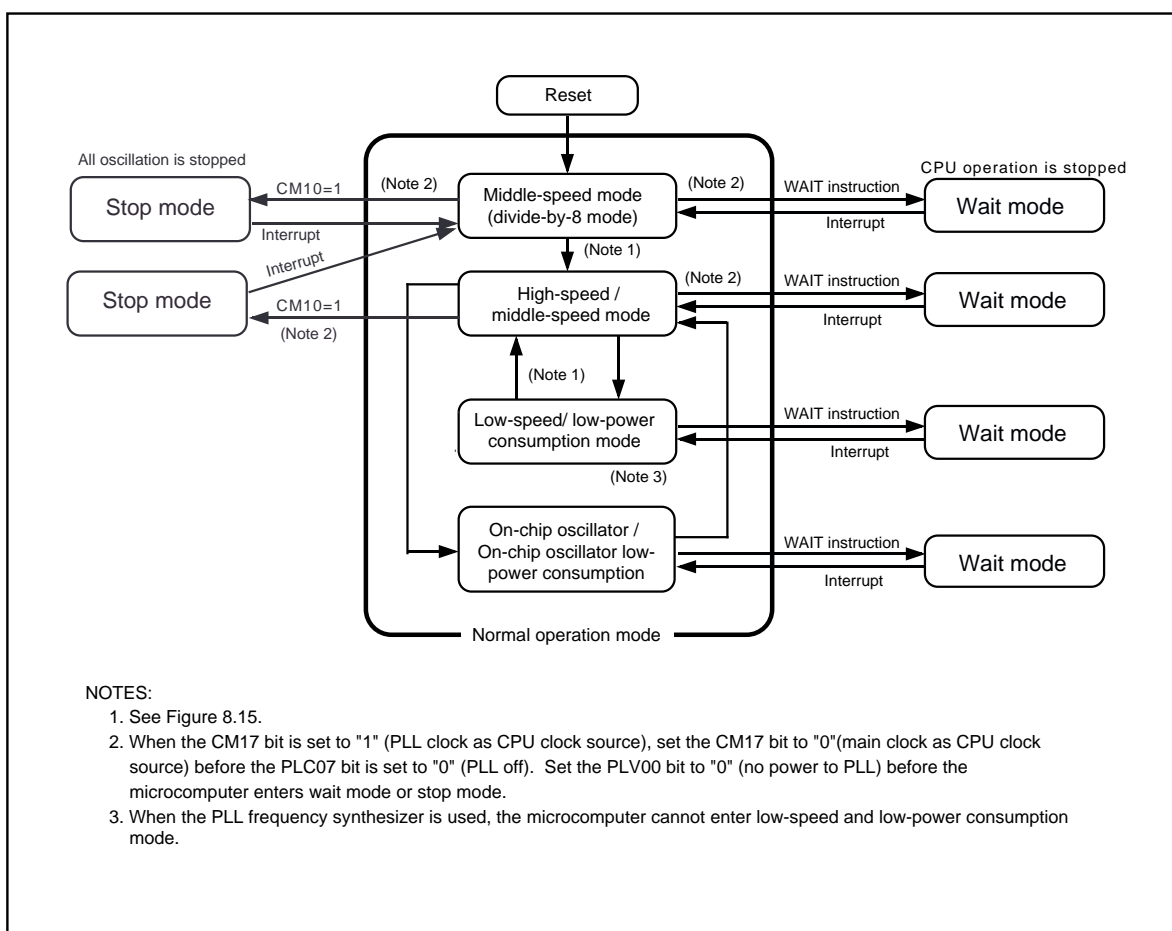


Figure 8.14 Status Transition in Wait Mode and Stop Mode

9. Protection

The protection function protects important registers from being easily overwritten when a program runs out of control.

Figure 9.1 shows the PRCR register. Each bit in the PRCR register protects the following registers:

- The PRC0 bit protects the CM0, CM1, CM2, MCD, PLC0 and PLC1 registers;
- The PRC1 bit protects the PM0, PM1, PM2, INVC0 and INVC1 registers;
- The PRC2 bit protects the PD9 and PS3 registers;
- The PRC3 bit protects the PLV and VDC0 registers.

The PRC2 bit is set to "0" (write disable) when data is written to a desired address after setting the PRC2 bit to "1" (write enable). Set the PD9 and PS3 registers immediately after setting the PRC2 bit in the PRCR register to "1" (write enable). Do not generate an interrupt or a DMA transfer between the instruction to set to the PRC2 bit to "1" and the following instruction. The PRC0, PRC1 and PRC3 bits are not set to "0" even if data is written to desired addresses. Set the PRC0, PRC1 and PRC3 bits to "0" by program.

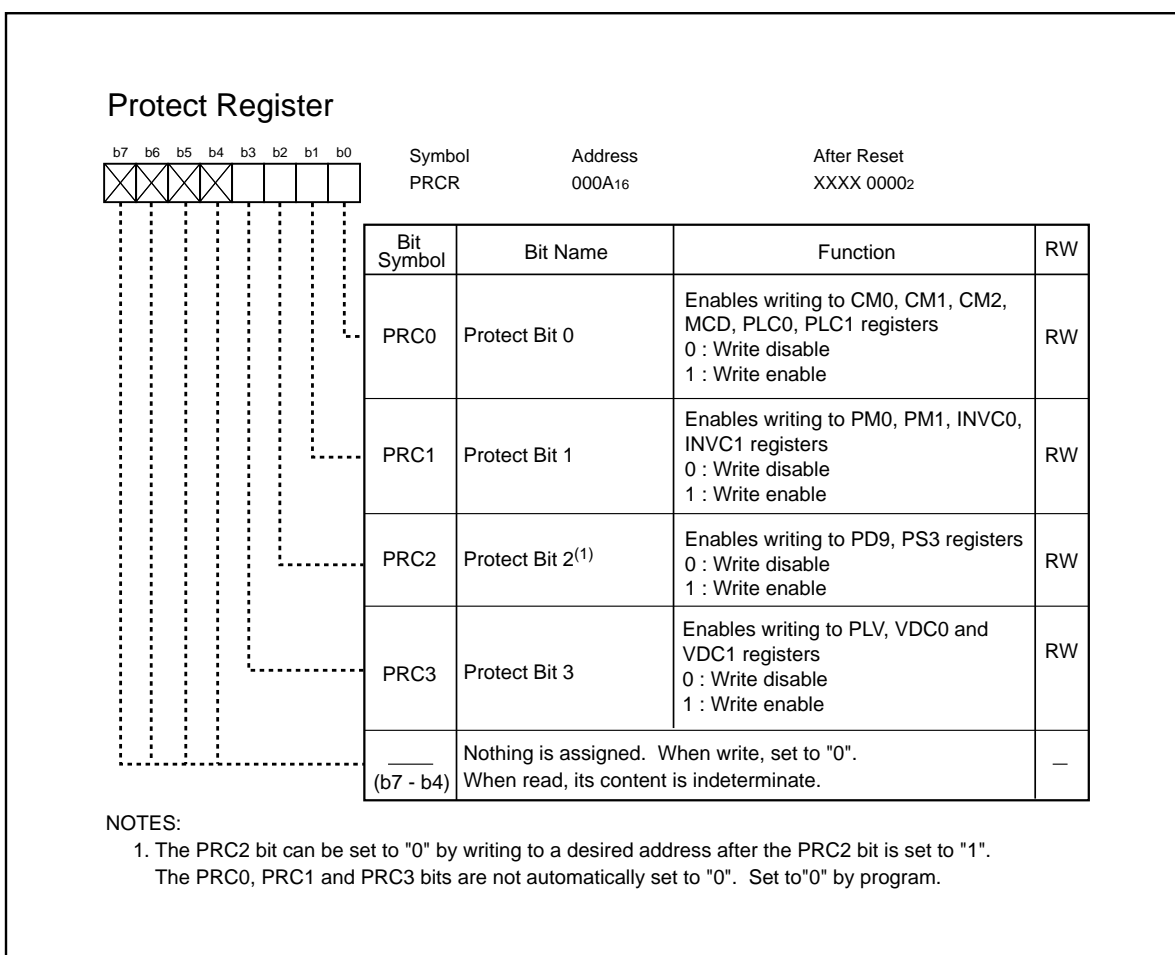


Figure 9.1 PRCR Register

10. Interrupts

10.1 Types of Interrupts

Figure 10.1 shows types of interrupts.

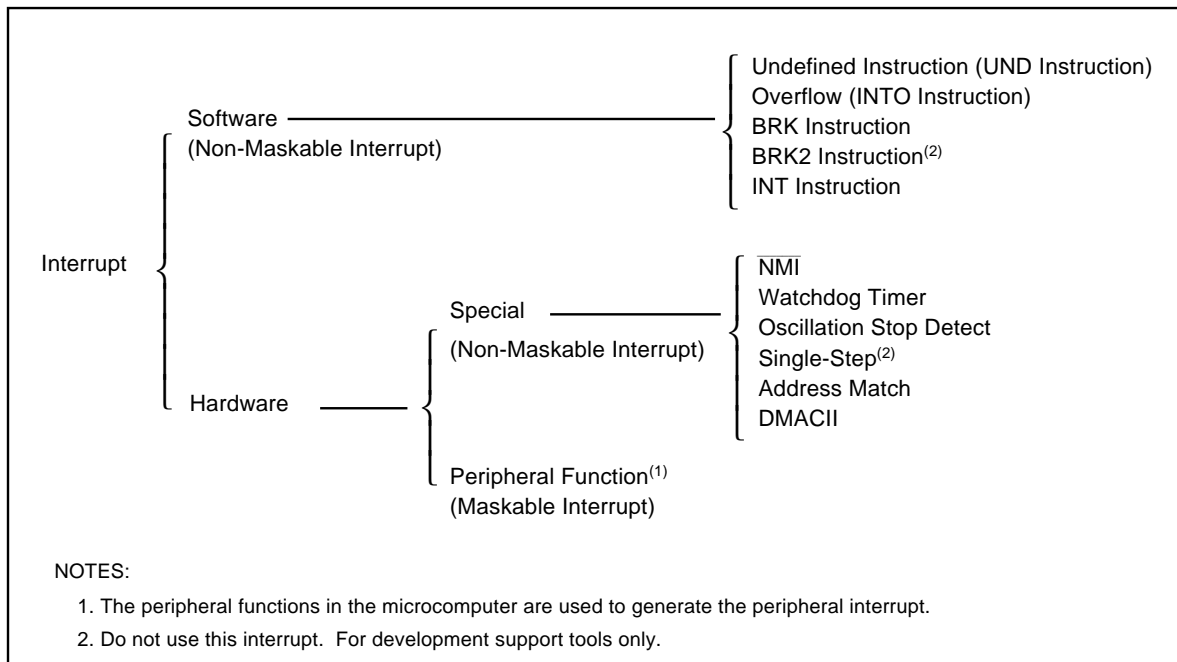


Figure 10.1 Interrupts

- Maskable Interrupt

The I flag enables or disables an interrupt.

The interrupt priority order based on interrupt priority level **can be changed**.

- Non-maskable Interrupt

The I flag does not enable nor disable an interrupt .

The interrupt priority order based on interrupt priority level **cannot be changed**.

10.2 Software Interrupts

Software interrupt occurs when an instruction is executed. The software interrupts are non-maskable interrupts.

10.2.1 Undefined Instruction Interrupt

The undefined instruction interrupt occurs when the UND instruction is executed.

10.2.2 Overflow Interrupt

The overflow interrupt occurs when the O flag in the FLG register is set to "1" (overflow of arithmetic operation) and the INTO instruction is executed.

Instructions to set the O flag are :

ABS, ADC, ADCF, ADD, ADDX, CMP, CMPX, DIV, DIVU, DIVX, NEG, RMPA, SBB, SCMPU, SHA, SUB, SUBX

10.2.3 BRK Interrupt

The BRK interrupt occurs when the BRK instruction is executed.

10.2.4 BRK2 Interrupt

The BRK2 interrupt occurs when the BRK2 instruction is executed.
Do not use this interrupt. For development support tools only.

10.2.5 INT Instruction Interrupt

The INT instruction interrupt occurs when the INT instruction is executed. The INT instruction can select software interrupt numbers 0 to 63. Software interrupt numbers 7 to 54, and 57 are assigned to the vector table used for the peripheral function interrupt. Therefore, the microcomputer executes the same service routine when the INT instruction is executed as when a peripheral function interrupt occurs.

When the INT instruction is executed, the FLG register and PC are saved to the stack. PC also stores the relocatable vector of the specified software interrupt number. Where the stack is saved varies, depending on the software interrupt number. ISP is selected as the stack for the software interrupt numbers 0 to 31 (the U flag is set to "0"). SP, which is set before the INT instruction is executed, is selected as the stack for the software interrupt numbers 32 to 63 (the U flag is not changed).

With the peripheral function interrupt, the FLG register is saved and the U flag is set to "0" (ISP select) when an interrupt request is acknowledged. With software interrupt numbers 32 to 54 and 57, the SP to be used varies, depending on whether the interrupt is generated by the peripheral function interrupt request or by the INT instruction.

10.3 Hardware Interrupts

Special interrupts and peripheral function interrupts are available as hardware interrupts.

10.3.1 Special Interrupts

Special interrupts are non-maskable interrupts.

10.3.1.1 $\overline{\text{NMI}}$ Interrupt

The $\overline{\text{NMI}}$ interrupt occurs when a signal applied to the $\overline{\text{NMI}}$ pin changes from an "H" signal to an "L" signal. Refer to **10.8 NMI Interrupt** for details.

10.3.1.2 Watchdog Timer Interrupt

The watchdog timer interrupt occurs when the count source of the watchdog timer underflows. Refer to **11. Watchdog Timer** for details.

10.3.1.3 Oscillation Stop Detection Interrupt

The oscillation stop detection interrupt occurs when the microcomputer detects a main clock oscillation stop. Refer to **8. Clock Generating Circuit** for details.

10.3.1.4 Single-Step Interrupt

Do not use the single-step interrupt. For development support tool only.

10.3.1.5 Address Match Interrupt

The address match interrupt occurs immediately before executing an instruction that is stored into an address indicated by the RMAD_i register (i=0 to 3) when the AIER_i bit in the AIER register is set to "1" (address match interrupt enabled). Set the starting address of the instruction in the RMAD_i register. The address match interrupt does not occur when a table data or addresses of the instruction other than the starting address, if the instruction has multiple addresses, is set. Refer to **10.10 Address Match Interrupt** for details.

10.3.2 Peripheral Function Interrupt

The peripheral function interrupt occurs when a request from the peripheral functions in the microcomputer is acknowledged. The peripheral function interrupts and software interrupt numbers 7 to 54 and 57 for the INT instruction use the same interrupt vector table. The peripheral function interrupt is a maskable interrupt.

See **Table 10.2** about how the peripheral function interrupt occurs. Refer to the descriptions of each function for details.

10.4 High-Speed Interrupt

The high-speed interrupt executes an interrupt sequence in five cycles and returns from the interrupt in 3 cycles.

When the FSIT bit in the RLV register is set to "1" (interrupt priority level 7 available for the high-speed interrupt), the ILVL2 to ILVL0 bits in the interrupt control registers can be set to "1112" (level 7) to use the high-speed interrupt.

Only one interrupt can be set as the high-speed interrupt. When using the high-speed interrupt, do not set multiple interrupts to interrupt priority level 7. Set the DMAII bit in the RLV register to "0" (interrupt priority level 7 available for interrupts).

Set the starting address of the high-speed interrupt service routine in the VCT register.

When the high-speed interrupt is acknowledged, the FLG register is saved to the SVF register and PC is saved to the SVP registers. The program is executed from an address indicated by the VCT register.

Execute the FREIT instruction to return from the high-speed interrupt service routine.

The values saved to the SVF and SVP registers are restored to the FLG register and PC by executing the FREIT instruction.

The high-speed interrupt and the DMA2 and DMA3 use the same register. When using the high-speed interrupt, neither DMA2 nor DMA3 is available. DMA0 and DMA1 can be used.

10.5 Interrupts and Interrupt Vectors

There are four bytes in one vector. Set the starting address of interrupt service routine in each vector table. When an interrupt request is acknowledged, the interrupt service routine is executed from the address set in the interrupt vectors. Figure 10.2 shows the interrupt vector.

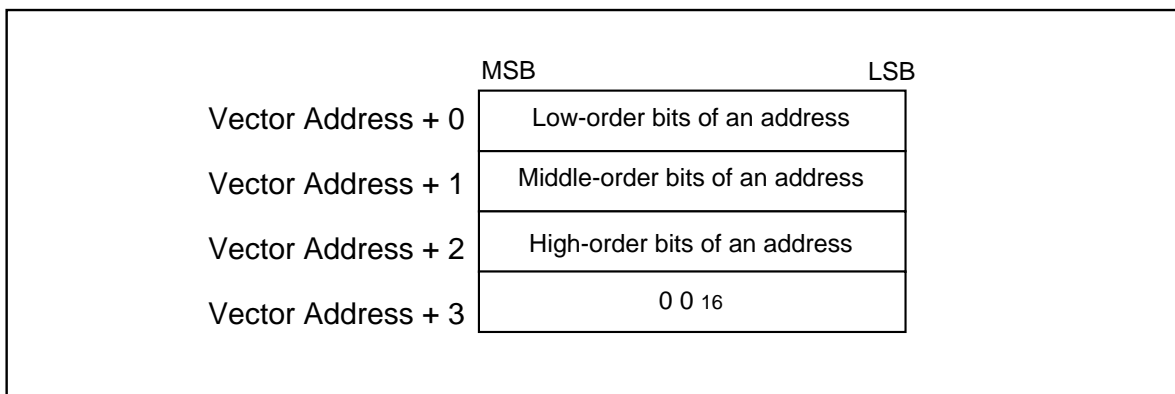


Figure 10.2 Interrupt Vector

10.5.1 Fixed Vector Tables

The fixed vector tables are allocated addresses FFFFDC₁₆ to FFFFFFF₁₆. Table 10.1 lists the fixed vector tables. Refer to **25.2 Functions to Prevent Flash Memory from Rewriting** for fixed vectors of the flash memory.

Table 10.1 Fixed Vector Table

Interrupt Generated by	Vector Addresses Address (L) to Address (H)	Remarks	Reference
Undefined Instruction	FFFFDC ₁₆ to FFFFDF ₁₆		M32C/80 series software manual
Overflow	FFFFE0 ₁₆ to FFFFFE3 ₁₆		
BRK Instruction	FFFFE4 ₁₆ to FFFFFE7 ₁₆	If the content of address FFFFFE7 ₁₆ is FF ₁₆ , the program is executed from the address stored into software interrupt number 0 in the relocatable vector table	
Address Match	FFFFE8 ₁₆ to FFFFFEB ₁₆		
-	FFFFEC ₁₆ to FFFFFEF ₁₆	Reserved space	
Watchdog Timer	FFFFF0 ₁₆ to FFFFF3 ₁₆	These addresses are used for the watchdog timer interrupt and the oscillation stop detect interrupt	Clock oscillation circuit, Watchdog timer
-	FFFFF4 ₁₆ to FFFFF7 ₁₆	Reserved space	
NMI	FFFFF8 ₁₆ to FFFFFB ₁₆		
Reset	FFFFFC ₁₆ to FFFFFFF ₁₆		Reset

10.5.2 Relocatable Vector Tables

The relocatable vector tables occupy 256 bytes from the starting address set in the INTB register. Table 10.2 lists the relocatable vector tables.

Set an even address as the starting address of the vector table set in the INTB register to increase interrupt sequence execution rate.

Table 10.2 Relocatable Vector Tables

Interrupt Generated by	Vector Table Address Address(L) to Address(H) ⁽¹⁾	Software Interrupt Number	Reference
BRK Instruction ⁽²⁾	+0 to +3 (0000 ₁₆ to 0003 ₁₆)	0	M32C/80 Series
Reserved Space	+4 to +27 (0004 ₁₆ to 001B ₁₆)	1 to 6	Software Manual
A/D1	+28 to +31 (001C ₁₆ to 001F ₁₆)	7	A/D Converter
DMA0	+32 to +35 (0020 ₁₆ to 0023 ₁₆)	8	DMAC
DMA1	+36 to +39 (0024 ₁₆ to 0027 ₁₆)	9	
DMA2	+40 to +43 (0028 ₁₆ to 002B ₁₆)	10	
DMA3	+44 to +47 (002C ₁₆ to 002F ₁₆)	11	
Timer A0	+48 to +51 (0030 ₁₆ to 0033 ₁₆)	12	Timer A
Timer A1	+52 to +55 (0034 ₁₆ to 0037 ₁₆)	13	
Timer A2	+56 to +59 (0038 ₁₆ to 003B ₁₆)	14	
Timer A3	+60 to +63 (003C ₁₆ to 003F ₁₆)	15	
Timer A4	+64 to +67 (0040 ₁₆ to 0043 ₁₆)	16	
UART0 Transmission, NACK ⁽³⁾	+68 to +71 (0044 ₁₆ to 0047 ₁₆)	17	Serial I/O
UART0 Reception, ACK ⁽³⁾	+72 to +75 (0048 ₁₆ to 004B ₁₆)	18	
UART1 Transmission, NACK ⁽³⁾	+76 to +79 (004C ₁₆ to 004F ₁₆)	19	
UART1 Reception, ACK ⁽³⁾	+80 to +83 (0050 ₁₆ to 0053 ₁₆)	20	
Timer B0	+84 to +87 (0054 ₁₆ to 0057 ₁₆)	21	Timer B
Timer B1	+88 to +91 (0058 ₁₆ to 005B ₁₆)	22	
Timer B2	+92 to +95 (005C ₁₆ to 005F ₁₆)	23	
Timer B3	+96 to +99 (0060 ₁₆ to 0063 ₁₆)	24	
Timer B4	+100 to +103 (0064 ₁₆ to 0067 ₁₆)	25	
INT5	+104 to +107 (0068 ₁₆ to 006B ₁₆)	26	Interrupt
INT4	+108 to +111 (006C ₁₆ to 006F ₁₆)	27	
INT3	+112 to +115 (0070 ₁₆ to 0073 ₁₆)	28	
INT2	+116 to +119 (0074 ₁₆ to 0077 ₁₆)	29	
INT1	+120 to +123 (0078 ₁₆ to 007B ₁₆)	30	
INT0	+124 to +127 (007C ₁₆ to 007F ₁₆)	31	
Timer B5	+128 to +131 (0080 ₁₆ to 0083 ₁₆)	32	Timer B
UART2 Transmission, NACK ⁽³⁾	+132 to +135 (0084 ₁₆ to 0087 ₁₆)	33	Serial I/O
UART2 Reception, ACK ⁽³⁾	+136 to +139 (0088 ₁₆ to 008B ₁₆)	34	
UART3 Transmission, NACK ⁽³⁾	+140 to +143 (008C ₁₆ to 008F ₁₆)	35	
UART3 Reception, ACK ⁽³⁾	+144 to +147 (0090 ₁₆ to 0093 ₁₆)	36	
UART4 Transmission, NACK ⁽³⁾	+148 to +151 (0094 ₁₆ to 0097 ₁₆)	37	
UART4 Reception, ACK ⁽³⁾	+152 to +155 (0098 ₁₆ to 009B ₁₆)	38	

Table 10.2 Relocatable Vector Tables (Continued)

Interrupt Generated by	Vector Table Address Address(L)to Address(H) ⁽¹⁾	Software Interrupt Number	Reference	
Bus Conflict Detect, Start Condition Detect, Stop Condition Detect, (UART2) ⁽³⁾ , Fault Error ⁽⁴⁾	+156 to +159 (009C ₁₆ to 009F ₁₆)	39	Serial I/O	
Bus Conflict Detect, Start Condition Detect, Stop Condition Detect, (UART3/UART0) ⁽⁵⁾ , Fault Error ⁽⁴⁾	+160 to +163 (00A0 ₁₆ to 00A3 ₁₆)	40		
Bus Conflict Detect, Start Condition Select, Stop Condition Detect, (UART4/UART1) ⁽⁵⁾ , Fault Error ⁽⁴⁾	+164 to +167 (00A4 ₁₆ to 00A7 ₁₆)	41		
A/D0	+168 to +171 (00A8 ₁₆ to 00AB ₁₆)	42	A/D Converter	
Key Input	+172 to +175 (00AC ₁₆ to 00AF ₁₆)	43	Interrupts	
Intelligent I/O Interrupt 0	+176 to +179 (00B0 ₁₆ to 00B3 ₁₆)	44	Intelligent I/O CAN	
Intelligent I/O Interrupt 1	+180 to +183 (00B4 ₁₆ to 00B7 ₁₆)	45		
Intelligent I/O Interrupt 2	+184 to +187 (00B8 ₁₆ to 00BB ₁₆)	46		
Intelligent I/O Interrupt 3	+188 to +191 (00BC ₁₆ to 00BF ₁₆)	47		
Intelligent I/O Interrupt 4	+192 to +195 (00C0 ₁₆ to 00C3 ₁₆)	48		
Intelligent I/O Interrupt 5	+196 to +199 (00C4 ₁₆ to 00C7 ₁₆)	49		
Intelligent I/O Interrupt 6	+200 to +203(00C8 ₁₆ to 00CB ₁₆)	50		
Intelligent I/O Interrupt 7	+204 to +207(00CC ₁₆ to 00CF ₁₆)	51		
Intelligent I/O Interrupt 8	+208 to +211(00D0 ₁₆ to 00D3 ₁₆)	52		
Intelligent I/O Interrupt 9, CAN 0	+212 to +215 (00D4 ₁₆ to 00D7 ₁₆)	53		
Intelligent I/O Interrupt 10, CAN 1	+216 to +219 (00D8 ₁₆ to 00DB ₁₆)	54		
Reserved Space	+220 to +227 (00DC ₁₆ to 00E3 ₁₆)	55 to 56		—
Intelligent I/O Interrupt 11, CAN 2	+228 to +231 (00E4 ₁₆ to 00E7 ₁₆)	57		Intelligent I/O CAN
Reserved Space	+232 to +255 (00E8 ₁₆ to 00FF ₁₆)	58 to 62	—	
INT Instruction ⁽²⁾	+0 to +3 (0000 ₁₆ to 0003 ₁₆) to +252 to +255 (00FC ₁₆ to 00FF ₁₆)	0 to 63	Interrupts	

NOTES:

1. These addresses are relative to those in the INTB register.
2. The I flag does not disable interrupts.
3. In I²C mode, NACK, ACK or start/stop condition detection causes interrupts to be generated.
4. When the \overline{SS} pin is selected, fault error causes an interrupt to be generated.
5. The IFSR6 bit in the IFSR register determines whether these addresses are used for an interrupt in UART0 or in UART3.
The IFSR7 bit in the IFSR register determines whether these addresses are used for an interrupt in UART1 or in UART4.

10.6 Interrupt Request Reception

Software interrupts and special interrupts occur when conditions to generate an interrupt are met.

The peripheral function interrupts are acknowledged when all conditions below are met.

- I flag = "1"
- IR bit = "1"
- ILVL2 to ILVL0 bits > IPL

The I flag, IPL, IR bit and ILVL2 to ILVL0 bits are independent of each other. The I flag and IPL are in the FLG register. The IR bit and ILVL2 to ILVL0 bits are in the interrupt control register.

10.6.1 I Flag and IPL

The I flag enables or disables maskable interrupts. When the I flag is set to "1" (enable), all maskable interrupts are enabled; when the I flag is set to "0" (disable), they are disabled. The I flag is automatically set to "0" after reset.

IPL, consisting of three bits, indicates the interrupt priority level from level 0 to level 7.

If a requested interrupt has higher priority than that indicated by IPL, the interrupt is acknowledged.

Table 10.3 lists interrupt priority levels associated with IPL.

Table 10.3 Interrupt Priority Levels

IPL2	IPL1	IPL0	Interrupt Priority Levels
0	0	0	Level 1 and above
0	0	1	Level 2 and above
0	1	0	Level 3 and above
0	1	1	Level 4 and above
1	0	0	Level 5 and above
1	0	1	Level 6 and above
1	1	0	Level 7 and above
1	1	1	All maskable interrupts are disabled

10.6.2 Interrupt Control Register and RLVL Register

The peripheral function interrupts use interrupt control registers to control each interrupt. Figures 10.3 and 10.4 show the interrupt control register. Figure 10.5 shows the RLVL register.

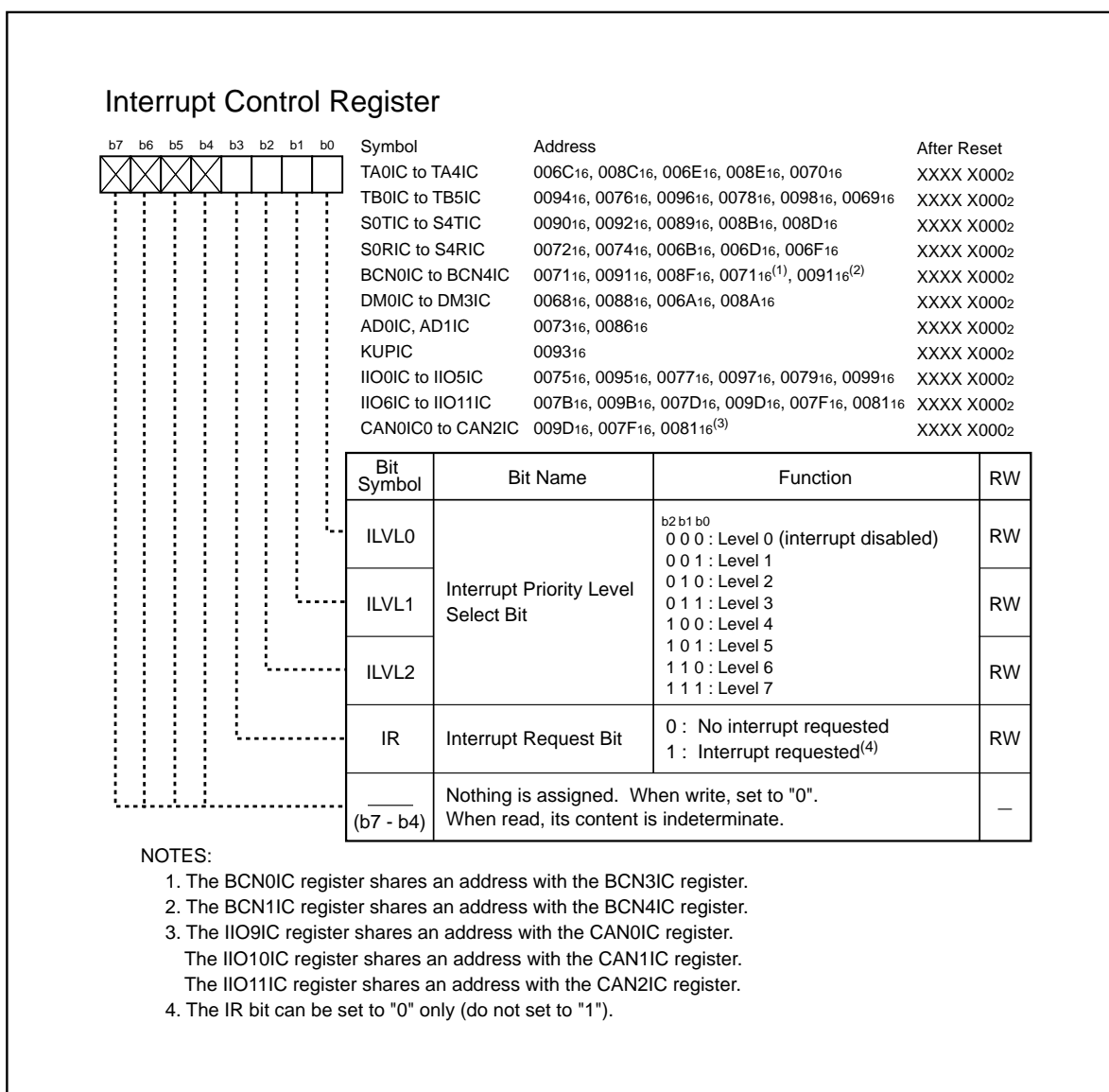


Figure 10.3 Interrupt Control Register (1)

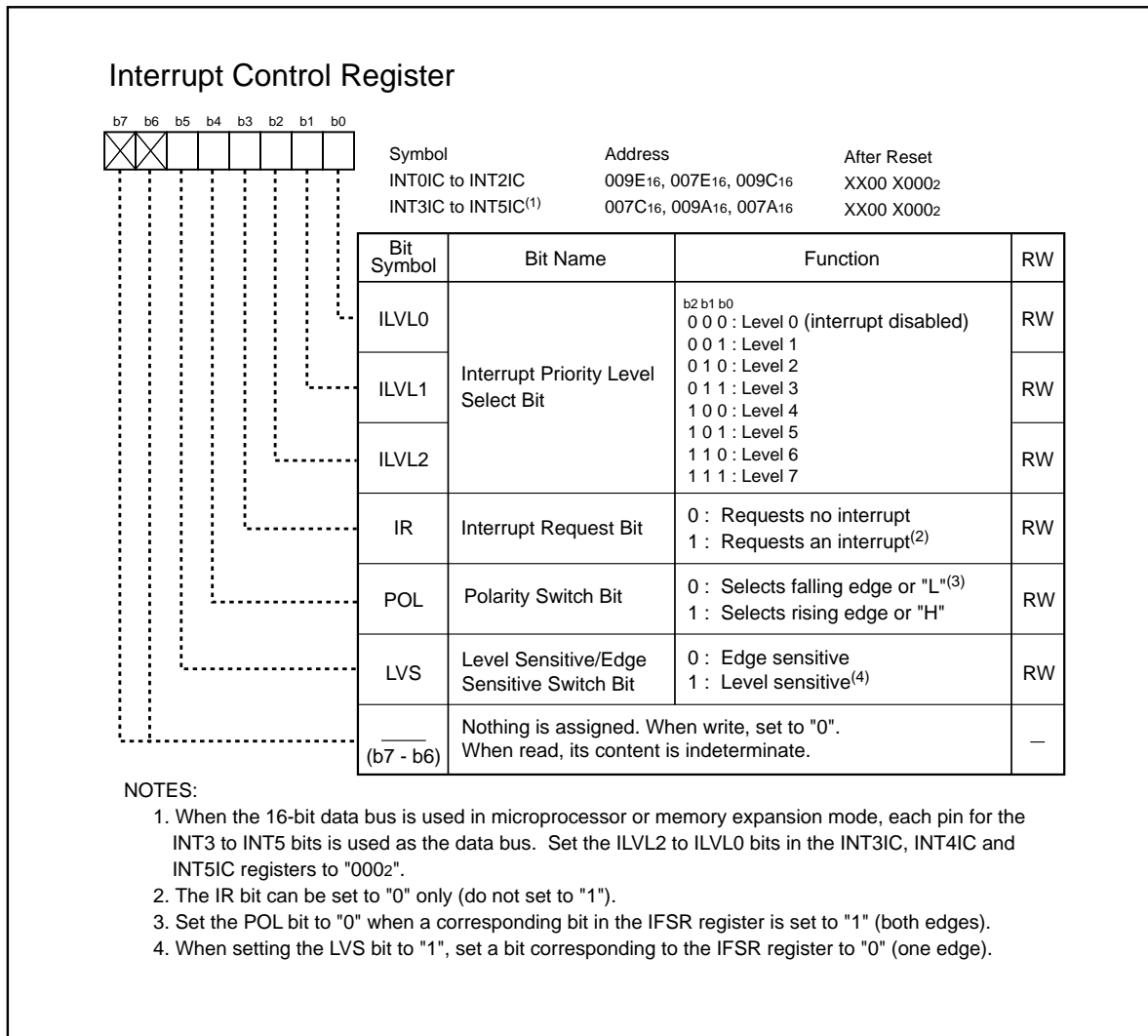


Figure 10.4 Interrupt Control Register (2)

10.6.2.1 ILVL2 to ILVL0 Bits

The ILVL2 to ILVL0 bits determines the interrupt priority level. The higher the interrupt priority level, the higher interrupt priority is.

When an interrupt request is generated, its interrupt priority level is compared to IPL. This interrupt is acknowledged only when its interrupt priority level is higher than IPL. When the ILVL2 to ILVL0 bits are set to "000₂" (level 0), this interrupt is ignored.

10.6.2.2 IR Bit

The IR bit is automatically set to "1" (interrupt requested) when an interrupt request is generated. The IR bit is automatically set to "0" (no interrupt requested) after an interrupt request is acknowledged and the program in the corresponding interrupt vector is executed.

The IR bit can be set to "0" by program. Do not set to "1".

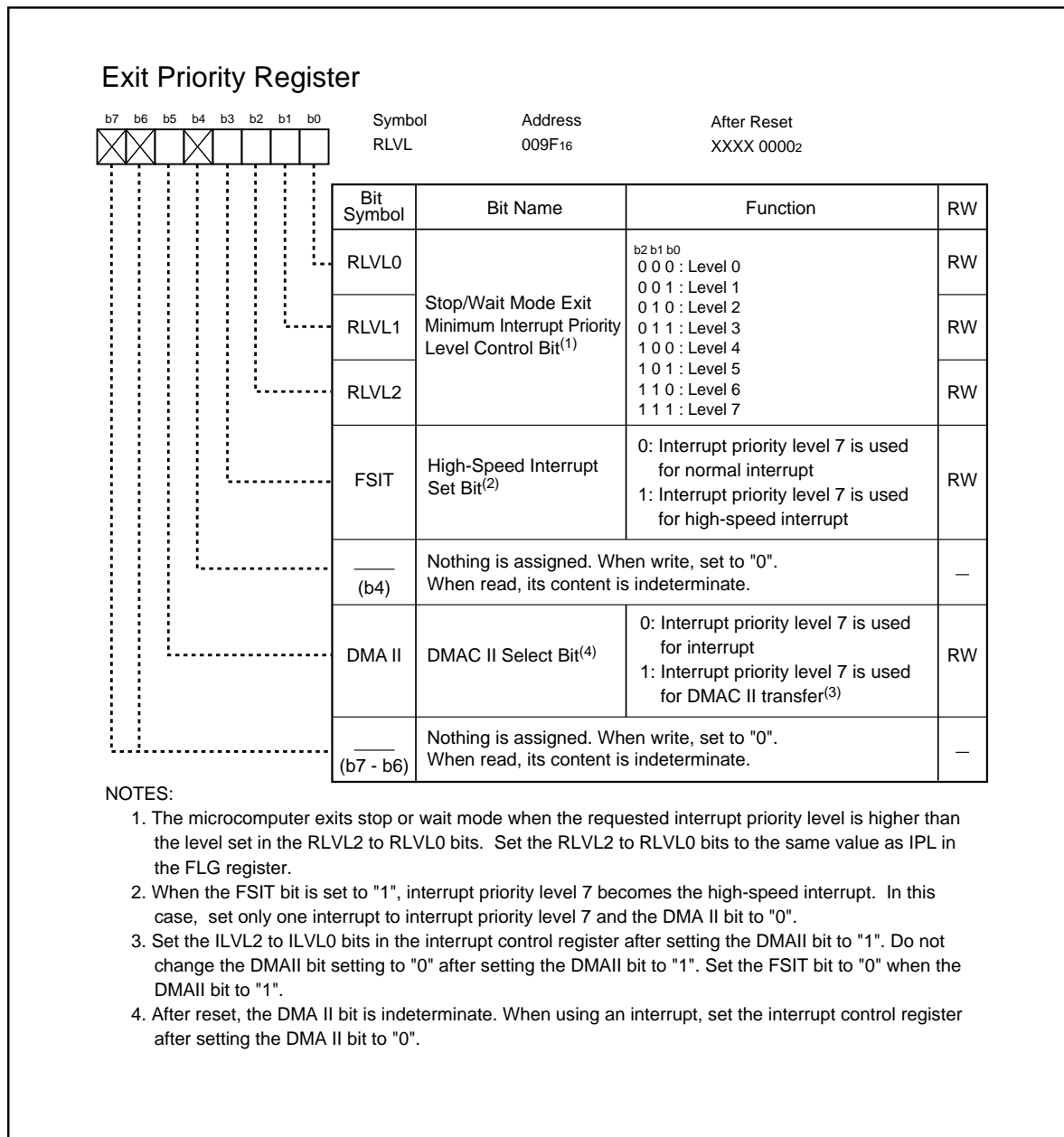


Figure 10.5 RLVL Register

10.6.2.3 RLVL2 to RLVL0 Bits

When using an interrupt to exit stop or wait mode, refer to **8.5.2 Wait Mode** and **8.5.3 Stop Mode** for details.

10.6.3 Interrupt Sequence

The interrupt sequence is performed between an interrupt request acknowledgment and interrupt routine execution.

When an interrupt request is generated while an instruction is executed, the CPU determines its interrupt priority level after the instruction is completed. The CPU starts the interrupt sequence from the following cycle. However, in regards to the SCMPU, SIN, SMOVB, SMOVF, SMOVU, SSTR, SOUT or RMPA instruction, if an interrupt request is generated while executing the instruction, the microcomputer suspends the instruction to start the interrupt sequence.

The interrupt sequence is performed as follows:

- (1) The CPU obtains interrupt information (interrupt number and interrupt request level) by reading address 000000₁₆ (address 000002₁₆ for the high-speed interrupt). Then, the IR bit applicable to the interrupt information is set to "0" (interrupt requested).
- (2) The FLG register, prior to an interrupt sequence, is saved to a temporary register⁽¹⁾ within the CPU.
- (3) Each bit in the FLG register is set as follows:
 - The I flag is set to "0" (interrupt disabled)
 - The D flag is set to "0" (single-step disabled)
 - The U flag is set to "0" (ISP selected)
- (4) A temporary register within the CPU is saved to the stack; or to the SVF register for the high-speed interrupt.
- (5) PC is saved to the stack; or to the SVP register for the high-speed interrupt.
- (6) The interrupt priority level of the acknowledged interrupt is set in IPL .
- (7) A relocatable vector corresponding to the acknowledged interrupt is stored into PC.

After the interrupt sequence is completed, an instruction is executed from the starting address of the interrupt service routine.

NOTES:

1. Temporary register cannot be modified by users.

10.6.4 Interrupt Response Time

Figure 10.6 shows an interrupt response time. Interrupt response time is the period between an interrupt generation and the execution of the first instruction in an interrupt service routine. An interrupt response time includes the period between an interrupt request generation and the completed execution of an instruction ((a) in Figure 10.6) and the period required to perform an interrupt sequence ((b) in Figure 10.6).

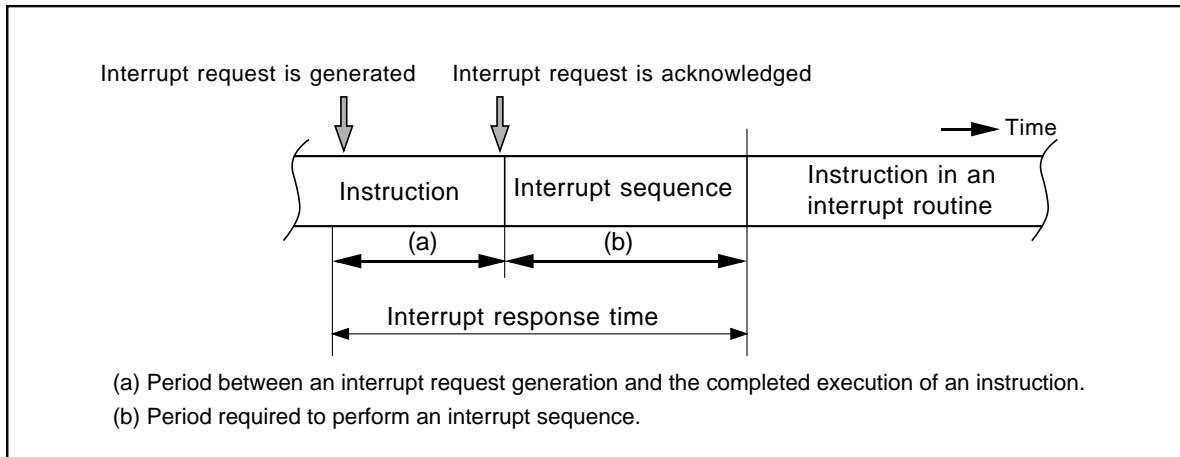


Figure 10.6 Interrupt Response Time

Time (a) varies depending on the instruction being executed. The DIV instruction requires the longest time (a); 40 cycles when an immediate value or register is set as the divisor .

When the divisor is a value in the memory, the following value is added.

- Normal addressing : $2 + X$
- Index addressing : $3 + X$
- Indirect addressing : $5 + X + 2Y$
- Indirect index addressing : $6 + X + 2Y$

X is the number of wait states for a divisor space. Y is the number of wait states for the space that stores indirect addresses. If X and Y are in an odd address or in 8-bit bus space, the X and Y value must be doubled.

Table 10.4 lists time (b).

Table 10.4 Interrupt Sequence Execution Time

Interrupt	Interrupt Vector Address	16-Bit Bus	8-Bit Bus
Peripheral Function	Even address	14 cycles	16 cycles
	Odd address ⁽¹⁾	16 cycles	16 cycles
INT Instruction	Even address	12 cycles	14 cycles
	Odd address ⁽¹⁾	14 cycles	14 cycles
$\overline{\text{NMI}}$ Watchdog Timer Undefined Instruction Address Match	Even address ⁽²⁾	13 cycles	15 cycles
Overflow	Even address ⁽²⁾	14 cycles	16 cycles
BRK Instruction (relocatable vector table)	Even address	17 cycles	19 cycles
	Odd address ⁽¹⁾	19 cycles	19 cycles
BRK Instruction (fixed vector table)	Even address ⁽²⁾	19 cycles	21 cycles
High-Speed Interrupt	Vector table is internal register	5 cycles	

NOTES:

1. Allocate interrupt vectors to even addresses.
2. Vectors are fixed to even addresses.

10.6.5 IPL Change when Interrupt Request is Acknowledged

When a peripheral function interrupt request is acknowledged, IPL sets the priority level for the acknowledged interrupt.

Software interrupts and special interrupts have no interrupt priority level. If an interrupt request that has no interrupt priority level is acknowledged, the value shown in Table 10.5 is set in IPL as the interrupt priority level.

Table 10.5 Interrupts without Interrupt Priority Levels and IPL

Interrupt Sources	Level that is Set to IPL
Watchdog Timer, $\overline{\text{NMI}}$, Oscillation Stop Detect	7
Reset	0
Software, Address Match	Not changed

10.6.6 Saving a Register

In the interrupt sequence, the FLG register and PC are saved to the stack.

After the FLG register is saved to the stack, 16 high-order bits and 16 low-order bits of PC, extended to 32 bits, are saved to the stack. Figure 10.7 shows the stack state before and after an interrupt request is acknowledged.

Other important registers are saved by program at the beginning of an interrupt service routine. The PUSHM instruction can save all registers except SP.

Refer to **10.4 High-Speed Interrupt** for the high-speed interrupt.

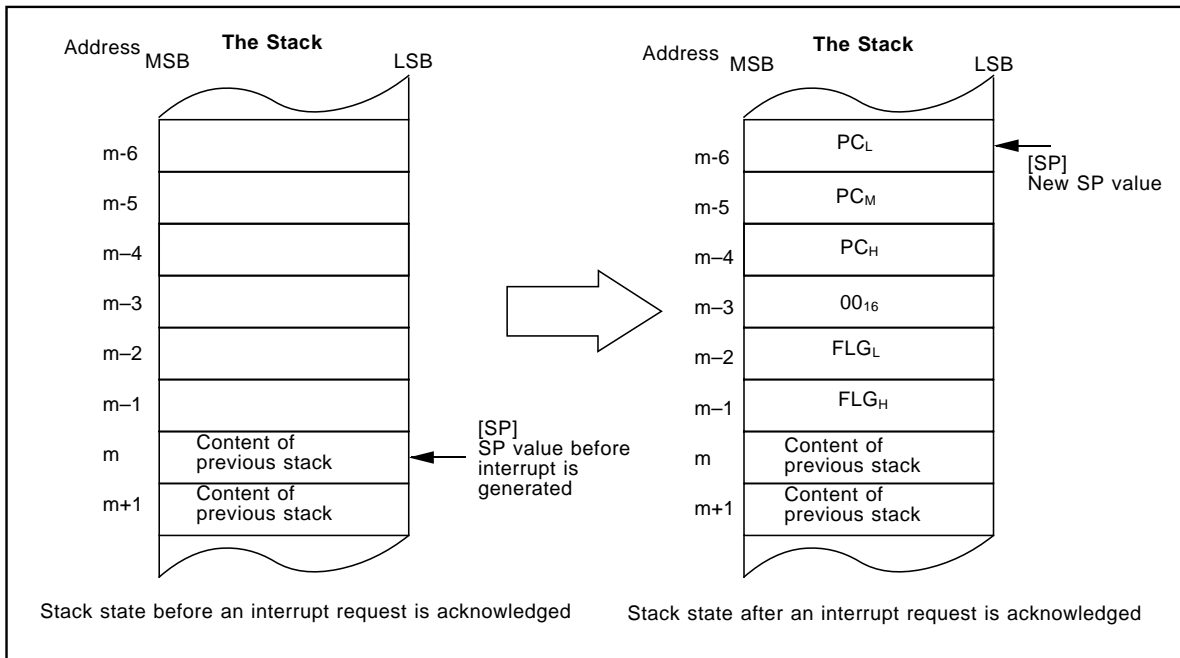


Figure 10.7 Stack States

10.6.7 Restoration from Interrupt Routine

When the REIT instruction is executed at the end of an interrupt service routine, the FLG register and PC, which have been saved to the stack, are automatically restored. The program, executed before an interrupt request has been acknowledged, starts running again. Refer to **10.4 High-Speed Interrupt** for the high-speed interrupt.

Restore registers saved by program in an interrupt service routine by the POPM instruction or others before the REIT and FREIT instructions. Register bank is switched back to the bank used prior to the interrupt sequence by the REIT or FREIT instruction.

10.6.8 Interrupt Priority

If two or more interrupt requests are sampled at the same sampling points (a timing to detect whether an interrupt request is generated or not), the interrupt with the highest priority is acknowledged.

Set the ILVL2 to ILVL0 bits to select the desired priority level for maskable interrupts (peripheral function interrupt).

Priority levels of special interrupts such as reset (reset has the highest priority) and watchdog timer are set by hardware. Figure 10.8 shows priority levels of hardware interrupts.

The interrupt priority does not affect software interrupts. The microcomputer jumps to the interrupt routine when the instruction is executed.

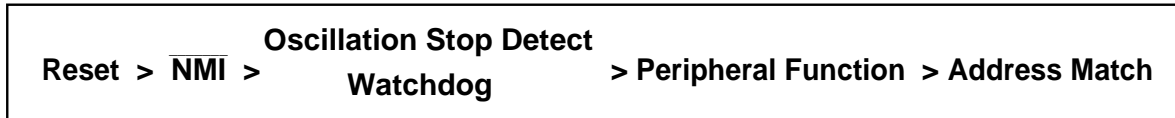


Figure 10.8 Interrupt Priority

10.6.9 Interrupt Priority Level Select Circuit

The interrupt priority level select circuit selects the highest priority interrupt when two or more interrupt requests are sampled at the same sampling point.

Figure 10.9 shows the interrupt priority level select circuit.

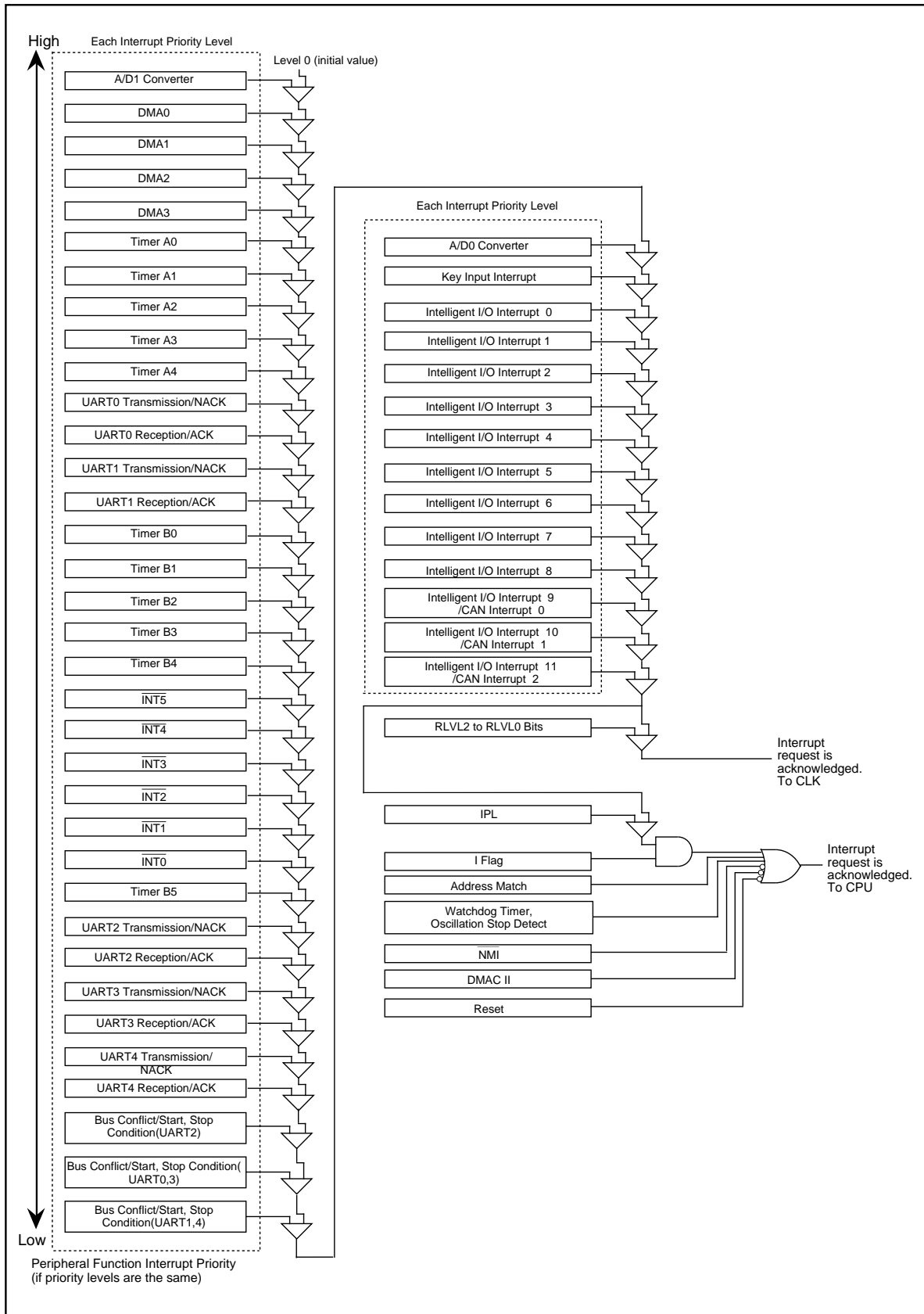


Figure 10.9 Interrupt Priority Level Select Circuit

10.7 $\overline{\text{INT}}$ Interrupt

External input generates the $\overline{\text{INT}}_i$ interrupt ($i = 0$ to 5). The LVS bit in the INTiIC register selects either edge sensitive triggering to generate an interrupt on any edge or level sensitive triggering to generate an interrupt at an applied signal level. The POL bit in the INTiIC register determines the polarity.

With an edge sensitive triggering, when the IFSR_i bit in the IFSR register is set to "1" (both edges), an interrupt occurs on both rising and falling edges of the external input. If the IFSR_i bit is set to "1", set the POL bit in the corresponding register to "0" (falling edge).

With a level sensitive triggering, set the IFSR_i bit to "0" (single edge). When the $\overline{\text{INT}}_i$ pin input level reaches the level set in the POL bit, the IR bit in the INTiIC register is set to "1". The IR bit remains set to "1" even if the $\overline{\text{INT}}_i$ pin level is changed. The IR bit is set to "0" when the $\overline{\text{INT}}_i$ interrupt is acknowledged or when "0" is written by program.

Figure 10.10 shows the IFSR register.

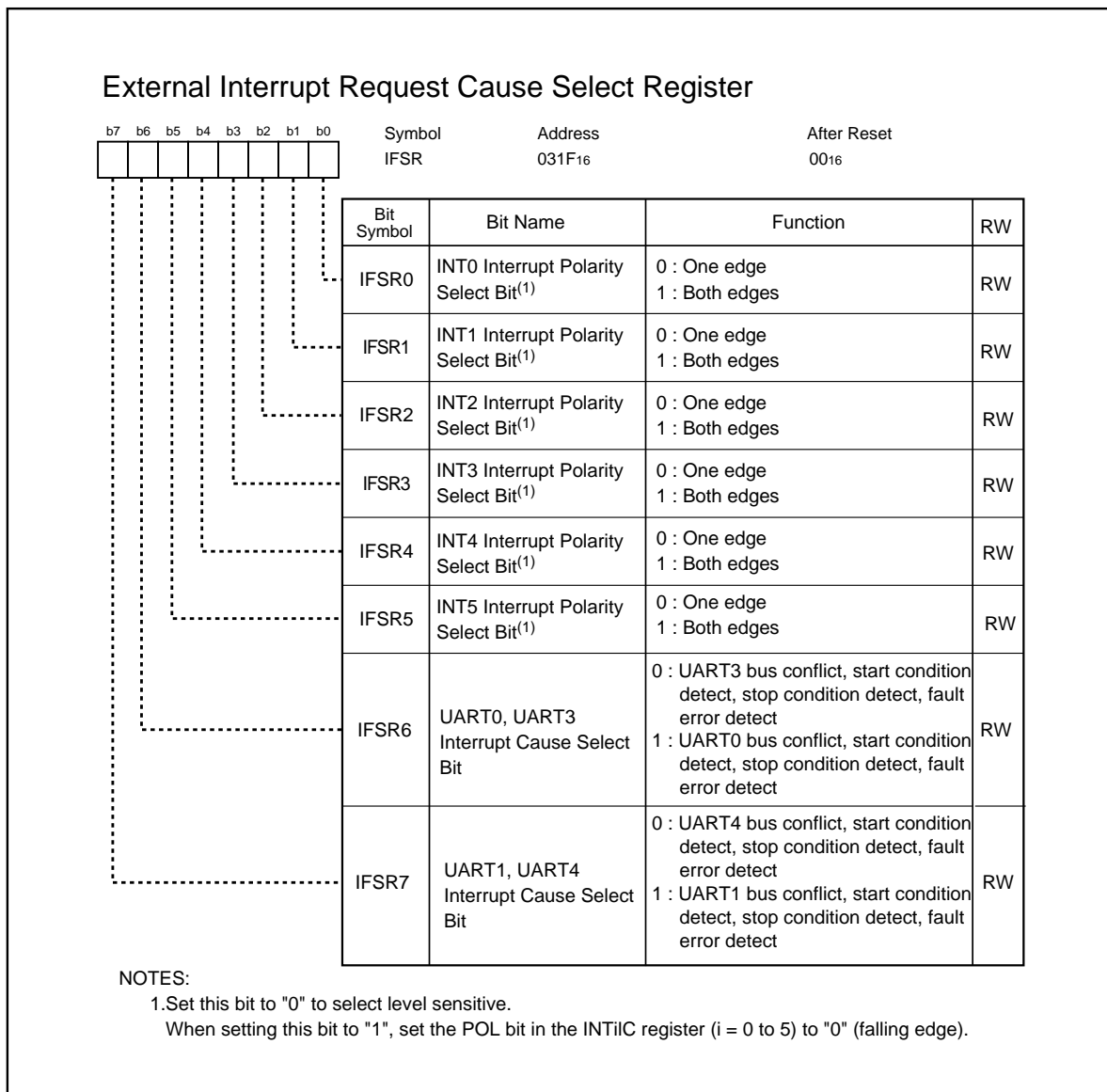


Figure 10.10 IFSR Register

10.8 $\overline{\text{NMI}}$ Interrupt

The $\overline{\text{NMI}}$ interrupt occurs when the signal applied to the P85/ $\overline{\text{NMI}}$ pin changes from an "H" signal to an "L" signal. The $\overline{\text{NMI}}$ interrupt is a non-maskable interrupt. Although the P85/ $\overline{\text{NMI}}$ pin is used as the $\overline{\text{NMI}}$ interrupt input pin, the P8_5 bit in the P85 register indicates input level for this pin.

NOTES:

When the $\overline{\text{NMI}}$ interrupt is not used, connect (pull-up) the $\overline{\text{NMI}}$ pin to Vcc via a resistor. Because the $\overline{\text{NMI}}$ interrupt cannot be ignored, the pin must be connected.

10.9 Key Input Interrupt

Key input interrupt request is generated when one of the signals applied to the P104 to P107 pins in input mode is on the falling edge. The key input interrupt can be also used as key-on wake-up function to exit wait or stop mode. To use the key input interrupt, do not use P104 to P107 as A/D input ports. Figure 10.11 shows a block diagram of the key input interrupt. When an "L" signal is applied to any pins in input mode, signals applied to other pins are not detected as a request signal for an interrupt.

When the PSC_7 bit in the PSC register⁽¹⁾ is set to "1" (key input interrupt disabled), no key input interrupt occurs regardless of interrupt control register settings. When the PSC_7 bit is set to "0", no input from a port pin is available even when in input mode.

NOTES:

1. Refer to **24. Programmable I/O Ports** for details on the PSC register.

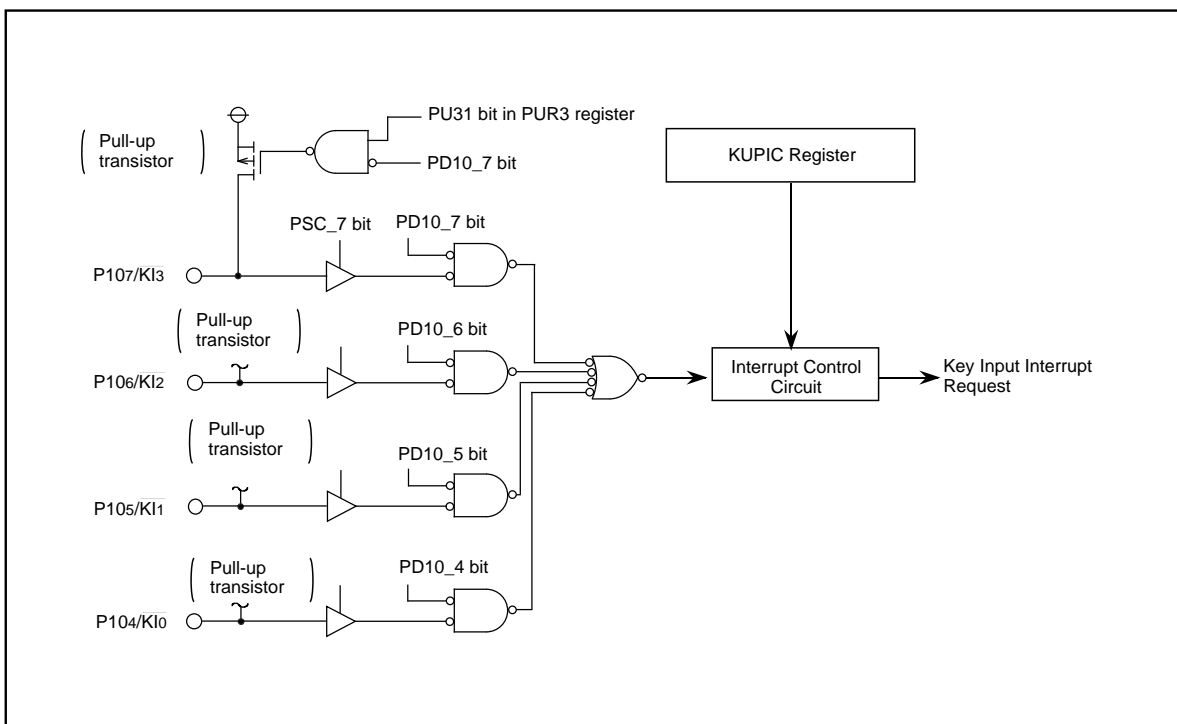


Figure 10.11 Key Input Interrupt

10.10 Address Match Interrupt

The address match interrupt occurs immediately before executing an instruction that is stored into an address indicated by the RMAD_i register (i=0 to 3). The address match interrupt can be set in four addresses. The AIER_i bit in the AIER register determines whether the interrupt is enabled or disabled. The I flag and IPL do not affect the address match interrupt.

Figure 10.12 shows registers associated with the address match interrupt.

Set the starting address of an instruction in the RMAD_i register. The address match interrupt does not occur when a table data or addresses other than the starting address of the instruction is set.

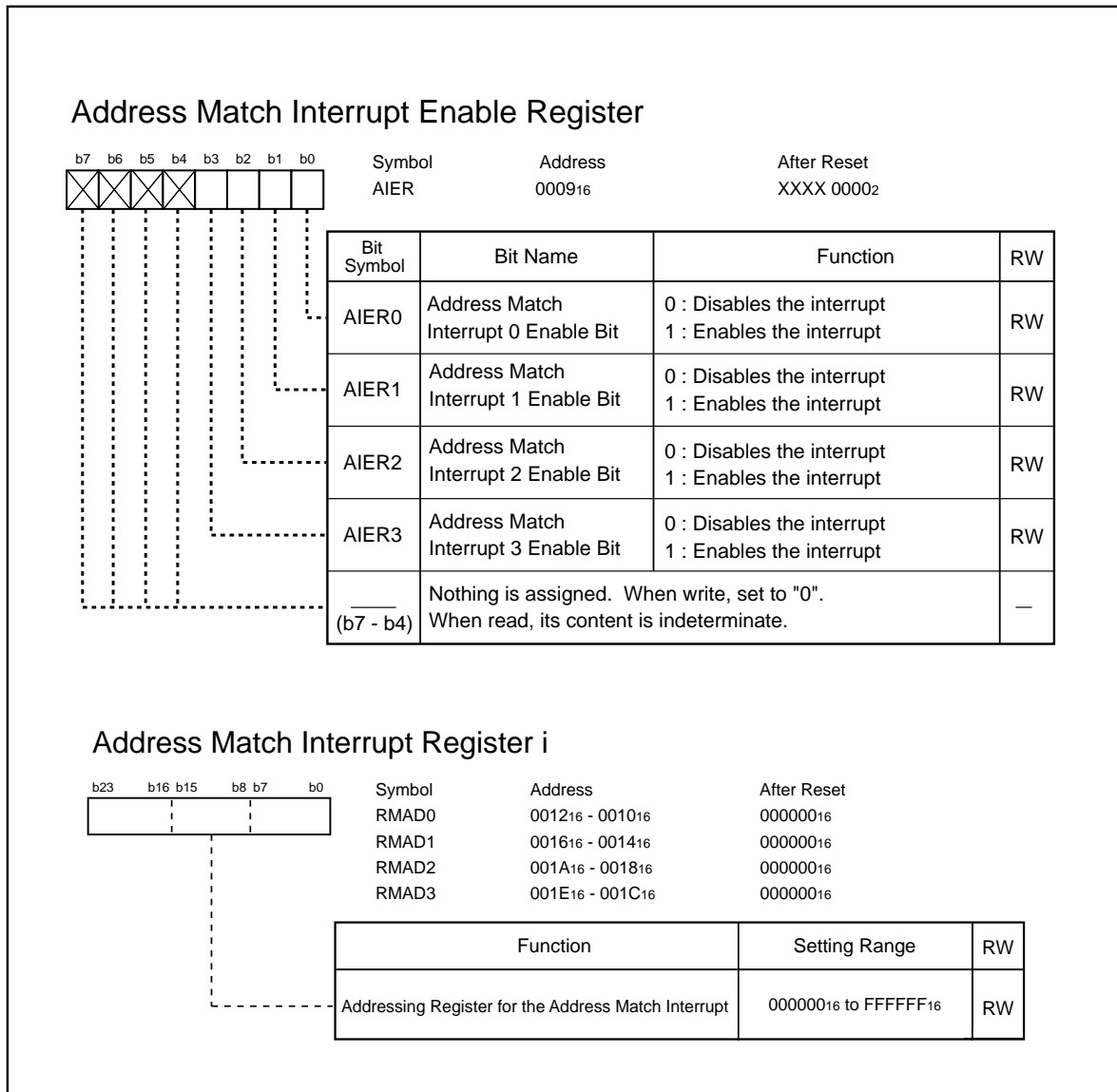


Figure 10.12 AIER Register and RMAD0 to RMAD3 Registers

10.11 Intelligent I/O Interrupt and CAN Interrupt

The intelligent I/O interrupt and CAN interrupt are assigned to software interrupt numbers 44 to 54, and 57. Figure 10.13 shows a block diagram of the intelligent I/O interrupt and CAN interrupt. Figure 10.14 shows the IIOiIR register (i = 0 to 11). Figure 10.15 shows the IIOiIE register.

When using the intelligent I/O interrupt or CAN interrupt, set the IRLT bit in the IIOiIE register to "1" (interrupt request for interrupt used).

Various interrupt requests cause the intelligent I/O interrupt to occur. When an interrupt request is generated with intelligent I/O or CAN functions, the corresponding bit in the IIOiIR register is set to "1" (interrupt requested). When the corresponding bit in the IIOiIE register is set to "1" (interrupt enabled), the IR bit in the corresponding IIOiIC register is set to "1" (interrupt requested).

After the IR bit setting changes from "0" to "1", the IR bit remains set to "1" when a bit in the IIOiIR register is set to "1" by another interrupt request and the corresponding bit in the IIOiIE register is set to "1".

Bits in the IIOiIR register are not set to "0" automatically, even if an interrupt is acknowledged. Set each bit to "0" by program. If these bits remain set to "1", all generated interrupt requests are ignored.

CAN interrupt uses bit 7 in the IIO9IR to IIO11IR registers and bit 7 in the IIO9IE to IIO11IE registers. IIO9IR to IIO11IR registers share addresses with the CAN0IC to CAN2IC registers. Refer to **22.3 CAN Interrupt** for details.

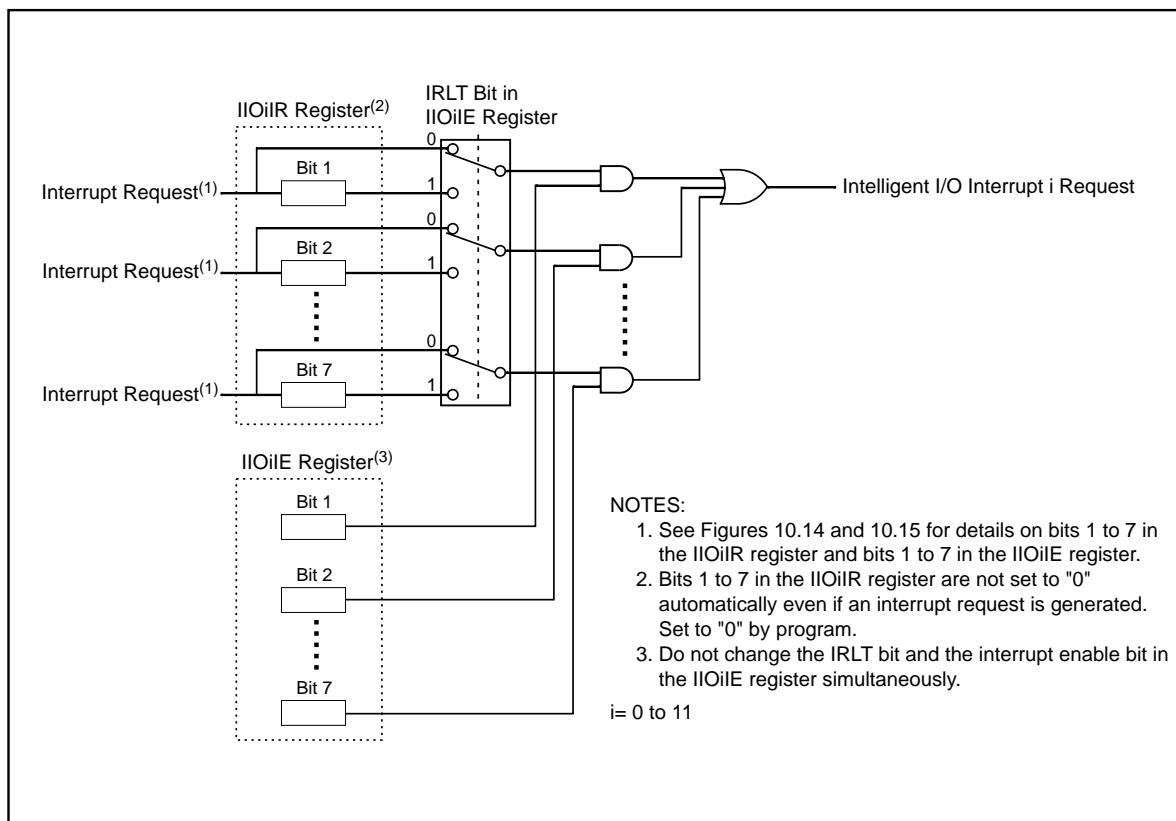


Figure 10.13 Intelligent I/O Interrupt and CAN Interrupt

When using the intelligent I/O interrupt or CAN interrupt to activate DMAC II, set the IRLT bit in the IIOiIE register to "0" (an interrupt used for DMAC, DMAC II) to enable the interrupt request that the IIOiIE register requires.

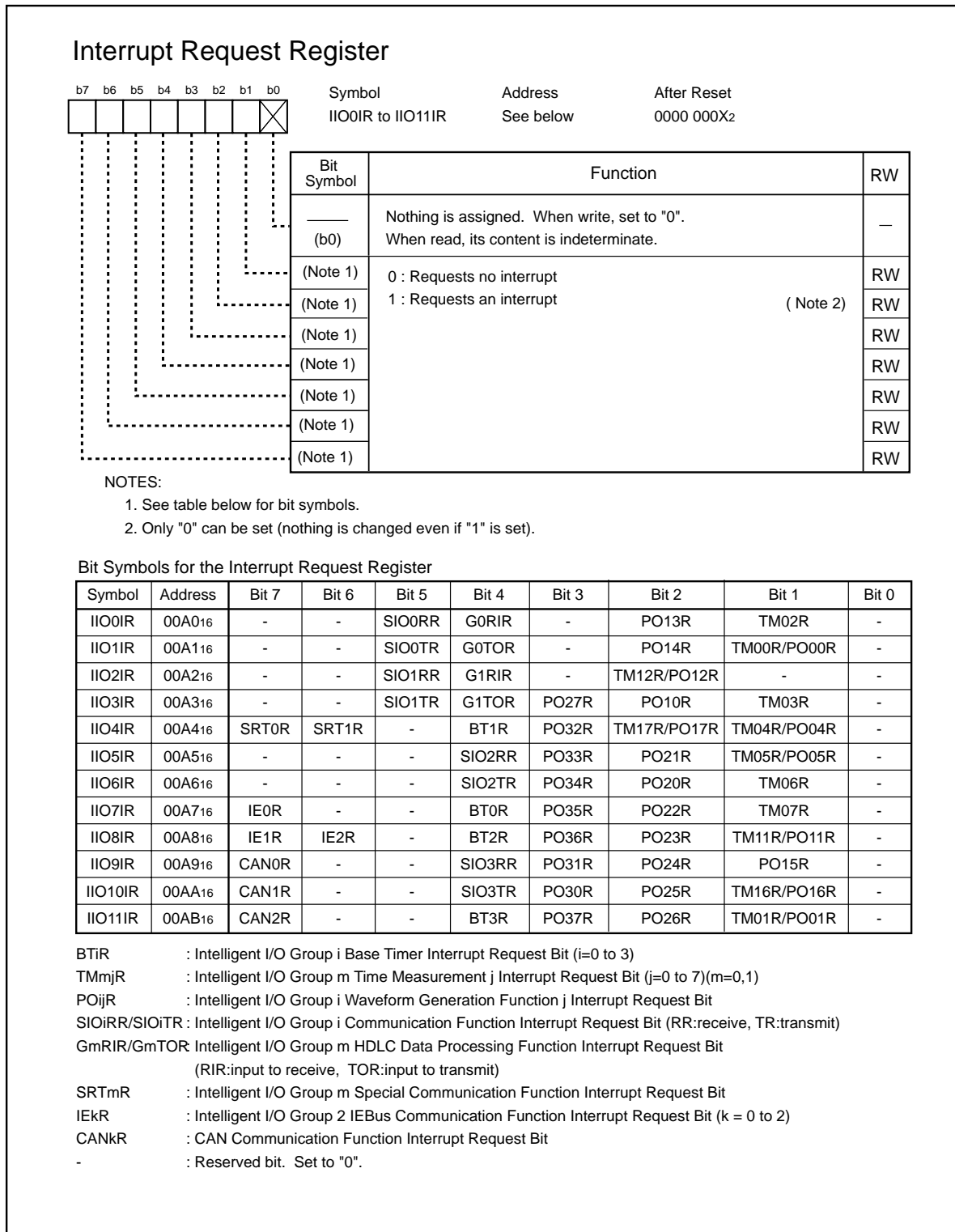


Figure 10.14 IIO0IR to IIO11IR Registers

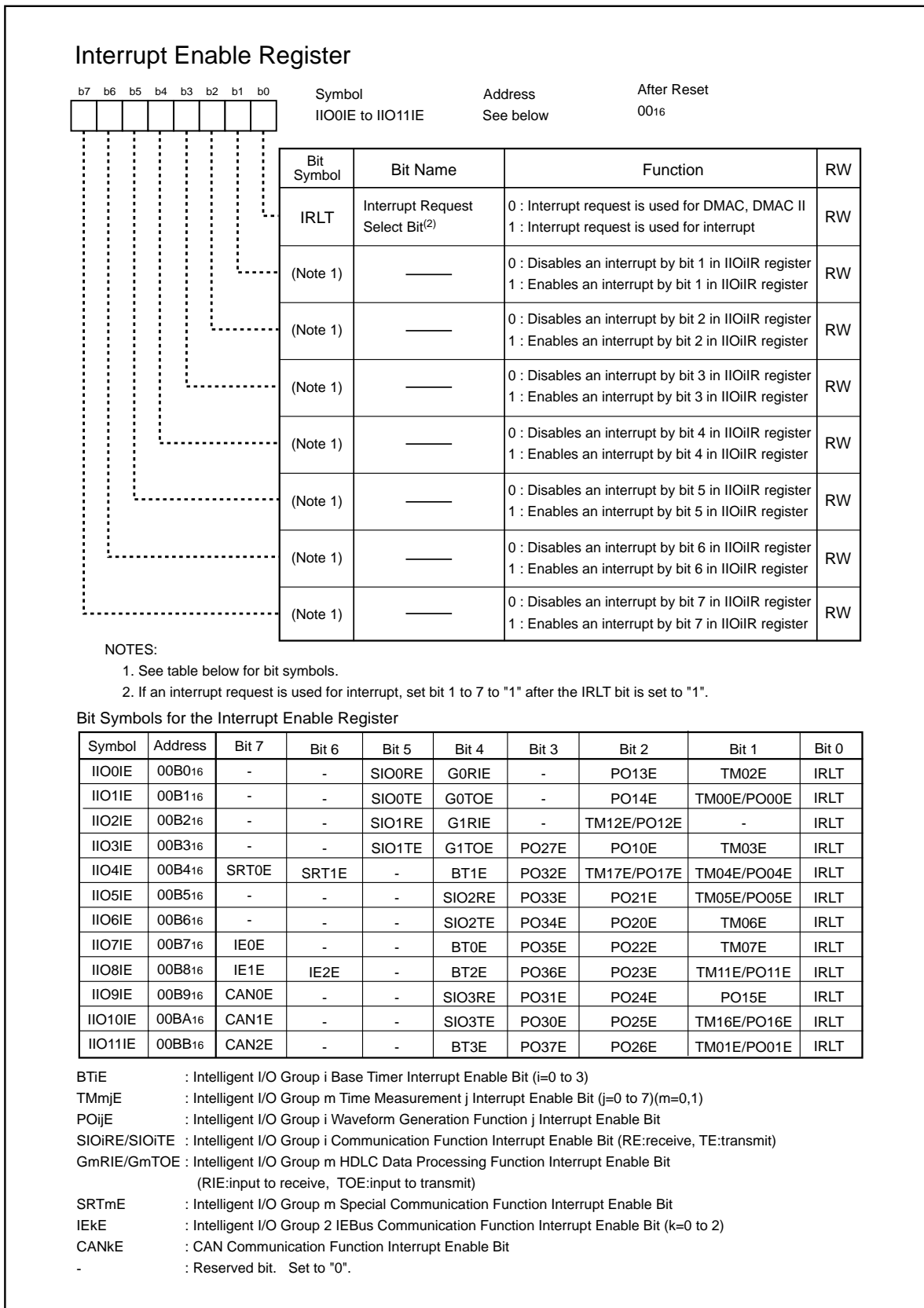


Figure 10.15 IIO0iE to IIO11iE Registers

11. Watchdog Timer

The watchdog timer detects a program which is out of control. The watchdog timer contains a 15-bit counter which is decremented by the CPU clock that the prescaler divides. The CM06 bit in the CM0 register determines whether the watchdog timer interrupt request or reset is generated when the watchdog timer underflows. The CM06 bit can be set to "1" (reset) only. Once the CM06 bit is set to "1", it cannot be changed to "0" (watchdog timer interrupt) by program. The CM06 bit is set to "0" only after reset.

When the main clock, on-chip oscillator clock, or the PLL clock runs as the CPU clock, the WDC7 bit in the WDC register determines whether the prescaler divides by 16 or by 128. When the sub clock runs as the CPU clock, the prescaler divides by 2 regardless of the WDC7 bit setting. Watchdog timer cycle is calculated as follows. Marginal errors, due to the prescaler, may occur in watchdog timer cycle.

When the main clock, on-chip oscillator clock, or PLL clock is selected as the CPU clock:

$$\text{Watchdog timer cycle} = \frac{\text{Divide by 16 or 128 prescaler} \times \text{counter value of watchdog timer (32768)}}{\text{CPU clock}}$$

When the sub clock is selected as the CPU clock,

$$\text{Watchdog timer cycle} = \frac{\text{Divided by 2 prescaler} \times \text{counter value of watchdog timer (32768)}}{\text{CPU clock}}$$

For example, if the CPU clock frequency is 30MHz and the prescaler divides by 16, watchdog timer cycle is approximately 17.5 ms.

The watchdog timer is reset when the WDTS register is set and when a watchdog timer interrupt request is generated. The prescaler is reset only when the microcomputer is reset. Both watchdog timer and prescaler stop after reset. They begin counting when the WDTS register is set.

Write the WDTS register with shorter cycle than the watchdog timer cycle. Set the WDTS register also in the beginning of the watchdog timer interrupt routine.

The watchdog timer and prescaler stop in stop mode, wait mode and hold state. They resume counting from the value held when the mode or state is exited.

Figure 11.1 shows a block diagram of the watchdog timer. Figure 11.2 shows registers associated with the watchdog timer.

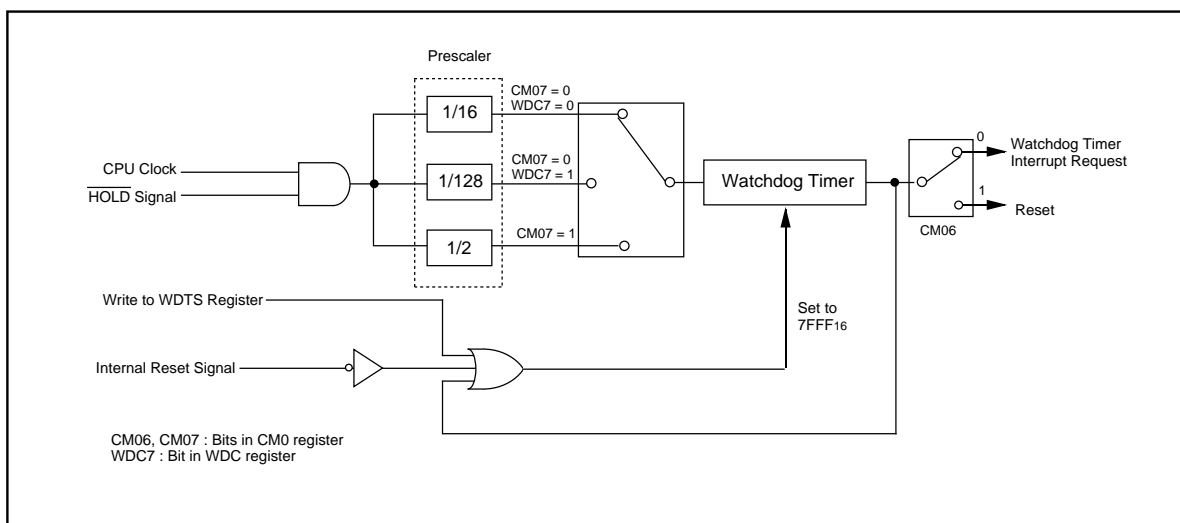


Figure 11.1 Watchdog Timer Block Diagram

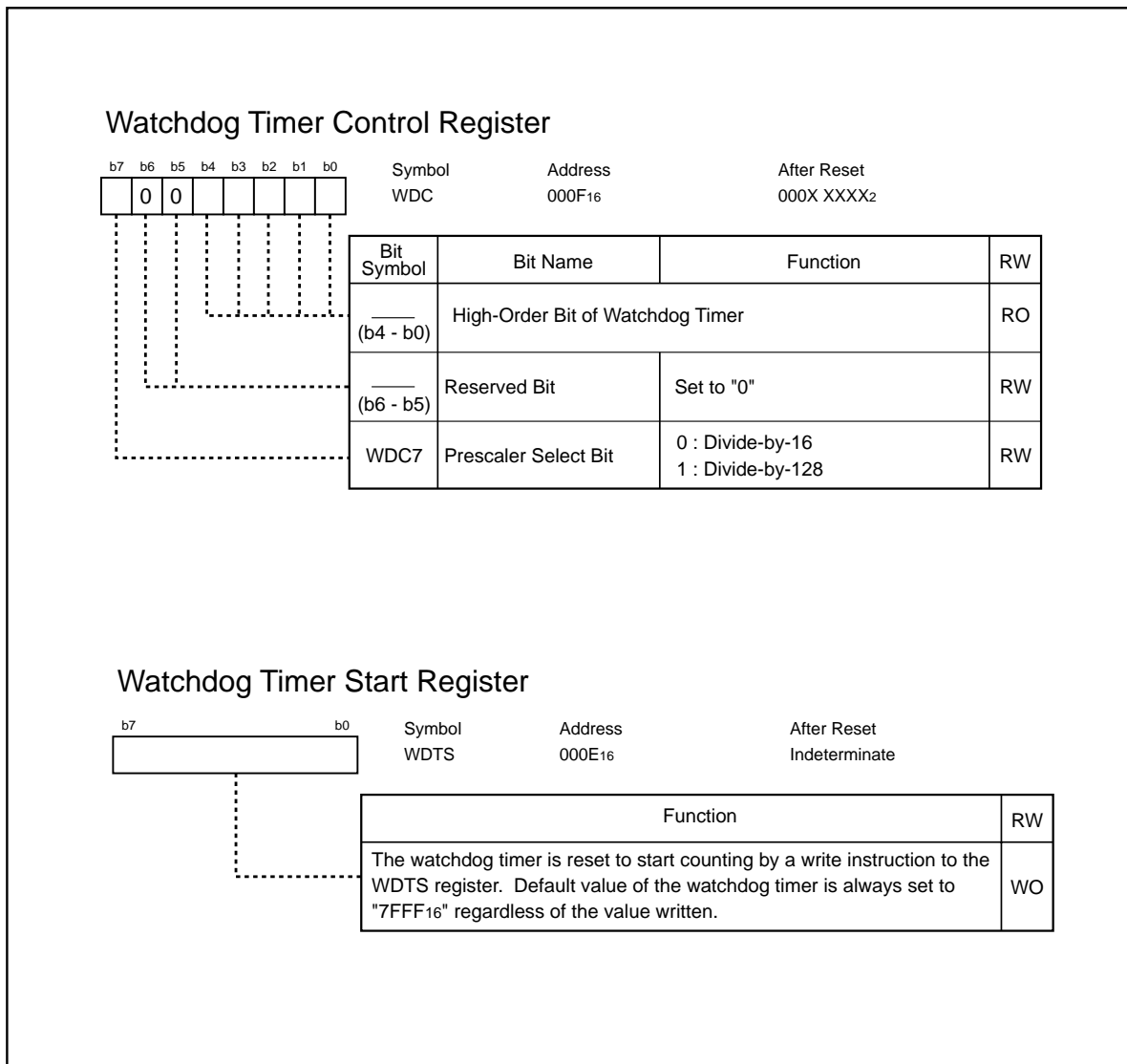


Figure 11.2 WDC Register and WDS Register

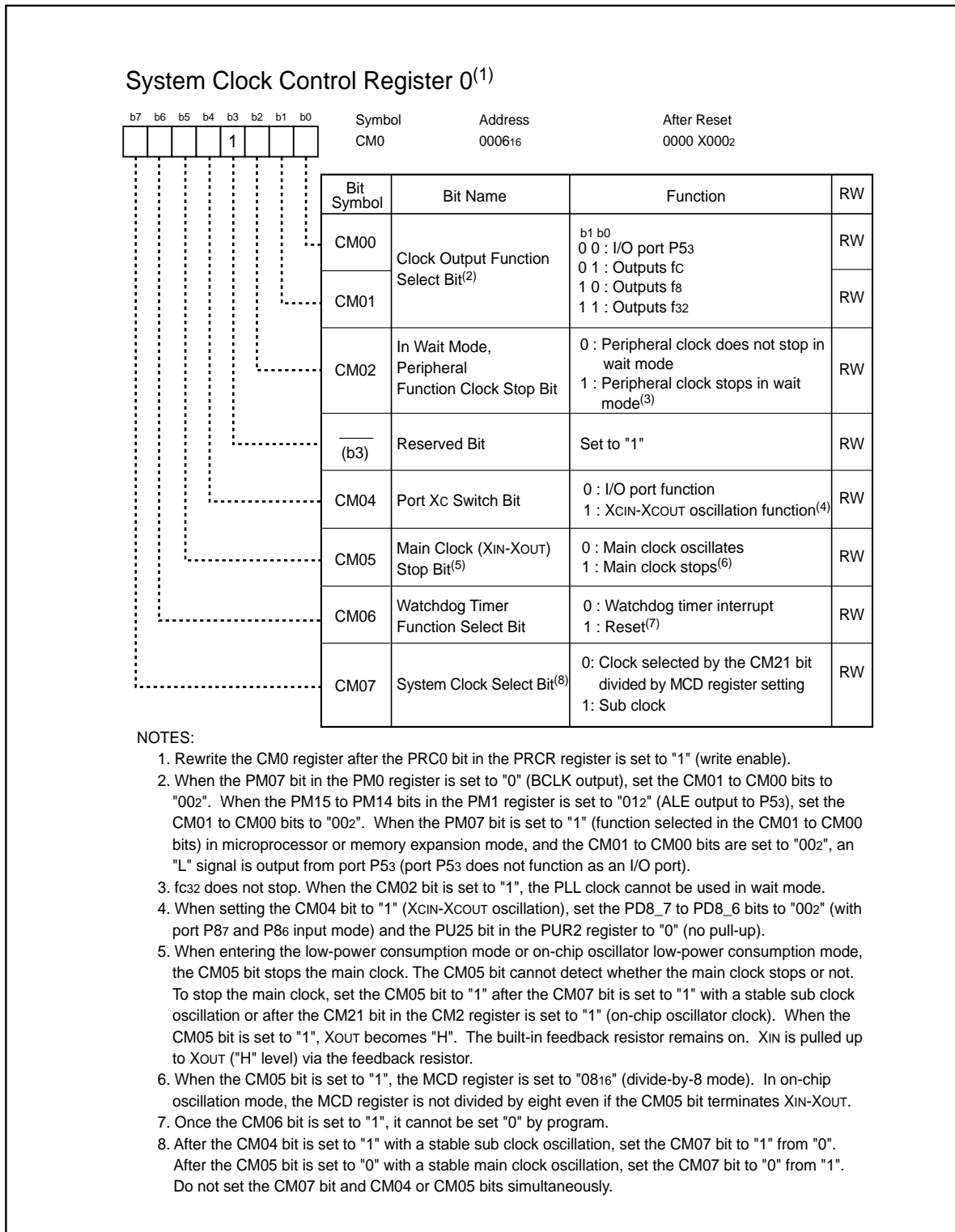


Figure 11.3 CM0 Register

12. DMAC

This microcomputer contains four DMAC (direct memory access controller) channels that allow data to be sent to memory without using the CPU. DMAC transmits a 8- or 16-bit data from a source address to a destination address whenever a transmit request occurs. DMA0 and DMA1 must be prioritized when using DMAC. DMAC2 and DMAC3 share registers required for high-speed interrupts. High-speed interrupts cannot be used when using three or more DMAC channels.

The CPU and DMAC use the same data bus, but DMAC has a higher bus access privilege than the CPU. The cycle-steal method employed by DMAC enables high-speed operation between a transfer request and the complete transmission of 16-bit (word) or 8-bit (byte) data. Figure 12.1 shows a mapping of registers to be used for DMAC. Table 12.1 lists specifications of DMAC. Figures 12.2 to 12.5 show registers associated with DMAC.

Because the registers shown in Figure 12.1 are allocated to the CPU, use the LDC instruction to write to the registers. To set DCT2, DCT3, DRC2, DRC3, DMA2 and DMA3 registers, set the B flag to "1" (register bank 1) and set R0 to R3, A0, A1 registers with the MOV instruction.

To set DSA2 and DSA3 registers, set the B flag to "1" and set the SB, FB, SVP, VCT registers with the LDC instruction. To set the DRA2 and DRA3 registers, set the SVP, VCT registers with the LDC instruction.

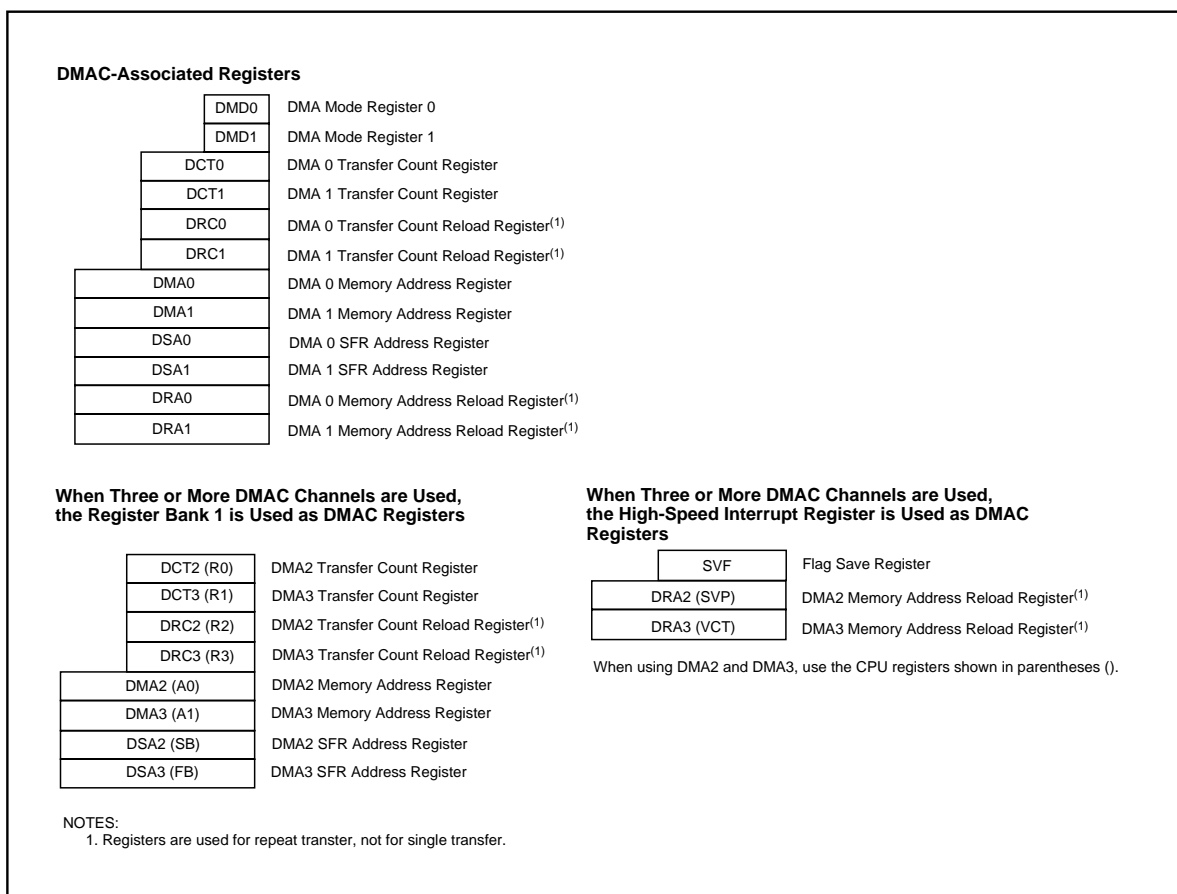


Figure 12.1 Register Mapping for DMAC

DMAC starts a data transfer by setting the DSR bit in the DMiSL register (i=0 to 3) or by using an interrupt request, generated by the functions determined by the DSEL 4 to DSEL0 bits in the DMiSL register, as a DMA request. Unlike interrupt requests, the I flag and interrupt control register do not affect DMA. Therefore, a DMA request can be acknowledged even if an interrupt is disabled and cannot be acknowledged. In addition, the IR bit in the interrupt control register does not change when a DMA request is acknowledged.

Table 12.1 DMAC Specifications

Item		Specification
Channels		4 channels (cycle-steal method)
Transfer Memory Space		<ul style="list-style-type: none"> From a desired address in a 16M-byte space to a fixed address in a 16M-byte space From a fixed address in a 16M-byte space to a desired address in a 16M-byte space
Maximum Bytes Transferred		128K bytes (when a 16-bit data is transferred) or 64K bytes (when an 8-bit data is transferred)
DMA Request Factors ⁽¹⁾		Falling edge or both edges of input signals to the INT0 to INT3 pins Timer A0 to timer A4 interrupt requests Timer B0 to timer B5 interrupt requests UART0 to UART4 transmit and receive interrupt requests A/D conversion interrupt request Intelligent I/O interrupt request CAN interrupt request Software trigger
Channel Priority		DMA0 > DMA1 > DMA2 > DMA3 (DMA0 has highest priority)
Transfer Unit		8 bits, 16 bits
Destination Address		Forward/fixed (forward and fixed directions cannot be specified when specifying source and destination addresses simultaneously)
Transfer Mode	Single Transfer	Transfer is completed when the DCTi register (i = 0 to 3) is set to "0000 ₁₆ "
	Repeat Transfer	When the DCTi register is set to "0000 ₁₆ ", the value of the DRCi register is reloaded into the DCTi register and the DMA transfer is continued
DMA Interrupt Request Generation Timing		When the DCTi register changes "0001 ₁₆ " to "0000 ₁₆ "
DMA Startup	Single Transfer	DMA starts when a DMA request is generated after the DCTi register is set to "0001 ₁₆ " or more and the MDi1 to MD0 bits in the DMDj register (j = 0 to 1) are set to "012" (single transfer)
	Repeat Transfer	DMA starts when a DMA request is generated after the DCTi register is set to "0001 ₁₆ " or more and the MDi1 to MDi0 bits are set to "112" (repeat transfer)
DMA Stop	Single Transfer	DMA stops when the MDi1 to MDi0 bits are set to "002" (DMA disabled) or when the DCTi register is set to "0000 ₁₆ " (0 DMA transfer) by DMA transfer or write
	Repeat Transfer	DMA stops when the MDi1 to MDi0 bits are set to "002" or when the DCTi register is set to "0000 ₁₆ " and the DRCi register set to "0000 ₁₆ "
Reload Timing to the DCTi or DMAi Register		When the DCTi register is set to "0000 ₁₆ " from "0001 ₁₆ " in repeat transfer mode
DMA Transfer Cycles		Minimum 3 cycles between SFR and internal RAM

NOTES:

1. The IR bit in the interrupt control register does not change when a DMA request is acknowledged.

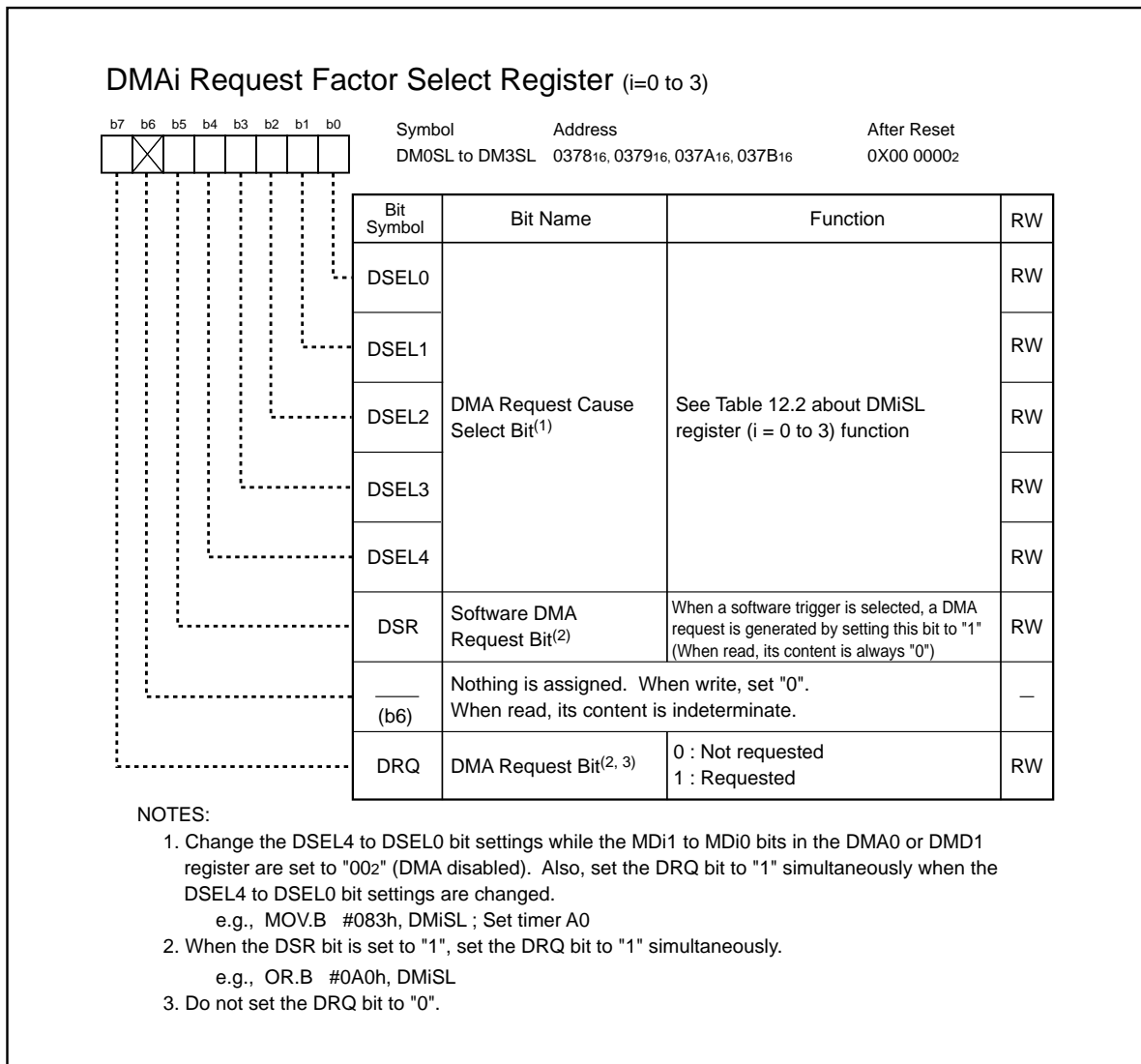


Figure 12.2 DM0SL to DM3SL Registers

Table 12.2 DMiSL Register (i = 0 to 3) Function

Setting Value	DMA Request Cause			
b4 b3 b2 b1 b0	DMA0	DMA1	DMA2	DMA3
0 0 0 0 0	Software Trigger			
0 0 0 0 1	Falling edge of INT0	Falling edge of INT1	Falling edge of INT2	Falling edge of INT3 ⁽¹⁾
0 0 0 1 0	Both edges of INT0	Both edges of INT1	Both edges of INT2	Both edges of INT3 ⁽¹⁾
0 0 0 1 1	Timer A0 Interrupt Request			
0 0 1 0 0	Timer A1 Interrupt Request			
0 0 1 0 1	Timer A2 Interrupt Request			
0 0 1 1 0	Timer A3 Interrupt Request			
0 0 1 1 1	Timer A4 Interrupt Request			
0 1 0 0 0	Timer B0 Interrupt Request			
0 1 0 0 1	Timer B1 Interrupt Request			
0 1 0 1 0	Timer B2 Interrupt Request			
0 1 0 1 1	Timer B3 Interrupt Request			
0 1 1 0 0	Timer B4 Interrupt Request			
0 1 1 0 1	Timer B5 Interrupt Request			
0 1 1 1 0	UART0 Transmit Interrupt Request			
0 1 1 1 1	UART0 Receive or ACK Interrupt Request ⁽³⁾			
1 0 0 0 0	UART1 Transmit Interrupt Request			
1 0 0 0 1	UART1 Receive or ACK Interrupt Request ⁽³⁾			
1 0 0 1 0	UART2 Transmit Interrupt Request			
1 0 0 1 1	UART2 Receive or ACK Interrupt Request ⁽³⁾			
1 0 1 0 0	UART3 Transmit Interrupt Request			
1 0 1 0 1	UART3 Receive or ACK Interrupt Request ⁽³⁾			
1 0 1 1 0	UART4 Transmit Interrupt Request			
1 0 1 1 1	UART4 Receive or ACK Interrupt Request ⁽³⁾			
1 1 0 0 0	A/D0 Interrupt Request	A/D1 Interrupt Request	A/D0 Interrupt request	A/D1 Interrupt Request
1 1 0 0 1	Intelligent I/O Interrupt 0 Request	Intelligent I/O Interrupt 7 Request	Intelligent I/O Interrupt 2 Request	Intelligent I/O Interrupt 9 Request ⁽⁴⁾
1 1 0 1 0	Intelligent I/O Interrupt 1 Request	Intelligent I/O Interrupt 8 Request	Intelligent I/O Interrupt 3 Request	Intelligent I/O Interrupt 10 Request ⁽⁵⁾
1 1 0 1 1	Intelligent I/O Interrupt 2 Request	Intelligent I/O Interrupt 9 Request ⁽⁴⁾	Intelligent I/O Interrupt 4 Request	Intelligent I/O Interrupt 11 Request ⁽⁶⁾
1 1 1 0 0	Intelligent I/O Interrupt 3 Request	Intelligent I/O Interrupt 10 Request ⁽⁵⁾	Intelligent I/O Interrupt 5 Request	Intelligent I/O Interrupt 0 Request
1 1 1 0 1	Intelligent I/O Interrupt 4 Request	Intelligent I/O Interrupt 11 Request ⁽⁶⁾	Intelligent I/O Interrupt 6 Request	Intelligent I/O Interrupt 1 Request
1 1 1 1 0	Intelligent I/O Interrupt 5 Request	Intelligent I/O Interrupt 0 Request	Intelligent I/O Interrupt 7 Request	Intelligent I/O Interrupt 2 Request
1 1 1 1 1	Intelligent I/O Interrupt 6 Request	Intelligent I/O Interrupt 1 Request	Intelligent I/O Interrupt 8 Request	Intelligent I/O Interrupt 3 Request

NOTES:

1. If the $\overline{\text{INT3}}$ pin is used as data bus in the memory expansion mode or microprocessor mode, a DMA3 interrupt request cannot be generated by an input signal to the $\overline{\text{INT3}}$ pin.
2. The falling edge and both edges of input signal into the $\overline{\text{INT}}_j$ pin ($j = 0$ to 3) cause a DMA request. The $\overline{\text{INT}}$ interrupt (the POL bit in the INTjIC register, the LVS bit, the IFSR register) is not affected and vice versa.
3. The UkSMR register and UksMR2 register ($k = 0$ to 4) switch the UARTj receive to ACK or ACK to UARTk receive.
4. The same setting is used to generate an intelligent I/O interrupt 9 request and a CAN interrupt 0 request.
5. The same setting is used to generate an intelligent I/O interrupt 10 request and a CAN interrupt 1 request.
6. The same setting is used to generate an intelligent I/O interrupt 11 request and a CAN interrupt 2 request.

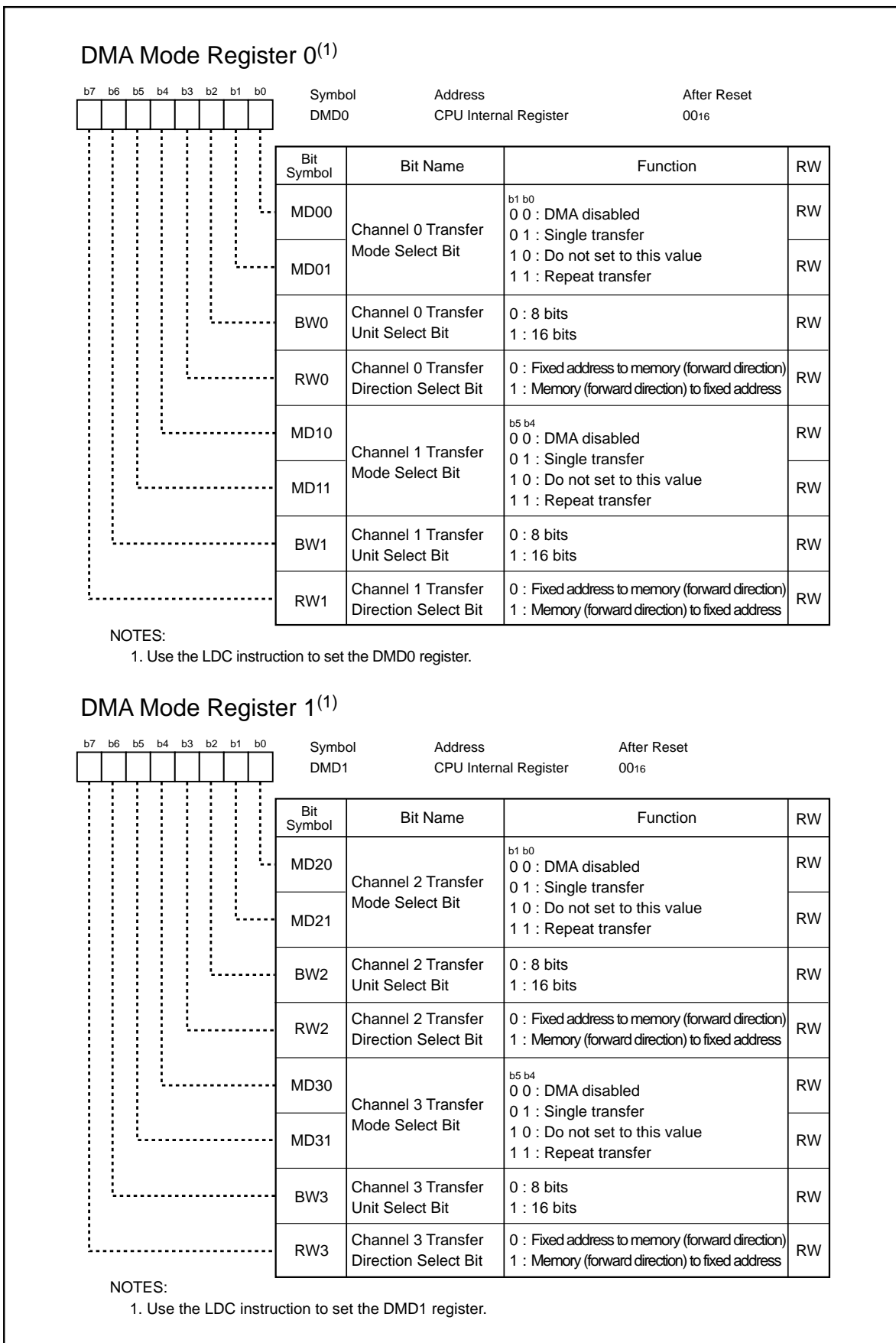


Figure 12.3 DMD0 Register, DMD1 Register

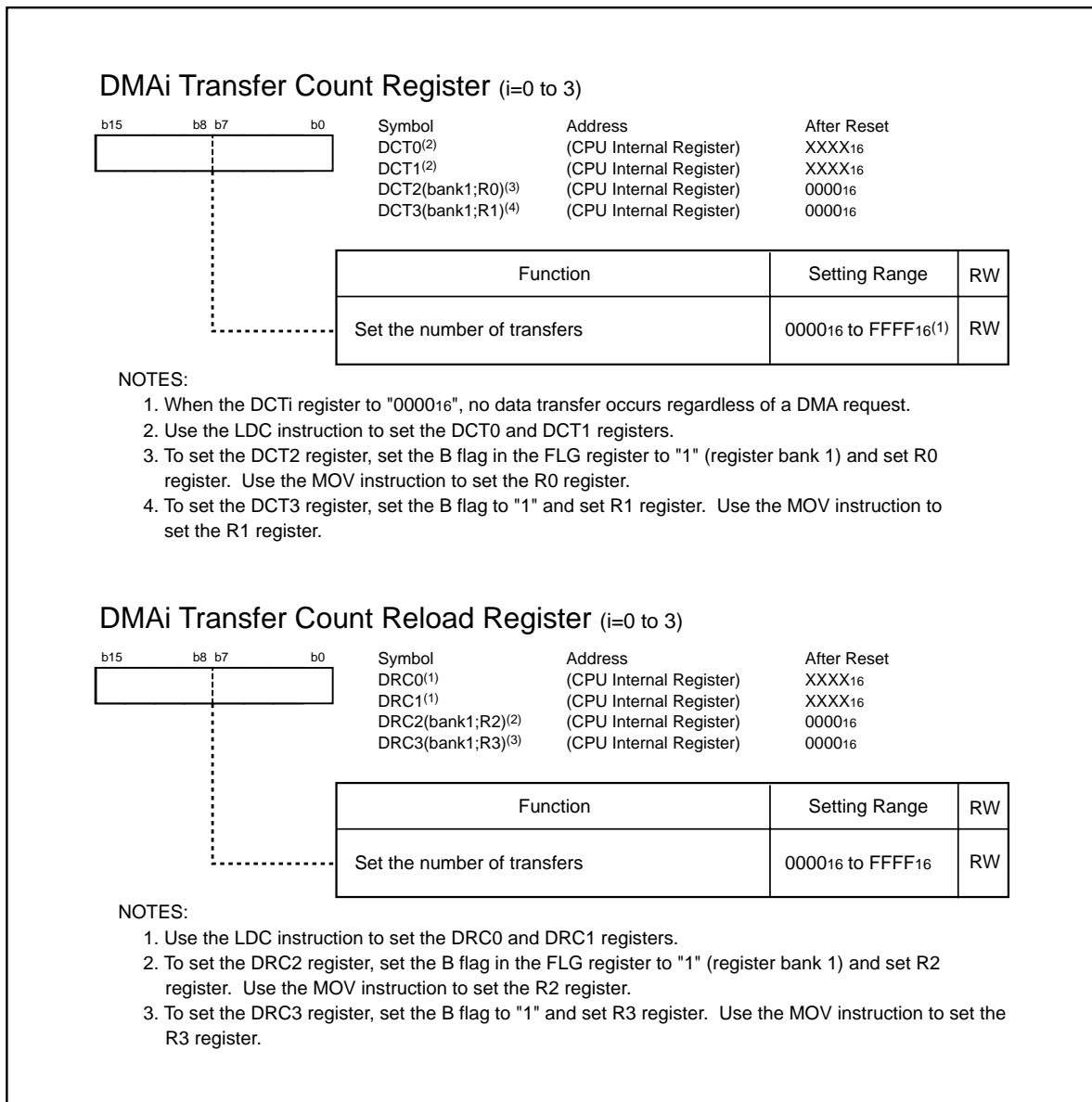


Figure 12.4 DCT0 to DCT3 Registers and DRC0 to DRC3 Registers

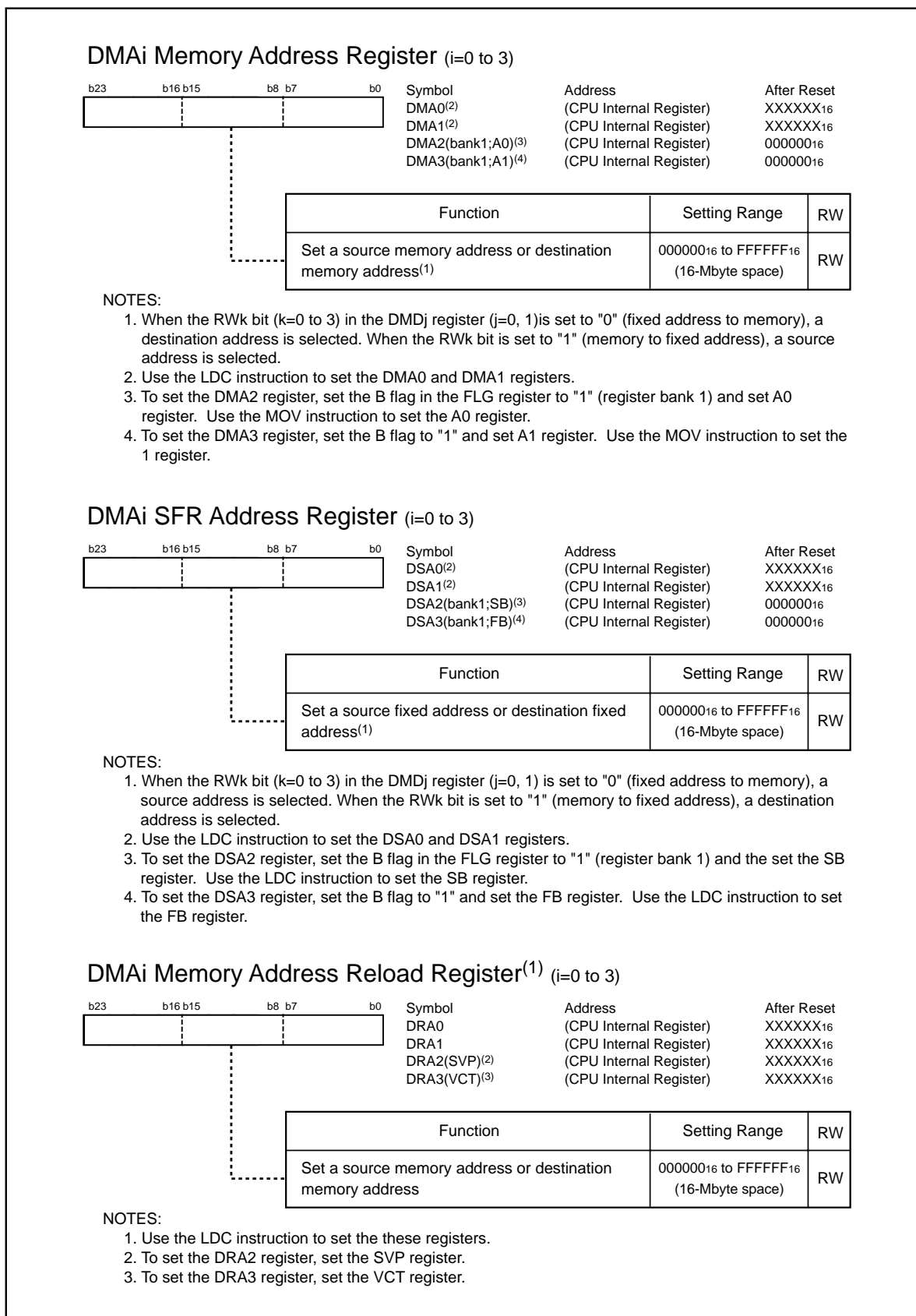


Figure 12.5 DMA0 to DMA3 Registers, DSA0 to DSA3 Registers and DRA0 to DRA3 Registers

12.1 Transfer Cycles

Transfer cycle contains a bus cycle to read data from a memory or the SFR area (source read) and a bus cycle to write data to a memory space or the SFR area (destination write). The number of read and write bus cycles depends on source and destination addresses. In memory expansion mode and microprocessor mode, the number of read and write bus cycles also depends on the DS register. Software wait state insertion and the $\overline{\text{RDY}}$ signal make a bus cycle longer.

12.1.1 Effect of Source and Destination Addresses

When a 16-bit data is transferred with a 16-bit data bus, and the source address starts with an odd address, source read cycle has one more bus cycle compared to a source address starting with an even address.

When a 16-bit data is transferred with a 16-bit data bus and the destination address starts with an odd address, destination write cycle has one more bus cycle compared to a destination address starting with an even address.

12.1.2 Effect of the DS Register

In an external space in memory expansion or microprocessor mode, transfer cycle varies depending on the data bus used at the source and destination addresses. See **Figure 7.1** for details about the DS register.

- (1) When an 8-bit data bus (the DS_i bit in the DS register is set to "0" (i=0 to 3)), accessing both source address and destination address, is used to transfer a 16-bit data, 8-bit data is transferred twice. Therefore, two bus cycles are required to read the data and another two bus cycles to write the data.
- (2) When an 8-bit data bus (the DS_i bit in the DS register is set to "0" (i=0 to 3)), accessing source address, and a 16-bit data bus, accessing destination address, are used to transfer a 16-bit data, 8-bit data is read twice but is written once as 16-bit data. Therefore, two bus cycles are required for reading and one bus cycle is for writing.
- (3) When a 16-bit data bus, accessing source address, and an 8-bit data bus, accessing destination address, are used to transfer a 16-bit data, 16-bit data is read once and 8-bit data is written twice. Therefore, one bus cycle is required for reading and two bus cycles is for writing.

12.1.3 Effect of Software Wait State

When the SFR area or memory space with software wait states is accessed, the number of cycles is incremented by software wait states.

Figure 12.6 shows an example of a transfer cycle for the source-read bus cycle. In Figure 12.6, the number of source-read bus cycles is illustrated under different conditions, provided that the destination address is an address of an external space with the destination write bus cycle as two BCLK cycles (=one bus cycle). In effect, the destination-write bus cycle is also affected by each condition and the transfer cycles change accordingly. To calculate a transfer cycle, apply respective conditions to both destination-write bus cycle and source-read bus cycle. As shown in example (2) of Figure 12.6, when an 8-bit data bus, accessing both source and destination addresses, is used to transfer a 16-bit data, two bus cycles each are required for the source-read bus cycle and destination-write bus cycle.

12.1.4 Effect of $\overline{\text{RDY}}$ Signal

In memory expansion or microprocessor mode, the $\overline{\text{RDY}}$ signal affects a bus cycle of source address or destination address is allocated address in an external space. Refer to **7.2.6 RDY Signal** for details.

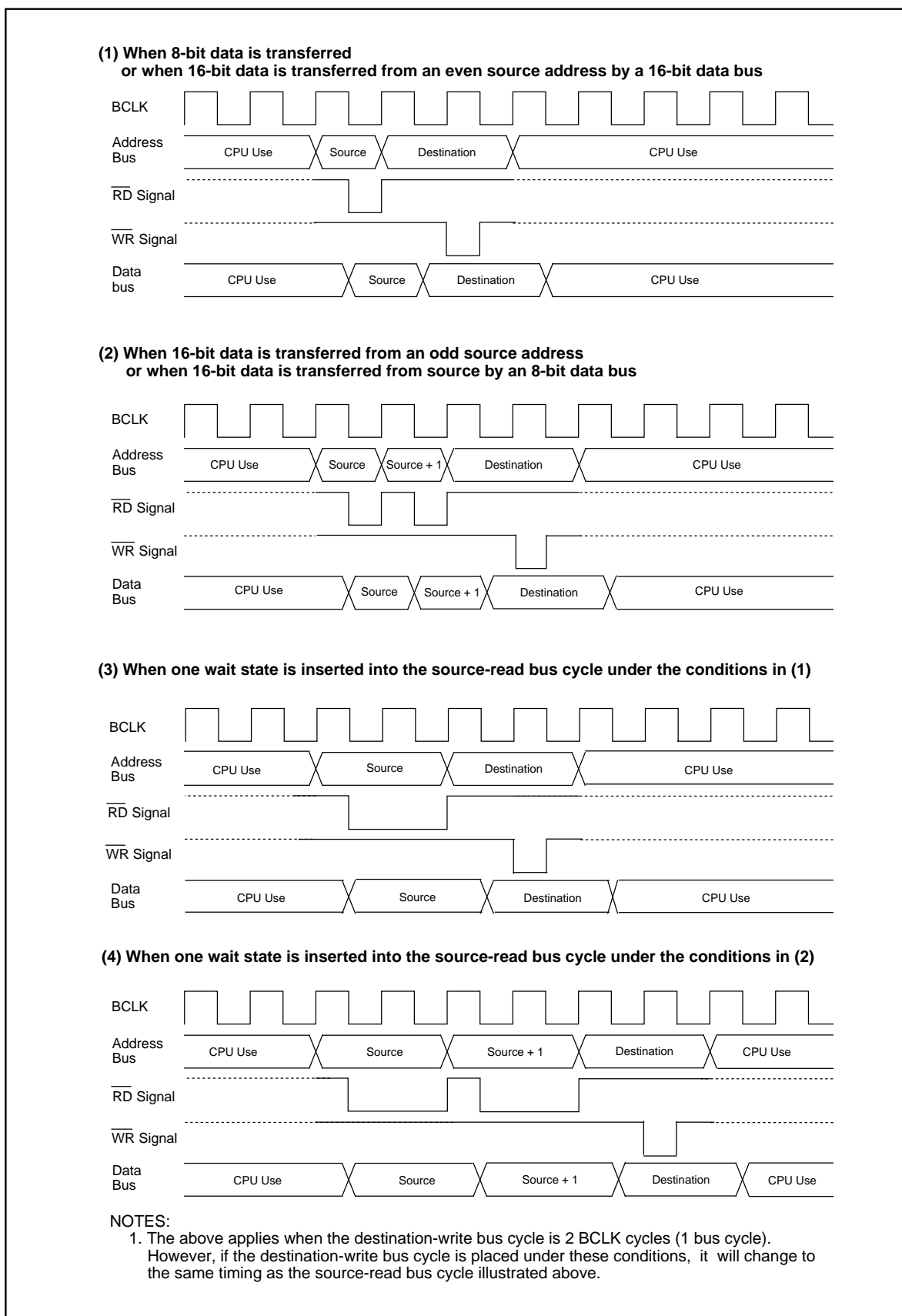


Figure 12.6 Transfer Cycle Examples with the Source-Read Bus Cycle

12.2 DMAC Transfer Cycles

The number of DMAC transfer cycle can be calculated as follows.

Any combination of even or odd transfer read and write addresses are possible. Table 12.3 lists the number of DMAC transfer cycles. Table 12.4 lists coefficient j, k.

$$\text{Transfer cycles per transfer} = \text{Number of read cycle} \times j + \text{Number of write cycle} \times k$$

Table 12.3 DMAC Transfer Cycles

Transfer Unit	Bus Width	Access Address	Single-Chip Mode		Memory Expansion Mode Microprocessor Mode	
			Read Cycle	Write Cycle	Read Cycle	Write Cycle
8-bit transfers (BWi bit in the DMDp register = 0)	16-bit	Even	1	1	1	1
		Odd	1	1	1	1
	8-bit	Even	—	—	1	1
		Odd	—	—	1	1
16-bit transfers (BWi bit = 1)	16-bit	Even	1	1	1	1
		Odd	2	2	2	2
	8-bit	Even	—	—	2	2
		Odd	—	—	2	2

i = 0 to 3, p = 0 to 1

Table 12.4 Coefficient j, k

Internal Space			External Space					
Internal ROM or Internal RAM with no wait state	Internal ROM or Internal RAM with a wait state	SFR Area	Separate Bus with no wait state	Separate Bus with 1 wait state	Separate Bus with 2 wait states	Separate Bus with 3 wait states	Multiplexed Bus with 2 wait states	Multiplexed Bus with 3 wait states
j = 1 k = 1	j = 2 k = 2	j = 2 k = 2	j = 1 k = 2	j = 2 k = 2	j = 3 k = 3	j = 4 k = 4	j = 3 k = 3	j = 4 k = 4

12.3 Channel Priority and DMA Transfer Timing

When multiple DMA requests are generated in the same sampling period, between the falling edge of the CPU clock and the next falling edge, the DRQ bit in the DMiSL register (i = 0 to 3) is set to "1" (requested) simultaneously. Channel priority in this case is : DMA0 > DMA1 > DMA2 > DMA3.

Figure 12.7 shows an example of the DMA transfer by external factors.

In Figure 12.7, the DMA0 request having the highest priority is received first to start a transfer when a DMA0 request and DMA1 request are generated simultaneously. After one DMA0 transfer is completed, the bus privilege is returned to the CPU. When the CPU has completed one bus access, the DMA1 transfer starts. After one DMA1 transfer is completed, the privilege is again returned to the CPU.

In addition, DMA requests cannot be counted up since each channel has one DRQ bit. Therefore, when DMA requests, as DMA1 in Figure 12.7, occur more than once before receiving bus privilege, the DRQ bit is set to "0" as soon as privilege is acquired. The bus privilege is returned to the CPU when one transfer is completed.

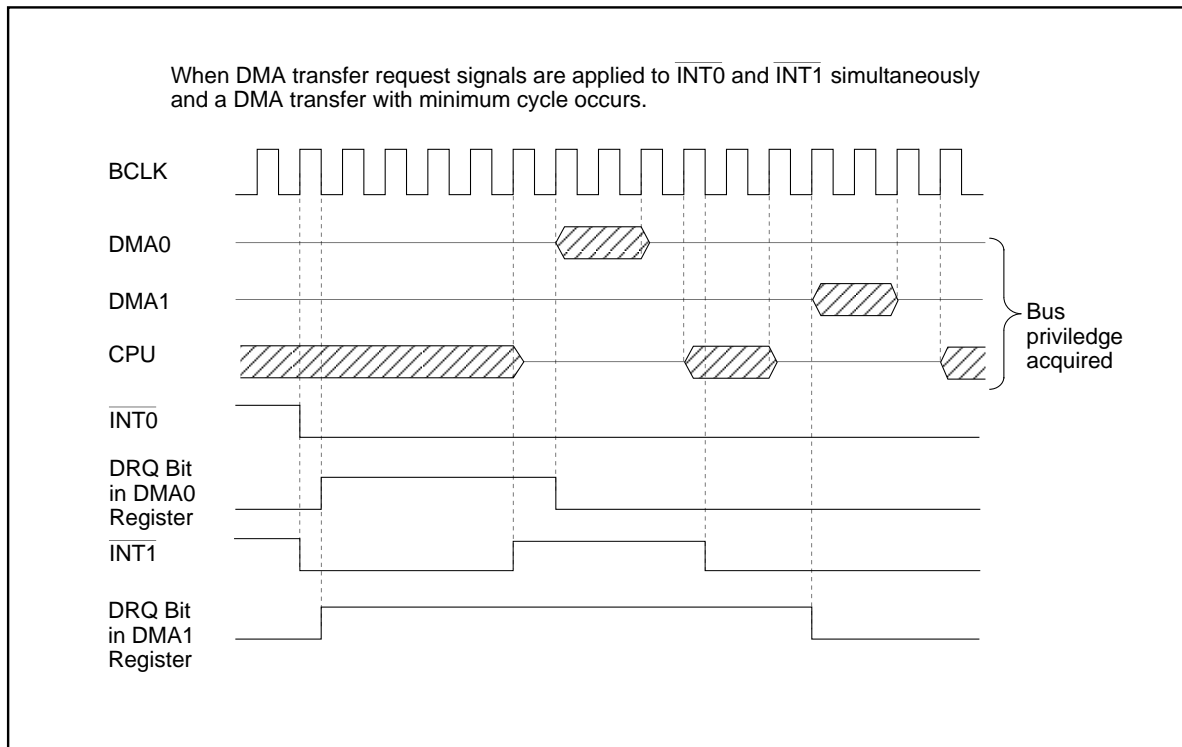


Figure 12.7 DMA Transfer by External Factors

13. DMAC II

The DMAC II performs memory-to-memory transfer, immediate data transfer and calculation transfer, which transfers the sum of two data added by an interrupt request from any peripheral functions.

Table 13.1 lists specifications of the DMAC II.

Table 13.1 DMAC II Specifications

Item	Specification
DMAC II Request Factor	Interrupt requests generated by all peripheral functions when the ILVL2 to ILVL0 bits are set to "1112"
Transfer Data	<ul style="list-style-type: none"> Data in memory is transferred to memory (memory-to-memory transfer) Immediate data is transferred to memory (immediate data transfer) Data in memory (or immediate data) + data in memory are transferred to memory (calculation transfer)
Transfer Block	8 bits or 16 bits
Transfer Space	64-Kbyte space in addresses 00000 ₁₆ to 0FFFF ₁₆ ^(1, 2)
Transfer Direction	Fixed or forward address Selected separately for each source address and destination address
Transfer Mode	Single transfer, burst transfer
Chained Transfer Function	Parameters (transfer count, transfer address and other information) are switched when transfer counter reaches zero
End-of-Transfer Interrupt	Interrupt occurs when a transfer counter reaches zero
Multiple Transfer Function	Multiple data can be transferred by a generated request for one DMA II transfer

NOTES:

- When transferring a 16-bit data to destination address 0FFFF₁₆, it is transferred to 0FFFF₁₆ and 10000₁₆. The same transfer occurs when the source address is 0FFFF₁₆.
- The actual space where transfer can occur is limited due to internal RAM capacity.

13.1 DMAC II Settings

DMAC II can be made available by setting up the following registers and tables.

- RLVL register
 - DMAC II Index
 - Interrupt control register of the peripheral function causing a DMAC II request
 - The relocatable vector table of the peripheral function causing a DMAC II request
 - IRLT bit in the IIOiIE register (i = 0 to 11) if using the intelligent I/O or CAN interrupt
- Refer to **10. Interrupts** for details on the IIOiIE register

13.1.1 RLVL Register

When the DMAII bit is set to "1" (DMAC II transfer) and the FSIT bit to "0" (normal interrupt), the DMAC II is activated by an interrupt request from any peripheral function with the ILVL2 to ILVL0 bits in the interrupt control register set to "1112" (level 7).

Figure 13.1 shows the RLVL register.

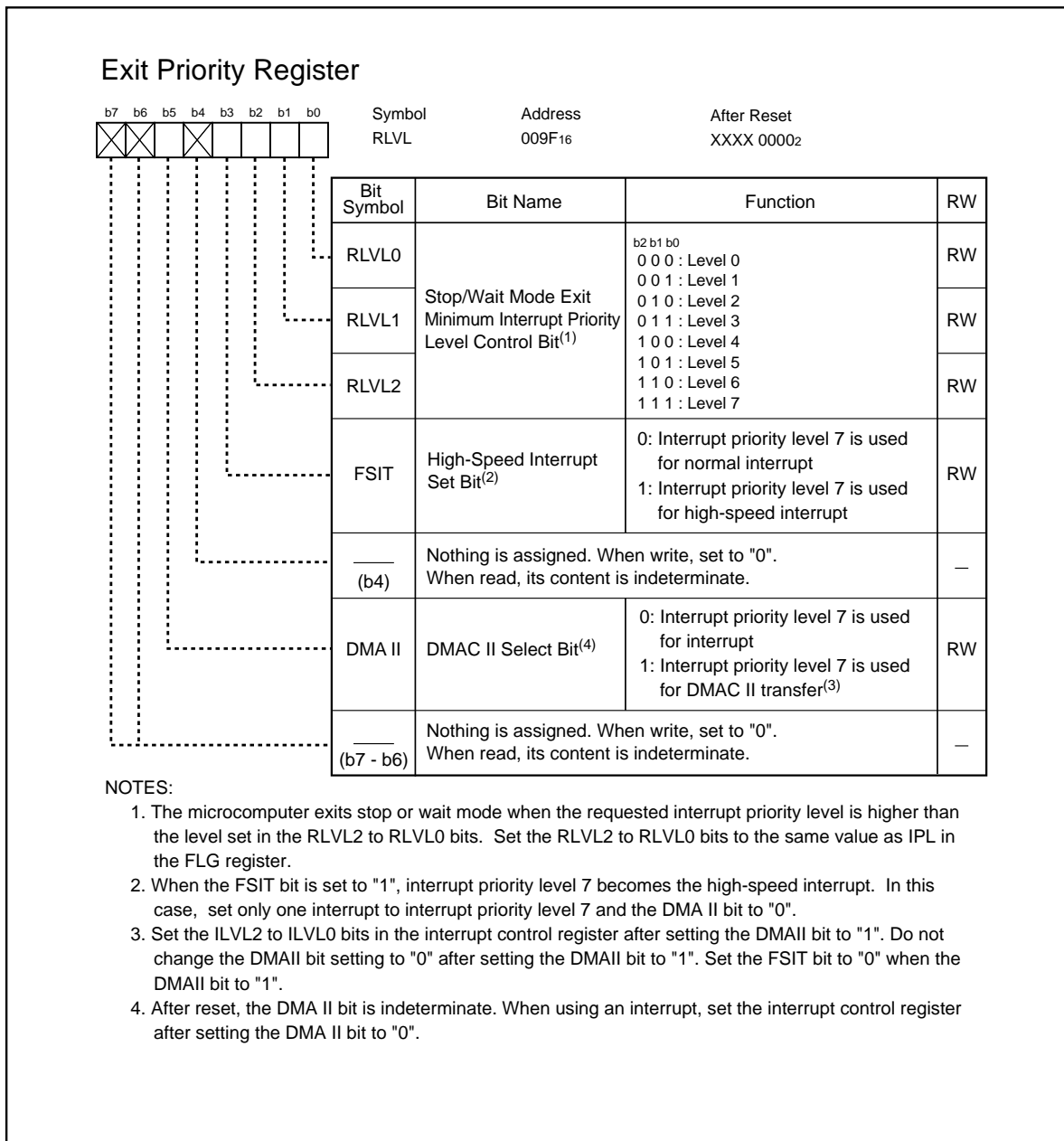


Figure 13.1 RLVL Register

13.1.2 DMAC II Index

The DMAC II index is a data table which comprises 8 to 18 bytes (maximum 32 bytes when the multiple transfer function is selected). The DMAC II index stores parameters for transfer mode, transfer counter, source address (or immediate data), operation address as an address to be calculated, destination address, chained transfer address, and end-of-transfer interrupt address.

This DMAC II index must be located on the RAM area.

Figure 13.2 shows a configuration of the DMAC II index. Table 13.2 lists a configuration of the DMAC II index in transfer mode.

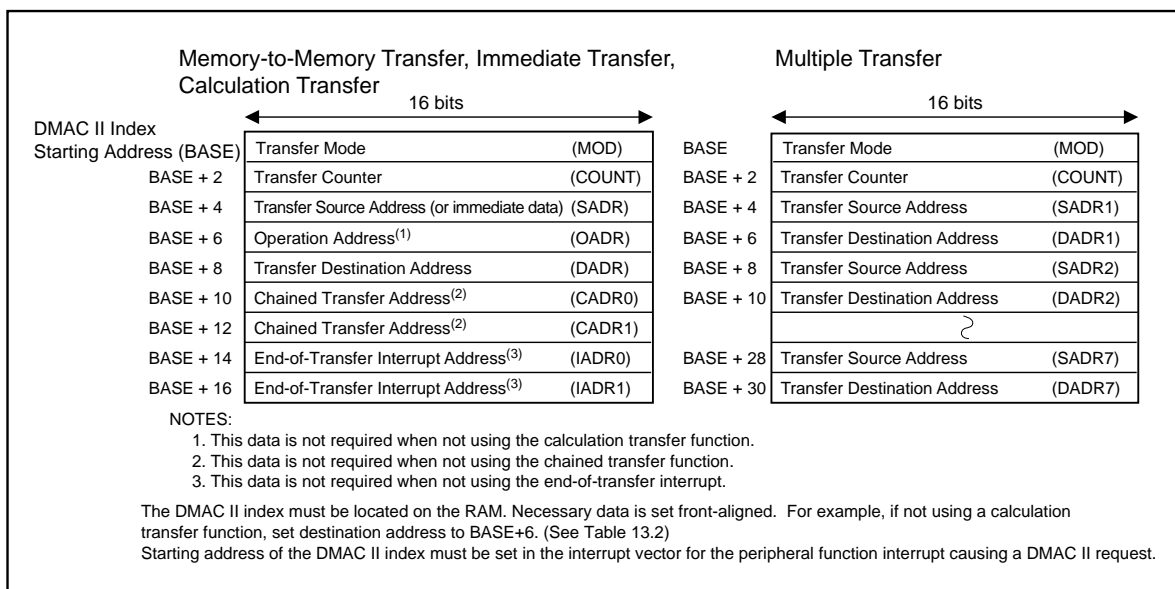


Figure 13.2 DMAC II Index

The followings are details of the DMAC II index. Set these parameters in the specified order listed in Table 13.2, according to DMAC II transfer mode.

- **Transfer mode (MOD)**

Two-byte data is required to set transfer mode. Figure 13.3 shows a configuration for transfer mode.

- **Transfer counter (COUNT)**

Two-byte data is required to set the number of transfer.

- **Transfer source address (SADR)**

Two-byte data is required to set the source memory address or immediate data.

- **Operation address (OADR)**

Two-byte data is required to set a memory address to be calculated. Set this data only when using the calculation transfer function.

- **Transfer destination address (DADR)**

Two-byte data is required to set the destination memory address.

- **Chained transfer address (CADR)**

Four-byte data is required to set the starting address of the DMAC II index for the next transfer. Set this data only when using the chained transfer function.

- **End-of-transfer interrupt address (IADR)**

Four-byte data is required to set a jump address for end-of-transfer interrupt processing. Set this data only when using the end-of-transfer interrupt.

Table 13.2 DMAC II Index Configuration in Transfer Mode

	Memory-to-Memory Transfer /Immediate Data Transfer				Calculation Transfer				Multiple Transfer																																																										
Chained Transfer	Not Used	Used	Not Used	Used	Not Used	Used	Not Used	Used	Not Available																																																										
End-of-Transfer Interrupt	Not Used	Not Used	Used	Used	Not Used	Not Used	Used	Used	Not Available																																																										
DMAC II Index	<table border="1"> <tr><td>MOD</td></tr> <tr><td>COUNT</td></tr> <tr><td>SADR</td></tr> <tr><td>DADR</td></tr> </table> <p>8 bytes</p>	MOD	COUNT	SADR	DADR	<table border="1"> <tr><td>MOD</td></tr> <tr><td>COUNT</td></tr> <tr><td>SADR</td></tr> <tr><td>DADR</td></tr> <tr><td>CADR0</td></tr> <tr><td>CADR1</td></tr> </table> <p>12 bytes</p>	MOD	COUNT	SADR	DADR	CADR0	CADR1	<table border="1"> <tr><td>MOD</td></tr> <tr><td>COUNT</td></tr> <tr><td>SADR</td></tr> <tr><td>DADR</td></tr> <tr><td>IADR0</td></tr> <tr><td>IADR1</td></tr> </table> <p>12 bytes</p>	MOD	COUNT	SADR	DADR	IADR0	IADR1	<table border="1"> <tr><td>MOD</td></tr> <tr><td>COUNT</td></tr> <tr><td>SADR</td></tr> <tr><td>DADR</td></tr> <tr><td>OADR</td></tr> <tr><td>DADR</td></tr> <tr><td>CADR0</td></tr> <tr><td>CADR1</td></tr> <tr><td>IADR0</td></tr> <tr><td>IADR1</td></tr> </table> <p>16 bytes</p>	MOD	COUNT	SADR	DADR	OADR	DADR	CADR0	CADR1	IADR0	IADR1	<table border="1"> <tr><td>MOD</td></tr> <tr><td>COUNT</td></tr> <tr><td>SADR</td></tr> <tr><td>OADR</td></tr> <tr><td>DADR</td></tr> <tr><td>CADR0</td></tr> <tr><td>CADR1</td></tr> </table> <p>10 bytes</p>	MOD	COUNT	SADR	OADR	DADR	CADR0	CADR1	<table border="1"> <tr><td>MOD</td></tr> <tr><td>COUNT</td></tr> <tr><td>SADR</td></tr> <tr><td>OADR</td></tr> <tr><td>DADR</td></tr> <tr><td>CADR0</td></tr> <tr><td>CADR1</td></tr> </table> <p>14 bytes</p>	MOD	COUNT	SADR	OADR	DADR	CADR0	CADR1	<table border="1"> <tr><td>MOD</td></tr> <tr><td>COUNT</td></tr> <tr><td>SADR</td></tr> <tr><td>OADR</td></tr> <tr><td>DADR</td></tr> <tr><td>IADR0</td></tr> <tr><td>IADR1</td></tr> </table> <p>14 bytes</p>	MOD	COUNT	SADR	OADR	DADR	IADR0	IADR1	<table border="1"> <tr><td>MOD</td></tr> <tr><td>COUNT</td></tr> <tr><td>SADR</td></tr> <tr><td>DADR</td></tr> <tr><td>OADR</td></tr> <tr><td>CADR0</td></tr> <tr><td>CADR1</td></tr> <tr><td>IADR0</td></tr> <tr><td>IADR1</td></tr> <tr><td>SADRi</td></tr> <tr><td>DADRi</td></tr> </table> <p>18 bytes</p>	MOD	COUNT	SADR	DADR	OADR	CADR0	CADR1	IADR0	IADR1	SADRi	DADRi	<p>i=1 to 7 Max 32 bytes (when i=7)</p>
	MOD																																																																		
COUNT																																																																			
SADR																																																																			
DADR																																																																			
MOD																																																																			
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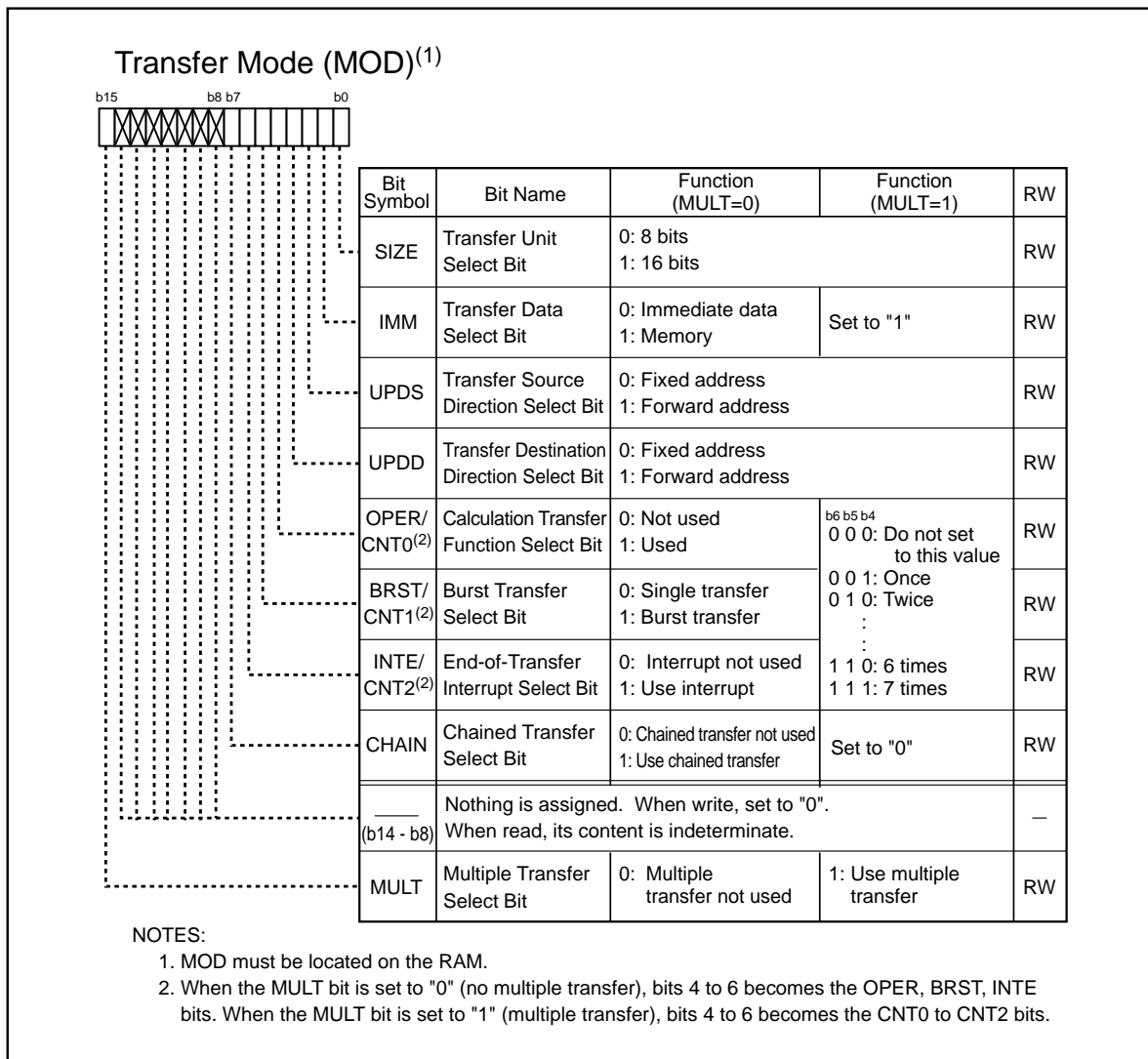


Figure 13.3 MOD

13.1.3 Interrupt Control Register for the Peripheral Function

For the peripheral function interrupt activating a DMAC II request, set the ILVL2 to ILVL0 bits to "1112" (level 7).

13.1.4 Relocatable Vector Table for the Peripheral Function

Set the starting address of the DMAC II index in the interrupt vector for the peripheral function interrupt activating a DMAC II request.

When using the chained transfer, the relocatable vector table must be located in the RAM.

13.1.5 IRLT Bit in the IIOiE Register (i=0 to 11)

When the intelligent I/O interrupt or CAN interrupt is used to activate DMAC II, set the IRLT bit in the IIOiE register of the interrupt to "0".

13.2 DMAC II Performance

The DMAC II function is selected by setting the DMA II bit to "1" (DMAC II transfer). DMAC II request is activated by all peripheral function interrupts with the ILVL2 to ILVL0 bits set to "1112" (level 7). These peripheral function interrupt request signals become DMAC II transfer request signals and the peripheral function interrupt cannot be used.

When an interrupt request is generated by setting the ILVL2 to ILVL0 bits to "1112" (level 7), the DMAC II is activated regardless of what state the I flag and IPL is in.

13.3 Transfer Data

The DMAC II transfers 8-bit or 16-bit data.

- Memory-to-memory transfer : Data is transferred from a desired memory location in a 64-Kbyte space (Addresses 00000₁₆ to 0FFFF₁₆) to another desired memory location in the same space.
- Immediate data transfer : Immediate data is transferred to a desired memory location in a 64-Kbyte space.
- Calculation transfer : Two 8-bit or 16-bit data are added together and the result is transferred to a desired memory location in a 64K-byte space.

When a 16-bit data is transferred to the destination address 0FFFF₁₆, it is transferred to 0FFFF₁₆ and 10000₁₆. The same transfer occurs when the source address is 0FFFF₁₆.

13.3.1 Memory-to-Memory Transfer

Data transfer between any two memory locations can be:

- a transfer from a fixed address to another fixed address
- a transfer from a fixed address to a relocatable address
- a transfer from a relocatable address to a fixed address
- a transfer from a relocatable address to another relocatable address

When a relocatable address is selected, the DMAC II increments address, after a transfer, for the next transfer. In a 8-bit transfer, the transfer address is incremented by one. In a 16-bit transfer, the transfer address is incremented by two.

When a source or destination address exceeds address 0FFFF₁₆ as a result of address incrementation, the source or destination address returns to address 00000₁₆ and continues incrementation. Maintain source and destination address at address 0FFFF₁₆ or below.

13.3.2 Immediate Data Transfer

The DMAC II transfers immediate data to a desired memory location. A fixed or relocatable address can be selected as the destination address. Store the immediate data into SADR. To transfer an 8-bit immediate data, write the data in the low-order byte of SADR (high-order byte is ignored).

13.3.3 Calculation Transfer

After two memory data, or an immediate data and memory data are added together, the calculated result is transferred to a desired memory location. SADR must have one memory location address to be calculated or immediate data. OADR must have the other memory location address to be calculated. Fixed or relocatable address can be selected as source and destination addresses when using a memory + memory calculation transfer. If the transfer source address is relocatable, the operation address also becomes relocatable. Fixed or relocatable address can be selected as the transfer destination address when using an immediate data + memory calculation transfer.

13.4 Transfer Modes

In DMAC II, single and burst transfers are available. The BRST bit in MOD selects transfer method, either the single transfer or burst transfer. COUNT determines how many transfers occur. No transfer occurs when COUNT is set to "0000₁₆". All interrupts are ignored while transfer is in progress.

13.4.1 Single Transfer

For every transfer request factor, the DMAC II transfers one transfer unit of 8-bit or 16-bit data once. When the source or destination address is relocatable, the DMAC II increments the address, after a transfer, for the next transfer.

COUNT is decremented every time a transfer occurs. When using the end-of-transfer interrupt, the interrupt is acknowledged when COUNT reaches "0".

13.4.2 Burst Transfer

For every transfer request factor, the DMAC II continuously transfers data the number of times determined by COUNT. The DMAC II decrements COUNT every time a transfer occurs. The burst transfer ends when COUNT reaches "0". The end-of-transfer interrupt is acknowledged when the burst transfer ends if using the end-of-transfer interrupt. All interrupts are ignored while the burst transfer is in progress.

13.4.3 Multiple Transfer

The MULT bit in MOD selects the multiple transfer. When using the multiple transfer, select the memory-to-memory transfer. One transfer request factor initiates multiple transfers. The CNT2 to CNT0 bits in MOD selects the number of transfers from "001₂" (once) to "111₂" (7 times). Do not set the CNT2 to CNT0 bits to "000₂".

The transfer source and destination addresses for each transfer must be allocated alternately to addresses following MOD and COUNT. When the multiple transfer is selected, the calculation transfer, burst transfer, end-of-transfer interrupt and chained transfer cannot be used.

13.4.4 Chained Transfer

The CHAIN bit in MOD selects the chained transfer.

The following process initiates the chained transfer.

- (1) Transfer, caused by a transfer request factor, occurs according to the content of the DMAC II index. The vectors of the request factor indicates the address where the DMAC II index is allocated. For each request, the BRST bit in MOD selects either single or burst transfer.
- (2) When COUNT reaches "0", the contents of CADR1 to CADR0 are written to the vector of the request factor. When the INTE bit in the MOD is set to "1," the end-of-transfer interrupt is generated simultaneously.
- (3) When the next DMAC II transfer request is generated, transfer occurs according to the contents of the DMAC II index indicated by the vector rewritten in (2).

Figure 13.4 shows the relocatable vector and DMACII index of when the chained transfer is in progress. For the chained transfer, the relocatable vector table must be located in the RAM.

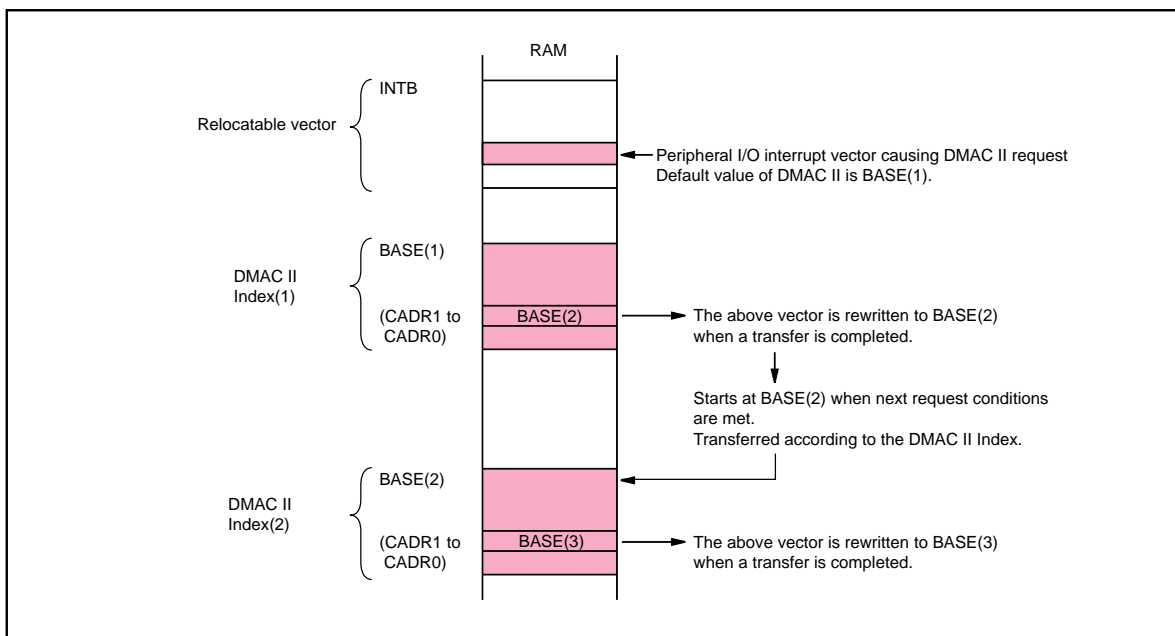


Figure 13.4 Relocatable Vector and DMAC II Index

13.4.5 End-of-Transfer Interrupt

The INTE bit in MOD selects the end-of-transfer interrupt. Set the starting address of the end-of-transfer interrupt service routine in the IADR1 to IADR0 bits. The end-of-transfer interrupt is generated when COUNT reaches "0."

13.5 Execution Time

DMAC II execution cycle is calculated by the following equations:

Multiple transfers: $t = 21 + (11 + b + c) \times k$ cycles

Other than multiple transfers: $t = 6 + (26 + a + b + c + d) \times m + (4 + e) \times n$ cycles

a: If IMM = 0 (source of transfer is immediate data), a = 0;

if IMM = 1 (source of transfer is memory), a = -1

b: If UPDS = 1 (source transfer address is a relocatable address), b = 0;

if UPDS = 0 (source transfer address is a fixed address), b = 1

c: If UPDD = 1 (destination transfer address is a relocatable address), c = 0;

if UPDD = 0 (destination transfer address is a fixed address), c = 1

d: If OPER = 0 (calculation function is not selected), d = 0;

if OPER = 1 (calculation function is selected) and UPDS = 0 (source of transfer is immediate data or fixed address memory), d = 7;

if OPER = 1 (calculation function is selected) and UPDS = 1 (source of transfer is relocatable address memory), d = 8

e: If CHAIN = 0 (chained transfer is not selected), e = 0; if CHAIN = 1 (chained transfer is selected), e = 4

m: BRST = 0 (single transfer), m = 1; BRST = 1 (burst transfer), m = the value set in COUNT

n: If COUNT = 1, n = 0; if COUNT = 2 or more, n = 1

k: Number of transfers set in the CNT2 to CNT0 bits

The equations above are approximations. The number of cycles may change with CPU state, bus wait state, and DMAC II index allocation.

The first instruction from the end-of-transfer interrupt service routine is executed in the 8th cycle after the DMAC II transfer is completed.

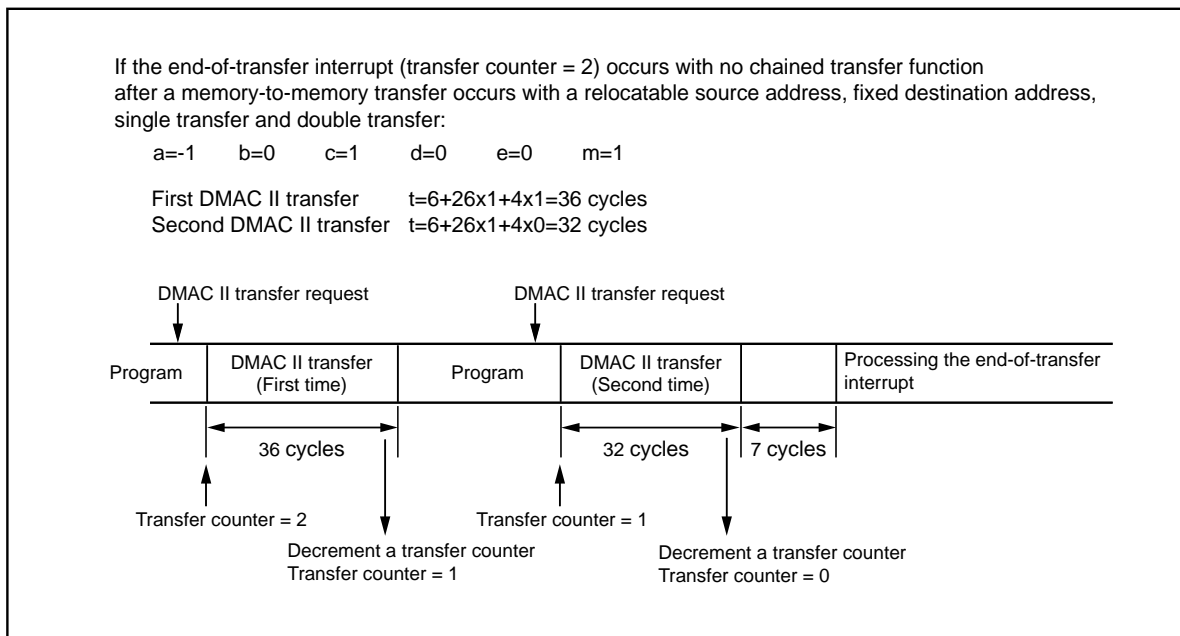


Figure 13.5 Transfer Cycle

When an interrupt request which acts as a DMAC II transfer request factor and another interrupt request with higher priority (e.g., $\overline{\text{NMI}}$ or watchdog timer) are generated simultaneously, the interrupt with higher priority takes precedence over the DMAC II transfer. The pending DMAC II transfer starts after the interrupt sequence has been completed.

14. Timer

The microcomputer has eleven 16-bit timers. Five timers A and six timers B have different functions. Each timer operates independently. The count source for each timer is the clock for timer operations including counting and reloading, etc. Figures 14.1 and 14.2 show block diagrams of timer A and timer B configuration.

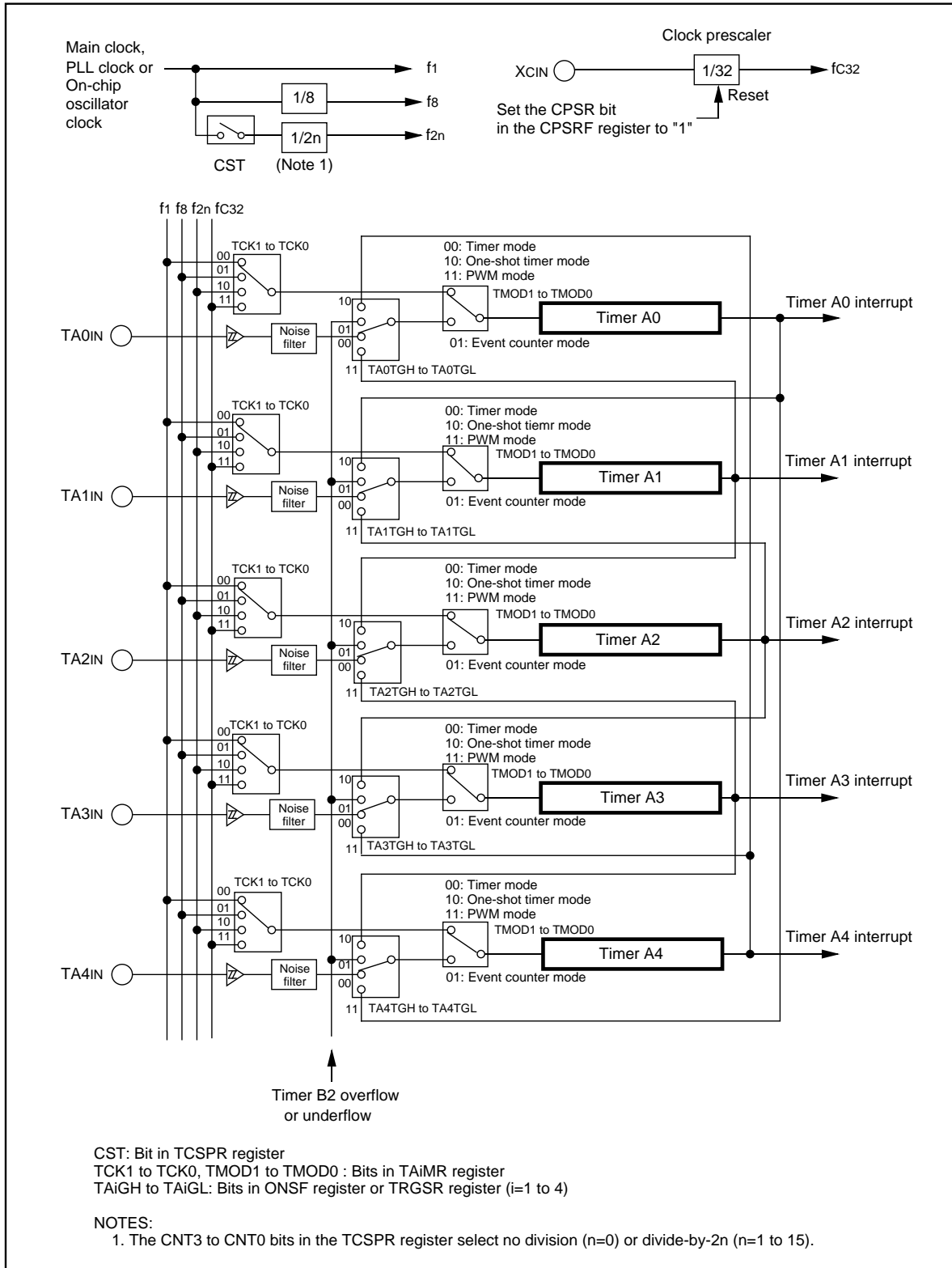


Figure 14.1 Timer A Configuration

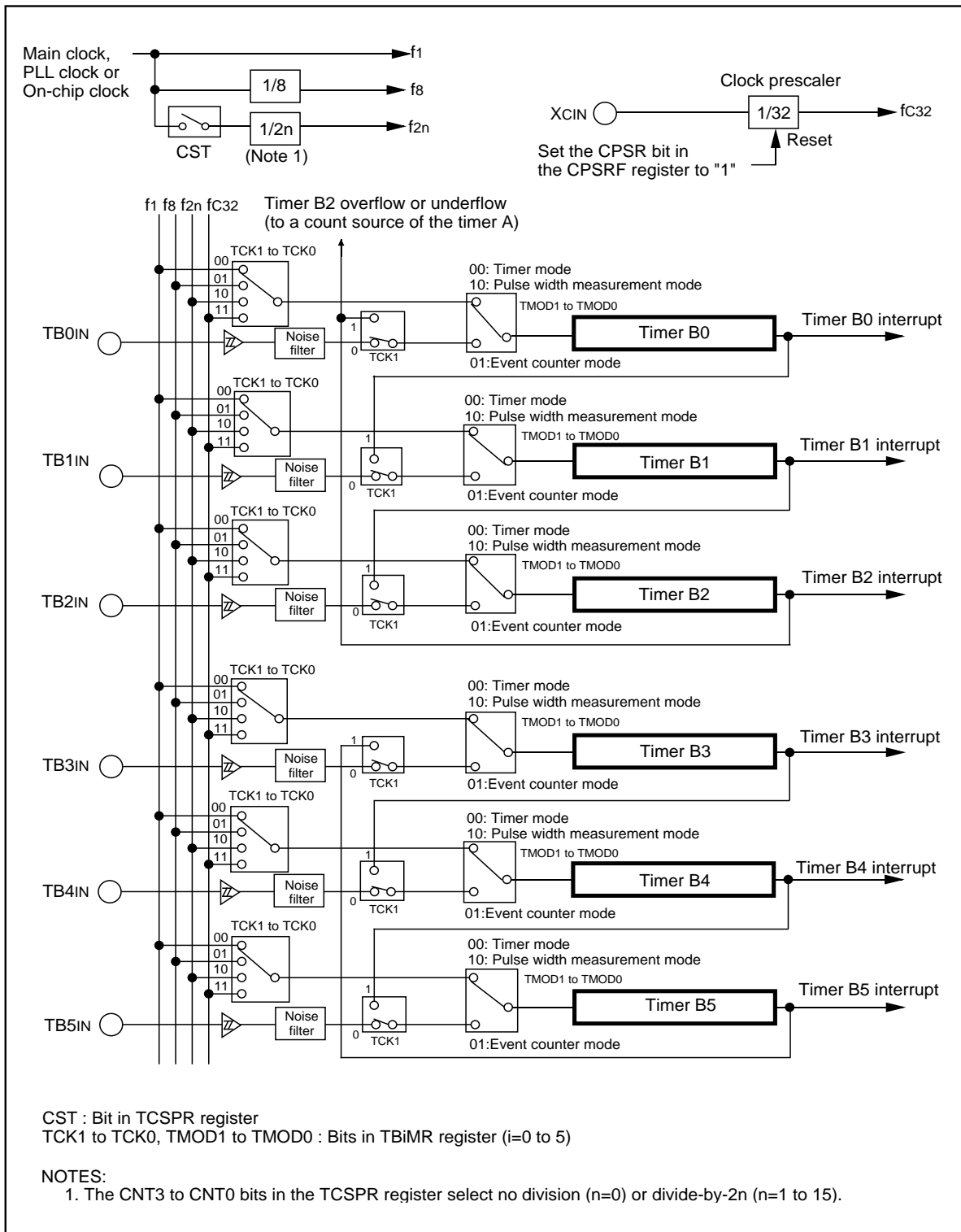


Figure 14.2 Timer B Configuration

14.1 Timer A

Figure 14.3 shows a block diagram of the timer A. Figures 14.4 to 14.7 show registers associated with the timer A.

The timer A supports the following four modes. Except in event counter mode, all timers A0 to A4 have the same function. The TMOD1 to TMOD0 bits in the TAI_{MR} register (i=0 to 4) determine which mode is used.

- Timer mode: The timer counts an internal count source.
- Event counter mode: The timer counts an external pulse or an overflow and underflow of other timers.
- One-shot timer mode: The timer outputs one valid pulse until the counter reaches "0000₁₆".
- Pulse width modulation mode: The timer continuously outputs desired pulse widths.

Table 14.1 lists TAI_{OUT} pin settings when used as an output. Table 14.2 lists TAI_{IN} and TAI_{OUT} pin settings when used as an input.

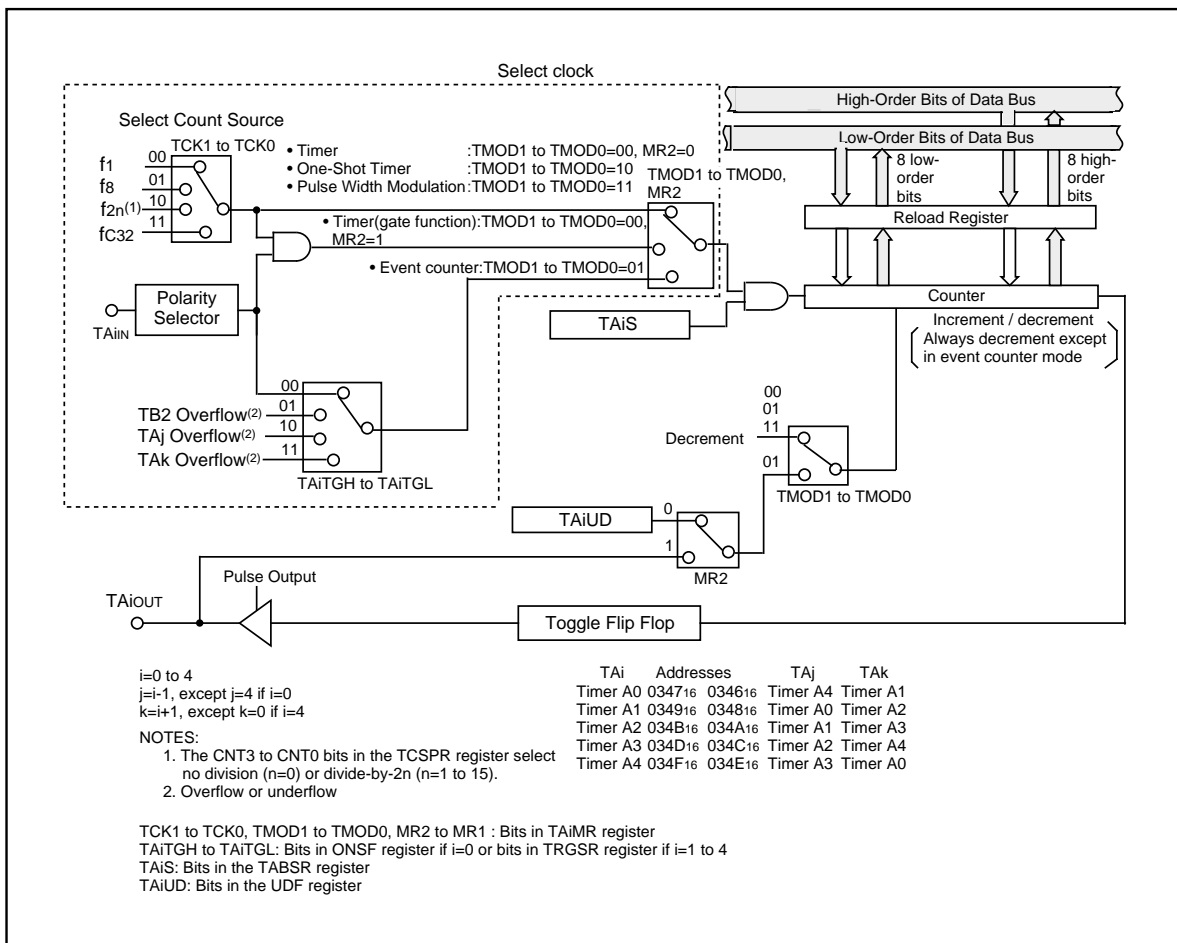


Figure 14.3 Timer A Block Diagram

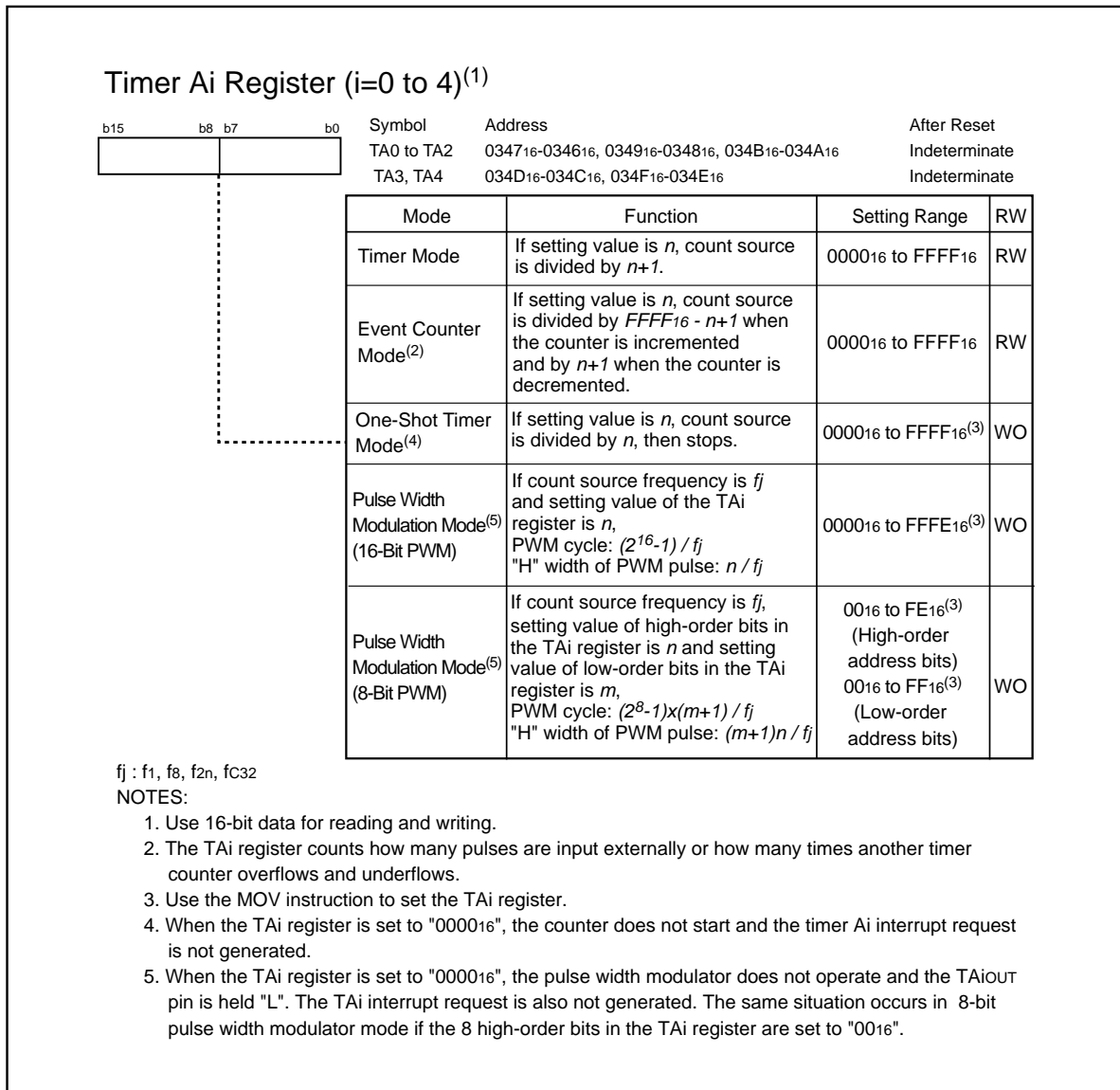


Figure 14.4 TA0 to TA4 Registers

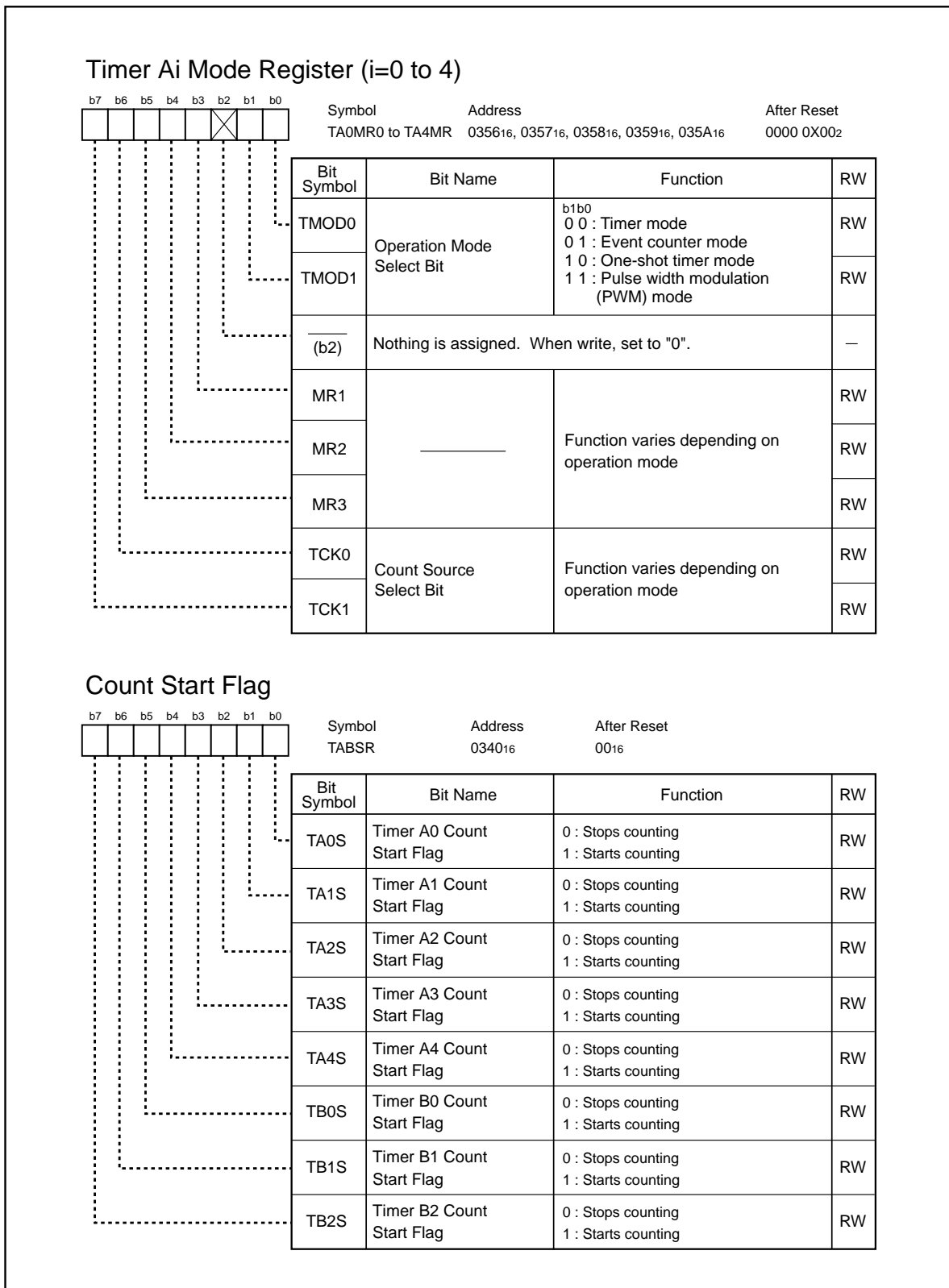


Figure 14.5 TA0MR to TA4MR Registers and TABSR Register

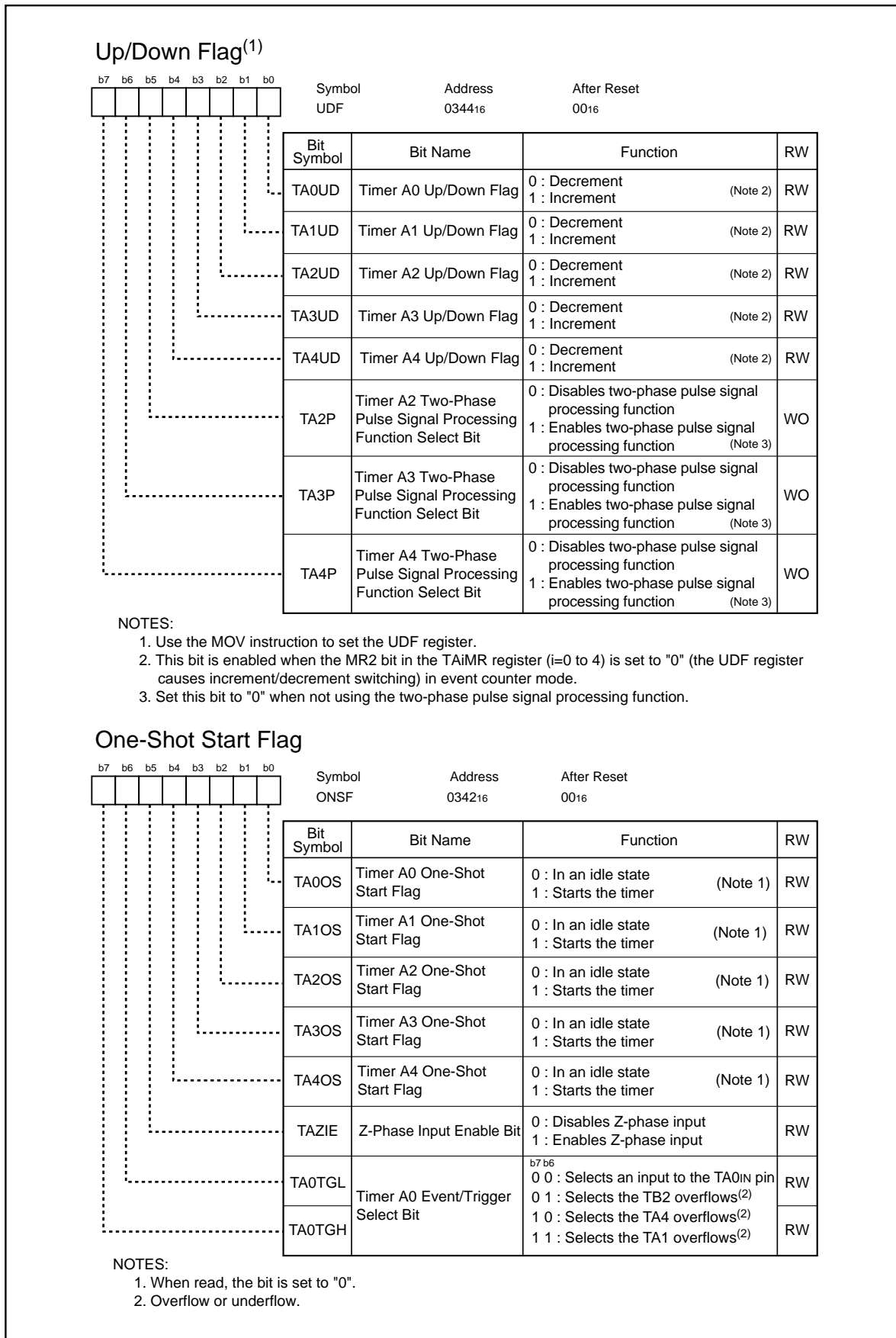


Figure 14.6 UDF Register and ONSF Register

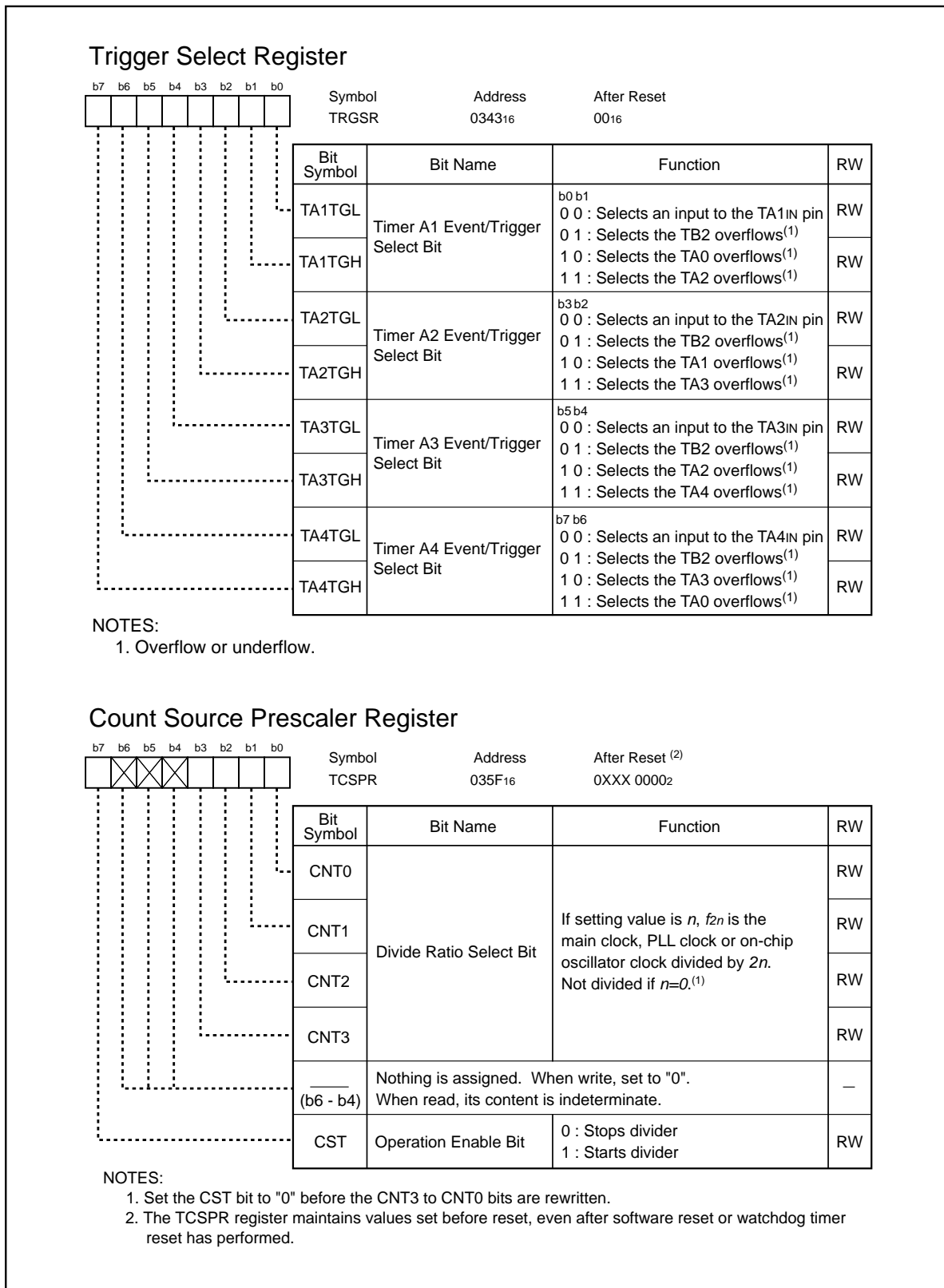


Figure 14.7 TRGSR Register and TCSPR Register

Table 14.1 Pin Settings for Output from TAIOUT Pin (i=0 to 4)

Pin	Setting		
	PS1, PS2 Registers	PSL1, PSL2 Registers	PSC Register
P70/TA0OUT ⁽¹⁾	PS1_0= 1	PSL1_0=1	PSC_0= 0
P72/TA1OUT	PS1_2= 1	PSL1_2=1	PSC_2= 0
P74/TA2OUT	PS1_4= 1	PSL1_4=0	PSC_4= 0
P76/TA3OUT	PS1_6= 1	PSL1_6=1	PSC_6= 0
P80/TA4OUT	PS2_0= 1	PSL2_0=0	–

NOTES:

1. P70/TA0OUT is a port for the N-channel open drain output.

Table 14.2 Pin Settings for Input to TAIIN and TAIOUT Pins (i=0 to 4)

Pin	Setting	
	PS1, PS2 Registers	PD7, PD8 Registers
P70/TA0OUT	PS1_0=0	PD7_0=0
P71/TA0IN	PS1_1=0	PD7_1=0
P72/TA1OUT	PS1_2=0	PD7_2=0
P73/TA1IN	PS1_3=0	PD7_3=0
P74/TA2OUT	PS1_4=0	PD7_4=0
P75/TA2IN	PS1_5=0	PD7_5=0
P76/TA3OUT	PS1_6=0	PD7_6=0
P77/TA3IN	PS1_7=0	PD7_7=0
P80/TA4OUT	PS2_0=0	PD8_0=0
P81/TA4IN	PS2_1=0	PD8_1=0

14.1.1 Timer Mode

In timer mode, the timer counts an internally generated count source (see Table 14.3). Figure 14.8 shows the TAI_{MR} register (i=0 to 4) in timer mode.

Table 14.3 Specifications in Timer Mode

Item	Specification
Count Source	f ₁ , f ₈ , f _{2n} ⁽¹⁾ , f _{C32}
Counting Operation	<ul style="list-style-type: none"> The timer decrements a counter value When the timer counter underflows, content of the reload register is reloaded into the count register and counting resumes.
Divide Ratio	1/(n+1) n: setting value of the TAI register (i=0 to 4) 0000 ₁₆ to FFFF ₁₆
Counter Start Condition	The TAI _S bit in the TABSR register is set to "1" (starts counting)
Counter Stop Condition	The TAI _S bit is set to "0" (stops counting)
Interrupt Request Generation Timing	The timer counter underflows
TAI _{IN} Pin Function	Programmable I/O port or gate input
TAI _{OUT} Pin Function	Programmable I/O port or pulse output
Read from Timer	The TAI register indicates counter value
Write to Timer	<ul style="list-style-type: none"> When the timer counter stops, the value written to the TAI register is also written to both reload register and counter While counting, the value written to the TAI register is written to the reload register (It is transferred to the counter at the next reload timing)
Selectable Function	<ul style="list-style-type: none"> Gate function Input signal to the TAI_{IN} pin determines whether the timer counter starts or stops counting Pulse output function The polarity of the TAI_{OUT} pin is inversed whenever the timer counter underflows

NOTES:

- The CNT3 to CNT0 bits in the TCSPR register select no division (n=0) or divide-by-2n (n=1 to 15).

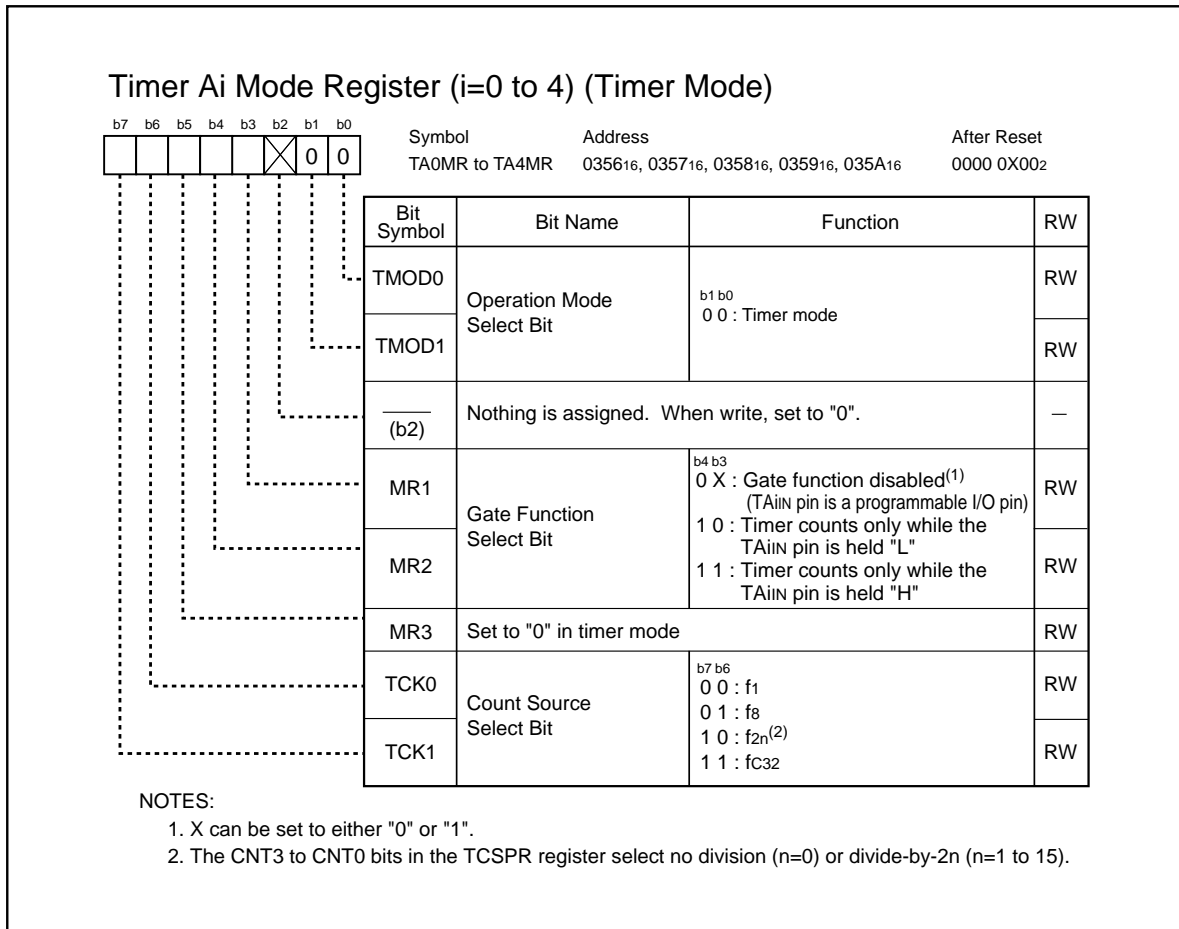


Figure 14.8 TA0MR to TA4MR Registers

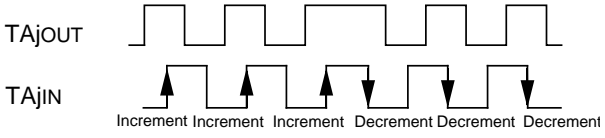
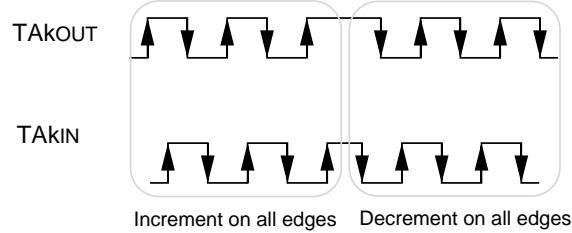
14.1.2 Event Counter Mode

In event counter mode, the timer counts how many external signals are applied or how many times another timer overflows and underflows. The timers A2, A3 and A4 can count externally generated two-phase signals. Table 14.4 lists specifications in event counter mode (when not handling a two-phase pulse signal). Table 14.5 lists specifications in event counter mode (when handling a two-phase pulse signal with the timer A2, A3 and A4). Figure 14.9 shows the TAI_{MR} (i=0 to 4) register in event counter mode.

Table 14.4 Specifications in Event Counter Mode (when not processing two-phase pulse signal)

Item	Specification
Count Source	<ul style="list-style-type: none"> External signal applied to the TAI_{IN} pin (i = 0 to 4) (valid edge can be selected by program) Timer B2 overflow or underflow signal, timer A_j overflow or underflow signal (j=i-1, except j=4 if i=0) and timer A_k overflow or underflow signal (k=i+1, except k=0 if i=4)
Counting Operation	<ul style="list-style-type: none"> External signal and program can determine whether the timer increments or decrements the counter When the timer counter underflows or overflows, the content of the reload register is reloaded into the count register and counting resumes. When the free-running count function is selected, the timer counter continues running without reloading.
Divide Ratio	<ul style="list-style-type: none"> 1/(FFFF₁₆ - n + 1) for counter increment 1/(n + 1) for counter decrement n : setting value of the TAI register 0000₁₆ to FFFF₁₆
Counter Start Condition	The TAI _S bit in the TABSR register is set to "1" (starts counting)
Counter Stop Condition	The TAI _S bit is set to "0" (stops counting)
Interrupt Request Generation Timing	The timer counter overflows or underflows
TAI _{IN} Pin Function	Programmable I/O port or count source input
TAI _{OUT} Pin Function	Programmable I/O port, pulse output or input selecting a counter increment or decrement
Read from Timer	The TAI register indicates counter value
Write to Timer	<ul style="list-style-type: none"> When the timer counter stops, the value written to the TAI register is also written to both reload register and counter While counting, the value written to the TAI register is written to the reload register (It is transferred to the counter at the next reload timing)
Selectable Function	<ul style="list-style-type: none"> Free-running count function Content of the reload register is not reloaded even if the timer counter overflows or underflows Pulse output function The polarity of the TAI_{OUT} pin is inversed whenever the timer counter overflows or underflows

Table 14.5 Specifications in Event Counter Mode (when processing two-phase pulse signal on timer A2, A3 and A4)

Item	Specification
Count Source	Two-phase pulse signal applied to the TAIIN pin, or TAIIN and TAIOUT pin (i = 2 to 4)
Counting Operation	<ul style="list-style-type: none"> Two-phase pulse signal determines whether the timer increments or decrements a counter value When the timer counter overflows or underflows, content of the reload register is reloaded into the count register and counting resumes. With the free-running count function, the timer counter continues running without reloading.
Divide Ratio	<ul style="list-style-type: none"> 1/ (FFFF₁₆ - n + 1) for counter increment 1/ (n + 1) for counter decrement n : setting value of the TAI register 0000₁₆ to FFFF₁₆
Counter Start Condition	The TAI _S bit in the TABSR register is set to "1" (starts counting)
Counter Stop Condition	The TAI _S bit is set to "0" (stops counting)
Interrupt Request Generation Timing	The timer counter overflows or underflows
TAIIN Pin Function	Two-phase pulse signal is applied
TAIOUT Pin Function	Two-phase pulse signal is applied
Read from Timer	The TAI register indicates counter value
Write to Timer	<ul style="list-style-type: none"> When the timer counter stops, the value written to the TAI register is also written to both reload register and counter While counting, the value written to the TAI register is written to the reload register (It is transferred to the counter at the next reload timing)
Selectable Function ⁽¹⁾	<ul style="list-style-type: none"> Normal processing operation (the timer A2 and timer A3) While a high-level ("H") signal is applied to the TAJOUT pin (j = 2 or 3), the timer increments a counter value on the rising edge of the TAJIN pin or decrements a counter value on the falling edge.  <ul style="list-style-type: none"> Multiply-by-4 processing operation (the timer A3 and timer A4) While an "H" signal is applied to the TAKOUT pin (k = 3 or 4) with the rising edge of the TAKIN pin, the timer counter increments a counter value on the rising and falling edges of the TAKOUT and TAKIN pins. While "H" is applied to the TAKOUT pin on the falling edge of the TAKIN pin, the timer decrements a counter value on the rising and falling edges of the TAKOUT and TAKIN pins. 

NOTES:

- Only timer A3 operation can be selected. The timer A2 is for the normal processing operation. The timer A4 is for the multiply-by-4 operation.

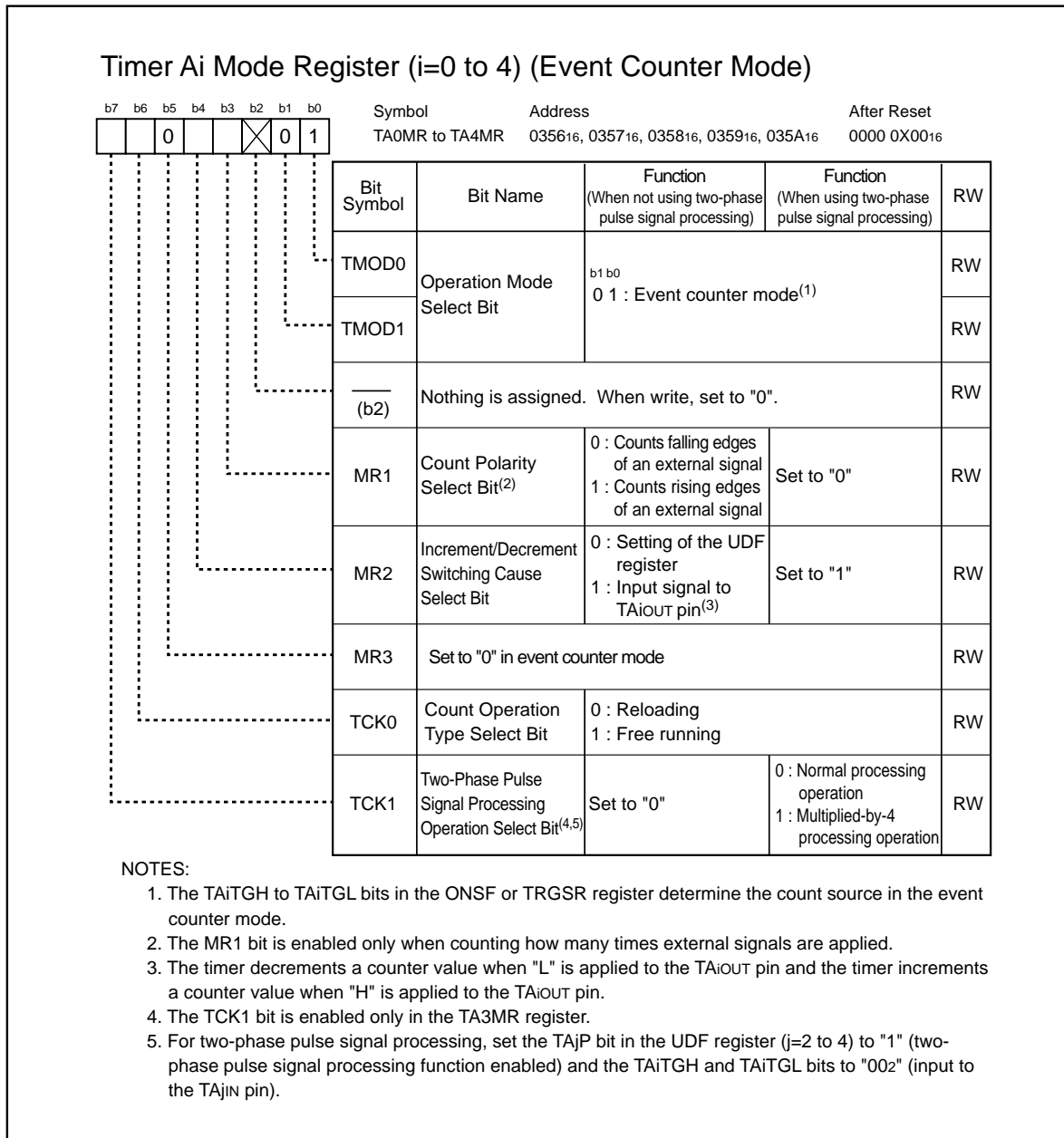


Figure 14.9 TA0MR to TA4MR Registers

14.1.2.1 Counter Reset by Two-Phase Pulse Signal Processing

The timer counter is reset to "0" by a Z-phase input when processing a two-phase pulse signal.

This function can be used in timer A3 event counter mode, two-phase pulse signal processing, free-run type or multiply-by-4 processing. The Z-phase signal is applied to the $\overline{\text{INT2}}$ pin.

When the TAZIE bit in the ONSF register is set to "1" (Z-phase input enabled), the timer counter can be reset by a Z-phase input. To reset the timer counter by a Z-phase input, set the TA3 register to "0000₁₆" beforehand.

Z-phase input is enabled when the edge of the signal applied to the $\overline{\text{INT2}}$ pin is detected. The POL bit in the INT2IC register can determine edge polarity. The Z-phase must have a pulse width of one timer A3 count source cycle or more. Figure 14.10 shows two-phase pulses (A-phase and B-phase) and the Z-phase.

Z-phase input resets the counter in the next count source following Z-phase input. Figure 14.11 shows the counter reset timing.

Timer A3 interrupt request is generated twice when a timer A3 overflow or underflow, and a counter reset by $\overline{\text{INT2}}$ input occur at the same time. Do not use the timer A3 interrupt request when this function is used.

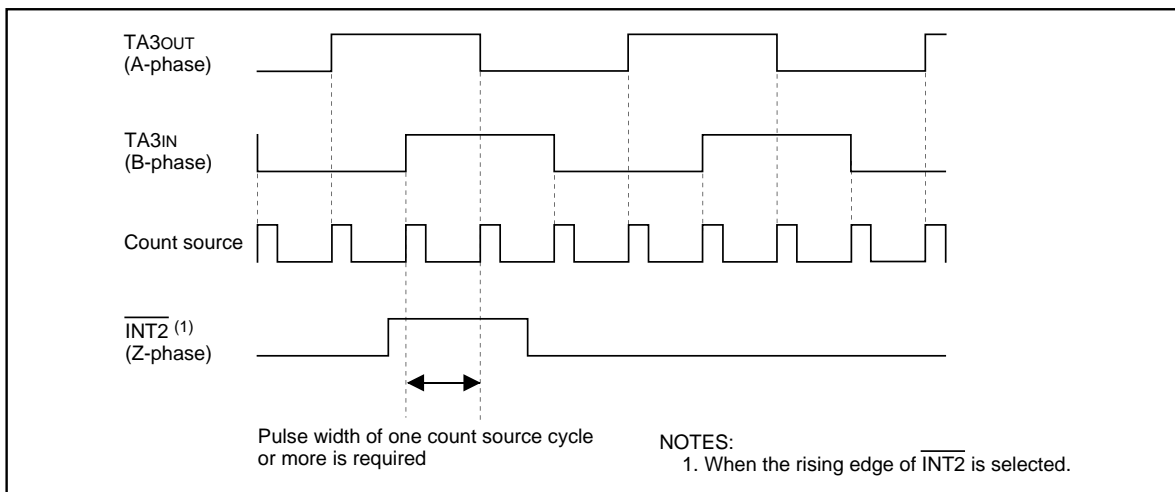


Figure 14.10 Two-phase Pulse (A-phase and B-phase) and Z-phase

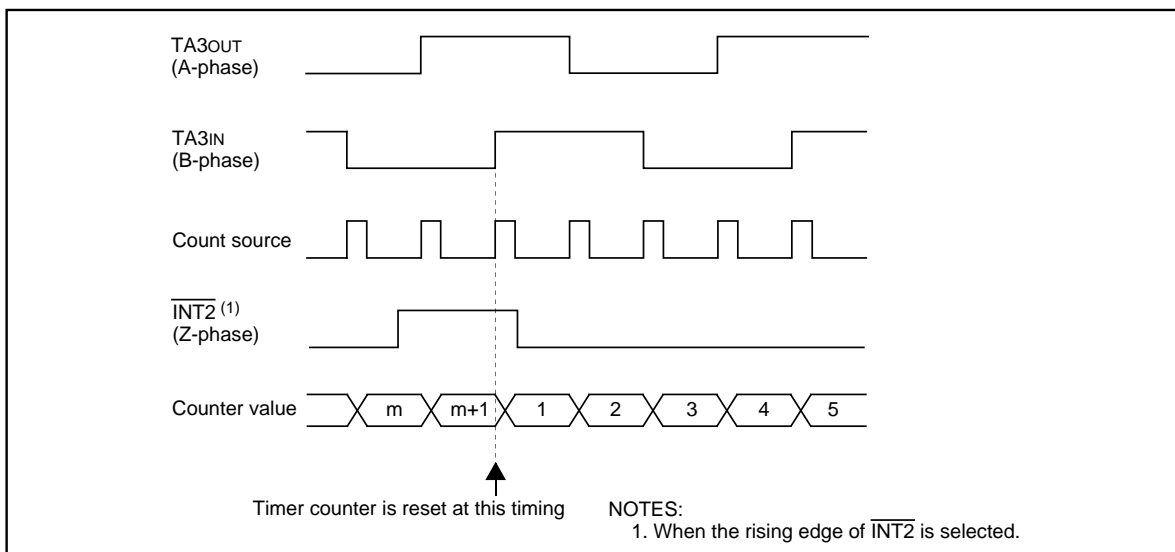


Figure 14.11 Counter Reset Timing

14.1.3 One-shot Timer Mode

In one-shot timer mode, the timer operates only once for each trigger (see **Table 14.6**). Once a trigger occurs, the timer starts and continues operating for a desired period. Figure 14.12 shows the TAI_{MR} register (i=0 to 4) in one-shot timer mode.

Table 14.6 Specifications in One-shot Timer Mode

Item	Specification
Count Source	f1, f8, f2 _n ⁽¹⁾ , fC32
Counting Operation	The timer decrements a counter value <ul style="list-style-type: none"> • When the timer counter reaches "0000₁₆", it stops counting after reloading. • If a trigger occurs while counting, content of the reload register is reloaded into the count register and counting resumes.
Divide Ratio	1/n n : setting value of the TAI register (i=0 to 4) 0000 ₁₆ to FFFF ₁₆ but the timer counter does not run if n=0000 ₁₆
Counter Start Condition	The TAI _S bit in the TABSR register is set to "1" (starts counting) and following triggers occur: <ul style="list-style-type: none"> • External trigger input • The timer overflow or underflow signal • The TAI_{OS} bit in the ONSF register is set to "1" (timer started)
Counter Stop Condition	<ul style="list-style-type: none"> • After the timer counter has reached "0000₁₆" and is reloaded • When the TAI_S bit is set to "0" (timer stopped)
Interrupt Request Generation Timing	The timer counter reaches "0000 ₁₆ "
TAI _{IN} Pin Function	Programmable I/O port or trigger input
TAI _{OUT} Pin Function	Programmable I/O port or pulse output
Read from Timer	The value in the TAI register is indeterminate when read
Write to Timer	<ul style="list-style-type: none"> • When the timer counter stops, the value written to the TAI register is also written to both reload register and counter • While counting, the value written to the TAI register is written to the reload register (It is transferred to the counter at the next reload timing)

NOTES:

1. The CNT3 to CNT0 bits in the TCSPR register select no division (n=0) or divide-by-2ⁿ (n=1 to 15).

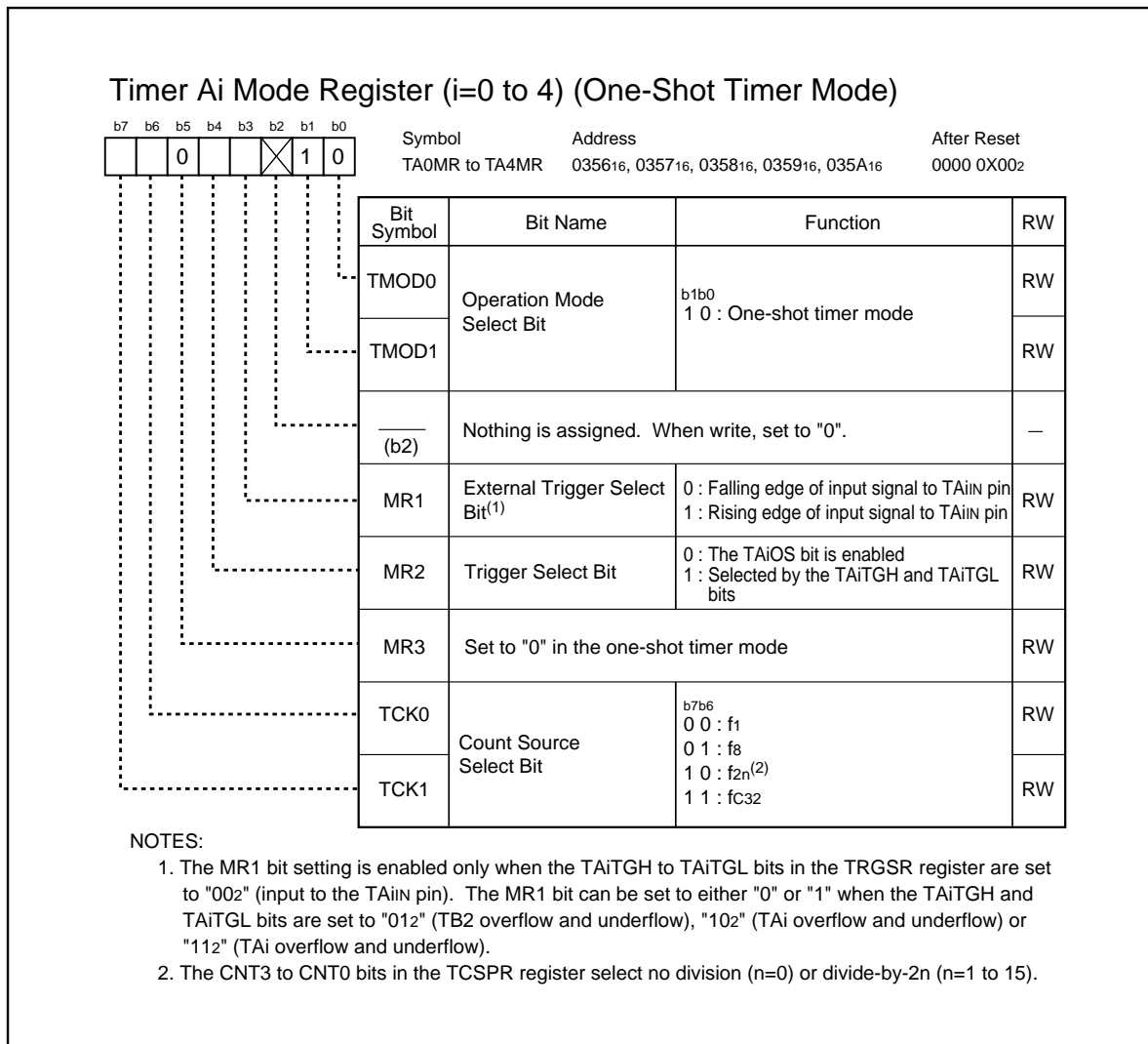


Figure 14.12 TA0MR to TA4MR Registers

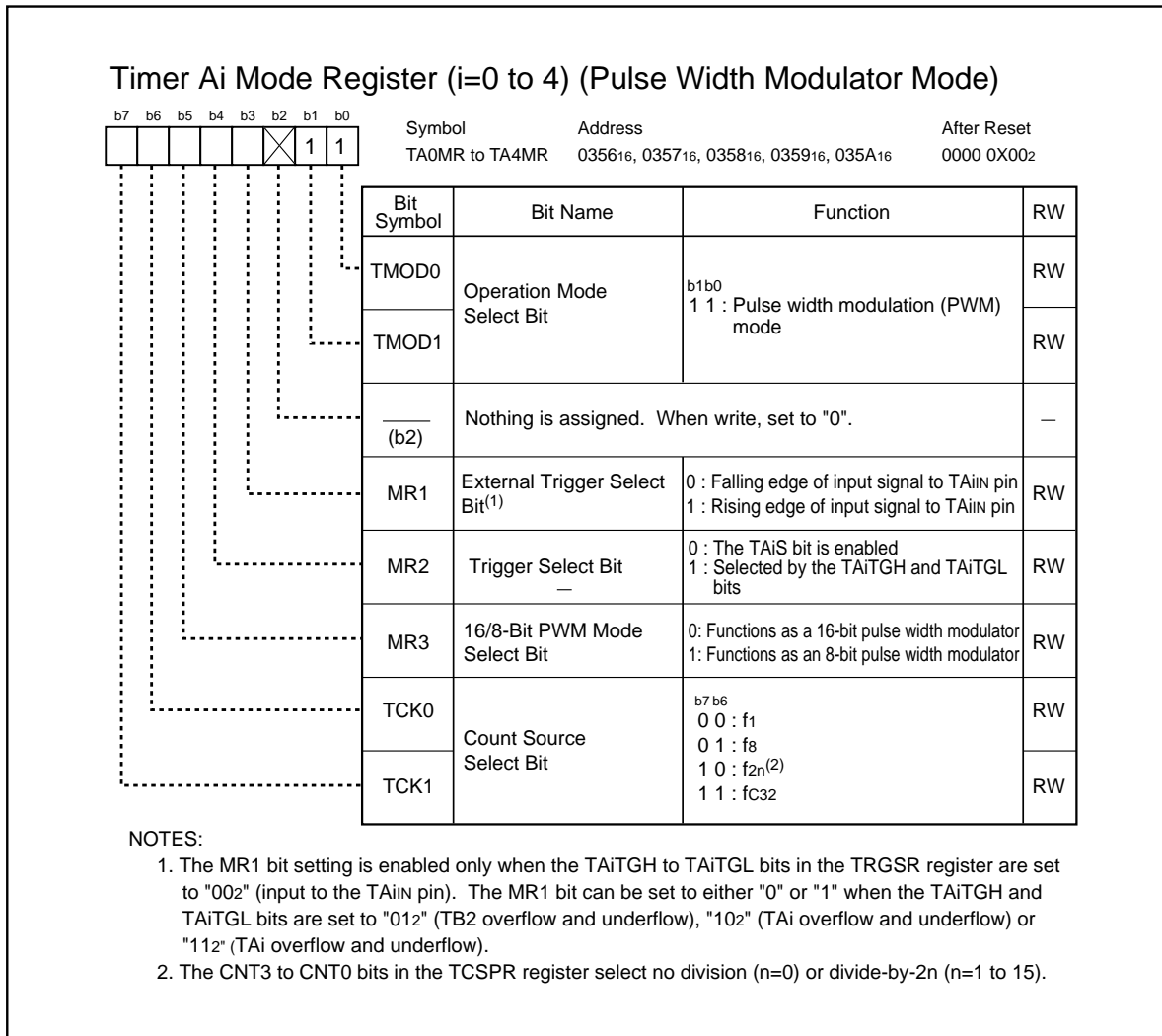


Figure 14.13 TA0MR to TA4MR Registers

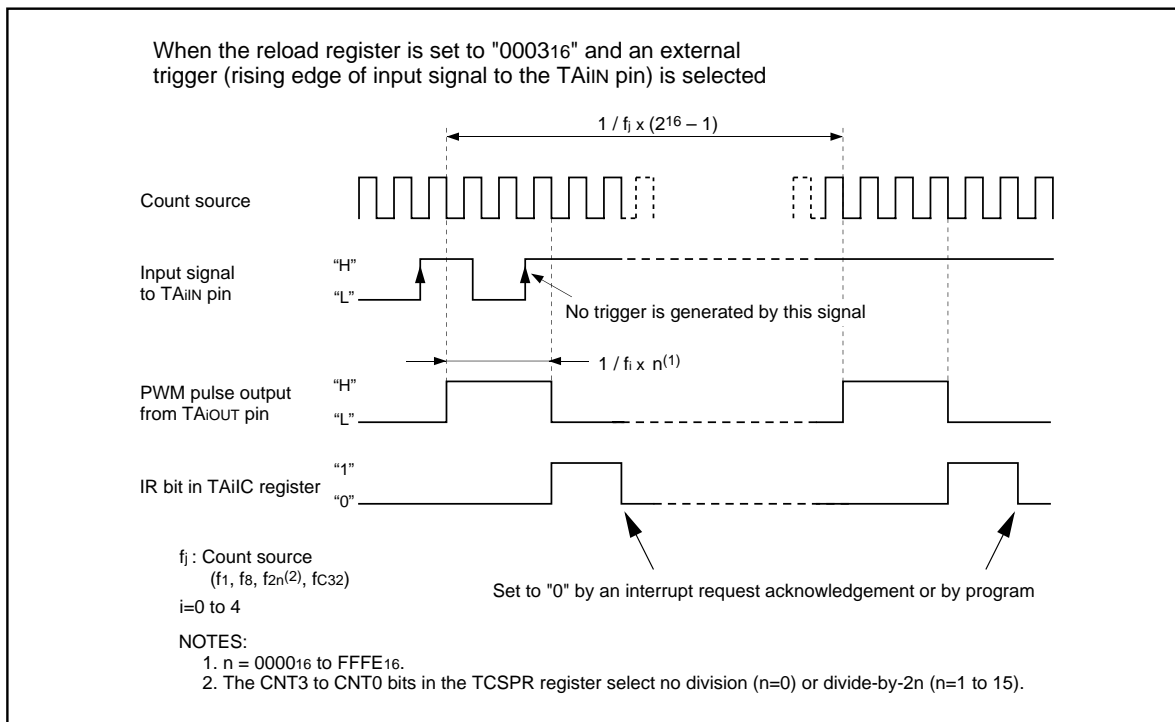


Figure 14.14 16-bit Pulse Width Modulator Operation

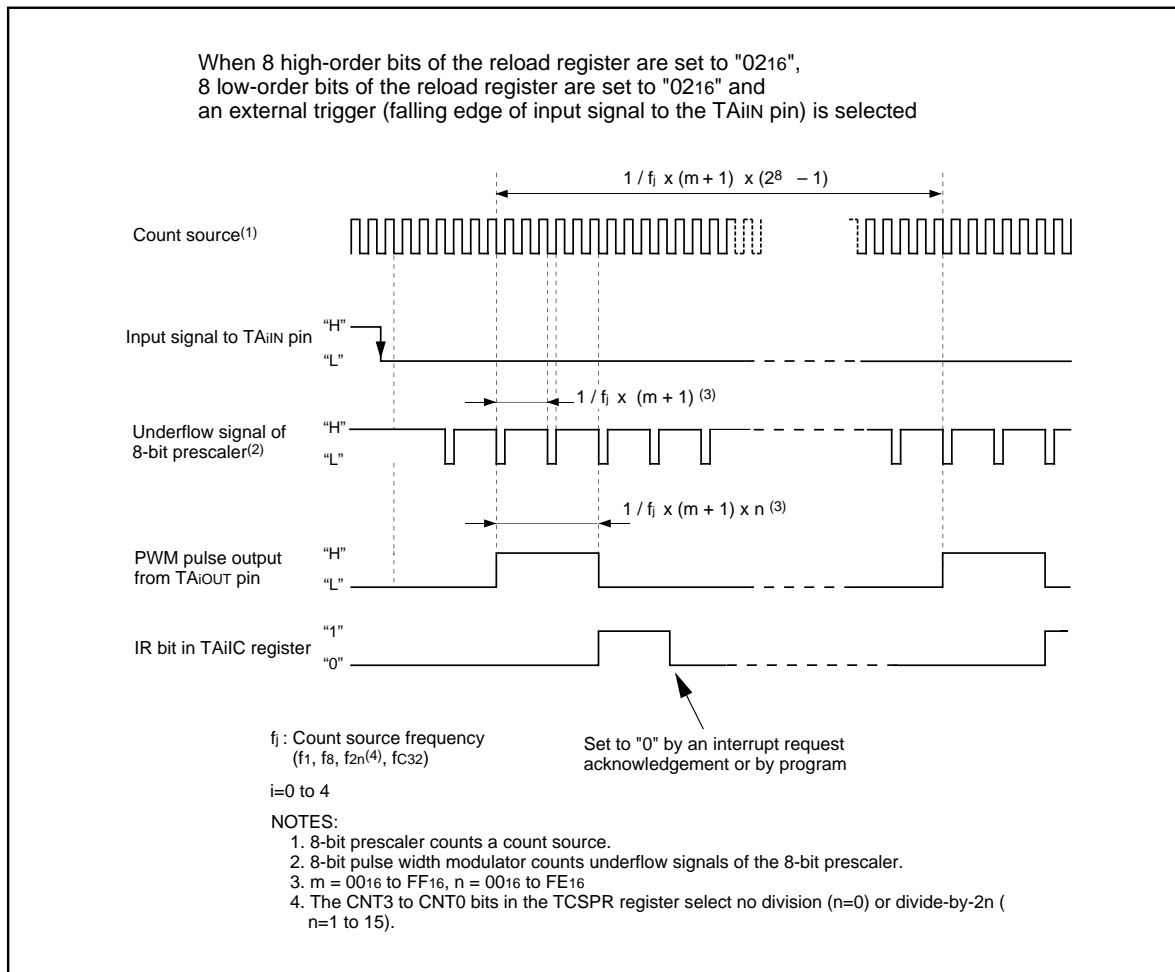


Figure 14.15 8-bit Pulse Width Modulator Operation

14.2 Timer B

Figure 14.16 shows a block diagram of the timer B. Figures 14.17 to 14.19 show registers associated with the timer B. The timer B supports the following three modes. The TMOD1 to TMOD0 bits in the TBiMR register (i=0 to 5) determine which mode is used.

- Timer mode : The timer counts an internal count source.
- Event counter mode : The timer counts pulses from an external source or overflow and underflow of another timer.
- Pulse period/pulse width measurement mode : The timer measures pulse period or pulse width of an external signal.

Table 14.18 lists TBiIN pin settings.

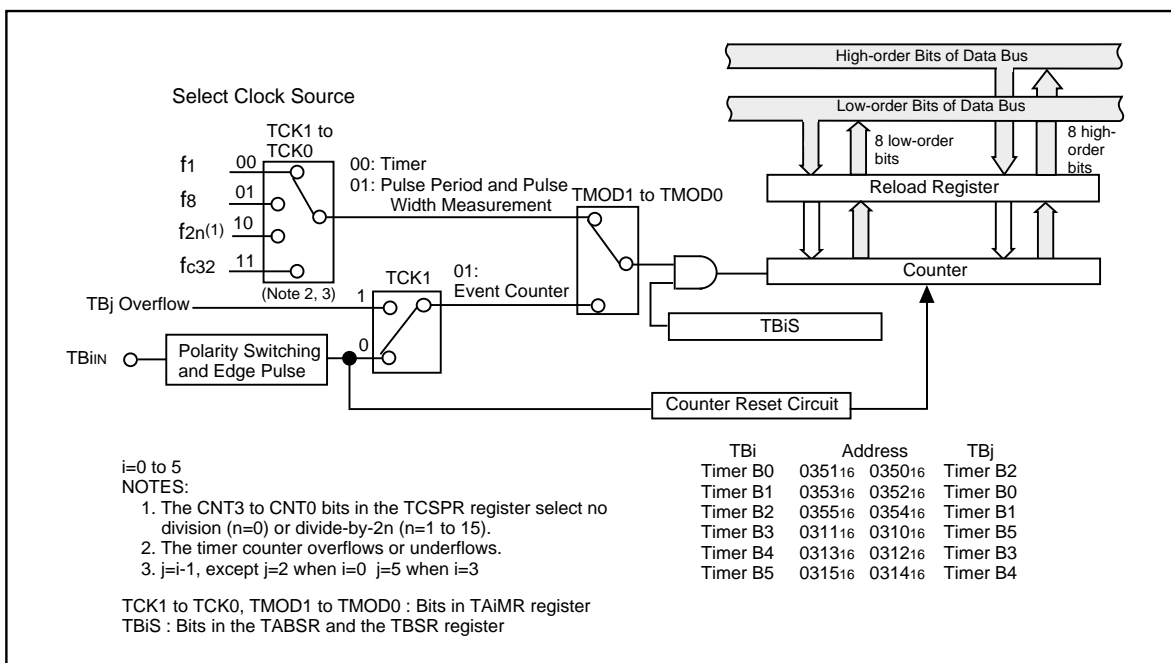


Figure 14.16 Timer B Block Diagram

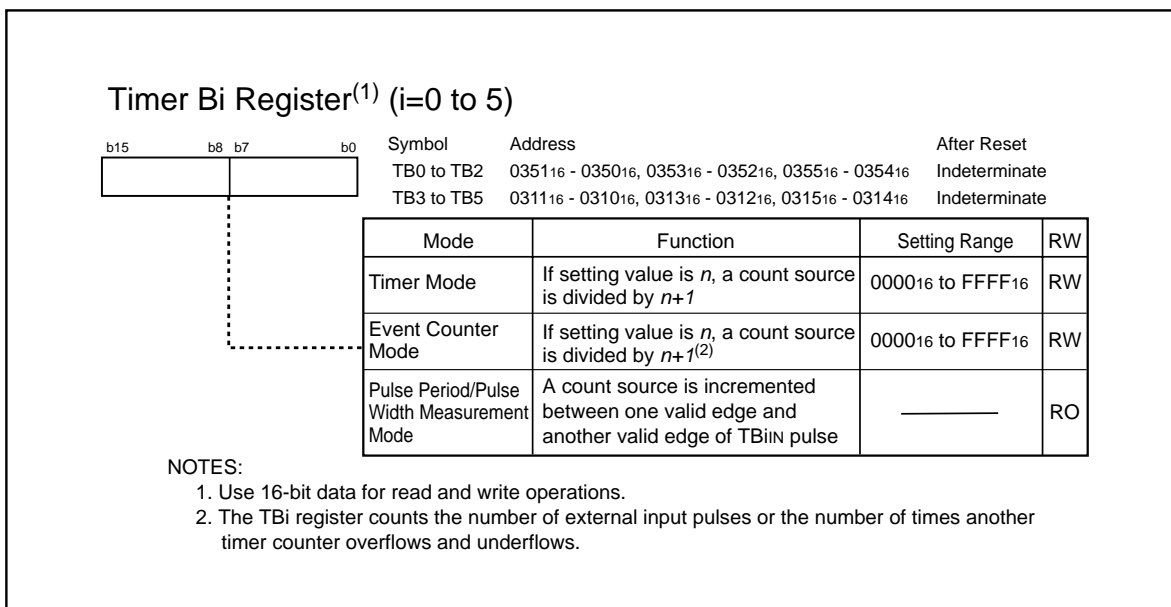


Figure 14.17 TB0 to TB5 Registers

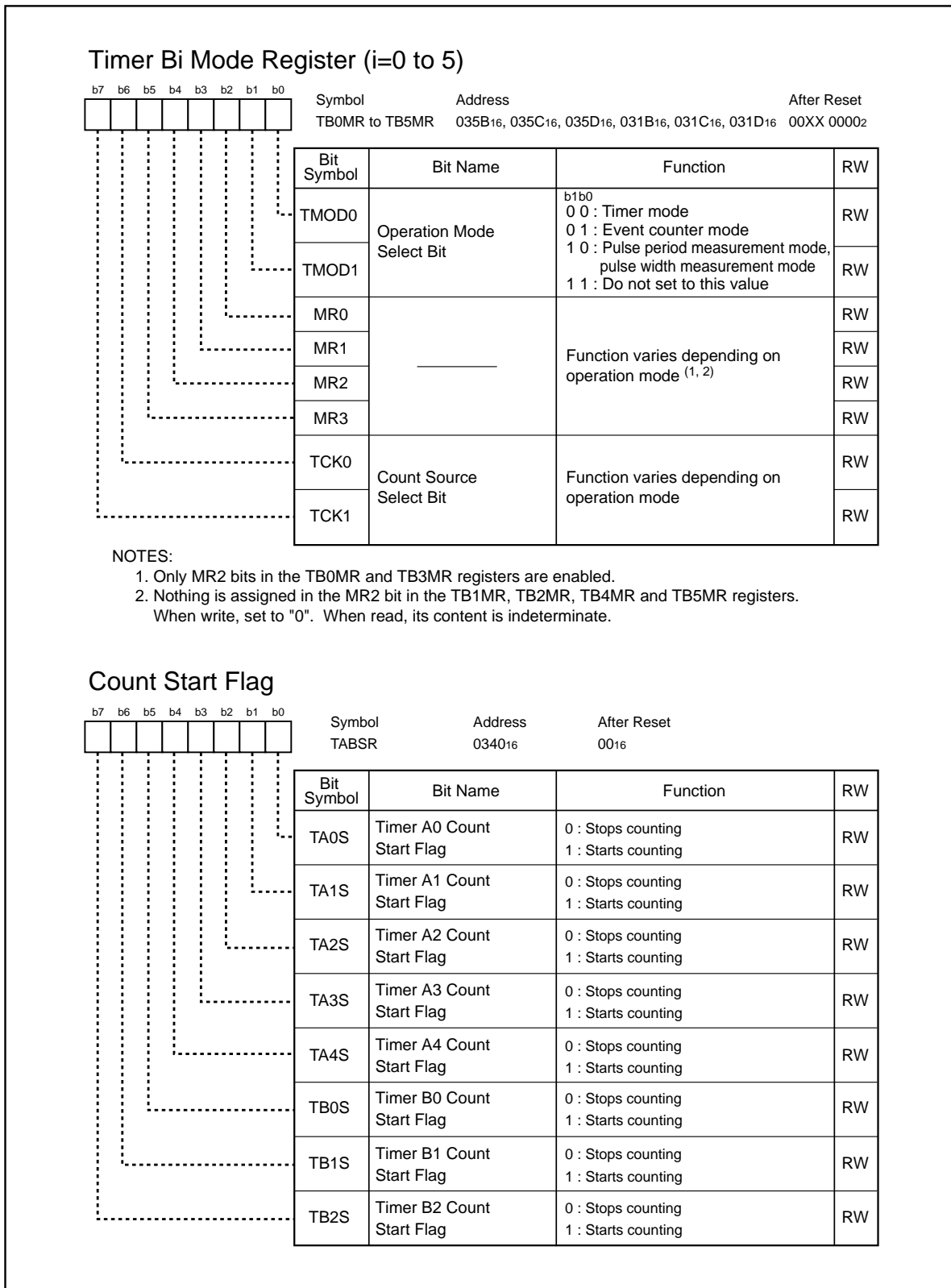


Figure 14.18 TB0MR to TB5MR Registers, TABSR Register

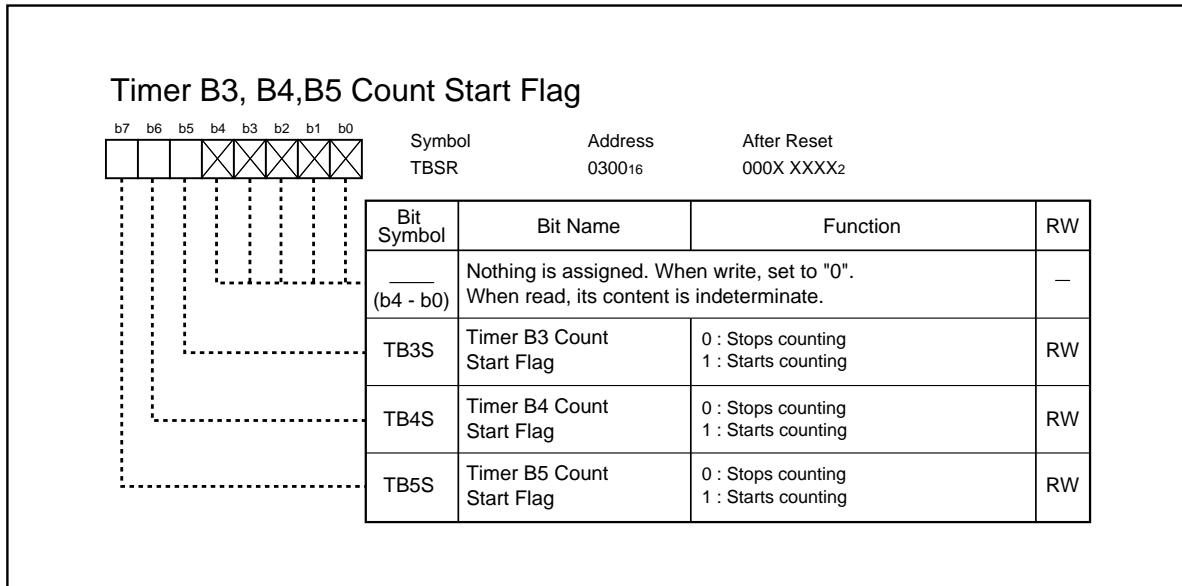


Figure 14.19 TBSR Register

Table 14.8 Settings for the TBiIN Pins (i=0 to 5)

Port Name	Function	Setting	
		PS1, PS3 ⁽¹⁾ Registers	PD7, PD9 ⁽¹⁾ Registers
P90	TB0IN	PS3_0=0	PD9_0=0
P91	TB1IN	PS3_1=0	PD9_1=0
P92	TB2IN	PS3_2=0	PD9_2=0
P93	TB3IN	PS3_3=0	PD9_3=0
P94	TB4IN	PS3_4=0	PD9_4=0
P71	TB5IN	PS1_1=0	PD7_1=0

NOTES:

- Set the PD9 and PS3 registers immediately after the PRC2 bit in the PRCR register is set to "1" (write enable). Do not generate an interrupt or a DMA transfer between the instruction to set the PRC2 bit to "1" and the instruction to set the PD9 and PS3 registers.

14.2.1 Timer Mode

In timer mode, the timer counts an internally generated count source (see Table 14.9). Figure 14.20 shows the TBiMR register (i=0 to 5) in timer mode.

Table 14.9 Specifications in Timer Mode

Item	Specification
Count Source	f1, f8, f2n ⁽¹⁾ , fC32
Counting Operation	The timer decrements a counter value <ul style="list-style-type: none"> When the timer counter underflows, content of the reload register is reloaded into the count register and counting resumes
Divide Ratio	1/(n+1) n: setting value of the TBi register (i=0 to 5) 0000 ₁₆ to FFFF ₁₆
Counter Start Condition	The TBiS bits in the TABSR or TBSR registers are set to "1" (starts counting)
Counter Stop Condition	The TBiS bit is set to "0" (stops counting)
Interrupt Request Generation Timing	The timer counter underflows
TBiIn Pin Function	Programmable I/O port
Read from Timer	The TBi register indicates counter value
Write to Timer	<ul style="list-style-type: none"> When the timer counter stops, the value written to the TBi register is also written to both reload register and counter While counting, the value written to the TBi register is written to the reload register (It is transferred to the counter at the next reload timing)

NOTES:

- The CNT3 to CNT0 bits in the TCSPR register select no division (n=0) or divide-by-2n (n=1 to 15).

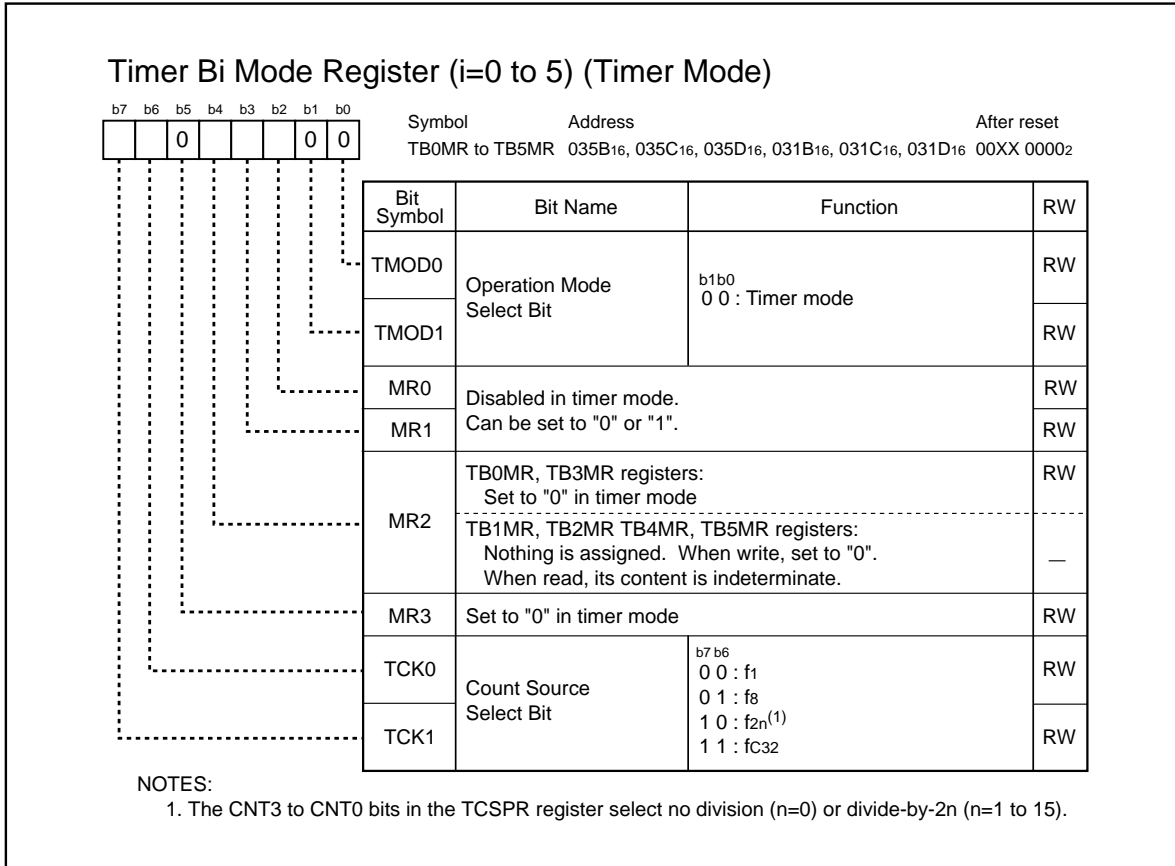


Figure 14.20 TB0MR to TB5MR Registers

14.2.2 Event Counter Mode

In event counter mode, the timer counts how many external signals are applied or how many times another timer overflows and underflows. (See Table 14.10) Figure 14.21 shows the TBiMR register (i=0 to 5) in event counter mode.

Table 14.10 Specifications in Event Counter Mode

Item	Specification
Count Source	<ul style="list-style-type: none"> External signal applied to the TBiIN pin (i = 0 to 5) (valid edge can be selected by program) TBj overflows or underflows (j=i-1, except j=2 when i=0, j=5 when i=3)
Counting Operation	<ul style="list-style-type: none"> The timer decrements a counter value <p>When the timer counter underflows, content of the reload register is reloaded into the count register to continue counting</p>
Divide Ratio	$1/(n+1)$ n : setting value of the TBi register 0000 ₁₆ to FFFF ₁₆
Counter Start Condition	The TBiS bit in the TABSR or TBSR register is set to "1" (starts counting)
Counter Stop Condition	The TBiS bit is set to "0" (stops counting)
Interrupt Request Generation Timing	The timer counter underflows
TBiIN Pin Function	Programmable I/O port or count source input
Read from Timer	The TBi register indicates the value of the counter
Write to Timer	<ul style="list-style-type: none"> When the timer counter stops, the value written to the TBi register is also written to both reload register and counter While counting, the value written to the TBi register is written to the reload register (It is transferred to the counter at the next reload timing)

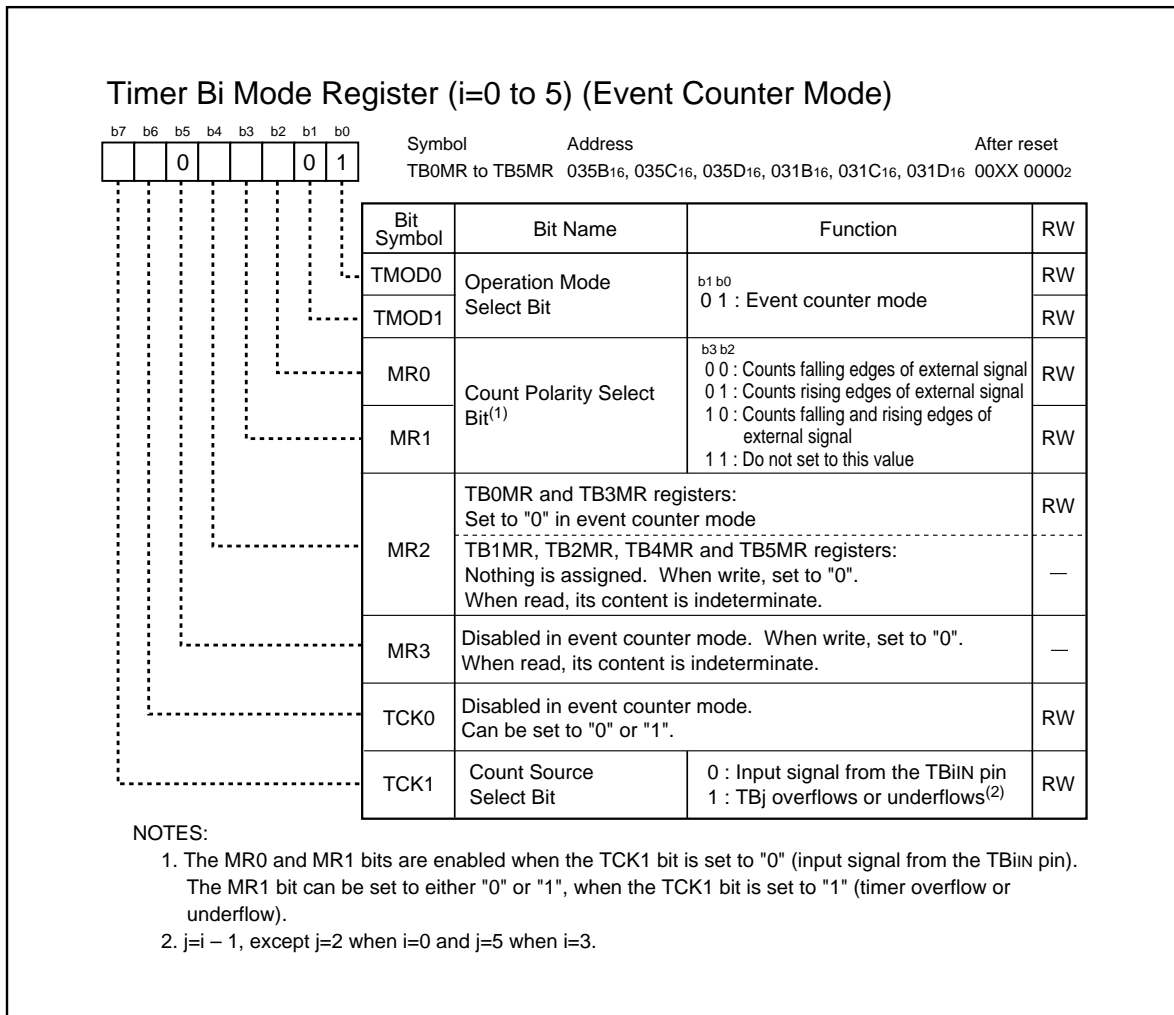


Figure 14.21 TB0MR to TB5MR Registers

14.2.3 Pulse Period/Pulse Width Measurement Mode

In pulse period/pulse width measurement mode, the timer measures pulse period or pulse width of an external signal. (See Table 14.11) Figure 14.22 shows the TBiMR register (i=0 to 5) in pulse period/pulse width measurement mode. Figure 14.23 shows an example of an operation timing when measuring a pulse period. Figure 14.24 shows an example of the pulse width measurement.

Table 14.11 Specifications in Pulse Period/Pulse Width Measurement Mode

Item	Specification
Count Source	f1, f8, f2n ⁽³⁾ , fc32
Counting Operation	<ul style="list-style-type: none"> The timer increments a counter value Counter value is transferred to the reload register on the valid edge of a pulse to be measured. It is set to "000016" and the timer continues counting
Counter Start Condition	The TBiS bit (i=0 to 5) in the TABSR or TBSR register is set to "1" (starts counting)
Counter Stop Condition	The TBiS bit is set to "0" (stops counting)
Interrupt Request Generation Timing	<ul style="list-style-type: none"> On the valid edge of a pulse to be measured⁽¹⁾ The timer counter overflows The MR3 bit in the TBiMR register is set to "1" (overflow) simultaneously. When the TBiS bit is set to "1" (start counting) and the next count source is counted after setting the MR3 bit to "1" (overflow), the MR3 bit can be set to "0" (no overflow) by writing to the TBiMR register.
TBiIn Pin Function	Input for a pulse to be measured
Read from Timer	The TBi register indicates reload register values (measurement results) ⁽²⁾
Write to Timer	Value written to the TBi register can be written to neither reload register nor counter

NOTES:

- No interrupt request is generated when the pulse to be measured is on the first valid edge after the timer has started counting.
- The TBi register is in an indeterminate state until the pulse to be measured is on the second valid edge after the timer has started counting.
- The CNT3 to CNT0 bits in the TCSPR register select no division (n=0) or divide-by-2n (n=1 to 15).

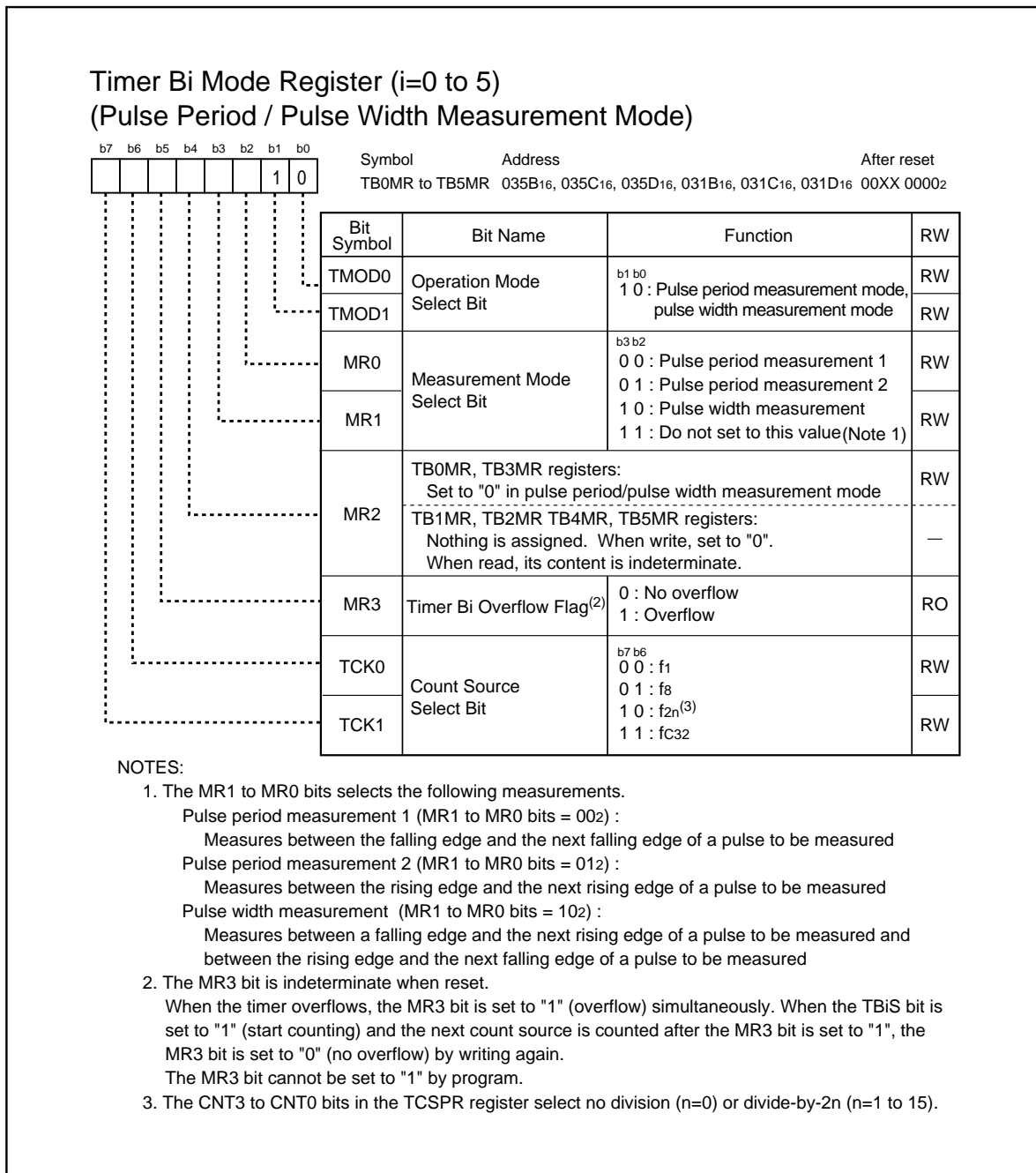


Figure 14.22 TB0MR to TB5MR Registers

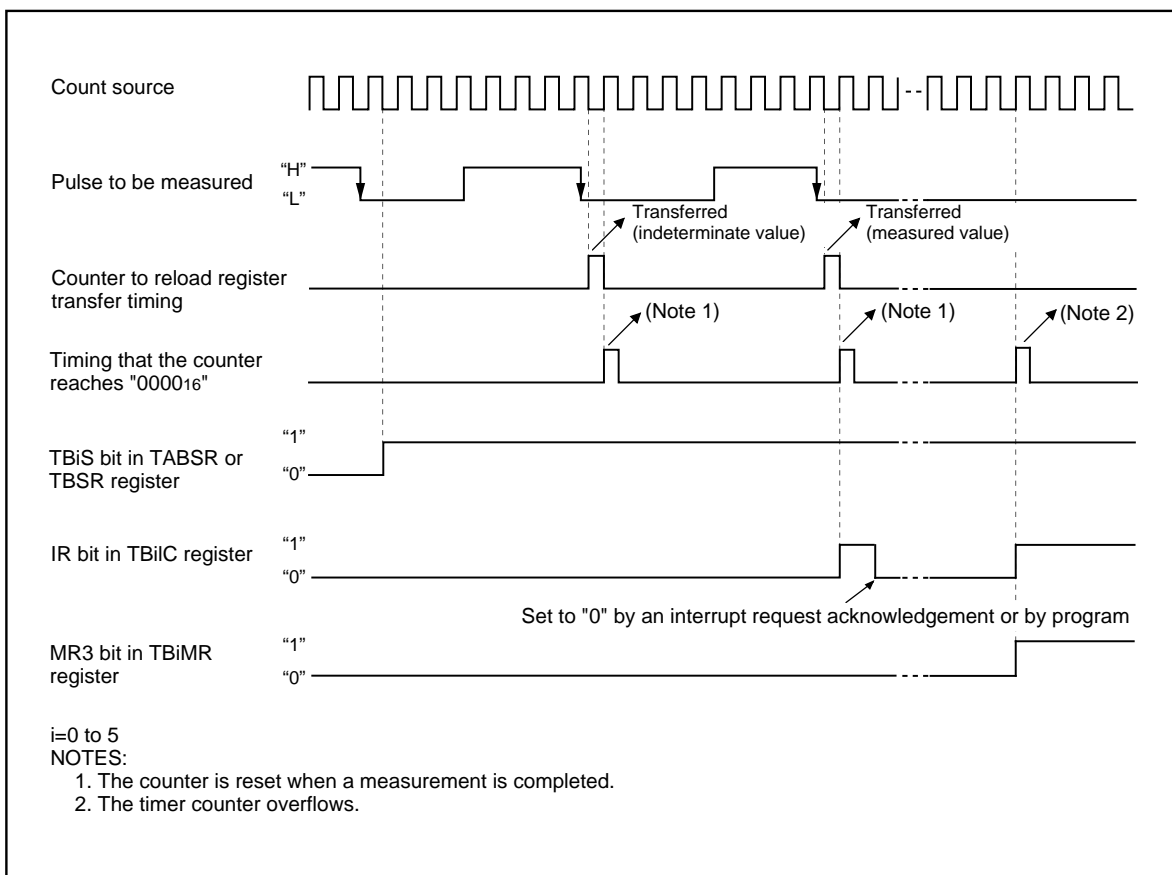


Figure 14.23 Pulse Period 1 Measurement

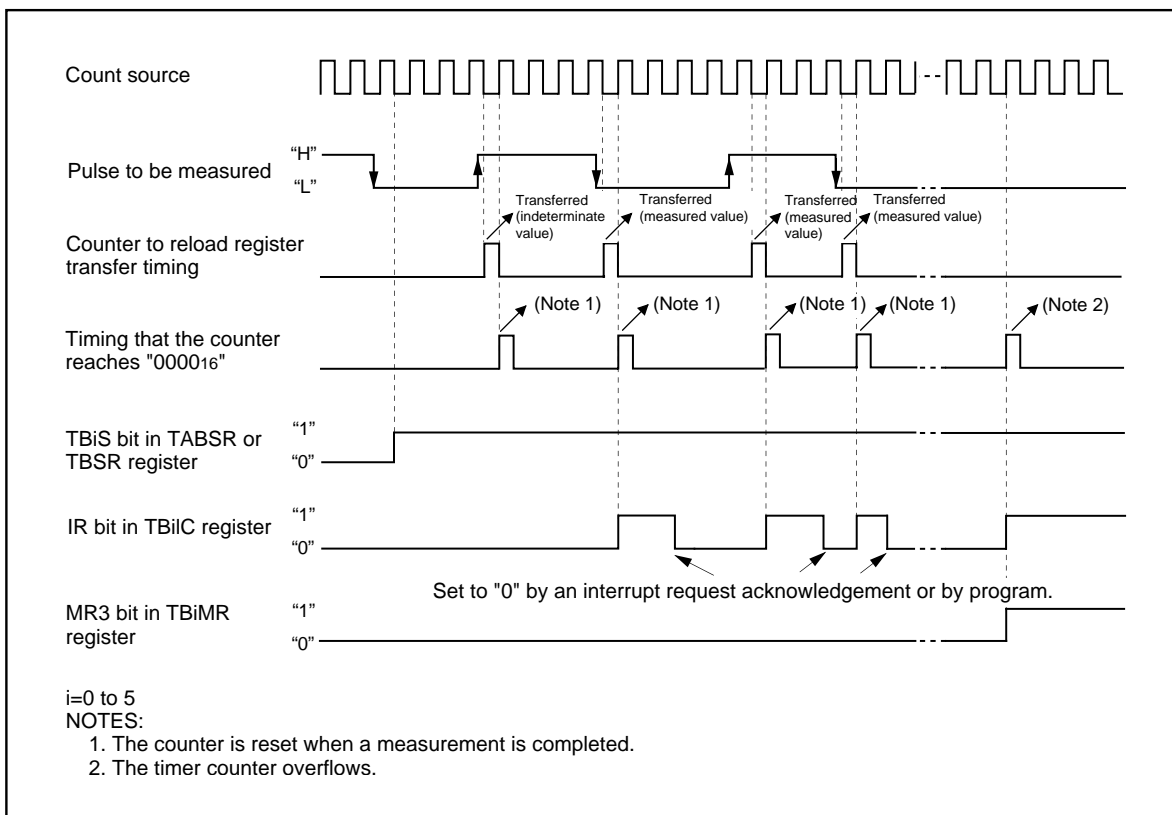


Figure 14.24 Pulse Width Measurement

15. Three-Phase Motor Control Timer Functions

Three-phase motor driving waveform can be output by using the timers A1, A2, A4 and B2. Table 15.1 lists specifications of the three-phase motor control timer functions. Table 15.2 lists pin settings. Figure 15.1 shows a block diagram. Figures 15.2 to 15.7 show registers associated with the three-phase control timer functions.

Table 15.1 Three-Phase Motor Control Timer Functions Specification

Item	Specification
Three-Phase Waveform Output Pin	Six pins (U, \bar{U} , V, \bar{V} , W, \bar{W})
Forced Cutoff ⁽¹⁾	Apply a low-level signal ("L") to the $\overline{\text{NMI}}$ pin
Timers to be Used	Timer A4, A1, A2 (used in one-shot timer mode) Timer A4: U- and \bar{U} -phase waveform control Timer A1: V- and \bar{V} -phase waveform control Timer A2: W- and \bar{W} -phase waveform control Timer B2 (used in timer mode) Carrier wave cycle control Dead time timer (three 8-bit timers share reload register) Dead time control
Output Waveform	Triangular wave modulation, Sawtooth wave modification Can output a high-level waveform or a low-level waveform for one cycle Can set positive-phase level and negative-phase level separately
Carrier Wave Cycle	Triangular wave modulation: $count\ source \times (m+1) \times 2$ Sawtooth wave modulation: $count\ source \times (m+1)$ m: setting value of the TB2 register, 0000 ₁₆ to FFFF ₁₆ Count source: f ₁ , f ₈ , f _{2n} ⁽²⁾ , f _{c32}
Three-Phase PWM Output Width	Triangular wave modulation: $count\ source \times n \times 2$ Sawtooth wave modulation: $count\ source \times n$ n: setting value of the TA4, TA1 and TA2 register (of the TA4, TA41, TA1, TA11, TA2 and TA21 registers when setting the INV11 bit to "1"), 0001 ₁₆ to FFFF ₁₆ Count source: f ₁ , f ₈ , f _{2n} ⁽²⁾ , f _{c32}
Dead Time	$Count\ source \times p$, or no dead time p: setting value of the DTT register, 01 ₁₆ to FF ₁₆ Count source: f ₁ , or f ₁ divided by 2
Active Level	Selected from a high level ("H") or low level ("L")
Positive and Negative-Phase Concurrent Active Disable Function	Positive and negative-phases concurrent active disable function Positive and negative-phases concurrent active detect function
Interrupt Frequency	For the timer B2 interrupt, one carrier wave cycle-to-cycle basis through 15 time- carrier wave cycle-to-cycle basis can be selected

NOTES:

1. Forced cutoff by the signal applied to the $\overline{\text{NMI}}$ pin is available when the INV02 bit is set to "1" (three-phase motor control timer functions) and the INV03 bit is set to "1" (three-phase motor control timer output enabled).
2. The CNT3 to CNT0 bits in the TCSPR register select no division (n=0) or divide-by-2n (n=1 to 15).

Table 15.2 Pin Settings

Pin	Setting		
	PS1, PS2 Registers ⁽¹⁾	PSL1, PSL2 Registers	PSC Register
P72/V	PS1_2 =1	PSL1_2 =0	PSC_2 =1
P73/ \bar{V}	PS1_3 =1	PSL1_3 =1	PSC_3 =0
P74/W	PS1_4 =1	PSL1_4 =1	PSC_4 =0
P75/ \bar{W}	PS1_5 =1	PSL1_5 =0	—
P80/U	PS2_0 =1	PSL2_0 =1	—
P81/ \bar{U}	PS2_1 =1	PSL2_1 =0	—

NOTES:

1. Set the PS1_2 to PS1_5 and PS2_0 to PS2_1 bits in the PS1 and PS2 registers to "1" after the INV02 bit is set to "1".

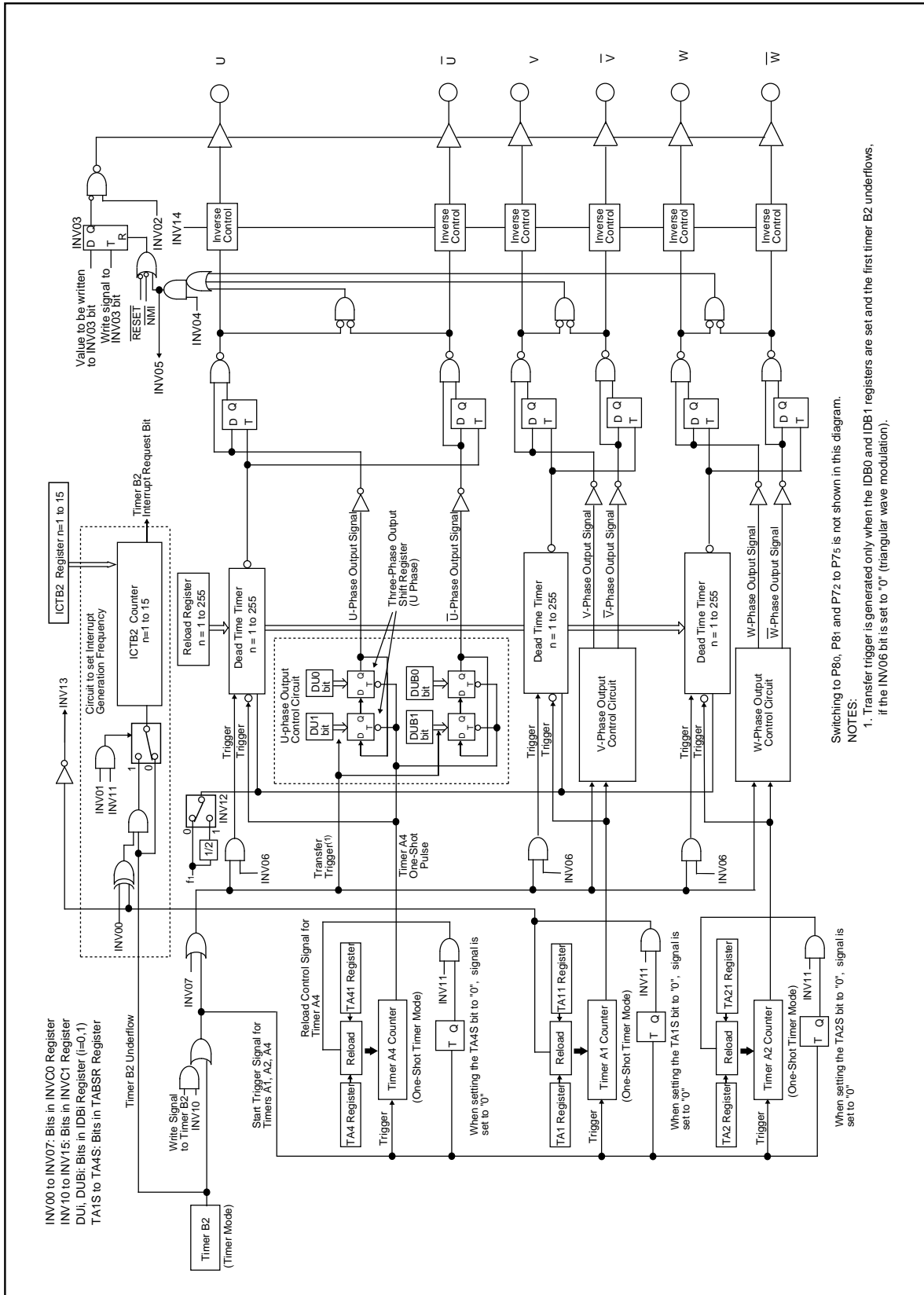


Figure 15.1 Three-Phase Motor Control Timer Functions Block Diagram

Switching to P80, P81, and P72 to P75 is not shown in this diagram.
 NOTES:
 1. Transfer trigger is generated only when the IDB0 and IDB1 registers are set and the first timer B2 underflows, if the INV06 bit is set to '0' (triangular wave modulation).

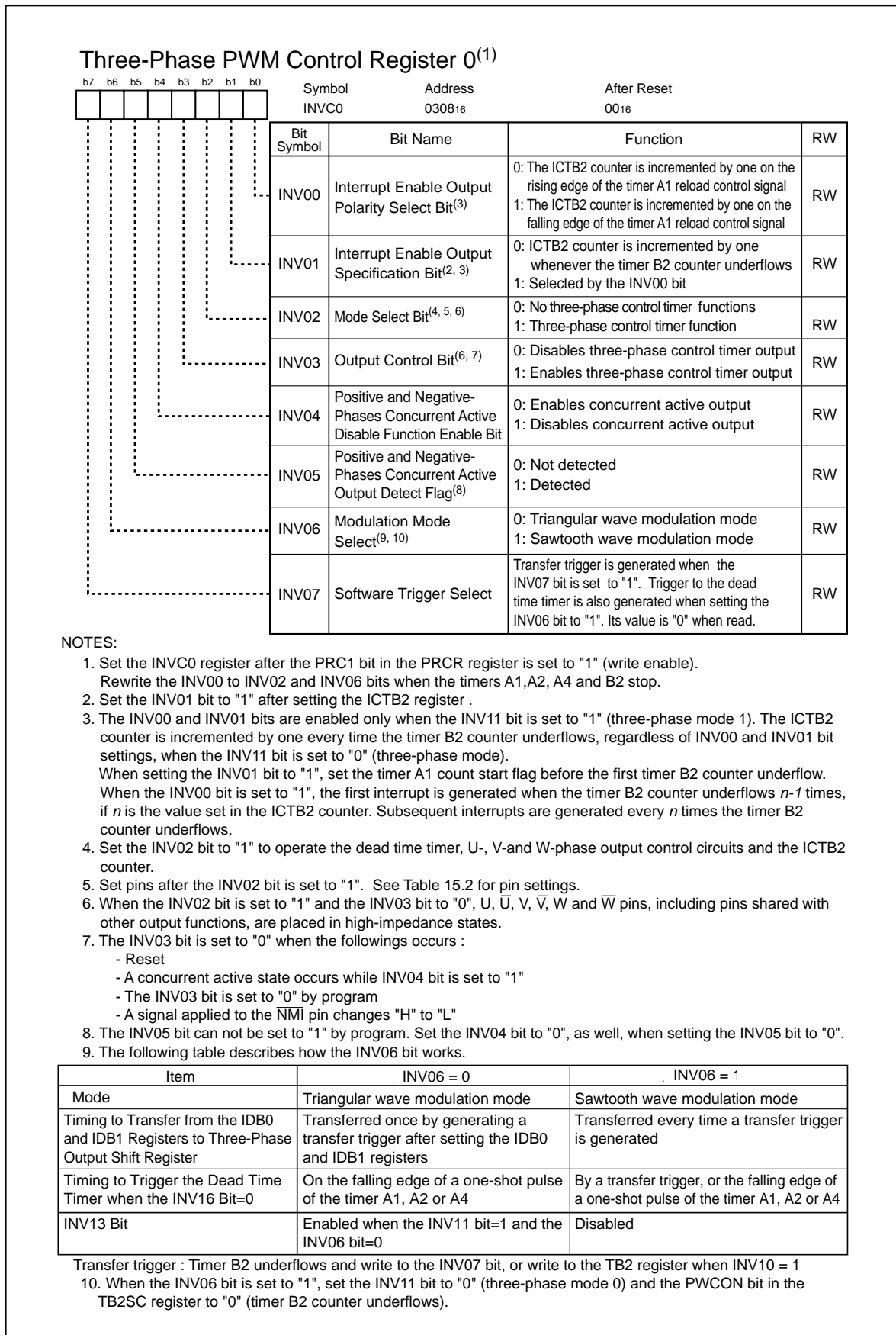


Figure 15.2 INVC0 Register

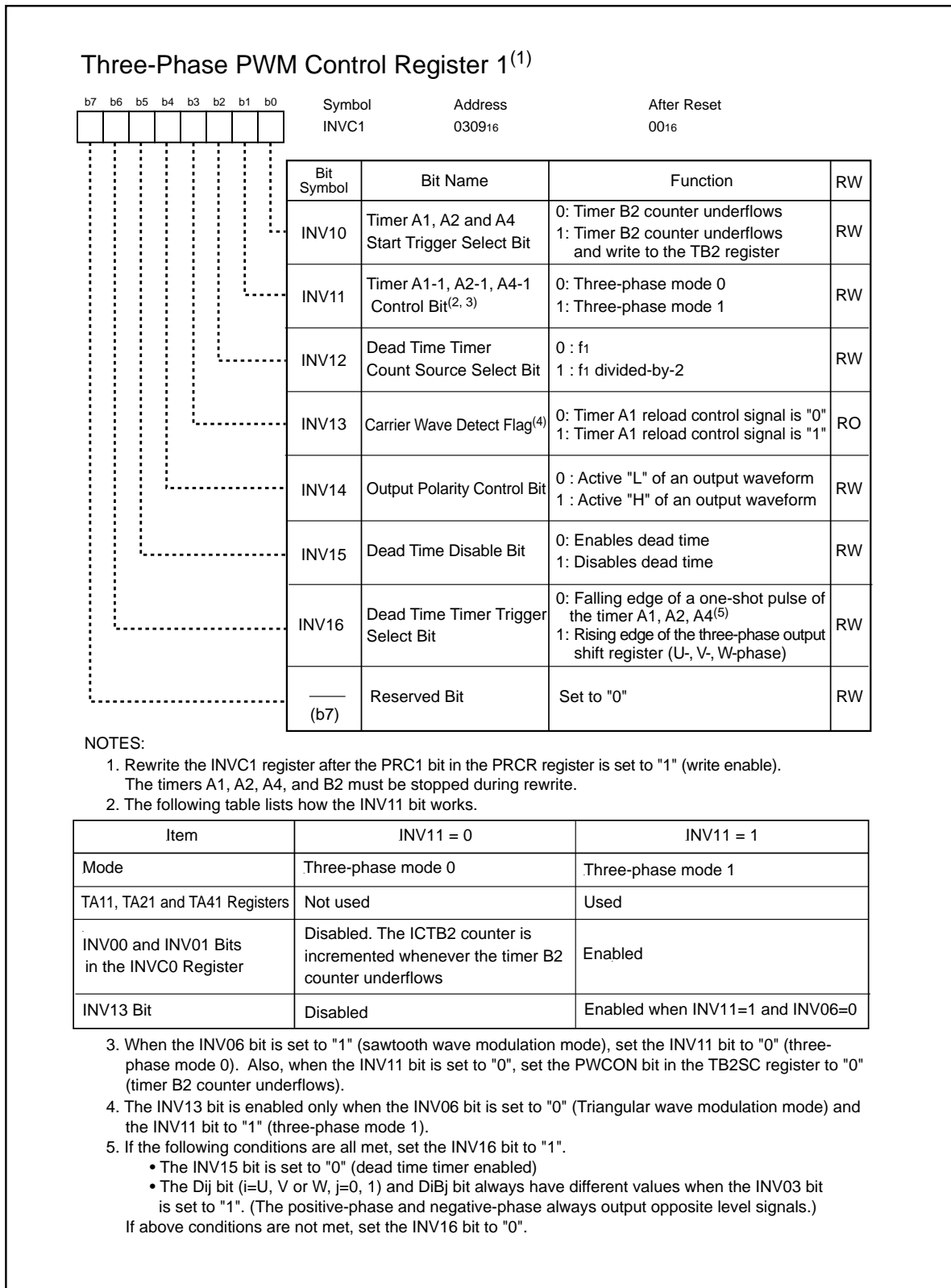


Figure 15.3 INVC1 Register

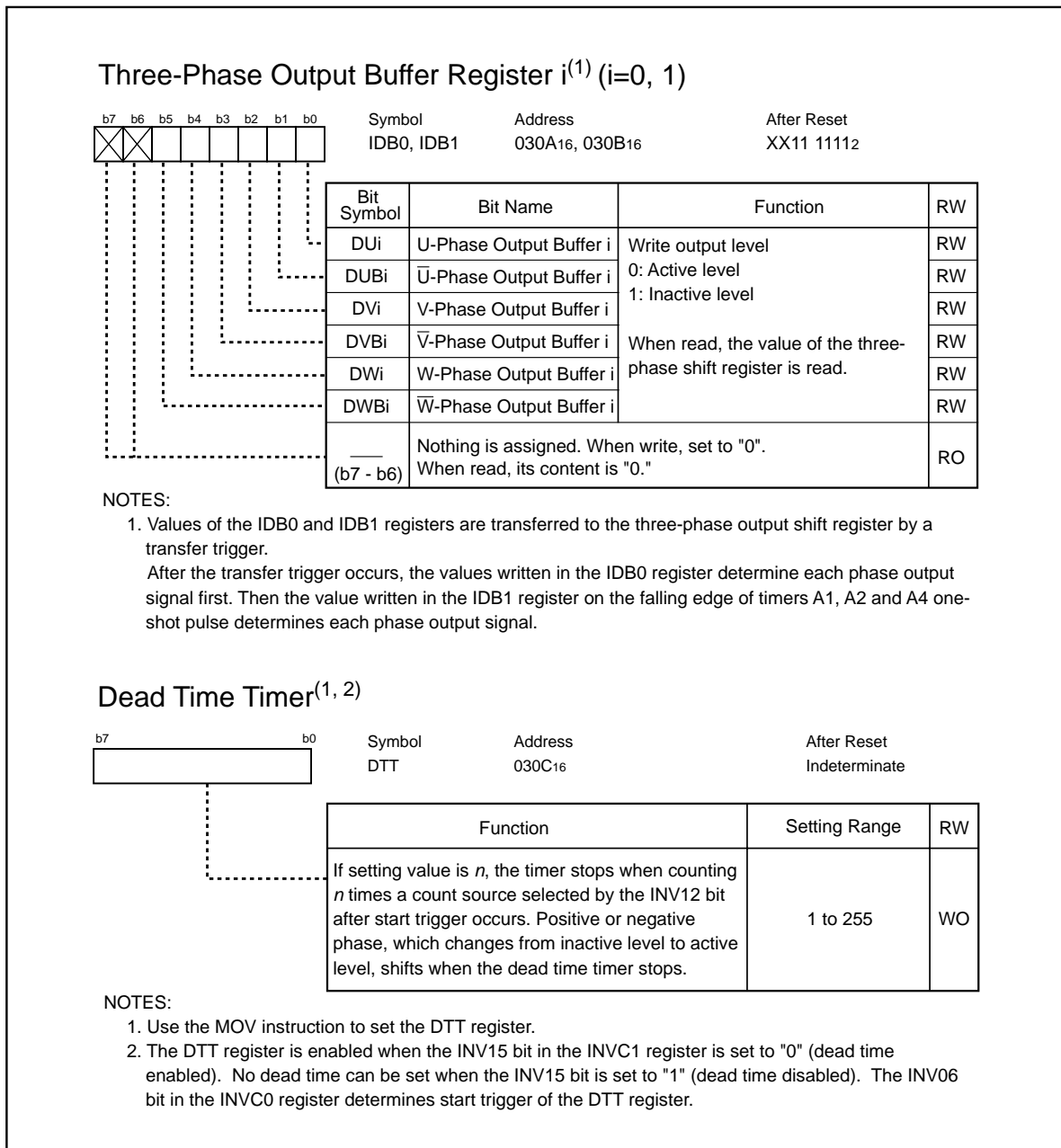


Figure 15.4 IDB0, IDB1 and DTT Registers

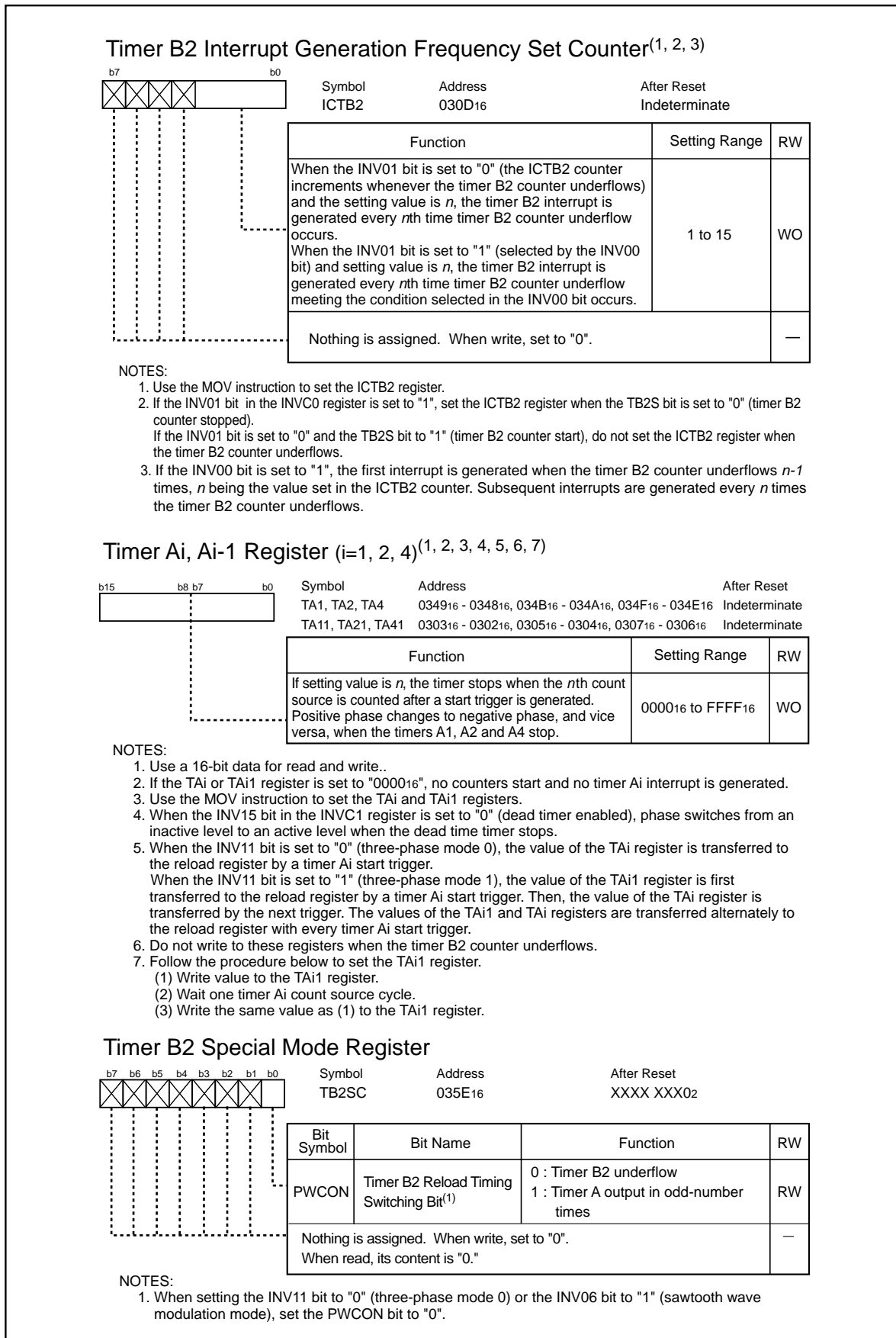


Figure 15.5 ICTB2 Register, TA1, TA2, TA4, TA11, TA21 and TA41 Registers and TB2SC Register

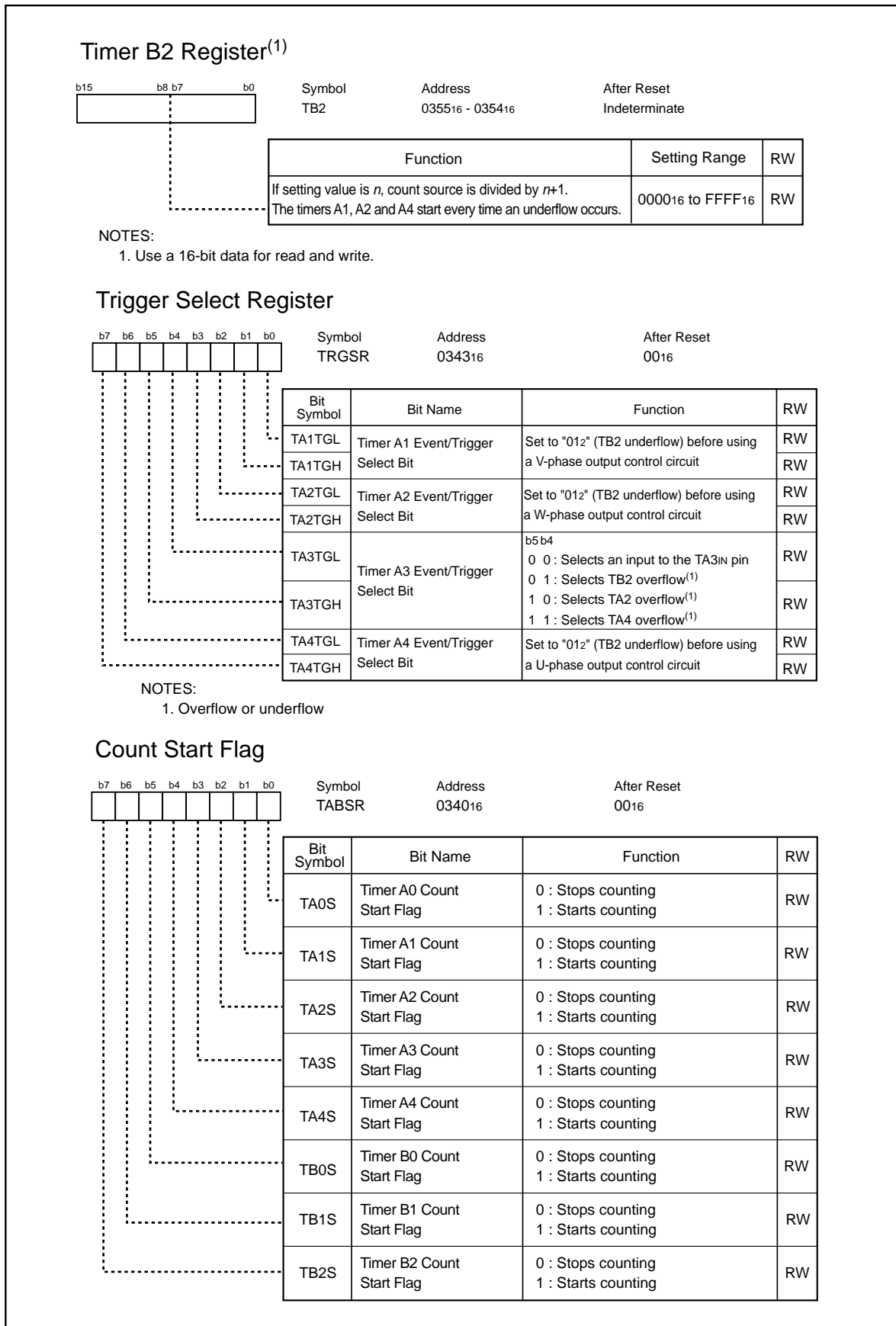


Figure 15.6 TB2, TRGSR and TABSR Registers

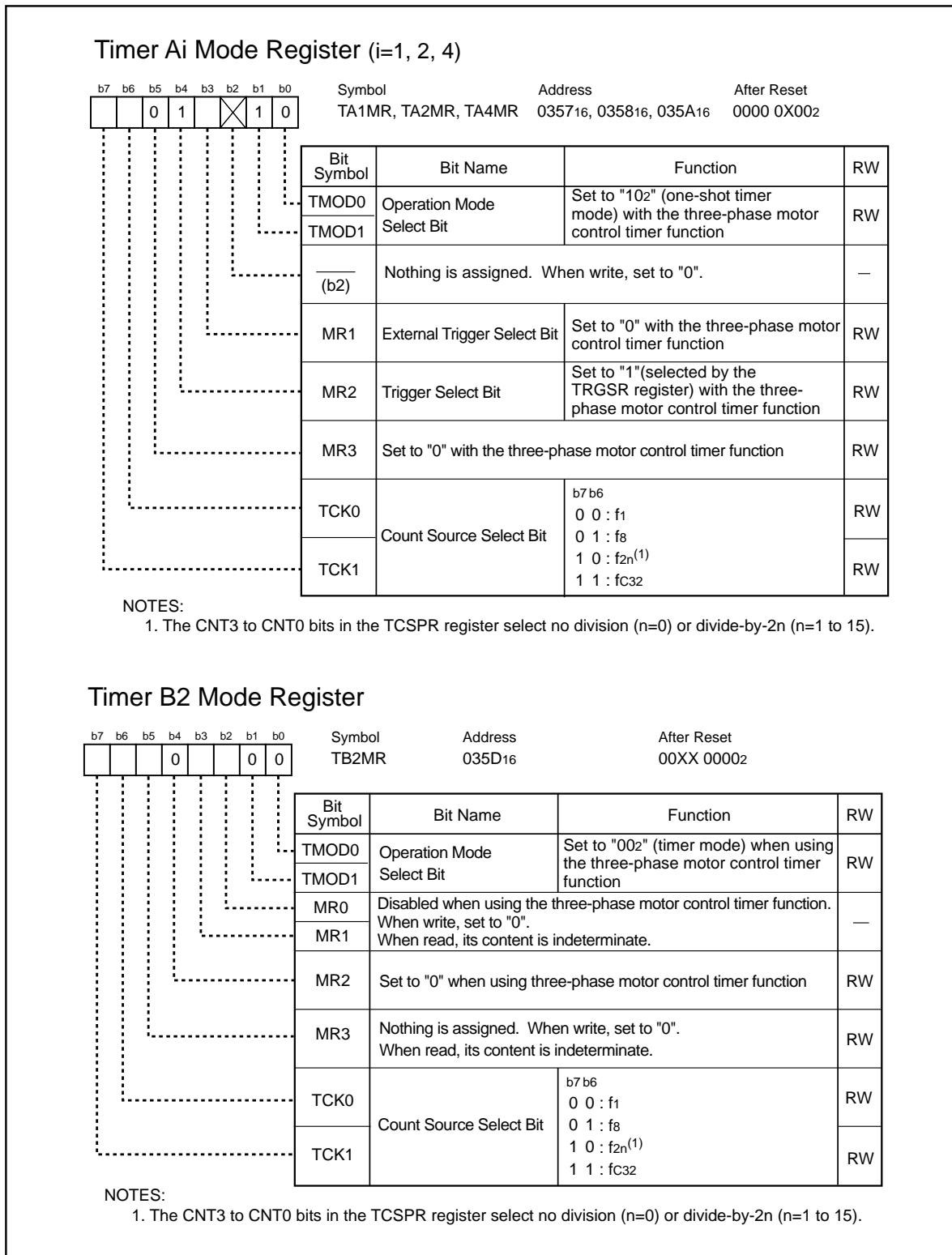


Figure 15.7 TA1MR, TA2MR, TA4MR Registers and TB2MR Register

The three-phase control timer function is available by setting the INV02 bit in the INVC0 register to "1". The timer B2 is used for carrier wave control and timers A4, A1, A2 for three-phase PWM output (U, \bar{U} , V, \bar{V} , W, \bar{W}) control. An exclusive dead time timer controls dead time. Figure 15.8 shows an example of the triangular modulation waveform. Figure 15.9 shows an example of the sawtooth modulation waveform.

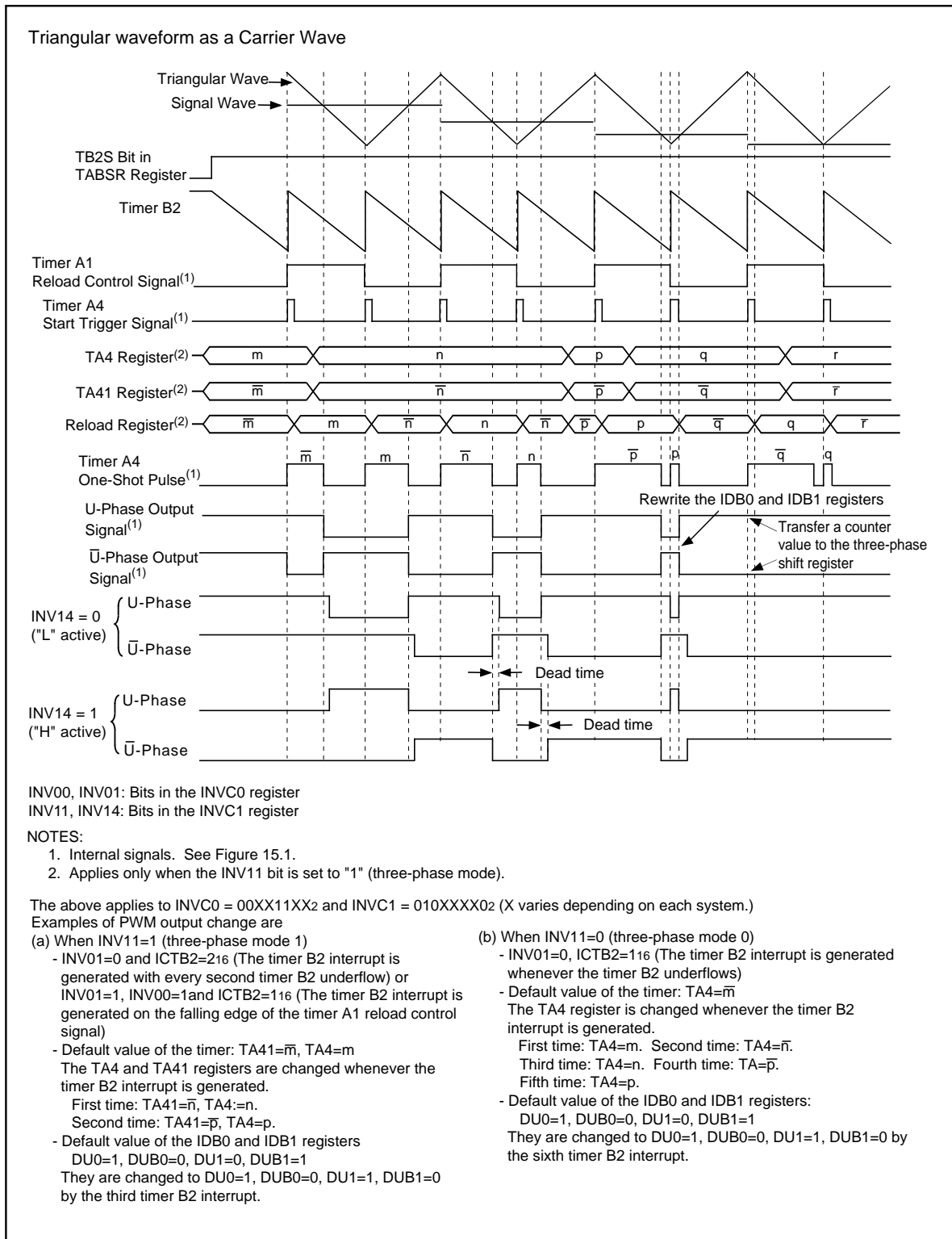


Figure 15.8 Triangular Wave Modulation Operation

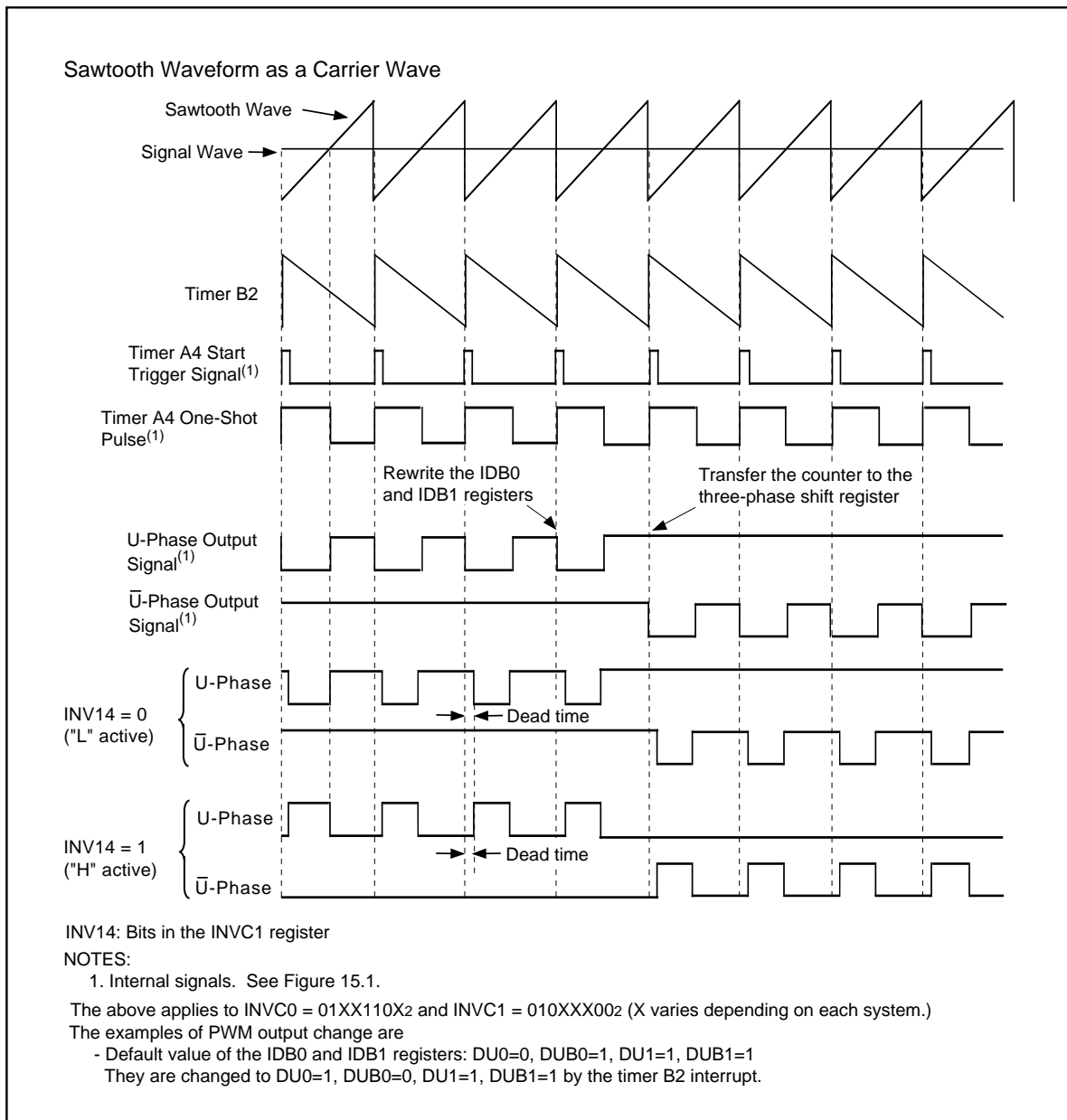


Figure 15.9 Sawtooth Wave Modulation Operation

16. Serial I/O

Serial I/O consists of five channels (UART0 to UART4).

Each UART_i (i=0 to 4) has an exclusive timer to generate the transfer clock and operates independently.

Figure 16.1 shows a UART_i block diagram.

UART_i supports the following modes :

- Clock synchronous serial I/O mode
- Clock asynchronous serial I/O mode (UART mode)
- Special mode 1 (I²C mode)
- Special mode 2
- Special mode 3 (Clock-divided synchronous function, GCI mode)
- Special mode 4 (Bus conflict detect function, IE mode)
- Special mode 5 (SIM mode)

Figures 16.2 to 16.9 show registers associated with UART_i.

Refer to the tables listing each mode for register and pin settings.

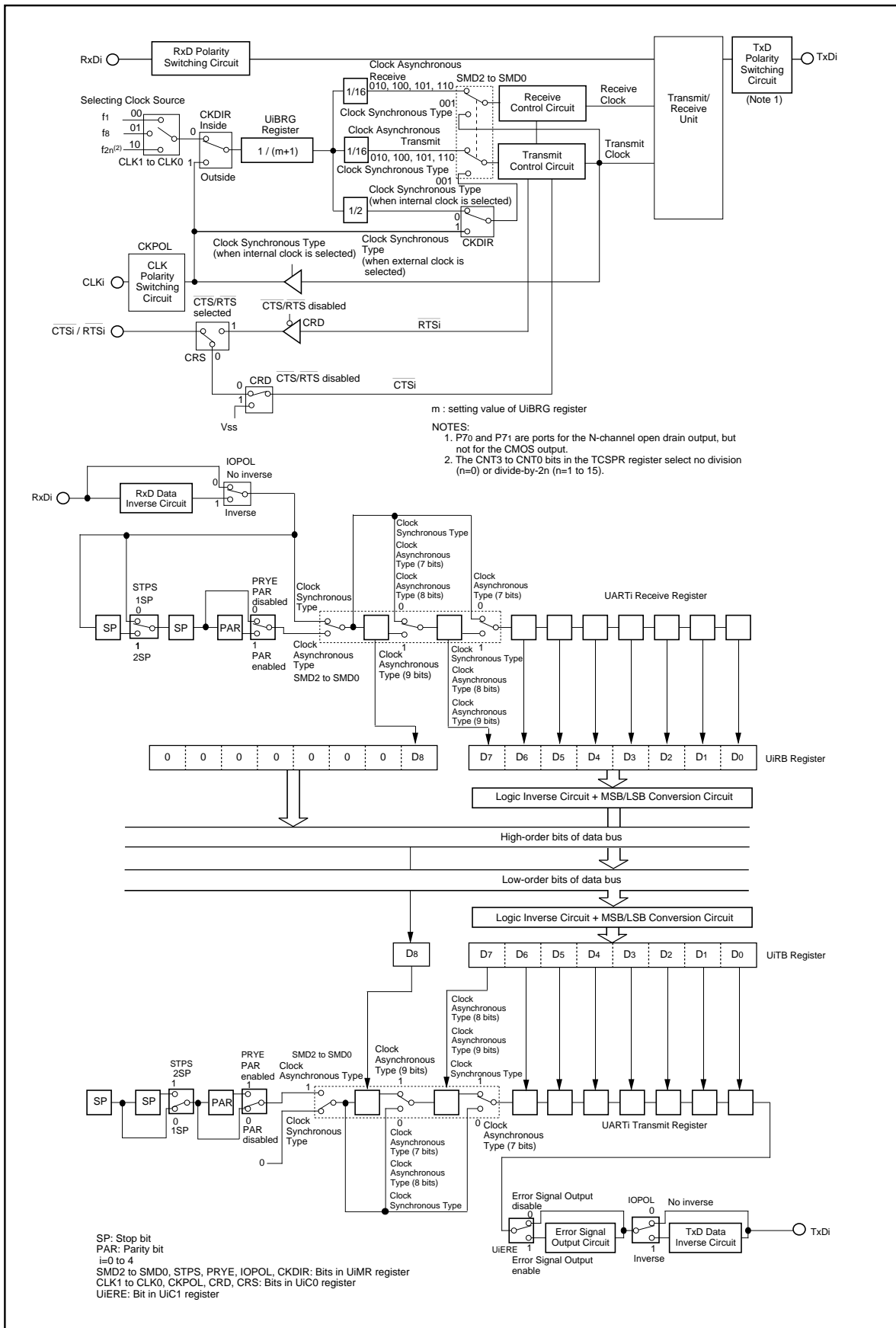


Figure 16.1 UARTi Block Diagram

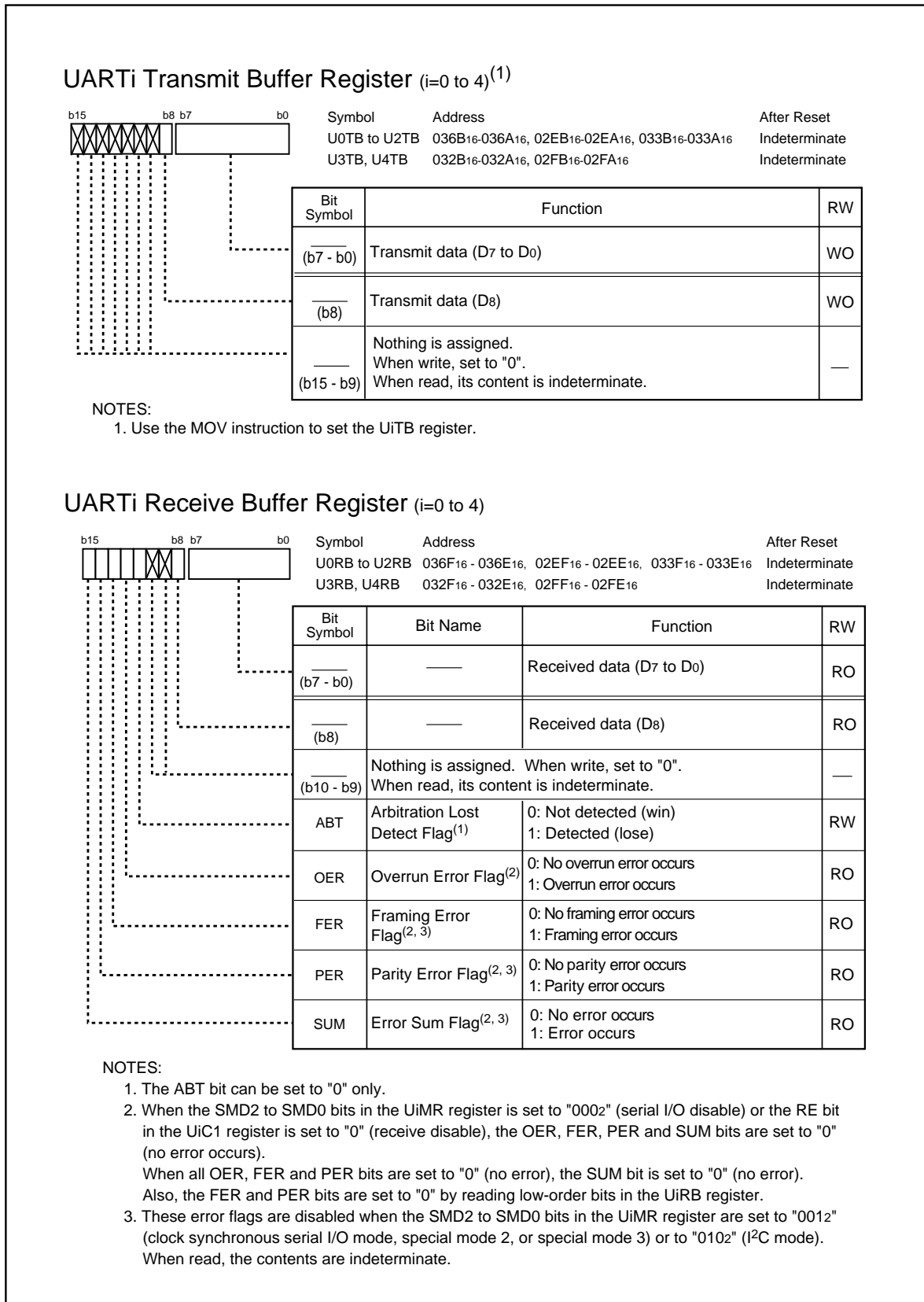


Figure 16.2 U0TB to U4TB Registers and U0RB to U4RB Registers

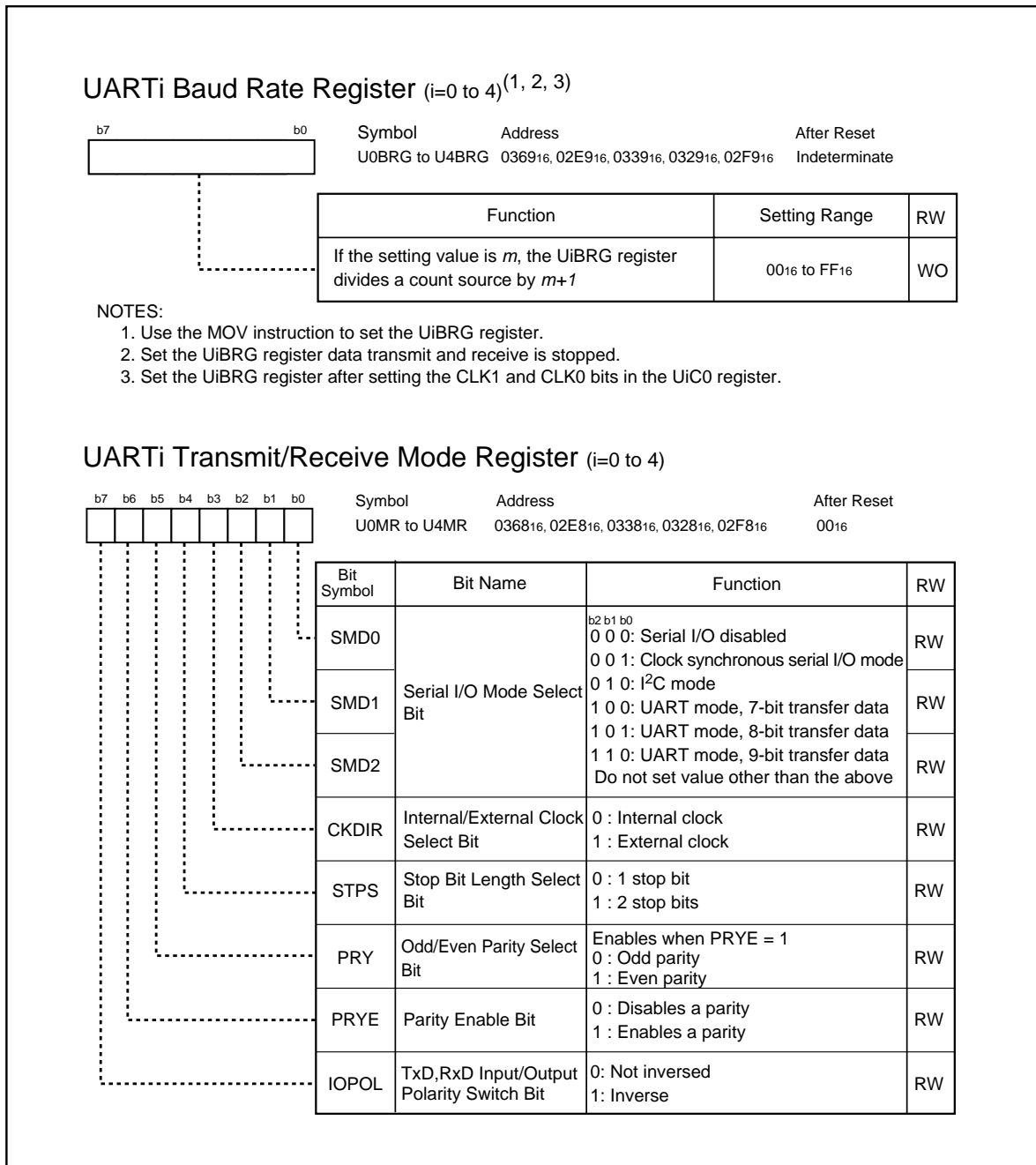


Figure 16.3 U0BRG to U4BRG Registers and U0MR to U4MR Registers

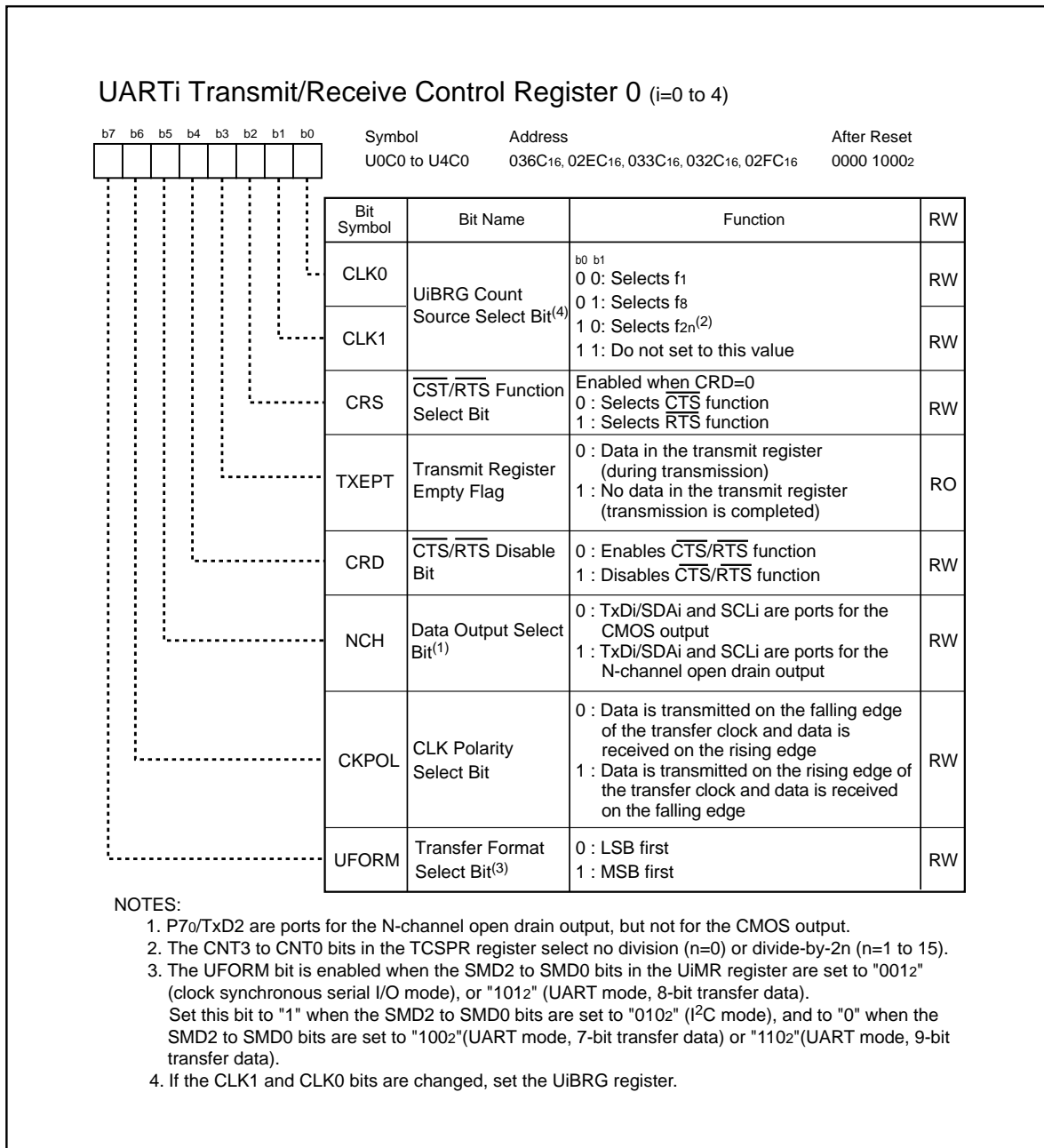


Figure 16.4 U0C0 to U4C0 Registers

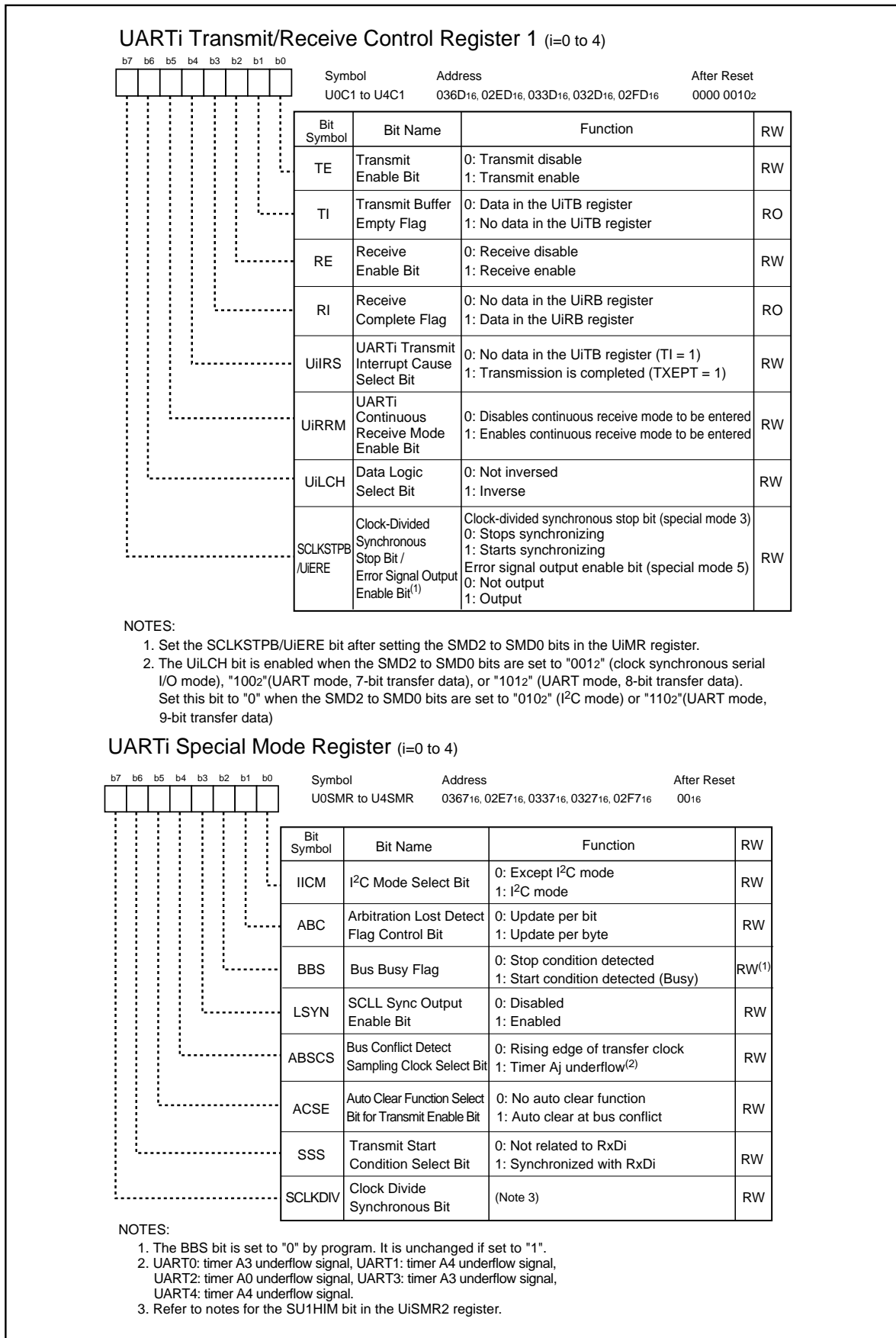


Figure 16.5 U0C1 to U4C1 Registers and U0SMR to U4SMR Registers

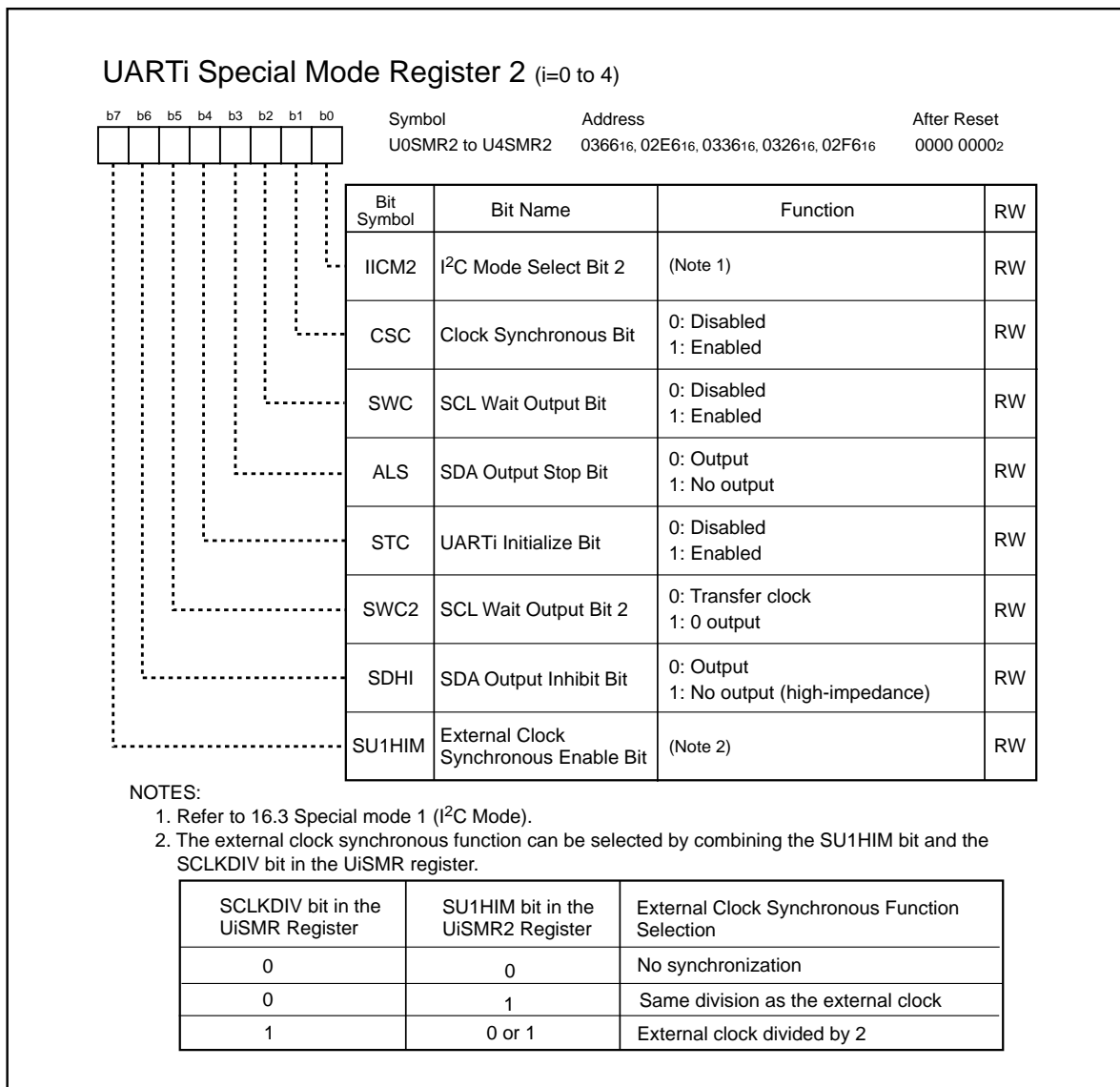


Figure 16.6 U0SMR2 to U4SMR2 Registers

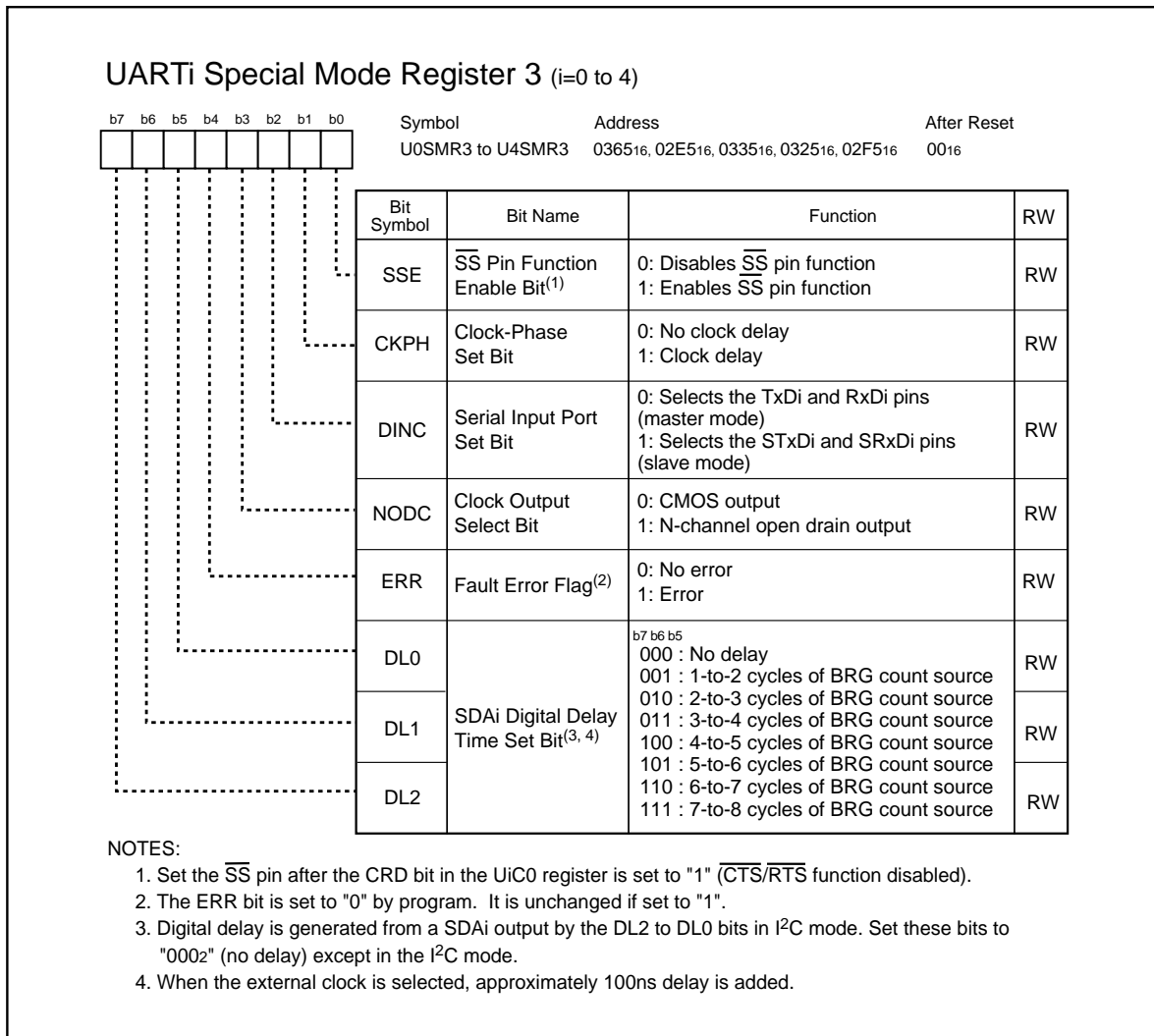


Figure 16.7 U0SMR3 to U4SMR3 Registers

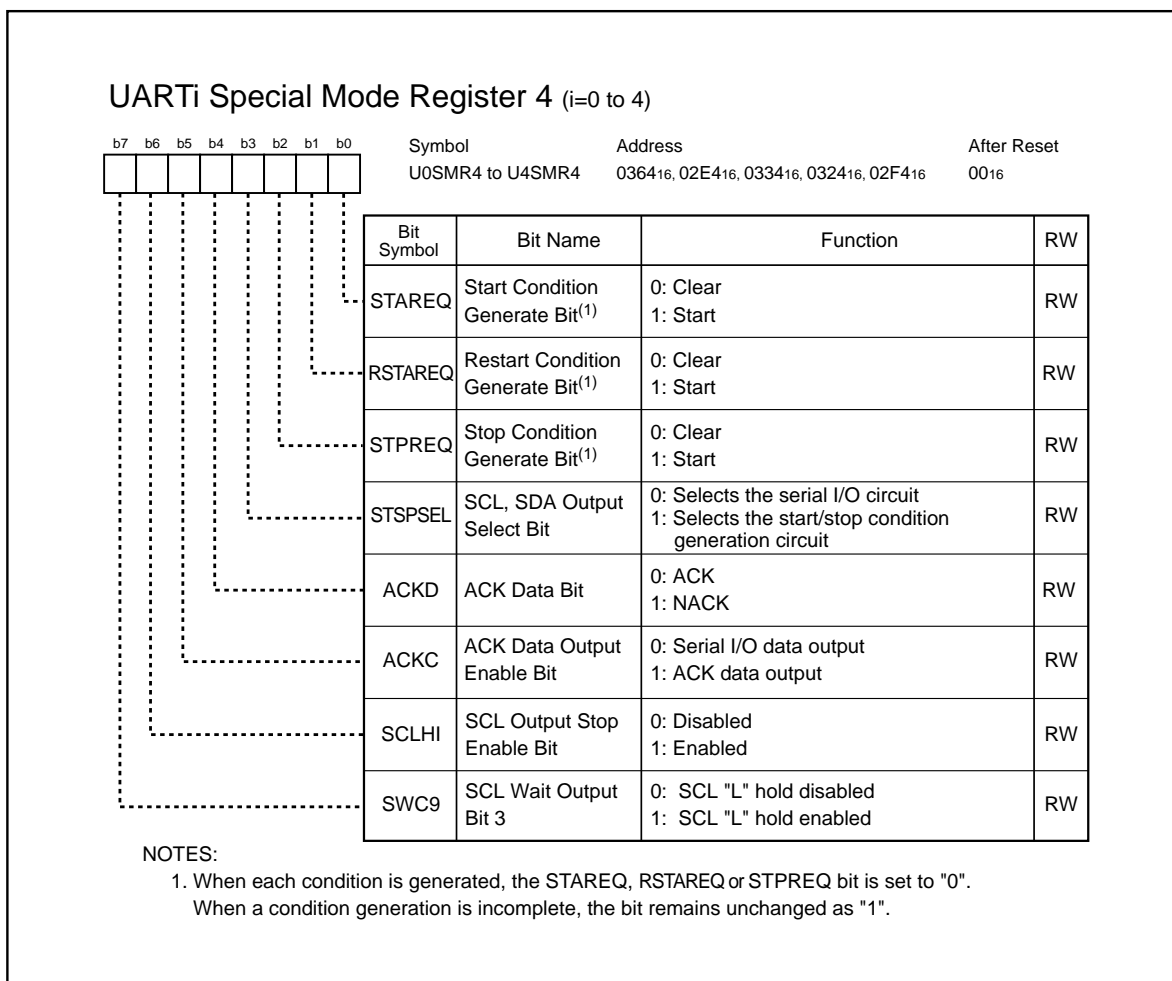


Figure 16.8 U0SMR4 to U4SMR4 Registers

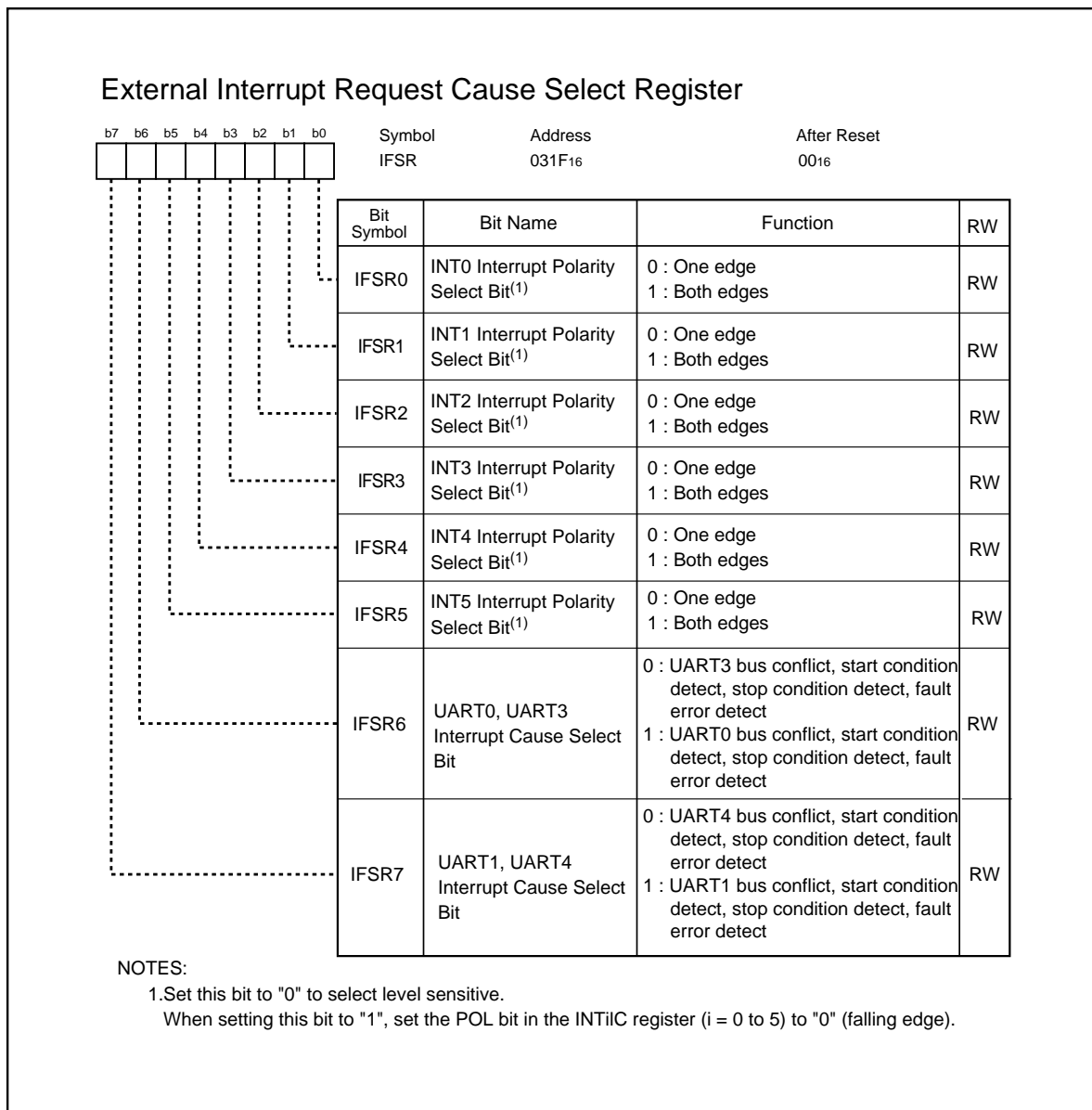


Figure 16.9 IFSR Register

16.1 Clock Synchronous Serial I/O Mode

In clock synchronous serial I/O mode, data is transmitted and received with the transfer clock. Table 16.1 lists specifications of clock synchronous serial I/O mode. Table 16.2 lists registers to be used and settings. Tables 16.3 to 16.5 list pin settings. When UARTi (i=0 to 4) operation mode is selected, the TxDi pin outputs an "H" signal before transfer starts (the TxDi pin is in a high-impedance state when the N-channel open drain output is selected). Figure 16.10 shows transmit and receive timings in clock synchronous serial I/O mode.

Table 16.1 Clock Synchronous Serial I/O Mode Specifications

Item	Specification
Transfer Data Format	<ul style="list-style-type: none"> Transfer data : 8 bits long
Transfer Clock	<ul style="list-style-type: none"> The CKDIR bit in the UiMR register (i=0 to 4) is set to "0" (internal clock selected): $\frac{f_j}{2^{(m+1)}} \quad f_j=f_1, f_8, f_{2n}^{(1)} \quad m : \text{setting value of the UiBRG register } 00_{16} \text{ to } FF_{16}.$ The CKDIR bit is set to "1" (external clock selected) : an input from the CLKi pin
Transmit/Receive Control	<ul style="list-style-type: none"> Selected from the $\overline{\text{CTS}}$ function, $\overline{\text{RTS}}$ function or $\overline{\text{CTS/RTS}}$ function disabled
Transmit Start Condition	<ul style="list-style-type: none"> To start transmitting, the following requirements must be met⁽²⁾: <ul style="list-style-type: none"> - Set the TE bit in the UiC1 register to "1" (transmit enable) - Set the TI bit in the UiC1 register to "0" (data in the UiTB register) - Apply an "L" signal to the CTSi pin when the CTS function is selected
Receive Start Condition	<ul style="list-style-type: none"> To start receiving, the following requirements must be met⁽²⁾: <ul style="list-style-type: none"> - Set the RE bit in the UiC1 register to "1" (receive enable) - Set the TE bit to "1" (transmit enable) - Set the TI bit to "0" (data in the UiTB register)
Interrupt Request Generation Timing	<ul style="list-style-type: none"> Transmit interrupt timing can be selected from the followings: <ul style="list-style-type: none"> - The UiIRS bit in the UiC1 register is set to "0" (no data in the transmit buffer) : when data is transferred from the UiTB register to the UARTi transmit register (transfer started) - The UiIRS bit is set to "1" (transmission completed) : when a data transfer from the UARTi transmit register is completed Receive interrupt timing When data is transferred from the UARTi receive register to the UiRB register (reception completed)
Error Detect	<ul style="list-style-type: none"> Overrun error⁽³⁾ This error occurs when the seventh bit of the next received data is read before reading the UiRB register
Selectable Function	<ul style="list-style-type: none"> CLK polarity Transferred data is output and input on either the rising edge or falling edge of the transfer clock LSB first / MSB first Data is transmitted or received in either bit 0 or in bit 7 Continuous receive mode Data can be received simultaneously by reading the UiRB register Serial data logic inverse This function inverts transmitted or received data logically

NOTES:

- The CNT3 to CNT0 bits in the TCSPR register select no division (n=0) or divide-by-2n (n=1 to 15).
- To start transmission/reception when selecting the external clock, these conditions must be met after the CKPOL bit in the UiC0 register is set to "0" (data is transmitted on the falling edge of the transfer clock and data is received on the rising edge) and the CLKi pin is held high ("H"), or when the CKPOL bit is set to "1" (Data is transmitted on the rising edge of the transfer clock and data is received on the falling edge) and the CLKi pin is held low ("L").
- If an overrun error occurs, the UiRB register is indeterminate. The IR bit in the SiRIC register does not change to "1" (interrupt requested).

Table 16.2 Registers to be Used and Setting Value in Clock Synchronous Serial I/O Mode

Register	Bit	Function
UiTB	0 to 7	Set transmit data
UiRB	0 to 7	Received data can be read
	OER	Overflow error flag
UiBRG	0 to 7	Set bit rate
UiMR	SMD2 to SMD0	Set to "0012"
	CKDIR	Select the internal clock or external clock
	IOPOL	Set to "0"
UiC0	CLK1 to CLK0	Select count source for the UiBRG register
	CRS	Select CTS or RTS when using either
	TXEPT	Transmit register empty flag
	CRD	Enables or disables the CTS or RTS function
	NCH	Select output format of the TxDi pin
	CKPOL	Select transmit clock polarity
	UFORM	Select either LSB first or MSB first
UiC1	TE	Set to "1" to enable data transmission and reception
	TI	Transmit buffer empty flag
	RE	Set to "1" to enable data reception
	RI	Reception complete flag
	UiIRS	Select how the UARTi transmit interrupt is generated
	UiRRM	Set to "1" when using continuous receive mode
	UiLCH	Set to "1" when using data logic inverse
	SCLKSTPB	Set to "0"
UiSMR	0 to 7	Set to "0016"
UiSMR2	0 to 7	Set to "0016"
UiSMR3	0 to 2	Set to "0002"
	NODC	Select clock output format
	4 to 7	Set to "00002"
UiSMR4	0 to 7	Set to "0016"

i=0 to 4

Table 16.3 Pin Settings in Clock Synchronous Serial I/O Mode (1)

Port	Function	Setting		
		PS0 Register	PSL0 Register	PD6 Register
P60	CTS0 input	PS0_0=0	-	PD6_0=0
	RTS0 output	PS0_0=1	-	-
P61	CLK0 input	PS0_1=0	-	PD6_1=0
	CLK0 output	PS0_1=1	-	-
P62	RxD0 input	PS0_2=0	-	PD6_2=0
P63	TxD0 output	PS0_3=1	-	-
P64	CTS1 input	PS0_4=0	-	PD6_4=0
	RTS1 output	PS0_4=1	PSL0_4=0	-
P65	CLK1 input	PS0_5=0	-	PD6_5=0
	CLK1 output	PS0_5=1	-	-
P66	RxD1 input	PS0_6=0	-	PD6_6=0
P67	TxD1 output	PS0_7=1	-	-

Table 16.4 Pin Settings (2)

Port	Function	Setting			
		PS1 Register	PSL1 Register	PSC Register	PD7 Register
P70 ⁽¹⁾	TxD2 output	PS1_0=1	PSL1_0=0	PSC_0=0	-
P71 ⁽¹⁾	RxD2 input	PS1_1=0	-	-	PD7_1=0
P72	CLK2 input	PS1_2=0	-	-	PD7_2=0
	CLK2 output	PS1_2=1	PSL1_2=0	PSC_2=0	-
P73	CTS2 input	PS1_3=0	-	-	PD7_3=0
	RTS2 output	PS1_3=1	PSL1_3=0	PSC_3=0	-

NOTES:

1. P70 and P71 are ports for the N-channel open drain output.

Table 16.5 Pin Settings (3)

Port	Function	Setting		
		PS3 Register ⁽¹⁾	PSL3 Register	PD9 Register ⁽¹⁾
P90	CLK3 input	PS3_0=0	-	PD9_0=0
	CLK3 output	PS3_0=1	-	-
P91	RxD3 input	PS3_1=0	-	PD9_1=0
P92	TxD3 output	PS3_2=1	PSL3_2=0	-
P93	CTS3 input	PS3_3=0	PSL3_3=0	PD9_3=0
	RTS3 output	PS3_3=1	-	-
P94	CTS4 input	PS3_4=0	PSL3_4=0	PD9_4=0
	RTS4 output	PS3_4=1	-	-
P95	CLK4 input	PS3_5=0	PSL3_5=0	PD9_5=0
	CLK4 output	PS3_5=1	-	-
P96	TxD4 output	PS3_6=1	-	-
P97	RxD4 input	PS3_7=0	-	PD9_7=0

NOTES:

1. Set the PD9 and PS3 registers immediately after the PRC2 bit in the PRCR register is set to "1" (write enable). Do not generate an interrupt or a DMA transfer between the instruction to set the PRC2 bit to "1" and the instruction to set the PD9 and PS3 registers.

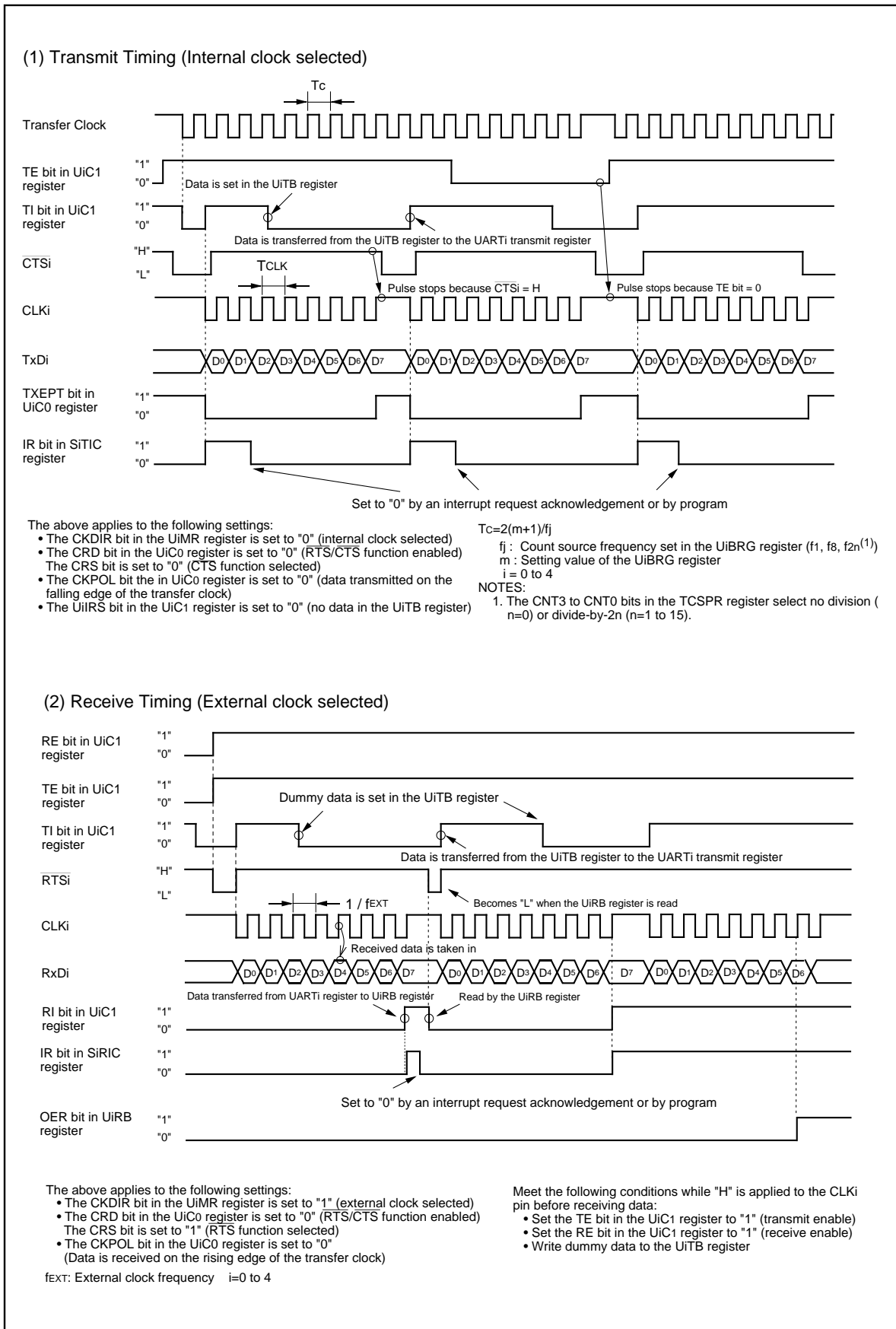


Figure 16.10 Transmit and Receive Operation

16.1.1 Selecting CLK Polarity

As shown in Figure 16.11, the CKPOL bit in the UiC0 register (i=0 to 4) determines the polarity of the transfer clock.

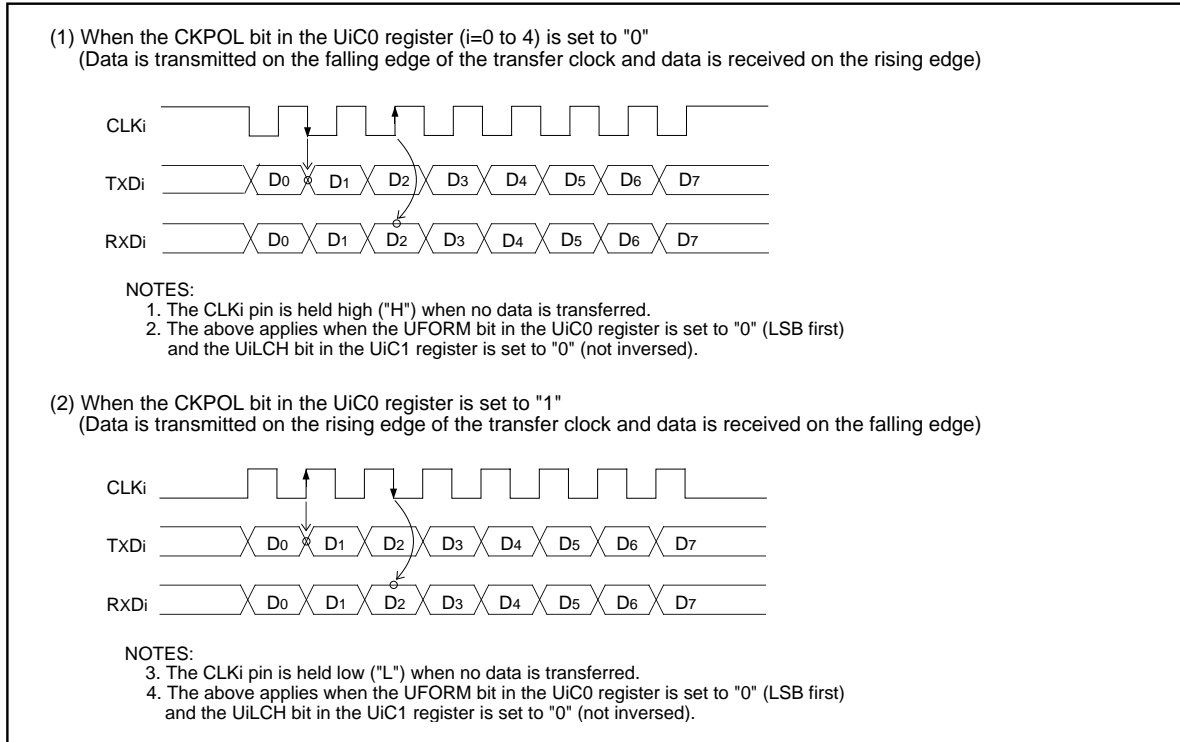


Figure 16.11 Transfer Clock Polarity

16.1.2 Selecting LSB First or MSB First

As shown in Figure 16.12, the UFORM bit in the UiC0 register (i=0 to 4) determines a data transfer format.

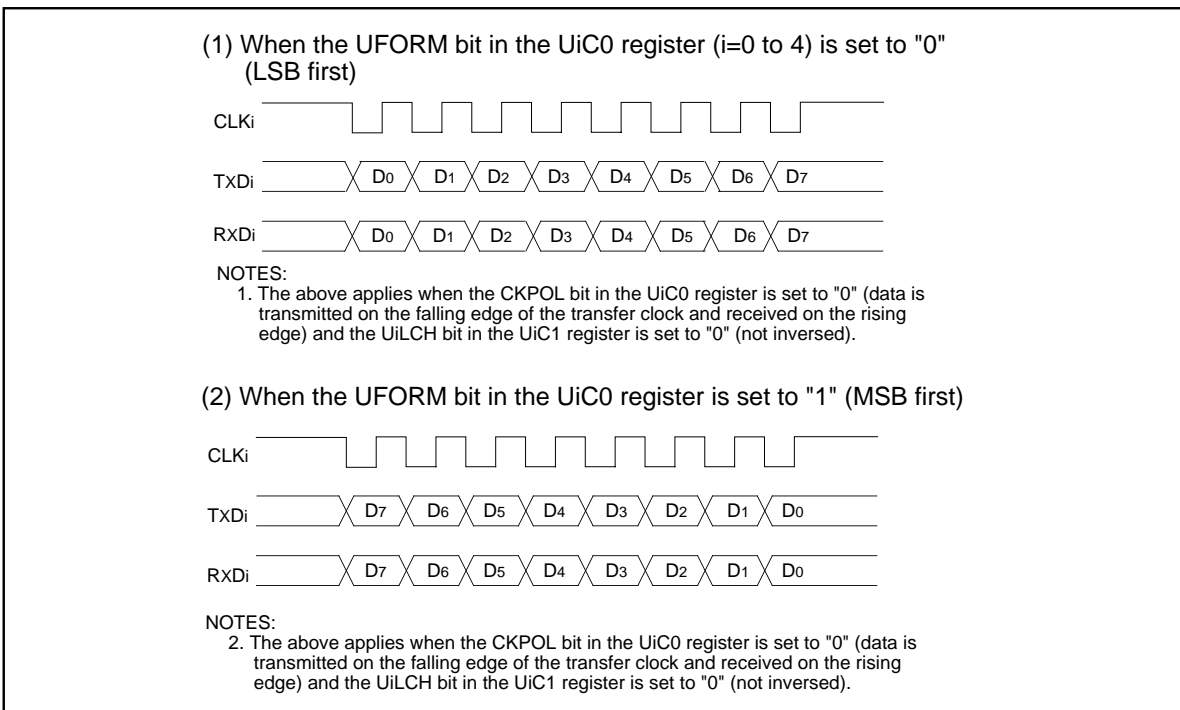


Figure 16.12 Transfer Format

16.1.3 Continuous Receive Mode

When the UiRRM bit in the UiC1 register (i=0 to 4) is set to "1" (continuous receive mode), the TI bit is set to "0" (data in the UiTB register) by reading the UiRB register. When the UiRRM bit is set to "1", do not set dummy data in the UiTB register by program.

16.1.4 Serial Data Logic Inverse

When the UiLCH bit in the UiC1 register is set to "1" (inverse), data logic written in the UiTB register is inverted when transmitted. The inverted receive data logic can be read by reading the UiRB register. Figure 16.13 shows a switching example of the serial data logic.

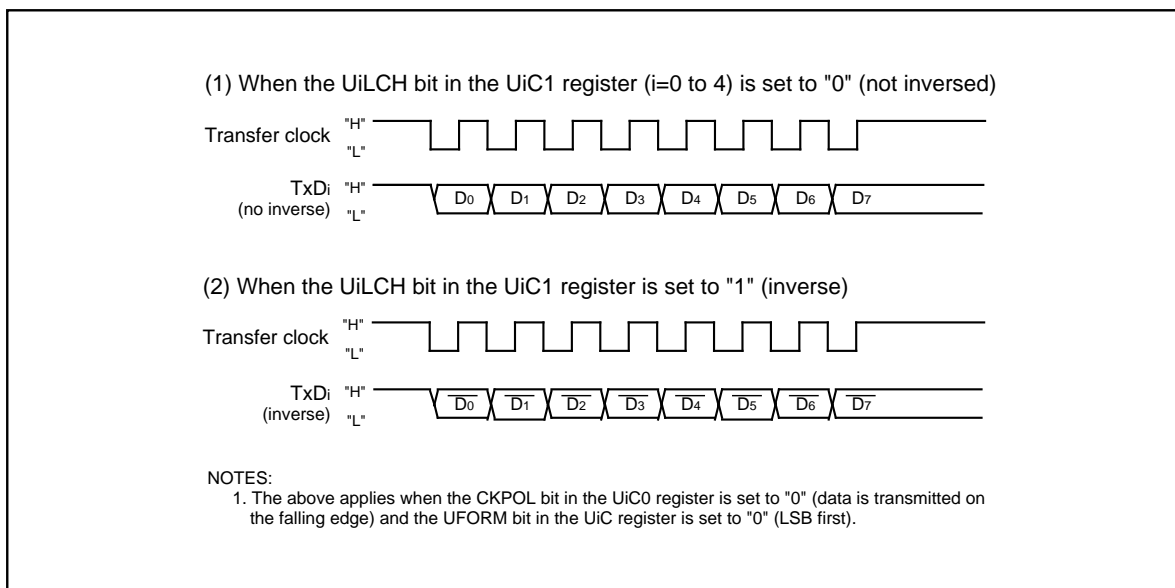


Figure 16.13 Serial Data Logic Inverse

16.2 Clock Asynchronous Serial I/O (UART) Mode

In UART mode, data is transmitted and received after setting a desired bit rate and data transfer format. Table 16.6 lists specifications of UART mode.

Table 16.6 UART Mode Specifications

Item	Specification
Transfer Data Format	<ul style="list-style-type: none"> • Character bit (transfer data) : selected from 7 bits, 8 bits, or 9 bits long • Start bit: 1 bit long • Parity bit: selected from odd, even, or none • Stop bit: selected from 1 bit or 2 bits long
Transfer Clock	<ul style="list-style-type: none"> • The CKDIR bit in the UiMR register is set to "0" (internal clock selected) : $f_j/16(m+1)$ $f_j = f_1, f_8, f_{2n}^{(1)}$ m: setting value of the UiBRG register 0016 to FF16 • The CKDIR bit is set to "1" (external clock selected) : $f_{EXT}/16(m+1)$ f_{EXT}: clock applied to the CLKi pin
Transmit/Receive Control	<ul style="list-style-type: none"> • Select from \overline{CTS} function, \overline{RTS} function or $\overline{CTS/RTS}$ function disabled
Transmit Start Condition	<ul style="list-style-type: none"> • To start transmitting, the following requirements must be met: <ul style="list-style-type: none"> - Set the TE bit in the UiC1 register to "1" (transmit enable) - Set the TI bit in the UiC1 register to "0" (data in the UiTB register) - Apply an "L" signal to the CTSi pin when the CTS function is selected
Receive Start Condition	<ul style="list-style-type: none"> • To start receiving, the following requirements must be met: <ul style="list-style-type: none"> - Set the RE bit in the UiC1 register to "1" (receive enable) - The start bit is detected
Interrupt Request Generation Timing	<ul style="list-style-type: none"> • Transmit interrupt timing can be selected from the followings: <ul style="list-style-type: none"> - The UiIRS bit in the UiC1 register is set to "0" (no data in the transmit buffer) : when data is transferred from the UiTB register to the UARTi transmit register (transfer started) - The UiIRS bit is set to "1" (transmission completed) : when data transmission from the UARTi transfer register is completed • Receive interrupt timing when data is transferred from the UARTi receive register to the UiRB register (reception completed)
Error Detect	<ul style="list-style-type: none"> • Overrun error⁽²⁾ This error occurs when the bit before the last stop bit of the next received data is read prior to reading the UiRB register (the first stop bit when selecting 2 stop bits) • Framing error This error occurs when the number of stop bits set is not detected • Parity error When parity is enabled, this error occurs when the number of "1" in parity and character bits does not match the number of "1" set • Error sum flag This flag is set to "1" when any of an overrun, framing or parity errors occur
Selectable Function	<ul style="list-style-type: none"> • LSB first / MSB first Data is transmitted or received in either bit 0 or in bit 7 • Serial data logic inverse Logic values of data to be transmitted or received data are inverted. The start bit and stop bit are not inverted • Tx/D, Rx/D I/O polarity switching Tx/D pin output and Rx/D pin input are inverted

NOTES:

1. The CNT3 to CNT0 bits in the TCSPPR register select no division (n=0) or divide-by-2n (n=1 to 15).
2. If an overrun error occurs, the UiRB register is indeterminate. The IR bit in the SiRIC register remains unchanged as "1" (interrupt requested).

Table 16.7 lists registers to be used and settings. Tables 16.8 to 16.10 list pin settings. When UART_i (i=0 to 4) operation mode is selected, the TxDi pin outputs an "H" signal before transfer is started (the TxDi pin is in a high-impedance state when the N-channel open drain output is selected). Figure 16.14 shows an example of a transmit operation in UART mode. Figure 16.15 shows an example of a receive operation in UART mode.

Table 16.7 Registers to be Used and Settings in UART

Register	Bit	Function
UiTB	0 to 8	Set transmit data ⁽¹⁾
UiRB	0 to 8	Received data can be read ⁽¹⁾
	OER, FER, PER, SUM	Error flags
UiBRG	0 to 7	Set bit rate
UiMR	SMD2 to SMD0	Set to "100 ₂ " when transfer data is 7 bits long Set to "101 ₂ " when transfer data is 8 bits long Set to "110 ₂ " when transfer data is 9 bits long
	CKDIR	Select the internal clock or external clock
	STPS	Select stop bit length
	PRY, PRYE	Select parity enable or disable, odd or even
	IOPOL	Select TxD / RxD I/O polarity
UiC0	CLK0, CLK1	Select count source for the UiBRG register
	CRS	Select either CTS or RTS when using either
	TXEPT	Transfer register empty flag
	CRD	Enables or disables the CTS or RTS function
	NCH	Select output format of the TxDi pin
	CKPOL	Set to "0"
	UFORM	Select the LSB first or MSB first when a transfer data is 8 bits long Set to "0" when transfer data is 7 bits or 9 bits long
UiC1	TE	Set to "1" to enable data transmission
	TI	Transfer buffer empty flag
	RE	Set to "1" to enable data reception
	RI	Reception complete flag
	UiIRS	Select how the UART _i transmit interrupt is generated
	UiRRM	Set to "0"
	UiLCH	Select whether or not data logic is inversed when transfer data length is 7 or 8 bits. Set to "0" when transfer data length is 9 bits.
	UiERE	Set to either "0" or "1"
UiSMR	0 to 7	Set to "00 ₁₆ "
UiSMR2	0 to 7	Set to "00 ₁₆ "
UiSMR3	0 to 7	Set to "00 ₁₆ "
UiSMR4	0 to 7	Set to "00 ₁₆ "

NOTES:

1. Use bits 0 to 6 when transfer data is 7 bits long, bits 0 to 7 when 8 bits long, bits 0 to 8 when 9 bits long.

Table 16.8 Pin Settings in UART (1)

Port	Function	Setting		
		PS0 Register	PSL0 Register	PD6 Register
P60	CTS0 input	PS0_0=0	–	PD6_0=0
	RTS0 output	PS0_0=1	–	–
P61	CLK0 input	PS0_1=0	–	PD6_1=0
P62	RxD0 input	PS0_2=0	–	PD6_2=0
P63	TxD0 output	PS0_3=1	–	–
P64	CTS1 input	PS0_4=0	–	PD6_4=0
	RTS1 output	PS0_4=1	PSL0_4=0	–
P65	CLK1 input	PS0_5=0	–	PD6_5=0
P66	RxD1 input	PS0_6=0	–	PD6_6=0
P67	TxD1 output	PS0_7=1	–	–

Table 16.9 Pin Settings (2)

Port	Function	Setting			
		PS1 Register	PSL1 Register	PSC Register	PD7 Register
P70 ⁽¹⁾	TxD2 output	PS1_0=1	PSL1_0=0	PSC_0=0	–
P71 ⁽¹⁾	RxD2 input	PS1_1=0	–	–	PD7_1=0
P72	CLK2 input	PS1_2=0	–	–	PD7_2=0
P73	CTS2 input	PS1_3=0	–	–	PD7_3=0
	RTS2 output	PS1_3=1	PSL1_3=0	PSC_3=0	–

NOTES:

1. P70 and P71 are ports for the N-channel open drain output.

Table 16.10 Pin Settings (3)

Port	Function	Setting		
		PS3 Register ⁽¹⁾	PSL3 Register	PD9 Register ⁽¹⁾
P90	CLK3 input	PS3_0=0	–	PD9_0=0
P91	RxD3 input	PS3_1=0	–	PD9_1=0
P92	TxD3 output	PS3_2=1	PSL3_2=0	–
P93	CTS3 input	PS3_3=0	PSL3_3=0	PD9_3=0
	RTS3 output	PS3_3=1	–	–
P94	CTS4 input	PS3_4=0	PSL3_4=0	PD9_4=0
	RTS4 output	PS3_4=1	–	–
P95	CLK4 input	PS3_5=0	PSL3_5=0	PD9_5=0
P96	TxD4 output	PS3_6=1	–	–
P97	RxD4 input	PS3_7=0	–	PD9_7=0

NOTES:

1. Set the PD9 and PS3 registers set immediately after the PRC2 bit in the PRCR register is set to "1" (write enable). Do not generate an interrupt or a DMA transfer between the instruction to set to the PRC2 bit to "1" and the instruction to set the PD9 and PS3 registers.

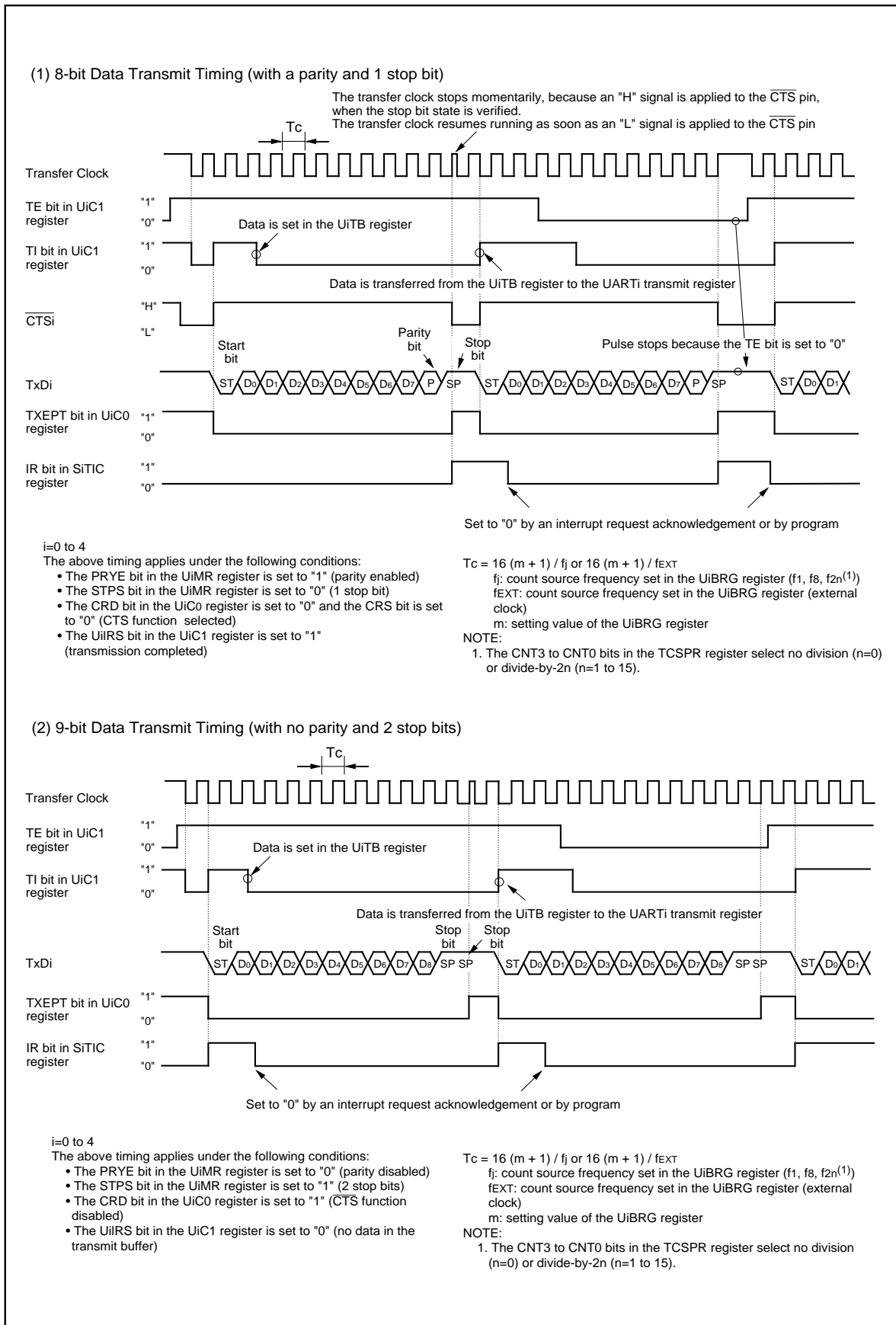


Figure 16.14 Transmit Operation

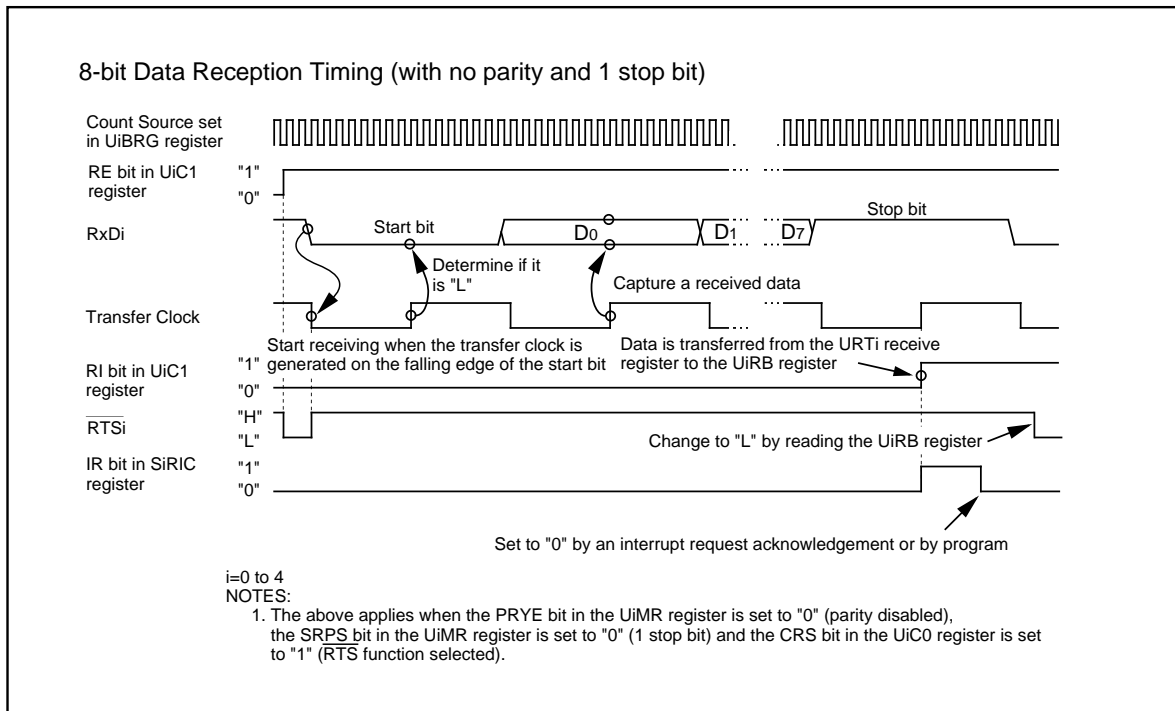


Figure 16.15 Receive Operation

16.2.1 Bit Rate

In UART mode, bit rate is clock frequency which is divided by a setting value of the UiBRG ($i=0$ to 4) register and again divided by 16. Table 16.11 lists an example of bit rate setting.

Table 16.11 Bit Rate

Bit Rate (bps)	Count Source of UiBRG	Peripheral Function Clock: 16MHz		Peripheral Function Clock: 24MHz		Peripheral Function Clock: 32MHz	
		Setting Value of UiBRG: n	Actual Bit Rate (bps)	Setting Value of UiBRG: n	Actual Bit Rate (bps)	Setting Value of UiBRG: n	Actual Bit Rate (bps)
1200	f8	103 (67h)	1202	155 (96h)	1202	207 (CFh)	1202
2400	f8	51 (33h)	2404	77 (46h)	2404	103 (67h)	2404
4800	f8	25 (19h)	4808	38 (26h)	4808	51 (33h)	4808
9600	f1	103 (67h)	9615	155 (96h)	9615	207 (CFh)	9615
14400	f1	68 (44h)	14493	103 (67h)	14423	138 (8Ah)	14388
19200	f1	51 (33h)	19231	77 (46h)	19231	103 (67h)	19231
28800	f1	34 (22h)	28571	51 (33h)	28846	68 (44h)	28986
31250	f1	31 (1Fh)	31250	47 (2Fh)	31250	63 (3Fh)	31250
38400	f1	25 (19h)	38462	38 (26h)	38462	51 (33h)	38462
51200	f1	19 (13h)	50000	28 (1Ch)	51724	38 (26h)	51282

16.2.2 Selecting LSB First or MSB First

As shown in Figure 16.16, the UFORM bit in the UiC0 register (i=0 to 4) determines data transfer format. This function is available for 8-bit transfer data.

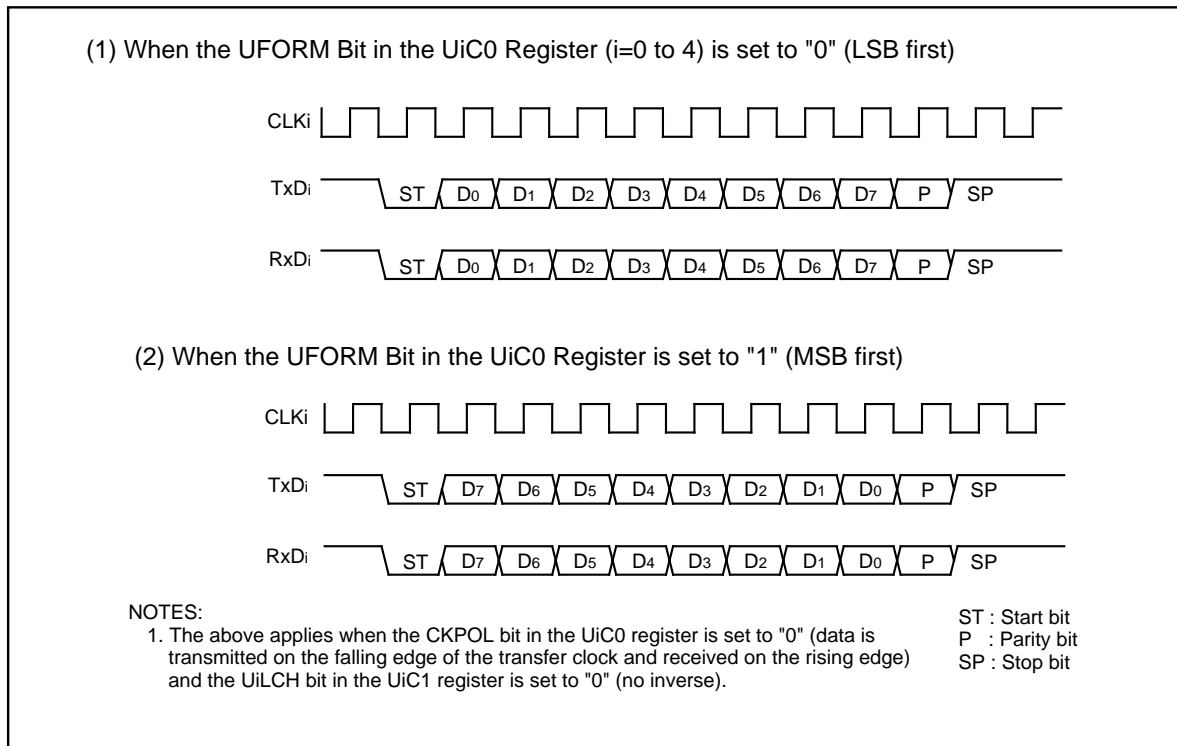


Figure 16.16 Transfer Format

16.2.3 Serial Data Logic Inverse

After the UiLCH bit in the UiC1 register is set to "1", data logic is inversed when writing to the UiTB register (i=0 to 4) and reading from the UiRB register. Figure 16.17 shows a switching example of the serial data logic.

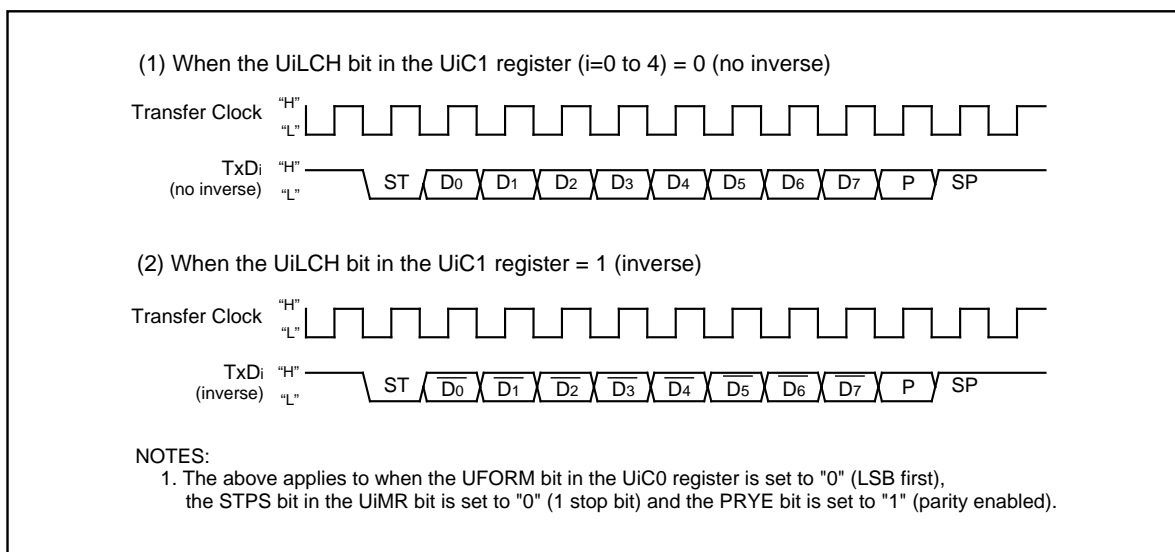


Figure 16.17 Serial Data Logic Inverse

16.2.4 TxD and RxD I/O Polarity Inverse

TxD pin output and RxD pin input are inverted. All I/O data level, including the start bit, stop bit and parity bit, are inverted. Figure 16.18 shows TxD and RxD I/O polarity inverse.

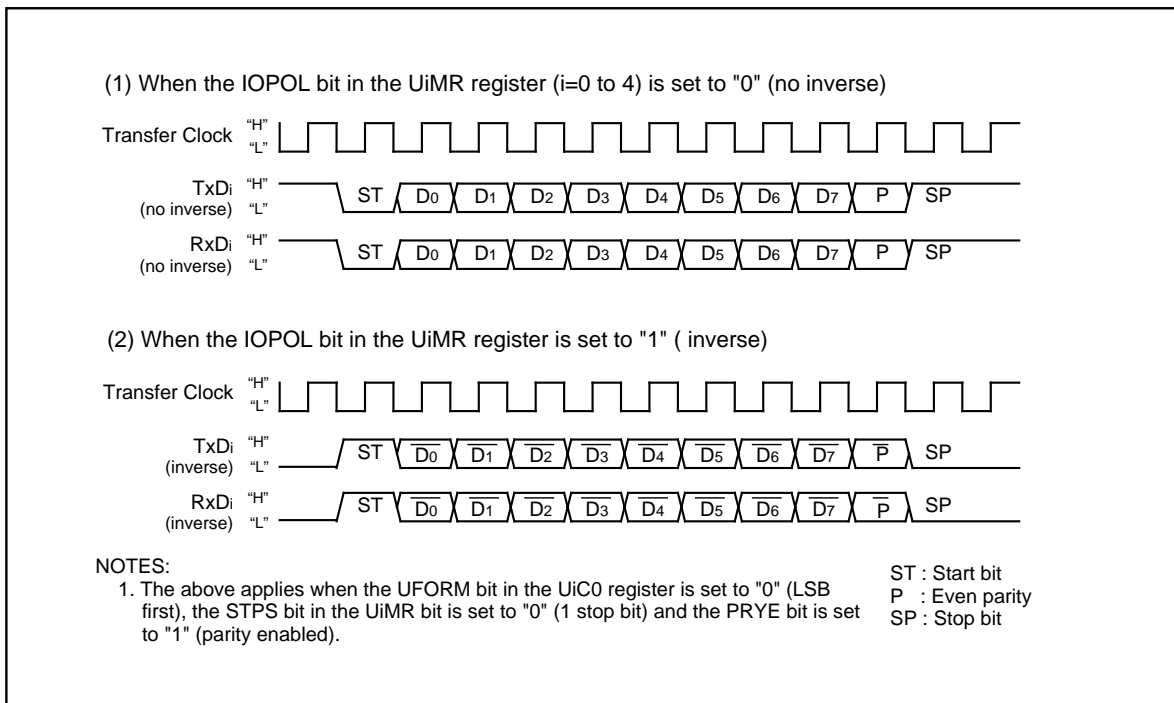


Figure 16.18 TxD, RxD I/O Polarity Inverse

16.3 Special Mode 1 (I²C Mode)

I²C mode is a mode to communicate with external devices with a simplified I²C. Table 16.12 lists specifications of I²C mode. Table 16.13 lists registers to be used and settings, Table 16.14 lists each function. Figure 16.19 shows a block diagram of I²C mode. Figure 16.20 shows timings for transfer to the UiRB register and interrupts. Tables 16.14 to 16.16 list pin settings.

As shown in Table 16.14, I²C mode is entered when the SMD2 to SMD0 bits in the UiMR register is set to "0102" and the IICM bit in the UiMR register is set to "1". SDAi output changes after SCLi becomes low ("L") and stabilizes due to a SDAi output via the delay circuit.

Table 16.12 I²C Mode Specifications

Item	Specifications
Interrupt	Start condition detect, stop condition detect, no acknowledgment detect, acknowledgment detect
Selectable Function	<ul style="list-style-type: none"> • Arbitration lost The update timing of the ABT bit in the UiRB register can be selected. Refer to 16.3.3 Arbitration. • SDAi digital delay Selected from no digital delay or 2 to 8 cycle delay of the count source of BRG. Refer to 16.3.5 SDA Output. • Clock phase setting Selected from clock delay or no clock delay. Refer to 16.3.4 Transfer Clock.

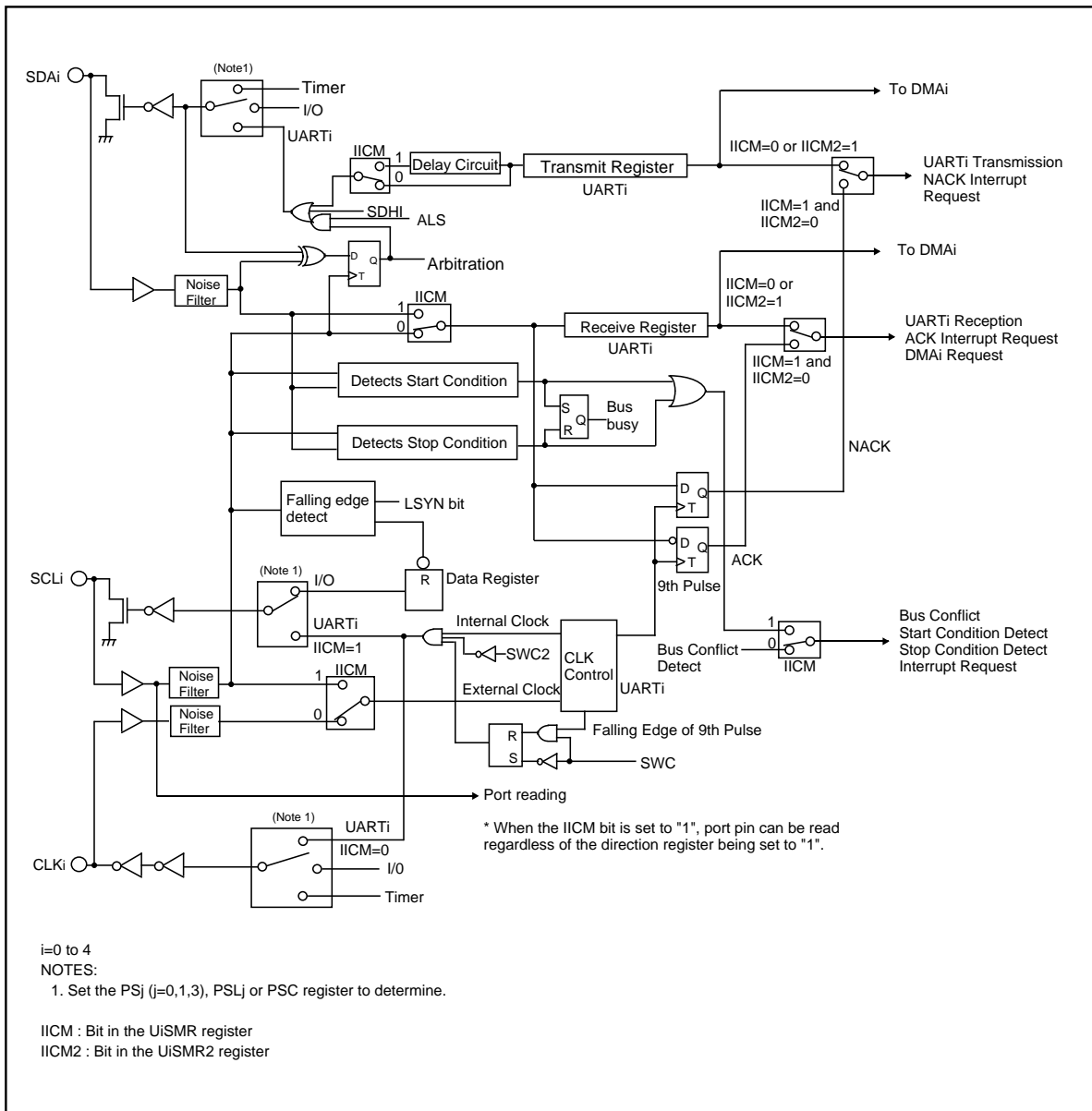


Figure 16.19 I²C Mode Block Diagram

Table 16.13 Registers To Be Used and Settings (I²C Mode)

Register	Bit	Function	
		Master	Slave
UiTB	0 to 7	Set transmit data	
UiRB	0 to 7	Received data can be read	
	8	ACK or NACK bit can be read	
	ABT	Arbitration lost detect flag	Disabled
	OER	Overrun error flag	
UiBRG	0 to 7	Set bit rate	Disabled
UiMR	SMD2 to SMD0	Set to "010z"	
	CKDIR	Set to "0"	Set to "1"
	IOPOL	Set to "0"	
UiC0	CLK1 to CLK0	Select count source of the UiBRG register	Disabled
	CRS	Disabled because CRD = 1	
	TXEPT	Transfer register empty flag	
	CRD, NCH	Set to "1"	
	CKPOL	Set to "0"	
	UFORM	Set to "1"	
UiC1	TE	Set to "1" to enable data transmission	
	TI	Transfer buffer empty flag	
	RE	Set to "1" to enable data reception	
	RI	Reception complete flag	
	UiRRM, UiLCH, UiERE	Set to "0"	
UiSMR	IICM	Set to "1"	
	ABC	Select an arbitration lost detect timing	Disabled
	BBS	Bus busy flag	
	3 to 7	Set to "00000z"	
UiSMR2	IICM2	See Table 16.14	
	CSC	Set to "1" to enable clock synchronization	Set to "0"
	SWC	Set to "1" to output fixed "L" from the SDAi on the falling edge of the ninth bit of the transfer clock	
	ALS	Set to "1" to terminate SDA output when detecting the arbitration lost	Not used. Set to "0"
	STC	Not used. Set to "0"	Set to "1" to reset UARTi by detecting a start condition
	SWC2	Set to "1" to forcibly output an "L" signal from SCL	
	SDHI	Set to "1" to disable SDA output	
	SU1HIM	Set to "0"	
UiSMR3	SSE	Set to "0"	
	CKPH	See Table 16.14.	
	DINC, NODC, ERR	Set to "0"	
	DL2 to DL0	Set digital delay value	
UiSMR4	STAREQ	Set to "1" when generating start condition	Not used. Set to "0"
	RSTAREQ	Set to "1" when generating restart condition	
	STPREQ	Set to "1" when generating stop condition	
	STSPSEL	Set to "1" when using a condition generating function	
	ACKD	Select ACK or NACK	
	ACKC	Set to "1" to output ACK data	
	SCLHI	Set to "1" to enable SCL output stop when detecting stop condition	Not used. Set to "0"
	SWC9	Not used. Set to "0"	Set to "1" to output fixed "L" from SCLi on the falling edge of the ninth bit of the transfer clock
IFSR	IFSR6, IFSR7	Set to "1"	

i=0 to 4

Table 16.14 I²C Mode Functions

Function	Clock Synchronous Serial I/O Mode (SMD2 to SMD0=0012, IICM=0)	I ² C Mode (SMD2 to SMD0=0102, IICM=1)			
		IICM2=0 (NACK/ACK interrupt)		IICM2=1 (UART transmit / UART receive interrupt)	
		CKPH=0 (No clock delay)	CKPH=1 (Clock delay)	CKPH=0 (No clock delay)	CKPH=1 (Clock delay)
Interrupt Numbers 39 to 41 Generated ⁽¹⁾ (See Figure 16.20)	-	Start condition or stop condition detect (See Table 16.17)			
Interrupt Number 17, 19, 33, 35 and 37 Generated ⁽¹⁾ (See Figure 16.20)	UARTi Transmission - Transmission started or completed (selected by the UiIRS register)	No Acknowledgement Detect (NACK) - Rising edge of 9th bit of SCLi	UARTi Transmission - Rising edge of 9th bit of SCLi	UARTi Transmission - Next falling edge after the 9th bit of SCLi	
Interrupt Numbers 18, 20, 34, 36 and 38 Generated ⁽¹⁾ (See Figure 16.20)	UARTi Reception - Receiving at 8th bit CKPOL=0(rising edge) CKPOL=1(falling edge)	Acknowledgement Detect (ACK) - Rising edge of 9th bit of SCLi	UARTi Reception - Falling edge of 9th bit of SCLi		
Data Transfer Timing from the UART Receive Shift Register to the UiRB Register	CKPOL=0(rising edge) CKPOL=1(falling edge)	Rising edge of 9th bit of SCLi	Falling edge of 9th bit of SCLi	Falling edge and rising edge of 9th bit of SCLi	
UARTi Transmit Output Delay	No delay	Delay			
P63, P67, P70, P92, P96 Pin Functions	TxDi output	SDAi input and output			
P62, P66, P71, P91, P97 Pin Functions	RxDi input	SCLi input and output			
P61, P65, P72, P90, P95 Pin Functions	Select CLKi input or output	- (Not used in I ² C mode)			
Noise Filter Width	15ns	200ns			
Reading RxDi and SCLi Pin Levels	Can be read if port direction bit is set to "0"	Can be read regardless of the port direction bit			
Default Value of TxDi, SDAi Output	CKPOL=0 (H) CKPOL=1 (L)	Values set in the port register before entering I ² C mode ⁽²⁾			
SCLi Default and End Value	-	H	L	H	L
DMA Generated (See Figure 16.20)	UARTi reception	Acknowledgement detect (ACK)		UARTi Reception - Falling edge of 9 bit of SCLi	
Store Received Data	1st to 8th bits of the received data are stored into bits 0 to 7 in the UiRB register	1st to 8th bits of the received data are stored into bits 7 to 0 in the UiRB register	1st to 7th bits of the received data are stored into bits 6 to 0 in the UiRB register. 8th bit is stored into bit 8 in the UiRB register.		
			1st to 8th bits are stored into bits 7 to 0 in the UiRB register ⁽³⁾		
Reading Received Data	The UiRB register status is read	Bits 6 to 0 in the UiRB registers ⁽⁴⁾ are read as bit 7 to 1. Bit 8 in the UiRB register is read as bit 0			

i=0 to 4

NOTES:

- Follow the procedures below to change how an interrupt is generated.
 - Disable interrupt of corresponding interrupt number.
 - Change how an interrupt is generated.
 - Set the IR bit of a corresponding interrupt number to "0" (no interrupt requested).
 - Set the ILVL2 to ILVL0 bits of a corresponding interrupt number.
- Set default value of the SDAi output when the SMD2 to SMD0 bits in the UiMR register are set to "0002" (serial I/O disabled).
- Second data transfer to the UiRB register (on the rising edge of the ninth bit of SCLi).
- First data transfer to the UiRB register (on the falling edge of the ninth bit of SCLi).

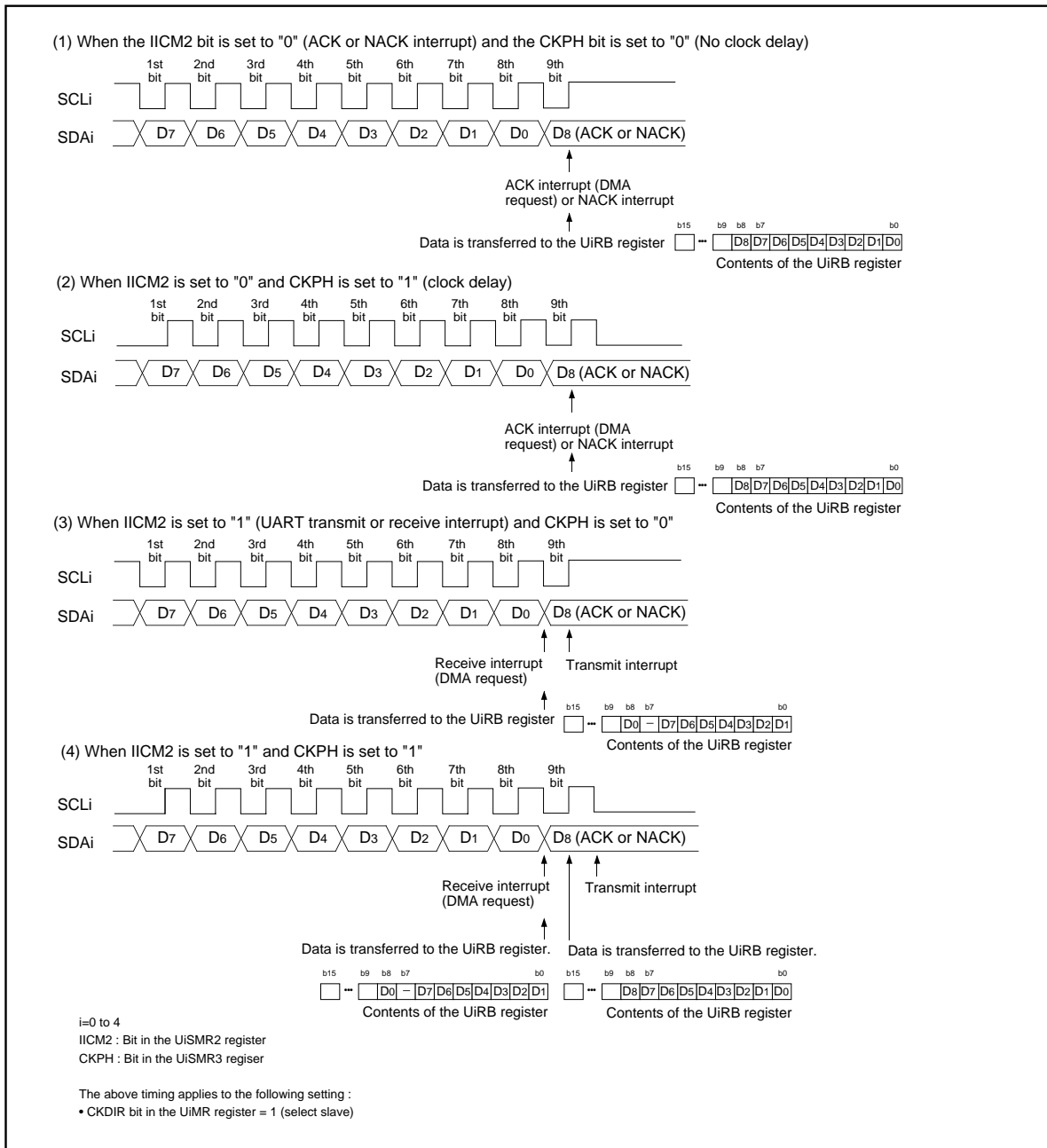


Figure 16.20 UIRB Register Transfer and Interrupt Timings

Table 16.15 Pin Settings in I²C Mode (1)

Port	Function	Setting		
		PS0 Register	PSL0 Register	PD6 Register
P62	SCL0 output	PS0_2=1	PSL0_2=0	-
	SCL0 input	PS0_2=0	-	PD6_2=0
P63	SDA0 output	PS0_3=1	-	-
	SDA0 input	PS0_3=0	-	PD6_3=0
P66	SCL1 output	PS0_6=1	PSL0_6=0	-
	SCL1 input	PS0_6=0	-	PD6_6=0
P67	SDA1 output	PS0_7=1	-	-
	SDA1 input	PS0_7=0	-	PD6_7=0

Table 16.16 Pin Settings (2)

Port	Function	Setting			
		PS1 Register	PSL1 Register	PSC Register	PD7 Register
P70 ⁽¹⁾	SDA2 output	PS1_0=1	PSL1_0=0	PSC_0=0	-
	SDA2 input	PS1_0=0	-	-	PD7_0=0
P71 ⁽¹⁾	SCL2 output	PS1_1=1	PSL1_1=0	PSC_1=0	-
	SCL2 input	PS1_1=0	-	-	PD7_1=0

NOTES:

1. P70 and P71 are ports for the N-channel open drain output.

Table 16.17 Pin Settings (3)

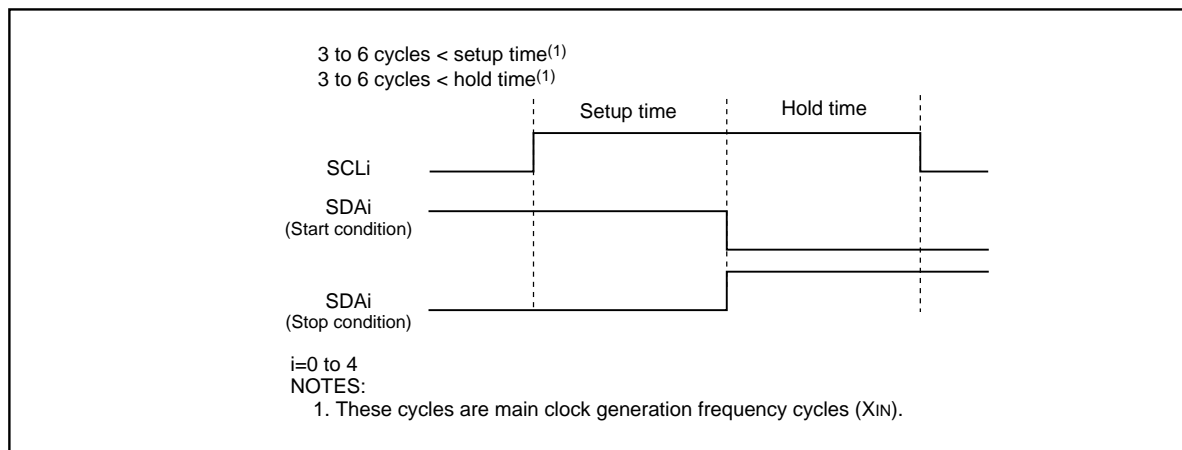
Port	Function	Setting		
		PS3 Register ⁽¹⁾	PSL3 Register	PD9 Register ⁽¹⁾
P91	SCL3 output	PS3_1=1	PSL3_1=0	-
	SCL3 input	PS3_1=0	-	PD9_1=0
P92	SDA3 output	PS3_2=1	PSL3_2=0	-
	SDA3 input	PS3_2=0	-	PD9_2=0
P96	SDA4 output	PS3_6=1	-	-
	SDA4 input	PS3_6=0	-	PD9_6=0
P97	SCL4 output	PS3_7=1	PSL3_7=0	-
	SCL4 input	PS3_7=0	-	PD9_7=0

NOTES:

1. Set the PD9 and PS3 registers immediately after the PRC2 bit in the PRCR register is set to "1" (write enable). Do not generate an interrupt or a DMA transfer between the instruction to set to the PRC2 bit to "1" and the instruction to set the PD9 and PS3 registers.

16.3.1 Detecting Start Condition and Stop Condition

The microcomputer detects either a start condition or stop condition. The start condition detect interrupt is generated when the SCL_i (i=0 to 4) pin is held high ("H") and the SDA_i pin changes high ("H") to low ("L"). The stop condition detect interrupt is generated when the SCL_i pin is held high ("H") and the SDA_i pin changes low ("L") to high ("H"). The start condition detect interrupt shares interrupt control registers and vectors with the stop condition detect interrupt. The BBS bit in the UiSMR register determines which interrupt is requested.

**Figure 16.21 Start Condition or Stop Condition Detect**

16.3.2 Start Condition or Stop Condition Output

The start condition is generated when the STAREQ bit in the UiSMR4 register (i=0 to 4) is set to "1" (start). The restart condition is generated when the RSTAREQ bit in the UiSMR4 register is set to "1" (start). The stop condition is generated when the STPREQ bit in the UiSMR4 is set to "1" (start).

The start condition is output when the STAREQ bit is set to "1" and the STSPSEL bit in the UiSMR4 register is set to "1" (start or stop condition generation circuit selected). The restart condition is output when the RSTAREQ bit and STSPSEL bit are set to "1". The stop condition is output when the STPREQ bit and the STSPSEL bit are set to "1".

When the start condition, stop condition or restart condition is output, do not generate an interrupt between the instruction to set the STAREQ bit, STPREQ bit or RSTAREQ bit to "1" and the instruction to set the STSPSEL bit to "1". When the start condition is output, set the STAREQ bit to "1" before the STSPSEL bit is set to "1".

Table 16.18 lists function of the STSPSEL bit. Figure 16.22 shows functions of the STSPSEL bit.

Table 16.18 STSPSEL Bit Function

Function	STSPSEL = 0	STSPSEL = 1
Start condition and stop condition output	Program with a port determines how the start condition or stop condition is output	The STAREQ bit, RSTAREQ bit and STPREQ bit determine how the start condition or stop condition is output
Timing to generate a start condition and stop condition interrupt request	The start condition and stop condition are detected	Start condition and stop condition generation are completed

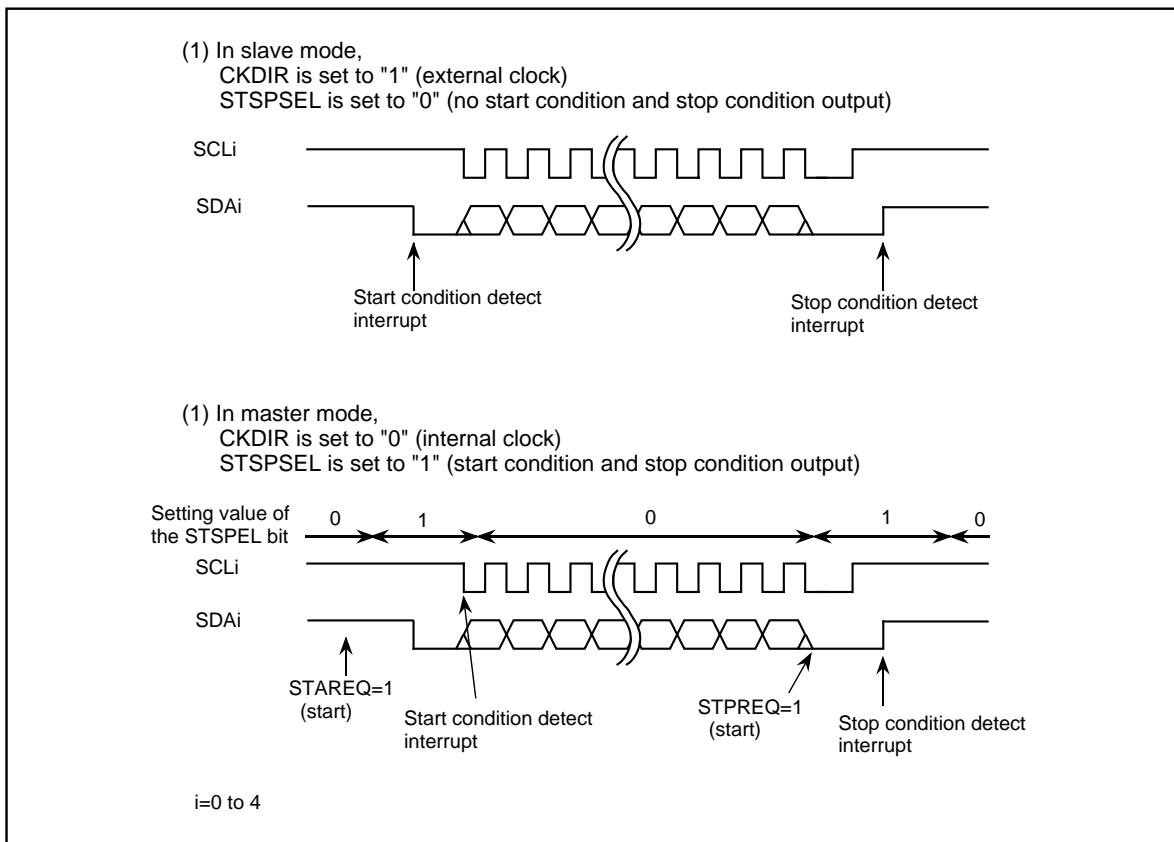


Figure 16.22 STSPSEL Bit Function

16.3.3 Arbitration

The ABC bit in the UiSMR register (i=0 to 4) determines an update timing for the ABT bit in the UiRB register. On the rising edge of SCLi, the microcomputer determines whether a transmit data matches data input to the SDAi pin.

When the ABC bit is set to "0" (update per bit), the ABT bit is set to "1" as soon as a data discrepancy is detected. The ABT bit is set to "0" if not detected. When the ABC bit is set to "1", the ABT bit is set to "1" (detected-arbitration is lost) on the falling edge of the ninth bit of the transfer clock if any discrepancy is detected. When the ABT bit is updated per byte, set the ABT bit to "0" (not detected-arbitration is won) between an ACK detection in the first byte data and the next byte data to be transferred. When the ALS bit in the UiSMR2 register is set to "1" (SDA output stop enabled), the arbitration lost occurs. As soon as the ABT bit is set to "1", the SDAi pin is placed in a high-impedance state.

16.3.4 Transfer Clock

The transfer clock transmits and receives data as is shown in Figure 16.22

The CSC bit in the UiSMR2 register (i=0 to 4) synchronizes an internally generated clock (internal SCLi) with the external clock applied to the SCLi pin. When the CSC bit is set to "1" (clock synchronous enabled) and the internal SCLi is held high ("H"), the internal SCLi become low ("L") if signal input to the SCLi pin is on the falling edge. Value of the UiBRG register is reloaded to start counting for low level. A counter stops when the SCLi pin is held "L" and then the internal SCLi changes "L" to "H". Counting is resumed when the SCLi pin become "H". The transfer clock of UARTi is equivalent to the AND for signals from the internal SCLi and the SCLi pin.

The transfer clock is synchronized between a half cycle before the falling edge of first bit of the internal SCLi and the rising edge of the ninth bit. Select the internal clock as the transfer clock while the CSC bit is set to "1".

The SWC bit in the UiSMR2 register determines whether the SCLi pin is fixed to output an "L" signal on the falling edge of the ninth cycle of the transfer clock or not.

When the SCLHI bit in the UiSMR4 register is set to "1" (enabled), a SCLi output stops when a stop condition is detected (high-impedance).

When the SWC2 bit in the UiSMR2 register is set to "1" (0 output), the SCLi pin forcibly outputs an "L" signal while transmitting and receiving. The fixed "L" signal applied to the SCLi pin is cancelled by setting the SWC2 bit to "0" (transfer clock) and the transfer clock is input to and output from the SCLi pin.

When the CKPH bit in the UiSMR3 register is set to "1" and the SWC9 bit in the UiSMR4 register is set to "1" (SCL "L" hold enabled), the SCLi pin is fixed to output an "L" signal on the next falling edge after the ninth bit of the clock. The fixed "L" signal applied to the SCLi pin is cancelled by setting the SWC9 bit to "0" (SCL "L" hold disabled).

16.3.5 SDA Output

Values in bits 7 to 0 (D7 to D0) in the UiTB register (i=0 to 4) are output in descending order from D7. The ninth bit (D8) is ACK or NACK.

Set the default value of SDAi transmit output when the IICM bit is set to "1" (I²C mode) and the SMD2 to SMD0 bits in the UiMR register are set to "0002" (serial I/O disabled).

The DL2 to DL0 bits in the UiSMR3 register determine no delay in the SDAi output or a delay of 2 to 8 UiBRG register count source cycles.

When the SDHI bit in the UiSMR2 register is set to "1" (SDA output disabled), the SDAi pin is forcibly placed in a high-impedance state. Do not set in the SDHI bit on the rising edge of the URTi transfer clock. The ABT bit in the UiRB register may be set to "1" (detected).

16.3.6 SDA Input

When the IICM2 bit in the UiSMR2 register (i=0 to 4) is set to "0", the first eight bits of received data are stored into bits 7 to 0 (D7 to D0) in the UiRB register. The ninth bit (D8) is ACK or NACK.

When the IICM2 bit is set to "1", the first seven bits (D7 to D1) of received data are stored into bits 6 to 0 in the UiRB register. Store the eighth bit (D0) into bit 8 in the UiRB register.

If the IICM bit in the UiSMR register is set to "1" and the CKPH bit is set to "1", the same data as that of when setting the IICM2 bit to "0" can be read. To read the data, read the UiRB register after the rising edge of the ninth bit of the transfer clock.

16.3.7 ACK, NACK

When the STPSEL bit in the UiSMR4 register (i=0 to 4) is set to "0" (serial I/O circuit selected) and the ACKC bit in the UiSMR4 register is set to "1" (ACK data output), the SDAi pin outputs the value set in the ACKD bit.

If the IICM2 bit is set to "0", the NACK interrupt request is generated when the SDAi pin is held high ("H") on the rising edge of the ninth bit of the transfer clock. The ACK interrupt request is generated when the SDAi pin is held low ("L") on the rising edge of the ninth bit of the transfer clock.

When ACK is selected to generate a DMA request, the DMA transfer is activated by an ACK detection.

16.3.8 Transmit and Receive Reset

When the STC bit in the UiSMR2 register is set to "1" (UARTi initialization enabled) and a start condition is detected,

- the transmit shift register is reset and the content of the UiTB register is transferred to the transmit shift register. The first bit starts transmitting when the next clock is input. UARTi output value remains unchanged between when clock is input and when data of the first bit is output. The value remains the same value as when start condition was detected.
- the receive shift register is reset and the first bit starts receiving when the next clock is input.
- the SWC bit is set to "1" (SCL wait output enabled). The SCLi pin becomes low ("L") on the falling edge of the ninth bit of the transfer clock.

If UARTi transmission and reception are started with this function, the TI bit in the UiC1 register remains unchanged. Select the external clock as the transfer clock when using this function.

16.4 Special Mode 2

In special mode 2, serial communication between one or multiple masters and multiple slaves is available. The \overline{SSi} input pin ($i=0$ to 4) controls the serial bus communication. Table 16.19 lists specifications of special mode 2. Table 16.20 lists registers to be used and settings. Tables 16.20 to 16.22 list pin settings.

Table 16.19. Special Mode 2 Specifications

Item	Specification
Transfer Data Format	Transfer data : 8 bits long
Transfer Clock	The CKDIR bit in the UiMR register ($i=0$ to 4) is set to "0" (internal clock selected) : $f_j/2(m+1)$ $f_j = f_1, f_8, f_{2n}^{(1)}$ m : setting value of the UiBRG register 00 ₁₆ to FF ₁₆ The CKDIR bit to "1" (external clock selected) : input clock from the CLKi pin
Transmit/Receive Control	\overline{SSi} input pin function
Transmit Start Condition	<ul style="list-style-type: none"> To start transmitting, the following requirements must be met⁽²⁾ : <ul style="list-style-type: none"> - Set the TE bit in the UiC1 register to "1" (transmit enable) - Set the TI bit in the UiC1 register to "0" (data in the UiTB register)
Receive Start Condition	<ul style="list-style-type: none"> To start receiving, the following requirement must be met⁽²⁾ : <ul style="list-style-type: none"> - Set the RE bit in the UiC1 register to "1" (receive enable) - Set the TE bit to "1" (receive enable) - Set the TI bit to "0" (data in the UiTB register)
Interrupt Request Generation Timing	<ul style="list-style-type: none"> Transmit interrupt timing can be selected from the followings: <ul style="list-style-type: none"> - The UiIRS bit in the UiC1 register is set to "0" (no data in a transmit buffer) : when data is transferred from the UiTB register to the UAR_{Ti} transmit register (transmission started) - The UiIRS register is set to "1" (transmission completed): when data transmission from UAR_{Ti} transfer register is completed Receive interrupt timing When data is transferred from the UAR_{Ti} receive register to the UiRB register (reception completed)
Error Detection	<ul style="list-style-type: none"> Overrun error⁽³⁾ This error occurs when the seventh bit of the next received data is read before reading the UiRB register Fault error In master mode, the fault error occurs an "L" signal is applied to the \overline{SSi} pin
Selectable Function	<ul style="list-style-type: none"> CLK polarity Select from the rising edge or falling edge of the transfer clock when transferred data is output and input LSB first / MSB first Data is transmitted or received in either bit 0 or in bit 7 Continuous receive mode Reception is enabled simultaneously by reading the UiRB register Serial data logic inverse This function inverses transmitted or received data logically TxD, RxD I/O polarity Inverse TxD pin output and RxD pin input are inverted. All I/O data levels are also inverted Clock phase Select from one of 4 combinations of transfer data polarity and phases \overline{SSi} input pin function Output pin is placed in a high-impedance state to avoid data conflict between master and other masters or slaves

NOTES:

- The CNT3 to CNT0 bits in the TCSPR register select no division ($n=0$) or divide-by- $2n$ ($n=1$ to 15).
- To start transmission/reception when selecting the external clock, these conditions must be met after the CKPOL bit in the UiC0 register is set to "0" (data is transmitted on the falling edge of the transfer clock and data is received on the rising edge) and the CLKi pin is held high ("H"), or when the CKPOL bit is set to "1" (Data is transmitted on the rising edge of the transfer clock and data is received on the falling edge) and the CLKi pin is held low ("L").
- If an overrun error occurs, the UiRB register is indeterminate. The IR bit in the SiRIC register does not change to "1" (interrupt requested).

Table 16.20. Registers To Be Used and Settings in Special Mode 2

Register	Bit	Function
UiTB	0 to 7	Set transmit data
UiRB	0 to 7	Received data can be read
	OER	Overflow error flag
UiBRG	0 to 7	Set bit rate
UiMR	SMD2 to SMD0	Set to "0012"
	CKDIR	Set to "0" in master mode or "1" in slave mode
	IOPOL	Set to "0"
UiC0	CLK0, CLK1	Select count source for the UiBRG register
	CRS	Disabled since CRD = 1
	TXEPT	Transfer register empty flag
	CRD	Set to "1"
	NCH	Select the output format of the TxDi pin
	CKPOL	Clock phase can be set by the combination of the CKPOL bit and the CKPH bit in the UiSMR3 register
	UFORM	Select either LSB first or MSB first
UiC1	TE	Set to "1" to enable data transmission and reception
	TI	Transfer buffer empty flag
	RE	Set to "1" to enable data reception
	RI	Reception complete flag
	UiIRS	Select how the UARTi transmit interrupt is generated
	UiRRM	Set to "1" to enable continuous receive mode
	UiLCH, SCLKSTPB	Set to "0"
UiSMR	0 to 7	Set to "0016"
UiSMR2	0 to 7	Set to "0016"
UiSMR3	SSE	Set to "1"
	CKPH	Clock phase can be set by the combination of the CKPH bit and the CKPOL bit in the UiC0 register
	DINC	Set to "0" in master mode or "1" in slave mode
	NODC	Set to "0"
	ERR	Fault error flag
	5 to 7	Set to "0002"
UiSMR4	0 to 7	Set to "0016"
IFSR	IFSR6, IFSR7	Select how fault error occurs

i=0 to 4

Table 16.21 Pin Settings in Special Mode 2 (1)

Port	Function	Setting		
		PS0 Register	PSL0 Register	PD6 Register
P60	SS0 input	PS0_0=0	–	PD6_0=0
P61	CLK0 input (slave)	PS0_1=0	–	PD6_1=0
	CLK0 output (master)	PS0_1=1	–	–
P62	RxD0 input (master)	PS0_2=0	–	PD6_2=0
	STxD0 output (slave)	PS0_2=1	PSL0_2=1	–
P63	TxD0 output (master)	PS0_3=1	–	–
	SRxD0 input (slave)	PS0_3=0	–	PD6_3=0
P64	SS1 input	PS0_4=0	–	PD6_4=0
P65	CLK1 input (slave)	PS0_5=0	–	PD6_5=0
	CLK1 output (master)	PS0_5=1	–	–
P66	RxD1 input (master)	PS0_6=0	–	PD6_6=0
	STxD1 output (slave)	PS0_6=1	PSL0_6=1	–
P67	TxD1 output (master)	PS0_7=1	–	–
	SRxD1 input (slave)	PS0_7=0	–	PD6_7=0

Table 16.21 Pin Settings (2)

Port	Function	Setting			
		PS1 Register	PSL1 Register	PSC Register	PD7 Register
P70 ⁽¹⁾	TxD2 output (master)	PS1_0=1	PSL1_0=0	PSC_0=0	–
	SRxD2 input (slave)	PS1_0=0	–	–	PD7_0=0
P71 ⁽¹⁾	RxD2 input (master)	PS1_1=0	–	–	PD7_1=0
	STxD2 output (slave)	PS1_1=1	PSL1_1=1	PSC_1=0	–
P72	CLK2 input (slave)	PS1_2=0	–	–	PD7_2=0
	CLK2 output (master)	PS1_2=1	PSL1_2=0	PSC_2=0	–
P73	SS2 input	PS1_3=0	–	–	PD7_3=0

NOTES:

1. P70 and P71 are ports for the N-channel open drain output.

Table 16.23 Pin Settings (3)

Port	Function	Setting		
		PS3 Register ⁽¹⁾	PSL3 Register	PD9 Register ⁽¹⁾
P90	CLK3 input (slave)	PS3_0=0	–	PD9_0=0
	CLK3 output (master)	PS3_0=1	–	–
P91	RxD3 input (master)	PS3_1=0	–	PD9_1=0
	STxD3 output (slave)	PS3_1=1	PSL3_1=1	–
P92	TxD3 output (master)	PS3_2=1	PSL3_2=0	–
	SRxD3 input (slave)	PS3_2=0	–	PD9_2=0
P93	SS3 input	PS3_3=0	PSL3_3=0	PD9_3=0
P94	SS4 input	PS3_4=0	PSL3_4=0	PD9_4=0
P95	CLK4 input (slave)	PS3_5=0	PSL3_5=0	PD9_5=0
	CLK4 output (master)	PS3_5=1	–	–
P96	TxD4 output (master)	PS3_6=1	–	–
	SRxD4 input (slave)	PS3_6=0	PSL3_6=0	PD9_6=0
P97	RxD4 input (master)	PS3_7=0	–	PD9_7=0
	STxD4 output (slave)	PS3_7=1	PSL3_7=1	–

NOTES:

1. Set the PD9 and PS3 registers immediately after the PRC2 bit in the PRCR register is set to "1" (write enable). Do not generate an interrupt or a DMA transfer between the instruction to set to the PRC2 bit to "1" and the instruction to set the PD9 and PS3 registers.

16.4.1 \overline{SS}_i Input Pin Function ($i=0$ to 4)

When the SSE bit in the UiSMR3 register is set to "1" (\overline{SS} function enabled), the \overline{SS}_i input pin function is selected, activating the pin function.

The DINC bit in the UiSMR3 register determines which microcomputer performs as master or slave. When multiple microcomputers perform as the masters (multi-master system), the \overline{SS}_i pin setting determines which master microcomputer is active and when.

16.4.1.1 When Setting the DINC Bit to "1" (Slave Mode)

When an "H" signal is applied to the \overline{SS}_i pin, the STxDi and SRxDi pins are placed in a high-impedance state and the transfer clock input to the CLKi pin is ignored. When a low-level signal ("L") is applied to the \overline{SS}_i input pin, the transfer clock input is valid and serial communication is enabled.

16.4.1.2 When Setting the DINC Bit to "0" (Master Mode)

When an "H" signal is applied to the \overline{SS}_i pin, serial communication is available due to transmission privilege. The master outputs the transfer clock. When an "L" signal is applied to the \overline{SS}_i pin, it indicates that another master is active and TxDi, RxDi and CLKi pins are placed in a high-impedance state. Moreover, a fault error occurs and the IR bit in the BCNiIC register is set to "1" (interrupt requested). The ERR bit in the UiSMR3 register indicates whether a fault error occurs.

In master mode, software interrupt numbers 39, 40 and 41 are used for the fault error interrupt. The fault error interrupt is generated when the ERR bit changes "0" to "1". The fault error interrupt of UART0 and of UART3 share an interrupt vector. The fault error interrupt of UART1 and of UART4 share an interrupt vector. The IFSR6 and IFSR7 bits in the IFSR register determine which fault error interrupt is used.

Communication is not terminated even if a fault error is generated while communicating. To stop communication, the SMD 2 to SMD0 bit in the UiMR register is set to "0002" (serial I/O disabled).

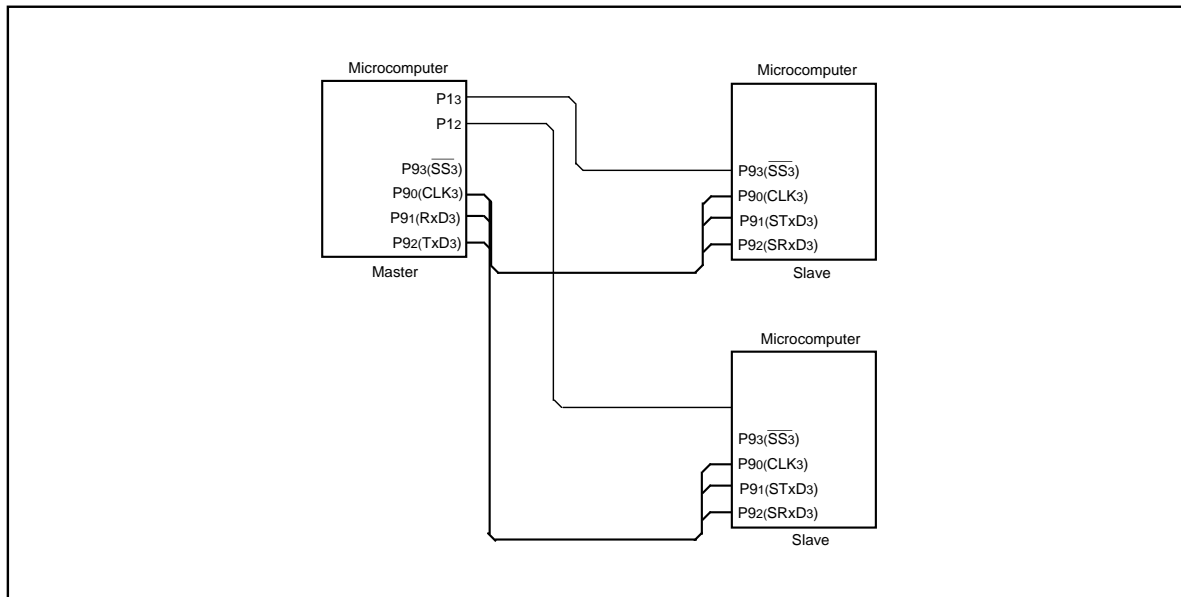


Figure 16.23 Serial Bus Communication Control with SS Pin

16.4.2 Clock Phase Setting Function

The CKPH bit in the UiSMR3 register ($i=0$ to 4) and the CKPOL bit in the UiC0 register select one of four combinations of transfer clock polarity and phases.

The transfer clock phase and polarity must be the same between the master and the slave involved in the transfer.

16.4.2.1 When setting the DINC Bit to "0" (Master (Internal Clock))

Figure 16.24 shows transmit and receive timing.

16.4.2.2 When Setting the DINC Bit to "1" (Slave (External Clock))

When the CKPH bit is set to "0" (no clock delay) and the \overline{SS}_i input pin is held high ("H"), the STxDi pin is placed in a high-impedance state. When the \overline{SS}_i input pin becomes low ("L"), conditions to start a serial transfer are met, but output is indeterminate. The serial transmission is synchronized with the transfer clock. Figure 16.25 shows the transmit and receive timing.

When the CKPH bit is set to "1" (clock delay) and the \overline{SS}_i input pin is held high ("H"), the STxDi pin is placed in a high-impedance state. When the \overline{SS}_i pin becomes low ("L"), the first data is output. The serial transmission is synchronized with the transfer clock. Figure 16.26 shows the transmit and receive timing.

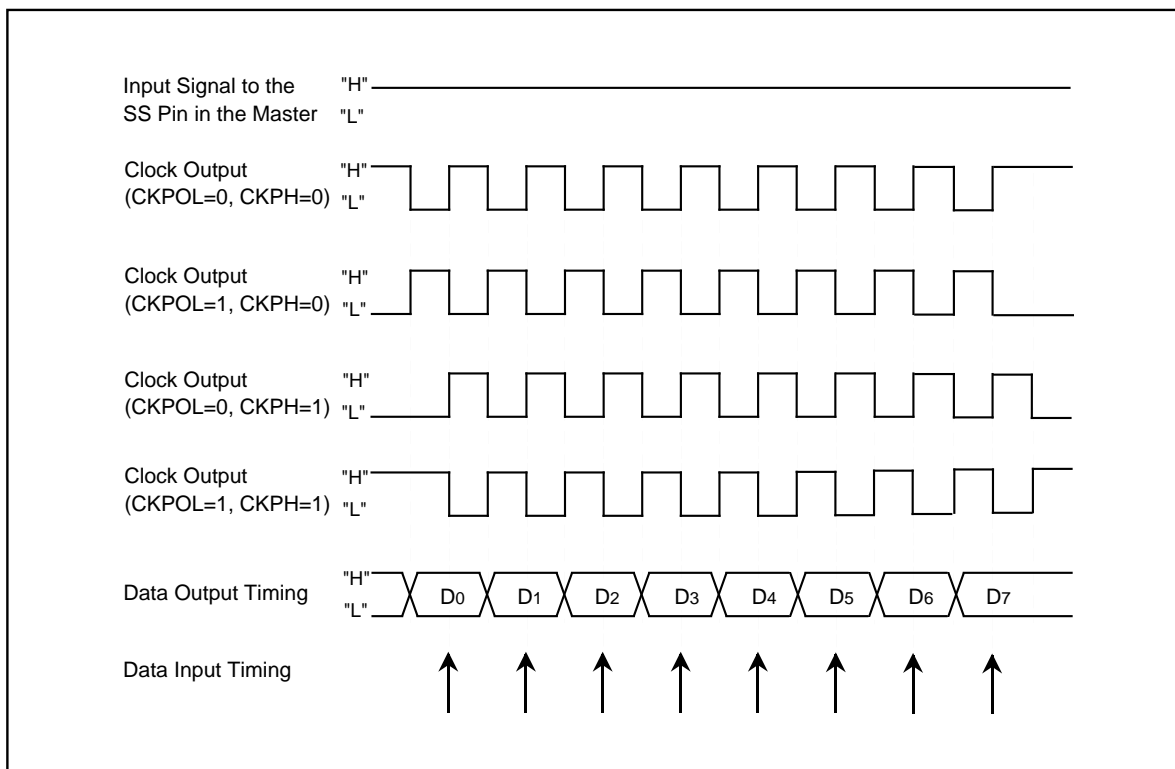


Figure 16.24 Transmit and Receive Timing in Master Mode (Internal Clock)

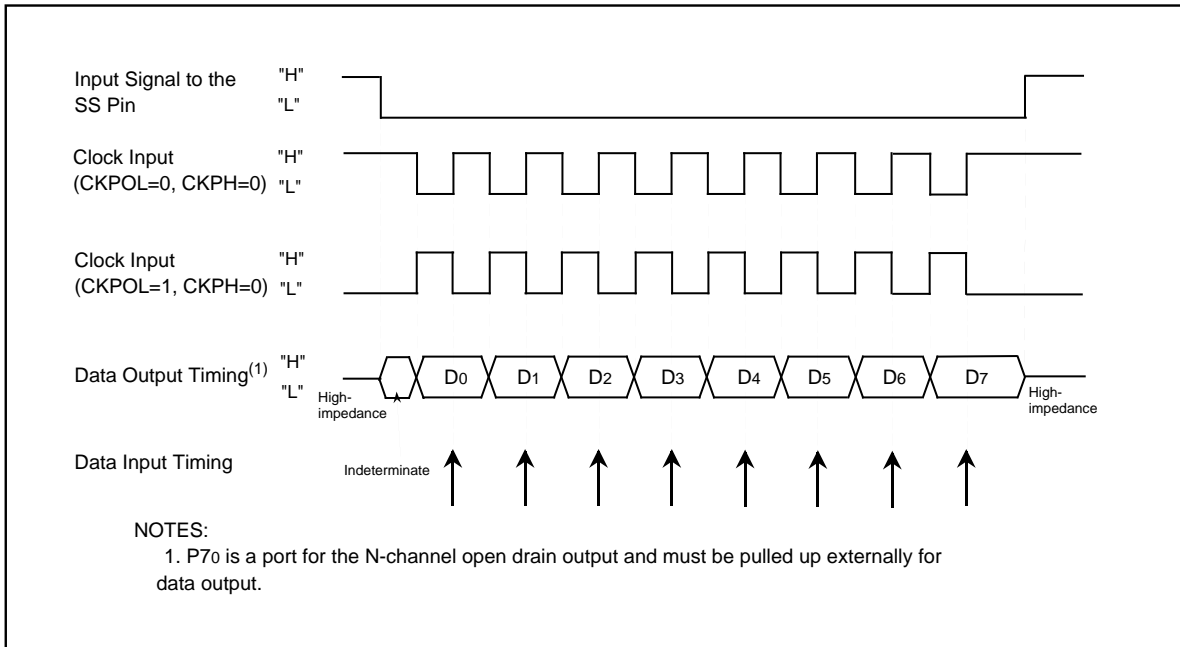


Figure 16.25 Transmit and Receive Timing in Slave Mode (External Clock) (CKPH=0)

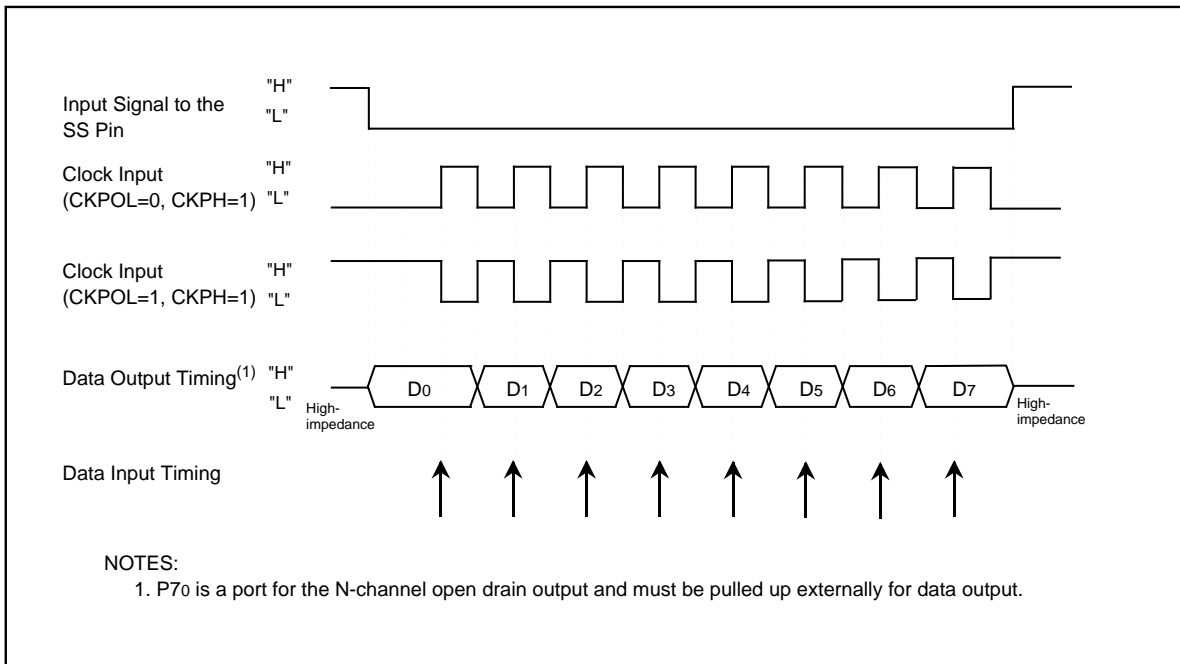


Figure 16.26 Transmit and Receive Timing in Slave Mode (External Clock) (CKPH=1)

16.5 Special Mode 3 (GCI Mode)

In GCI mode, the external clock is synchronized with the transfer clock used in the clock synchronous serial I/O mode.

Table 16.24 lists specifications of GCI mode. Table 16.25 lists registers to be used and settings. Tables 16.25 to 16.27 list pin settings.

Table 16.24 GCI Mode Specifications

Item	Specification
Transfer Data Format	Transfer data : 8 bits long
Transfer Clock	The CKDIR bit in the UiMR register (i=0 to 4) is set to "1" (external clock selected): an input from the CLKi pin
Clock Synchronization Function	The CTSi pin inputs a trigger
Transmit/Receive Start Conditions	When a trigger signal is applied to the CTSi pin under the following conditions: <ul style="list-style-type: none"> • Set the TE bit in the UiC1 register to "1" (transmit enable) • Set the RE bit in the UiC1 register to "1" (receive enable) • Set the TI bit in the UiC1 register to "0" (data in UiTB register)
Interrupt Request Generation Timing	Transmit interrupt timing can be selected from the followings: <ul style="list-style-type: none"> • The UiIRS bit in the UiC1 register is set to "0" (UiTB register empty) : when data is transferred from the UiTB register to the UARTi transmit register (transmission started) • The UiIRS bit is set to "1" (transmit completed): when a data transmission from the UARTi transfer register is completed Receive interrupt timing when data is transferred from the UARTi receive register to the UiRB register (reception completed)
Error Detection	Overrun error ⁽¹⁾ This error occurs when the seventh bit of the next received data is read before reading the UiRB register.

NOTES:

1. If an overrun error occurs, the UiRB register is indeterminate. The IR bit in the SiRIC register does not change to "1" (interrupt requested).

Table 16.25 Registers To Be Used and Settings in GCI Mode

Register	Bit	Function
UiTB	0 to 7	Set transmit data
UiRB	0 to 7	Received data
	OER	Overflow error flag
UiBRG	0 to 7	Set to "0016"
UiMR	SMD2 to SMD0	Set to "0012"
	CKDIR	Set to "1"
	IOPOL	Set to "0"
UiC0	CLK1 to CLK0	Set to "002"
	CRS	Disabled because CRD = 1
	TXEPT	Transfer register empty flag
	CRD	Set to "1"
	NCH	Select the output format of the TxDi pin
	CKPOL	Set to "0"
	UFORM	Set to "0"
UiC1	TE	Set to "1" to enable data transmission and reception
	TI	Transfer buffer empty flag
	RE	Set to "1" to enable data reception
	RI	Reception complete flag
	UiIRS	Select how the UARTi transmit interrupt is generated
	UiRRM, UiLCH	Set to "0"
	SCLKSTPB	Set to "0"
UiSMR	0 to 6	Set to "00000002"
	SCLKDIV	See Table 16.29
UiSMR2	0 to 6	Set to "00000002"
	SU1HIM	See Table 16.29
UiSMR3	0 to 2	Set to "0002"
	NODC	Set to "0"
	4 to 7	Set to "00002"
UiSMR4	0 to 7	Set to "0016"

i=0 to 4

Table 16.26 Pin Settings in CGI Mode (1)

Port	Function	Setting		
		PS0 Register	PSL0 Register	PD6 Register
P60	CTS0 input ⁽¹⁾	PS0_0=0	–	PD6_0=0
P61	CLK0 input	PS0_1=0	–	PD6_1=0
P62	RxD0 input	PS0_2=0	–	PD6_2=0
P63	TxD0 output	PS0_3=1	–	–
P64	CTS1 input ⁽¹⁾	PS0_4=0	–	PD6_4=0
P65	CLK1 input	PS0_5=0	–	PD6_5=0
P66	RxD1 input	PS0_6=0	–	PD6_6=0
P67	TxD1 output	PS0_7=1	–	–

NOTES:

1. CTS input is used to input a trigger.

Table 16.27 Pin Settings (2)

Port	Function	Setting			
		PS1 Register	PSL1 Register	PSC Register	PD7 Register
P70 ⁽¹⁾	TxD2 output	PS1_0=1	PSL1_0=0	PSC_0=0	–
P71 ⁽¹⁾	RxD2 input	PS1_1=0	–	–	PD7_1=0
P72	CLK2 input	PS1_2=0	–	–	PD7_2=0
P73	CTS2 input ⁽²⁾	PS1_3=0	–	–	PD7_3=0

NOTES:

1. P70 and P71 are ports for the N-channel open drain output.
2. CTS input is used to input a trigger.

Table 16.28 Pin Settings (3)

Port	Function	Setting		
		PS3 Register ⁽¹⁾	PSL3 Register	PD9 Register ⁽¹⁾
P90	CLK3 input	PS3_0=0	–	PD9_0=0
P91	RxD3 input	PS3_1=0	–	PD9_1=0
P92	TxD3 output	PS3_2=1	PSL3_2=0	–
P93	CTS3 input ⁽²⁾	PS3_3=0	PSL3_3=0	PD9_3=0
P94	CTS4 input ⁽²⁾	PS3_4=0	PSL3_4=0	PD9_4=0
P95	CLK4 input	PS3_5=0	PSL3_5=0	PD9_5=0
P96	TxD4 output	PS3_6=1	–	–
P97	RxD4 input	PS3_7=0	–	PD9_7=0

NOTES:

1. Set the PD9 and PS3 registers immediately after the PRC2 bit in the PRCR register is set to "1" (write enable). Do not generate an interrupt or a DMA transfer between the instruction to set to the PRC2 bit to "1" and the instruction to set the PD9 and PS3 registers.
2. CTS input is used to input a trigger.

To generate the internal clock synchronized with the external clock, first set the SU1HIM bit in the UiSMR2 register ($i=0$ to 4) and the SCLKDIV bit in the UiSMR register to values shown in Table 16.29. Then apply a trigger signal to the CTSi pin. Either the same clock cycle as the external clock or external clock divided by two can be selected as the transfer clock. The SCLKSTPB bit in the UiC1 register controls the transfer clock. Set the SCLKSTPB bit accordingly, to start or stop the transfer clock during an external clock operation. Figure 16.27 shows an example of the clock-divided synchronous function.

Table 16.29 Clock-Divided Synchronous Function Select

SCLKDIV Bit in UiSMR Register	SU1HIM Bit in UiSMR2 Register	Clock-Divided Synchronous Function	Example of Waveform
0	0	Not synchronized	-
0	1	Same division as the external clock	A in Figure 16.27
1	0 or 1	Same division as the external clock divided by 2	B in Figure 16.27

$i=0$ to 4

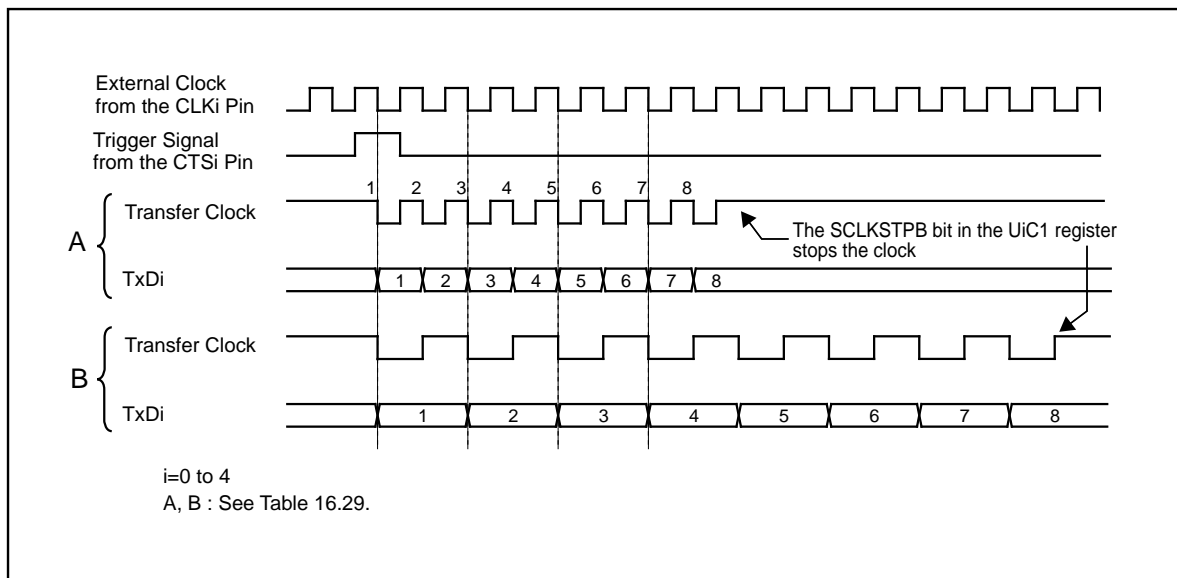


Figure 16.27 Clock-Divided Synchronous Function

16.6 Special Mode 4 (IE Mode)

In IE mode, devices connected with the IEBus can communicate in UART mode.

Table 16.30 lists registers to be used and settings. Tables 16.30 to 16.32 list pin settings.

Table 16.30. Registers To Be Used and Settings in IE Mode

Register	Bit	Function
UiTB	0 to 8	Set transmit data
UiRB	0 to 8	Received data can be read
	OER, FER, PER, SUM	Error flags
UiBRG	0 to 7	Set bit rate
UiMR	SMD2 to SMD0	Set to "1102"
	CKDIR	Select the internal clock or external clock
	STPS	Set to "0"
	PRY	Disabled because PRYE=0
	PRYE	Set to "0"
	IOPOL	Select TxD and RxD I/O polarity
UiC0	CLK1 to CLK0	Select the count source for the UiBRG register
	CRS	Disabled because CRD=1
	TXEPT	Transfer register empty flag
	CRD	Set to "1"
	NCH	Select output format of the TxDi pin
	CKPOL	Set to "0"
	UFORM	Set to "0"
UiC1	TE	Set to "1" to enable data transmission
	TI	Transfer buffer empty flag
	RE	Set to "1" to enable data reception
	RI	Reception complete flag
	UiIRS	Select how the UARTi transmit interrupt is generated
	UiRRM, UiLCH, SCLKSTPB	Set to "0"
UiSMR	0 to 3	Set to "00002"
	ABSCS	Select bus conflict detect sampling timing
	ACSE	Set to "1" to automatically clear the transmit enable bit
	SSS	Select transmit start condition
	SCLKDIV	Set to "0"
UiSMR2	0 to 7	Set to "0016"
UiSMR3	0 to 7	Set to "0016"
UiSMR4	0 to 7	Set to "0016"
IFSR	IFSR6, IFSR7	Select how the bus conflict interrupt occurs

i=0 to 4

Table 16.31 Pin Settings in IE Mode (1)

Port	Function	Setting		
		PS0 Register	PSL0 Register	PD6 Register
P61	CLK0 input	PS0_1=0	–	PD6_1=0
	CLK0 output	PS0_1=1	–	–
P62	RxD0 input	PS0_2=0	–	PD6_2=0
P63	TxD0 output	PS0_3=1	–	–
P65	CLK1 input	PS0_5=0	–	PD6_5=0
	CLK1 output	PS0_5=1	–	–
P66	RxD1 input	PS0_6=0	–	PD6_6=0
P67	TxD1 output	PS0_7=1	–	–

Table 16.32 Pin Settings (2)

Port	Function	Setting			
		PS1 Register	PSL1 Register	PSC Register	PD7 Register
P70 ⁽¹⁾	TxD2 output	PS1_0=1	PSL1_0=0	PSC_0=0	–
P71 ⁽¹⁾	RxD2 input	PS1_1=0	–	–	PD7_1=0
P72	CLK2 input	PS1_2=0	–	–	PD7_2=0
	CLK2 output	PS1_2=1	PSL1_2=0	PSC_2=0	–

NOTES:

1. P70 and P71 are ports for the N-channel open drain output.

Table 16.33 Pin Settings (3)

Port	Function	Setting		
		PS3 Register ⁽¹⁾	PSL3 Register	PD9 Register ⁽¹⁾
P90	CLK3 input	PS3_0=0	–	PD9_0=0
	CLK3 output	PS3_0=1	–	–
P91	RxD3 input	PS3_1=0	–	PD9_1=0
P92	TxD3 output	PS3_2=1	PSL3_2=0	–
P95	CLK4 input	PS3_5=0	PSL3_5=0	PD9_5=0
	CLK4 output	PS3_5=1	–	–
P96	TxD4 output	PS3_6=1	–	–
P97	RxD4 input	PS3_7=0	–	PD9_7=0

NOTES:

1. Set the PD9 and PS3 registers immediately after the PRC2 bit in the PRCR register is set to "1" (write enable). Do not generate an interrupt or a DMA transfer between the instruction to set to the PRC2 bit to "1" and the instruction to set the PD9 and PS3 registers.

If the output level of the TxDi pin (i=0 to 4) differs from the input level of the RxDi pin, an interrupt request is generated.

UART0 and UART3 are assigned software interrupt number 40. UART1 and UART4 are assigned number 41. When using the bus conflict detect function of UART0 or UART3, of UART1 or UART4, set the IFSR6 bit and the IFSR7 bit in the IFSR register accordingly.

When the ABSCS bit in the UiSMR register is set to "0" (rising edge of the transfer clock), it is determined, on the rising edge of the transfer clock, if the output level of the TxD pin and the input level of the RxD pin match. When the ABSCS bit is set to "1" (timer Aj underflow), it is determined when the timer Aj (timer A3 in UART0, timer A4 in UART1, timer A0 in UART2, timer A3 in UART3, the timer A4 in UART4) overflows. Use the timer Aj in one-shot timer mode.

When the ACSE bit in the UiSMR register is set to "1" (automatic clear at bus conflict) and the IR bit in the BCNiIC register to "1" (discrepancy detected), the TE bit is set to "0" (transmit disable).

When the SSS bit in the UiSMR register is set to "1" (synchronized with RxDi), the TxDi pin starts transmitting data on the falling edge of the RxDi pin. Figure 16.28 shows bits associated with the bus conflict detect function.

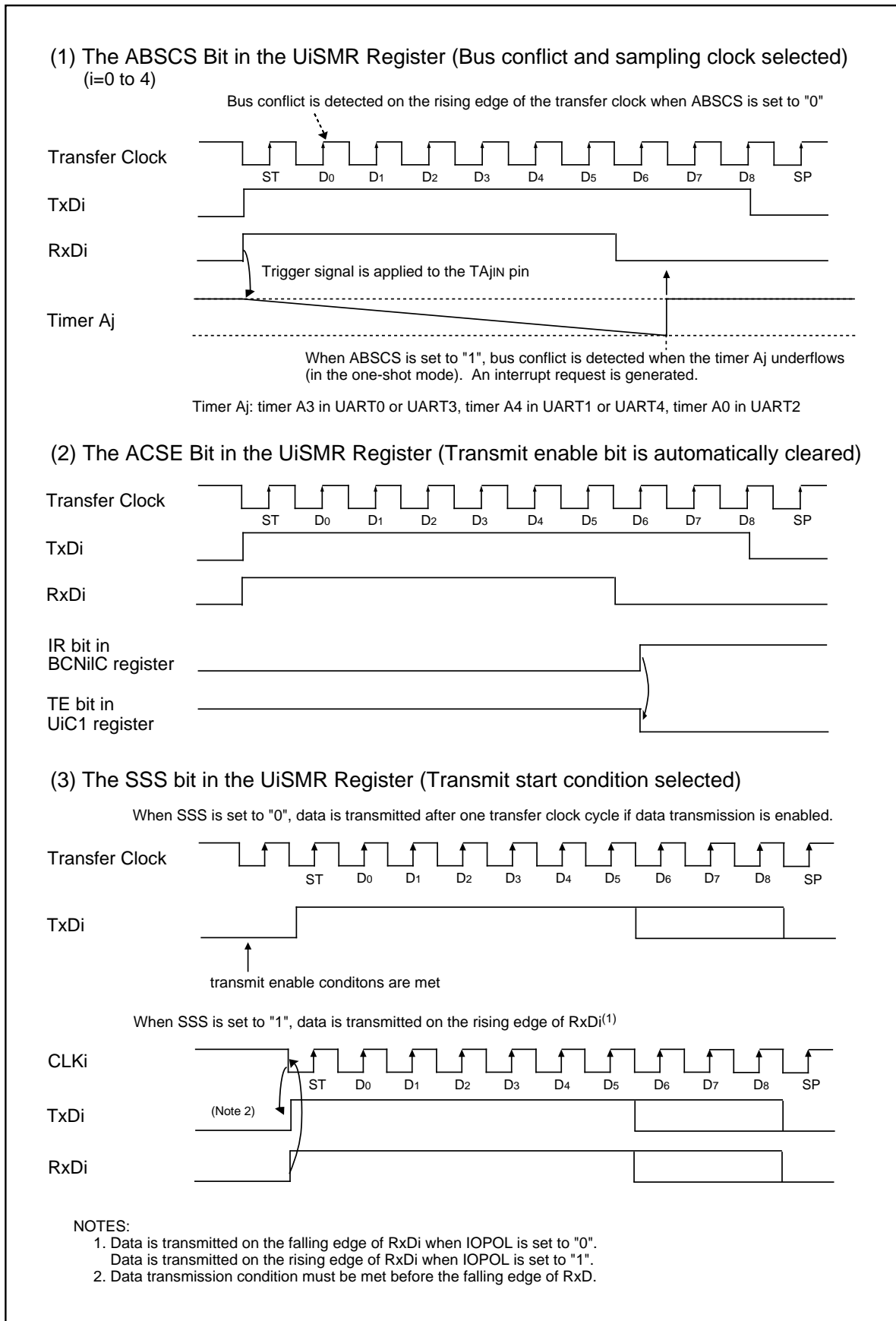


Figure 16.28 Bit Function Related Bus Conflict Detection

16.7 Special Mode 5 (SIM Mode)

In SIM mode, SIM interface devices can communicate in UART mode. Both direct and inverse formats are available and the TxDi pin (i=0 to 4) can output an "L" signal when a parity error is detected.

Table 16.34 lists specifications of SIM mode. Table 16.35 lists registers to be used and register settings in SIM mode. Tables 16.36 to 16.38 list the pin settings.

Table 16.34 SIM Mode Specifications

Item	Specification
Transfer Data Format	<ul style="list-style-type: none"> • Transfer data: 8-bit UART mode • One stop bit • In direct format <ul style="list-style-type: none"> Parity: Even Data logic: Direct Transfer format: LSB first • In inverse format <ul style="list-style-type: none"> Parity: Odd Data logic: Inverse Transfer format: MSB first
Transfer Clock	<p>The CKDIR bit in the UiMR register (i=0 to 4) is "0" (internal clock selected): $f_j/16(m+1)^{(1)}$ $f_j = f_1, f_8, f_{2n}^{(2)}$ m : setting value of the UiBRG register 00₁₆ to FF₁₆ Do not set the CKDIR bit to "1" (external clock selected)</p>
Transmit/Receive Control	The CRD bit in the UiC0 register is set to "1" (CTS, RTS function disabled)
Other Setting Items	The UiIRS bit in the UiC1 register is set to "1" (transmission completed)
Transmit Start Condition	<p>To start transmitting, the following requirements must be met:</p> <ul style="list-style-type: none"> • Set the TE bit in the UiC1 register to "1" (transmit enable) • Set the TI bit in the UiC1 register to "0" (data being in the UiTB register)
Receive Start Condition	<p>To start receiving, the following requirements must be met:</p> <ul style="list-style-type: none"> • Set the RE bit in the UiC1 register to "1" (receive enable) • Detect the start bit
Interrupt Request Generation Timing	<p>Transmit interrupt timing</p> <ul style="list-style-type: none"> • The UiIRS bit is set to "1" (transmission is completed): when data transmission from the UARTi transfer register is completed <p>Receive interrupt timing</p> <ul style="list-style-type: none"> • when data is transferred from the UARTi receive register to the UiRB register (reception completed)
Error Detection	<ul style="list-style-type: none"> • Overrun error⁽¹⁾ This error occurs when the eighth bit of the next data is received before reading the UiRB register • Framing error This error occurs when the number of the stop bit set is not detected • Parity error This error occurs when the number of "1" in parity bit and character bits differ from the number set. • Error sum flag The SUM bit is set to "1" when an overrun error, framing error or parity error occurs.

NOTES:

1. If an overrun error occurs, the UiRB register is indeterminate. The IR bit in the SiRIC register does not change to "1" (interrupt requested).
2. The CNT3 to CNT0 bits in the TCSPR register select no division (n=0) or divide-by-2n (n=1 to 15).

Table 16.35 Registers To Be Used and Settings

Register	Bit	Function
UiTB	0 to 7	Set transmit data
UiRB	0 to 7	Received data can be read
	OER, FER, PER, SUM	Error flags
UiBRG	0 to 7	Set bit rate
UiMR	SMD2 to SMD0	Set to "101 ₂ "
	CKDIR	Set to "0"
	STPS	Set to "0"
	PRY	Set to "1" for direct format or "0" for inverse format
	PRYE	Set to "1"
	IOPOL	Set to "0"
UiC0	CLK1 to CLK0	Select count source for the UiBRG register
	CRS	Disabled because CRD=1
	TXEPT	Transfer register empty flag
	CRD	Set to "1"
	NCH	Set to "1"
	CKPOL	Set to "0"
	UFORM	Set to "0" for direct format or "1" for inverse format
UiC1	TE	Set to "1" to enable data transmission
	TI	Transfer buffer empty flag
	RE	Set to "1" to enable data reception
	RI	Reception complete flag
	UiIRS	Set to "1"
	UiRRM	Set to "0"
	UiLCH	Set to "0" for direct format or "1" for inverse format
	UiERE	Set to "1"
UiSMR	0 to 3	Set to "00 ₁₆ "
UiSMR2	0 to 7	Set to "00 ₁₆ "
UiSMR3	0 to 7	Set to "00 ₁₆ "
UiSMR4	0 to 7	Set to "00 ₁₆ "

i=0 to 4

Table 16.36 Pin Settings in SIM Mode (1)

Port	Function	Setting		
		PS0 Register	PSL0 Register	PD6 Register
P62	RxD0 input	PS0_2=0	–	PD6_2=0
P63	TxD0 output	PS0_3=1	–	–
P66	RxD1 input	PS0_6=0	–	PD6_6=0
P67	TxD1 output	PS0_7=1	–	–

Table 16.37 Pin Settings (2)

Port	Function	Setting			
		PS1 Register	PSL1 Register	PSC Register	PD7 Register
P70 ⁽¹⁾	TxD2 output	PS1_0=1	PSL1_0=0	PSC_0=0	–
P71 ⁽¹⁾	RxD2 input	PS1_1=0	–	–	PD7_1=0

NOTES:

1. P70 and P71 are ports for the N-channel open drain output.

Table 16.38 Pin Settings (3)

Port	Function	Setting		
		PS3 Register ⁽¹⁾	PSL3 Register	PD9 Register ⁽¹⁾
P91	RxD3 input	PS3_1=0	–	PD9_1=0
P92	TxD3 output	PS3_2=1	PSL3_2=0	–
P96	TxD4 output	PS3_6=1	–	–
P97	RxD4 input	PS3_7=0	–	PD9_7=0

NOTES:

1. Set the PD9 and PS3 registers immediately after the PRC2 bit in the PRCR register is set to "1" (write enable). Do not generate an interrupt or a DMA transfer between the instruction to set to the PRC2 bit to "1" and the instruction to set the PD9 and PS3 registers.

Figure 16.29 shows an example of a SIM interface operation. Figure 16.30 shows an example of a SIM interface connection. Connect TxDi to RxDi for a pull-up.

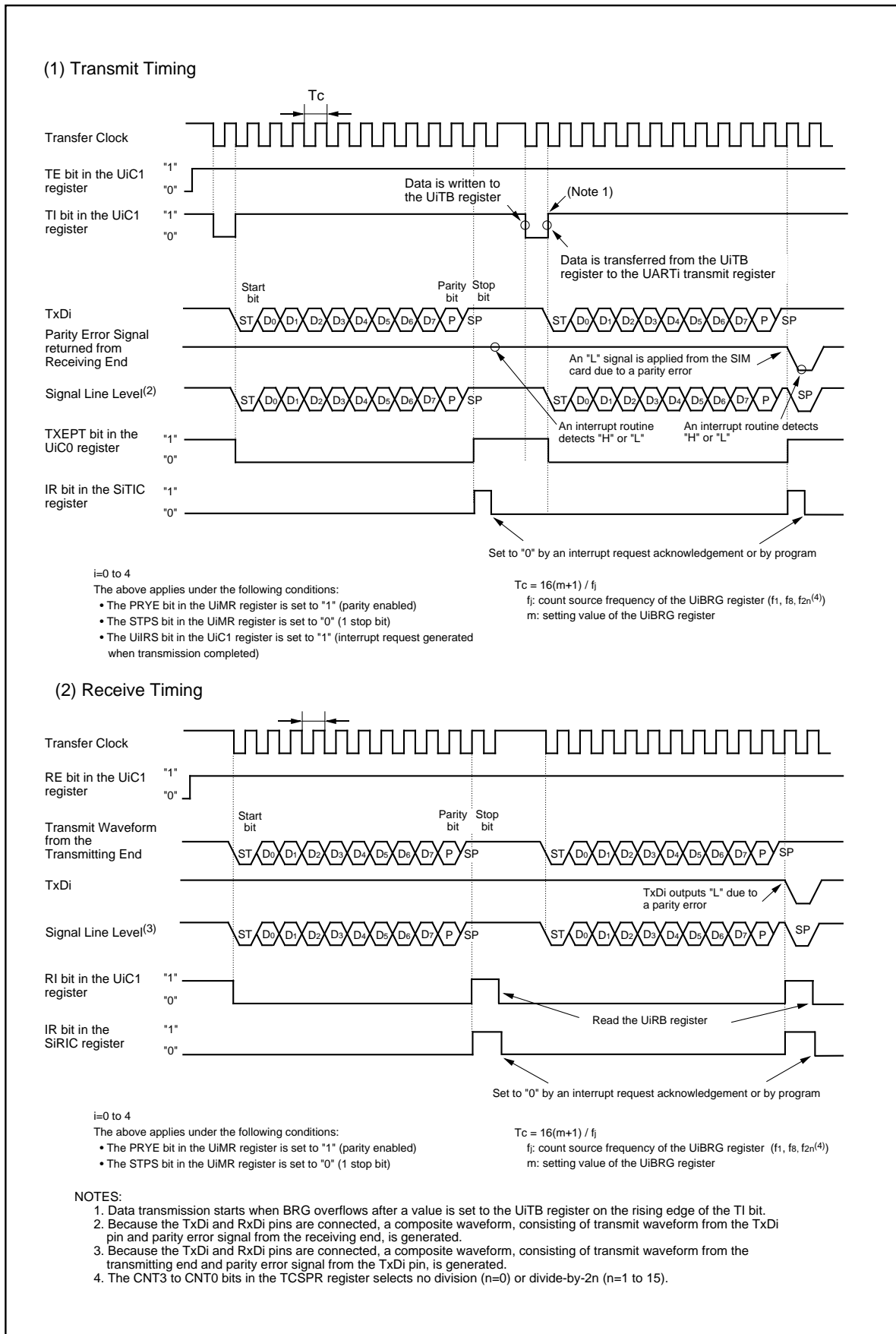


Figure 16.29 SIM Interface Operation

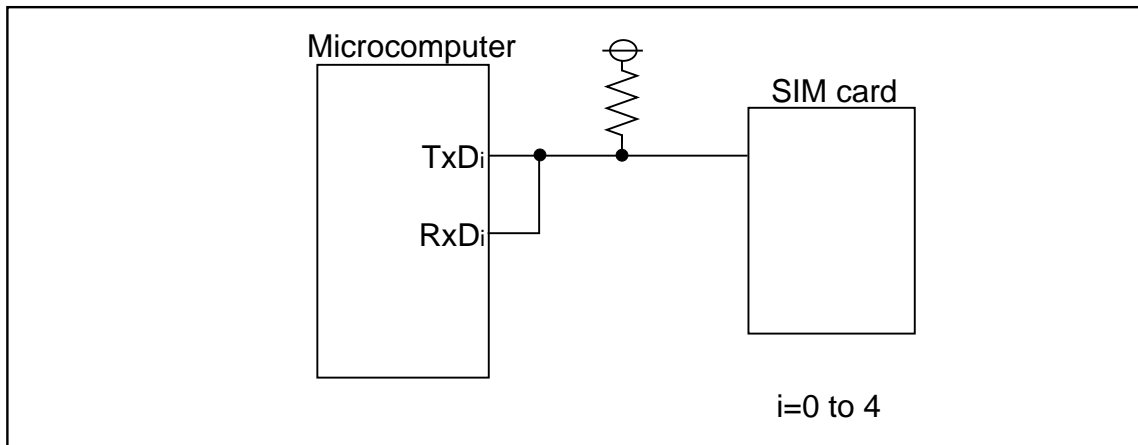


Figure 16.30 SIM Interface Connection

16.7.1 Parity Error Signal

16.7.1.1 Parity Error Signal Output Function

When the UiERE bit in the UiC1 register ($i=0$ to 4) is set to "1", the parity error signal can be output. The parity error signal is output when a parity error is detected upon receiving data. TxDi outputs an "L" signal in the timing shown in Figure 16.31. When reading the UiRB register during a parity error output, the PER bit in the UiRB register is set to "0" and TxDi again outputs an "H" signal simultaneously.

16.7.1.2 Parity Error Signal

To determine whether the parity error signal is output, the port that shares a pin with RxDi is read by using a transmit complete interrupt routine.

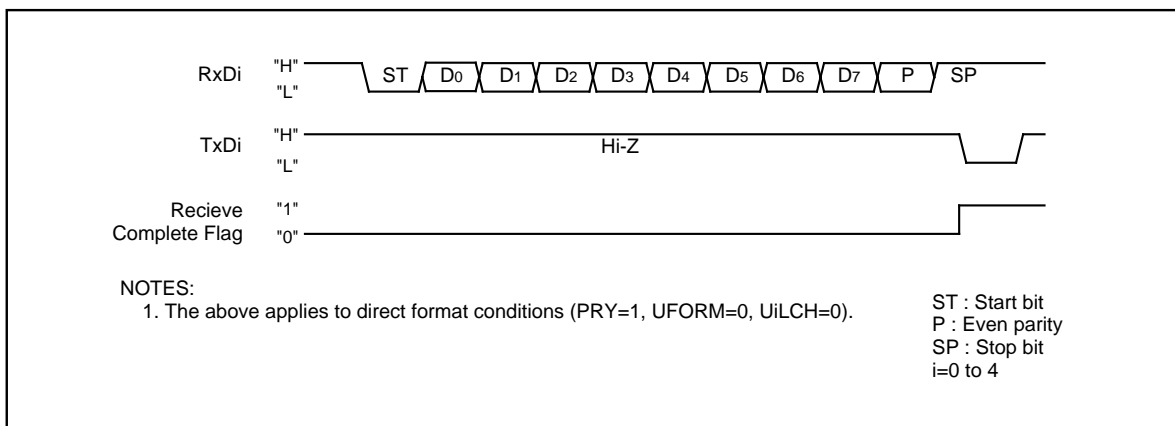


Figure 16.31 Parity Error Signal Output Timing (LSB First)

16.7.2 Format

16.7.2.1 Direct Format

Set the PRYE bit in the UiMR register ($i=0$ to 4) to "1", the PRY bit to "1", the UFORM bit in the UiC0 register to "0" and the UiLCH bit in the UiC1 register to "0". When data are transmitted, data set in UiTB register are transmitted with the even-numbered parity, starting from D0. When data are received, received data are stored in the UIRB register, starting from D0. The even-numbered parity determines whether a parity error occurs.

16.7.2.2 Inverse Format

Set the PRYE bit to "1", the PRY bit to "0", the UFORM bit to "1" and the UiLCH bit to "1". When data are transmitted, values set in the UiTB register are logically inverted and are transmitted with the odd-numbered parity, starting from D7. When data are received, received data are logically inverted to be stored in the UIRB register, starting from D7. The odd-numbered parity determines whether a parity error occurs.

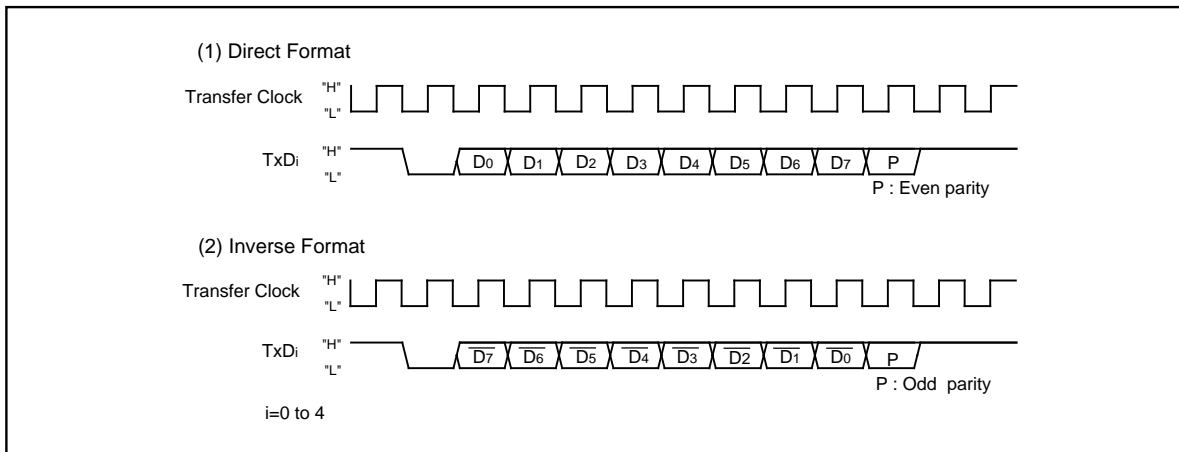


Figure 16.32 SIM Interface Format

17. A/D Converter

The A/D converter consists of two 10-bit successive approximation A/D converters, each with a capacitive coupling amplifier.

The result of an A/D conversion is stored into the A/D register corresponding to selected pins.

Table 17.1 lists specifications of the A/D converter. Figure 17.1 shows a block diagram of the A/D converter. Table 17.2 lists the differences between A/D0 and A/D1 conversions, which share the same conversion method. A/D0 and A/D1 can perform conversions simultaneously. Table 17.3 lists settings of the following pins; AN0 to AN7, AN00 to AN07, AN20 to AN27, AN150 to AN157, ANEX0, ANEX1 and ADTRG. Figures 17.2 to 17.7 show registers associated with the A/D converter.

NOTE

In this section, the 144-pin package is given as the example.

The AN150 to AN157 pins are not included in the 100-pin package.

Table 17.1 A/D Converter Specifications

Item	Specification
A/D Conversion Method	Successive approximation (with a capacitive coupling amplifier)
Analog Input Voltage ⁽¹⁾	0V to AVCC (VCC)
Operating Clock, \emptyset_{AD} ⁽²⁾	fAD, fAD/2, fAD/3, fAD/4
Resolution	Select from 8 bits or 10 bits
Operating Mode	One-shot mode, repeat mode, single sweep mode, repeat sweep mode 0, repeat sweep mode 1
Analog Input Pins ⁽³⁾	34 pins 8 pins each for AN (AN0 to AN7), AN0 (AN00 to AN07), AN2 (AN20 to AN27), AN15 (AN150 to AN157) 2 extended input pins (ANEX0 and ANEX1)
A/D Conversion Start Condition	Software trigger <ul style="list-style-type: none"> The ADST bit in the ADiCON0 (i=0, 1) register is set to "1" (A/D conversion started) by program The PST bit in the AD0CON2 register is set to "1" (A/D0 and A/D1 start a conversion simultaneously) by program External trigger (re-trigger is enabled) When a falling edge is applied to the \overline{ADTRG} pin after the ADST bit is set to "1" by program Hardware trigger (re-trigger is enabled) One of the following interrupt requests is generated after the ADST bit is set to "1" by program: <ul style="list-style-type: none"> The timer B2 interrupt request of the three-phase motor control timer functions (after the ICTB2 counter completes counting) The intelligent I/O interrupt request Channel 1 in the group 2 (A/D0), channel 1 in the group 3 (A/D1)
Conversion Rate Per Pin	<ul style="list-style-type: none"> Without the sample and hold function 8-bit resolution : 49 \emptyset_{AD} cycles 10-bit resolution : 59 \emptyset_{AD} cycles With the sample and hold function 8-bit resolution : 28 \emptyset_{AD} cycles 10-bit resolution : 33 \emptyset_{AD} cycles

NOTES:

- Analog input voltage is not affected by the sample and hold function status.
- \emptyset_{AD} frequency must be under 16 MHz when VCC=5V.
 \emptyset_{AD} frequency must be under 10 MHz when VCC=3.3V.
Without the sample and hold function, the \emptyset_{AD} frequency must be 250 kHz or more.
With the sample and hold function, the \emptyset_{AD} frequency must be 1 MHz or more.
- AVCC = VREF = VCC, A/D input voltage (for AN0 to AN7, AN00 to AN07, AN20 to AN27, AN150 to AN157, ANEX0 and ANEX1) \leq VCC.

Table 19.2 Difference between A/D0 and A/D1

Item	A/D0	A/D1
Analog Input Pins ⁽¹⁾	AN (AN0 to AN7)	Select from AN0 (AN00 to AN07), AN2 (AN20 to AN27) or AN15 (AN150 to AN157)
Extended Analog Input Pins	ANEX0, ANEX1	Not provided
External Op-Amp ⁽¹⁾	Enabled	Disabled
Intelligent I/O used as a Trigger	Channel 1 in group 2	Channel 1 in group 3

NOTES:

- When the ADS bit in the AD0CON2 register is set to "0" (channel replacement disabled)

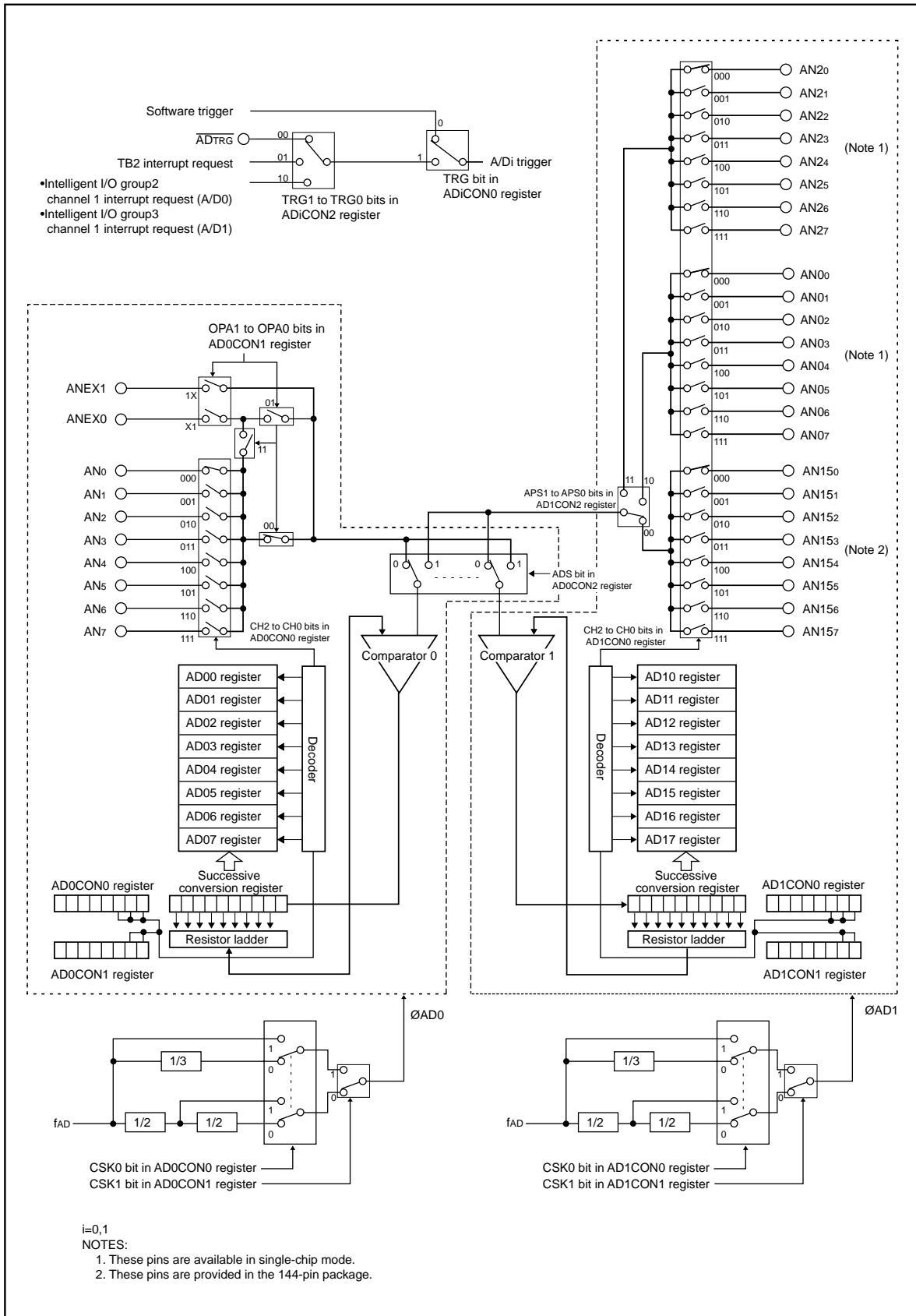


Figure 17.1 A/D Converter Block Diagram

Table 17.3 Pin Settings

Port Name	Function	Bit and Setting					
		PD10, PD0, PD2, PD15, PD9 ⁽³⁾ Registers	PS3 ⁽³⁾ , PS9 Registers	PSL3, IPS Registers	PUR0, PUR3, PUR4 Registers		
P100	AN ₀	PD10_0 = 0	-	-	PU30 = 0		
P101	AN ₁	PD10_1 = 0					
P102	AN ₂	PD10_2 = 0					
P103	AN ₃	PD10_3 = 0					
P104	AN ₄	PD10_4 = 0			-	-	PU31 = 0
P105	AN ₅	PD10_5 = 0					
P106	AN ₆	PD10_6 = 0					
P107	AN ₇	PD10_7 = 0					
P00	AN0 ₀ ⁽¹⁾	PD0_0 = 0	-	-	PU00 = 0		
P01	AN0 ₁ ⁽¹⁾	PD0_1 = 0					
P02	AN0 ₂ ⁽¹⁾	PD0_2 = 0					
P03	AN0 ₃ ⁽¹⁾	PD0_3 = 0					
P04	AN0 ₄ ⁽¹⁾	PD0_4 = 0			-	-	PU01 = 0
P05	AN0 ₅ ⁽¹⁾	PD0_5 = 0					
P06	AN0 ₆ ⁽¹⁾	PD0_6 = 0					
P07	AN0 ₇ ⁽¹⁾	PD0_7 = 0					
P20	AN2 ₀ ⁽¹⁾	PD2_0 = 0	-	-	PU04 = 0		
P21	AN2 ₁ ⁽¹⁾	PD2_1 = 0					
P22	AN2 ₂ ⁽¹⁾	PD2_2 = 0					
P23	AN2 ₃ ⁽¹⁾	PD2_3 = 0					
P24	AN2 ₄ ⁽¹⁾	PD2_4 = 0	-	-	PU05 = 0		
P25	AN2 ₅ ⁽¹⁾	PD2_5 = 0					
P26	AN2 ₆ ⁽¹⁾	PD2_6 = 0					
P27	AN2 ₇ ⁽¹⁾	PD2_7 = 0					
P150	AN15 ₀ ⁽²⁾	PD15_0 = 0				PS9_0 = 0	IPS2 = 1
P151	AN15 ₁ ⁽²⁾	PD15_1 = 0	PS9_1 = 0				
P152	AN15 ₂ ⁽²⁾	PD15_2 = 0	-				
P153	AN15 ₃ ⁽²⁾	PD15_3 = 0	-				
P154	AN15 ₄ ⁽²⁾	PD15_4 = 0	PS9_4 = 0	-	PU43 = 0		
P155	AN15 ₅ ⁽²⁾	PD15_5 = 0	PS9_5 = 0				
P156	AN15 ₆ ⁽²⁾	PD15_6 = 0	-				
P157	AN15 ₇ ⁽²⁾	PD15_7 = 0	-				
P95	ANEX0	PD9_5 = 0	PS3_5 = 0	PSL3_5 = 1	PU27 = 0		
P96	ANEX1	PD9_6 = 0	PS3_6 = 0	PSL3_6 = 1			
P97	ADTRG	PD9_7 = 0	PS3_7 = 0	-	-		

NOTES:

1. This pin is available in single-chip mode.
2. This pin is provided in the 144-pin package.
3. Set the PD9 and PS3 registers immediately after the PRC2 bit in the PRCR register is set to "1" (write enable). Do not generate an interrupt or a DMA transfer between the instruction to set to the PRC2 bit to "1" and the instruction to set the PD9 and PS3 registers.

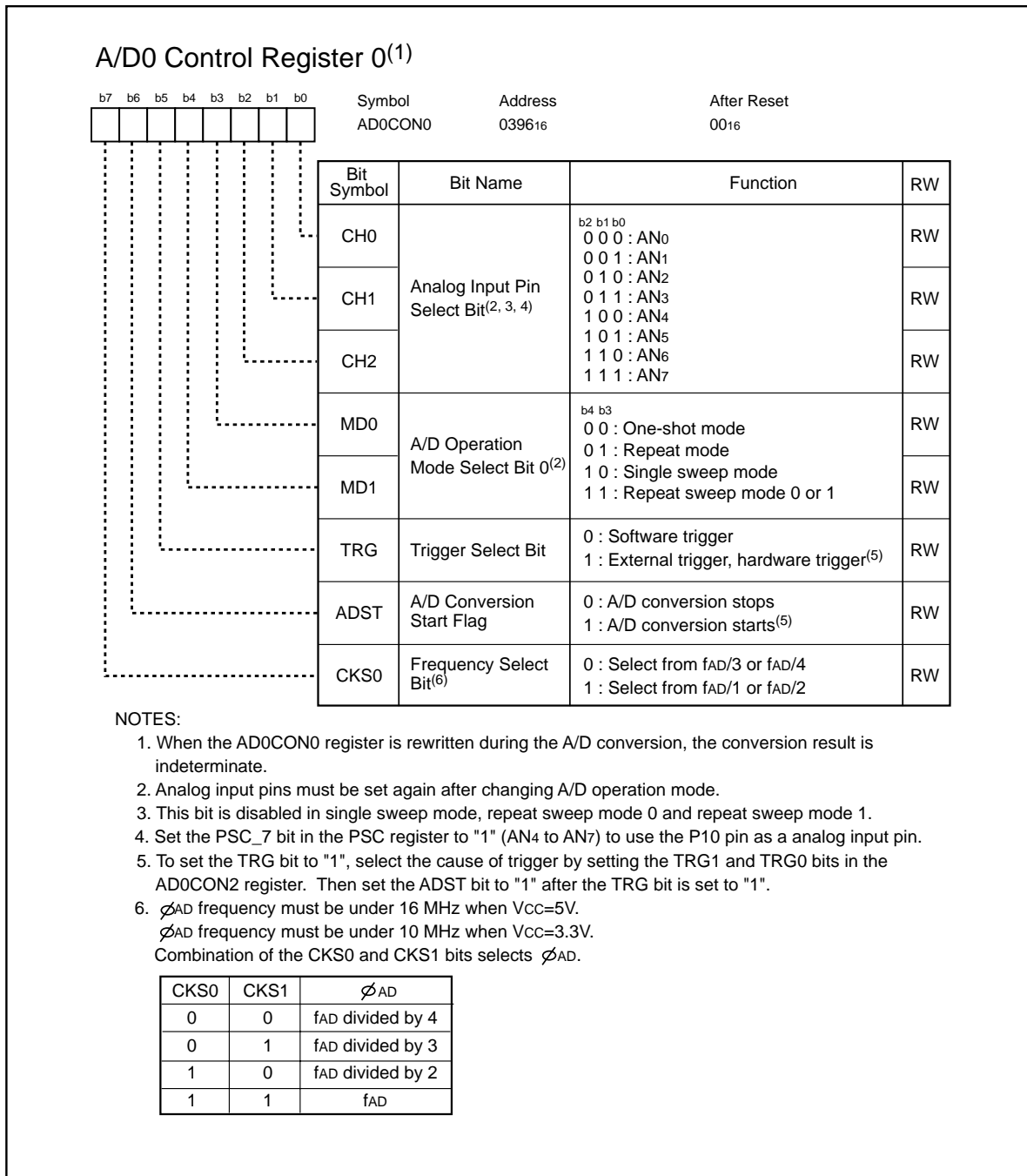


Figure 17.2 AD0CON0 Register

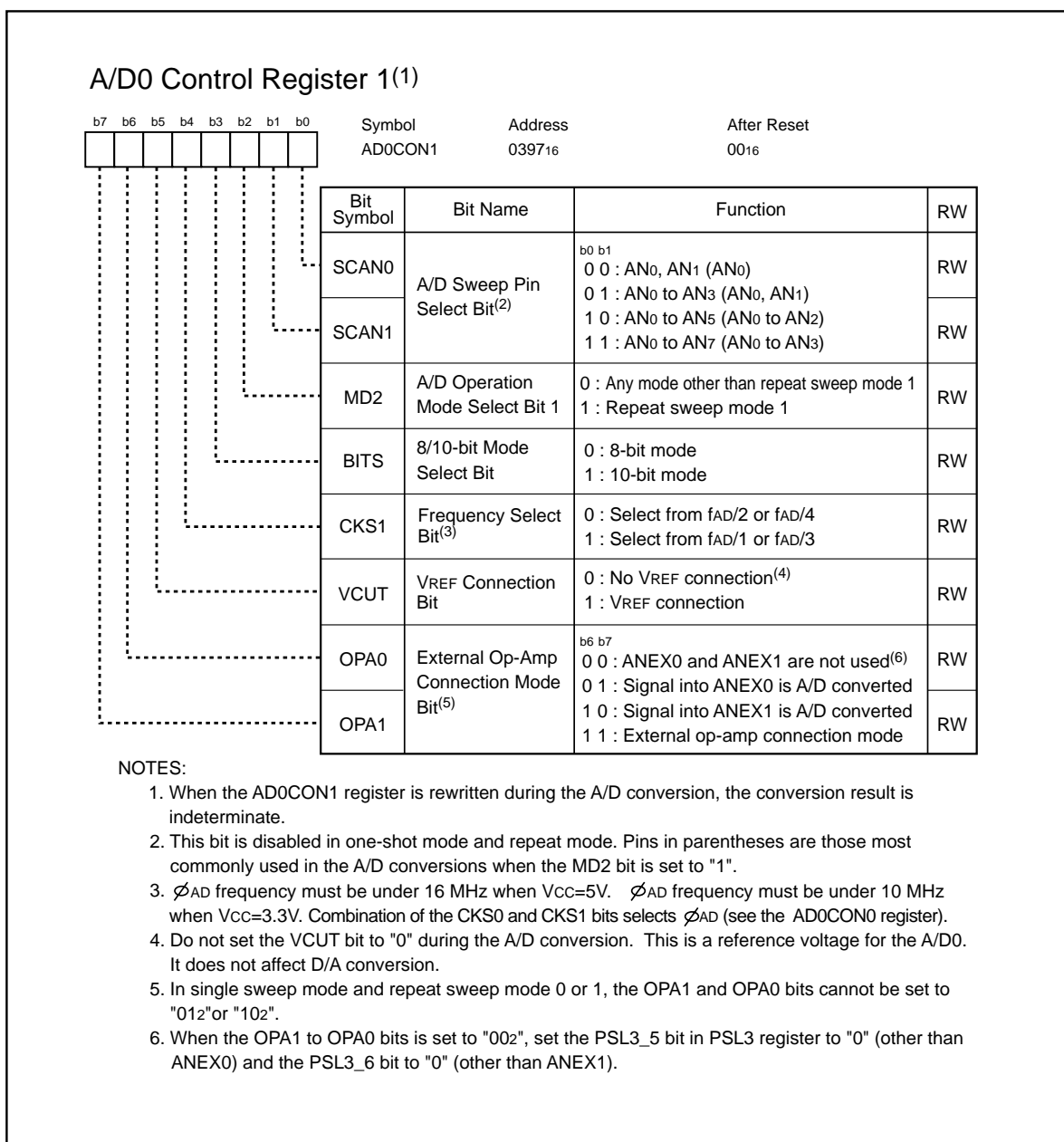


Figure 17.3 AD0CON1 Register

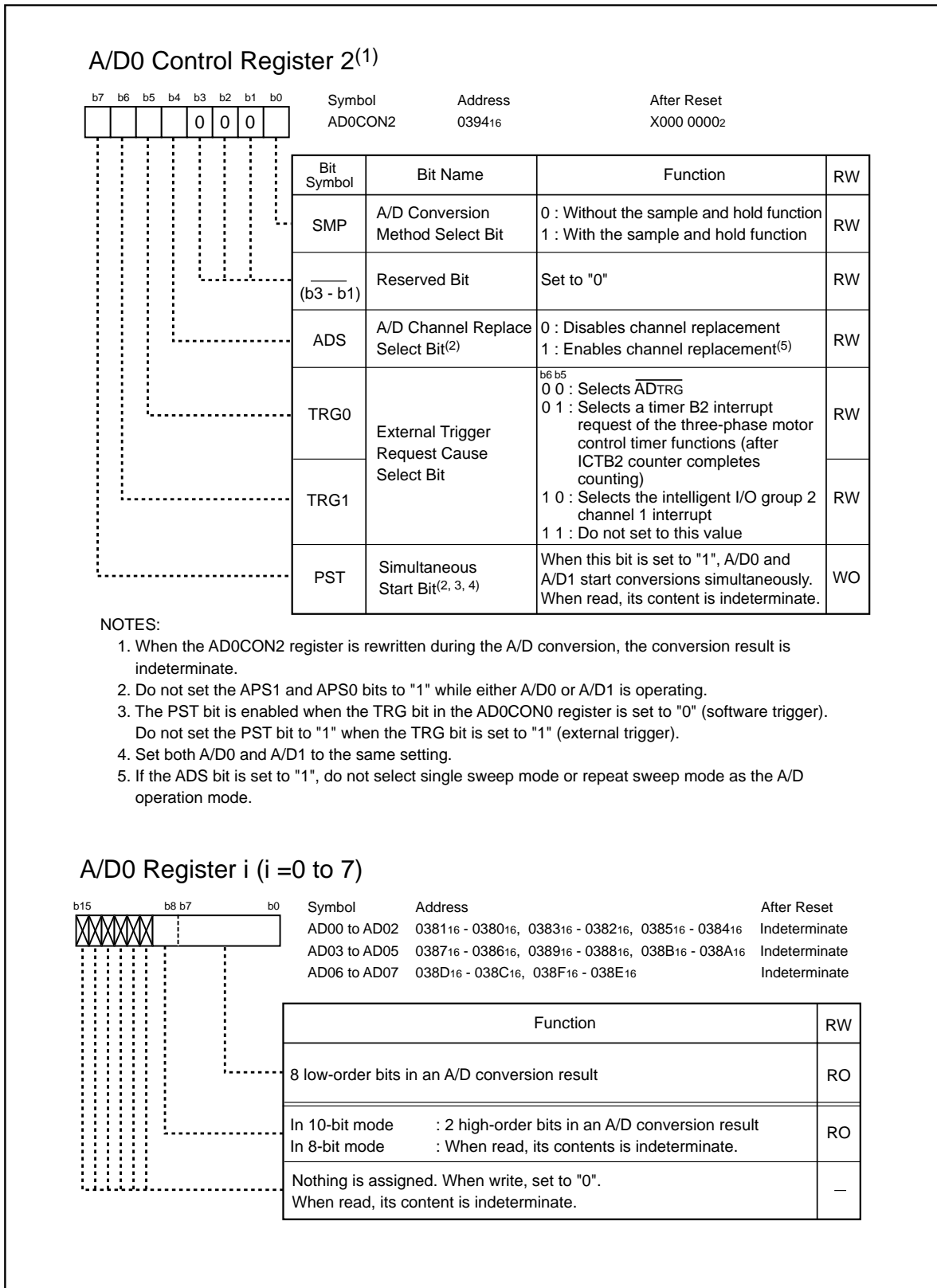


Figure 17.4 AD0CON2 Register, AD00 to AD07 Registers

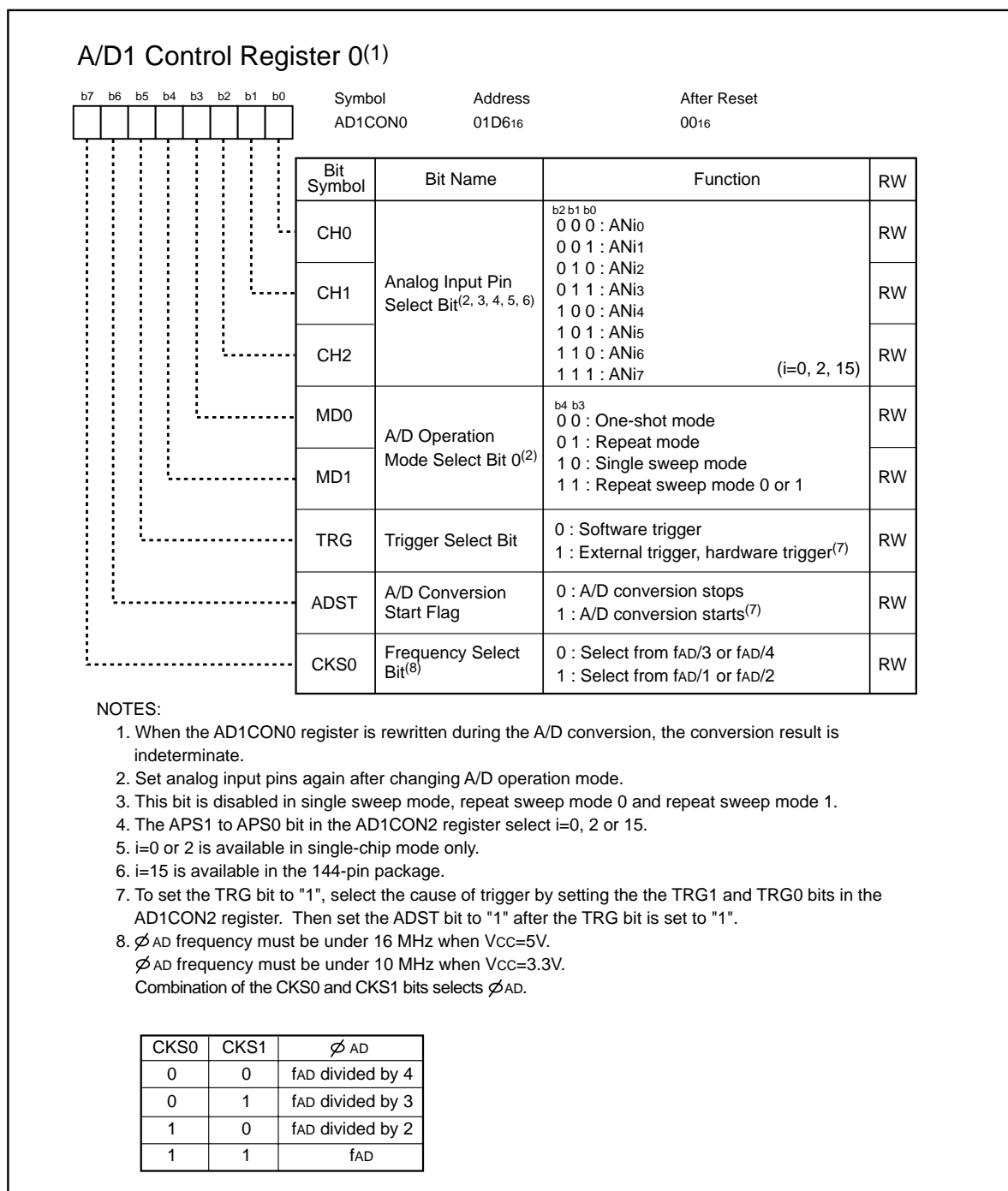


Figure 17.5 AD1CON0 Register

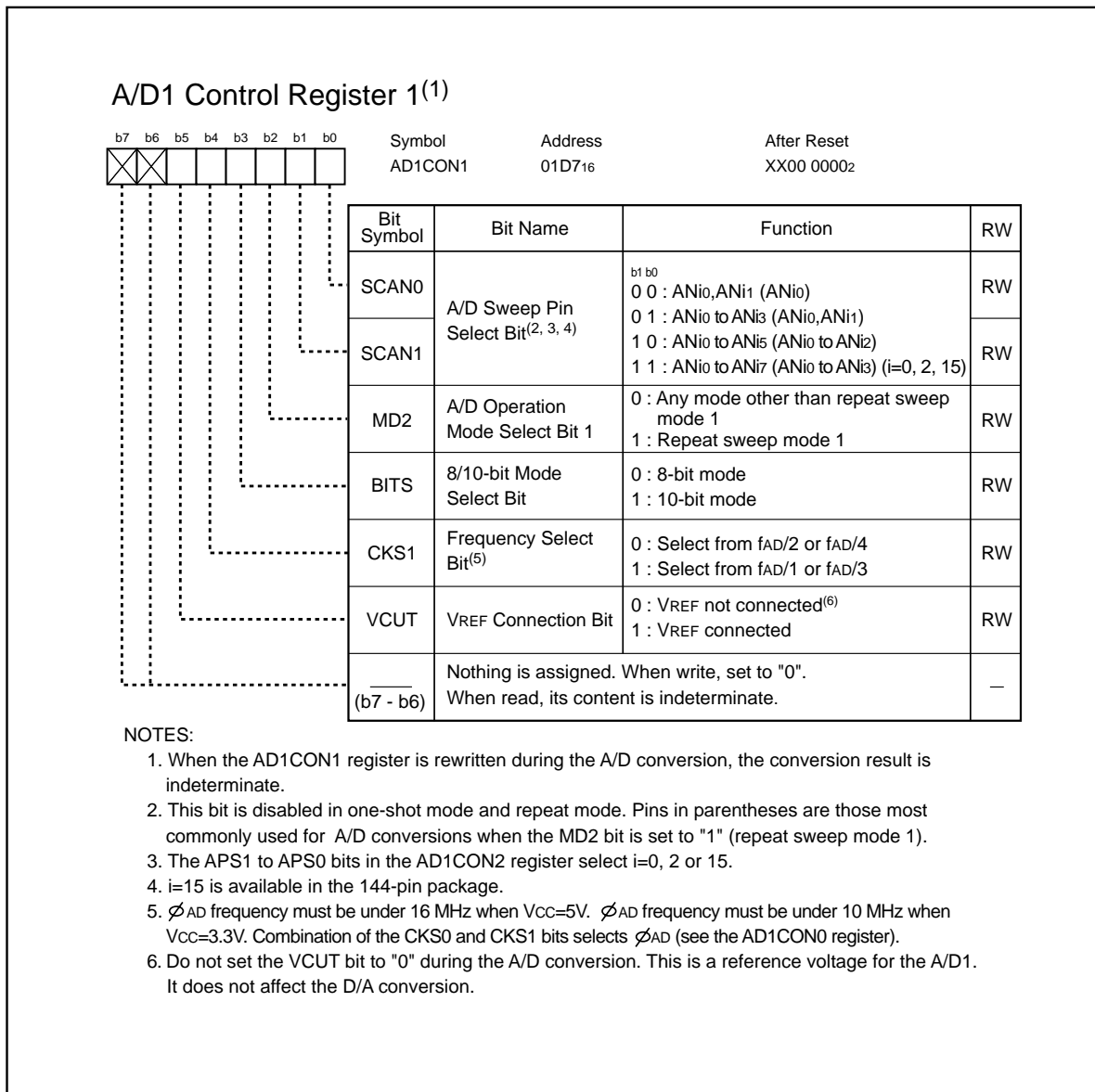


Figure 17.6 AD1CON1 Register

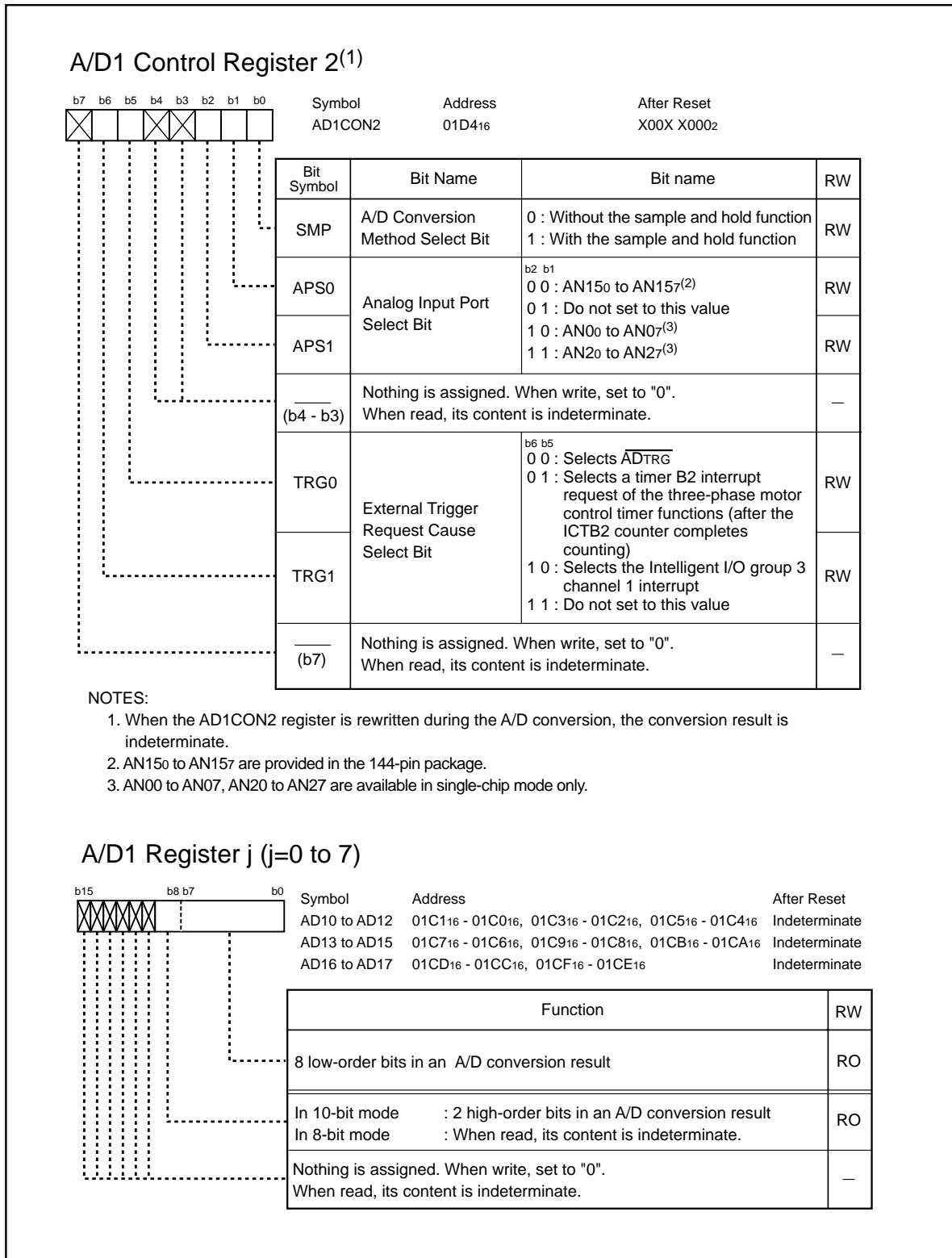


Figure 17.7 AD1CON2 Register, AD10 to AD17 Register

17.1 Mode Description

17.1.1 One-shot Mode

In one-shot mode, analog voltage applied to a selected pin is converted to a digital code once. Table 17.4 lists specifications of one-shot mode.

Table 17.4 One-shot Mode Specifications

Item	Specification
Function	Analog voltage, applied to a pin selected by the CH2 to CH0 bits in the ADiCON0 register (i=0, 1), is converted to a digital code once.
Start Condition	When the TRG bit in the ADiCON0 register is set to "0" (software trigger), <ul style="list-style-type: none"> • The ADST bit in the ADiCON0 register is set to "1" (A/D conversion starts) by program • The PST bit in the AD0CON2 register is set to "1" (A/D0 and A/D1 start a conversion simultaneously) by program When the TRG bit is set to "1" (external trigger, hardware trigger), <ul style="list-style-type: none"> • A falling edge is applied to the $\overline{\text{ADTRG}}$ pin after the ADST bit is set to "1" by program • One of the following interrupt requests is generated after the ADST bit is set to "1" by program: <ul style="list-style-type: none"> - The timer B2 interrupt request of three-phase motor control timer functions (after the ICTB2 counter completes counting) is generated - The intelligent I/O interrupt request is generated Channel 1 in the group 2 (A/D0), channel 1 in the group 3 (A/D1)
Stop Condition	<ul style="list-style-type: none"> • A/D conversion is completed (the ADST bit is set to "0" when the internal trigger is selected) • The ADST bit is set to "0" (A/D conversion stopped) by program
Interrupt Request Generation Timing	A/D conversion is completed
Analog Voltage Input Pins	Select one from AN0 to AN7, ANEX0, or ANEX1 Select one from ANj0 to ANj7 (j=0, 2, 15)
Reading of A/D Conversion Result	The ADik register (k=0 to 7) corresponding to selected pin

17.1.2 Repeat Mode

In repeat mode, analog voltage applied to a selected pin is repeatedly converted to a digital code. Table 17.5 lists specifications of repeat mode.

Table 17.5 Repeat Mode Specifications

Item	Specification
Function	Analog voltage, applied to a pin selected by the CH2 to CH0 bits in the ADiCON0 register (i=0, 1), is converted to a digital code once.
Start Condition	Same as one-shot mode
Stop Condition	The ADST bit in the ADiCON0 register is set to "0" (A/D conversion stopped) by program
Interrupt Request Generation Timing	Not generated
Analog Voltage Input Pins	Select one from AN0 to AN7, ANEX0, or ANEX1 Select from ANj0 to ANj7 (j=0, 2, 15)
Reading of A/D Conversion Result	The ADik register (k=0 to 7) corresponding to selected pins

17.1.3 Single Sweep Mode

In single sweep mode, analog voltage that is applied to selected pins is converted one-by-one to a digital code. Table 17.6 lists specifications of single sweep mode.

Table 17.6 Single Sweep Mode Specifications

Item	Specification
Function	Analog voltage, applied to pins selected by the SCAN1 to SCAN0 bits in the ADiCON0 register (i=0, 1), are converted one-by-one to a digital code
Start Condition	Same as one-shot mode
Stop Condition	<ul style="list-style-type: none"> A/D conversion is completed (the ADST bit in the ADiCON0 register is set to "0" when the internal trigger is selected) The ADST bit is set to "0" (A/D conversion stopped) by program
Interrupt Request Generation Timing	Sweep operation is completed
Analog Voltage Input Pins	Select from AN0 to AN1 (2 pins), AN0 to AN3 (4 pins), AN0 to AN5 (6 pins), AN0 to AN7 (8 pins) Select from ANj0 (j=0, 2, 15) to ANj1 (2 pins), ANj0 to ANj3 (4 pins), ANj0 to ANj5 (6 pins), or ANj0 to ANj7 (8 pins)
Reading of A/D Conversion Result	The ADik register (k=0 to 7) corresponding to selected pins

17.1.4 Repeat Sweep Mode 0

In repeat sweep mode 0, analog voltage applied to selected pins is repeatedly converted to a digital code. Table 17.7 lists specifications of repeat sweep mode 0.

Table 17.7 Repeat Sweep Mode 0 Specifications

Item	Specification
Function	Analog voltage, applied to pins selected by the SCAN1 to SCAN0 bits in the ADiCON0 register (i=0, 1), are repeatedly converted to a digital code
Start Condition	Same as one-shot mode
Stop Condition	The ADST bit in the ADiCON0 register is set to "0" (A/D conversion stopped) by program
Interrupt Request Generation Timing	Not generated
Analog Voltage Input Pins	Select from AN0 to AN1 (2 pins), AN0 to AN3 (4 pins), AN0 to AN5 (6 pins), AN0 to AN7 (8 pins) Select from ANj0 (j=0, 2, 15) to ANj1 (2 pins), ANj0 to ANj3 (4 pins), ANj0 to ANj5 (6 pins), or ANj0 to ANj7 (8 pins)
Reading of A/D Conversion Result	The ADik register (k=0 to 7) corresponding to selected pins

17.1.5 Repeat Sweep Mode 1

In repeat sweep mode 1, analog voltage selectively applied to eight pins is repeatedly converted to a digital code. Table 17.8 lists specifications of repeat sweep mode 1.

Table 17.8 Repeat Sweep Mode 1 Specifications

Item	Specification
Function	Analog voltage selectively applied to 8 pins selected by the SCAN1 to SCAN0 bits in the ADiCON1 register (i=0,1) is repeatedly converted to a digital code. e.g., When ANj0 is selected (j =none, 0, 2, 15), analog voltage is converted to a digital code in the following order: ANj0 → ANj1 → ANj0 → ANij2 → ANj0 → ANj3 etc.
Start Condition	Same as one-shot mode
Stop Condition	The ADST bit in the ADiCON1 register is set to "0" (A/D conversion stopped) by program
Interrupt Request Generation Timing	Not generated
Analog Voltage Input Pins	ANj0 to ANj7 (8 pins)
Prioritized Pins	Select from AN0 (1 pin), AN0 to AN1 (2 pins), AN0 to AN2 (3 pins), or AN0 to AN3 (4 pins) Select from ANj0 (j=0, 2, 15) (1 pin), ANj0 to ANj1 (2 pins), AN0 to AN2 (3 pins), ANj0 to ANj3 (4 pins)
Reading of A/D Conversion Result	The ADik register (k=0 to 7) corresponding to selected pins

17.2 Function

17.2.1 Resolution Select Function

The BITS bit in the ADiCON1 (i=0, 1) register determines the resolution. When the BITS bit is set to "1" (10-bit precision), the A/D conversion result is stored into bits 0 to 9 in the ADij register (j = 0 to 7). When the BITS bit is set to "0" (8-bit precision), the A/D conversion result is stored into bits 0 to 7 in the ADij register.

17.2.2 Sample and Hold

When the SMP bit in the ADiCON2 register is set to "1" (with the sample and hold function), A/D conversion rate per pin increases to 28 \varnothing AD cycles for 8-bit resolution and 33 \varnothing AD cycles for 10-bit resolution. The sample and hold function is available in all operating modes. Start the A/D conversion after selecting whether the sample and hold function is to be used or not.

17.2.3 Trigger Select Function

The TRG bit in the ADiCON0 register and the TRG1 to TRG0 bits in the ADiCON2 register determine the trigger to start the A/D conversion. Table 17.9 lists settings of the trigger select function.

Table 17.9 Trigger Select Function Settings

Bit and Setting		Trigger
ADiCON0 Register	ADiCON2 Register	
TRG = 0	-	Software trigger The A/Di starts the A/D conversion when the ADST bit in the ADiCON0 register is set to "1"
	-	Two-circuit simultaneous start A/D0 and A/D1 start the A/D conversion simultaneously when the PST bit in the AD0CON2 register is set to "1" by program (Refer to 17.2.4 Two-Circuit Simultaneous Start)
TRG = 1 ⁽¹⁾	TRG1 to TRG0 = 00 ₂	External trigger ⁽²⁾ Falling edge of a signal applied to $\overline{\text{ADTRG}}$
	TRG1 to TRG0 = 01 ₂	Hardware trigger ⁽²⁾ The timer B2 interrupt request of three-phase motor control timer functions (after the ICTB2 counter completes counting)
	TRG1 to TRG0 = 10 ₂	Hardware trigger ⁽²⁾ The intelligent I/O interrupt request is generated Channel 1 in the group 2 (A/D0), channel 1 in the group 3 (A/D1)

i = 0,1

NOTES:

1. The A/Di starts the A/D conversion when the ADST bit is set to "1" (A/D conversion started) and a trigger is generated.
2. The A/D conversion is restarted if an external trigger or a hardware trigger is inserted during the A/D conversion. (The A/D conversion in process is aborted.)

17.2.4 Two-Circuit Simultaneous Start (Software Trigger)

A/D0 and A/D1 start simultaneously when the PST bit in the AD0CON2 register is set to "1" (two-circuit simultaneous start).

Do not set the PST bit to "1" while either A/D0 or A/D1 is performing an A/D conversion, or if the TRG bit is set "1" (external trigger).

Do not set the ADST bit to "1" (A/D conversion started) when using the PST bit.

17.2.5 Pin Input Replacement Function

When the ADS bit in the AD0CON2 register is set to "1" (channel replacement enabled), channels of the A/D0 can be replaced with channels of the A/D1 and vice versa.

Voltage applied to the AN_j (j = 0 to 7) pin is converted to digital code in the A/D1 and the conversion result is stored into the AD1_j register. Voltage applied to the AN0_j, AN2_j or AN15_j pin is converted to digital code in the A/D0 and the conversion results are stored into the AD0_j register.

To set the ADS bit to "1", set the MD1 to MD0 bits in the AD0CON0 register to "00₂" (one-shot mode) or "01₂" (repeat mode). Single sweep, repeat sweep 0, and repeat sweep 1 modes cannot be used. Set the OPA1 to OPA0 bits in the AD0CON1 register to "00₂" (no ANEX0 and ANEX1 used). Set the same value to both AD0CON0 register and AD1CON0 register, and to both AD0CON1 register and AD1CON1 register.

17.2.6 Extended Analog Input Pins

In one-shot mode and repeat mode, the ANEX0 and ANEX1 pins can be used as analog input pins. The OPA1 to OPA0 bits in the AD0CON1 register select which pins to use as analog input pins. An A/D conversion result for the ANEX0 pin is stored into the AD00 register. The result for the ANEX1 pin is stored into the AD01 register.

17.2.7 External Operation Amplifier (Op-Amp) Connection Mode

In external op-amp connection mode, multiple analog voltage can be amplified by one external op-amp using extended analog input pins ANEX0 and ANEX1.

When the OPA1 to OPA0 bits in the AD0CON1 register are set to "112" (external op-amp connection), voltage applied to the AN0 to AN7 pins are output from ANEX0. Amplify this output signal by an external op-amp and apply it to ANEX1.

Analog voltage applied to ANEX1 is converted to a digital code and the A/D conversion result is stored into the corresponding AD_{ij} register (i=0, 1; j=0 to 7). A/D conversion rate varies depending on the response of the external op-amp. Do not connect the ANEX0 pin to the ANEX1 pin directly.

Figure 17.8 shows an example of an external op-amp connection.

Table 17.10 Extended Analog Input Pin Settings

AD0CON1 Register		ANEX0 Function	ANEX1 Function
OPA1	OPA0		
0	0	Not used	Not used
0	1	P95 as an analog input	Not used
1	0	Not used	P96 as an analog input
1	1	Output to an external op-amp	Input from an external op-amp

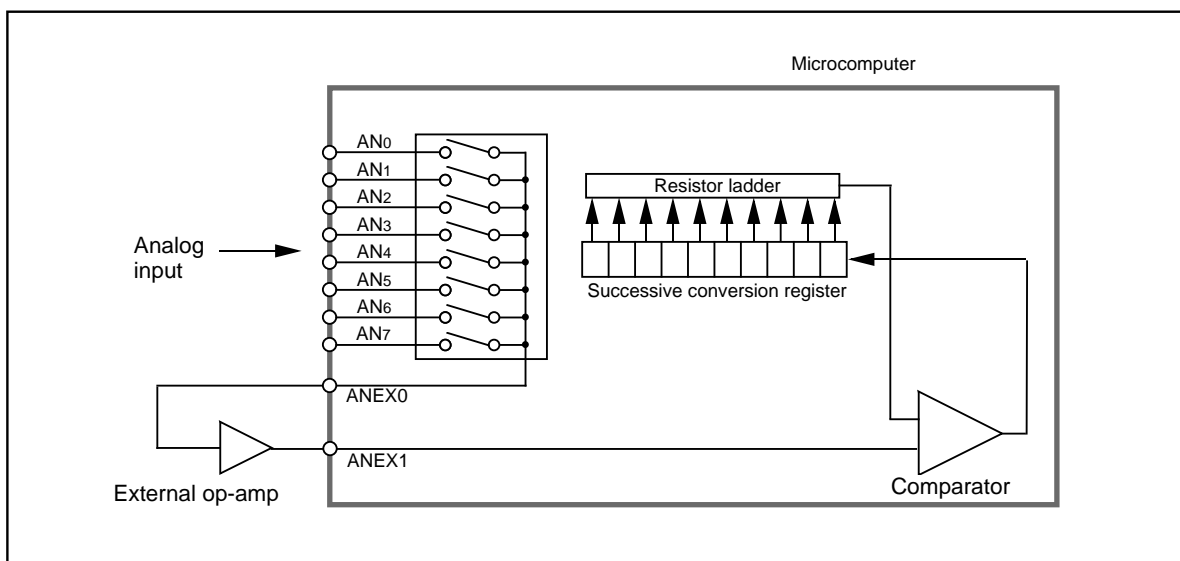


Figure 17.8 External Op-Amp Connection

17.2.8 Power Consumption Reducing Function

When the A/D converter is not used, the VCUT bit in the ADiCON1 register (i=0, 1) isolates the resistor ladder of the A/D converter from the reference voltage input pin (VREF). Power consumption is reduced by shutting off any current flow into the resistor ladder from the VREF pin.

When using the A/D converter, set the VCUT bit to "1" (VREF connection) before setting the ADST bit in the ADiCON0 register to "1" (A/D conversion started). Do not set the ADST bit and VCUT bit to "1" simultaneously, nor set the VCUT bit to "0" (no VREF connection) during the A/D conversion. The VCUT bit does not affect the VREF performance of the D/A converter.

17.2.9 Analog Input Pin and External Sensor Equivalent Circuit

Figure 17.9 shows an example of the analog input pin and external sensor equivalent circuit.

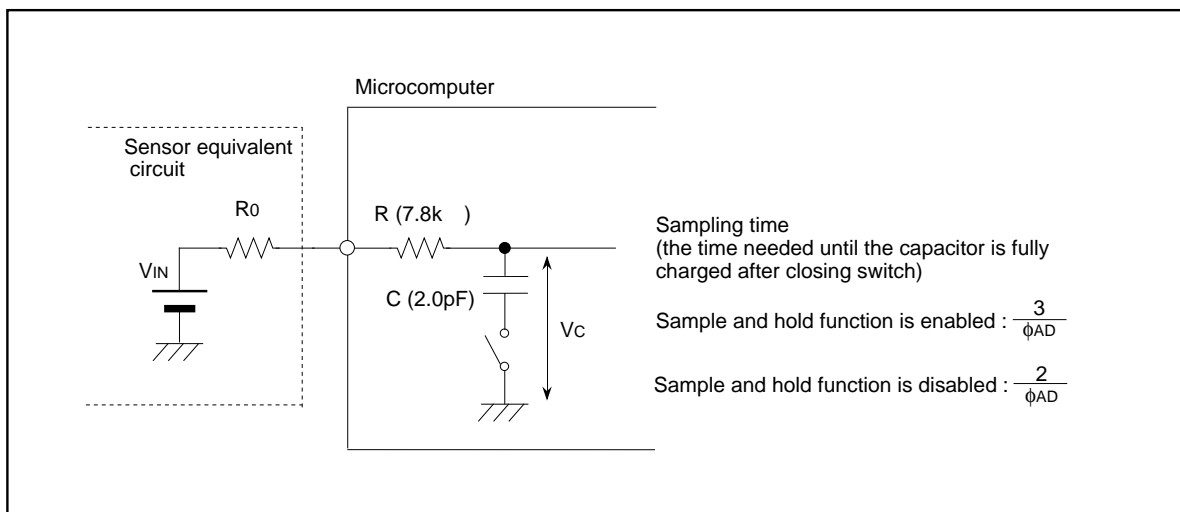


Figure 17.9 Analog Input Pin and External Sensor Equivalent Circuit

18. D/A Converter

The D/A converter consists of two separate 8-bit R-2R ladder D/A converters.

Digital code is converted to an analog voltage when a value is written to the corresponding DAi registers (i=0,1). The DAiE bit in the DACON register determines whether the D/A conversion result is output or not. Set the DAiE bit to "1" (output enabled) to disable a pull-up of a corresponding port.

Output analog voltage (V) is calculated from value n (n=decimal) set in the DAi register.

$$V = \frac{V_{REF} \times n}{256} \quad (n = 0 \text{ to } 255)$$

V_{REF} : reference voltage (not related to VCUT bit setting in the ADiCON1 register)

Table 18.1 lists specifications of the D/A converter. Table 18.2 lists pin settings of the DA0 and DA1 pins. Figure 18.1 shows a block diagram of the D/A converter. Figure 18.2 shows the D/A control register. Figure 18.3 shows a D/A converter equivalent circuit.

When the D/A converter is not used, set the DAi register to "0016" and the DAiE bit to "0" (output disabled).

Table 18.1 D/A Converter Specifications

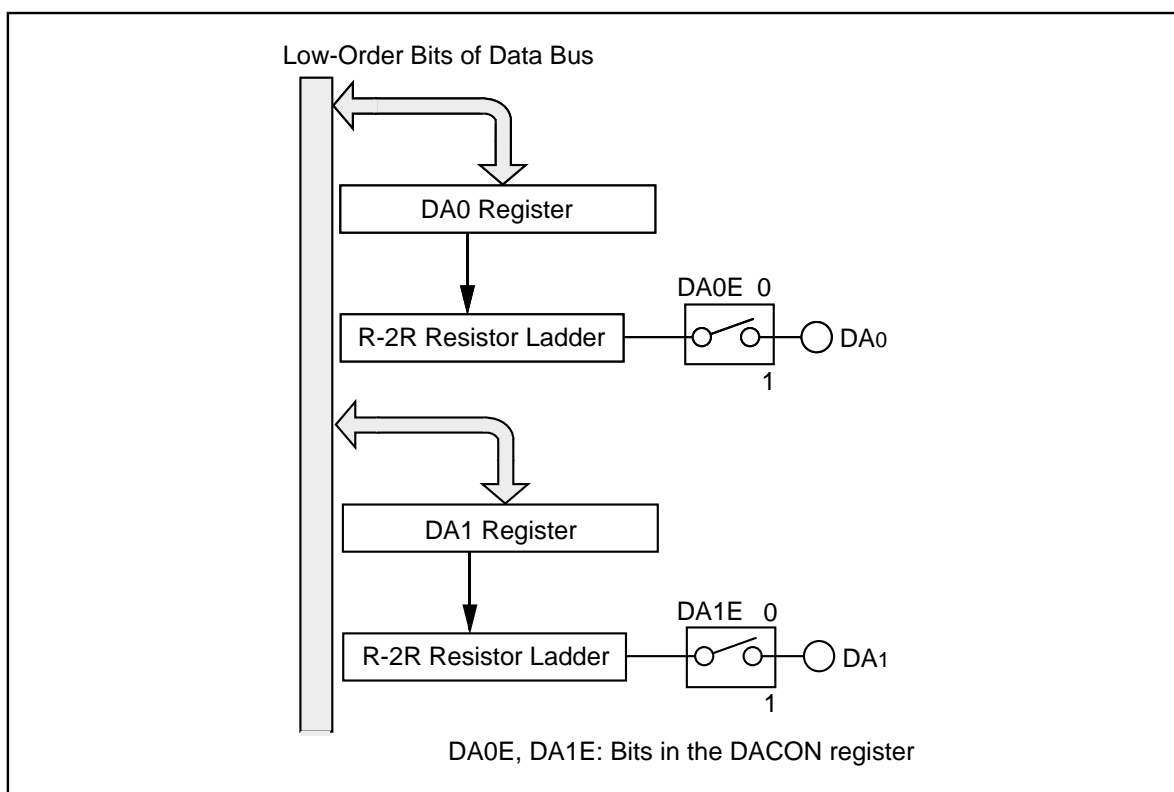
Item	Specification
D/A Conversion Method	R-2R
Resolution	8 bits
Analog Output Pin	2 channels

Table 18.2 Pin Settings

Port	Function	Bit and Setting		
		PD9 Register ⁽¹⁾	PS3 Register ⁽¹⁾	PSL3 Register
P93	DA0 output	PD9_3=0	PS3_3=0	PSL3_3=1
P94	DA1 output	PD9_4=0	PS3_4=0	PSL3_4=1

NOTES:

1. Set the PD9 and PS3 registers immediately after the PRC2 bit in the PRCR register is set to "1" (write enable). Do not generate an interrupt or a DMA transfer between the instruction to set the PRC2 bit to "1" and the instruction to set the PD9 and PS3 registers.

**Figure 18.1 D/A Converter**

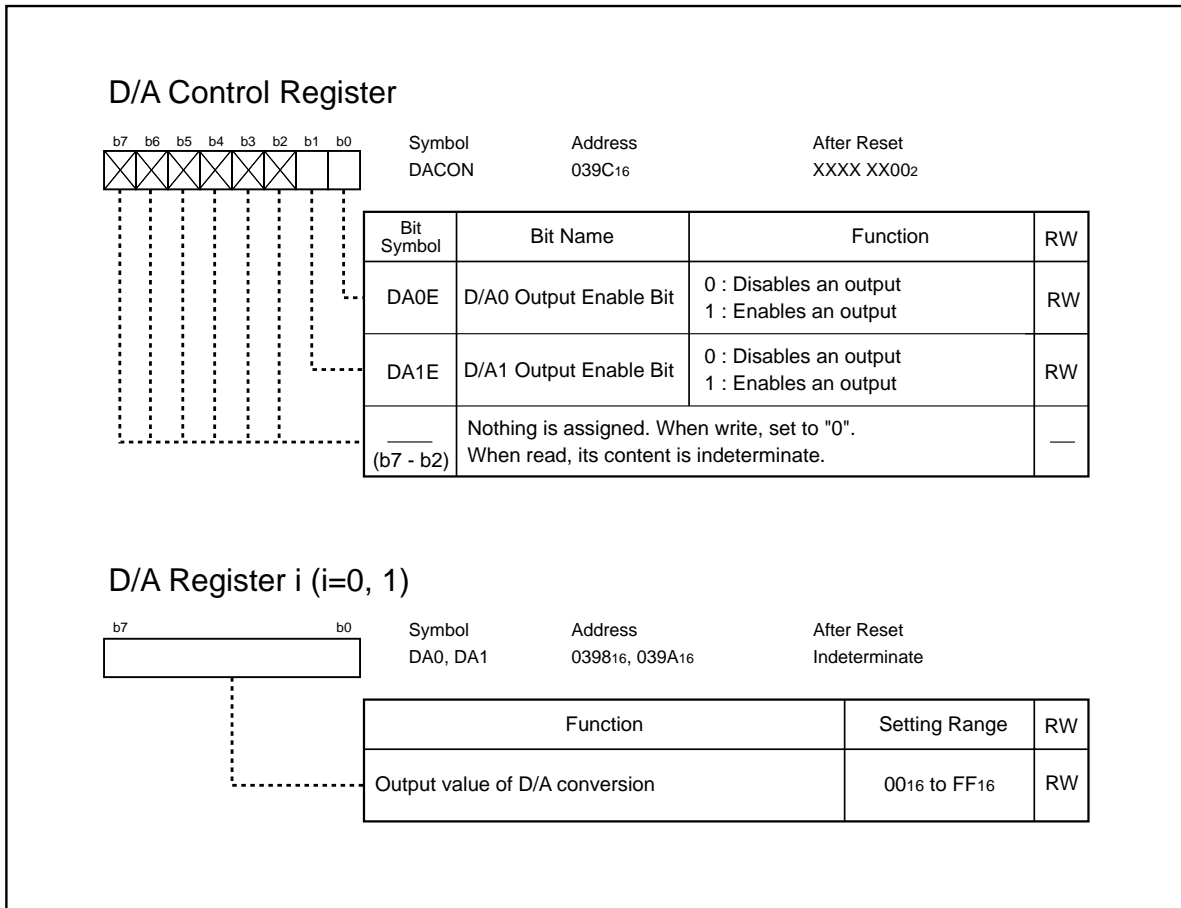


Figure 18.2 DACON Register, DA0 and DA1 Registers

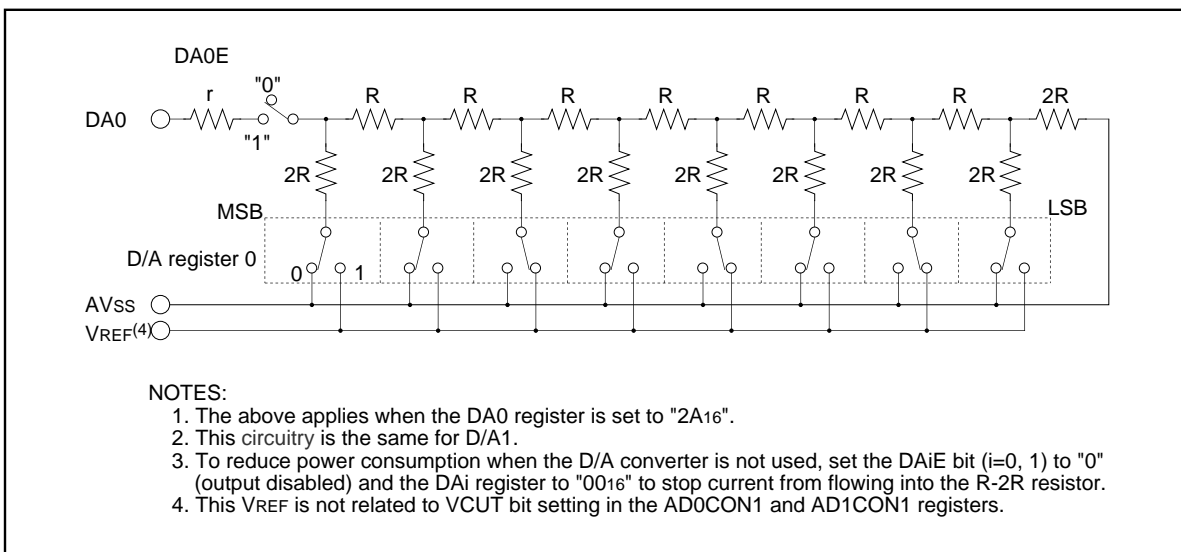


Figure 18.3 D/A Converter Equivalent Circuit

19. CRC Calculation

The CRC (Cyclic Redundancy Check) calculation detects an error in data blocks. A generator polynomial of CRC_CCITT ($X^{16} + X^{12} + X^5 + 1$) generates CRC code.

The CRC code is a 16-bit code generated for a block of data of desired length. This block of data is in 8-bit units. The CRC code is set in the CRCD register every time one-byte data is transferred to the CRCIN register after a default value is written to the CRCD register. CRC code generation for one-byte data is completed in two cycles.

Figure 19.1 shows a block diagram of a CRC circuit. Figure 19.2 shows registers related to CRC. Figure 19.3 shows an example of the CRC calculation.

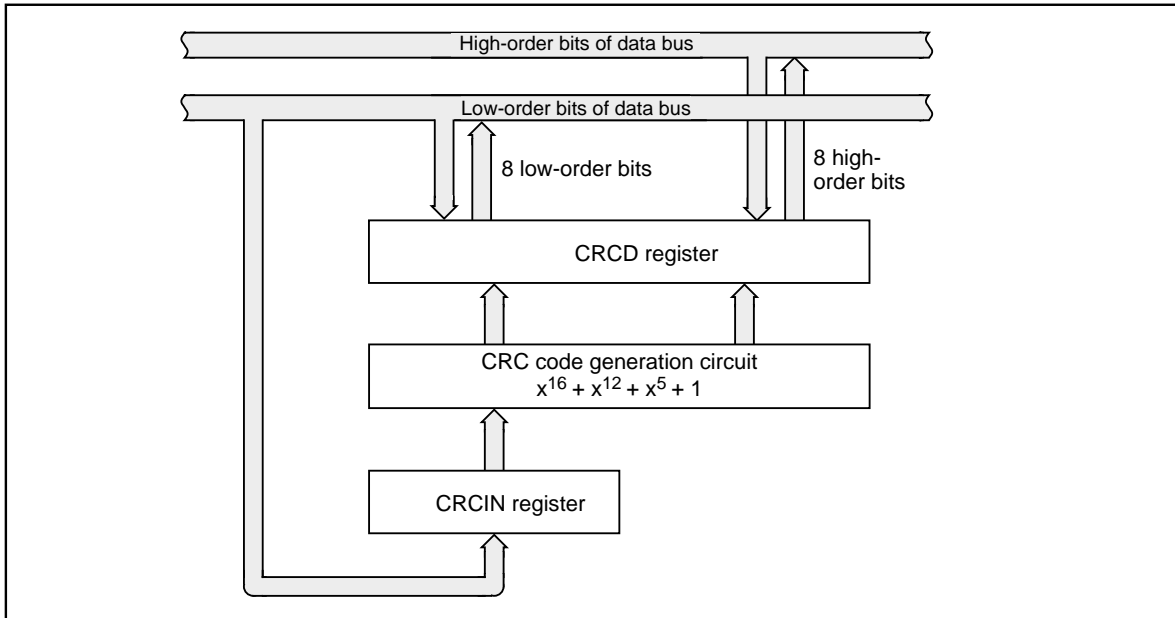


Figure 19.1 CRC Calculation Block Diagram

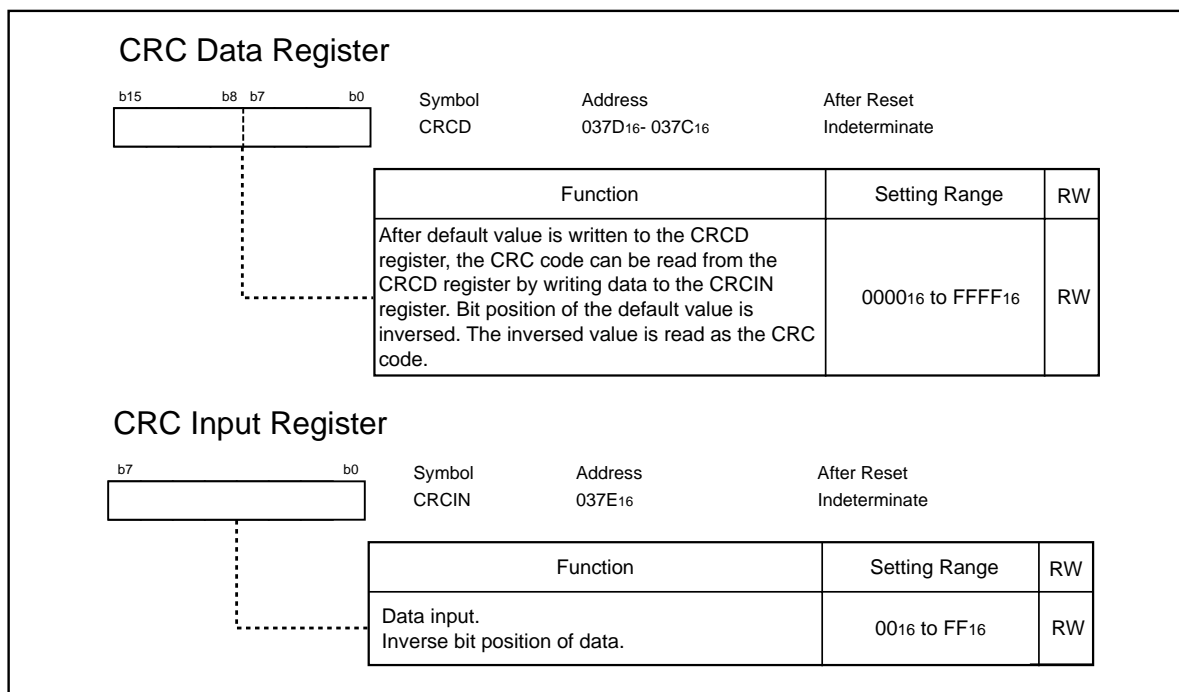


Figure 19.2 CRCD Register and CRCIN Register

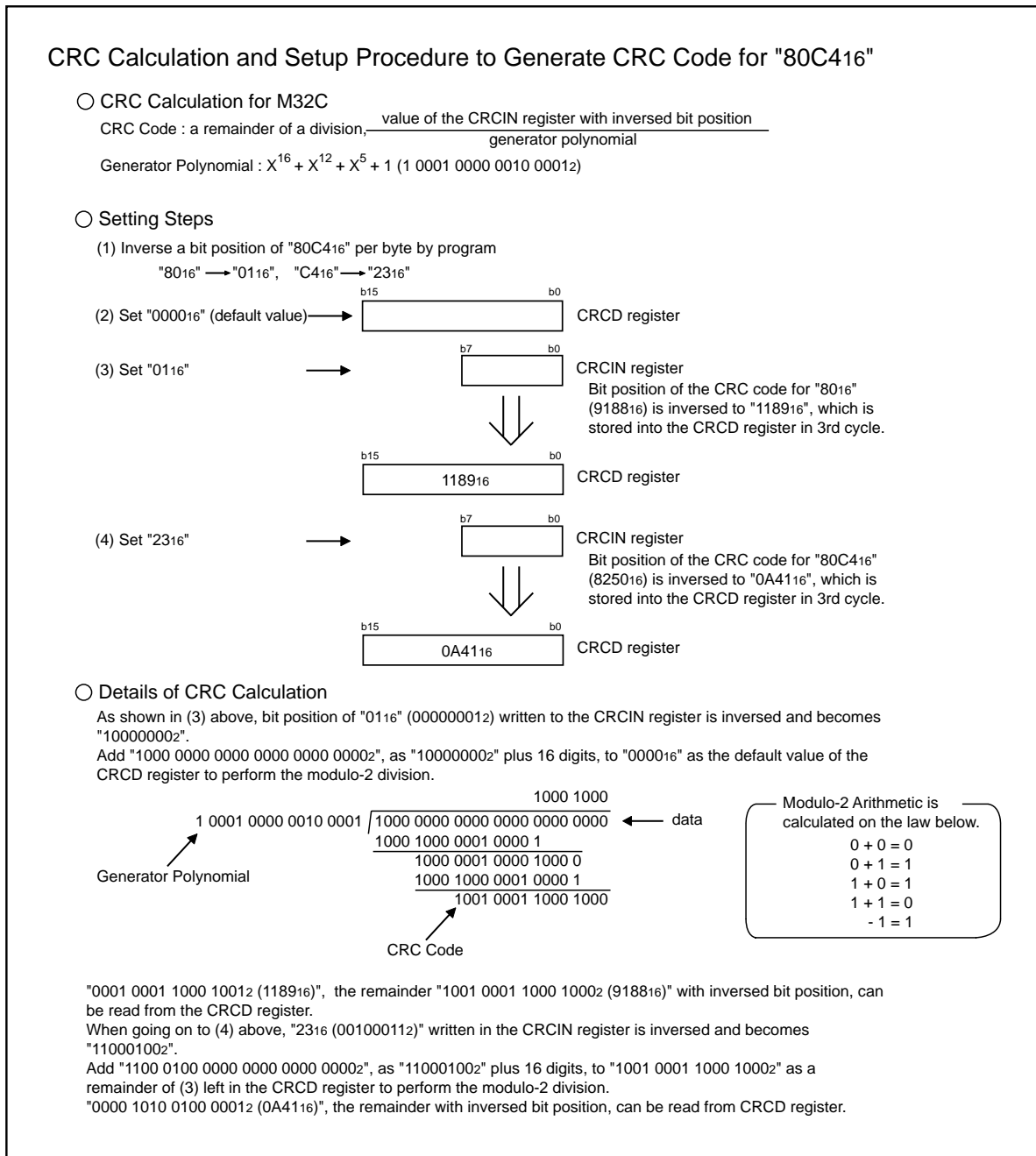


Figure 19.3 CRC Calculation

20. X/Y Conversion

The X/Y conversion rotates a 16 x 16 matrix data by 90 degrees and inverses high-order bits and low-order bits of a 16-bit data. Figure 20.1 shows the XYC register.

The 16-bit XiR register (i=0 to 15) and 16-bit YjR register (j=0 to 15) are allocated to the same address. The XiR register is a write-only register, while the YjR register is a read-only register. Access the XiR and YjR registers from an even address in 16-bit units. Performance cannot be guaranteed if the XiR and YiR registers are accessed in 8-bit units.

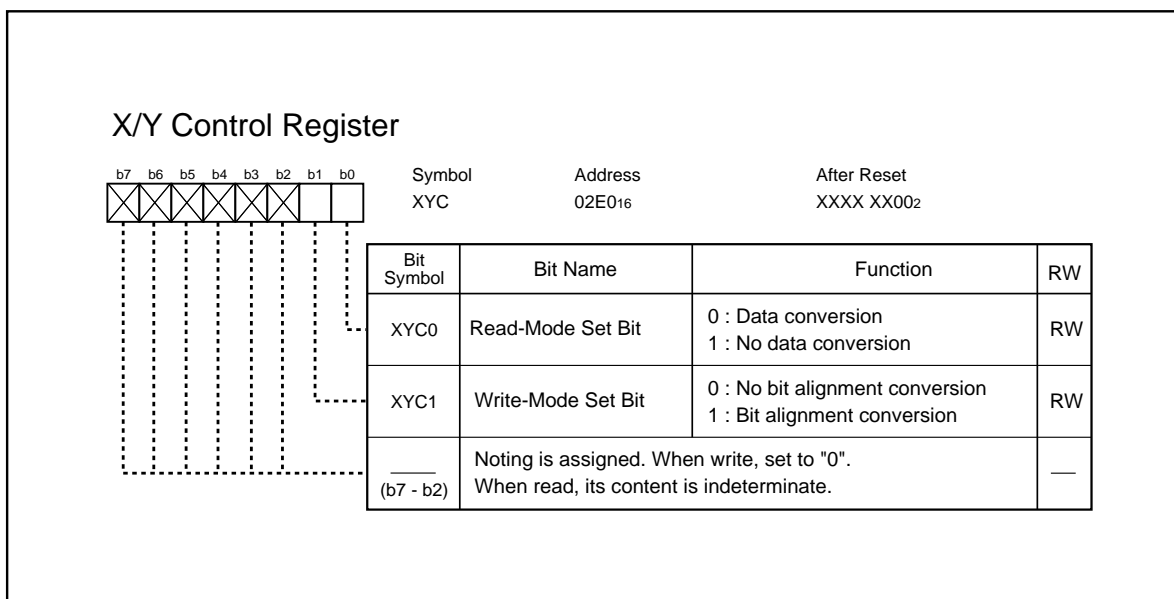


Figure 20.1 XYC Register

The XYC0 bit in the XYC register determines how to read the YjR register.

By reading the YjR register when the XYC0 bit is set to "0" (data conversion), bit j in the X0R to X15R registers can be read simultaneously.

For example, bit 0 in the X0R register can be read if reading bit 0 in the Y0R register, bit 0 in the X1R register if reading bit 1 in the Y0R register..., bit 0 in the X14R register if reading bit 14 in the Y0R register and bit 0 in the X15R register if reading bit 15 in the Y0R register.

Figure 20.2 shows the conversion table when the XYC0 bit is set to "0". Figure 20.3 shows an example of the X/Y conversion.

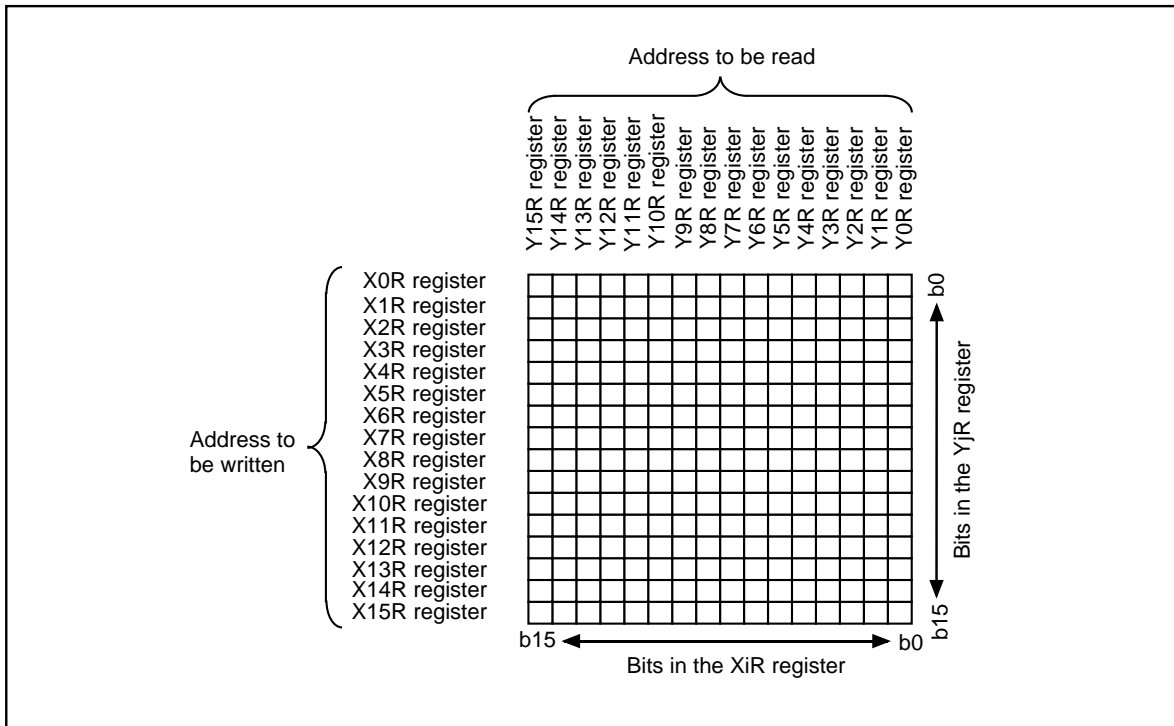


Figure 20.2 Conversion Table when Setting the XYC0 Bit to "0"

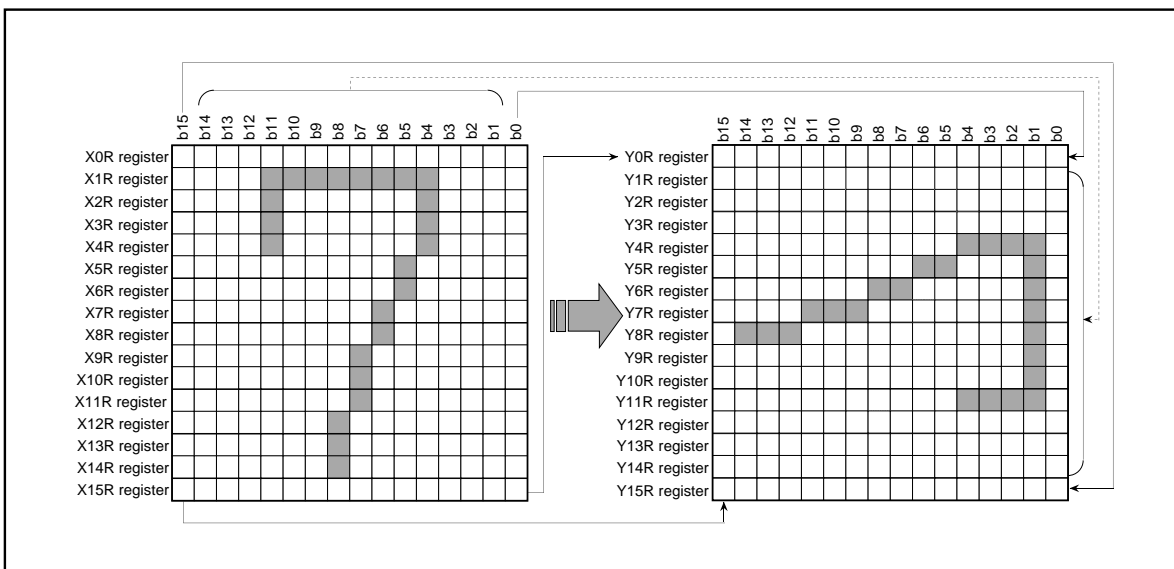


Figure 20.3 X/Y Conversion

By reading the YjR register when the XYC0 bit in the XYC register is set to "1" (no data conversion), the value written to the XiR register can be read directly. Figure 20.4 shows the conversion table when the XYC0 bit is set to "1."

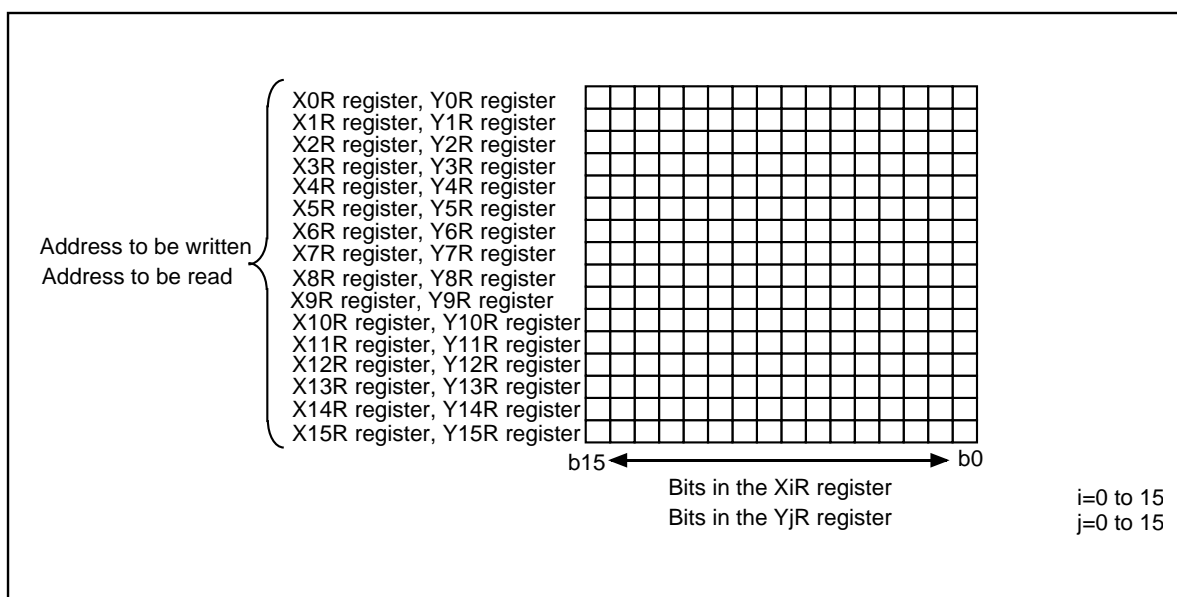


Figure 20.4 Conversion Table when Setting the XYC0 Bit to "1"

The XYC1 bit in the XYC register selects bit alignment of the value in the XiR register.

By writing to the XiR register while the XYC1 bit is set to "0" (no bit alignment conversion), bit alignment is written as is. By writing to the XiR register while the XYC1 bit is set to "1" (bit sequence replaced), bit alignment is written inverted.

Figure 20.5 shows the conversion table when the XYC1 bit is set to "1".

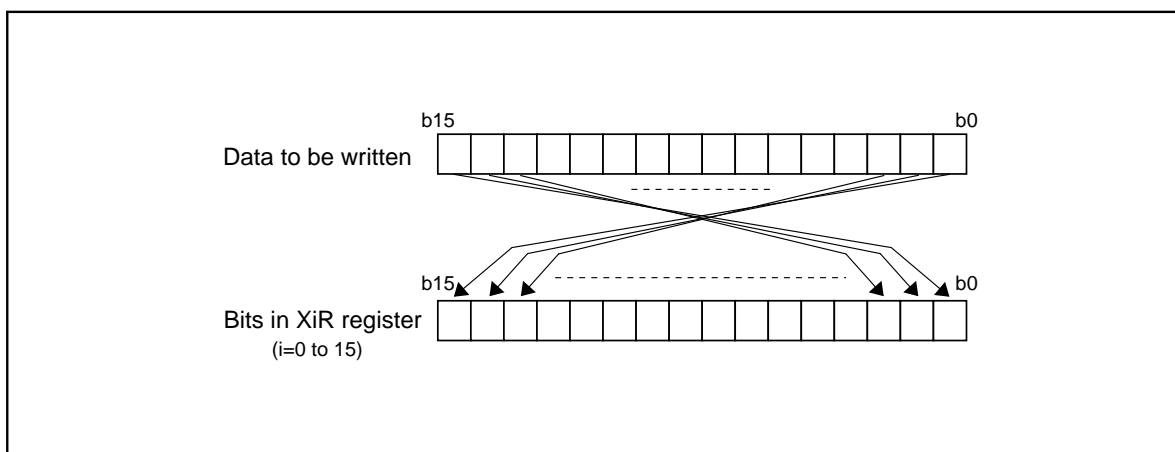


Figure 20.5 Conversion Table when Setting the XYC1 Bit to "1"

21. Intelligent I/O

The intelligent I/O is a multifunctional I/O port for time measurement, waveform generation, clock synchronous serial I/O, clock asynchronous serial I/O (UART), IEBus⁽¹⁾ communications, HDLC data processing and more.

The intelligent I/O consists of four groups. Each group has one 16-bit base timer for free-running operation, eight 16-bit registers for time measurement and waveform generation and two 8-bit shift registers (or one 16-bit shift register) for communications.

Table 21.1 lists functions and channels of the intelligent I/O.

NOTES:

1. IEBus is a trademark of NEC Electronics Corporation.

Table 21.1 Intelligent I/O Functions and Channels

Function	Group 0	Group 1	Group 2	Group 3	Group 0, 1 cascaded
Time Measurement ⁽¹⁾	8 channels (3 channels) ⁽²⁾	4 channels (2 channels)			8 channels (3 channels)
Digital Filter	8 channels (3 channels)	4 channels (2 channels)	Not Available	Not Available	8 channels (3 channels)
Trigger Input Prescaler	2 channels	2 channels			2 channels
Trigger Input Gate	2 channels	2 channels			2 channels
Waveform Generation	4 channels (2 channels)	8 channels (3 channels)	8 channels (3 channels)	8 channels (2 channels)	8 channels (3 channels)
Single-phase Waveform Output					
Phase-delayed Waveform Output	Available	Available			Available
SR Waveform Output			Available	Available	
Bit Modulation PWM Mode					
RTP Mode	Not Available	Not Available			Not Available
Parallel RTP Mode					
Communication	8 bits fixed		Variable	8 or 16 bits	Not Available
Clock Synchronous Serial I/O Mode			Available	Available	
UART Mode	Available		Not Available	Not Available	Not Available
HDLC Data Processing Mode					
IEBus Mode	Not Available		Available		

NOTES:

1. Time measurement function and waveform generation function share pins
2. The number of channels available in the 100-pin package are indicated in parentethese ().

The time measurement function and waveform generation function can be selected for each channel.

The communication function is available by a combination of multiple channels.

Figures 21.1 to 21.4 show block diagram of the intelligent I/O groups 0 to 3.

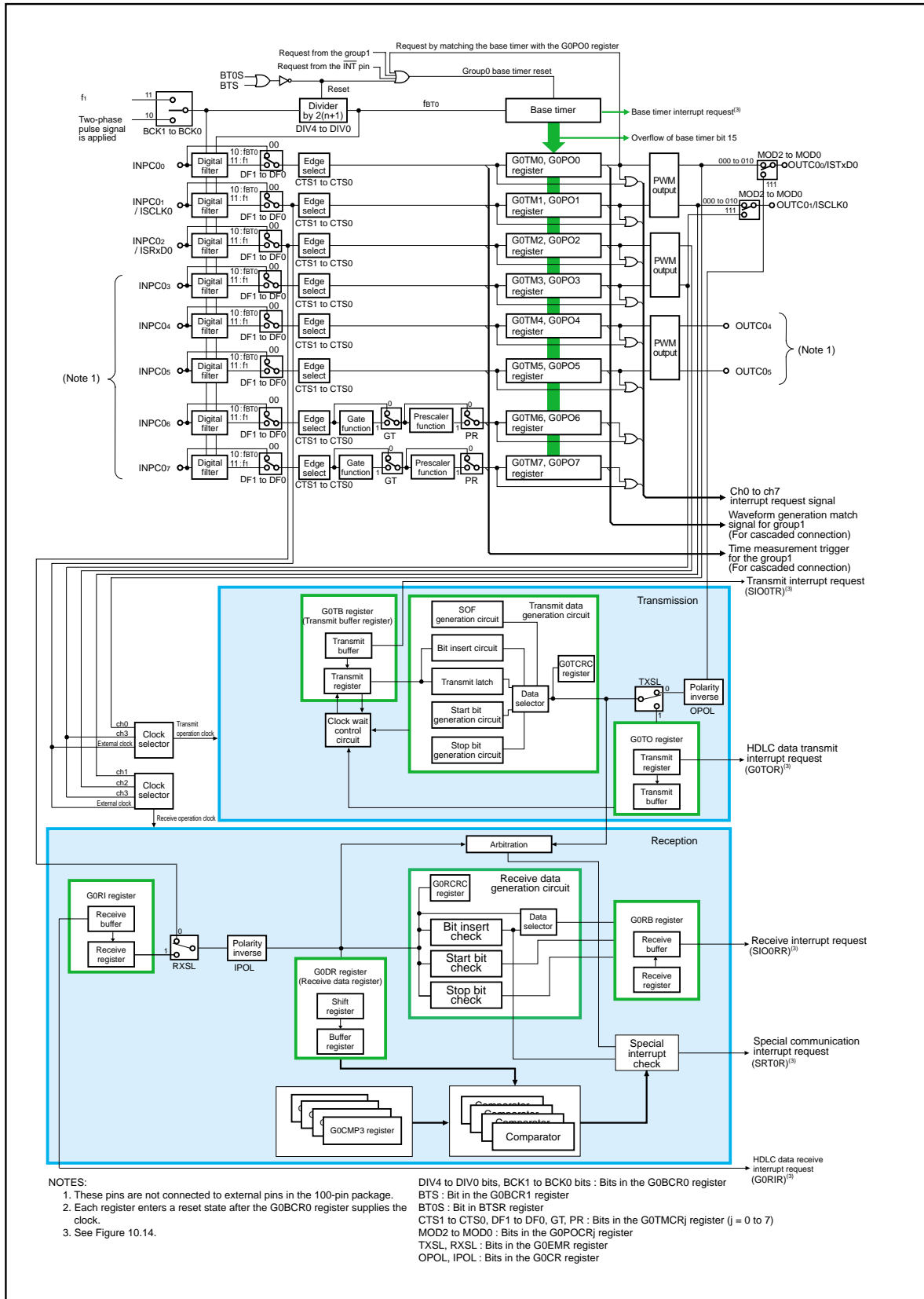


Figure 21.1 Intelligent I/O Group 0 Block Diagram

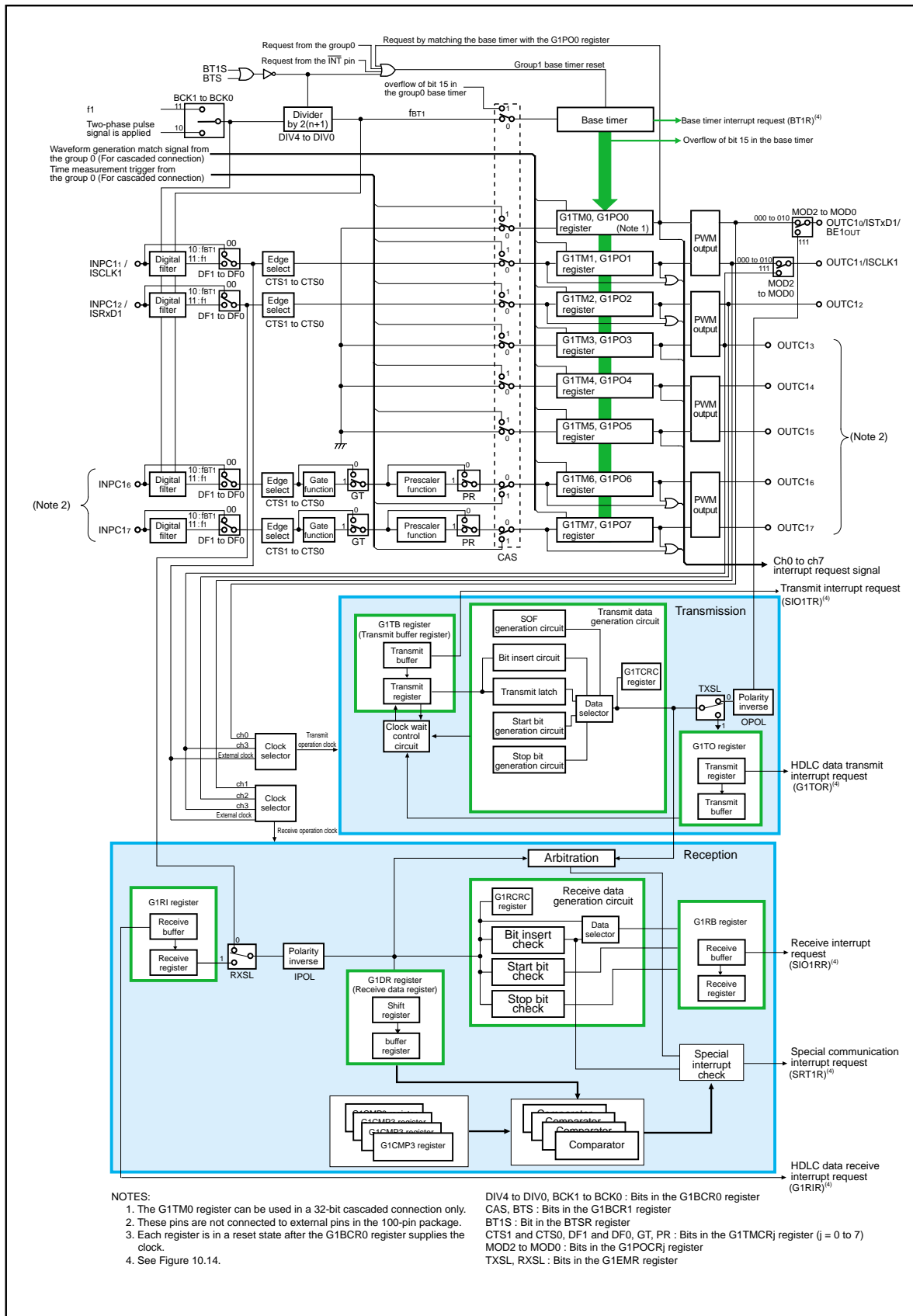


Figure 21.2 Intelligent I/O Group 1 Block Diagram

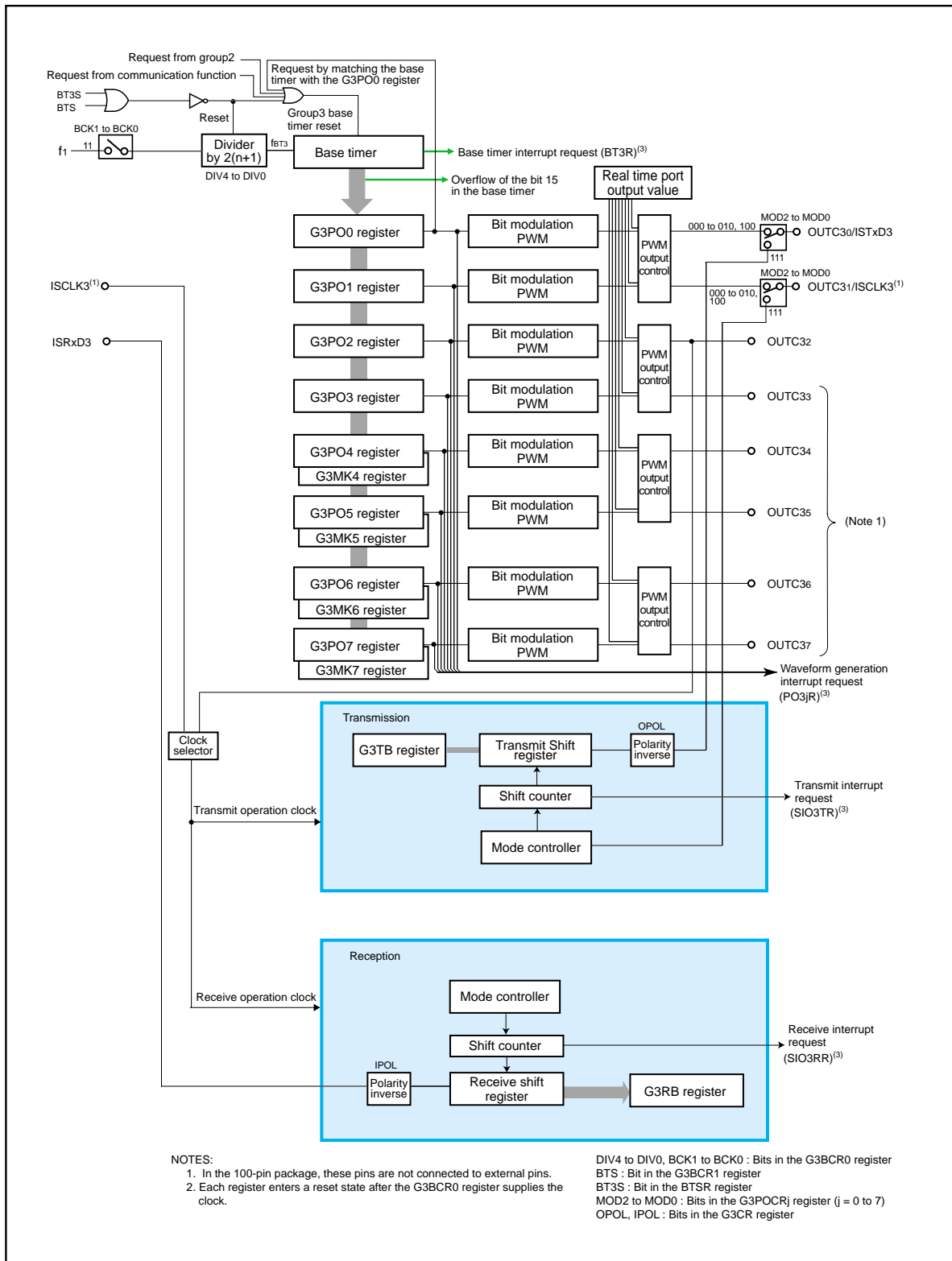


Figure 21.4 Intelligent I/O Group 3 Block Diagram

Figures 21.5 to 21.15 show registers associated with the intelligent I/O base timer, the time measurement function and waveform generation function. (For registers associated with the communication function, see Figures 21.32 to 21.38, Figures 21.42 to 21.45, Figures 21.47 to 21.49.)

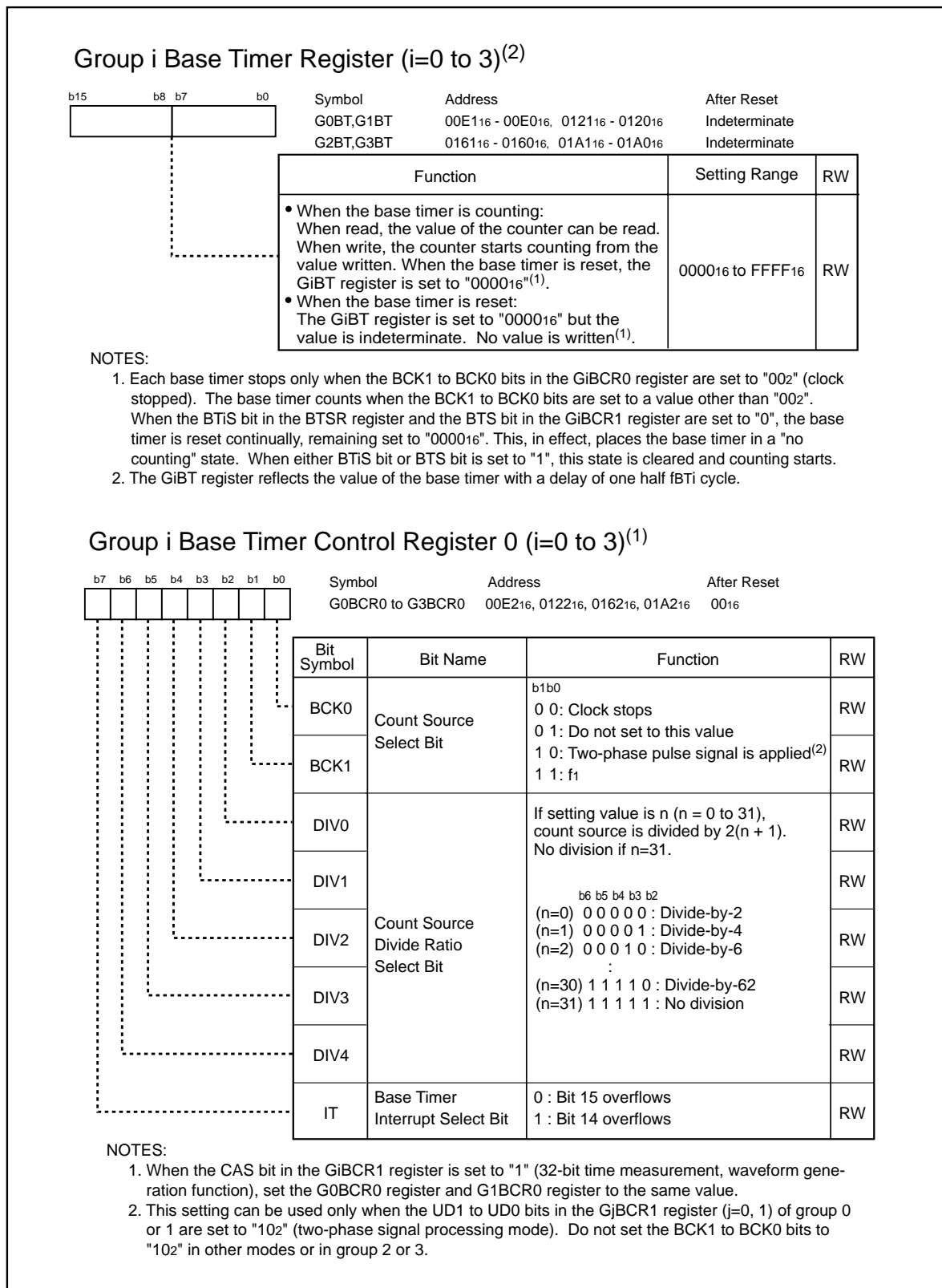


Figure 21.5 G0BT to G3BT Register and G0BCR0 to G3BCR0 Register

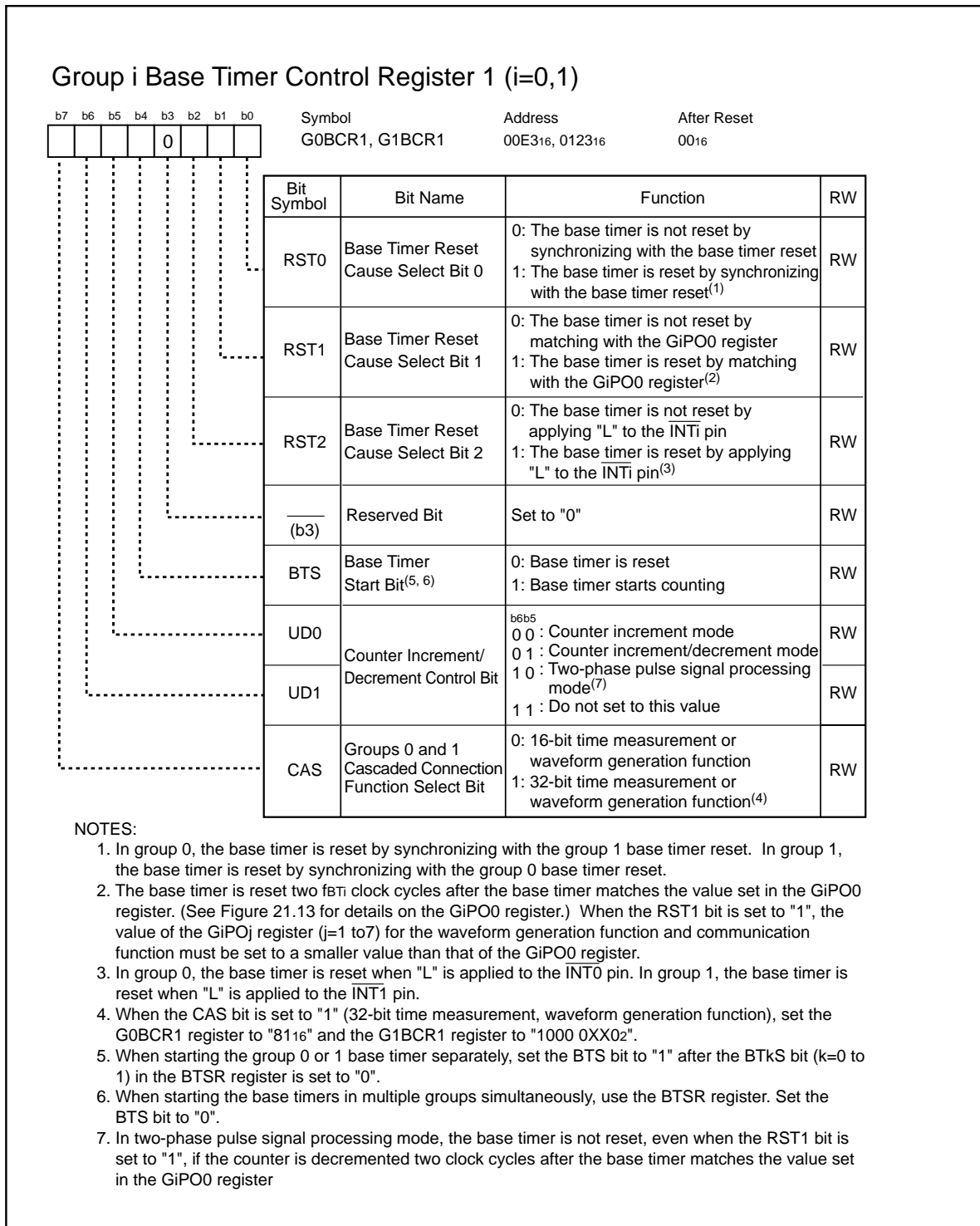


Figure 21.6 G0BCR1 and G1BCR1 Registers

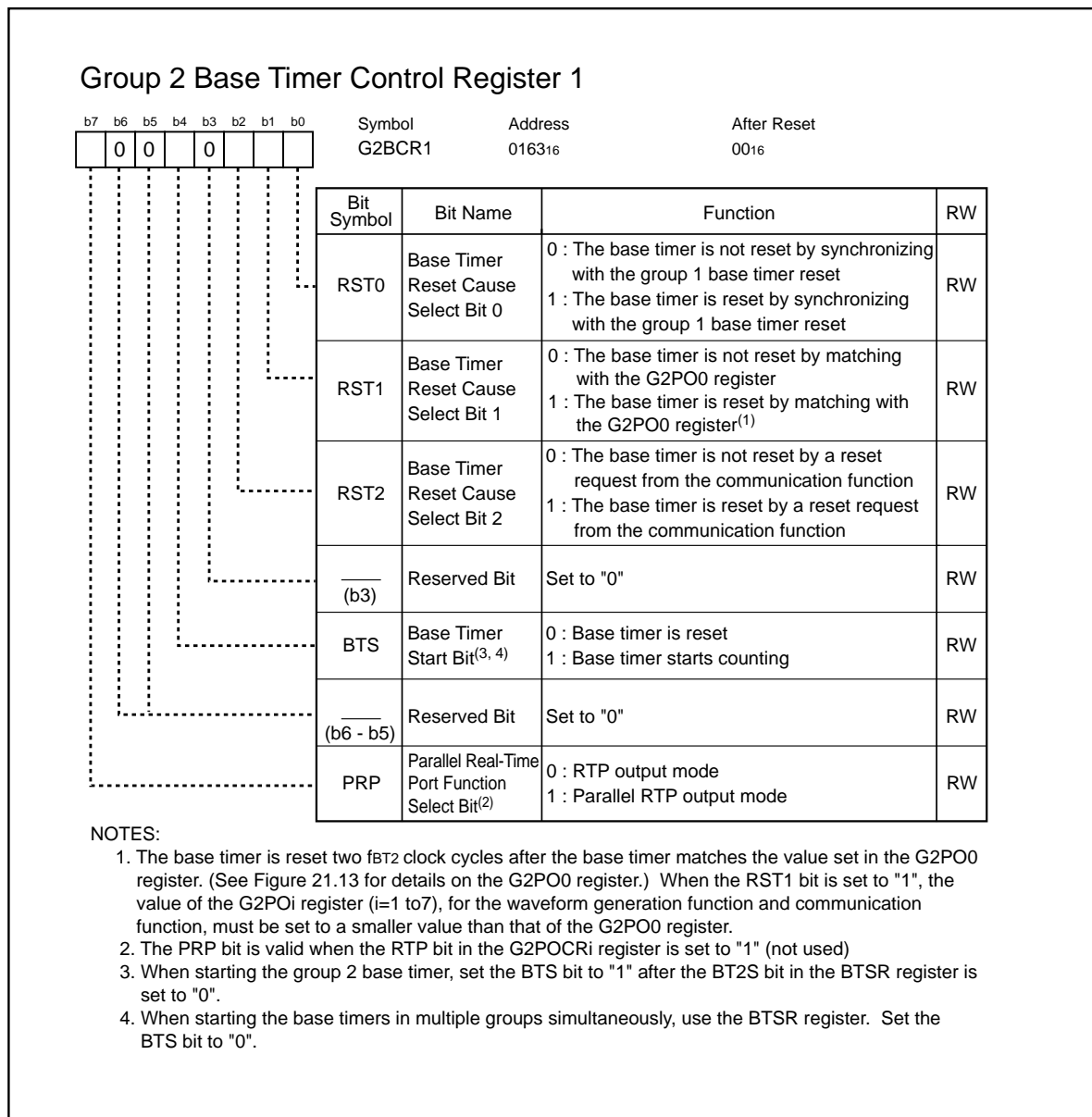


Figure 21.7 G2BCR1 Register

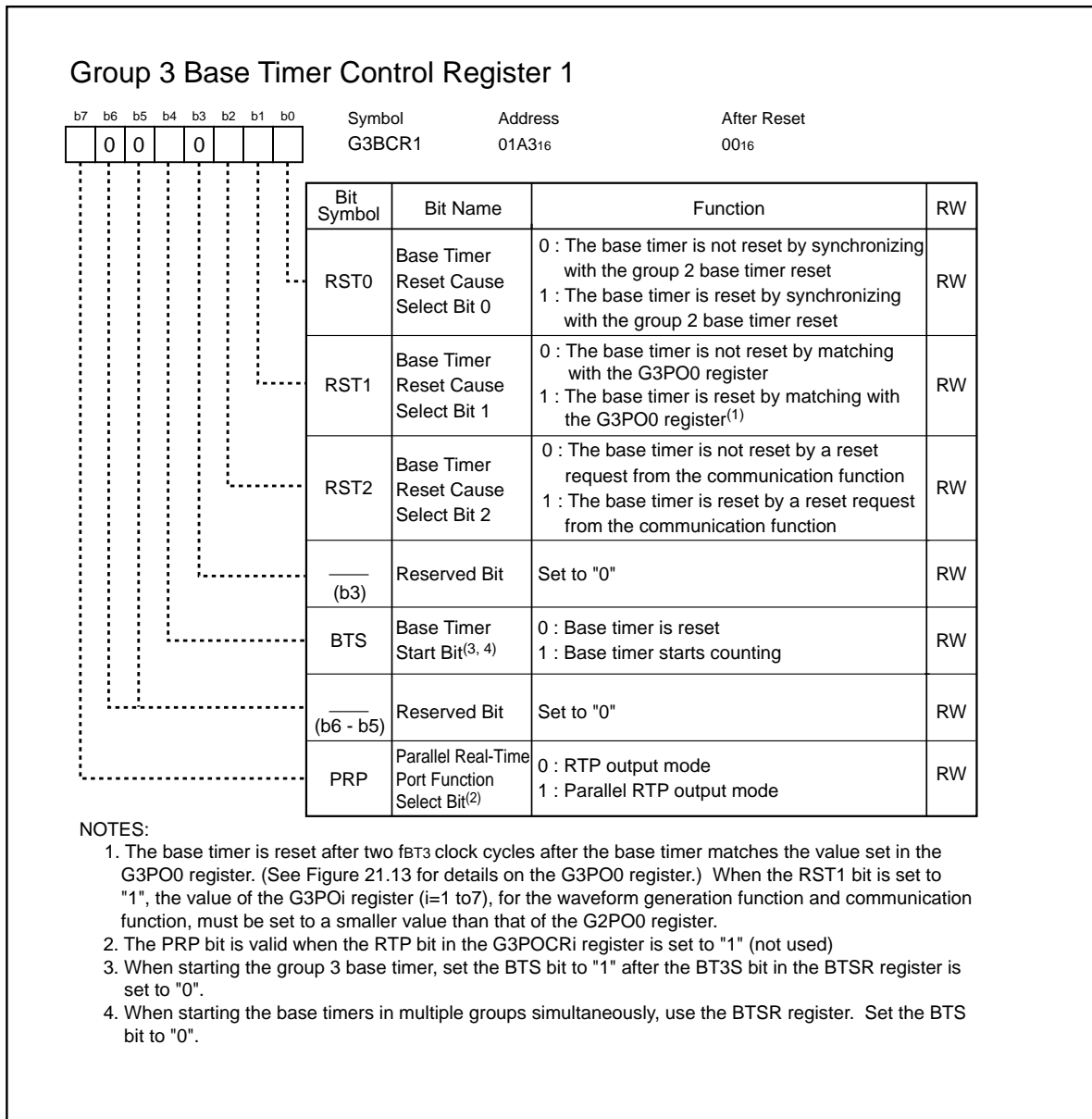


Figure 21.8 G3BCR1 Register

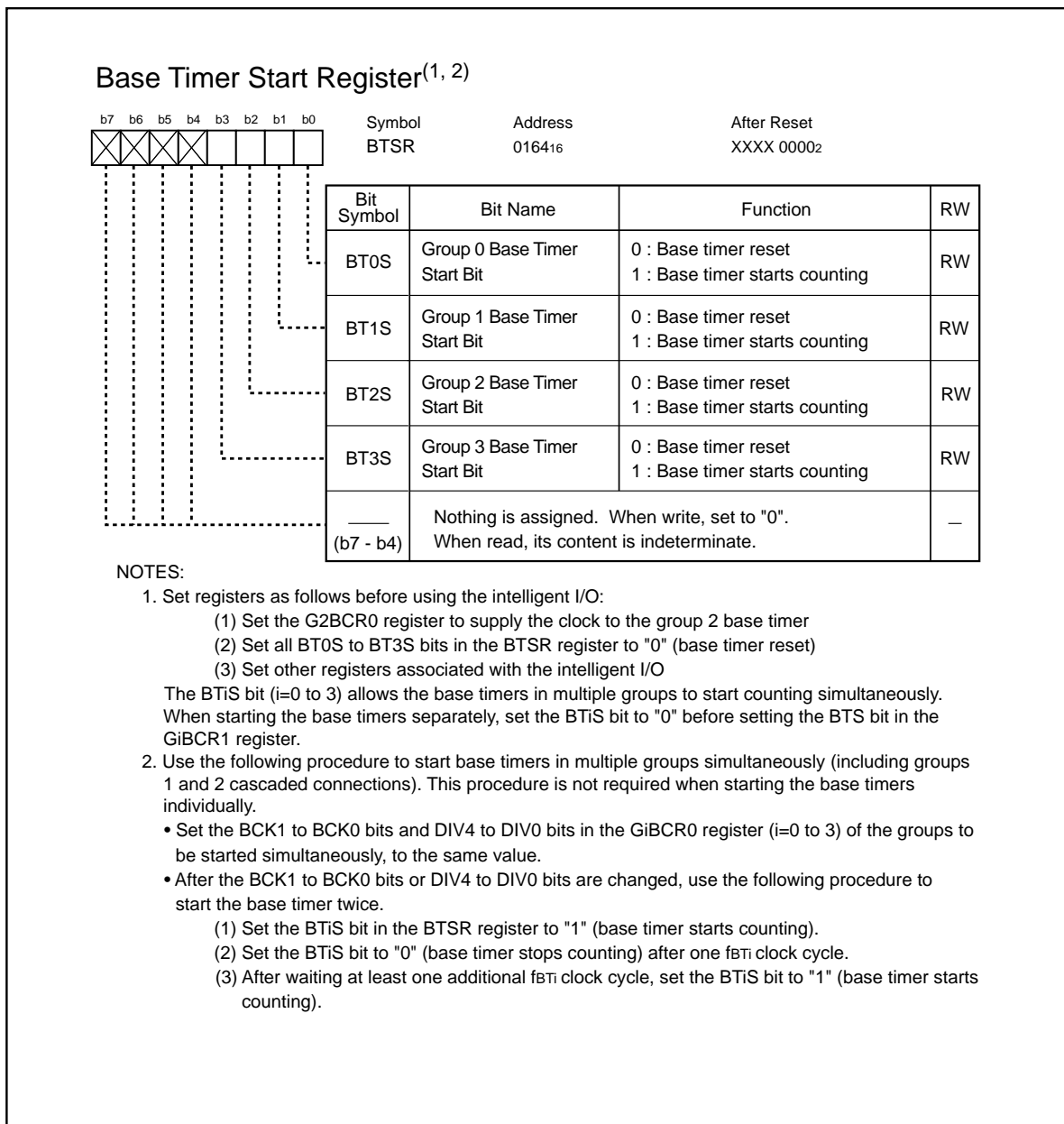
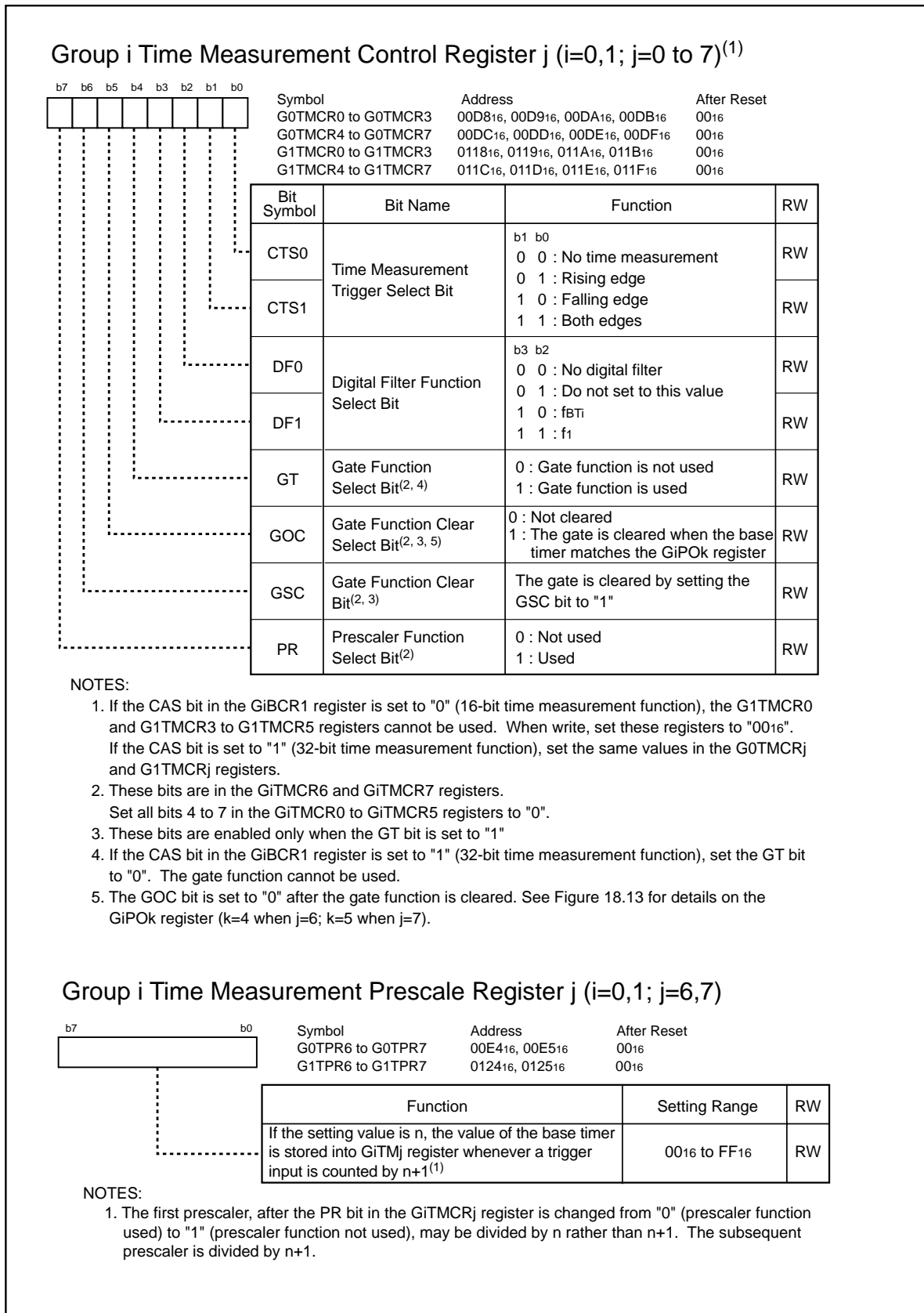


Figure 21.9 BTSR Register



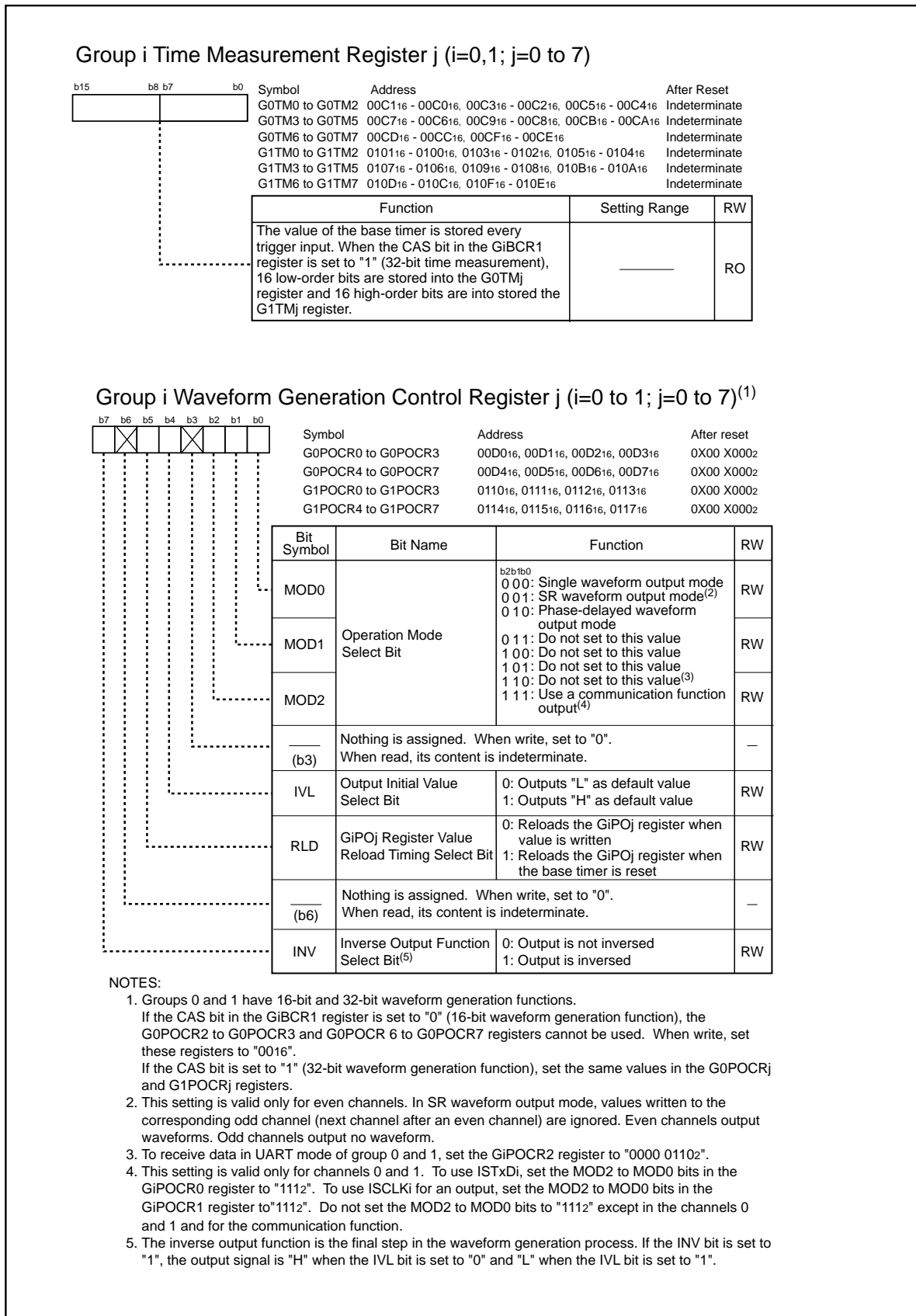


Figure 21.11 G0TM0 to G0TM7, G1TM0 to G1TM7, Registers and G0POCR0 to G0POCR7, G1POCR0 to G1POCR7 Registers

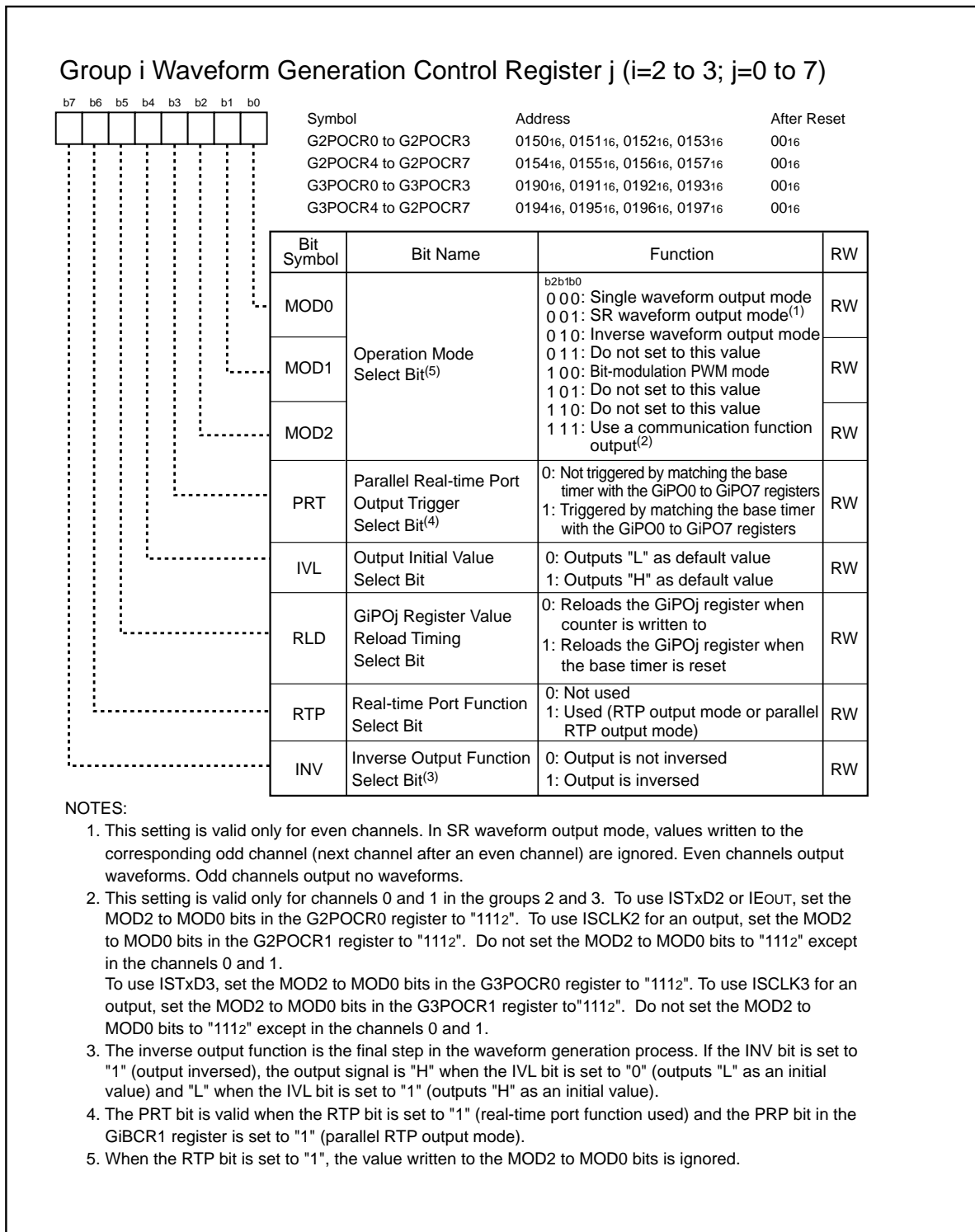


Figure 21.12 G2POCR0 to G2POCR7 and G3POCR0 to G3POCR7 Registers

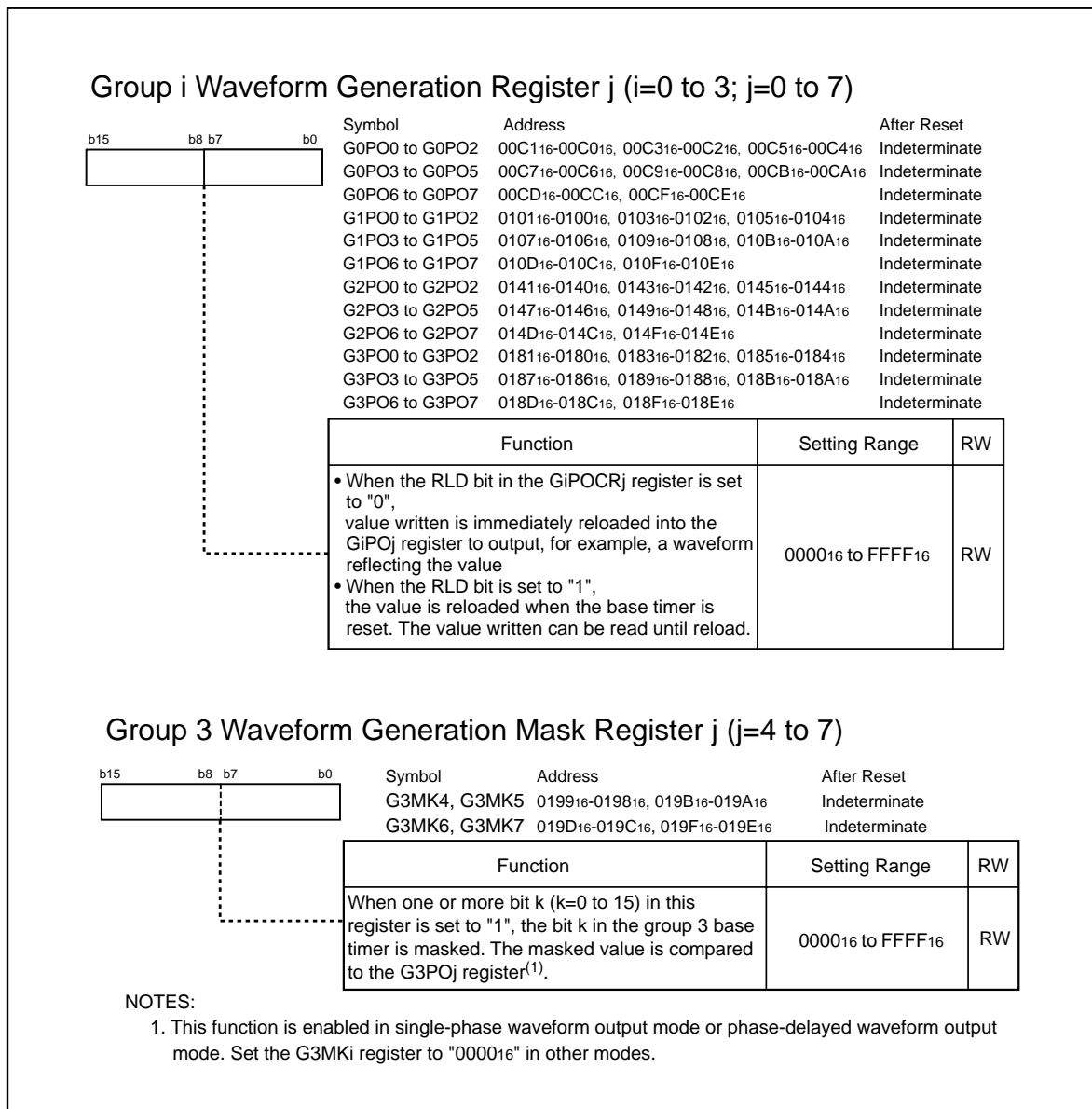


Figure 21.13 G0PO0 to G0PO7, G1PO0 to G1PO7, G2PO0 to G2PO7, G3PO0 to G3PO7 Registers and G3MK4 to G3MK7 Registers

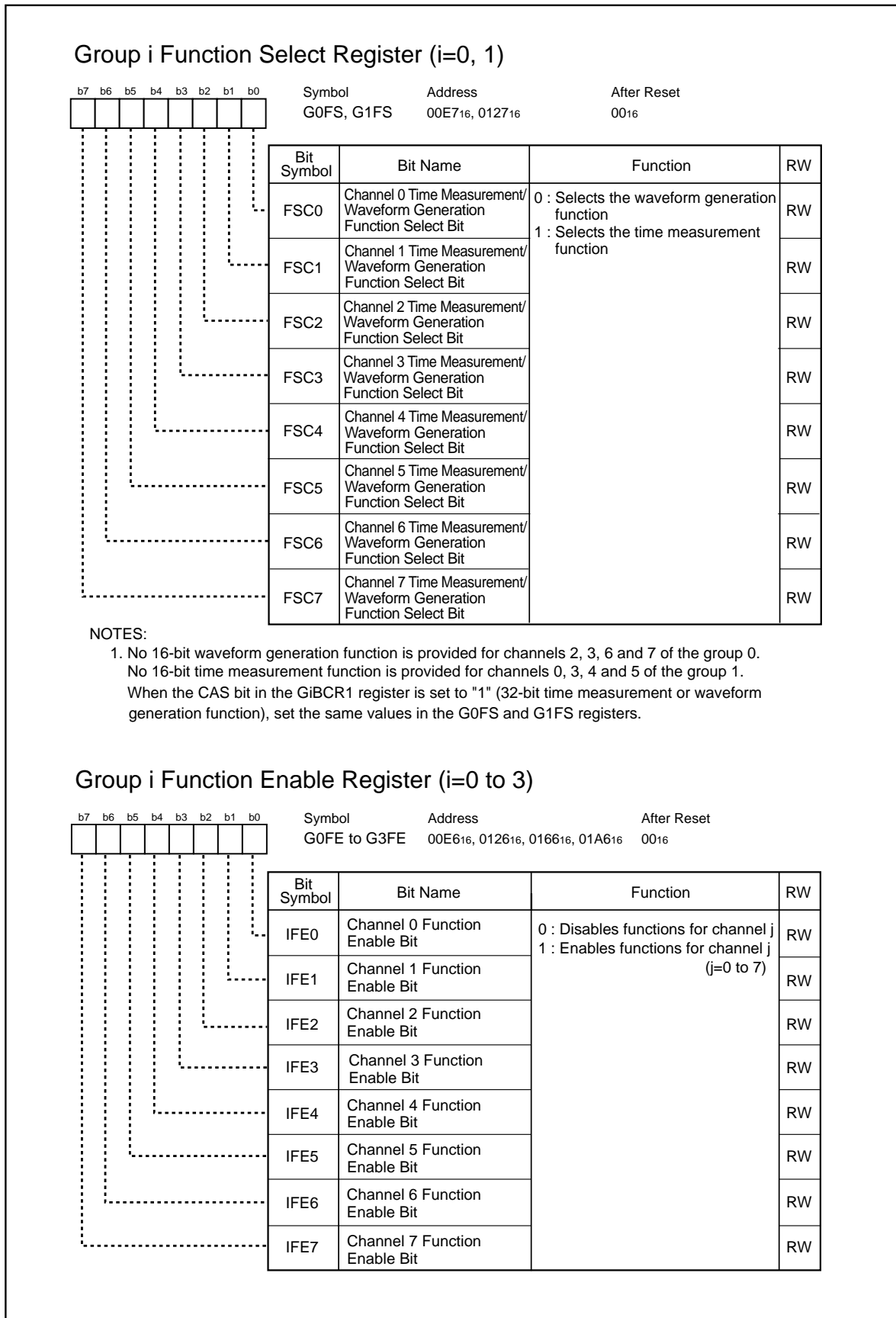


Figure 21.14 G0FS and G1FS Registers and G0FE to G3FE Registers

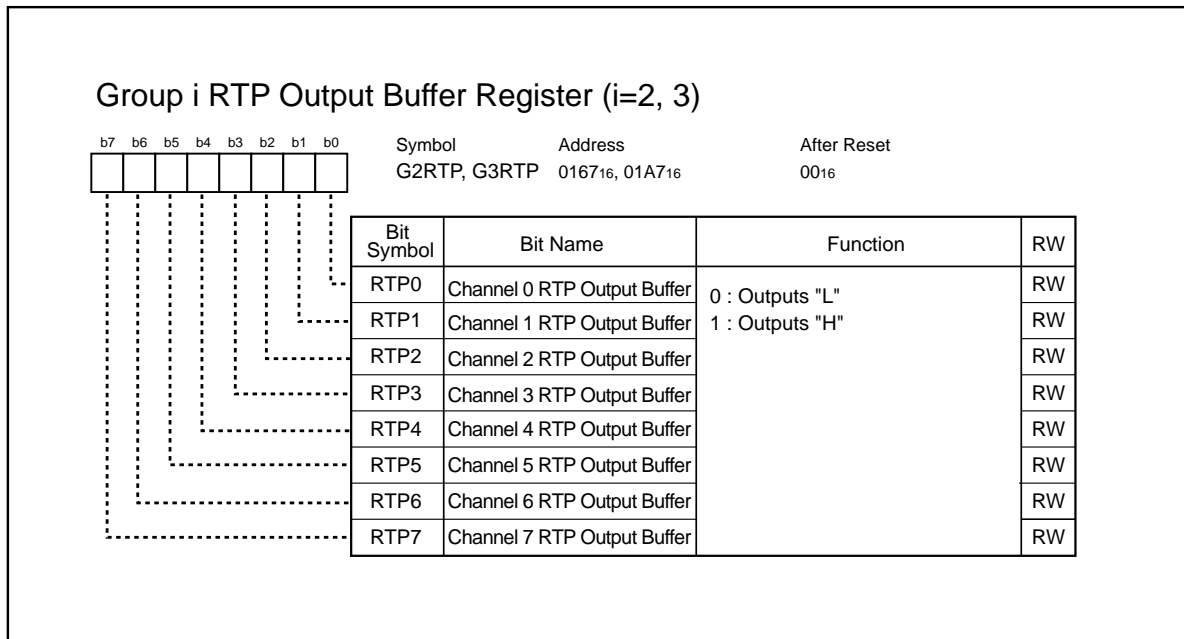


Figure 21.15 G2RTP AND G3RTP Registers

21.1 Base Timer

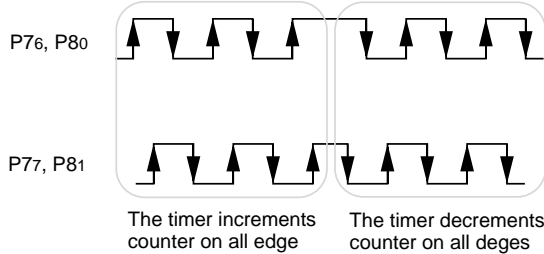
The base timer is a free-running counter that counts an internally generated count source.

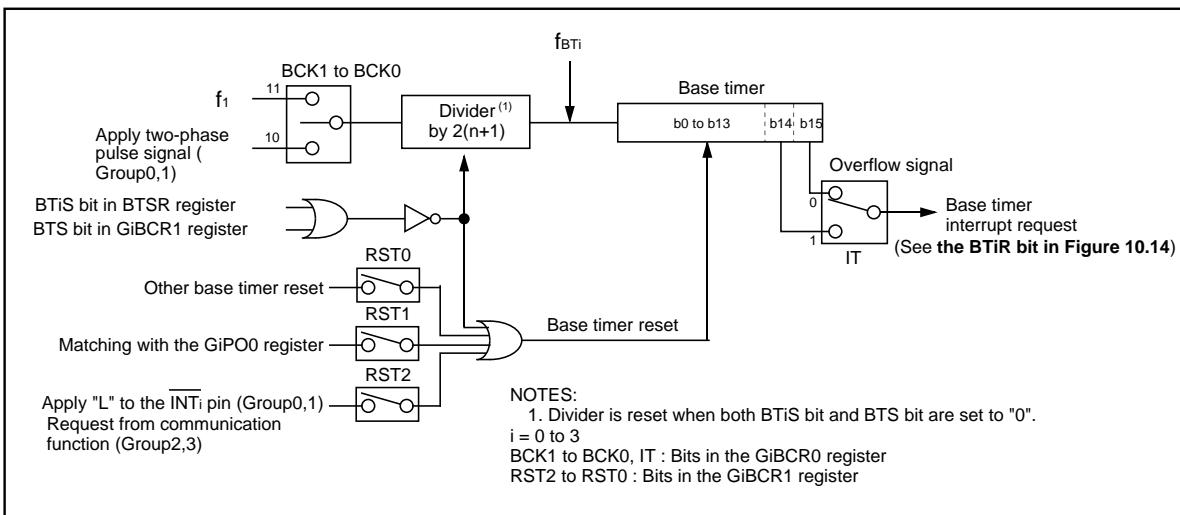
Table 21.2 lists specifications of the base timer. Figures 21.5 to 21.9 show registers associated with the base timer. Figure 21.16 shows a block diagram of the base timer. Figure 21.17 shows an example of a cascaded connection. Figure 21.18 shows an example of the base timer in counter increment mode. Figure 21.19 shows an example of the base timer in counter increment/decrement mode. Figure 21.20 shows an example of two-phase pulse signal processing mode.

Table 21.2 Base Timer Specifications

Item	Specification
Count Source (fBTi) (i=0 to 3)	f1 divided by $2^{(n+1)}$ (Group 0 to 3), two-phase pulse input divided by $2^{(n+1)}$ (Group 0 and 1) n : determined by the DIV4 to DIV0 bits in the GiBCR0 register $n=0$ to 31; however no division when $n=31$
Counting Operation	The base timer increments the counter The base timer increments/decrements the counter Two-phase pulse signal processing
Counter Start Condition	<ul style="list-style-type: none"> When starting the base timer of each group separately, set the BTS bit in the GiBCR1 register to "1" (base timer starts counting) When starting the base timer of multiple groups simultaneously, set the BTIS bit in the B TSR register to "1" (base timer starts counting)
Counter Stop Condition	Set the BTIS bit in the B TSR register to "0" (base timer reset) and the BTS bit in the GiBCR1 register to "0" (base timer reset)
Base Timer Reset Condition	<ul style="list-style-type: none"> Synchronized with the base timer reset in different groups: Group0 : synchronized with group 1 base timer reset Group1 : synchronized with group 0 base timer reset Group2 : synchronized with group 1 base timer reset Group3 : synchronized with group 2 base timer reset Matching values in the base timer and GiPO0 register "L" signal applied to the external interrupt pin Group 0 : INT0 pin Group 1 : INT1 pin Reset request from communication function (Group 2 and 3)
Value when the Base Timer is Reset	"0000 ₁₆ "
Interrupt Request	The BTIR bit in the interrupt request register is set to "1" (interrupt requested) when bit 14 or bit 15 in the base timer overflows (See Figure 10.14.)
Read from Base Timer	<ul style="list-style-type: none"> The GiBT register indicates counter value while the base timer is running The GiBT register is indeterminate when the base timer is reset
Write to Base Timer	When a value is written while the base timer is running, the counter immediately starts counting from this value. No value can be written while the base timer is reset.
Selectable Function	<ul style="list-style-type: none"> Cascaded connection (Group 0 and 1) Group 1 base timer is incremented every time bit 15 in the group 0 base timer overflows (See Figure 21.17) Counter increment/decrement mode (Group 0 and 1) The base timer starts when the BTS bit or the BTIS bit is set to "1". After incrementing to "FFFF₁₆", the counter is then decremented back to "0000₁₆". If the RST1 bit in the GiBCR1 register is set to "1" (the base timer is reset by matching with the GiPO0 register), the counter decrements after the base timer matches the GiPO0 register. The base timer increments the counter again when the counter becomes "0000₁₆." (See Figure 21.19.)

Table 21.2 Base Timer Specifications (Continued)

Item	Specification
Selectable Function	<ul style="list-style-type: none"> Two-phase pulse processing mode (Group 0 and 1) Two-phase pulse signals from P76 and P77 pins in group 0, and P80 and P81 pins in group 1 are counted (See Figure 21.20)  <p>The timer increments counter on all edge The timer decrements counter on all edges</p>

**Figure 21.16 Base Timer Block Diagram****Table 21.3 Base Timer Associated Register Settings (for Time Measurement Function, Waveform Generation Function, and Communication Function)**

Register	Bit	Function
G2BCR0	-	Supplies operation clock to the BTSR register. Set to "0111 11112".
BTSR	-	Set to "0000 00002"
GiBCR0	BCK1 to BCK0	Select count source
	DIV4 to DIV0	Select divide ratio of count source
	IT	Selects the base timer interrupt
GiBCR1	RST2 to RST1	Select factors for a base timer reset
	BTS	Used to start the base timer independently
	UD1 to UD0	Select how to count (Group 0 and 1)
	CAS	Selects cascaded connection (Group 0 and 1)
GiBT	-	Read or write base timer value

Set the following registers to set the RST1 bit to "1" (base timer reset by matching the base timer with the G1PO0 register).

GiPOCR0	MOD2 to MOD0	Set to "0002" (single-phase waveform output mode)
GiPO0	-	Set reset cycle
GiFS	FSC0	Set to "0" (waveform generation function)
GiFE	IFE0	Set to "1" (channel operation start)

i : Bit configurations and functions vary with each group

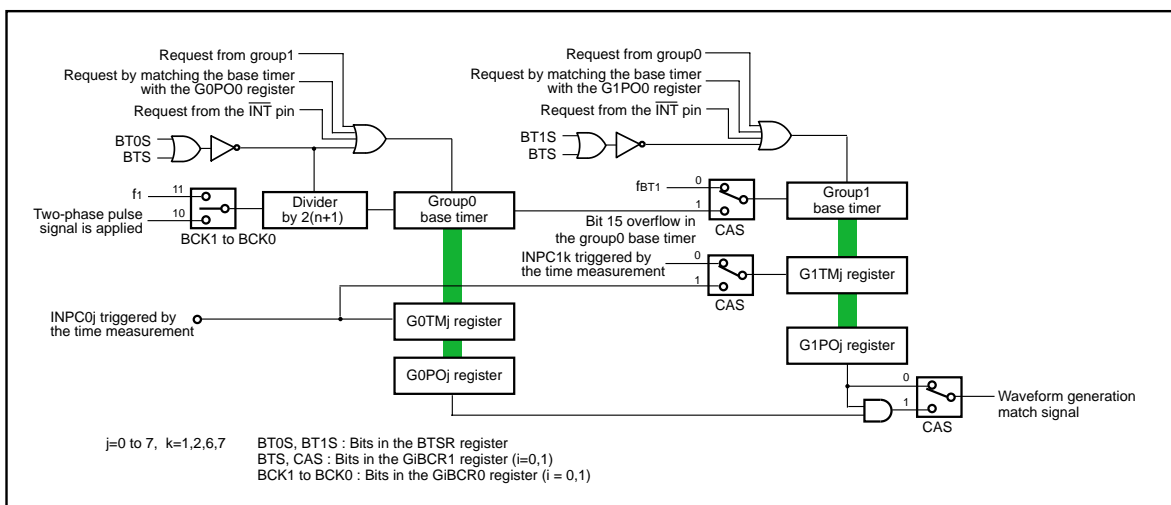


Figure 21.17 Cascaded Connection

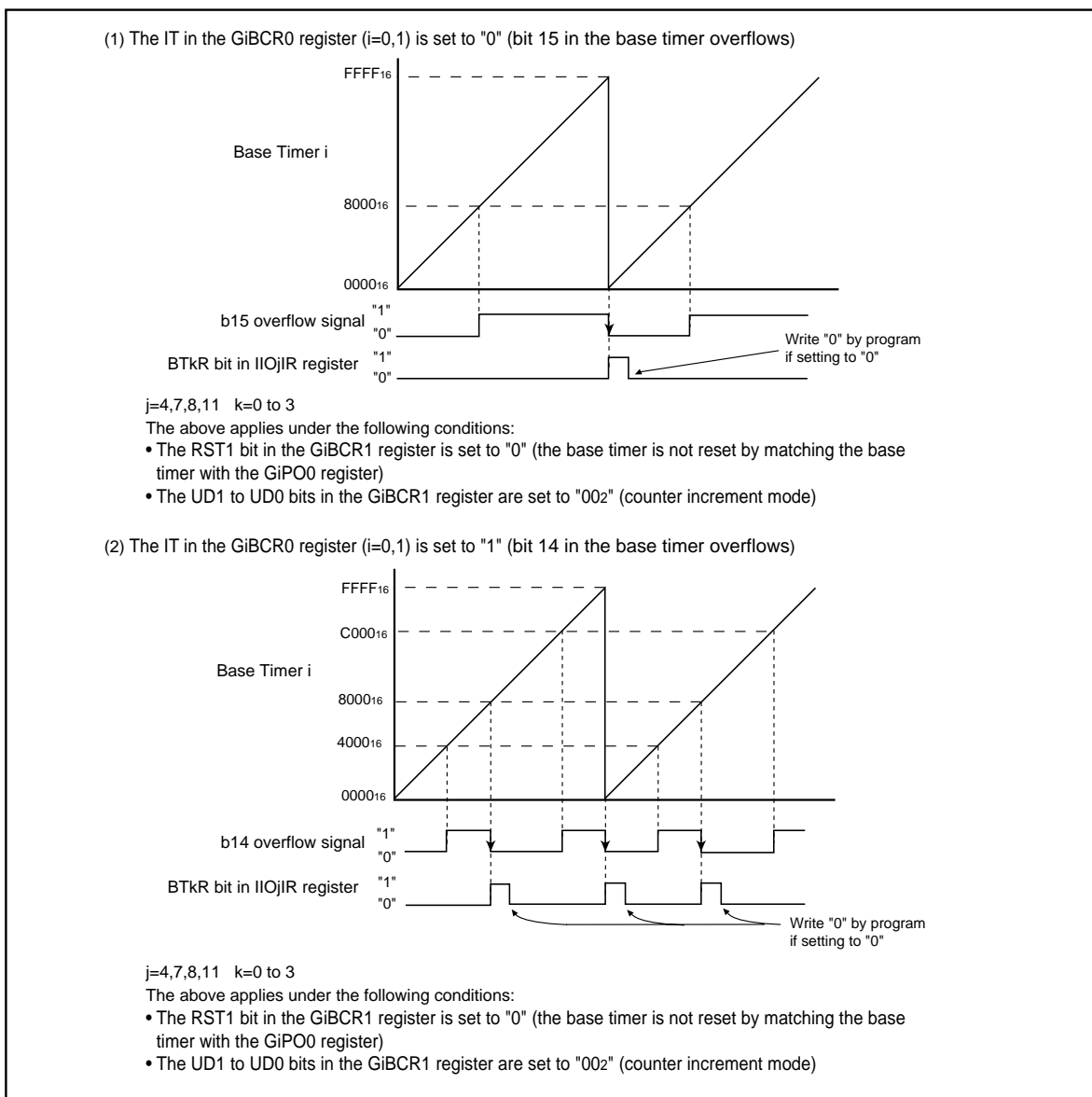


Figure 21.18 Counter Increment Mode (Group 0 and 1)

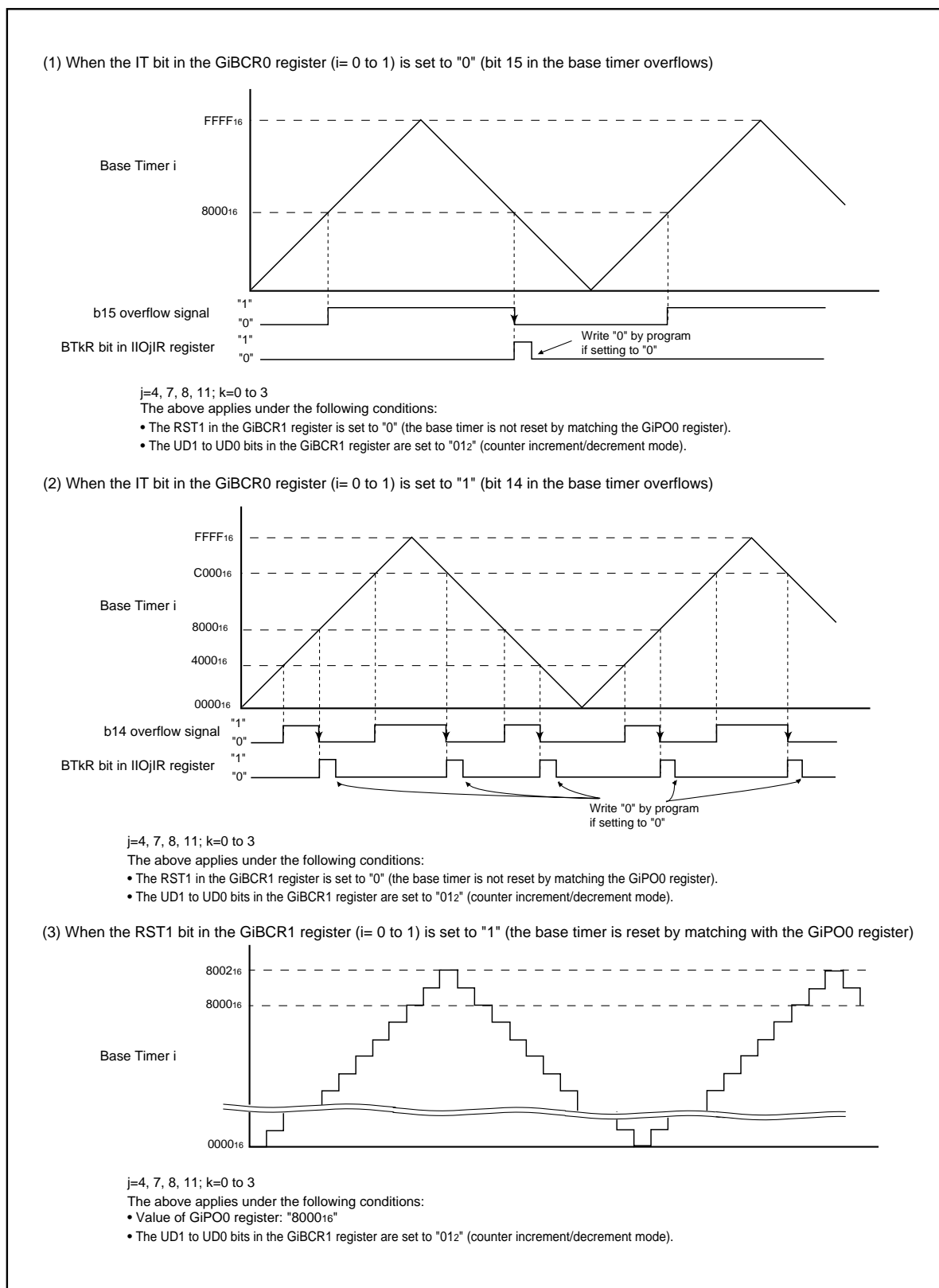


Figure 21.19 Counter Increment/ Decrement Mode (Group 0 and 1)

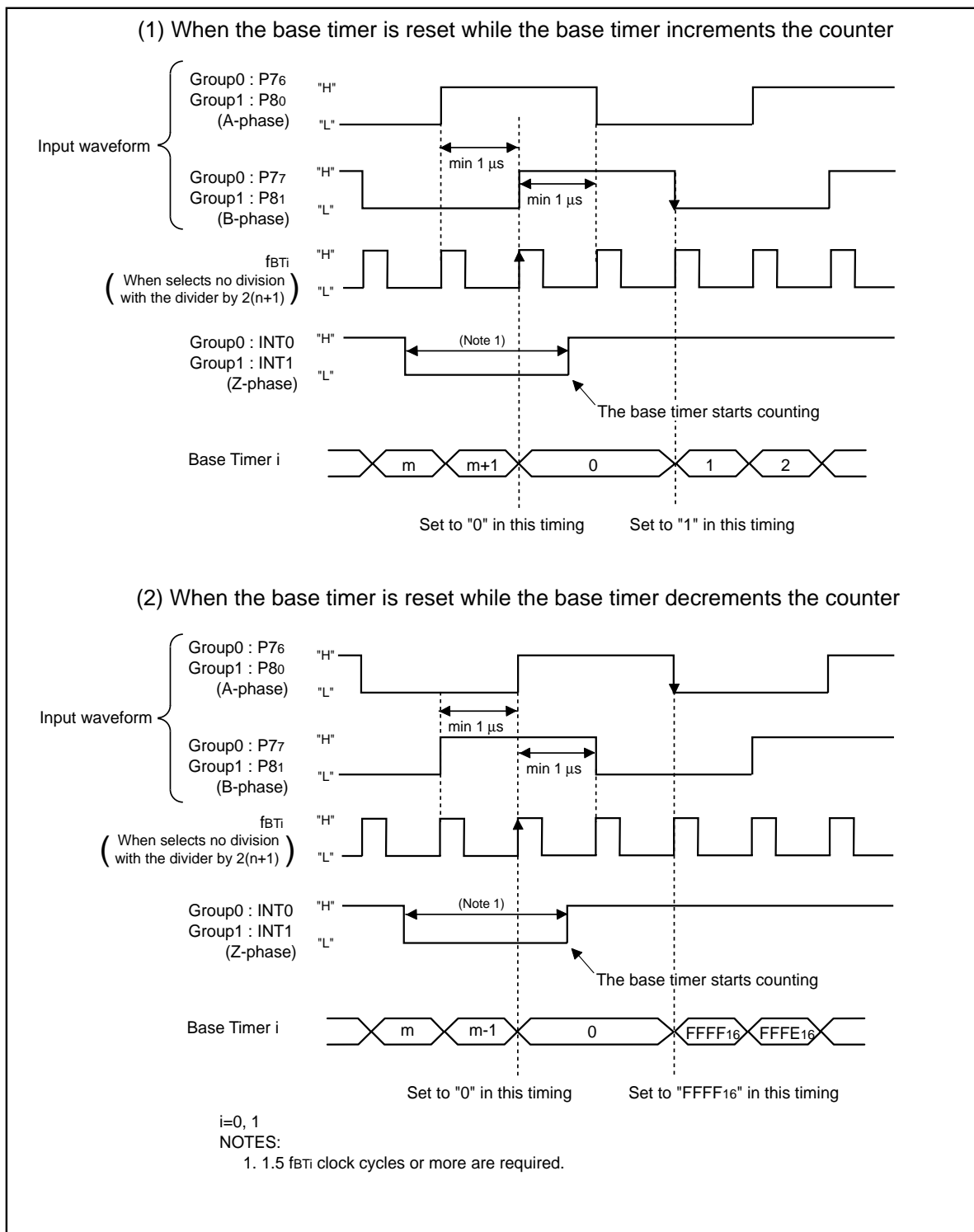


Figure 21.20 Base Timer Operation in Two-phase Pulse Signal Processing Mode (Group 0 and 1)

21.2 Time Measurement Function (Group 0 and 1)

When external trigger is applied, the value of the base timer is stored into the GiTMj register (i=0 to 1; j=0 to 7). Table 21.4 shows specifications of the time measurement function. Table 21.5 lists pin settings of the time measurement function. Table 21.6 lists settings of time measurement function associated registers. Figures 21.21 and 21.22 show operating examples of the time measurement function. Figure 21.23 shows an operating example of the prescaler function and gate function.

Table 21.4 Time Measurement Function Specifications

Item	Specification
Measurement Channel	Group 0: Channels 0 to 7 Group 1: Channels 1, 2, 6, 7
Trigger Input Polarity	Rising edge, falling edge or both edges of the INPCij pin ⁽¹⁾
Measurement Start Condition	The IFEj bit in the GiFE register is set to "1" (channel j function enabled) when the FSCj bit (i=0 to 1; j=0 to 7) in the GiFS register is set to "1" (time measurement function selected)
Measurement Stop Condition	The IFEj bit is set to "0" (channel j function disabled)
Time Measurement Timing	<ul style="list-style-type: none"> No prescaler : every time a trigger signal is applied Prescaler (for channel 6 and channel 7): every <i>GiTPRk register (k=6, 7) + 1</i> times a trigger signal is applied
Interrupt Request Generation Timing	The TMijR bit in the interrupt request register (See Figure 10.14) is set to "1" (interrupt requested) at time measurement timing
INPCij Pin Function ⁽¹⁾	Trigger input pin
Selectable Function	<ul style="list-style-type: none"> Digital filter function The digital filter samples a trigger input signal level every f1 or fBTi cycles and passes pulse signals, matching trigger input signal level, three times Cascaded connection function Group 0 and group 1 are connected to operate as a 32-bit base timer Prescaler function (for channel 6 and channel 7) Time measurement is executed every <i>GiTPRk register value + 1</i> times a trigger signal is applied Gate function (for channel 6 and channel 7) After time measurement by the first trigger input, trigger input cannot be received. However, trigger input can be received again by matching the base timer with the GiPOp register, or by setting the GSC bit in the GiTMCRk register to "1", when the GOC bit in the GiTMCRk register is set to "1" (gate cleared by matching the base timer with the GiPOp register (p=4 when k=6, p=5 when k=7))

NOTES:

- INPC00 to INPC07, INPC11 to INPC12, INPC16 to INPC17 pins (INPC00 to INPC07 pins during cascaded connection)

Table 21.5 Pin Settings for Time Measurement Function

Pin ⁽²⁾	Bit and Setting		
	PS1, PS2, PS5, PS8, PS9 Registers	PD7, PD8, PD11, PD14, PD15 Registers	IPS Register
P74/INPC11	PS1_4 = 0	PD7_4 = 0	IPS1 = 0
P75/INPC12	PS1_5 = 0	PD7_5 = 0	
P76/INPC00	PS1_6 = 0	PD7_6 = 0	IPS0 = 0
P77/INPC01	PS1_7 = 0	PD7_7 = 0	
P80/INPC02	PS2_0 = 0	PD8_0 = 0	
P111/INPC11 ⁽¹⁾	PS5_1 = 0	PD11_1 = 0	IPS1 = 1
P112/INPC12 ⁽¹⁾	PS5_2 = 0	PD11_2 = 0	
P142/INPC16 ⁽¹⁾	PS8_2 = 0	PD14_2 = 0	—
P143/INPC17 ⁽¹⁾	PS8_3 = 0	PD14_3 = 0	
P150/INPC00 ⁽¹⁾	PS9_0 = 0	PD15_0 = 0	IPS0 = 1, IPS2 = 0
P151/INPC01 ⁽¹⁾	PS9_1 = 0	PD15_1 = 0	
P152/INPC02 ⁽¹⁾	—	PD15_2 = 0	
P153/INPC03 ⁽¹⁾	—	PD15_3 = 0	IPS2 = 0
P154/INPC04 ⁽¹⁾	PS9_4 = 0	PD15_4 = 0	
P155/INPC05 ⁽¹⁾	PS9_5 = 0	PD15_5 = 0	
P156/INPC06 ⁽¹⁾	—	PD15_6 = 0	
P157/INPC07 ⁽¹⁾	—	PD15_7 = 0	

NOTES:

1. This port is provided in the 144-pin package only.
2. Apply trigger to INPC0j pin (j=0 to 7) when the CAS bit in the GiBCR register is set to "1" (32-bit time measurement function). Trigger input to INPC1k pin (k=1, 2, 6, 7) is invalid.

Table 21.6 Time Measurement Function Associated Register Settings

Register	Bit	Function
GiTMCRj	CTS1 to CTS0	Select a time measurement trigger
	DF1 to DF0	Select the digital filter function
	GT, GOC, GSC	Select the gate function
	PR	Select the prescaler function
GiTPRk	-	Setting value of the prescaler
GiFS	FSCj	Set to "1" (time measurement function)
GiFE	IFEj	Set to "1" (channel j function enabled)

i = 0 to 1; j = 0 to 7; k = 6, 7

Bit configurations and functions vary with channels and groups used.

Registers associated with the time measurement function must be set after setting registers associated with the base timer.

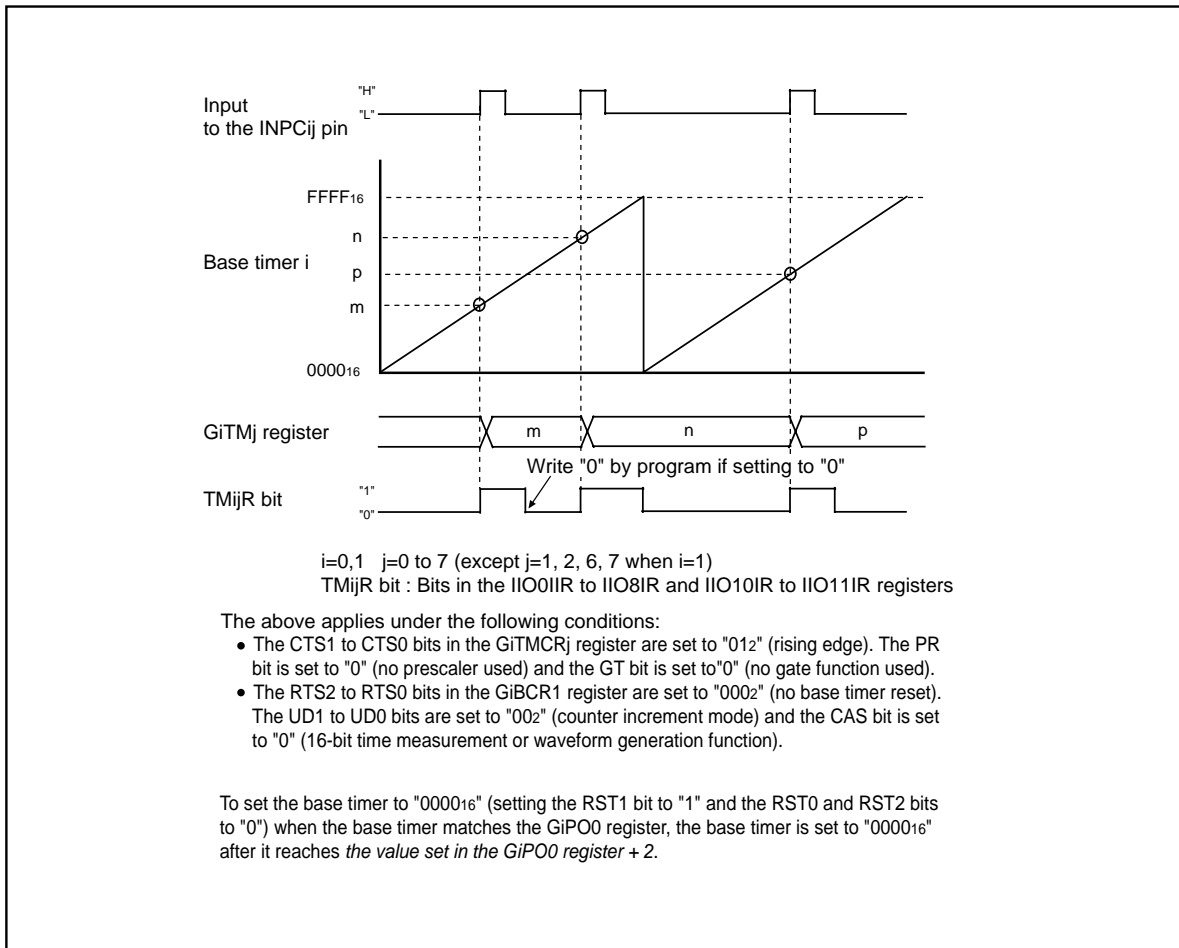


Figure 21.21 Time Measurement Function (1)

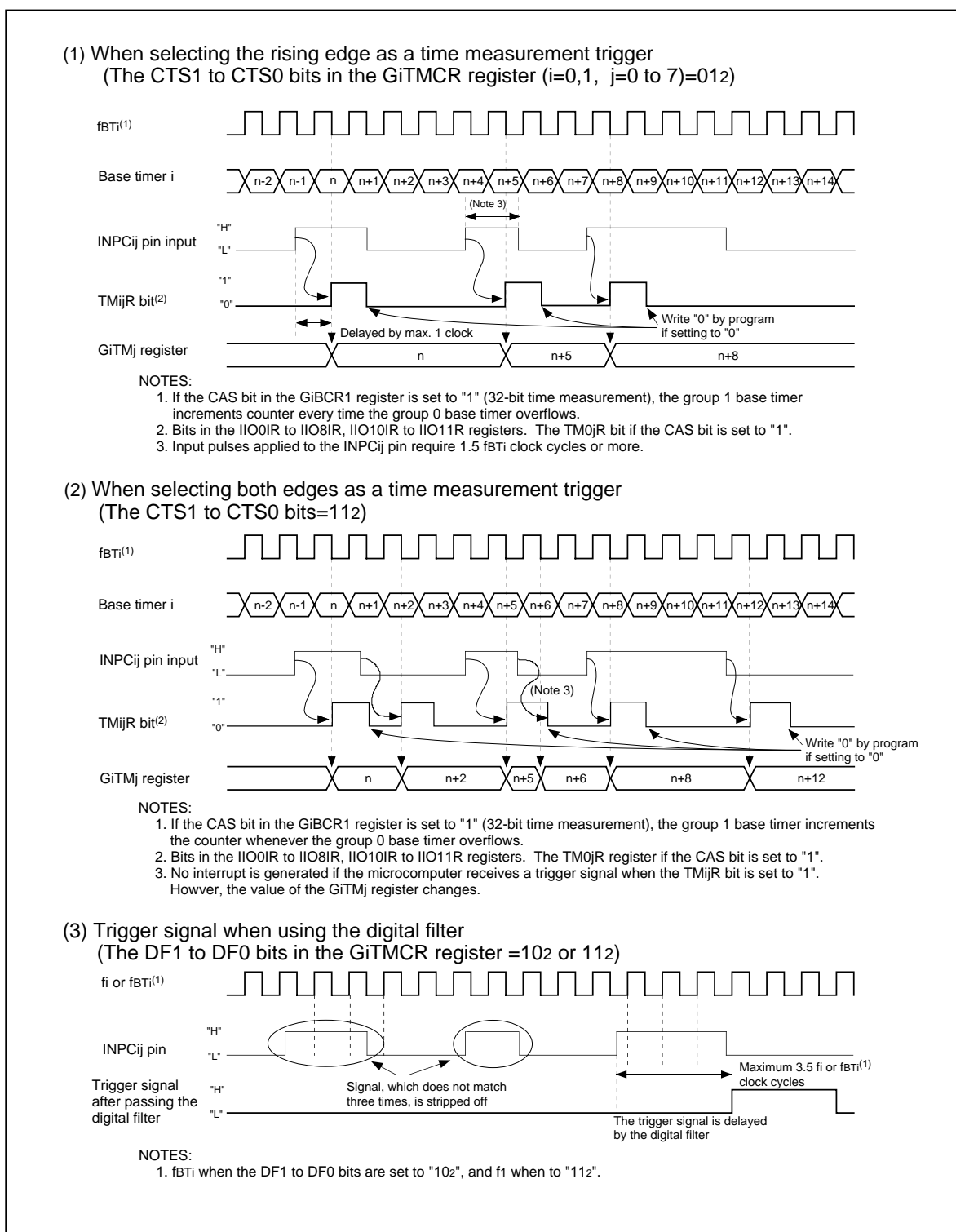


Figure 21.22 Time Measurement Function (2)

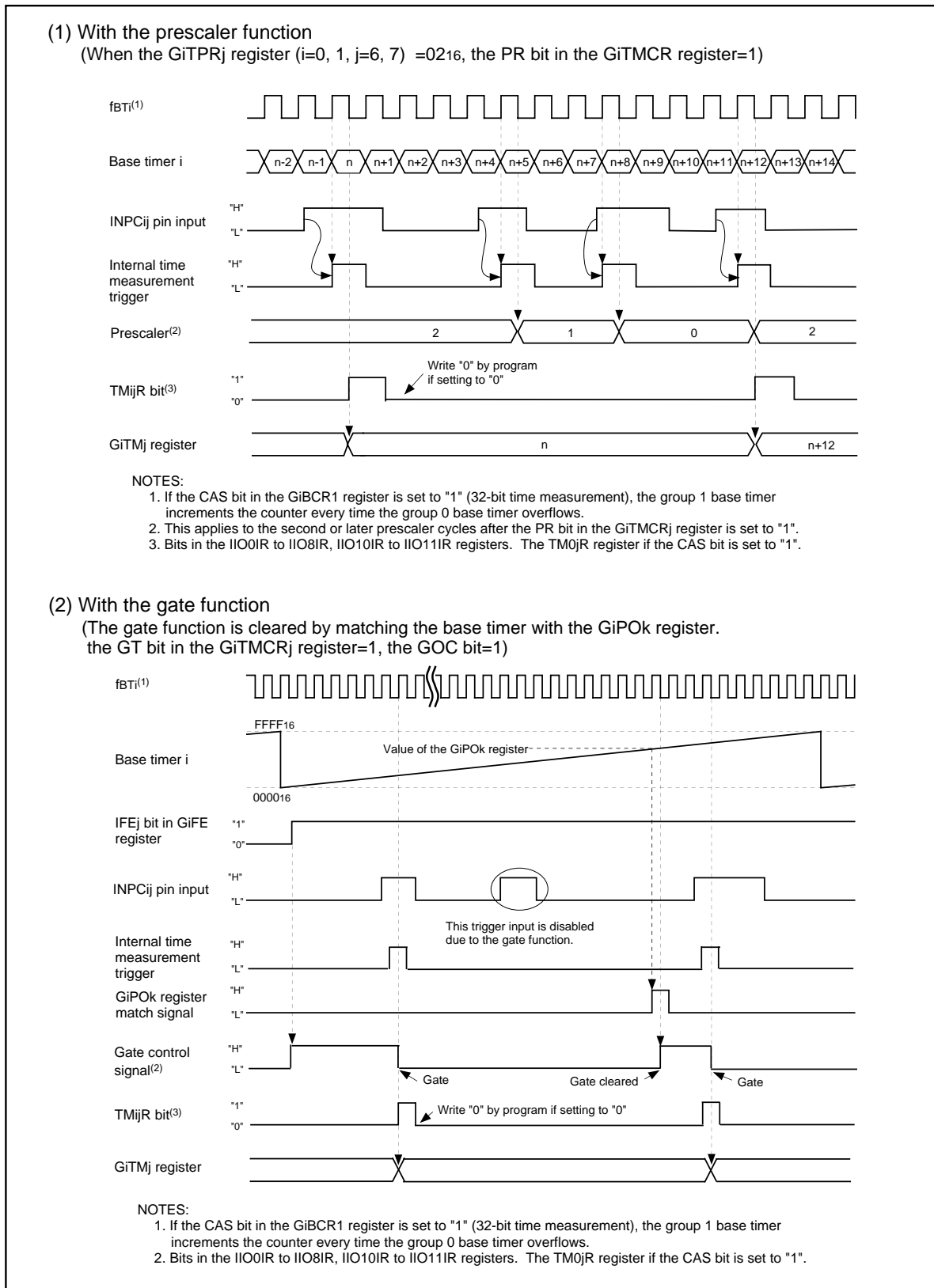


Figure 21.23 Prescaler Function and Gate Function

21.3 Waveform Generation Function

Waveforms are generated when the value of the base timer matches the GiPOj register (i=0 to 3; j=0 to 7).

The waveform generation function has the following six modes :

- Single-phase waveform output mode (group 0 to 3)
- Phase-delayed waveform output mode (group 0 to 3)
- Set/Reset waveform output (SR waveform output) mode (group 0 to 3)
- Bit modulation PWM output mode (group 2 and 3)
- Real-time port output (RTP output) mode (group 2 and 3)
- Parallel real-time port output (parallel RTP output) mode (group 2 and 3)

Table 21.7 lists pin settings of the waveform generation function. Table 21.8 lists registers associated with the waveform generation function.

Table 21.7 Pin Settings for Waveform Generation Function (1/2)

Pin	Bit and Setting		
	PS0 to PS2, PS5 to PS9 Registers	PSL0, PSL1, PSL2, PSL3 Registers	PSC Register
P64/OUTC21	PS0_4 = 1	PSL0_4 = 1	-
P70/OUTC20	PS1_0 = 1	PSL1_0 = 0	PSC_0 = 1
P71/OUTC22	PS1_1 = 1	PSL1_1 = 0	PSC_1 = 1
P73/OUTC10 ⁽²⁾	PS1_3 = 1	PSL1_3 = 0	PSC_3 = 1
P74/OUTC11 ⁽²⁾	PS1_4 = 1	PSL1_4 = 0	PSC_4 = 1
P75/OUTC12 ⁽²⁾	PS1_5 = 1	PSL1_5 = 1	-
P76/OUTC00 ⁽²⁾	PS1_6 = 1	PSL1_6 = 0	PSC_6 = 0
P77/OUTC01 ⁽²⁾	PS1_7 = 1	-	-
P81/OUTC30	PS2_1 = 1	PSL2_1 = 1	-
P82/OUTC32	PS2_2 = 1	PSL2_2 = 0	-
P92/OUTC20	PS3_2 = 1	PSL3_2 = 1	-
P110/OUTC10 ^(1,2)	PS5_0 = 1	-	-
P111/OUTC11 ^(1,2)	PS5_1 = 1		
P112/OUTC12 ^(1,2)	PS5_2 = 1		
P113/OUTC13 ^(1,2)	PS5_3 = 1		
P120/OUTC30 ⁽¹⁾	PS6_0 = 1	-	-
P121/OUTC31 ⁽¹⁾	PS6_1 = 1		
P122/OUTC32 ⁽¹⁾	PS6_2 = 1		
P123/OUTC33 ⁽¹⁾	PS6_3 = 1		
P124/OUTC34 ⁽¹⁾	PS6_4 = 1		
P125/OUTC35 ⁽¹⁾	PS6_5 = 1		
P126/OUTC36 ⁽¹⁾	PS6_6 = 1		
P127/OUTC37 ⁽¹⁾	PS6_7 = 1		
P130/OUTC24 ⁽¹⁾	PS7_0 = 1	-	-
P131/OUTC25 ⁽¹⁾	PS7_1 = 1		

NOTES:

1. This port is provided in the 144-pin package only.
2. When the CAS bit in the GiBCR1 register is set to "1" (32-bit time measurement function), the OUTC1j pin (j=0 to 7) outputs a waveform and the OUTC0k pin (k=0, 1, 4, 5), set as above, outputs a 16-bit low-order waveform.

Table 21.7 Pin Settings for Waveform Generation Function (2/2)

Pin	Bit and Setting		
	PS0 to PS2, PS5 to PS9 Registers	PSL0, PSL1, PSL2, PSL3 Registers	PSC Register
P132/OUTC26 ⁽¹⁾	PS7_2 = 1	-	-
P133/OUTC23 ⁽¹⁾	PS7_3 = 1		
P134/OUTC20 ⁽¹⁾	PS7_4 = 1		
P135/OUTC22 ⁽¹⁾	PS7_5 = 1		
P136/OUTC21 ⁽¹⁾	PS7_6 = 1		
P137/OUTC27 ⁽¹⁾	PS7_7 = 1		
P140/OUTC14 ^(1,2)	PS8_0 = 1	-	-
P141/OUTC15 ^(1,2)	PS8_1 = 1		
P142/OUTC16 ^(1,2)	PS8_2 = 1		
P143/OUTC17 ^(1,2)	PS8_3 = 1		
P150/OUTC00 ^(1,2)	PS9_0 = 1	-	-
P151/OUTC01 ^(1,2)	PS9_1 = 1		
P154/OUTC04 ^(1,2)	PS9_4 = 1		
P155/OUTC05 ^(1,2)	PS9_5 = 1		

NOTES:

1. This port is provided in the 144-pin package only.
2. When the CAS bit in the GiBCR1 register is set to "1" (32-bit time measurement function), the OUTC1j pin (j=0 to 7) outputs a waveform and the OUTC0k pin (k=0, 1, 4, 5), set as above, outputs a 16-bit low-order waveform.

Table 21.8 Waveform Generation Function Associated Register Settings

Register	Bit	Function
GiPOCRj	MOD2 to MOD0	Select waveform output mode
	PRT ⁽¹⁾	Set to "1" when using the parallel RTP output mode
	IVL	Select default value
	RLD	Select reload timing of GiPOj register value
	RTP ⁽¹⁾	Set to "1" when using the RTP output or the parallel RTP output mode MOD2 to MOD0 bits are invalid when the RTP bit is set to "1"
	INV	Select inversed output
G2BCR1 G3BCR1	PRP	Set to "1" when using the parallel RTP output mode
GiPOj	-	Select output waveform inverse timing
G3MK4 to G3MK7	-	Set masked values of the base timer and G3PO4 to G3PO7 registers (group 3 only)
GiFS	FSCj	Set to "0" (waveform generation function) (group 0 and 1 only)
GiFE	IFEj	Set to "1" (enables channel j function)
G2RTP G3RTP	RTP0 to RTP7	Set RTP output value in RTP output or parallel RTP output mode

i = 0 to 3; j = 0 to 7

Bit configurations and functions vary with channels and groups used.

Set registers associated with the waveform generation function after setting registers associated with the base timer.

NOTES:

1. This bit is in the G2POCRj and G3POCRj registers only.

21.3.1 Single-Phase Waveform Output Mode (Group 0 to 3)

Output signal level of the OUTCij pin (i=0 to 3; j=0 to 7) becomes high ("H") when the value of the base timer matches that of the GiPOj register. The "H" signal switches to an "L" signal when the base timer reaches "0000₁₆". If the IVL bit in the GiPOCRj register is set to "1" (outputs "H" as default value), an "H" signal is output when waveform output starts. If the INV bit is set to "1" (output inversed), the level of the waveform being output is inversed. See Figure 21.24 for details on single-phase waveform mode operation. Table 21.9 lists specifications of single-phase waveform mode.

Table 21.9 Single-phase Waveform Output Mode Specifications

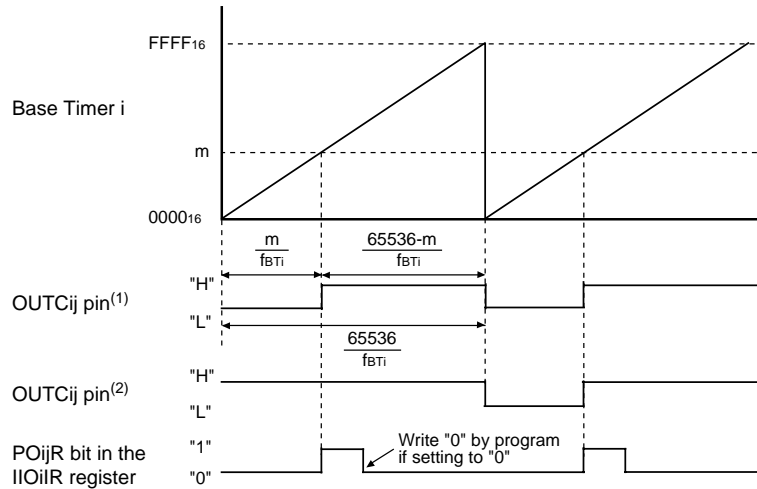
Item	Specification
Output Waveform ⁽³⁾	<ul style="list-style-type: none"> Free-running operation (the RST2 to RST0 bits in the GiBCR1 (i=0 to 3) register are set to "0002") <ul style="list-style-type: none"> Cycle : $\frac{65536}{f_{BTi}}$ "L" width : $\frac{m}{f_{BTi}}$ "H" width : $\frac{65536-m}{f_{BTi}}$ <p>m : setting value of the GiPOj register (j=0 to 7), 0000₁₆ to FFFF₁₆</p> The base timer is reset by matching the base timer with the GiPO0 register (the RST1 bit is set to "1", and the RST0 and the RST2 bit are set to "0") <ul style="list-style-type: none"> Cycle : $\frac{n+2}{f_{BTi}}$ "L" width : $\frac{m}{f_{BTi}}$ "H" width : $\frac{n+2-m}{f_{BTi}}$ <p>m : setting value of the GiPOj register (j=1 to 7), 0000₁₆ to FFFF₁₆ n : setting value of the GiPO0 register, 0001₁₆ to FFFD₁₆ If $m \geq n+2$, the output level is fixed to "L"</p>
Waveform Output Start Condition ⁽¹⁾	The IFEj bit in the GiFE register is set to "1" (channel j function enabled)
Waveform Output Stop Condition	The IFEj bit is set to "0" (channel j function disabled)
Interrupt Request	The POijR bit in the interrupt request register is set to "1" (interrupt requested) when the value of the base timer matches that of the GiPOj register. (See Figure 10.14)
OUTCij Pin ⁽²⁾	Pulse signal output pin
Selectable Function	<ul style="list-style-type: none"> Default value set function : Set starting waveform output level Inversed output function : Waveform output level is inversed and output from the OUTCij pin Cascaded connection function: Connect group 0 and group 1 to operate as a 32-bit base timer

NOTES:

- Set the FSCj bit in the GiFS register to "0" (waveform generation function selected) when using channels shared by both time measurement function and waveform generation function
- OUTC00, OUTC01, OUTC04, OUTC05, OUTC10 to OUTC17, OUTC20 to OUTC27, and OUTC30 to OUTC37 pins (OUTC10 to OUTC17 pins when using group 0 and group 1 cascaded connection)
- When the INV bit in the GiPOCRj register is set to "1" (output inversed), the "L" width and "H" width are inversed

(1) Free-Running Operation

(The RST2 to RST0 bits in the GiBCR1 register are set to "0002")

 $i=0$ to 3; $j=0$ to 7 (however, $i=0$ when $j=0, 1, 4, 5$) m : Setting value of the GiPOj register (0000₁₆ to FFFF₁₆)

POijR bit: Bits in the IIO0iR to IIO11iR register

NOTES:

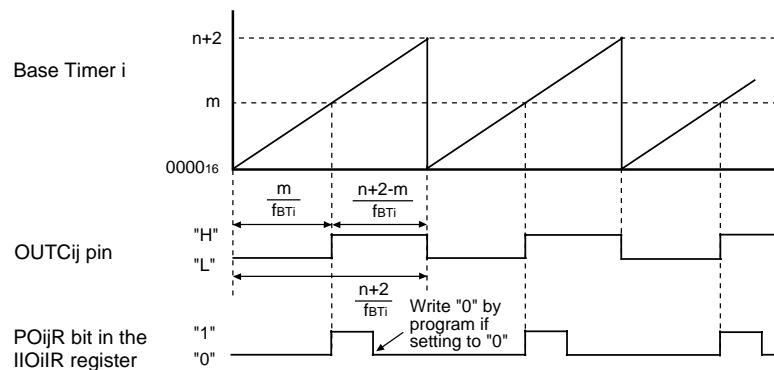
1. Waveform output when the INV bit in the GiPOCRj register is set to "0" (not inverted) and the IVL bit is set to "0" (output "L" as default value).
2. Waveform output when the INV bit is set to "0" (not inverted) and the IVL bit is set to "1" (output "H" as default value).

The above applies under the following conditions:

- The RST2 to RST0 bits in the GiBCR1 register are set to "0002" (no base timer reset), the UD1 to UD0 bits to "002" (counter increment mode), and CAS bit to "0" (16-bit waveform generation function)

(2) The Base Timer is Reset when the Base Timer Matches the GiPO0 Register

(The RST1 bit is set to "1", and the RST0 and RST2 bits are set to "0")

 $i=0$ to 3; $j=1$ to 7 (however, $i=0$ when $j=1, 4, 5$) m : Setting value of the GiPOj register (0000₁₆ to FFFF₁₆) n : Setting value of the GiPO0 register (0001₁₆ to FFFD₁₆)

POijR bit: Bits in the IIO0iR to IIO11iR register

The above diagram applies under the following conditions:

- The IVL bit in the GiPOCRj register is set to "0" (outputs "L" as default value). The INV bit is set to "0" (not inverse).
- The UD1 to UD0 bits in the GiBCR1 register are set to "002" (counter increment mode), and the CAS bit to "0" (16-bit waveform generation function)
- $m < n+2$

Figure 21.24 Single-Phase Waveform Output Mode

21.3.2 Phase-Delayed Waveform Output Mode (Group 0 to 3)

Output signal level of the OUTCij pin (i=0 to 3; j=0 to 7) is inversed every time the value of the base timer matches that of the GiPOj register. Table 21.10 lists specifications of phase-delayed waveform mode. Figure 21.25 shows an example of phase-delayed waveform mode operation.

Table 21.10 Phase-delayed Waveform Output Mode Specifications

Item	Specification
Output Waveform	<ul style="list-style-type: none"> Free-running operation (the RST2 to RST0 bits in the GiBCR1 register (i=0 to 3) are set to "0002") <p>Cycle : $\frac{65536 \times 2}{f_{BTi}}$</p> <p>"H" and "L" width : $\frac{65536}{f_{BTi}}$</p> <p>Setting value of the GiPOj (j=0 to 7) register is 0000₁₆ to FFFF₁₆</p> <ul style="list-style-type: none"> The base timer is reset by matching the base timer with the GiPO0 register (the RST1 bit is set to "1", and the RST0 and RST2 bit are set to "0") <p>Cycle : $\frac{2(n+2)}{f_{BTi}}$</p> <p>"H" and "L" width : $\frac{n+2}{f_{BTi}}$</p> <p>n : setting value of the GiPO0 register, 0001₁₆ to FFFD₁₆ Setting value of the GiPOj (j=1 to 7) register is 0000₁₆ to FFFF₁₆ If GiPOj register $\geq n+2$, the output level is not inversed </p>
Waveform Output Start Condition ⁽¹⁾	The IFEj bit (j=0 to 7) in the GiFE register is set to "1" (channel j function enabled)
Waveform Output Stop Condition	The IFEj bit is set to "0" (channel j function disabled)
Interrupt Request	The POijR bit in the interrupt request register is set to "1" (interrupt requested) when the value of the base timer matches that of the GiPOj register. (See Figure 10.14)
OUTC1j Pin	Pulse signal output pin
Selectable Function	<ul style="list-style-type: none"> Default value set function : Set starting waveform output level Inversed output function : Waveform output level is inversed and output from the OUTCij pin Cascaded connection function: Connect group 0 and group 1 to operate as a 32-bit base timer

NOTES:

- Set the FSCj bit in the GiFS register to "0" (waveform generation function selected) when using channels shared by both time measurement function and waveform generation function
- OUTC0₀, OUTC0₁, OUTC0₄, OUTC0₅, OUTC1₀ to OUTC1₇, OUTC2₀ to OUTC2₇, and OUTC3₀ to OUTC3₇ pins (OUTC1₀ to OUTC1₇ pins when using group 0 and group 1 cascaded connection)

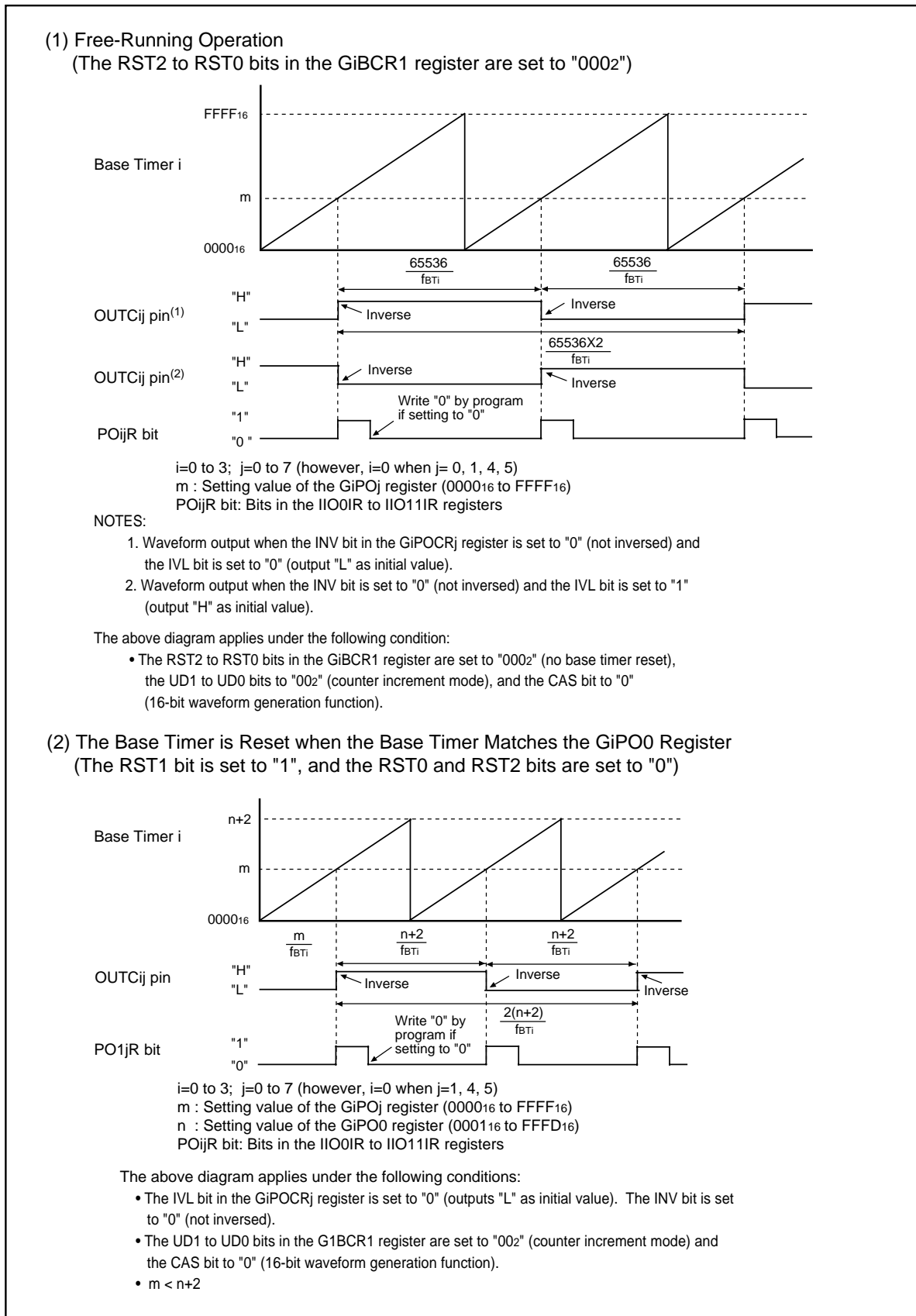


Figure 21.25 Phase-delayed Waveform Output Mode

21.3.3 Set/Reset Waveform Output (SR Waveform Output) Mode (Group 0 to 3)

Output signal level of the OUTCij pin (i=0 to 3; j=0, 2, 4, 6) becomes "H" when the value of the base timer matches that of the GiPOj register. The "H" signal switches to an "L" signal when the value of the base timer matches that of the GiPOk register (k=j+1) or when the base timer is set to "000016". If the IVL bit in the GiPOCRj register (j=0 to 7) is set to "1" (outputs "H" as initial value), an "H" signal is output when waveform output starts. If the INV bit is set to "1" (output is inversed), the level of the waveform being output is inversed. Table 21.11 lists specifications of SR waveform mode. Figure 21.26 shows an example of a SR waveform mode operation.

Table 21.11 SR Waveform Output Mode Specifications (1/2)

Item	Specification
Output Waveform ⁽²⁾	<ul style="list-style-type: none"> • Free-running operation (the RST2 to RST0 bits in the GiBCR1 register are set to "0002") (1) $m < n$ " H " width : $\frac{n - m}{f_{BTi}}$ " L " width : $\frac{m}{f_{BTi}}$ + $\frac{65536 - n^{(4)}}{f_{BTi}}$ (2) $m \geq n$ " H " width : $\frac{65536 - m}{f_{BTi}}$ " L " width : $\frac{m}{f_{BTi}}$ m : setting value of the GiPOj register (j=0, 2, 4, 6) n : setting value of the GiPOk register (k=j+1) m, n=000016 to FFFF16 • The base timer is reset by matching the base timer with the GiPO0 register⁽¹⁾ (the RST1 bit is set to "1", and the RST0 and RST2 bits are set to "0") (1) $m < n < p+2$ " H " width : $\frac{n-m}{f_{BTi}}$ " L " width : $\frac{m}{f_{BTi}}$ + $\frac{p + 2 - n^{(4)}}{f_{BTi}}$ (2) $m < p+2 \leq n$ " H " width : $\frac{p + 2 - n}{f_{BTi}}$ " L " width : $\frac{m}{f_{BTi}}$ (3) If $m \geq p+2$, the output level is fixed to "L" m : setting value of the GiPOj register (j=2, 4, 6) n : setting value of the GiPOk register (k=j+1) p : setting value of the GiPO0 register m, n=000016 to FFFF16 p=000116 to FFFD16

NOTES:

1. When the GiPO0 register resets the base timer, the channel 0 and 1 SR waveform generation functions are not available.
2. When the INV bit in the GiPOCRj register is set to "1" (output inversed), the "L" width and "H" width are inversed.
3. Waveform from base timer reset until when output level becomes "H".
4. Waveform from when output level becomes "L" until base timer reset.

Table 21.11 SR Waveform Output Mode Specifications (2/2)

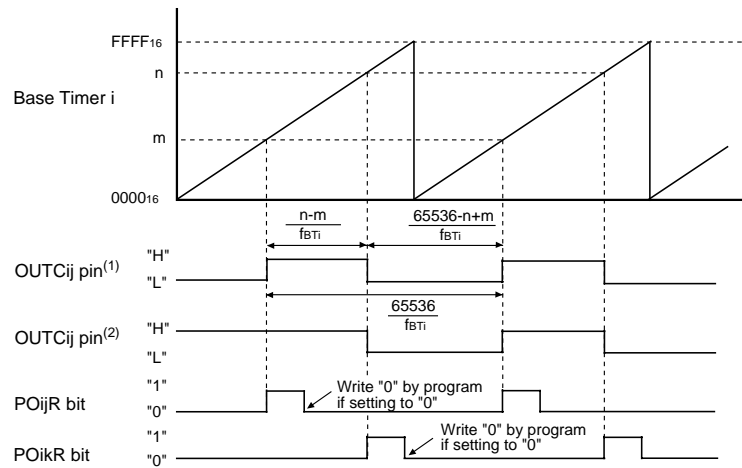
Item	Specification
Waveform Output Start Condition ⁽⁵⁾	The IFEq bit (q=0 to 7) in the GiFE register is set to "1" (channel q function enabled)
Waveform Output Stop Condition	The IFEq bit is set to "0" (channel q function disabled)
Interrupt Request	The POijR bit in the interrupt request register is set to "1" (interrupt requested) when the value of the base timer matches that of the GiPOj register. The POikR bit in the interrupt request register is set to "1" (interrupt requested) when the value of the base timer matches that of the GiPOk register. (See Figure 10.14)
OUTCij Pin ⁽⁶⁾	Pulse signal output pin
Selectable Function	<ul style="list-style-type: none"> • Default value set function : Set starting waveform output level • Inversed output function : Waveform output level is inversed and output from the OUTCij pin • Cascaded connection function: Connect group 0 and group 1 to operate as a 32-bit base timer

NOTES:

5. Set the FSCj bit in the GiFS register to "0" (waveform generation function selected) when using channels shared by both time measurement function and waveform generation function
6. OUTC00, OUTC04, OUTC10, OUTC12, OUTC14, OUTC16, OUTC20, OUTC22, OUTC24, OUTC26, OUTC30, OUTC32, OUTC34, and OUTC36 pins
(OUTC10, OUTC12, OUTC14, and OUTC16 pins when using group 0 and group 1 cascaded connection)

(1) Free-Running Operation

(The RST2 to RST0 bits in the GiBCR1 register are set to "0002")



$i=0, 3; j=0, 2, 4, 6$ (however, $i=0$ when $j=0, 4$); $k=j+1$
 m : Setting value of the GiPOj register (0000₁₆ to FFFF₁₆)
 n : Setting value of the GiPOk register (0000₁₆ to FFFF₁₆)
 POijR, POikR bits: Bits in the IIOiR to IIO11iR registers

NOTES:

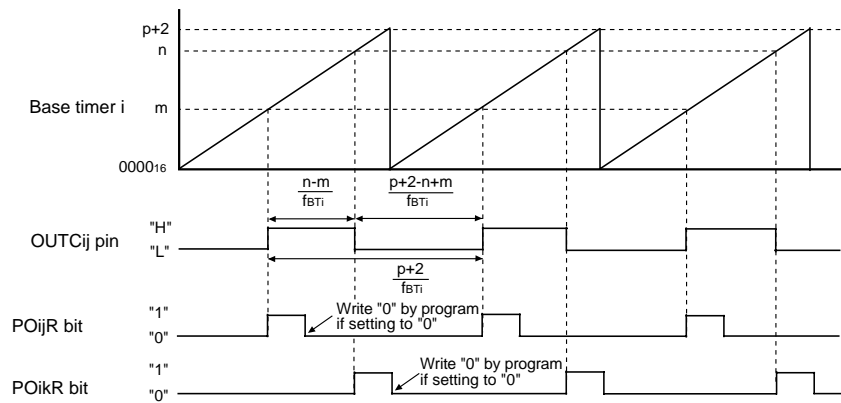
1. Waveform output when the INV bit in the GiPOCRj register is set to "0" (not inverted) and the IVL bit is set to "0" (output "L" as default value).
2. Waveform output when the INV bit is set to "0" (not inverted) and the IVL bit is set to "1" (output "H" as default value).

The diagram above applies under the following condition:

- The RST2 to RST0 bits in the GiBCR1 register are set to "0002" (no base timer reset), the UD1 to UD0 bits to "002" (counter increment mode), and the CAS bit to "0" (16-bit waveform generation function).
- $m < n$

(2) The Base Timer is Reset when the Base Timer Matches the GiPO0 Register

(The RST1 bit is set to "1", and the RST0 and RST2 bits are set to "0")



$i=0$ to 3; $j=2, 4, 6$ (however, $i=0$ when $j=4$); $k=j+1$
 m : Setting value of the GiPOj register (0000₁₆ to FFFF₁₆)
 n : Setting value of the GiPOk register (0000₁₆ to FFFF₁₆)
 p : Setting value of the GiPO0 register (0001₁₆ to FFFD₁₆)
 POijR, POikR bits: Bits in the IIOiR to IIO11iR registers

The diagram above applies under the following conditions:

- The IVL bit in the GiPOCRk register is set to "0" (outputs "0" as default value). The INV bit is set to "0" (not inverted).
- The UD1 to UD0 bits in the GiBCR1 register are set to "002" (counter increment mode) and the CAS bit to "0" (16-bit waveform generation function).
- $m < n < p+2$

Figure 21.26 SR Waveform Output Mode

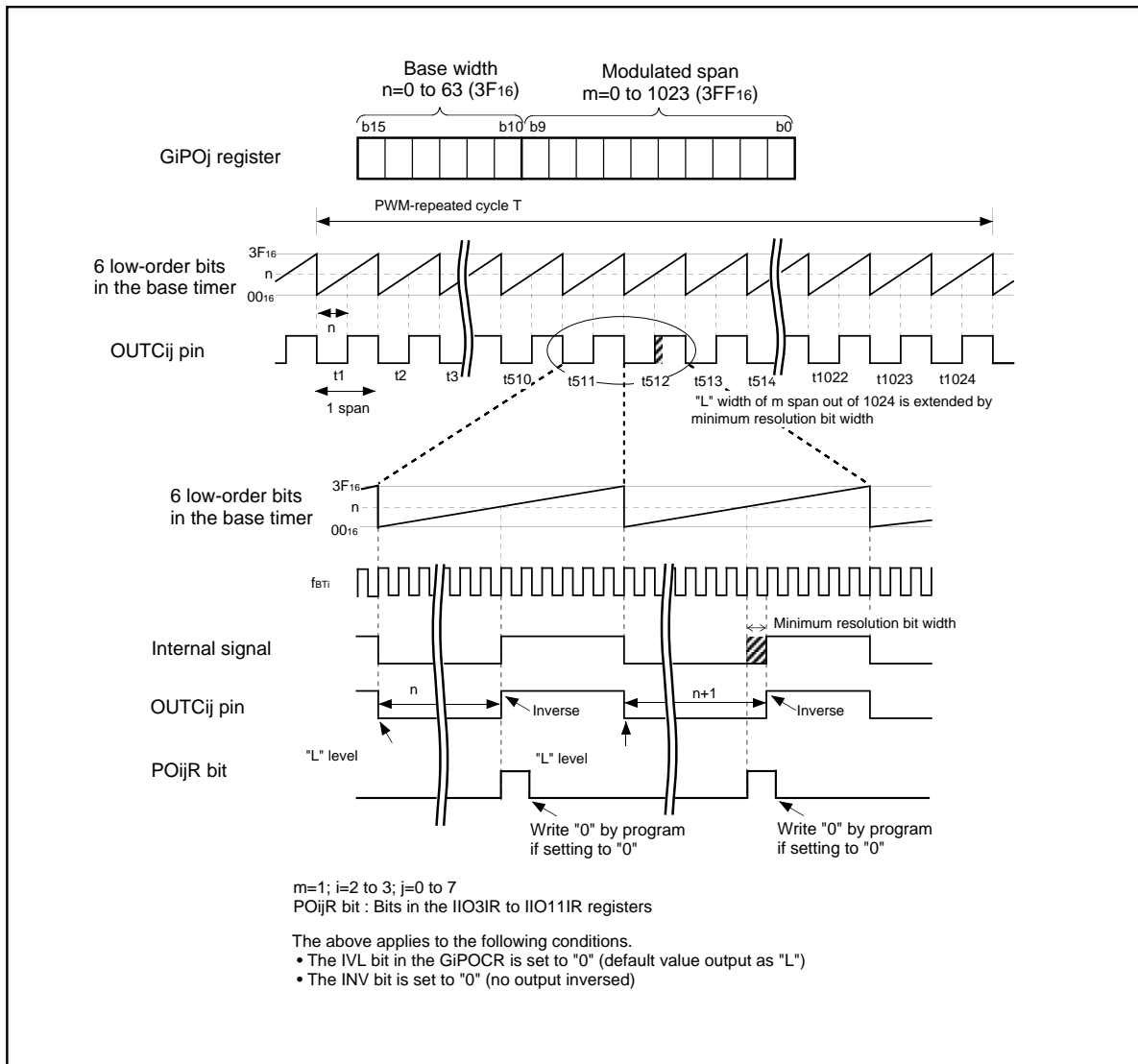


Figure 21.27 Bit Modulation PWM Mode

21.3.5 Real-Time Port (RTP) Output Mode (Group 2 and 3)

The OUTCij pin outputs the value set in the GiRTP register in one-byte units by matching the value of the base timer with that of the GiPOj register (i=2 to 3, j=0 to 7). Table 21.14 lists specifications of RTP output mode. Figure 21.28 shows a block diagram of the RTP output function. Figure 21.29 shows an example of RTP output mode operation.

Table 21.14 RTP Output Mode Specifications

Item	Specification
Waveform Output Start Condition	The IFEj bit in the GiFE register (i=2 to 3, j=0 to 7) is set to "1" (channel j function enabled)
Waveform Output Stop Condition	The IFEj bit is set to "0" (channel j function disabled)
Interrupt Request	The POijR bit in the interrupt request register is set to "1" when the value of the base timer matches that of the GiPOj register (0000 ₁₆ to FFFF ₁₆ ⁽¹⁾). (See Figure 10.14.)
OUTCij Pin	RTP output pin
Selectable Function	<ul style="list-style-type: none"> • Default value set function : Set starting waveform output level • Inversed output function : Waveform output level is inversed and output from the OUTCij pin

NOTES:

1. Set the GiPO0 register to 0001₁₆ to FFFD₁₆ when setting the base timer to "0000₁₆" (the RST1 bit in the GiBCR1 register is set to "1", and the RST0 and RST2 bits are set to "0") while the values in the base timer and the GiPO0 register match

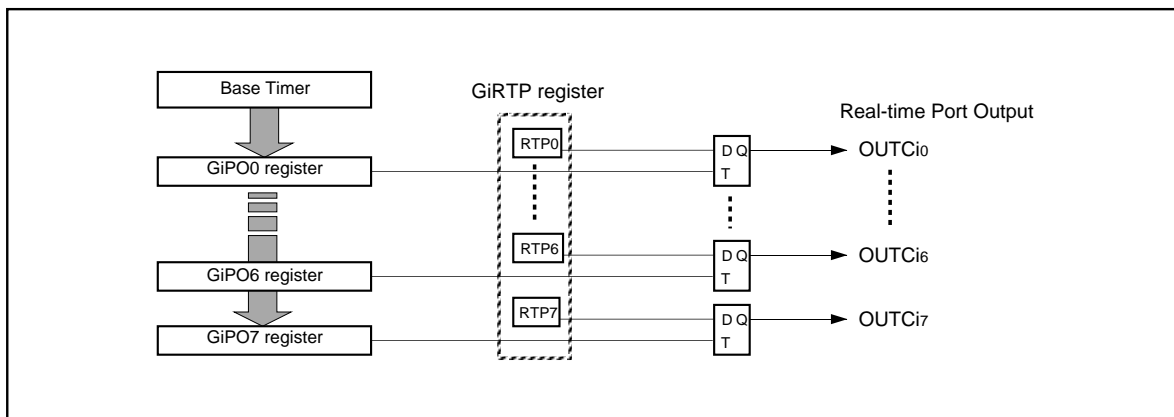
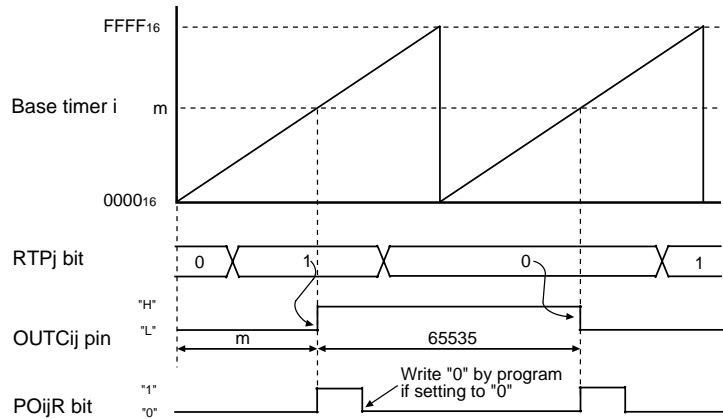


Figure 21.28 Real-time Port Output Function Block Diagram

(1) Free-running operation
(RST2 to RST0 bits in the GiBCR1 register are set to "0002")



$i=2$ to 3 , $j=0$ to 7

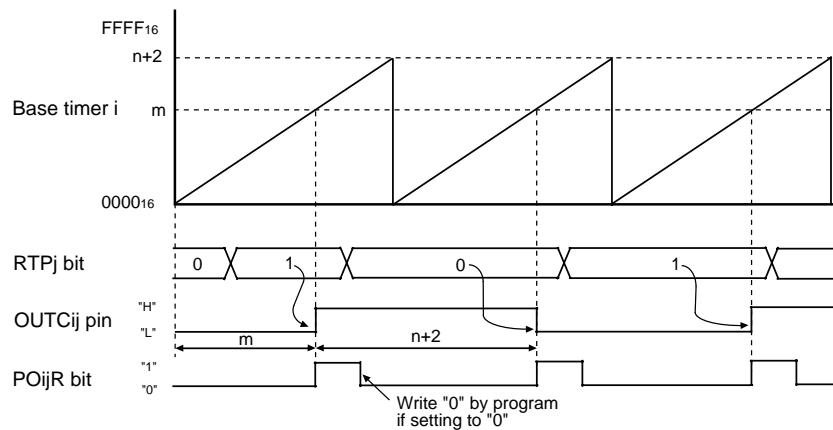
m : Setting value of the GiPOj register (0000₁₆ to FFFF₁₆)

POijR bit : Bits in the IIO3IR to IIO11IR registers

The above applies to the following conditions.

- The IVL bit in the GIPOCRj register is set to "0" (output "L" as an initial value). The INV bit is set to "0" (no output inverted).
- RST2 to RST0 bits in the GiBCR1 register are set to "0002" (no base timer reset).

(2) The base timer is reset when the base timer matches the GiPO0 register
(The RST1 bit is set to "1" and both RST0 and RST2 bits are set to "0")



$i=2$ to 3 , $j=1$ to 7

m : Setting value of the GiPOj register (0000₁₆ to FFFF₁₆)

n : Setting value of the GiPO0 register (0001₁₆ to FFFD₁₆)

POijR bit : Bits in the IIO0IR to IIO11IR registers

The above applies to the following condition.

- The IVL bit in the GIPOCRj register is set to "0" (output "L" as an initial value). The INV bit is set to "0" (no output inverted).
- $m < n+2$

Figure 21.29 Real-time Port Output Mode

21.3.6 Parallel Real-Time Port Output Mode (Group 2 and 3)

The OUTCij pin outputs the value set by the GiRTP register in one-byte units when the value of the base timer matches that of the GiPOj register ($i=2$ to 3 , $j=0$ to 7). Table 21.15 lists specifications of the parallel RTP output mode. Figure 21.30 shows a block diagram of the parallel RTP output function. Figure 21.31 shows an example of the parallel RTP output mode operation. (See Figure 21.7 for the G2BCR1 register and Figure 21.8 for the G3BCR1 register.)

Table 21.15 Parallel RTP Output Mode Specifications

Item	Specification
Waveform Output Start Condition	The IFEj bit in the GiFE register ($i=2$ to 3 , $j=0$ to 7) is set to "1" (channel j function enabled)
Waveform Output Stop Condition	The IFEj bit is set to "0" (channel j function disabled)
Interrupt Request	The POijR bit in the interrupt request register is set to "1" when value of the base timer matches that of the GiPOj register (0000_{16} to $FFFF_{16}^{(1)}$). (See Figure 10.14.)
OUTCij Pin	RTP output
Selectable Function	<ul style="list-style-type: none"> • Default value set function: Set starting waveform output level • Inverse output function: Waveform output level is inverted and output from the OUTCij pin

NOTES:

1. Set the GiPO0 register to 0001_{16} to $FFFD_{16}$ when setting the base timer to "0000₁₆" (the RST1 bit in the GiBCR1 register is set to "1", and the RST0 and RST2 bits are set to "0") while the values in the base timer and the GiPO0 register match

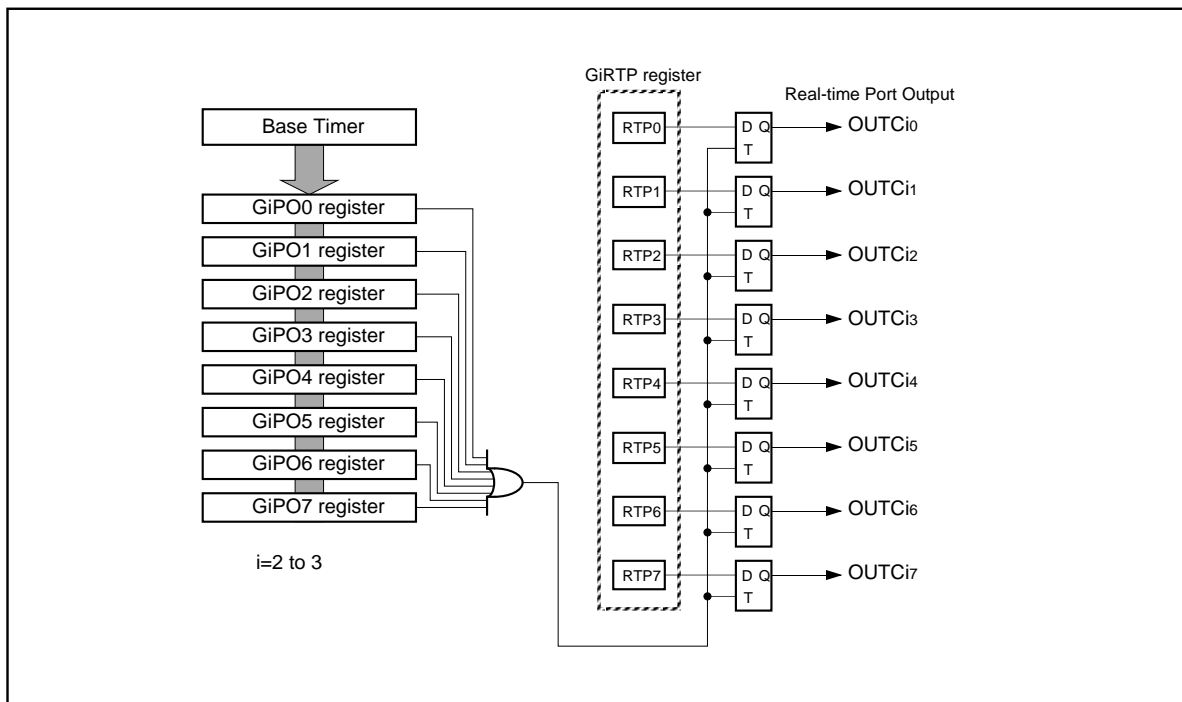


Figure 21.30 Parallel RTP Output Function Block Diagram

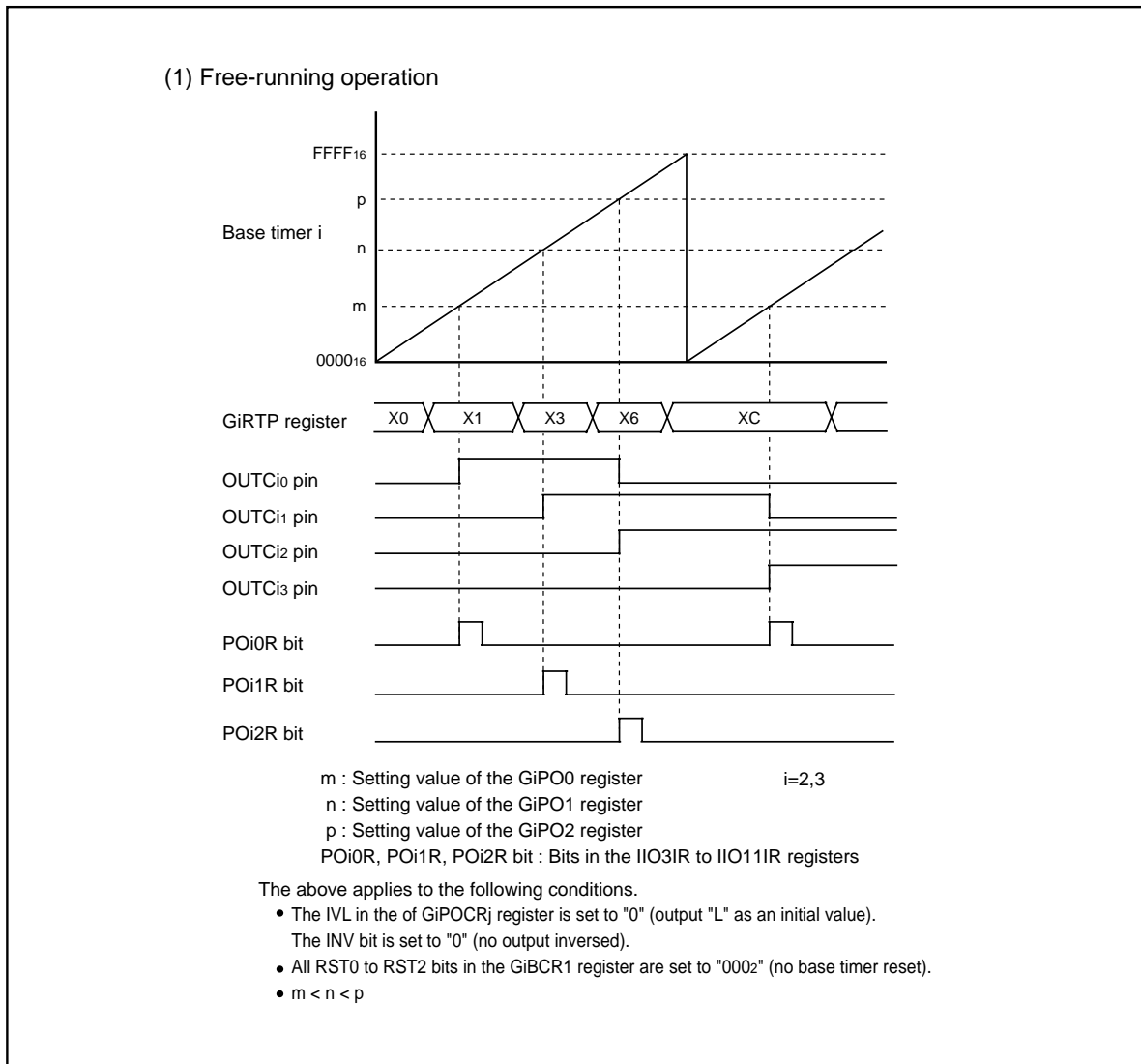


Figure 21.31 Parallel RTP Output Mode

21.4 Communication Unit 0 and 1 Communication Function

The communication function is available when two 8-bit shift registers are used with either timer measurement function or waveform generation function.

In the intelligent I/O groups 0 and 1, 8-bit clock synchronous serial I/O, 8-bit clock asynchronous serial I/O (UART) and HDLC data processing are available.

Figures 21.32 to 21.38 show registers associated with the communication function.

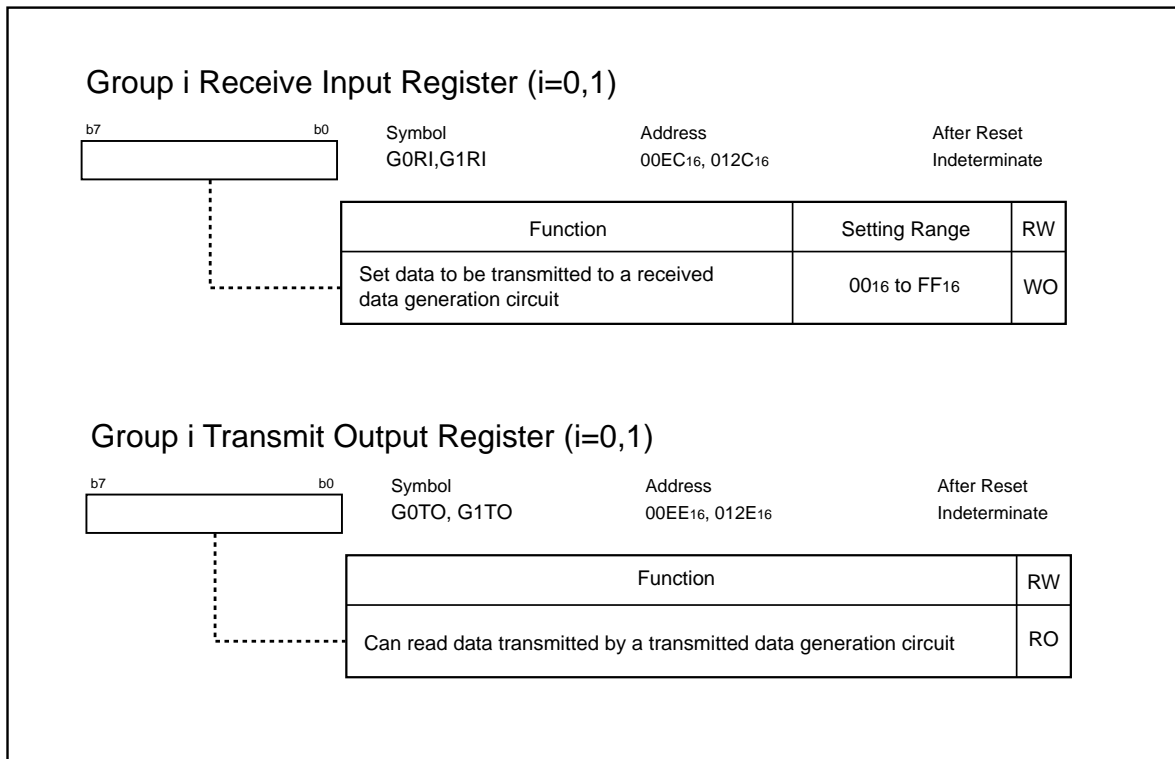


Figure 21.32 G0RI to G1RI Registers and G0TO to G1TO Registers

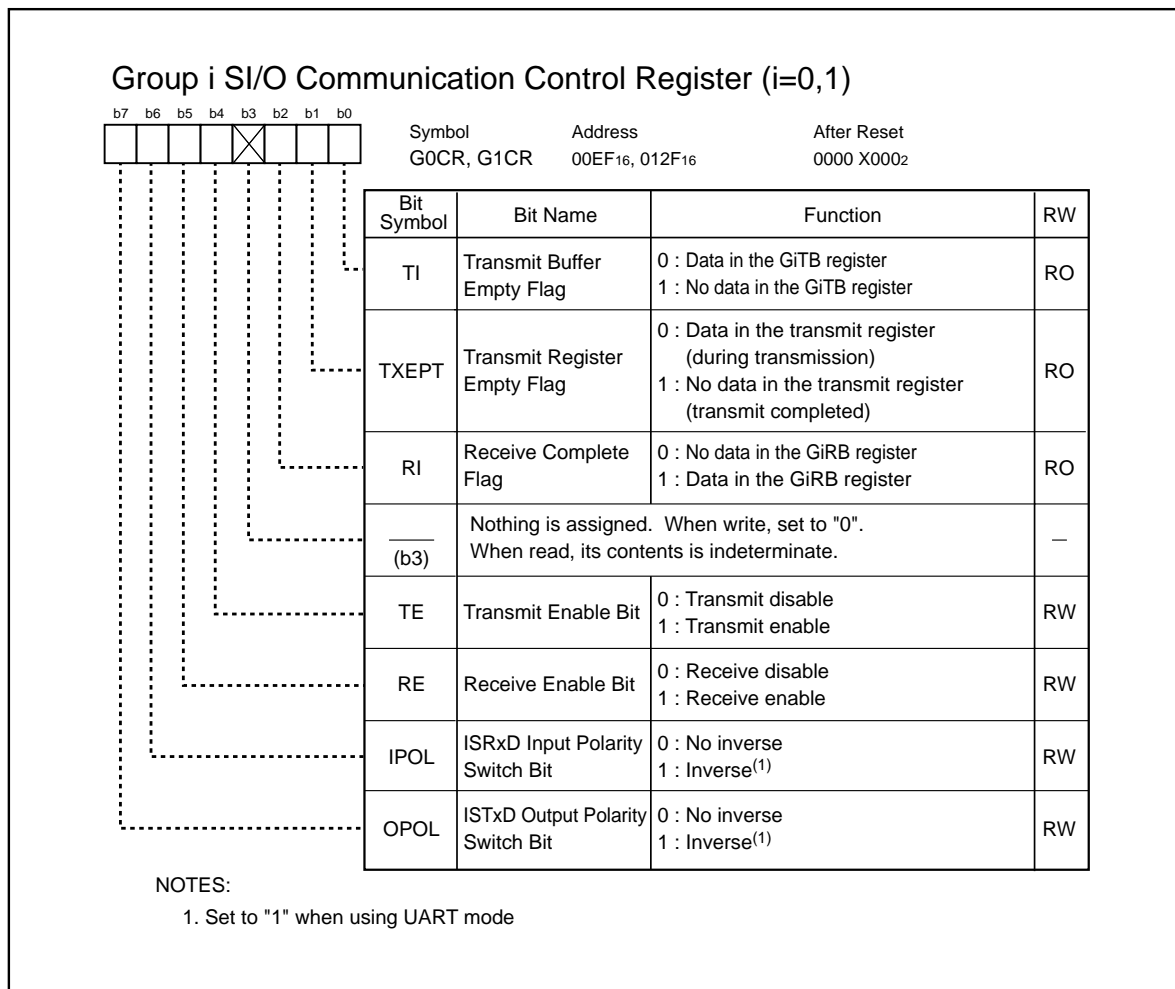


Figure 21.33 G0CR to G1CR Registers

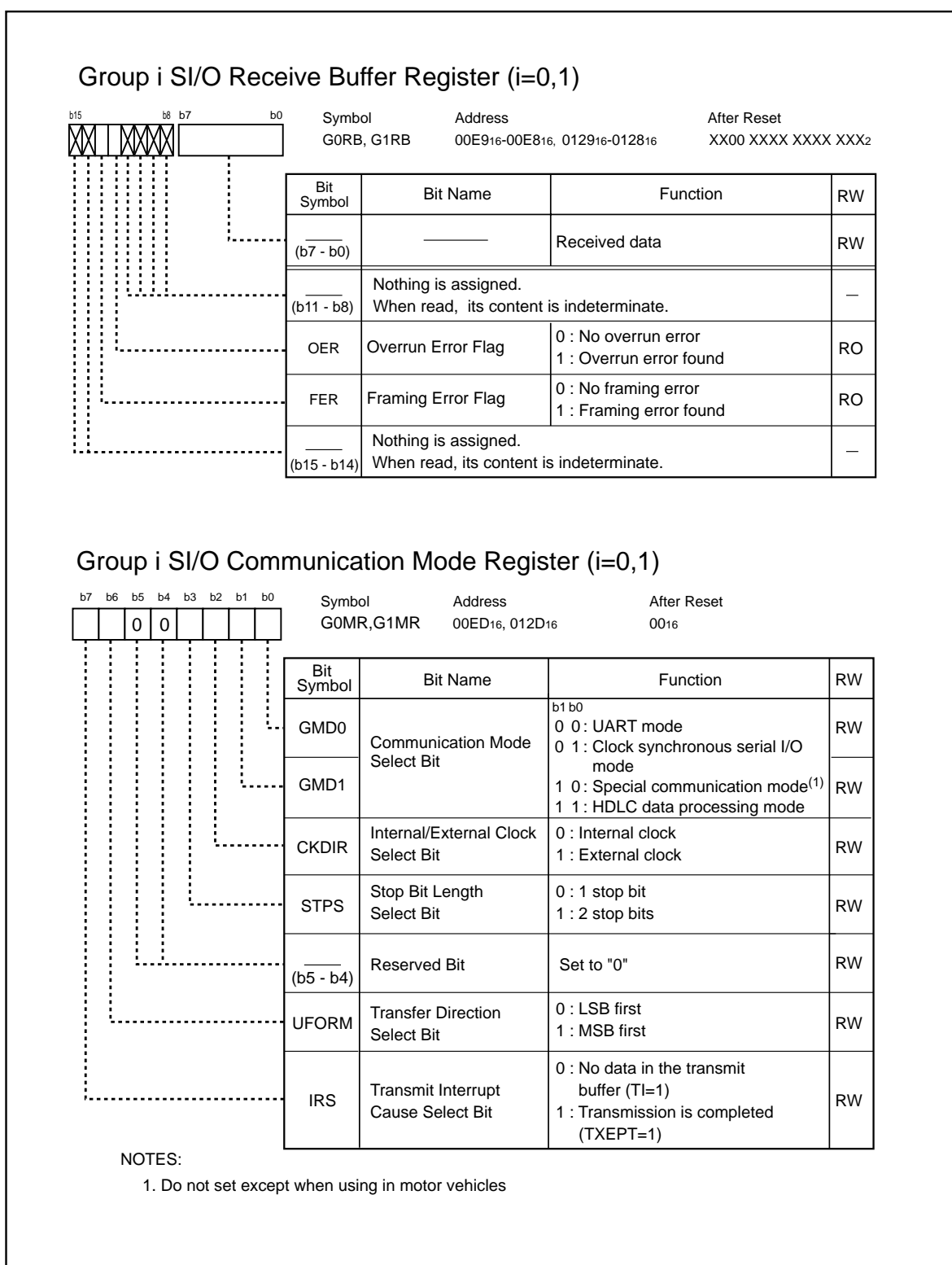


Figure 21.34 G0RB to G1RB Registers and G0MR to G1MR Registers

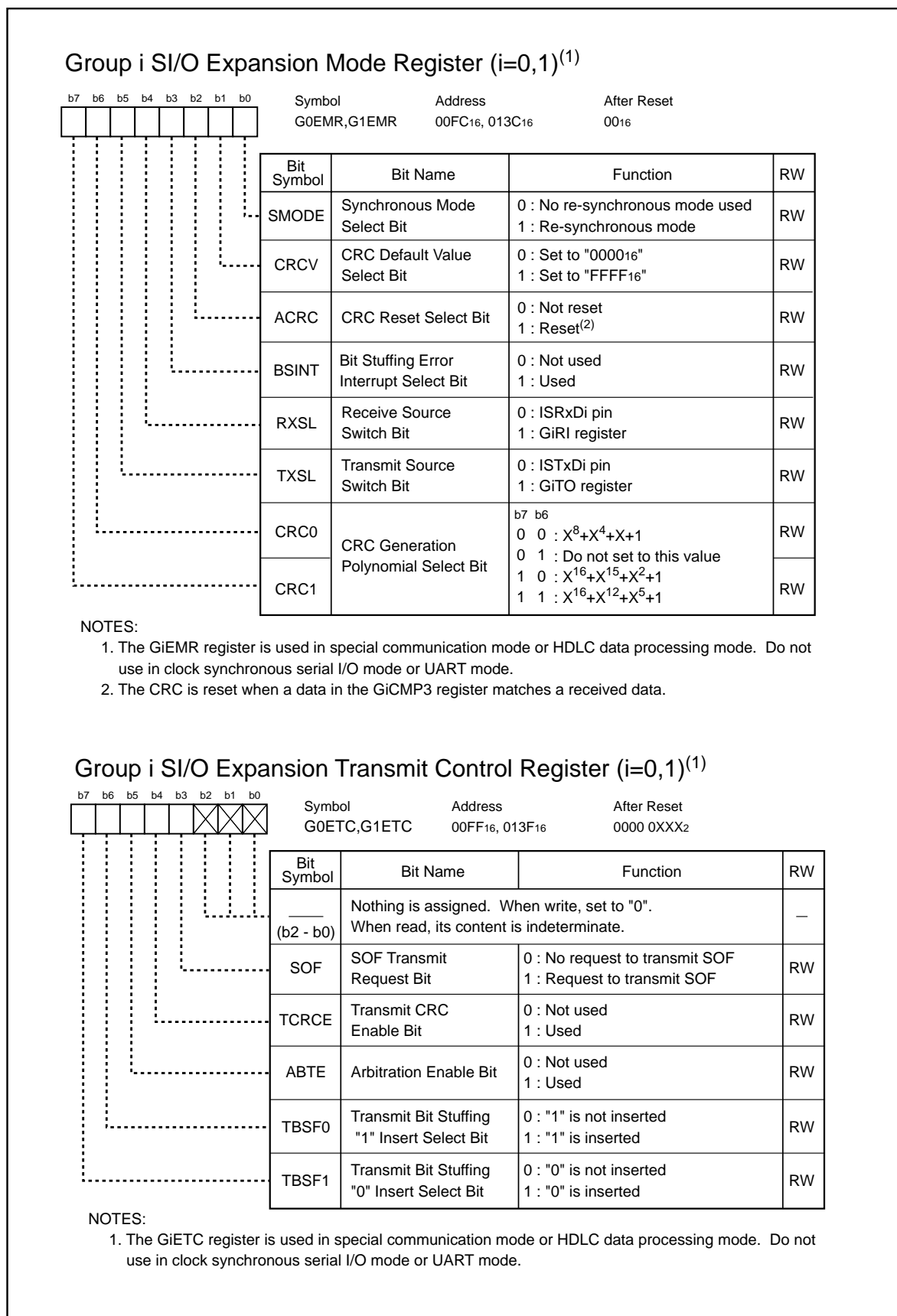


Figure 21.35 G0EMR to G1EMR Registers and G0ETC to G1ETC Registers

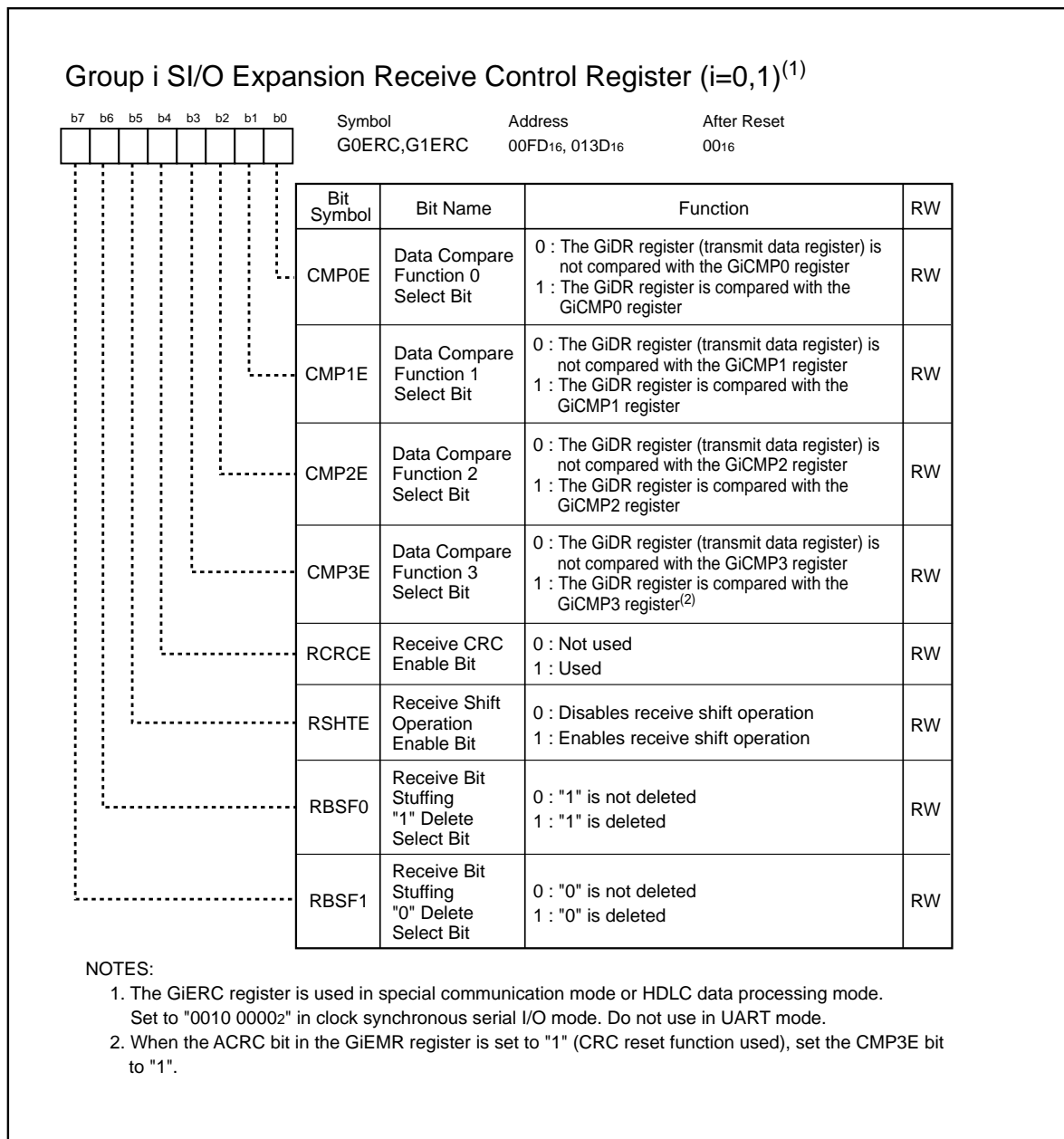


Figure 21.36 G0ERC to G1ERC Registers

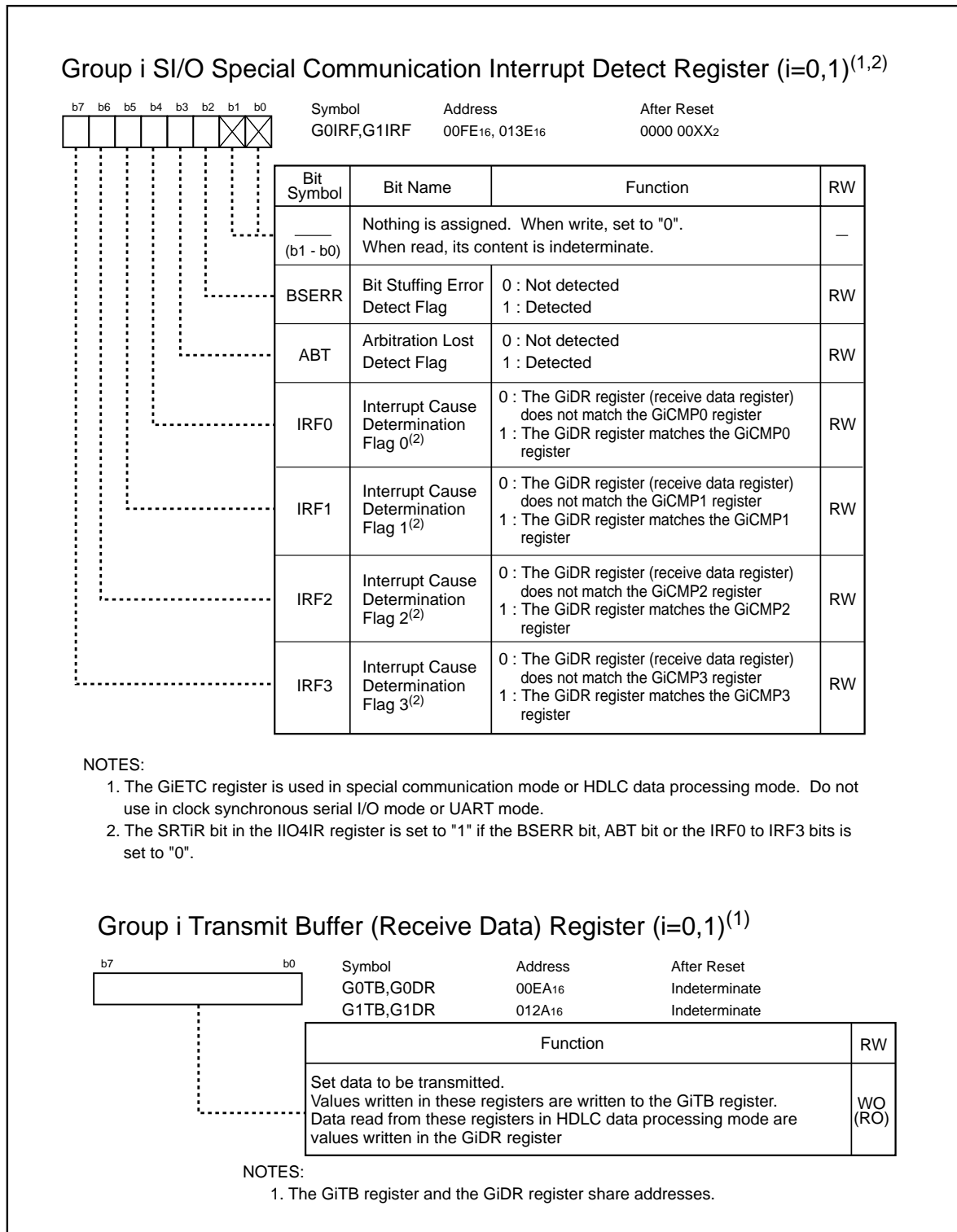


Figure 21.37 G0IRF to G1IRF Registers and G0TB to G1TB Registers

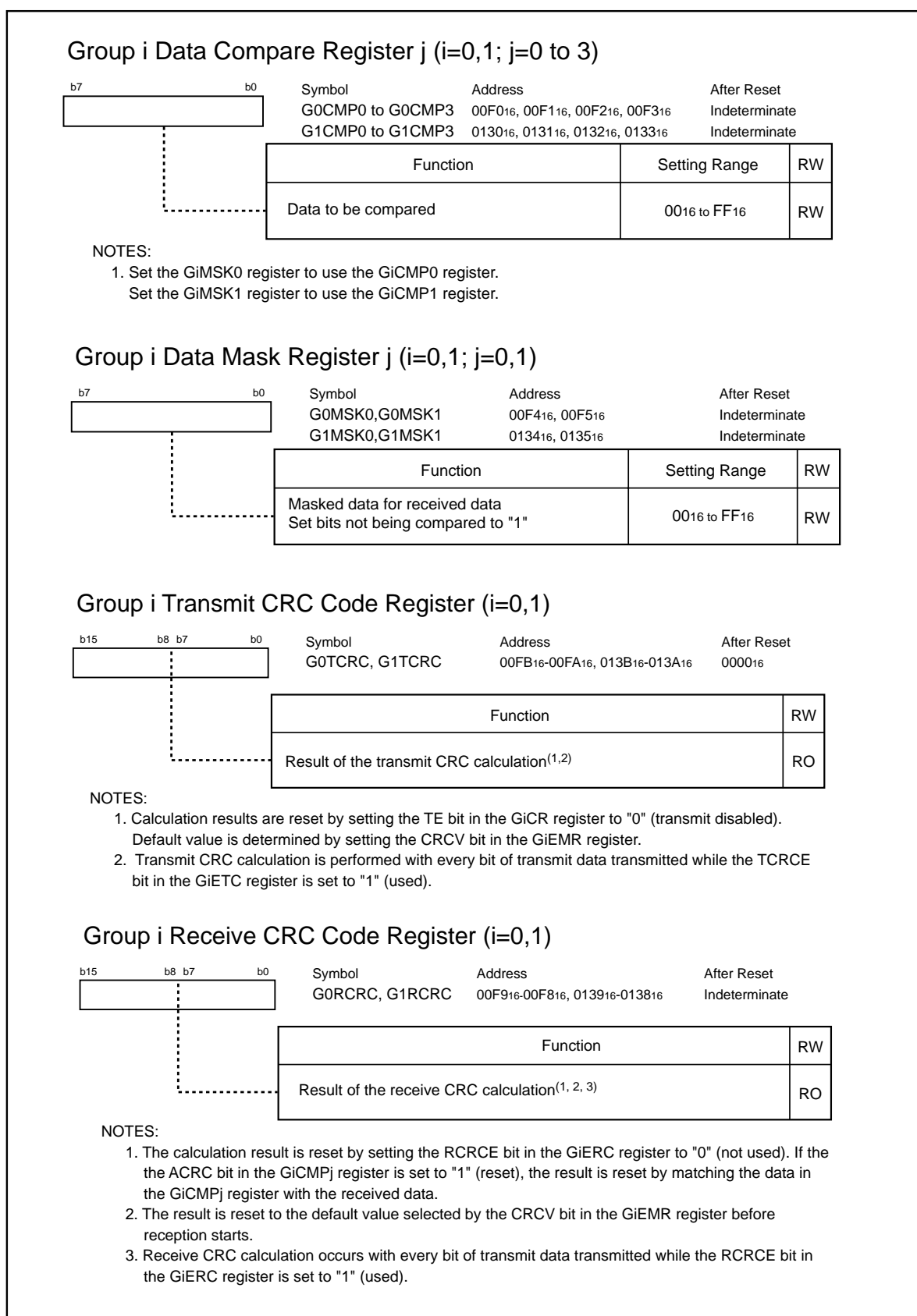


Figure 21.38 G0CMP0 to G0CMP3 Registers, G1CMP0 to G1CMP3 Registers, G0MSK0 to G0MSK1 Registers, G1MSK0 to G1MSK1 Registers, G0TCRC to G1TCRC Registers, and G0RCRC to G1RCRC Registers

21.4.1 Clock Synchronous Serial I/O Mode (Groups 0 and 1)

In clock synchronous serial I/O mode, data is transmitted and received with the transfer clock. When the internal clock is selected as the transfer clock, the channel 0 and channel 3 waveform generation functions generate the internal clock. ISTxDi (i=0, 1), ISCLKi, and ISRxDi share pins with INPCi0 to INPCi2 and OUTCi0 to OUTCi2.

Table 21.16 lists specifications of clock synchronous serial I/O mode. Table 21.17 lists registers to be used and their settings. Tables 21.18 to 21.21 list pin settings. Figure 21.39 shows an example of a transmit and receive operation.

Table 21.16 Clock Synchronous Serial I/O Mode Specifications (Groups 0 and 1)

Item	Specification
Transfer Data Format	Transfer data : 8 bits long
Transfer Clock ^(1, 2)	When the CKDIR bit in the GiMR register (i=0, 1) is set to "0" (internal clock) : $\frac{f_{BTi}}{2(n+2)}$ n : setting value of the GiPO0 register, 0000 ₁₆ to FFFF ₁₆ <ul style="list-style-type: none"> The GiPO0 register determines the bit rate and the transfer clock is generated in phase-delayed waveform output mode by the channel 3 waveform generation function. When the CKDIR bit is set to "1" (external clock) : input from the ISCLKi pin
Transmit Start Condition	Set registers associated with the waveform generation function, the GiMR register and the GiERC register. Then set as written below after at least one transfer clock cycle: <ul style="list-style-type: none"> Set the TE bit in the GiCR register to "1" (transmit enable) Set the TI bit in the GiCR register to "0" (data in the GiTB register)
Receive Start Condition	Set registers associated with the waveform generation function, the GiMR register and GiERC register. Then set as written below after at least one transfer clock cycle: <ul style="list-style-type: none"> Set the RE bit in the GiCR register to "1" (receive enable) Set the TE bit to "1" (transmit enable) Set the TI bit to "0" (data in the GiTB register)
Interrupt Request	<ul style="list-style-type: none"> While transmitting, one of the following conditions can be selected to set the SIOiTR bit to "1" (see Figure 10.14): <ul style="list-style-type: none"> The IRS bit in the GiMR register is set to "0" (no data in the GiTB register) and data is transferred to the transmit register from the GiTB register The IRS bit is set to "1" (transmission completed) and data transfer from the transmit register is completed While receiving, the following condition can be selected to set the SIOiRR bit to "1" (see Figure 10.14): Data is transferred from the receive register to the GiRB register
Error Detection	Overrun error ⁽³⁾ This error occurs when the 8th bit of the next data is received before reading the GiRB register
Selectable Function	<ul style="list-style-type: none"> LSB first/MSB first Select either bit 0 or bit 7 to transmit/receive data ISTxDi and ISRxDi I/O polarity inverse ISTxDi pin output level and ISRxDi pin input level are inverted

NOTES:

- The transfer clock must be f_{BTi} divided by six or more.
- In clock synchronous serial I/O mode, set the RSHTe bit in the GiERC register (i=0, 1) to "1" (receive shift operation enabled).
- When an overrun error occurs, the GiRB register is indeterminate.

When the OPOL bit in the GiCR register is set to "0" (no ISTxDi output polarity inverted), the ISTxDi pin outputs an "H" signal after selecting operation mode until transfer starts. When the OPOL bit is set to "1", the ISTxDi pin outputs an "L" signal.

Table 21.17 Registers to be Used and Settings

Register	Bit	Function
GiBCR0	BCK1 to BCK0	Set to "112"
	DIV4 to DIV0	Select divide ratio of count source
	IT	Set to "0"
GiBCR1	7 to 0	Set to "0001 00102"
GiPOCR0	7 to 0	Set to "0000 01112"
GiPOCR1	7 to 0	Set to "0000 01112"
GiPOCR3	7 to 0	Set to "0000 00102" ⁽¹⁾
GiPO0	15 to 0	Set the bit rate $\frac{f_{BTi}}{2x(\text{setting value} + 2)} = \text{transfer clock frequency}^{(1)}$
GiPO3	15 to 0	Set to a value smaller than the GiPO0 register ⁽¹⁾
GiFS	FSC3,1,0	Set to "0"
GiFE	IFE3,1,0	Set to "1"
GiERC	7 to 0	Set to "0010 00002"
GiMR	GMD1 to GMD0	Set to "012"
	CKDIR	Select the internal clock or external clock
	STPS	Set to "0"
	UFORM	Select either LSB first or MSB first
	IRS	Select how the transmit interrupt is generated
GiCR	TI	Transmit buffer empty flag
	TXEPT	Transmit register empty flag
	RI	Receive complete flag
	TE	Set to "1" to enable transmission and reception
	RE	Set to "1" to enable reception
	IPOL	Select ISRxD input polarity (usually set to "0")
	OPOL	Select ISTxD output polarity (usually set to "0")
GiTB	7 to 0	Write data to be transmitted
GiRB	15 to 0	Received data and error flag are stored

i = 0 to 1

NOTES:

1. The CKDIR bit in the GiMR register is set to "0" (internal clock)

Table 21.18 Pin Settings (1)

Port Name	Function	Bit and Setting					Register ⁽¹⁾
		PS1 Register	PSL1 Register	PSC Register	PD7 Register	IPS Register	
P73	ISTxD1 output	PS1_3 = 1	PSL1_3 = 0	PSC_3 = 1	-	-	G1POCR0
P74	ISCLK1 input	PS1_4 = 0	-	-	PD7_4 = 0	IPS1 = 0	-
	ISCLK1 output	PS1_4 = 1	PSL1_4 = 0	PSC_4 = 1	-	-	G1POCR1
P75	ISRxD1 input	PS1_5 = 0	-	-	PD7_5 = 0	IPS1 = 0	-
P76	ISTxD0 output	PS1_6 = 1	PSL1_6 = 0	PSC_6 = 0	-	-	G0POCR0
P77	ISCLK0 input	PS1_7 = 0	-	-	PD7_7 = 0	IPS0 = 0	-
	ISCLK0 output	PS1_7 = 1	-	-	-	-	G0POCR1

NOTES:

1. Set the MOD2 to MOD0 bits in the corresponding register to "1112" (output of the communication function used).

Table 21.19 Pin Settings (2)

Port Name	Function	Bit and Setting			Register
		PS2 Register	PD8 Register	IPS register	
P80	ISRxD0 input	PS2_0 = 0	PD8_0 = 0	IPS0 = 0	-

Table 21. 20 Pin Settings (3)

Port Name	Function	Bit and Setting			Register ⁽¹⁾
		PS5 Register	PD11 Register	IPS Register	
P110	ISTxD1 output	PS5_0 = 1	-	-	G1POCR0
P111	ISCLK1 input	PS5_1 = 0	PD11_1 = 0	IPS1 = 1	-
	ISCLK1 output	PS5_1 = 1	-	-	G1POCR1
P112	ISRxD1 input	PS5_2 = 0	PD11_2 = 0	IPS1 = 1	-

NOTES:

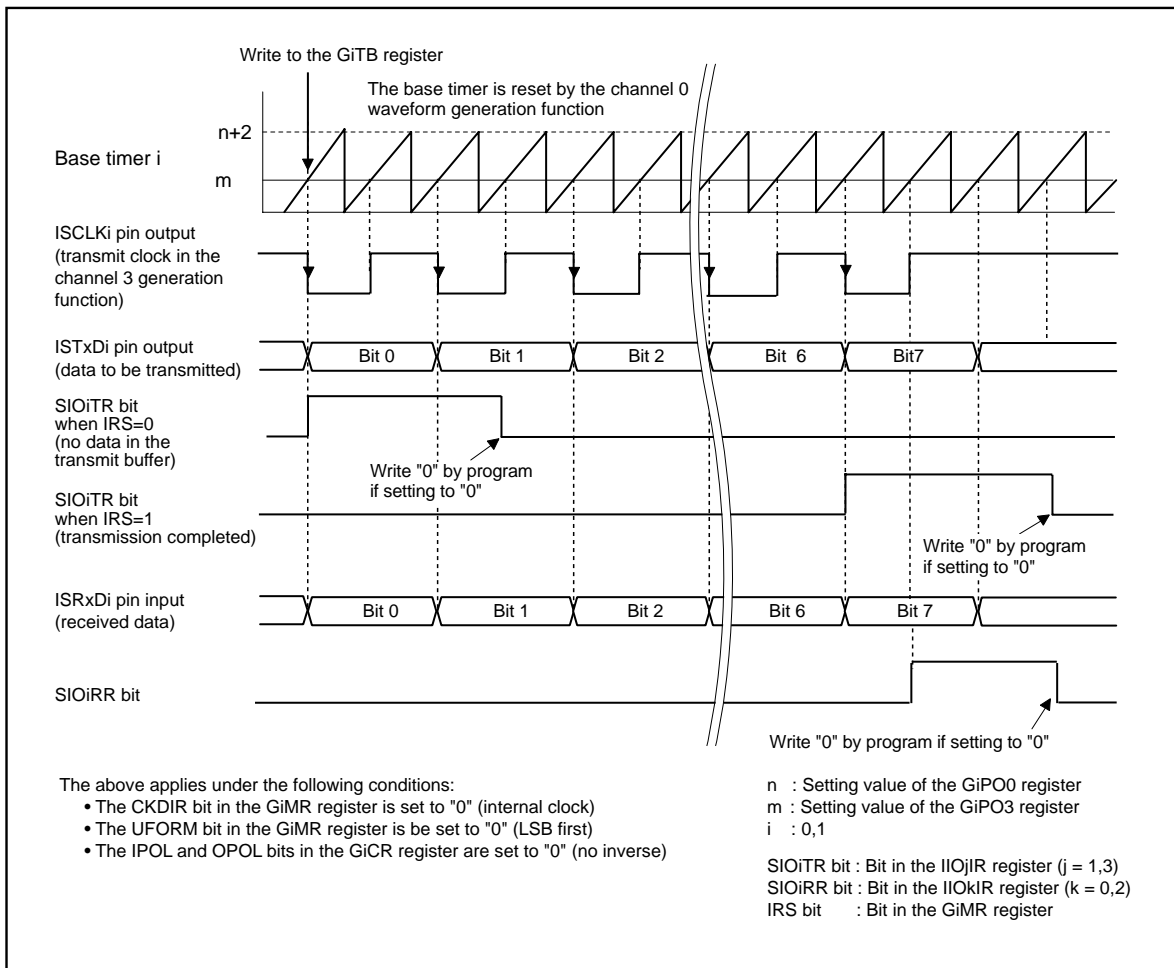
- Set the MOD2 to MOD0 bits in the corresponding register to "1112" (output of the communication function used).

Table 21. 21 Pin Settings (4)

Port Name	Function	Bit and Setting			Register ⁽¹⁾
		PS9 Register	PD15 Register	IPS Register	
P150	ISTxD0 output	PS9_0 = 1	-	-	G0POCR0
P151	ISCLK0 input	PS9_1 = 0	PD15_2 = 0	IPS0 = 1	-
	ISCLK0 output	PS9_1 = 1	-	-	G0POCR1
P152	ISRxD0 input	PS9_2 = 0	PD15_2 = 0	IPS0 = 1	-

NOTES:

- Set the MOD2 to MOD0 bits in the corresponding register to "1112" (output of the communication function used).

**Figure 21.39 Transmit and Receive Operation**

21.4.2 Clock Asynchronous Serial I/O Mode (UART) (Groups 0 and 1)

In clock asynchronous serial I/O mode (UART), data is transmitted at a desired bit rate and in a desired transfer data format. Table 21.22 lists specifications of UART mode groups 0 and 1. Table 21.23 lists registers to be used and their settings. Tables 21.24 to 21.27 list pin settings. Figure 21.40 shows an example of transmit operation. Figure 21.41 shows an example of receive operation.

Table 21.22 UART Mode Specifications

Item	Specification
Transfer Data Format	<ul style="list-style-type: none"> Character Bit (transfer data) : 8 bits long Start bit : 1 bit long Stop bit : select length from 1 bit or 2 bits
Transfer Clock ^(1, 2)	<p>When the CKDIR bit in the GiMR register (i=0, 1) is set to "0" (internal clock) : $\frac{f_{BTi}}{2(n+2)}$</p> <p>n : setting value of the GiPO0 register, 0000₁₆ to FFFF₁₆.</p> <ul style="list-style-type: none"> The GiPO0 register determines the bit rate. <p>Transmit clock is generated in phase-delayed waveform output mode of the channel 3 waveform generation function.</p> <p>Receive clock is generated with the channel 2 time measurement function.</p>
Transmit Start Condition	<p>Set the registers associated with the waveform generation function, the GiMR register and GiERC register. Then, set as written below after at least one transfer clock cycle.</p> <ul style="list-style-type: none"> Set the TE bit in the GiCR register to "1" (transmit enable) Set the TI bit in the GiCR register to "0" (data in the GiTB register)
Receive Start Condition	<p>Set the registers associated with the waveform generation function, the GiMR register and GiERC register. Then, set as written below after at least one transfer clock cycle.</p> <ul style="list-style-type: none"> Set the RE bit in the GiCR register to "1" (receive enable) Detect the start bit
Interrupt Request	<ul style="list-style-type: none"> While transmitting, one of the following conditions can be selected to set the SIOiTR bit to "1" (see Figure 10.14): <ul style="list-style-type: none"> The IRS bit in the GiMR register is set to "0" (no data in the GiTB register) and data is transferred to the transmit register from the GiTB register. The IRS bit is set to "1" (transmission completed) and data transfer from the transmit register is completed While receiving, the following condition can be selected to set the SIOiRR bit to "1" (see Figure 10.14) : <ul style="list-style-type: none"> Data is transferred from the receive register to the GiRB register (data reception is completed)
Error detection	<ul style="list-style-type: none"> Overrun error⁽³⁾ <ul style="list-style-type: none"> This error occurs when the final stop bit of the next data is received before reading the GiRB register Framing Error <ul style="list-style-type: none"> This error occurs when the number of the stop bits set is not detected
Selectable function	<ul style="list-style-type: none"> Stop bit length <ul style="list-style-type: none"> The length of the stop bit is selected from 1 bit or 2 bits LSB first/MSB first <ul style="list-style-type: none"> Select either bit 0 or bit 7 to transmit/receive data

NOTES:

1. The transfer clock must be f_{BTi} divided by six or more.
2. Set the GiPOCR2 register and the GiTMCR2 register.
3. When an overrun error occurs, the GiRB register is indeterminate.

Table 21.23 Registers to be Used and Settings

Register	Bit	Function
GiBCR0	BCK1 to BCK0	Set to "112"
	DIV4 to DIV0	Select divide ratio of count source
	IT	Set to "0"
GiBCR1	7 to 0	Set to "0001 0010 ₂ "
GiPOCR0	7 to 0	Set to "0000 0111 ₂ "
GiPOCR2	7 to 0	Set to "0000 0110 ₂ "
GiPOCR3	7 to 0	Set to "0000 0010 ₂ "
GiTMCR2	7 to 0	Set to "0000 0010 ₂ "
GiPO0	15 to 0	Set bit rate $\frac{f_{BTi}}{2 \times (\text{setting value} + 2)} = \text{transfer clock frequency}$
GiPO3	15 to 0	Set to a value smaller than the GiPO0 register
GiFS	FSC3 to FSC0	Set to "0100 ₂ "
GiFE	IFE3 to IFE0	Set to "1101 ₂ "
GiMR	GMD1 to GMD0	Set to "00 ₂ "
	CKDIR	Set to "0"
	STPS	Select stop bit length
	UFORM	Select LBS first or MSB first
	IRS	Select how the receive interrupt is generated
GiCR	TI	Transmit buffer empty flag
	TXEPT	Transmit register empty flag
	RI	Receive complete flag
	TE	Set to "1" to enable transmission
	RE	Set to "1" to enable reception
	IPOL	Set to "1"
	OPOL	Set to "1"
GiTB	7 to 0	Write data to be transmitted
GiRB	15 to 0	Received data and error flag are stored

i = 0 to 1

Table 21.24 Pin Settings in UART Mode (1)

Port Name	Function	Bit and Setting					Register ⁽¹⁾
		PS1 Register	PSL1 Register	PSC Register	PD7 Register	IPS Register	
P73	ISTxD1 output	PS1_3 = 1	PSL1_3 = 0	PSC_3 = 1	-	-	G1POCR0
P75	ISRxD1 input	PS1_5 = 0	-	-	PD7_5 = 0	IPS1 = 0	-
P76	ISTxD0 output	PS1_6 = 1	PSL1_6 = 0	PSC_6 = 0	-	-	G0POCR0

NOTES:

1. Set the MOD2 to MOD0 bits in the corresponding register to "1112" (output of the communication function used).

Table 21.25 Pin Settings (2)

Port Name	Function	Bit and Setting				Register
		PS2 Register	PSL2 Register	PD8 Register	IPS Register	
P80	ISRxD0 input	PS2_0 = 0	-	PD8_0 = 0	IPS0 = 0	-

Table 21.26 Pin Settings (3)

Port Name	Function	Bit and Setting			Register ⁽¹⁾
		PS5 Register	PD11 Register	IPS Register	
P110	ISTxD1 output	PS5_0 = 1	-	-	G1POCR0
P112	ISRxD1 input	PS5_2 = 0	PD11_2 = 0	IPS1 = 1	-

NOTES:

1. Set the MOD2 to MOD0 bits in the corresponding register to "1112" (output of the communication function used).

Table 21.27 Pin Settings (4)

Port Name	Function	Bit and Setting			Register ⁽¹⁾
		PS9 Register	PD15 Register	IPS Register	
P150	ISTxD0 output	PS9_0 = 1	-	-	G0POCR0
P152	ISRxD0 input	-	PD15_2 = 0	IPS0 = 1	-

NOTES:

1. Set the MOD2 to MOD0 bits in the corresponding register to "1112" (output of the communication function used).

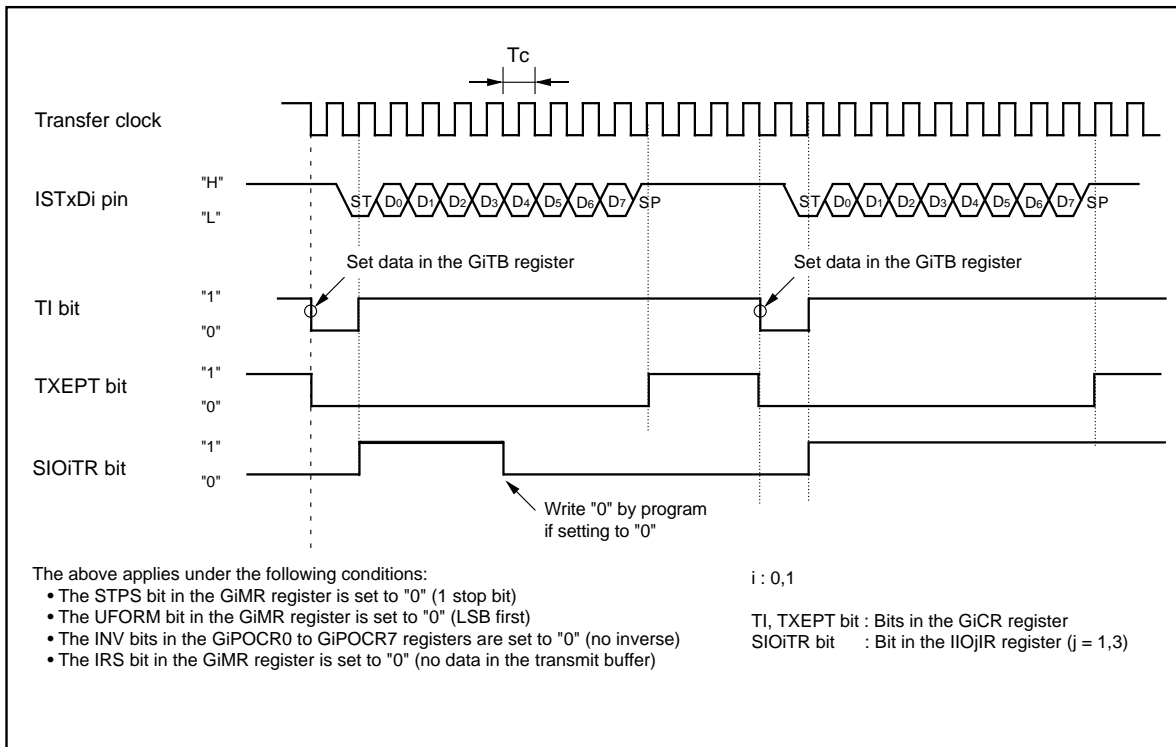


Figure 21.40 Transmit Operation

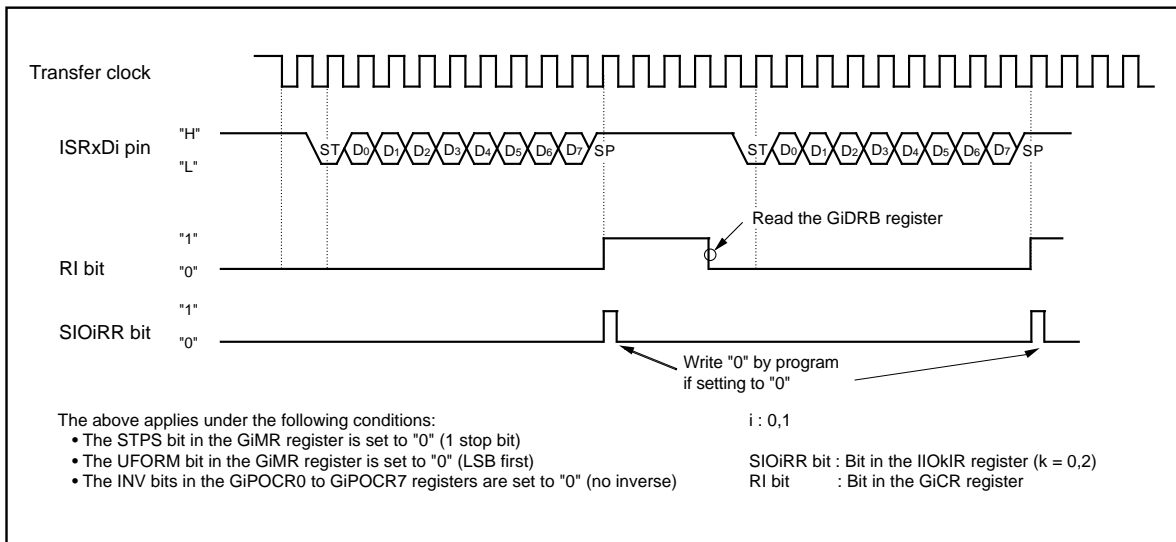


Figure 21.41 Receive Operation

21.4.3 HDLC Data Processing Mode (Group 0 and 1)

In HDLC data processing mode, bit stuffing, flag detection, abort detection and CRC calculation are available for HDLC control. The channel 0 and 1 are used to generate the transfer clock. No pins are used.

To convert data, data to be transmitted is written to the GiTB register (i=0,1) and the data conversion result is restored after data conversion. If any data are in the GiTO register after data conversion, the conversion is terminated. If no data is in the GiTO register, bit stuffing processing is executed regardless of there being no data in the transmit output buffer. A CRC value is calculated every time one bit is converted. If no data is in the GiRI register, received data conversion is terminated.

Table 21.28 list specifications of the HDLC data processing mode. Table 21.29 lists registers to be used and their settings.

Table 21.28 HDLC Processing Mode Specifications

Item	Specification
Input Data Format	8-bit data fixed, bit alignment is optional
Output Data Format	8-bit data fixed
Transfer Clock	<p>When the CKDIR bit in the GiMR register (i=0, 1) is set to "0" (internal clock) : $\frac{f_{BTi}}{n+2}$</p> <p>n : setting value of the GiPO0 register 0000₁₆ to FFFF₁₆</p> <ul style="list-style-type: none"> The GiPO0 register determines bit rate. <p>The transfer clock is generated in phase-delayed waveform output mode of the channel 1 waveform generation function.</p> <p>When the RSHTTE bit in the GiERC register is set to "1" (reception shift operation enabled), the transfer clock is generated in the receiver</p>
I/O Method	<ul style="list-style-type: none"> While transmitting, value set in the GiTB register is converted in HDLC data processing mode and transferred to the GiTO register While receiving, value set in the GiRI register is converted in HDLC data processing mode and transferred to the GiRB register. The value in the GiRI register is also transferred to the GiDR register (received data register).
Bit Stuffing	<p>While transmitting, "0" following five consecutive "1" is inserted.</p> <p>While receiving, "0" following five consecutive "1" is deleted.</p>
Flag Detection	Write the flag data "7E ₁₆ " to the GiCMP3 register to use the special communication interrupt (the SRTiR bit in the IIO4IR register)
Abort Detection	Write the masked data "01 ₁₆ " to the GiMSKk(k=0, 1) register
CRC	<p>The CRC1 to CRC0 bits are set to "11₂" ($X^{16}+X^{12}+X^5+1$)</p> <p>The CRCV bit is set to "1" (set to "FFFF₁₆")</p> <ul style="list-style-type: none"> While transmitting, CRC calculation result is stored into the GiTCRC register. The TCRCE bit in the GiETC register is set to "1" (transmit CRC used). The CRC calculation result is reset when the TE bit in the GiCR register is set to "0" (transmit disabled)⁽¹⁾. While receiving, CRC calculation result is stored into the GiRCRC register. The RCRCE bit in the GiERC register is set to "1" (receive CRC used). The CRC calculation result is reset by comparing the flag data "7E₁₆" and matching the result with the value in the GiCMP3 register. The ACRC bit in the GiEMR register is set to "1" (CRC reset)⁽²⁾

Table 21.28 HDLC Processing Mode Specifications (Continued)

Item	Specification
Data Processing Start Conditions	<p>The following conditions are required to start transmit data processing:</p> <ul style="list-style-type: none"> • The TE bit in the GiCR register is set to "1" (transmit enable) • Data is written to the GiTB register <p>The following conditions are required to start receive data processing:</p> <ul style="list-style-type: none"> • The RE bit in the GiCR register is set to "1" (receive enable) • Data is written to the GiRI register
Interrupt Request ⁽³⁾	<p>During transmit data processing,</p> <p>(1) One of the following conditions can be selected to set the GiTOR bit in the interrupt request register to "1" (interrupt request) (see Figure 10.14)</p> <ul style="list-style-type: none"> – When the IRS bit in the GiMR register is set to "0" (no data in the GiTB register) and data is transferred from the GiTB register to the transmit register (transmit start) – When the IRS bit is set to "1" (transmission completed) and data transfer from the transmit register to the GiTO register is completed <p>(2) When data, which is already converted to HDLC data, is transferred from the receive register of the GiTO register to the transmit buffer, the GiTOR bit is set to "1"</p> <p>During received data processing,</p> <p>(1) When data is transferred from the GiRI register to the GiRB register (reception completed), the GiRIR bit is set to "1" (See Figure 10.14)</p> <p>(2) When received data is transferred from the receive buffer of the GiRI register to the receive register, the GiRIR bit is set to "1"</p> <p>(3) When the GiTB register is compared to the GiCMPj register (j=0 to 3), the SRTiR bit is set to "1"</p>

NOTES:

1. Set the CRCV bit and ACRC bit in the GiEMR register to "1".
2. The CRC calculation circuit is reset after the GiRCRC register stores CRC data.
3. See Figure 10.14 for details on the GiTOR bit, GiRIR bit and SRTiR bit.

Table 21.29 Registers to be Used and Settings

Register	Bit	Function
GiBCR0	BCK1 to BCK0	Select count source
	DIV4 to DIV0	Select divide ratio of count source
	IT	Select the base timer interrupt
GiBCR1	7 to 0	Set to "0001 0010 ₂ "
GiPOCR0	7 to 0	Set to "0000 0000 ₂ "
GiPOCR1	7 to 0	Set to "0000 0000 ₂ "
GiPO0	15 to 0	Set bit rate
GiPO1	15 to 0	Set the timing of the rising edge of the transfer clock. Timing of the falling edge (high-level signal ("H") width of the transfer clock) is fixed. Setting value of GiPO1 ≤ Setting value of GiPO0 .
GiFS	FSC1 to FSC0	Set to "00 ₂ "
GiFE	IFE1 to IFE0	Set to "11 ₂ "
GiMR	GMD1 to GMD0	Set to "11 ₂ "
	CKDIR	Set to "0"
	UFORM	Set to "0"
	IRS	Select how the transmit interrupt is generated
GiEMR	7 to 0	Set to "1111 0110 ₂ "
GiCR	TI	Transmit buffer empty flag
	TXEPT	Transmit register empty flag
	RI	Receive complete flag
	TE	Transmit enable bit
	RE	Receive enable bit
GiETC	SOF	Set to "0"
	TCRCE	Select whether the transmit CRC is used or not
	ABTE	Set to "0"
	TBSF0, TBSF1	Transmit bit stuffing
GiERC	CMP2E to CMP0E	Select whether received data is compared or not
	CMP3E	Set to "1"
	RRCCE	Select whether receive CRC is used or not
	RSHTe	Set to "1" to use it in the receiver
	RBSF0, RBSF1	Receive bit stuffing
GiIRF	BSERR, ABT	Set to "0"
	IRF3 to IRF0	Select how an interrupt is generated
GiCMP0, GiCMP1	7 to 0	Write "FE ₁₆ " to abort processing
GiCMP2	7 to 0	Data to be compared
GiCMP3	7 to 0	Write "7E ₁₆ "
GiMSK0, GiMSK1	7 to 0	Write "01 ₁₆ " to abort processing
GiTCRC	15 to 0	Transmit CRC calculation result can be read
GiRCRC	15 to 0	Receive CRC calculation result can be read
GiTO	7 to 0	Data, which is output from a transmit data generation circuit, can be read
GiRI	7 to 0	Set data input to a receive data generation circuit
GiRB	7 to 0	Received data is stored
GiTB	7 to 0	For transmission : write data to be transmitted For reception : received data for comparison is stored

i = 0,1

21.5 Group 2 Communication Function

The communication function is available when two 8-bit shift registers are used with the waveform generation function.

In the intelligent I/O group 2, the variable clock synchronous serial I/O or IEBus⁽¹⁾ communication function is available. Figures 21.42 to 21.45 show registers associated with the communication function.

NOTES:

1. IEBus is a trademark of NEC Electronics Corporation.

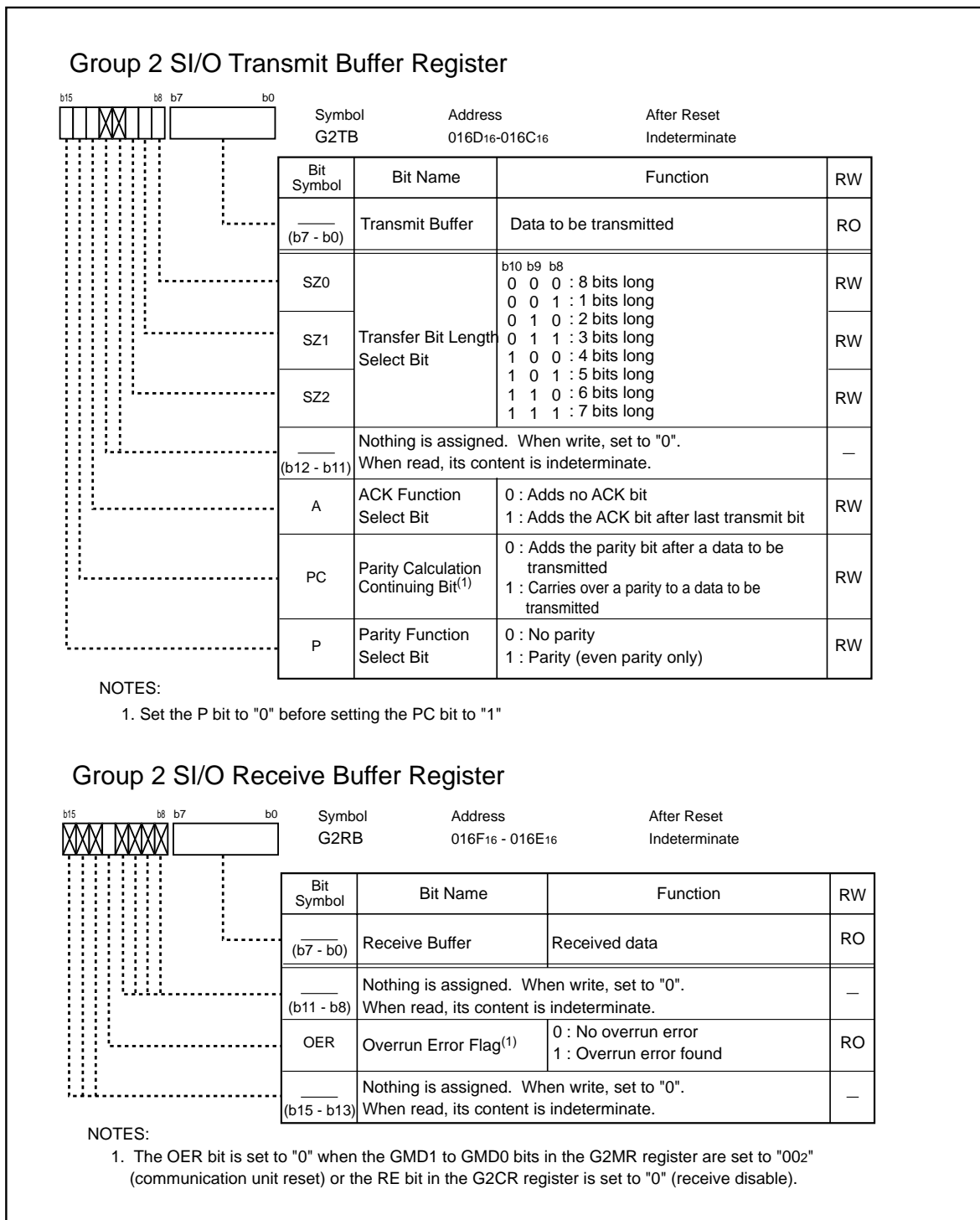


Figure 21.42 G2TB and G2RB Register

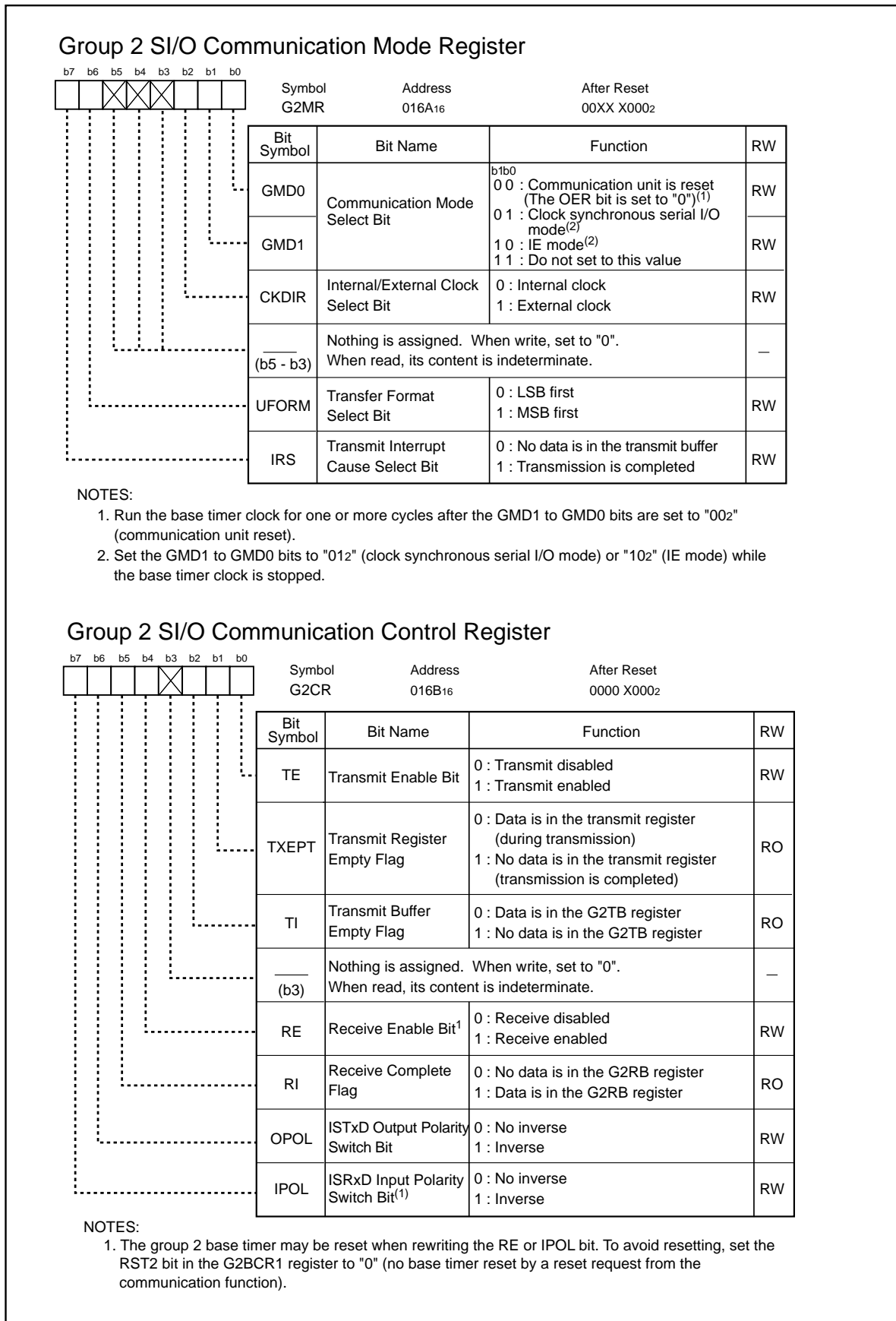


Figure 21.43 G2MR and G2CR Register

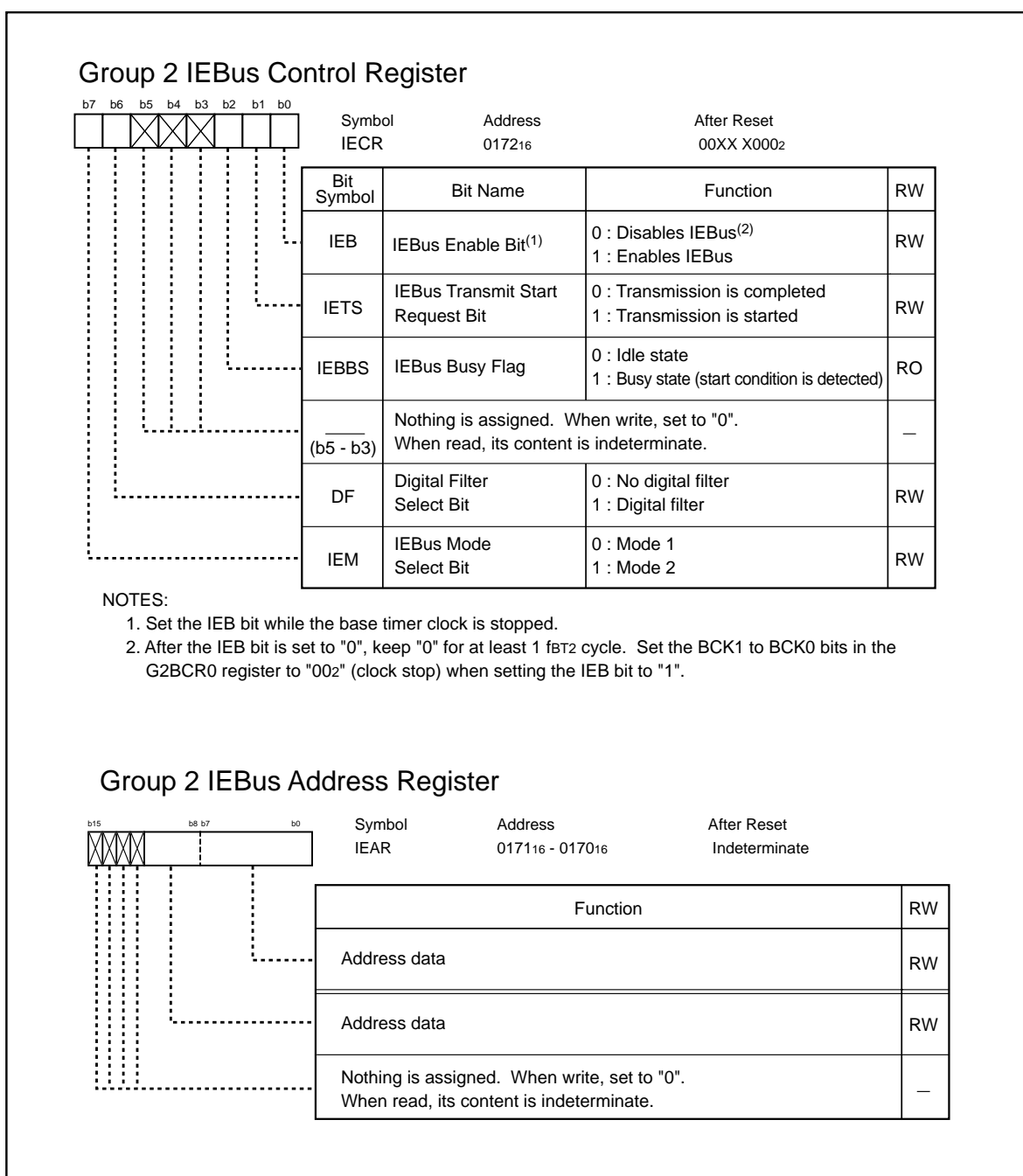


Figure 21.44 IECR and IEAR Registers

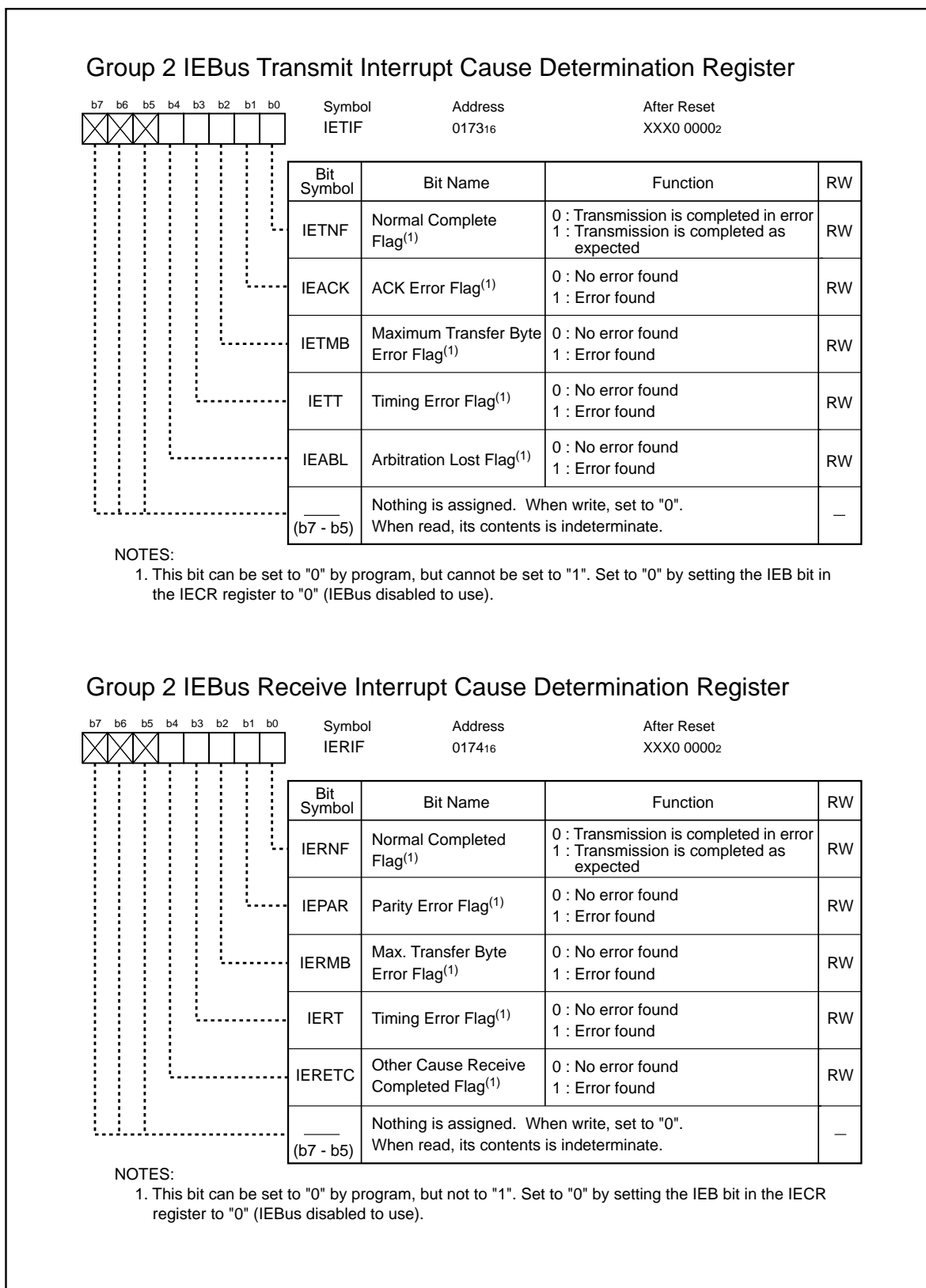


Figure 21.45 IETIF and IERIF Registers

21.5.1 Variable Clock Synchronous Serial I/O Mode (Group 2)

In variable clock synchronous serial I/O mode, data is transmitted and received using the transfer clock. The length of data transferred is selected from 1 to 8 bits. Table 21.30 lists specifications of the group 2 variable clock synchronous serial I/O mode. Table 21.31 lists registers to be used and their settings. Tables 21.32 to 21.35 lists pin settings. Figure 21.46 shows an example of a transmit and receive operation.

Table 21.30 Variable Clock Synchronous Serial I/O Mode Specifications (Group 2)

Item	Specification
Transfer Data Format	<ul style="list-style-type: none"> Transfer data length : 1 to 8 bits
Transfer Clock ⁽¹⁾	<ul style="list-style-type: none"> When the CKDIR bit in the G2MR register is set to "0" (internal clock) : $\frac{f_{BT2}}{2(n+2)}$ n : setting value of the G2PO0 register 0000₁₆ to FFFF₁₆ The G2PO0 register determines bit rate and the transfer clock is generated in phase-delayed waveform output mode of the channel 2 waveform generation function. When the CKDIR bit is set to "1" (external clock) : input from the ISCLK2 pin⁽²⁾
Transmit Start Condition	<ul style="list-style-type: none"> To start transmitting, the following conditions are required : <ul style="list-style-type: none"> - Set the TE bit in the G2CR register to "1" (transmit enable) - Write data to the G2TB register
Receive Start Condition	<ul style="list-style-type: none"> To start receiving, the following conditions are required : <ul style="list-style-type: none"> - Set the RE bit in the G2CR register to "1" (receive enable) - Set the TE bit in the G2CR register to "1" (transmit enable) - Write data to the G2TB register
Interrupt Request	<ul style="list-style-type: none"> While transmitting, one of the following conditions can be selected to set the SIO2TR bit in the IIO6IR register to "1" (see Figure 10.14): <ul style="list-style-type: none"> - The IRS bit in the G2MR register is set to "0" (no data in the G2TB register): when data is transferred from the G2TB register to the transmit register. - The IRS bit is set to "1" (reception completed): when data transfer from the transmit register is completed While receiving, the following condition can be selected to set the SIO2RR bit in the IIO5IR register to "1" (interrupt request) (see Figure 10.14): when data is transferred from the receive register to the G2RB register (data reception is completed)
Error Detection	<p>Overrun error⁽³⁾</p> <p>This error occurs when receiving the j bit (j=1 to 8) of the next data (transfer data length: j bits) before reading the G2RB register</p>
Selectable Function	<ul style="list-style-type: none"> LSB first/MSB first Select either bit 0 or bit 7 to transmit/receive data ISTxD2 and ISRxD2 I/O polarity inverse ISTxD2 pin output level and ISRxD2 pin input level are inverted Data transfer bit length Select from 1 to 8 bits

NOTES:

- The transfer clock must be fBT2 divided by six or more when both transfer clock and transfer data are transmitted. Under conditions other than this, the transfer clock must be fBT2 divided by 20 or more.
- Transfer clocks must be fBT2 divided by 20 or more.
- When an overrun error occurs, the G2RB register is indeterminate.

Table 21.31 Register to be Used and Settings

Register	Bit	Function
G2BCR0	BCK1 to BCK0	Set to "112"
	DIV4 to DIV0	Select divide ratio of count source
	IT	Set to "0"
G2BCR1	7 to 0	Set to "0001 00102"
G2POCR0	7 to 0	Set to "0000 01112"
G2POCR1	7 to 0	Set to "0000 01112"
G2BCR2	7 to 0	Set to "0000 00102"
G2PO0	15 to 0	Set bit rate $\frac{f_{BT2}}{2 \times (\text{setting value} + 2)} = \text{transfer clock frequency}$
G2PO2	15 to 0	Set to a value smaller than the G2PO0 register
G2FE	IFE2 to IFE0	Set to "1112"
G2MR	GMD1 to GMD0	Set to "012"
	CKDIR	Select internal or external clock
	UFORM	Select either LSB first or MSB first
	IRS	Select how the transmit interrupt is generated
G2CR	TE	When transmission is enabled, set to "1"
	TXEPT	Transmit register empty flag
	TI	Transmit buffer empty flag
	RE	When reception is enabled, set to "1"
	RI	Receive complete flag
	OPOL	ISTxD2 output polarity inverse (usually set to "0")
	IPOL	ISRxD2 input polarity inverse (usually set to "0")
G2TB	15 to 0	Write transfer bit length and transmit data
G2RB	15 to 0	Received data and error flag are stored

Table 21.32 Pin Settings (1)

Port Name	Function	Bit and Setting					Register ⁽²⁾
		PS1 Register	PSL1 Register	PSC Register	PD7 Register	IPS Register	
P70 ⁽¹⁾	ISTxD2 output	PS1_0 = 1	PSL1_0 = 0	PSC_0 = 1	-	-	G2POCR0
P71	ISRxD2 input	PS1_1 = 0	-	-	PD7_1 = 0	IPS5 to 4 = 002	-

NOTES:

1. P70 is a port for the N-channel open drain output.
2. Set the MOD2 to MOD0 bits in the corresponding register to "1112" (output of the communication function is used).

Table 21.33 Pin Settings (2)

Port Name	Function	Bit and Setting				Register ⁽²⁾
		PS3 Register ⁽¹⁾	PSL3 Register	PD9 Register ⁽¹⁾	IPS Register	
P91	ISRxD2 input	PS3_1=0	-	PD9_1=0	IPS5 to 4=012	-
P92	ISTxD2 output	PS3_2=1	PSL3_2=1	-	-	G2POCR0

NOTES:

1. Set the PD9 and PS3 registers immediately after the PRC2 bit in the PRCR register is set to "1" (write enable). Do not generate an interrupt or a DMA transfer between the instruction to set to the PRC2 bit to "1" and the instruction to set the PD9 and PS3 registers.
2. Set the MOD2 to MOD0 bits in the corresponding register to "1112" (output of the communication function used).

Table 21.34 Pin Settings (3)

Port Name	Function	Bit and Setting				Register ⁽¹⁾
		PS0 Register	PSL0 Register	PD6 Register	IPS Register	
P64	ISCLK2 input	PS0_4 = 0	-	PD6_4 = 0	IPS6 = 0	-
	ISCLK2 output	PS0_4 = 1	PSL0_4 = 1	-	-	G2POCR1

NOTES:

1. Set the MOD2 to MOD0 bits in the corresponding register to "1112" (output of the communication function used).

Table 21.35 Pin Settings (4)

Port Name	Function	Bit and Setting			Register ⁽¹⁾
		PS7 Register	PD13 Register	IPS Register	
P134	ISTxD2 output	PS7_4 = 1	-	-	G2POCR0
P135	ISRxD2 input	PS7_5 = 0	PD13_5 = 0	IPS5 to 4 = 102	-
P136	ISCLK2 input	PS7_6 = 0	PD13_6 = 0	IPS6 = 1	-
	ISCLK2 output	PS7_6 = 1	-	-	G2POCR1

NOTES:

1. Set the MOD2 to MOD0 bits in the corresponding register to "1112" (output of the communication function used).

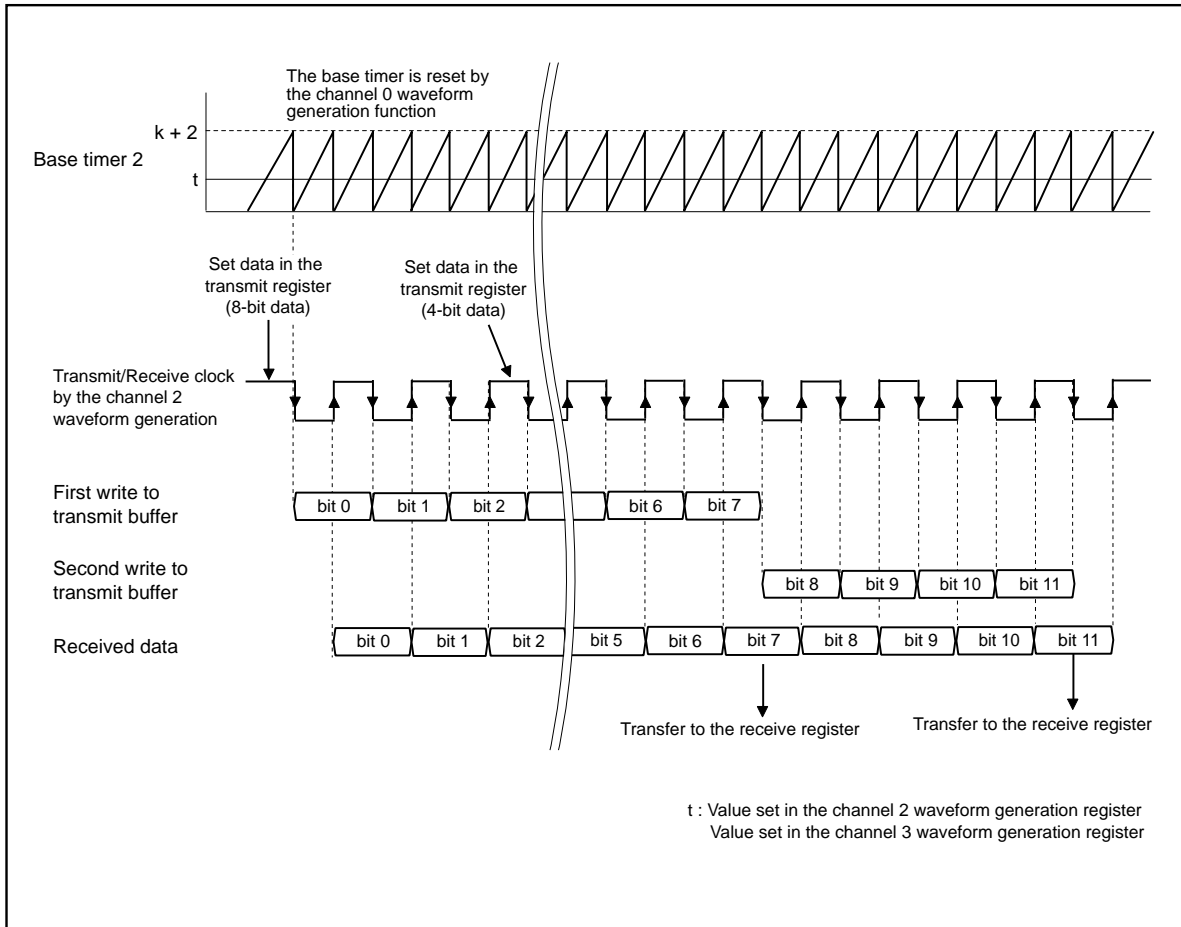


Figure 21.46 Transmit and Receive Operation

21.5.2 IEBus Mode (Group 2)

Table 21.36 lists specifications of IEBus mode. Table 21.37 lists registers to be used and settings. Tables 21.38 to 21.40 lists pin settings.

Table 21.36 IEBus Mode Specifications

Item	Specification
Transfer Data Format	<ul style="list-style-type: none"> Transfer data length: 1 to 8 bits
Transfer Clock	<ul style="list-style-type: none"> When the CKDIR bit in the G2MR register is set to "0" (internal clock) : $\frac{f_{BT2}}{2(n+2)}$ n : setting value of the G2PO0 register, 0000₁₆ to FFFF₁₆. The G2PO0 register determines bit rate and the transfer clock is generated in phase-delayed waveform output mode of the channel 2 waveform generation function. The G2PO2 register = $(n+2)/2^{(1)}$ When the CKDIR bit is set to "1" (external clock) : input from the ISCLK2 pin⁽²⁾
Transmit Start Condition	<p>To start transmitting, the following conditions are required :</p> <ul style="list-style-type: none"> Set the TE bit in the G2CR register to "1" (transmit enable) Write data to G2TB register
Receive Start Condition	<p>To start receiving, the following requirements must be met:</p> <ul style="list-style-type: none"> Set the RE bit in the G2CR register to "1" (receive enable) Set the TE bit in the G2CR register to "1" (transmit enable) Write data to the G2TB register
Interrupt Request	<ul style="list-style-type: none"> While transmitting, the following conditions can be selected to set the SIO2TR bit in the IIO6IR register to "1" (see Figure 10.14): <ul style="list-style-type: none"> The IRS bit in the G2MR register is set to "0" (no data in the G2TB register): when data is transferred to the transmit register from the G2TB register (transmission started) The IRS bit is set to "1" (transmission completed): when data transfer from the transmit register to the G2TO register is completed While receiving, the following condition can be selected to set the SIO2RR bit in the IIO5IR register to "1" (see Figure 10.14): when data is transferred from receive register to the G2RB register (data reception is completed)
Error Detection	<p>Overrun error⁽³⁾</p> <p>This error occurs when receiving the j bit (j=1 to 8) of the next data (transfer data length: j bits) before reading the G2RB register</p>
Selectable Function	<ul style="list-style-type: none"> LSB first/MSB first select Select either bit 0 or bit 7 to transmit/receive data ISTxD2 and ISRxD2 I/O polarity inverse ISTxD2 pin output and ISRxD2 pin input levels are inversed Data transfer bit length Select from 1 to 8 bits

NOTES:

- The transfer clock must be f_{BT2} divided by six or more when both transfer clock and transfer data are transmitted. Under conditions other than this, the transfer clock must be f_{BT2} divided by 20 or more.
- Transfer clock must be input f_{BT2} divided by 20 or more.
- When an overrun error occurs, the G2RB register is indeterminate.

Table 21.37 Registers to be Used and Settings

Register	Bit	Function
G2BCR0	BCK1 to BCK0	Set to "112"
	DIV4 to DIV0	Select divide ratio of count source
	IT	Set to "0"
G2BCR1	7 to 0	Set to "000100102"
G2POCR0 to G2POCR7	MOD2 to MOD0	Set to "1112"
	PRT	Set to "0"
	IVL	Set to "0"
	RLD	Set to "0"
	RTP	Set to "0"
	INV	Set to "0"
G2PO0 to G2PO7	15 to 0	Set compared data for waveform generation
G2FE	7 to 0	Set bit of corresponding channel to "1"
G2MR	GMD1 to GMD0	Select serial I/O mode
	CKDIR	Select internal clock or external clock
	UFORM	Select either LSB first or MSB first
	IRS	Select how the transmit interrupt is generated
G2CR	TI	Transmit buffer empty flag
	TXEPT	Transmit register empty flag
	RI	Receive complete flag
	TE	When transmission is enabled, set to "1"
	RE	When reception is enabled, set to "1"
	IPOL	ISRxD2 input polarity inverse (usually set to "0")
	OPOL	ISTxD2 output polarity inverse (usually set to "0")
IECR	IEB	Set to "1"
	IETS	When transmission starts, set to "1"
	IEBBS	Select IEBus busy flag
	DF	Select whether the digital filter is available or not
	IEM	Select mode
IEAR	11 to 0	Set address data
IETIF	IETNF	Normal complete flag when transmitting
	IEACK	ACK error flag when transmitting
	IETMB	Maximum transfer byte error flag when transmitting
	IETT	Timing error flag when transmitting
	IEABL	Arbitration lost flag when transmitting
IERIF	IERNF	Normal complete flag when receiving
	IEPAR	Parity error flag when receiving
	IERMB	Maximum transfer byte error flag when receiving
	IERT	Timing error flag when receiving
	IERETC	Other cause receive completed flag when receiving
G2RB	7 to 0	Received data and error flag are stored
	OER	Overrun error flag
G2TB	7 to 0	Write transfer bit length and data to be transmitted

Table 21.38 Pin Settings (1)

Port Name	Function	Bit and Setting					Register ⁽²⁾
		PS1 Register	PSL1 Register	PSC Register	PD7 Register	IPS Register	
P70 ⁽¹⁾	IEOUT output	PS1_0 = 1	PSL1_0 = 0	PSC_0 = 1	-	-	G2POCR0
P71	IEIN input	PS1_1 = 0	-	-	PD7_1 = 0	IPS5 to 4 = 002	-

NOTES:

1. P70 is a port for the N-channel open drain output.
2. Set the MOD2 to MOD0 bits in the G2POCR0 register to "1112".

Table 21.39 Pin Settings (2)

Port Name	Function	Bit and Setting				Register ⁽¹⁾
		PS3 Register ⁽²⁾	PSL3 Register	PD9 Register ⁽²⁾	IPS Register	
P91	IEIN input	PS3_1 = 0	-	-	IPS5 to 4 = 012	-
P92	IEOUT output	PS3_2 = 1	PSL3_2 = 1	PD9_2 = 0	-	G2POCR0

NOTES:

1. Set the MOD2 to MOD0 bits in the G2POCR0 register to "1112".
2. Set the PD9 and PS3 registers immediately after the PRC2 bit in the PRCR register is set to "1" (write enable). Do not generate an interrupt or a DMA transfer between the instruction to set to the PRC2 bit to "1" and the instruction to set the PD9 and PS3 registers.

Table 21.40 Pin Settings (3)

Port Name	Function	Bit and Setting			Register ⁽¹⁾
		PS7 Register	PSL7 Register	IPS Register	
P134	IEOUT output	PS7_4 = 1	-	-	G2POCR0
P135	IEIN input	PS7_5 = 0	PD13_5 = 0	IPS5 to 4 = 102	-

NOTES:

1. Set the MOD2 to MOD0 bits in the G2POCR0 register to "1112".

21.6 Group 3 Communication Function

The communication function is available when two 16-bit shift registers are used with the waveform generation function.

In the intelligent I/O group 3, 8-bit or 16-bit synchronous communication function is available. Figures 21.47 to 21.49 show registers associated with the communication function.

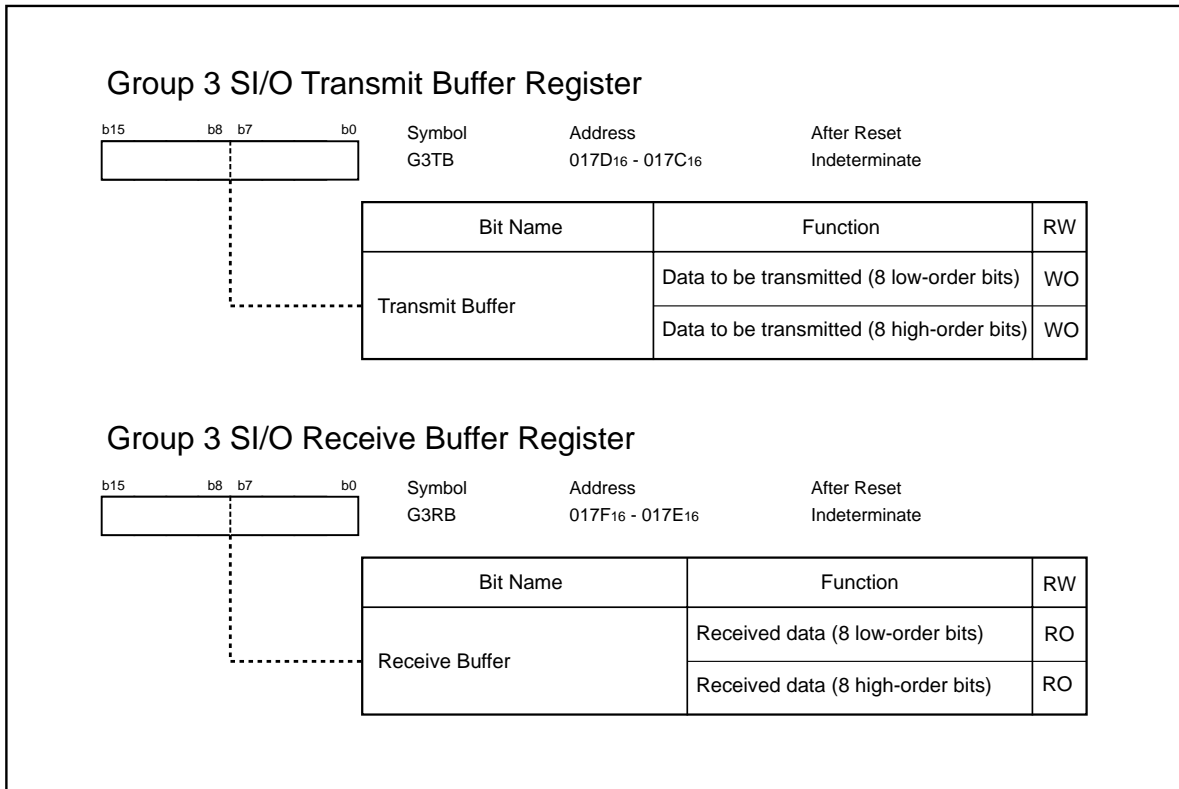


Figure 21.47 G3TB Register and G3RB Register

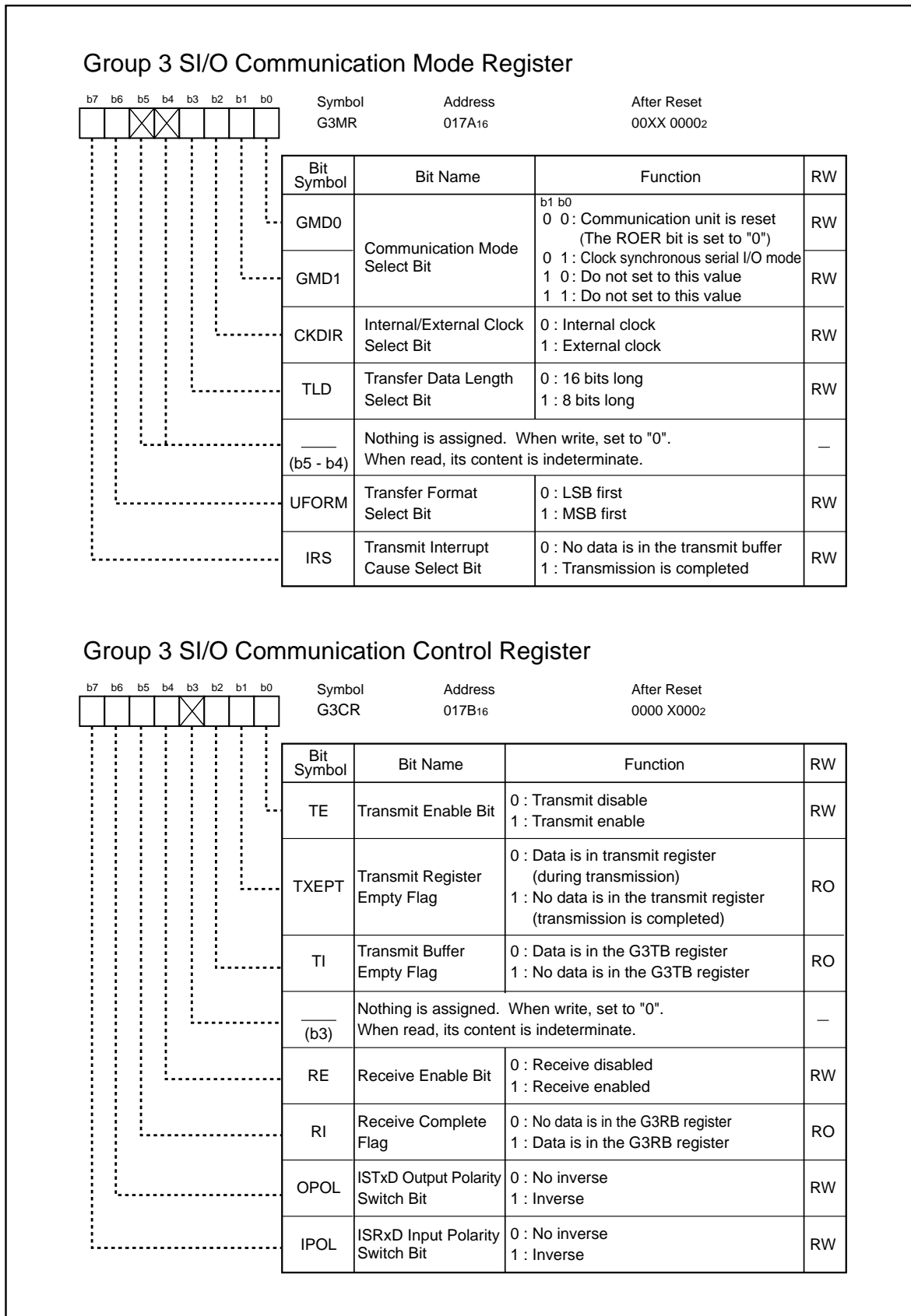
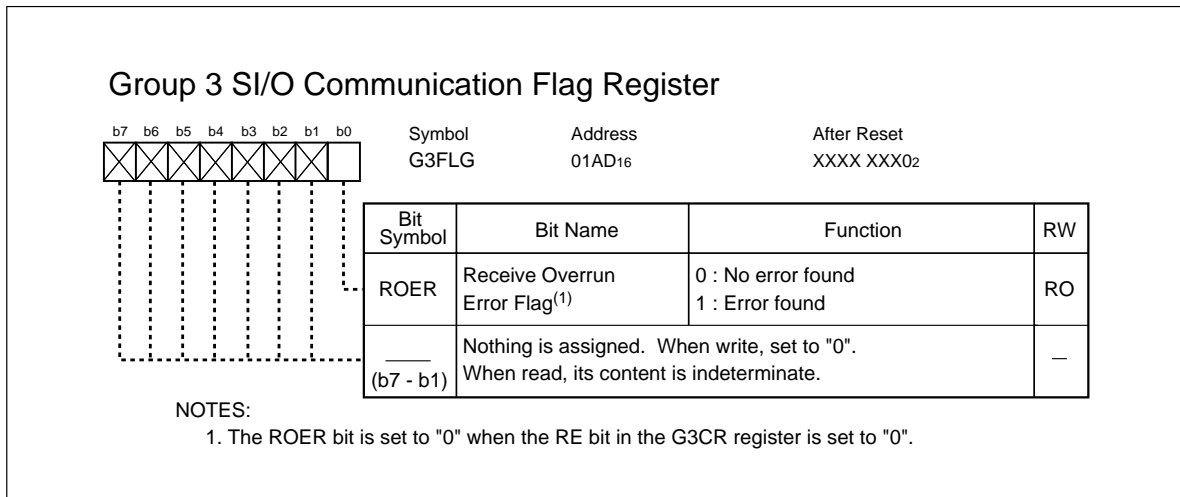


Figure 21.48 G3MR Register and G3CR Register

**Figure 21.49 G3FLG Register**

21.6.1 8-bit or 16-bit Clock Synchronous Serial I/O Mode (Group 3)

In 8-bit or 16-bit clock synchronous serial I/O mode, data is transmitted and received using the transfer clock. When the internal clock is selected as the transfer clock, the channel 0 and channel 2 waveform generation functions generate the transfer clock. ISTxD3, ISCLK3 and ISRxD3 share pins with OUTC30 to OUTC32 and are available in the 144-pin package only.

Table 21.41 lists specifications of clock synchronous serial I/O mode. Table 21.42 lists registers to be used and their settings. Tables 21.43 and 21.44 list pin settings. Figure 21.50 and 21.51 shows an example of transmit and receive operation.

Table 21.41 Clock Synchronous Serial I/O Mode (Group 3)

Item	Specification
Transfer Data Format	• Transfer data : 8 bits or 16 bits long
Transfer Clock ⁽¹⁾	<ul style="list-style-type: none"> When the CKDIR bit in the G3MR register is set to "0" (internal clock) : $\frac{f_{BT3}}{2(n+2)}$ n : setting value of the G3PO0 register, 0001₁₆ to FFFD₁₆ <ul style="list-style-type: none"> The G3PO0 register determines the bit rate and the transfer clock is generated in phase-delayed waveform output mode of the channel 2 waveform generation function. When the CKDIR bit is set to "1" (external clock) : input from the ISCLK3 pin
Transmit Start Condition ⁽²⁾	Set registers associated with the waveform generation function and the G3MR register. Then, set as written below after waiting at least one transfer clock cycle. <ul style="list-style-type: none"> Set the TE bit in the G3CR register to "1" (transmit enable) Set the TI bit in the G3CR register to "0" (data in the G3TB register)
Receive Start Condition	Set registers associated with the waveform generation function and the G3MR register. Then, set as written below after waiting at least one transfer clock cycle. <ul style="list-style-type: none"> Set the RE bit in the G3CR register to "1" (receive enable) Set the TE bit to "1" (transmit enable) Set the TI bit to "0" (data in the G3TB register)
Interrupt Request	<ul style="list-style-type: none"> While transmitting, one of the following conditions can be selected to set the SIO3TR bit in the IIO10IR register to "1" (see Figure 10.14) : <ul style="list-style-type: none"> When the IRS bit in the G3MR register is set to "0" (no data in the transmit buffer), one transfer clock cycle after data transmission starts When the IRS bit is set to "1" (reception completed), 15 transfer clock cycles after data transmission starts in 16-bit clock synchronous serial I/O mode (set the DLS bit in the G3MR register to "0"), or 7 transfer clock cycles after data transmission starts in 8-bit clock synchronous serial I/O mode (set the DLS bit to "1"). While receiving, the following condition can be selected to set the SIO3RR bit in the IIO9IR register to "1" (see Figure 10.14) : <ul style="list-style-type: none"> 15.5 transfer clock cycles after data transmission starts in 16-bit clock synchronous serial I/O mode, or 7.5 transfer clock cycles after data transmission starts in 8-bit clock synchronous serial I/O mode
Error Detection	<ul style="list-style-type: none"> Overrun error⁽³⁾ This error occurs in 16-bit clock synchronous serial I/O mode when the 15th bit of the next data is received before reading the G3RB register. This error occurs in 8-bit clock synchronous serial I/O mode when the 7th bit of the next data is received before reading the G3RB register.
Selectable Function	<ul style="list-style-type: none"> LSB first/MSB first Select either bit 0 or bit 7 to transmit/receive data ISTxD3 and ISRxD3 I/O polarity inverse ISTxD3 pin output level and ISRxD3 pin input level are inversed

NOTES:

- The transfer clock must be fBT3 divided by six or more.
- Transmit interrupt request is generated when the TE bit is set to "1". Set the interrupt-associated registers after setting the TE bit.
- When an overrun error occurs, the G3RB register is indeterminate.

Table 21.42 Registers to be Used and Settings

Register	Bit	Function
G3BCR0	BCK1 to BCK0	Set to "112"
	DIV4 to DIV0	Select divide ratio of count source
	IT	Set to "0"
G3BCR1	7 to 0	Set to "0001 0010 ₂ "
G3POCR0	7 to 0	Set to "0000 0111 ₂ "
G3POCR1	7 to 0	Set to "0000 0111 ₂ "
G3POCR2	7 to 0	Set to "0000 0010 ₂ "
G3PO0	15 to 0	Set bit rate $\frac{f_{BT3}}{2 \times (\text{setting value} + 2)} = \text{transfer clock frequency}$
G3PO2	15 to 0	Set to a value smaller than the G3PO0 register
G3FE	7 to 0	Set to "0000 0111 ₂ "
G3MR	GMD1 to GMD0	Set to "01 ₂ "
	CKDIR	Select the internal clock or external clock
	TLD	Select transfer data length
	UFORM	Select either LSB first or MSB first
	IRS	Select how the transmit interrupt is generated
G3CR	TE	Set to "1" to enable transmission
	TXEPT	Transmit register empty flag
	TI	Transmit buffer empty flag
	RE	Set to "1" to enable reception
	RI	Receive complete flag
	OPOL	ISTxD3 output polarity inverse (usually set to "0")
	IPOL	ISRxD3 input polarity inverse
G3TB	15 to 0	Write transmit data
G3RB	15 to 0	Received data is stored

Table 21.43 Pin Setting in Clock Synchronous Serial I/O Mode (Group 3)

Port Name	Function	Bit and Setting				Register ⁽¹⁾
		PS2 Register	PSL2 Register	PD8 Register	IPS Register	
P81	ISTxD3 output	PS2_1 = 1	PSL2_1 = 1	-	-	G3POCR0
P82	ISRxD3 input	PS2_2 = 0	-	PD8_2 = 0	IPS7 = 0	-

NOTES:

- Set the MOD2 to MOD0 bits in the corresponding register to "111₂" (output of the communication function used).

Table 21.44 Pin Setting (Continued)

Port Name	Function	Bit and Setting			Register ⁽¹⁾
		PS6 Register	PD12 Register	IPS Register	
P120	ISTxD3 output	PS6_0 = 1	-	-	G3POCR0
P121	ISCLK3 input	PS6_1 = 0	PD12_1 = 0	-	-
	ISCLK3 output	PS6_1 = 1	-	-	G3POCR1
P122	ISRxD3 input	PS6_2 = 0	PD12_2 = 0	IPS7 = 1	-

NOTES:

- Set the MOD2 to MOD0 bits in the corresponding register to "111₂" (output of the communication function used).

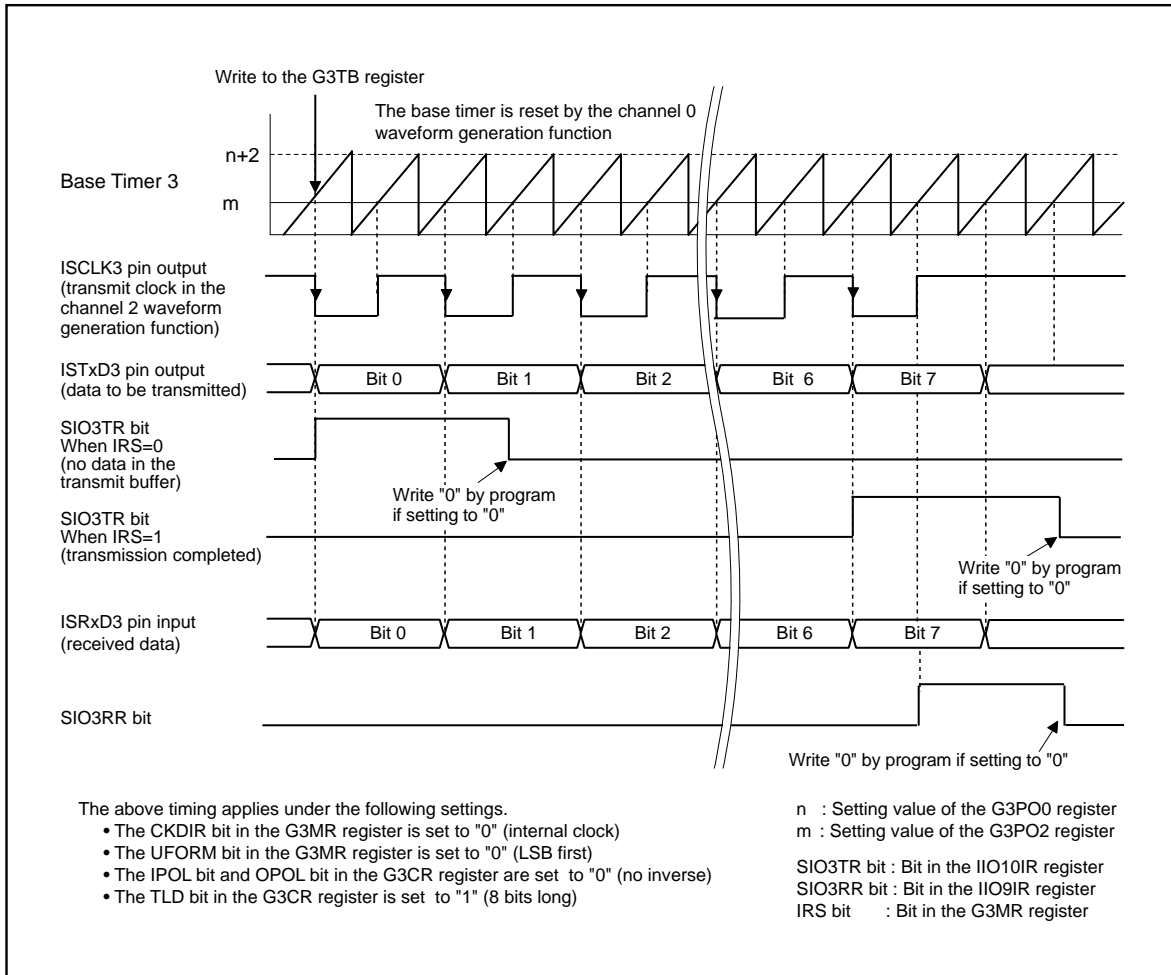


Figure 21. 50 Transmit and Receive Operation (8-bit Length)

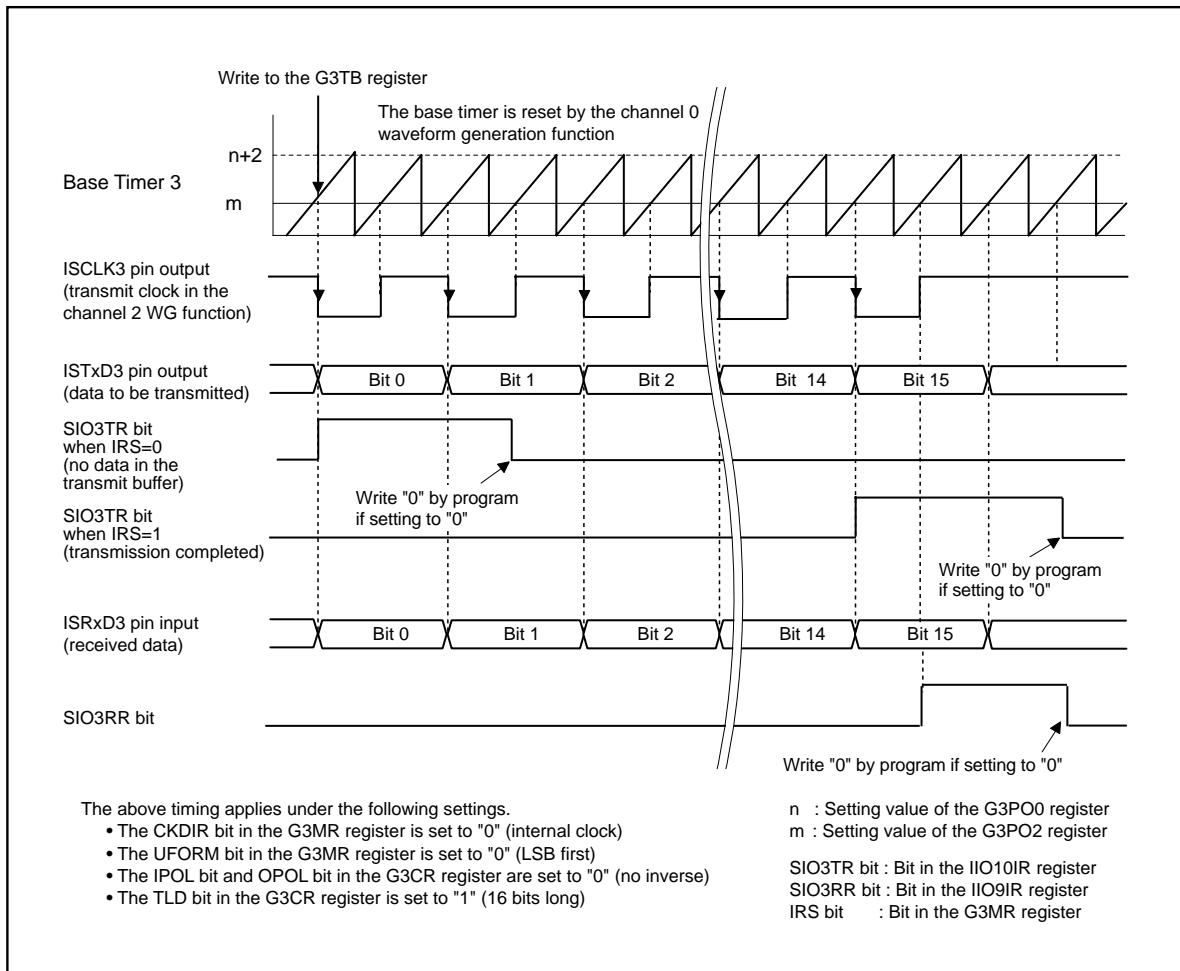


Figure 21. 51 Transmit and Receive Operation (16-bit Length)

22. CAN Module

The CAN (Controller Area Network) module incorporated in the M32C/83 group is a Full CAN module, compatible with CAN Specification 2.0 Part B. Table 22.1 lists specifications of the CAN module.

Table 22.1 CAN Module Specifications

Item	Specification
Protocol	CAN Specification 2.0 Part B
Message Slots	16 slots
Polarity	Dominant: "L" Recessive: "H"
Acceptance Filter	Global mask: 1 mask (for message slots 0 to 13) Local mask: 2 masks (for message slots 14 and 15 respectively)
Baud Rate	$\text{Baud rate} = \frac{1}{T_q \text{ clock cycle} \times T_q \text{ per bit}} \quad \text{--- Max. 1 Mbps}$ $T_q \text{ clock cycle} = \frac{\text{BRP} + 1}{f_1}$ $T_q \text{ per bit} = \text{SS} + \text{PTS} + \text{PBS1} + \text{PBS2}$ <p> Tq: Time quantum BRP: Setting value in the C0BRP and C1BRP registers, 1-255 SS: Synchronization Segment; 1 Tq PTS: Propagation Time Segment; 1 to 8 Tq PBS1: Phase Buffer Segment 1; 2 to 8 Tq PBS2: Phase Buffer Segment 2; 2 to 8 Tq </p>
Remote Frame Automatic Answering Function	Message slot that receives the remote frame transmits the data frame automatically
Time Stamp Function	Time stamp function with a 16-bit counter. Count source can be selected from the CAN bus bit clock divided by 1, 2, 3 or 4.
BasicCAN Mode	BasicCAN function can be used with the CANi message slots 14 and 15.
Transmit Abort Function	Transmit request is aborted
Loopback Function	Frame transmitted by the CAN module is received by the same CAN module
Forcible Error Active Clear Function	The CAN module is forced into an error active state

NOTES:

1. Use an oscillator with maximum 1.58% oscillation tolerance.

Figure 22.1 shows a block diagram of the CAN module. Figure 22.2 shows CANi message slot buffer (the message slot buffer) (i=0,1) and CANi message slot (the message slot) j (j=0 to 15). Table 22.2 lists pin settings of the CAN module.

The message slot cannot be accessed directly from the CPU. Allocate the message slot j to be used to the message slot buffer 0 or 1. The message slot j is accessed via the message slot buffer address. The CiSBS register selects the message slot j to be allocated. Figure 22.2 shows the 16-byte message slot buffer and message slot.

22.1 CAN-Associated Registers

Figures 22.3 to 22.26 show registers associated with CAN. To access the associated registers, set the MCD4 to MCD0 bits in the MCD register to "100102" (no division of CPU clock), the PM13 bit in the PM1 register to "1" (2 wait states), and the CM07 bit in the CM0 register to "0" (XIN-XOUT selected).

22.1.1 CAN0 Control Register 0 (C0CTRL0 Register)

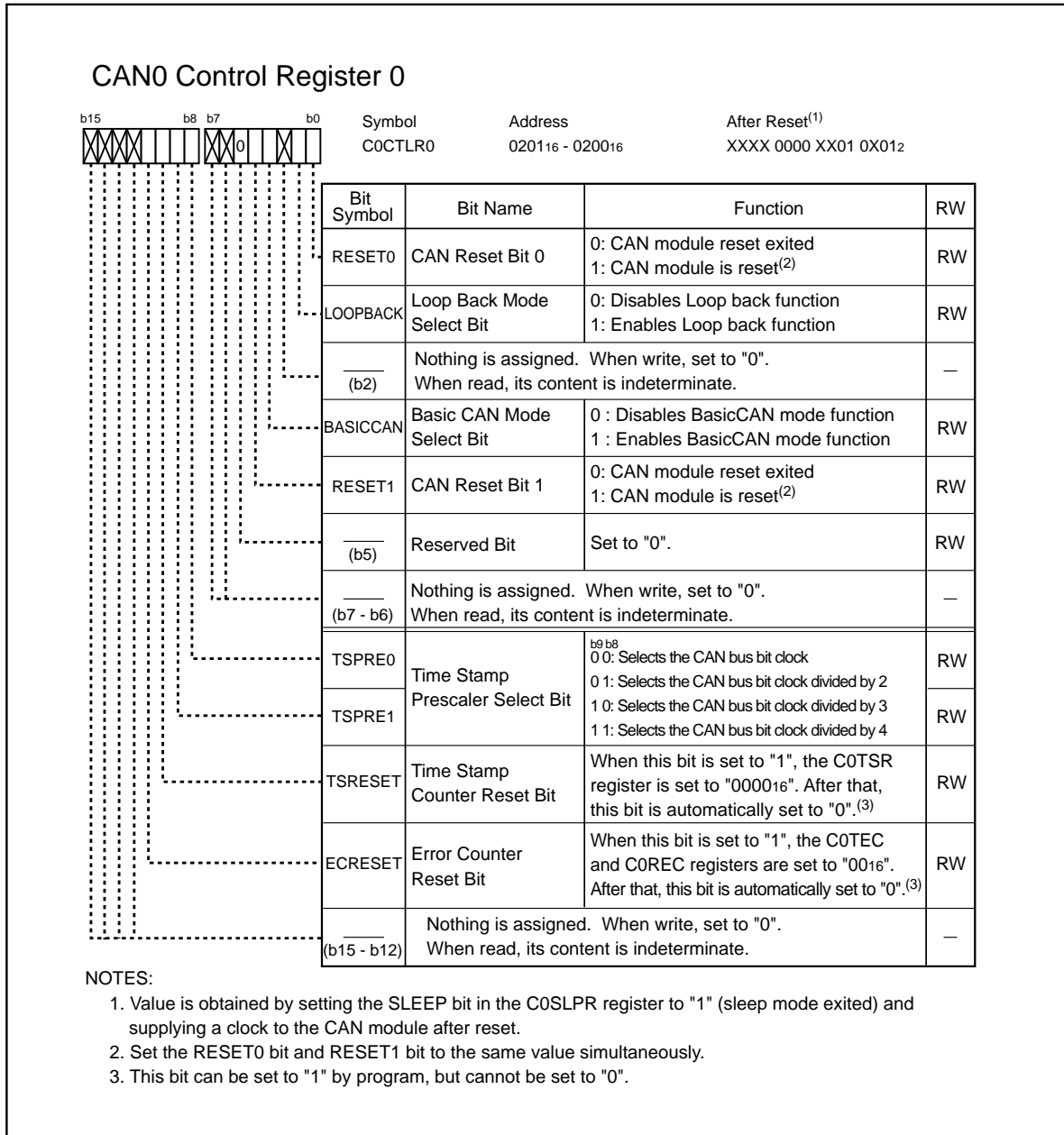


Figure 22.3 C0CTRL0 Register

22.1.1.1 RESET0 Bit and RESET1 Bit

When both RESET0 and RESET1 bits are set to "1", the CAN module is immediately reset regardless of ongoing CAN communication.

After the RESET0 and RESET1 bits are set to "1" and the CAN module reset is completed, the C0TSR register is set to "0000₁₆". The C0TEC and C0REC registers are set to "00₁₆" and the STATE_ERRPAS and STATE_BUSOFF bits in the C0STR register are set to "0" as well.

When both RESET0 and RESET1 bits are changed "1" to "0", the C0TSR register starts counting. CAN communication is available after 11 continuous recessive bits are detected.

NOTES:

1. Set the same value in both RESET0 and RESET1 bits simultaneously.
2. Set CAN configuration upon confirming that the STATE_RESET bit in the C0STR register is set to "1" (CAN module reset completed) after setting the RESET0 and RESET1 bits to "1".
3. The CANOUT pin outputs an "H" signal as soon as the RESET0 and RESET1 bits are set to "1". CAN bus error may occur when the RESET0 and RESET1 bits are set to "1" while the CAN frame is transmitting.
4. For CAN communication, set the PS1, PS2, PSL1, PSL2, PSC, and IPS registers when the STATE_RESET bit is set to "1" (CAN module reset completed).

22.1.1.2 LOOPBACK Bit

When the LOOPBACK bit is set to "1" (loopback function enabled) and the receive message slot has a matched ID and frame format with a transmitted frame, the transmitted frame is stored to the receive message slot.

NOTES:

1. No ACK for the transmitted frame is returned.
2. Change the LOOPBACK bit only when the STATE_RESET bit is set to "1" (CAN module reset completed).

22.1.1.3 BASICCAN Bit

When the BASICCAN bit is set to "1", the message slots 14 and 15 enter BasicCAN mode.

In BasicCAN mode, the message slots 14 and 15 are used as dual-structured buffers. The message slot 14 and 15 alternately store a received frame having matched ID detected by acceptance filtering. The ID in the message slot 14 and the C0LMAR0 to C0LMAR4 registers are used for acceptance filtering when the message slot 14 is active (the next received frame is to be stored in the message slot 14). The ID in the message slot 15 and the C0LMBR0 to C0LMBR4 registers are used when the message slot 15 is active. Both data frame and remote frame can be received.

When entering BasicCAN mode, set the same ID in two message slots and set the same values in the C0LMAR0 to C0LMAR4 registers and in the C0LMBR0 to C0LMBR4 registers.

Follow the procedure below to enter BasicCAN mode.

- (1) Set the BASICCAN bit to "1".
- (2) Set IDs in the message slots 14 and 15. Set the C0LMAR0 to C0LMAR4 registers and C0LMBR0 to C0LMBR4 registers. (Set to the same values.)
- (3) Set the IDE14 and 15 bits in the C0IDR register to select a frame format (standard or extended) for the message slots 14 and 15. (Set to the same format.)
- (4) Set the REMACTIVE bit in the C0MCTL14 and C0MCTL15 registers in the message slots 14 and 15 to "0" (data frame received) and the RECREQ bit to "1" (request to receive).

NOTES:

1. Change the BASICCAN bit only when the STATE_RESET bit is set to "1" (CAN module reset completed).
2. The message slot 14 is the first slot to become active after the RESET0 and RESET1 bits are set to "0".
3. The message slots 0 to 13 are not affected by entering BasicCAN mode.

22.1.1.4 TSPRE1, TSPRE0 Bits

The TSPRE1 and TSPRE0 bits determine which count source is used for the time stamp counter.

NOTES:

1. Change the TSPRE1 to TSPRE0 bits only when the STATE_RESET bit is set to "1" (CAN module reset completed).

22.1.1.5 TSRESET Bit

When the TSRESET bit is set to "1" (counter reset), the C0TSR register is set to "0000₁₆". The TSRESET bit is automatically set to "0" after the C0TSR register is set to "0000₁₆".

22.1.1.6 ECRESET Bit

When the ECRESET bit is set to "1", the C0TEC and C0REC registers are set to "00₁₆". The CAN module forcibly goes into an error active state.

The ECRESET bit is automatically set to "0" after the CAN module enters an error active state.

NOTES:

1. In an error active state, the CAN module is ready to communicate when 11 continuous recessive bits are detected on the CAN bus.

22.1.2 CAN0 Control Register 1 (C0CTRL1 Register)

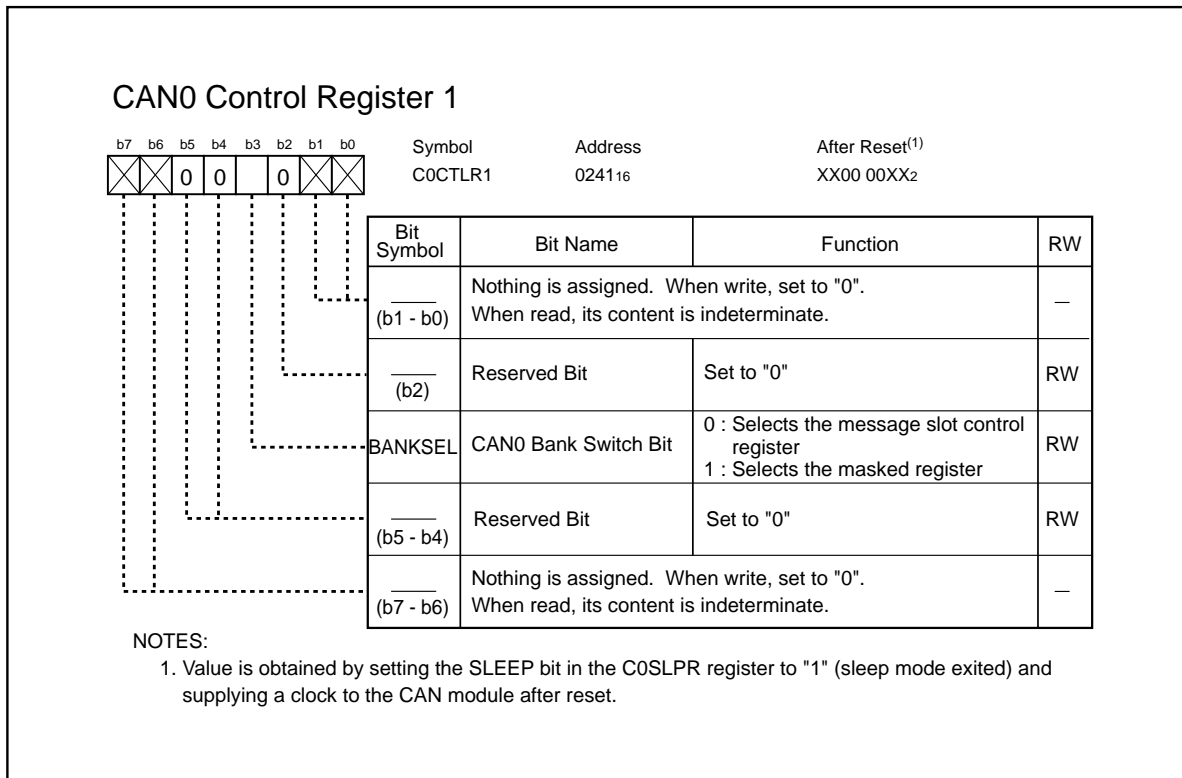


Figure 22.4 C0CTRL1 Register

22.1.2.1 BANKSEL Bit

The BANKSEL bit in the C0CTRL1 register selects the registers allocated to addresses 0220₁₆ to 023F₁₆.

The C0MCTL0 to C0MCTL15 registers can be accessed by setting the BANKSEL bit to "0". The C0GMR0 to C0GMR4 registers, C0LMAR0 to C0LMAR4 registers and C0LMBR0 to C0LMBR4 registers can be accessed by setting the BANKSEL bit to "1".

22.1.3 CAN0 Sleep Control Register (C0SLPR Register)

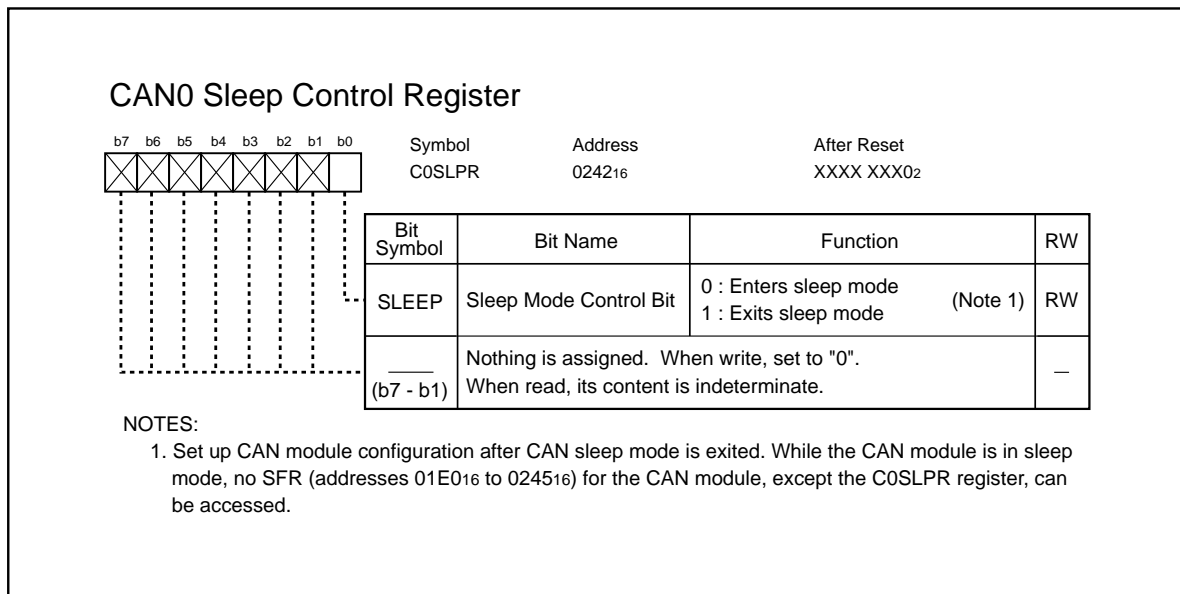


Figure 22.5 C0SLPR Register

22.1.3.1 SLEEP Bit

When the SLEEP bit is set to "0", the clock supplied to the CAN module stops running and enters sleep mode.

When the SLEEP bit is set to "1", the clock supplied to the CAN module starts running and exits sleep mode.

NOTES:

- Enter sleep mode after the STATE_RESET bit in the C0STR register is set to "1" (CAN module reset completed).

22.1.4 CAN0 Status Register (C0STR Register)

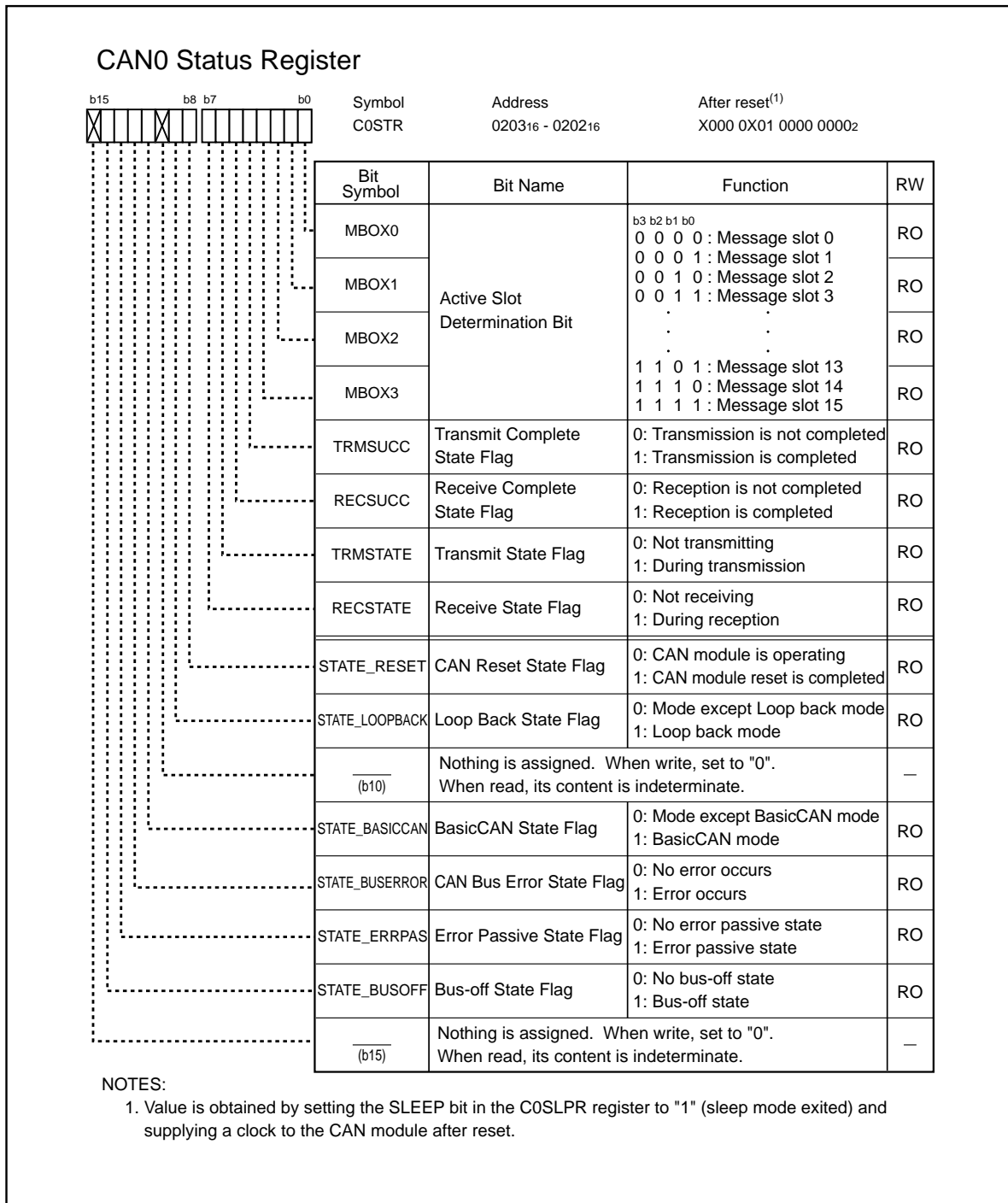


Figure 22.6 C0STR Register

22.1.4.1 MBOX3 to MBOX0 Bits

The MBOX3 to MBOX0 bits store relevant slot numbers when the CAN module has completed transmitting data or storing received data.

22.1.4.2 TRMSUCC Bit

The TRMSUCC bit is set to "1" when the CAN module has transmitted data as expected.

The TRMSUCC bit is set to "0" when the CAN module has received data as expected.

22.1.4.3 RECSUCC Bit

The RECSUCC bit is set to "1" when the CAN module has received data as expected. (Whether received message has been stored in the message slot or not is irrelevant.) If the received message is transmitted in loopback mode, the TRMSUCC bit is set to "1" and the RECSUCC bit is set to "0". The RECSUCC bit is set to "0" when the CAN module has transmitted data as expected.

22.1.4.4 TRMSTATE Bit

The TRMSTATE bit is set to "1" when the CAN module is performing as a transmit node. The TRMSTATE bit is set to "0" when the CAN module is in a bus-idle state or starts performing as a receive node.

22.1.4.5 RECSTATE Bit

The RECSTATE bit is set to "1" when the CAN module is performing as a receive node. The RECSTATE bit is set to "0" when the CAN module is in a bus-idle state or starts performing as a transmit node.

22.1.4.6 STATE_RESET Bit

After both RESET0 and RESET1 bits are set to "1" (CAN module reset), the STATE_RESET bit is set to "1" as soon as the CAN module is reset. The STATE_RESET bit is set to "0" when the RESET0 and RESET1 bits are set to "0".

22.1.4.7 STATE_LOOPBACK Bit

The STATE_LOOPBACK bit is set to "1" when the CAN module is in loopback mode. The STATE_LOOPBACK bit is set to "1" when the LOOPBACK bit in the C0CTRL0 register is set to "1" (loop back function enabled). The STATE_LOOPBACK bit is set to "0" when the LOOPBACK bit is set to "0" (loop back function disabled).

22.1.4.8 STATE_BASICCAN Bit

The STATE_BASICCAN bit is set to "1" when the CAN module is in BasicCAN mode. Refer to **22.1.1.3 BASICCAN Bit** for BasicCAN mode. The STATE_BASICCAN bit is set to "0" when the BASICCAN bit is set to "0" (BasicCAN mode function disabled). The STATE_BASICCAN bit is set to "1" when the BASICCAN bit is set to "1" (BasicCAN mode function enabled), the REMACTIVE bits in the COMCTL14 and COMCTL15 registers in the message slot 14 and 15 are set to "0" (data frame received) and the RECREQ bit is set to "1" (request to receive the frame).

22.1.4.9 STATE_BUSERROR Bit

The STATE_BUSERROR bit is set to "1" when an CAN communication error is detected. The STATE_BUSERROR bit is set to "0" when the CAN module has transmitted or received data as expected. Whether a received message has been stored into the message slot or not is irrelevant. NOTES:

1. When the STATE_BUSERROR bit is set to "1", the STATE_BUSERROR bit remains unchanged even if both RESET 0 and RESET1 bits are set to "1" (CAN module reset).

22.1.4.10 STATE_ERRPAS Bit

The STATE_ERRPAS bit is set to "1" when the value of the C0TEC or C0REC register exceeds 127 and places the CAN module in an error-passive state. The STATE_ERRPAS bit is set to "0" when the CAN module in an error passive state is placed in another error state. The STATE_ERRPAS bit is set to "0" when both RESET0 and RESET1 bits are set to "1" (CAN module is reset).

22.1.4.11 STATE_BUSOFF Bit

The STATE_BUSOFF bit is set to "1" when the value of the C0TEC register exceeds 255 and the CAN module in a bus-off state. The STATE_BUSOFF bit is set to "0" when the CAN module in a bus-off state is placed in an error-active state. The STATE_BUSOFF bit is set to "0" when both RESET0 and RESET1 bits are set to "1" (CAN module reset).

22.1.5 CAN0 Extended ID Register (C0IDR Register)

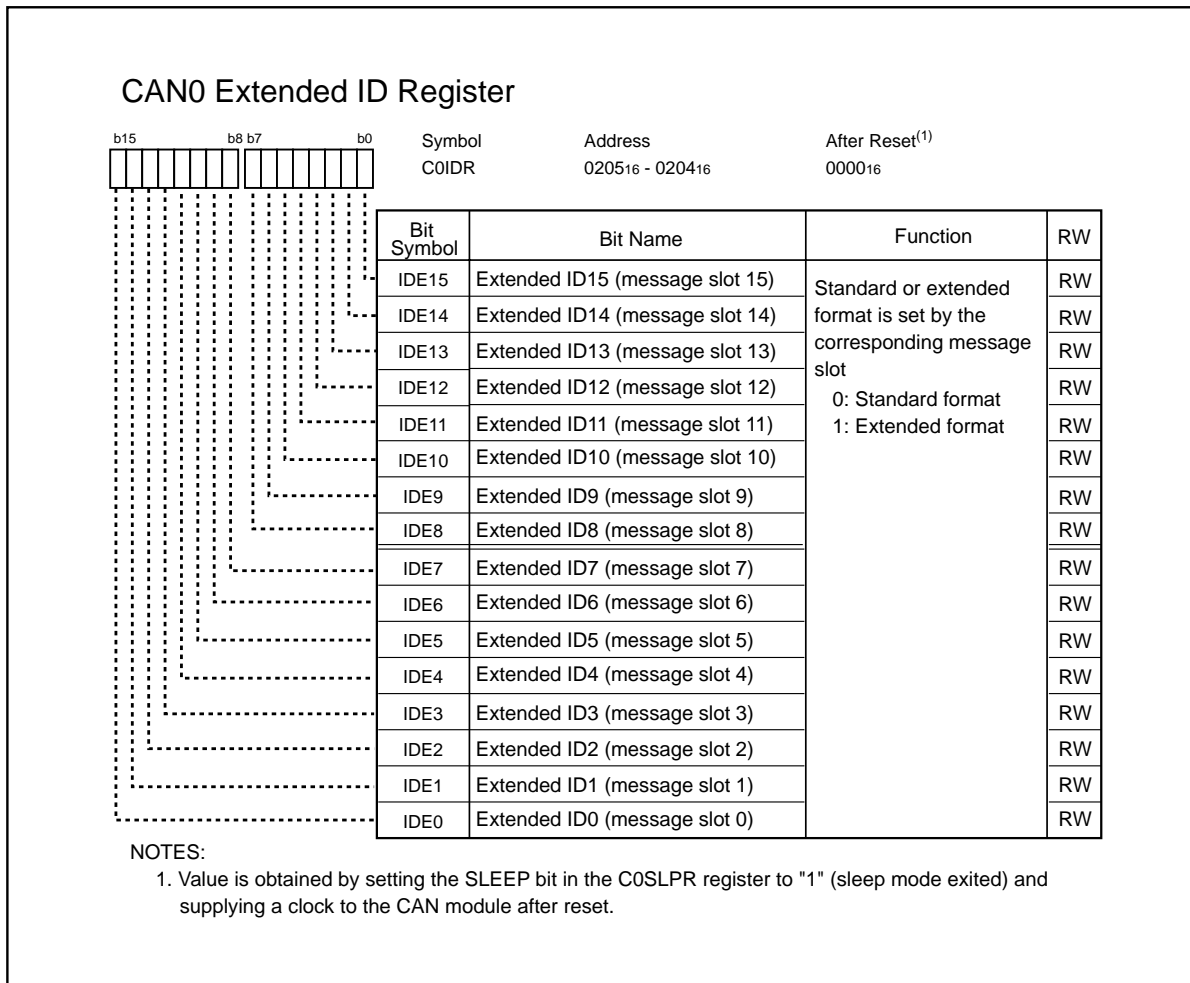


Figure 22.7 C0IDR Register

Bits in the C0IDR register determine the frame format in the message slot corresponding to each bit. The standard format is selected when the bit is set to "0". The extended format is selected when the bit is set to "1".

NOTES:

- Set each bit in the C0IDR register when neither transmit request nor receive request from the message slot is generated.

22.1.6 CAN0 Configuration Register (C0CONR Register)

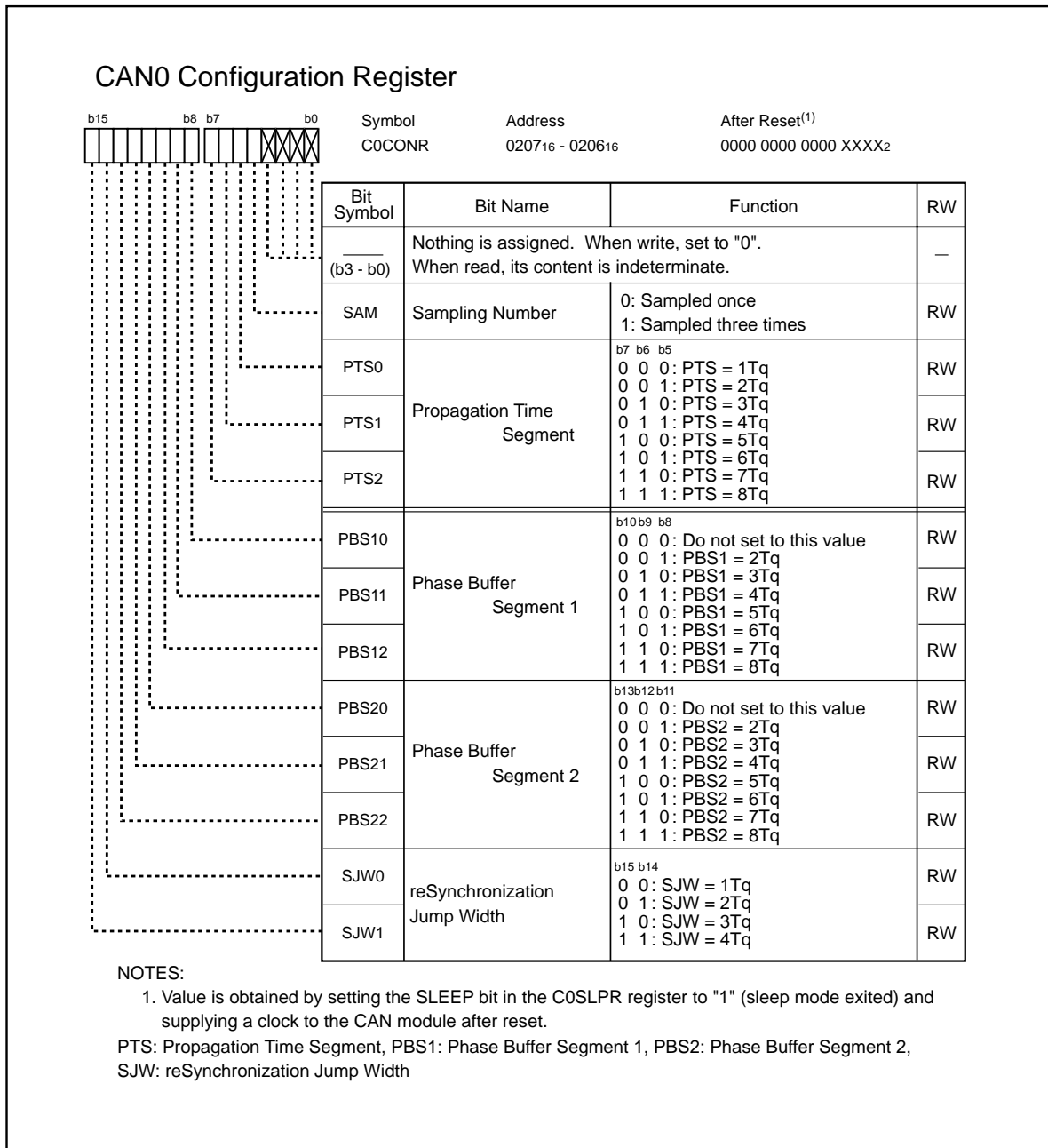


Figure 22.8 C0CONR Register

22.1.6.1 SAM Bit

The SAM bit determines the number of sample points to be taken per bit.

When the SAM bit is set to "0", only one sample is taken per bit at the end of the Phase Buffer Segment 1 (PBS1) to determine the value of the bit.

When the SAM bit is set to "1", three samples per bit are taken; one time quantum and two time quanta before the end of PBS1, and at the end of PBS1. The sample result value which is detected more than twice becomes the value of the bit sampled.

22.1.6.2 PTS2 to PTS0 Bits

The PTS2 to PTS0 bits determine PTS width.

22.1.6.3 PBS12 to PBS10 Bits

The PBS12 to PBS10 bits determine PBS1 width. Set the PBS12 to 10 bits to "0012" or more.

22.1.6.4 PBS22 to PBS20 Bits

The PBS22 to PBS20 bits determine PBS2 width. Set the PBS22 to PBS20 bits to "0012" or more.

22.1.6.5 SJW1 to SJW0 Bits

The SJW1 to SJW0 bits determine SJW width. Set the SJW1 to SJW0 bits to a value equal to or less than that of the PBS12 to PBS10 bits and PBS22 to PBS20 bits.

Table 22.3 Bit Timing when CPU Clock = 30 MHz

Baud Rate	BRP	Tq Clock Cycles (ns)	Tq Per Bit	PTS+PBS1	PBS2	Sample Point
1Mbps	1	66.7	15	12	2	87%
	1	66.7	15	11	3	80%
	1	66.7	15	10	4	73%
	2	100	10	7	2	80%
	2	100	10	6	3	70%
	2	100	10	5	4	60%
500Kbps	2	100	20	16	3	85%
	2	100	20	15	4	80%
	2	100	20	14	5	75%
	3	133.3	15	12	2	87%
	3	133.3	15	11	3	80%
	3	133.3	15	10	4	73%
	4	166.7	12	9	2	83%
	4	166.7	12	8	3	75%
	4	166.7	12	7	4	67%
	5	200	10	7	2	80%
	5	200	10	6	3	70%
	5	200	10	5	4	60%

22.1.7 CAN0 Time Stamp Register (C0TSR Register)

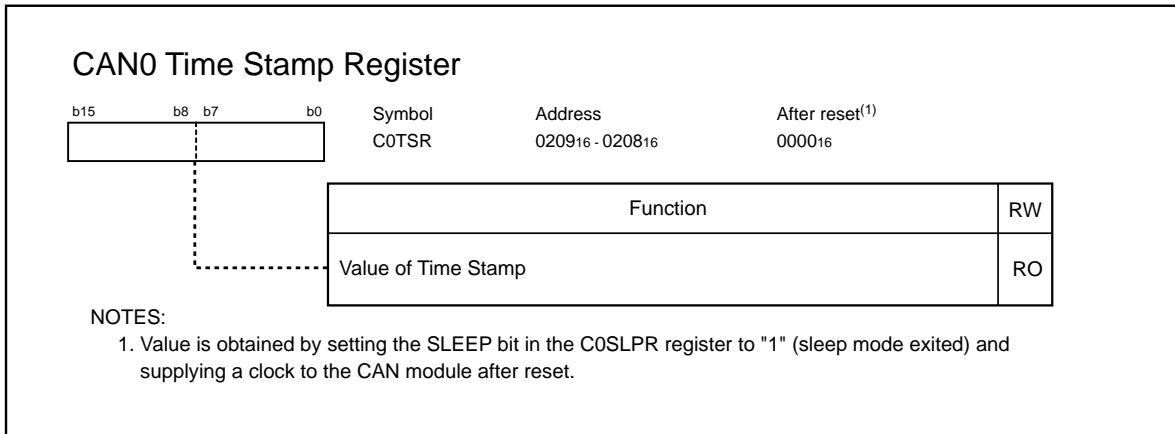


Figure 22.9 C0TSR Register

The C0TSR register is a 16-bit counter. The TSPRE0 and TSPRE1 bits in the C0CTRL0 register select the CAN bus bit clock divided by 1, 2, 3 or 4 as the count source for the C0TSR register. When data transmission or reception is completed, the value of the C0TSR register is automatically stored into the message slot.

The C0TSR register starts a counter increment when the RESET0 and RESET1 bits in the C0CTRL0 register are set to "0".

The C0TSR register is set to "0000₁₆":

- at the next count timing after the C0TSR register is set to "FFFF₁₆";
- when the RESET0 and RESET1 bits are set to "1" (CAN module reset) by program, or
- when the TSRESET bit is set to "1" (C0TSR register reset) by program.

In loopback mode, when either data frame receive message slot or remote frame receive message slot is available to store the message, the value of the C0TSR register is also stored into the message slot when data reception is completed. The value of the C0TSR register is not stored when data transmission is completed.

22.1.8 CAN0 Transmit Error Count Register (C0TEC Register)

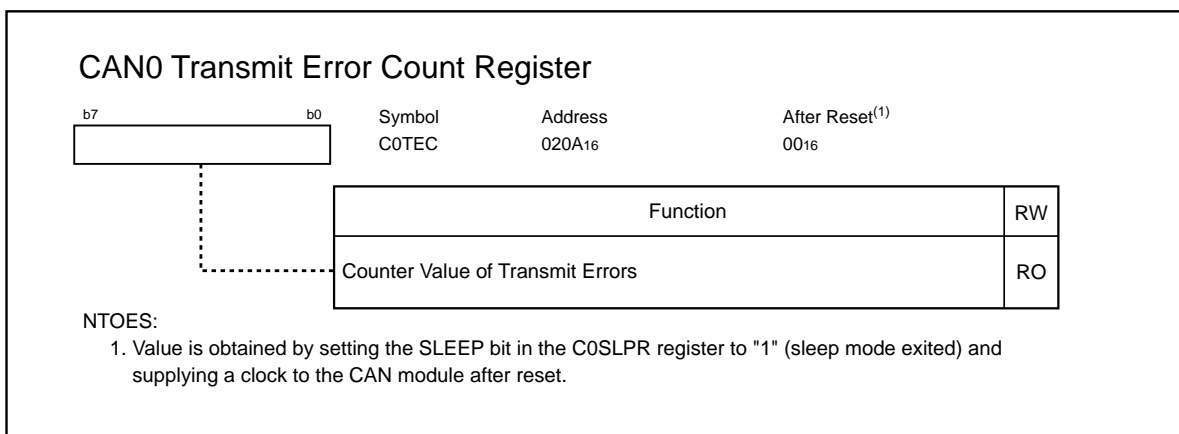


Figure 22.10 C0TEC Register

In an error active or an error passive state, the count value of a transmission error is stored into the C0TEC register. The counter is decremented when the CAN module has transmitted data as expected or is incremented when a transmit error occurs.

In a bus-off state, an indeterminate value is stored into the C0TEC register. The C0TEC register is set to "00₁₆" when the CAN module is placed in an error active state again.

22.1.9 CAN0 Receive Error Count Register (C0REC Register)

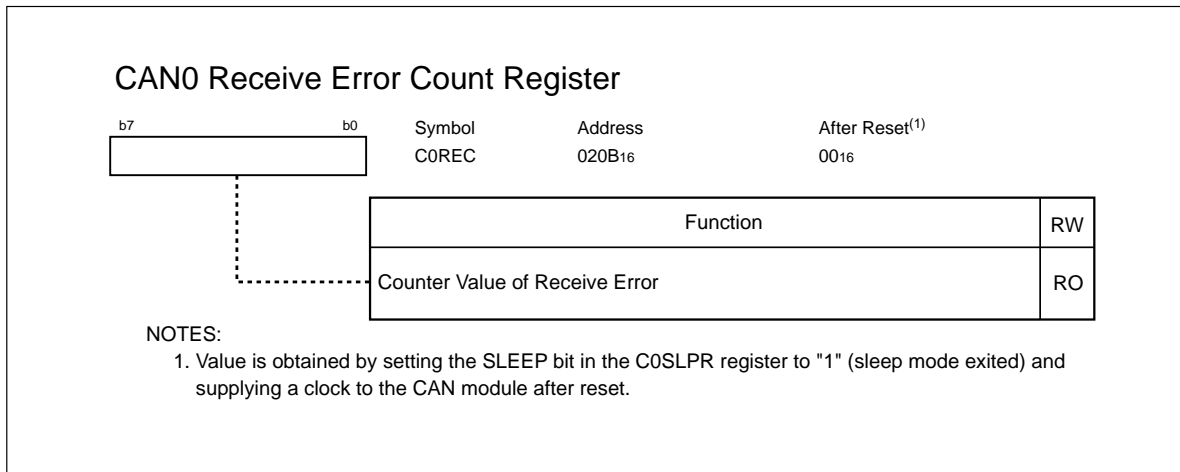


Figure 22.11 C0REC Register

In an error active or an error passive state, a count value of the reception error is stored into the C0REC register. The counter is decremented when the CAN module has received data as expected or is incremented when a receive error occurs.

The C0REC register is set to 127 when the C0REC register is 128 (error passive state) or more and the CAN module has received as expected.

In a bus-off state, an indeterminate value is stored into the C0REC register. The C0REC register is set to "00₁₆" when the CAN module is placed in an error active state again.

22.1.10 CAN0 Baud Rate Prescaler (C0BRP Register)

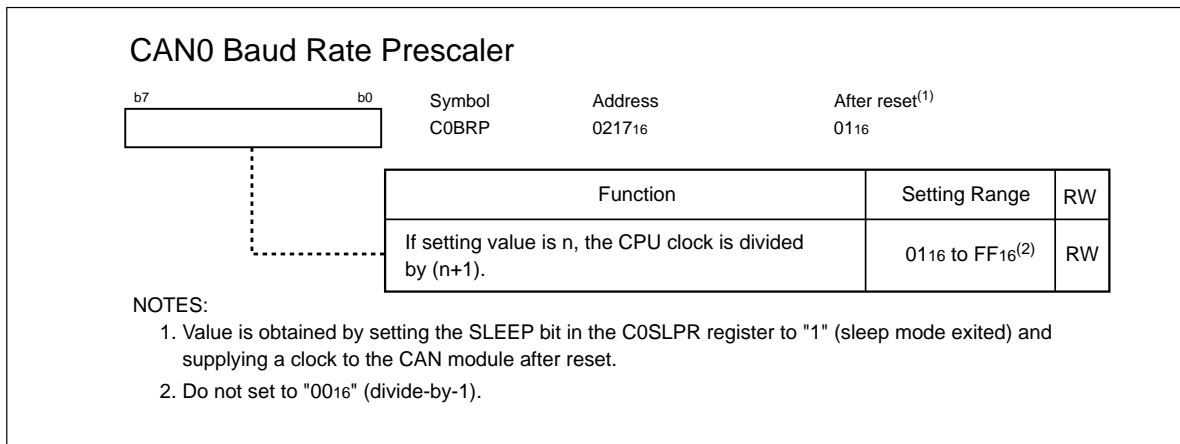


Figure 22.12 C0BRP Register

The C0BRP register determines the Tq clock cycle of the CAN bit timing. The baud rate is obtained from Tq clock cycle x Tq per bit.

$$Tq \text{ clock cycle} = (BRP+1) / f_1$$

$$\text{Baud rate} = \frac{1}{Tq \text{ clock cycle} \times Tq \text{ per bit}}$$

$$Tq \text{ per bit} = SS + PTS + PBS1 + PBS2$$

Tq: Time quantum

SS: Synchronization Segment; 1 Tq

PBS1: Phase Buffer Segment 1; 2 to 8 Tq

BRP: Setting value of the C0BRP register; 1-255

PTS: Propagation Time Segment; 1 to 8 Tq

PBS2: Phase Buffer Segment 2; 2 to 8 Tq

22.1.11 CAN0 Slot Interrupt Status Register (C0SISTR Register)

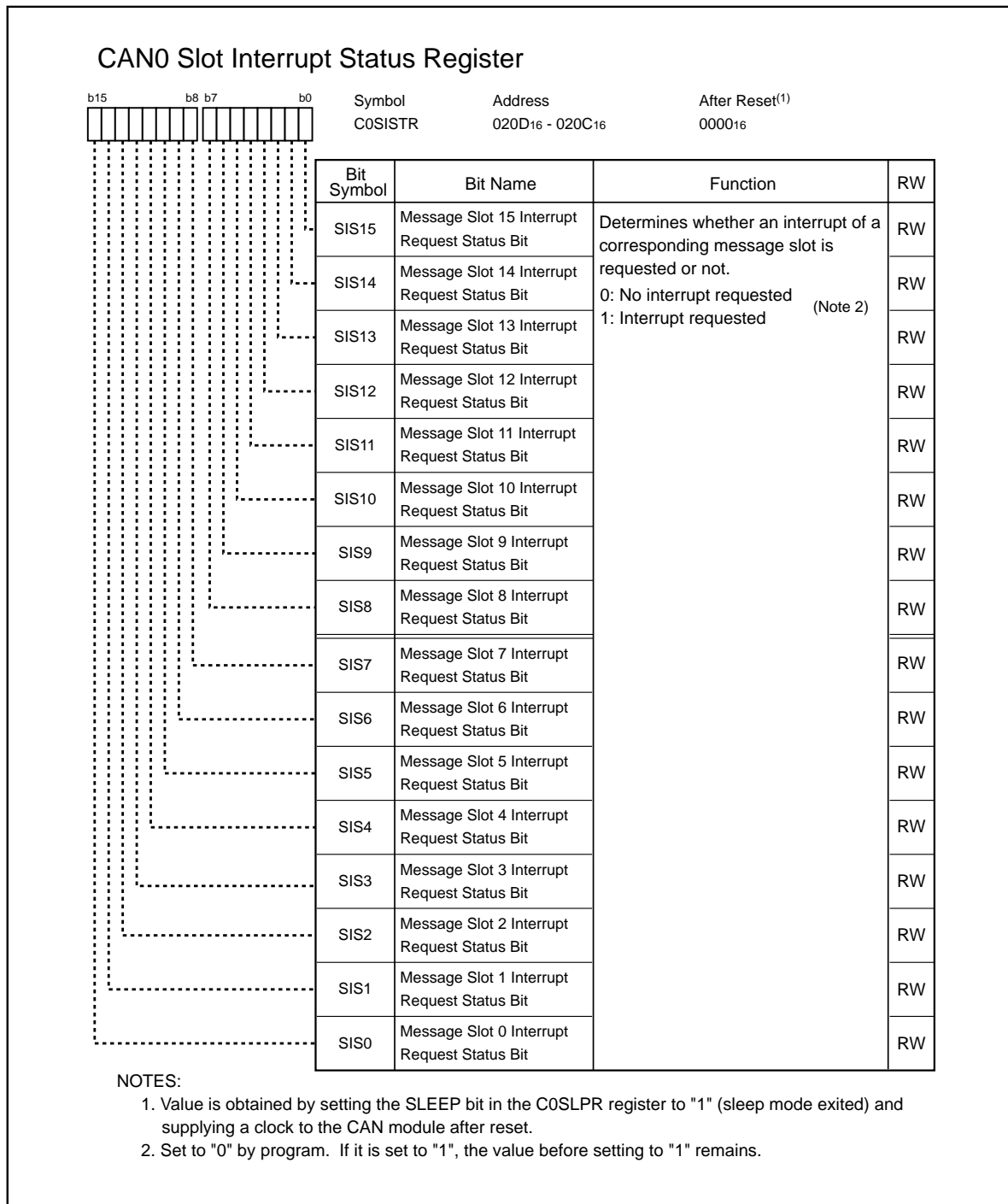


Figure 22.13 C0SISTR Register

When using the CAN interrupt, the C0SISTR register indicates which message slot is requesting an interrupt. The SISi bits (i=0 to 15) are not automatically set to "0" (no interrupt requested) when an interrupt is acknowledged. Set the SISj bits to "0" by program⁽¹⁾.

Refer to **22.3 CAN Interrupt** for details.

22.1.11.1 Message Slot for Transmission

The SISi bit is set to "1" (interrupt requested) when the C0TSR register is stored into the message slot i after data transmission is completed.

22.1.11.2 Message Slot for Reception

The SISi bit is set to "1" when the received message is stored in the message slot i after data reception is completed.

NOTES:

1. Use the MOV instruction, instead of the bit clear instruction, to set the SISi bit to "0". Bits in the C0SISTR register, which are not being changed to "0", must be to "1".

For example: To set the SIS0 bit to "0"

Assembly language: `mov.w #07FFFh, C0SISTR`

C language: `c0sistr = 0x7FFF;`

2. If the automatic answering function is enabled in the remote frame receive message slot, the SISi bit is set to "1" after the remote frame is received and after the data frame is transmitted.
3. In the remote frame transmit message slot, the SISi bit is set to "1" after the remote frame is transmitted and after the data frame is received.
4. The SISi bit is set to "1" if the SISi bit is set to "1" by an interrupt request and "0" by program simultaneously.

22.1.12 CAN0 Slot Interrupt Mask Register (C0SIMKR Register)

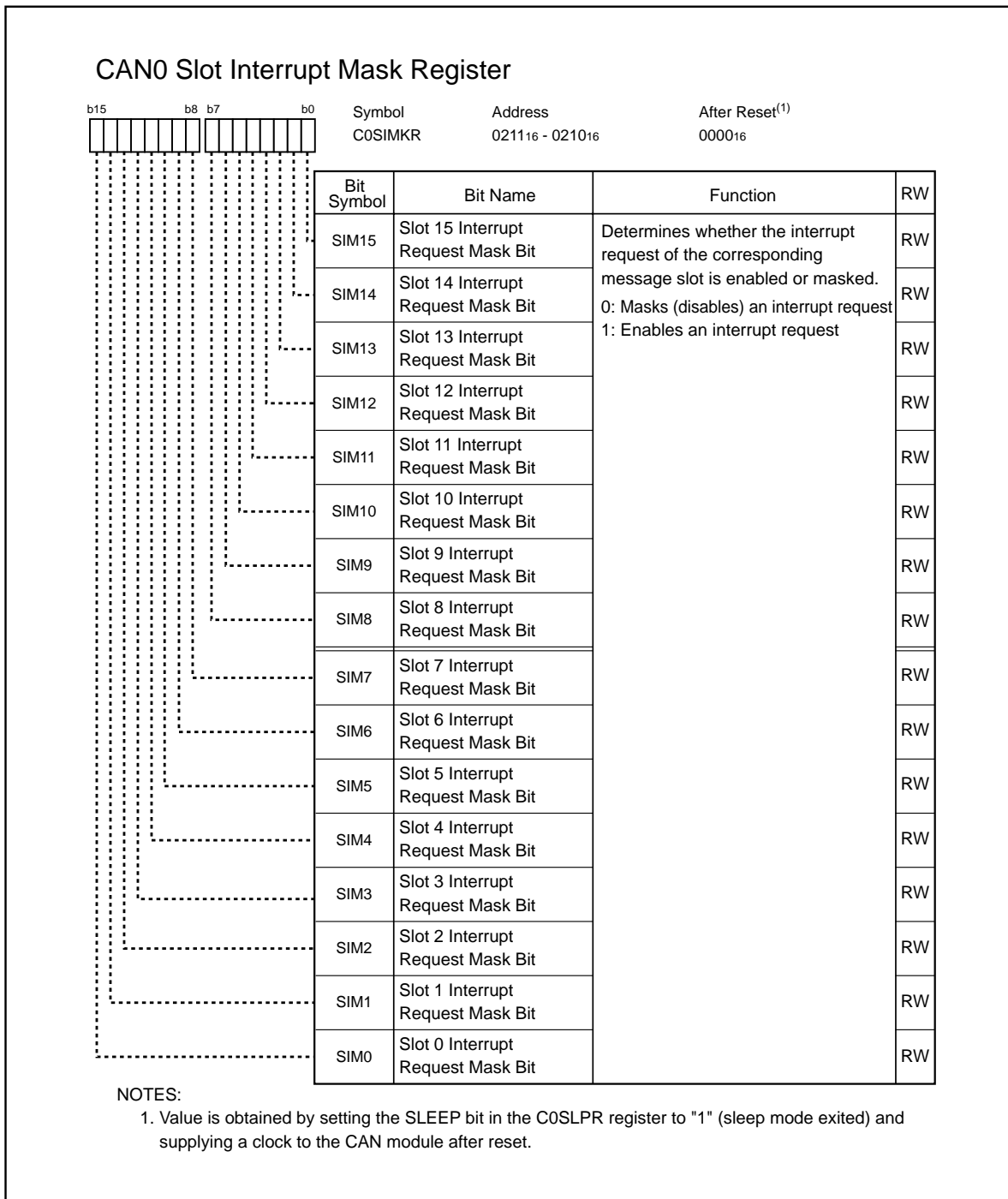


Figure 22.14 C0SIMKR Register

The CiSIMKR register determines whether an interrupt request that is generated by a data transmission or reception in the corresponding message slot is enabled or disabled. When the SIM_i bit (i=0 to 15) is set to "1", an interrupt request generated by a data transmission or reception in the corresponding message slot is enabled. Refer to **22.3 CAN Interrupt** for details.

22.1.13 CAN0 Error Interrupt Mask Register (C0EIMKR Register)

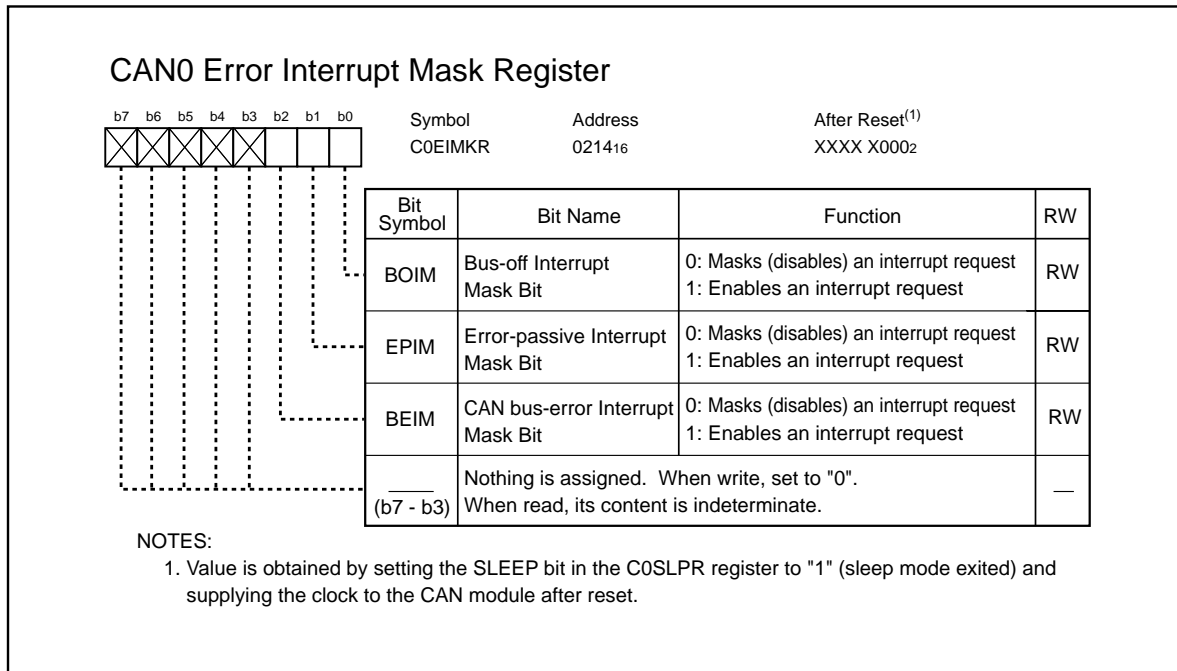


Figure 22.15 C0EIMKR Register

22.1.13.1 BOIM Bit

The BOIM bit determines whether an interrupt request is enabled or disabled when the CAN module is placed in a bus-off state. When the BOIM bit is set to "1", the bus-off interrupt request is enabled.

22.1.13.2 EPIM Bit

The EPIM bit determines whether an interrupt request is enabled or disabled when the CAN module is placed in an error passive state. When the EPIM bit is set to "1", the error passive interrupt request is enabled.

22.1.13.3 BEIM Bit

The BEIM bit determines whether an interrupt request is enabled or disabled when a CAN bus error occurs. When the BEIM bit is set to "1", the CAN bus error interrupt request is enabled.

Refer to **22.3 CAN Interrupt** for details.

22.1.14 CAN0 Error Interrupt Status Register (C0EISTR Register)

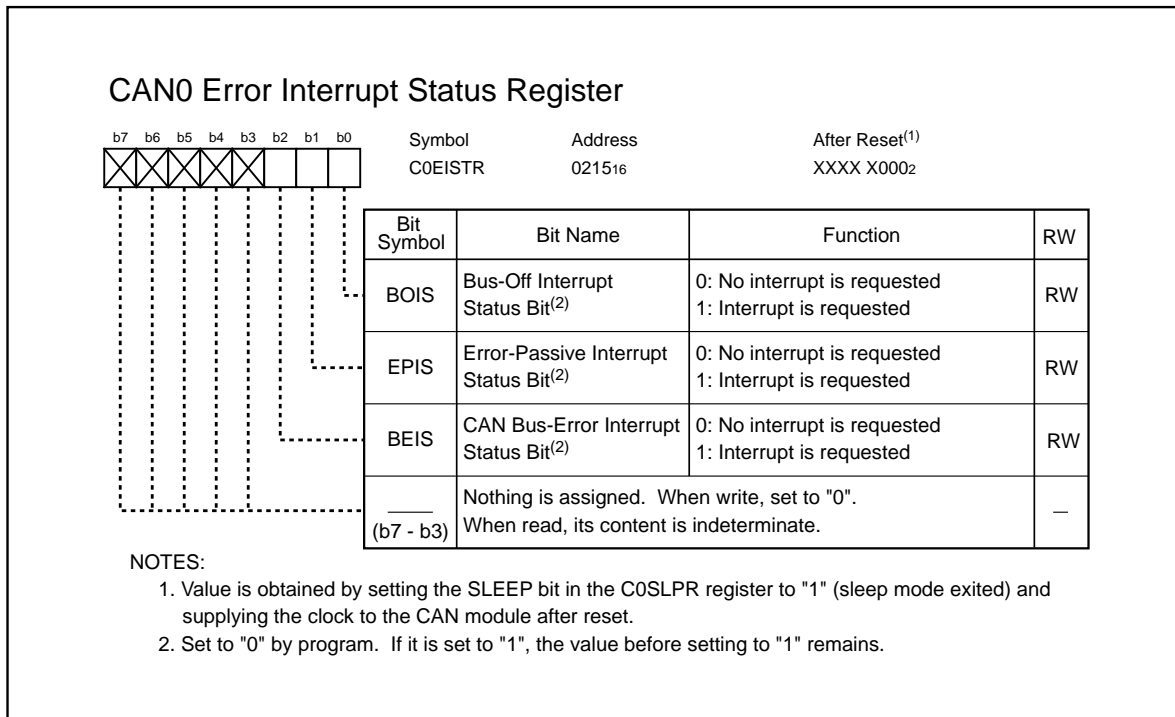


Figure 22.16 C0EISTR Register

When using the CAN interrupt, the C0EISTR register indicates the cause of the generated error interrupt. The BOIS, EPIS and BEIS bits are not automatically set to "0" (no interrupt requested) even if an interrupt is acknowledged. Set these bits to "0" by program⁽¹⁾.

Refer to **22.3 CAN Interrupt** for details.

22.1.14.1 BOIS Bit

The BOIS bit is set to "1" when the CAN module is placed in a bus-off state.

22.1.14.2 EPIS Bit

The EPIS bit is set to "1" when the CAN module is placed in an error passive state.

22.1.14.3 BEIS Bit

The BEIS bit is set to "1" when a CAN bus error is detected.

NOTES:

1. Use the MOV instruction, instead of the bit clear instruction, to set each bit in the CoEISTR register to "0". Bits not being changed to "0" must be set to "1".

For example: To set the BOIS bit to "0"

Assembly language: mov.b#006h, C0EISTR

C language: c0eistr = 0x06;

22.1.15 CAN0 Global Mask Register, CAN0 Local Mask Register A and CAN0 Local Mask Register B (COGMRj (j=0 to4), COLMARj and COLMBRj Registers)

The COGMRj, COLMARj and COLMBRj registers are used for acceptance filtering.

The COGMRj register determines whether the IDs in the message slots 0 to 13 are verified. The COLMARj register determines whether the ID in the message slot 14 is verified. The COLMBRj register determines whether the ID in the message slot 15 is verified.

- When bits in these registers are set to "0", each ID bit, standard ID 0 to 1 bit and extended ID0 to 2 bit in the CAN0 message slots i (i=0 to 15) corresponding to the bits in the above registers, is masked while acceptance filtering. (The corresponding bits are assumed to have matching IDs.)
- When bits in these registers are set to "1", corresponding ID bits are compared with received IDs while acceptance filtering. If the received ID matches the ID in the message slot i, the received data having the matching ID is stored into that message slot.

NOTES:

1. Change the COGMRj register only when the message slots 0 to 13 have no receive request.
2. Change the COLMARj register only when the message slot 14 has no receive request.
3. Change the COLMBRj register only when the message slot 15 has no receive request.

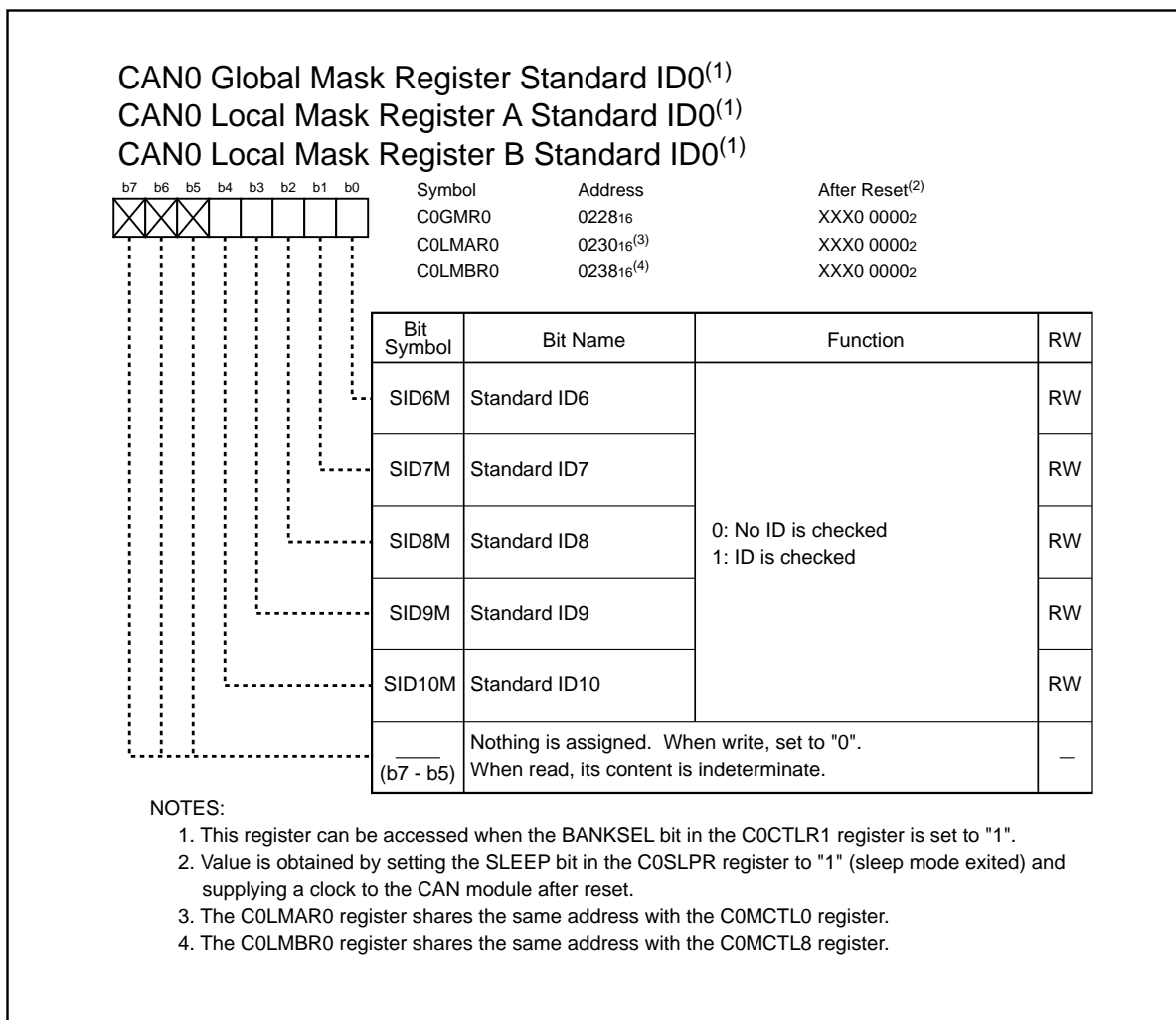


Figure 22.17 COGMR0, COLMAR0 and COLMBR0 Registers

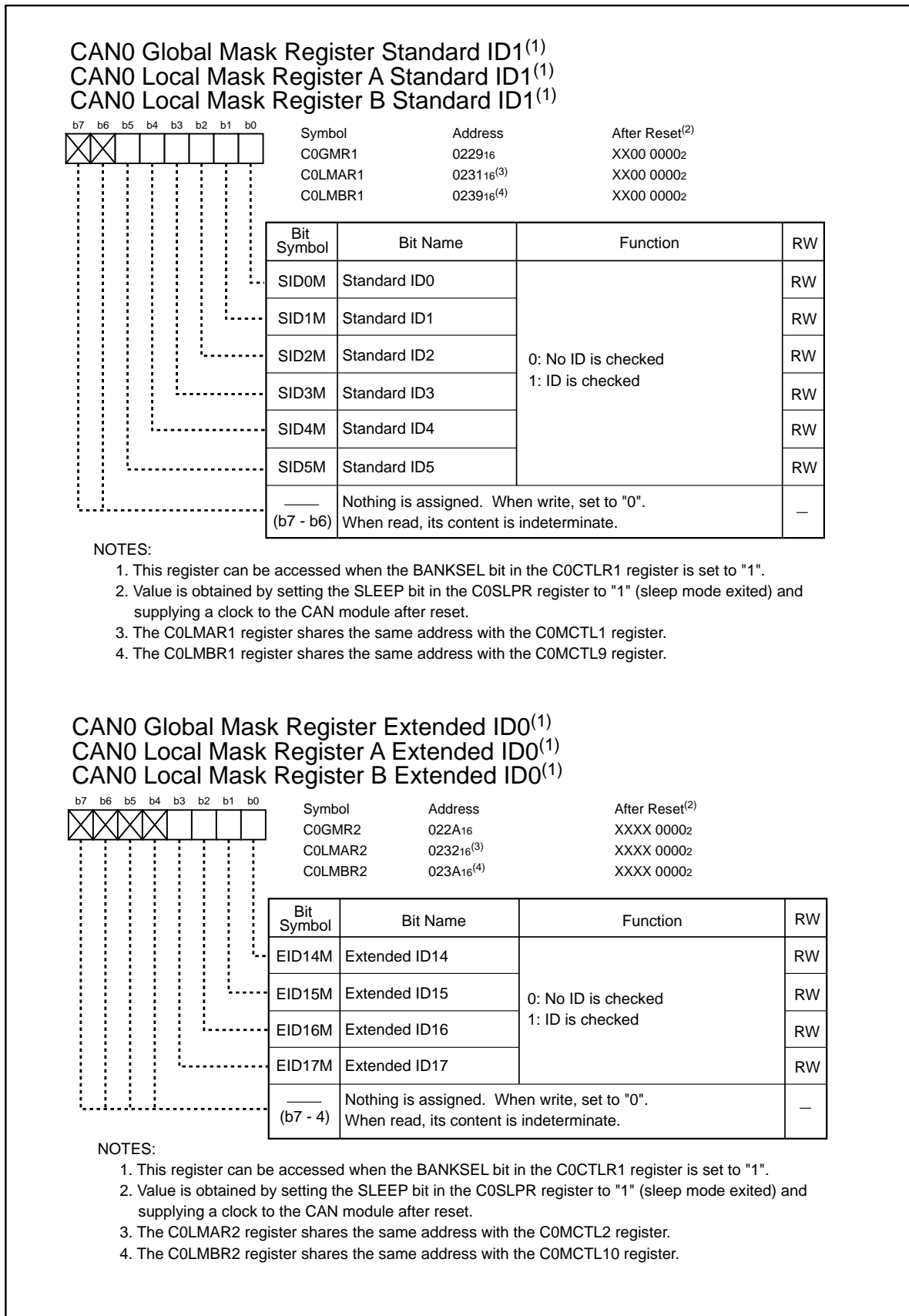


Figure 22.18 C0GMR1, C0LMAR1 and C0LMBR1 Registers and C0GMR2, C0LMAR2 and C0LMBR2 Registers

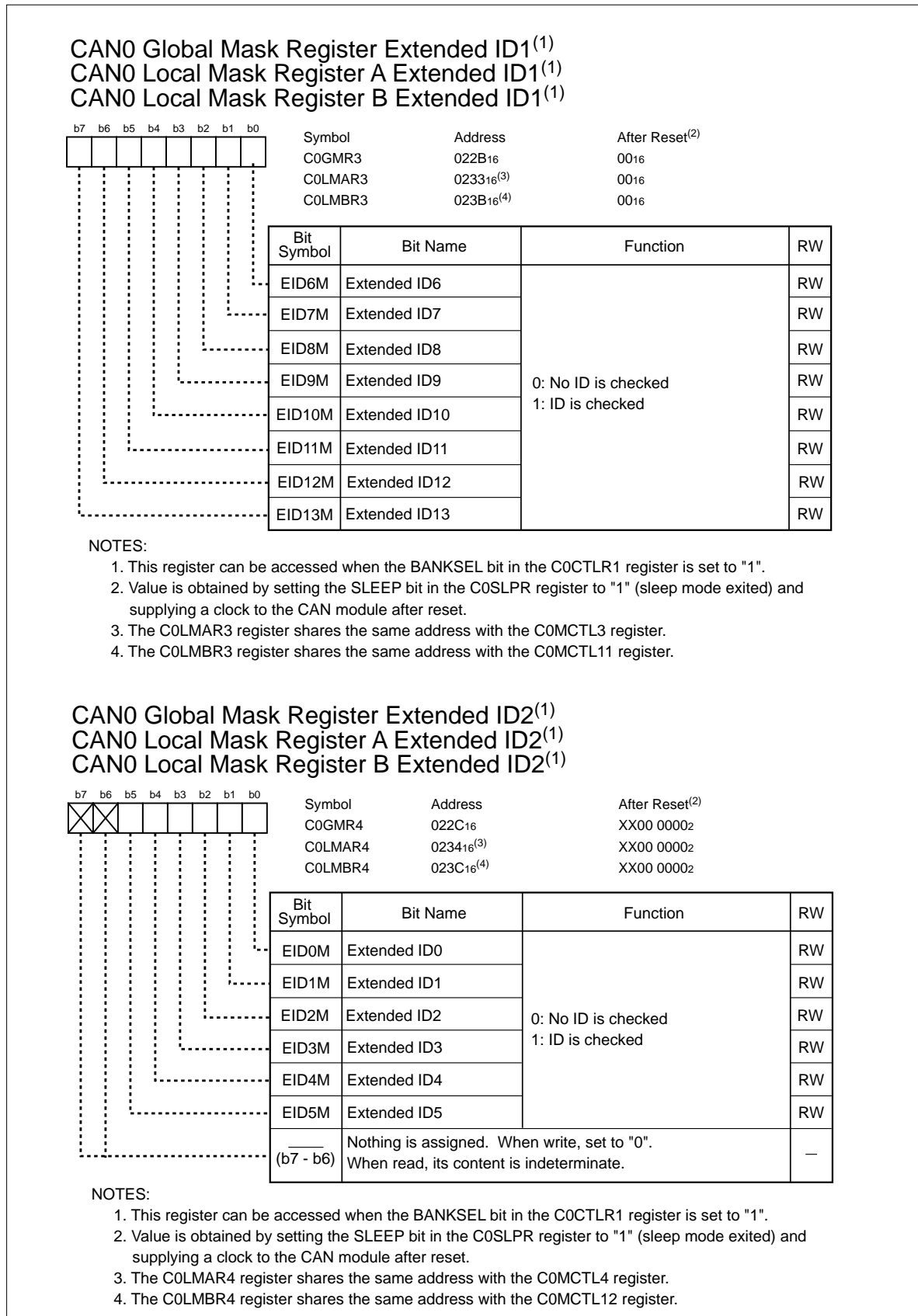


Figure 22.19 C0GMR3, C0LMAR3 and C0LMBR3 Registers and C0GMR4, C0LMAR4 and C0LMBR4 Registers

22.1.16 CAN0 Message Slot i Control Register (COMCTLi Register) (i=0 to 15)

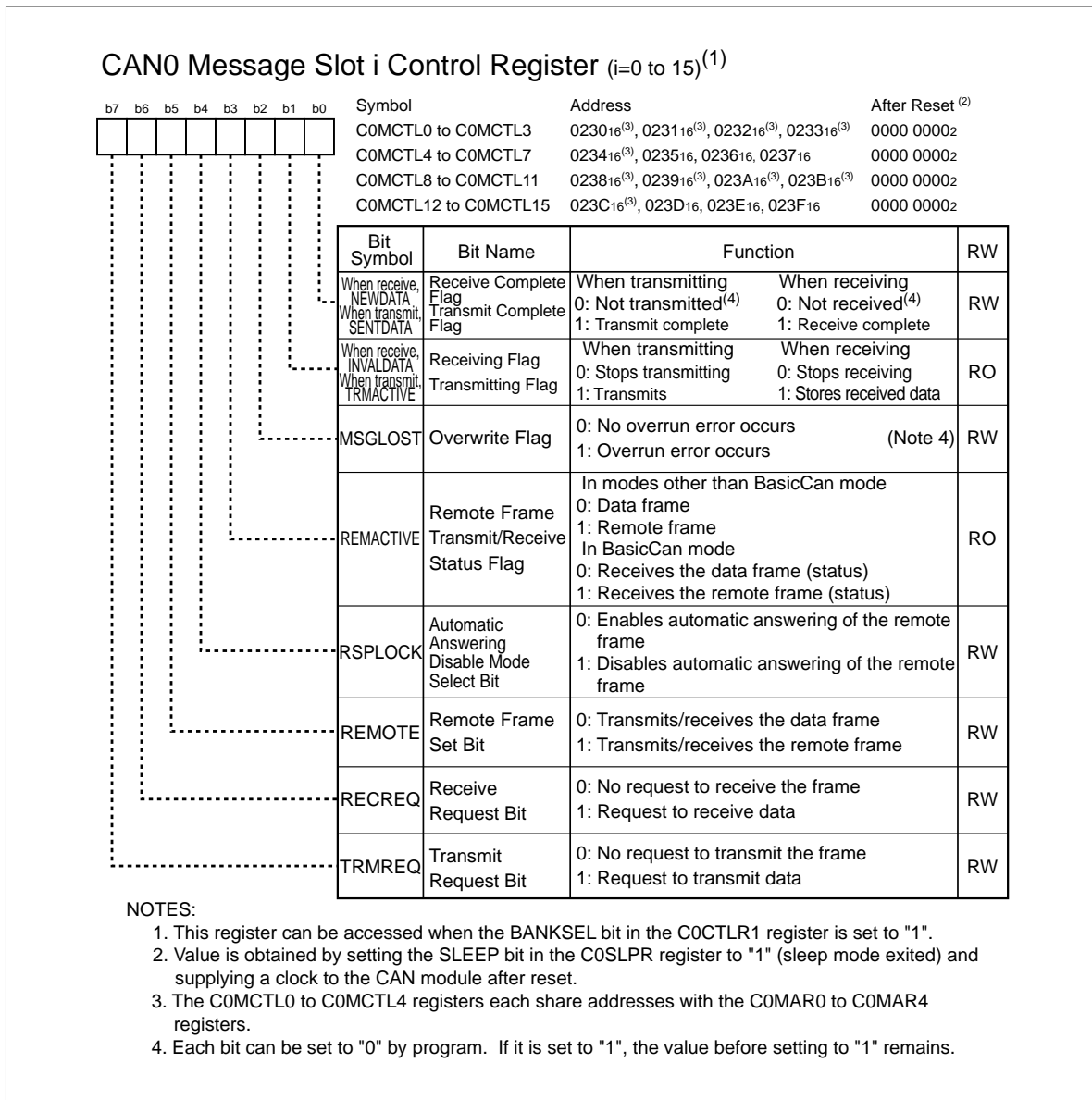


Figure 22.20 COMCTL0 to COMCTL15 Registers

Table 22.4 COMCTLi Register (i= 0 to 15) Settings and Transmit/Receive Mode

Settings for the COMCTLi Register								Transmit/Receive Mode
TRMREQ	RECREQ	REMOTE	RSPLOCK	REMACTIVE	MSGLOST	TRMACTIVE INVALIDDATA	SENTDATA NEWDATA	
0	0	0	0	0	0	0	0	No frame is transmitted or received
0	1	0	0	0	0	0	0	Data frame is received
0	1	1	1 or 0	0	0	0	0	Remote frame is received (The data frame is transmitted after receiving the remote frame.)
1	0	0	0	0	0	0	0	Data frame is transmitted
1	0	1	0	0	0	0	0	Remote frame is transmitted (The data frame is received after transmitting the remote frame)

22.1.16.1 SENTDATA/NEWDATA Bit

The SENTDATA/NEWDATA bit indicates that the CAN module has transmitted or received the CAN message. Set the SENTDATA/NEWDATA bit to "0" (not transmitted or not received) by program before data transmission and reception is started. The SENTDATA/NEWDATA bit is not set to "0" automatically. When the TRMACTIVE/INVALIDDATA bit is set to "1" (during transmission or storing received data), the SENTDATA/NEWDATA bit cannot be set to "0".

- SENTDATA : The SENTDATA bit is set to "1" (transmit complete) when a data transmission is completed in the transmit message slot.
- NEWDATA : The NEWDATA bit is set to "1" (receive complete) when the message to be stored into the message slot i ($i=0$ to 15) is received in the receive message slot as expected.

NOTES:

1. To read a received data from the message slot i , set the NEWDATA bit to "0" before reading. If the NEWDATA bit is set to "1" immediately after reading, this indicates that new received data has been stored into the message slot while reading and the data read contains an indeterminate value. In this case, discard the data with indeterminate value and then read the message slot again after the NEWDATA bit is set to "0".
2. When the remote frame is transmitted or received, the SENTDATA/NEWDATA bit remains unchanged after the remote frame transmission or reception is completed. The SENTDATA/NEWDATA bit is set to "1" when a subsequent data frame transmission or reception is completed.

22.1.16.2 TRMACTIVE/INVALIDDATA Bit

The TRMACTIVE/INVALIDDATA bit indicates that the CAN module is transmitting or receiving a message and accessing the message slot i . The TRMACTIVE/INVALIDDATA bit is set to "1" when the CAN module is accessing the message slot and to "0" when not accessing the message slot.

- TRMACTIVE : The TRMACTIVE bit is set to "1" (transmitting) when a data transmission is started in the message slot. The TRMACTIVE bit is set to "0" (stops transmitting) if the CAN module loses in bus arbitration and a CAN bus error occurs or when a data transmission is completed.
- INVALIDDATA : The INVALIDDATA bit is set to "1" (storing received data) when receiving a message and storing a received data into the message slot i . Data, if read from the message slot i while this bit is set to "1", is indeterminate.

22.1.16.3 MSGLOST Bit

The MSGLOST bit is valid only when the message slot is set for reception. The MSGLOST bit is set to "1" (overflow error occurred) when the message slot i is overwritten by a new received message while the NEWDATA bit set to "1" (already received).

The MSGLOST bit is not automatically set to "0". Set to "0" (no overflow error occurred) by program.

22.1.16.4 REMACTIVE Bit

The C0MCTL0 to C0MCTL15 registers all have the same function when the STATE_BASICCAN bit is set to "0" (other than BasicCAN mode).

The REMACTIVE bit is set to "1" (remote frame) when the message slot i is set to transmit or receive the remote frame. The REMACTIVE bit is set to "0" (data frame) after the remote frame has been transmitted or received.

The functions of the C0MCTL14 and C0MCTL15 registers change when the STATE_BASICCAN bit is set to "1" (BasicCAN mode). When the REMACTIVE bit is set to "0", this indicates that a message stored into the message slot is the data frame. When the REMACTIVE bit is set to "1", this indicates a message stored into the message slot is the remote frame.

22.1.16.5 RSPLOCK Bit

The RSPLOCK bit is valid only when remote frame reception shown in Table 22.4 is selected. The RSPLOCK bit determines whether the received remote frame is processed or not.

When the RSPLOCK bit is set to "0" (automatic answering of the remote frame enabled), the slot automatically changes to a transmit slot after the remote frame is received, and the message stored into the message slot is automatically transmitted as the data frame.

When the RSPLOCK bit is set to "1" (automatic answering of the remote frame disabled), message is not automatically transmitted upon receiving the remote frame.

Set the RSPLOCK bit to "0" to select any transmit/receive mode other than the remote frame reception.

22.1.16.6 REMOTE Bit

The REMOTE bit selects transmit/receive mode shown in Table 22.4. Set the REMOTE bit to "0" to transmit or receive data frame. Set to "1" to transmit or receive remote frame.

The followings occur during remote frame transmission or reception.

- Transmitting the remote frame

A message stored into the message slot i ($i=0$ to 15) is transmitted as the remote frame. After transmission, the slot automatically becomes ready to receive data frame.

If the data frame is received before the remote frame is transmitted, the data frame is stored into the message slot i . The remote frame is not transmitted.

- Receiving the remote frame

The message slot receives the remote frame. The RSPLOCK bit determines whether or not to process the received remote frame.

22.1.16.7 RECREQ Bit

The RECREQ bit selects transmit/receive mode shown in Table 22.4. Set the RECREQ bit to "1" (receive requested) when data frame or remote frame is received. Set the RECREQ bit to "0" (no receive requested) when data frame or remote frame is transmitted.

When a data frame is automatically transmitted after a remote frame is received, the RECREQ bit remains set to "1". Set the RECREQ bit to "0" to transmit a remote frame. After a remote frame is transmitted, a data frame is automatically received while the RECREQ bit remains set to "0".

When setting the TRMREQ bit to "1" (transmit requested), do not set the RECREQ bit to "1" (receive requested).

22.1.16.8 TRMREQ Bit

The TRMREQ bit selects transmit/receive mode shown in Table 22.4. Set the TRMREQ bit to "1" (transmit requested) when data frame or remote frame is transmitted.

Set the TRMREQ bit to "0" (no request to transmit the frame) when data frame or remote frame is received.

When the data frame is automatically received after the remote frame is transmitted, the TRMREQ bit remains set to "1". Set the TRMREQ bit to "0" to receive the remote frame. After the remote frame is received, data frame is automatically transmitted while the TRMREQ bit remains set to "0".

If the RECREQ bit is set to "1" (request to receive the frame), do not set the TRMREQ bit to "1" (request to transmit the frame).

22.1.17 CAN0 Slot Buffer Select Register (C0SBS Register)

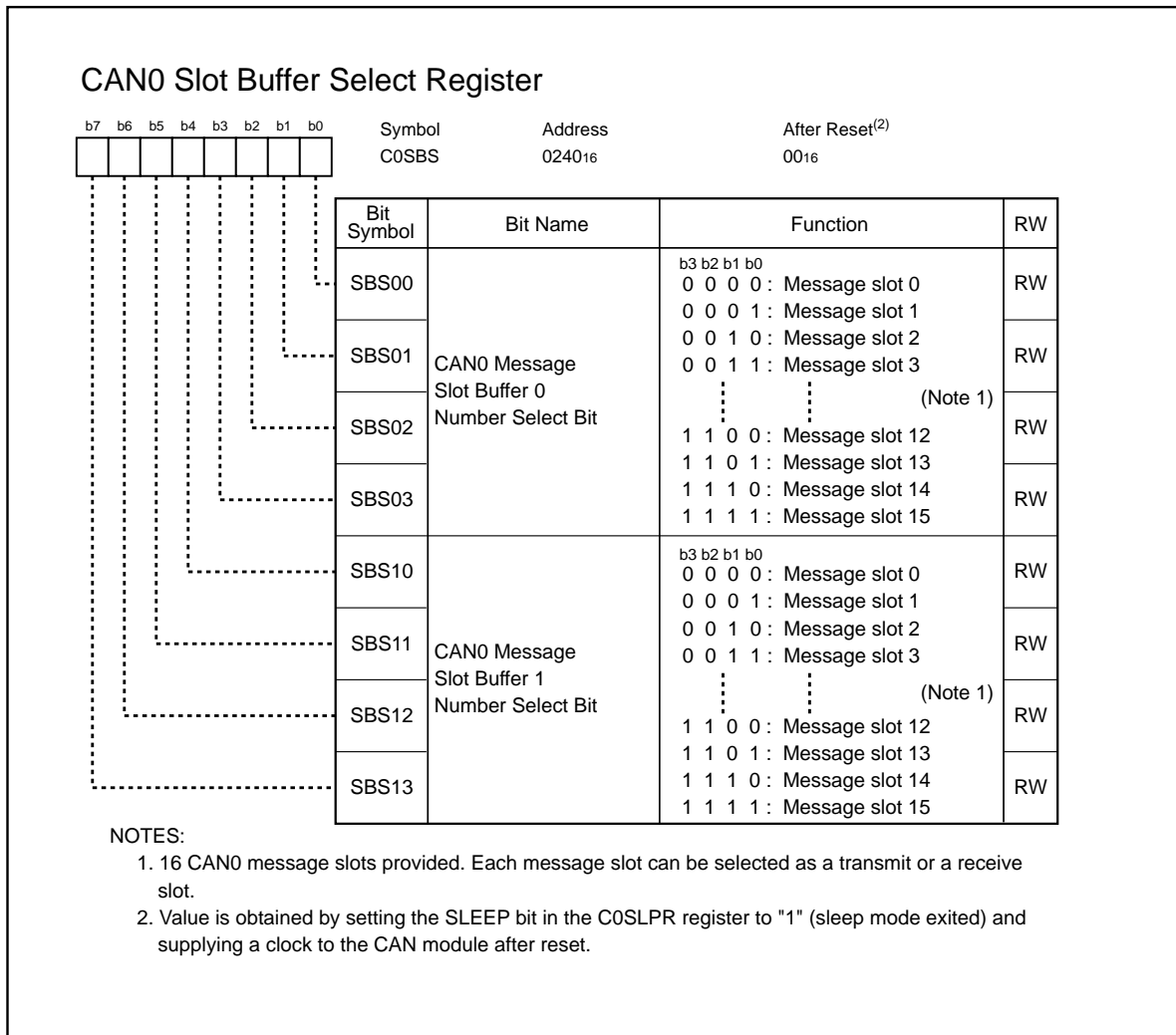


Figure 22.21 C0SBS Register

22.1.17.1 SBS03 to SBS00 Bits

If the SBS03 to SBS00 bits select a number i ($i=0$ to 15), the message slot i is allocated to the CAN0 message slot buffer 0. The message slot i can be accessed via addresses 01E0₁₆ to 01EF₁₆.

22.1.17.2 SBS13 to SBS10 Bits

If the SBS13 to SBS10 bits select a number i , the message slot i is allocated to the CAN0 message slot buffer 1. The message slot i can be accessed via addresses 01F0₁₆ to 01FF₁₆.

22.1.18 Message Slot Buffer

The message slot, selected by setting the C0SBS register, is read by reading the message slot buffer. A message can be written in the message slot selected by the C0SBS register if the message is written to the message slot buffer.

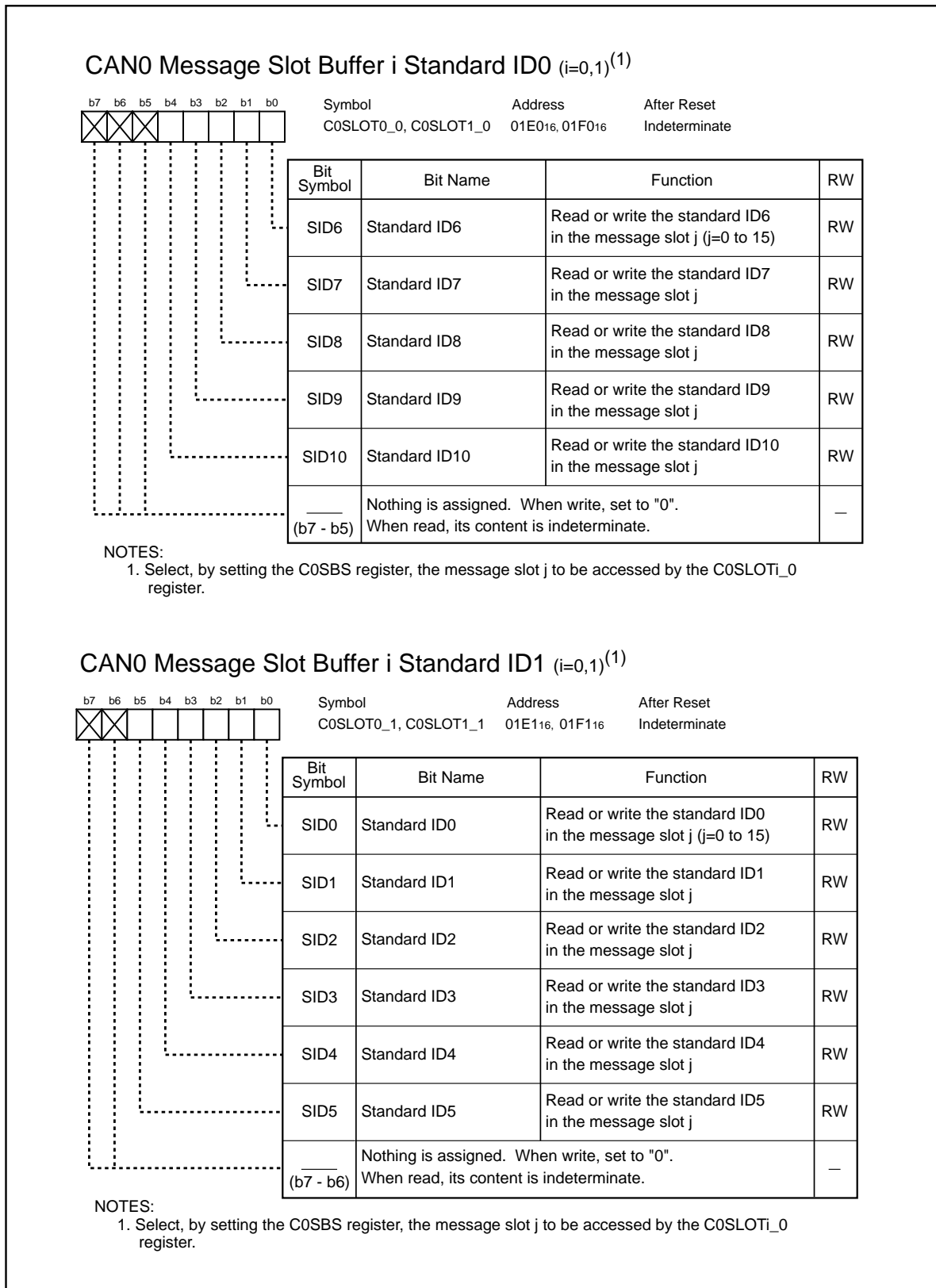


Figure 22.22 C0SLOT0_0, C0SLOT1_0 Registers and C0SLOT0_1, C0SLOT1_1 Registers

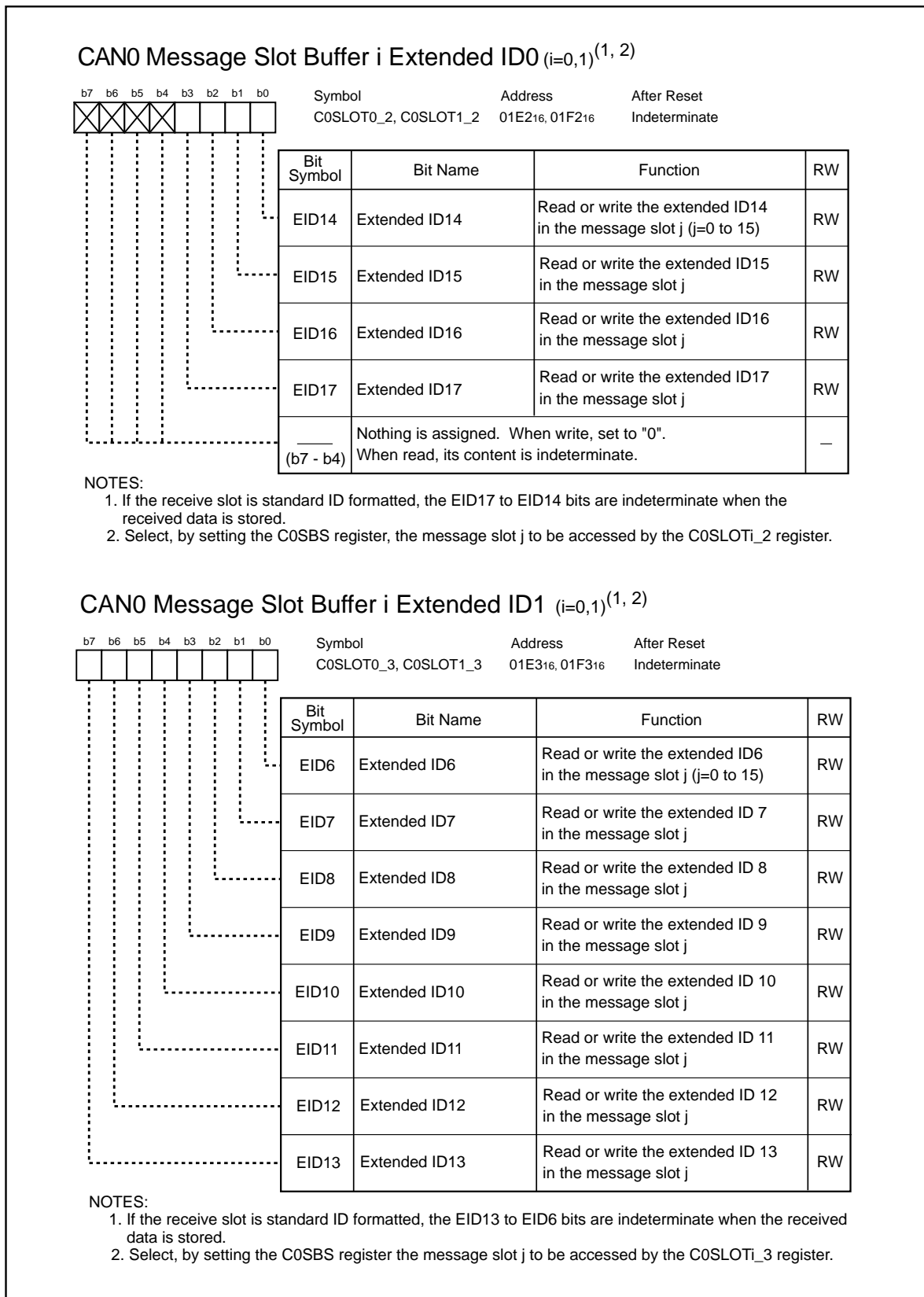


Figure 22.23 C0SLOT0_2, C0SLOT1_2 Registers and C0SLOT0_3, C0SLOT1_3 Registers

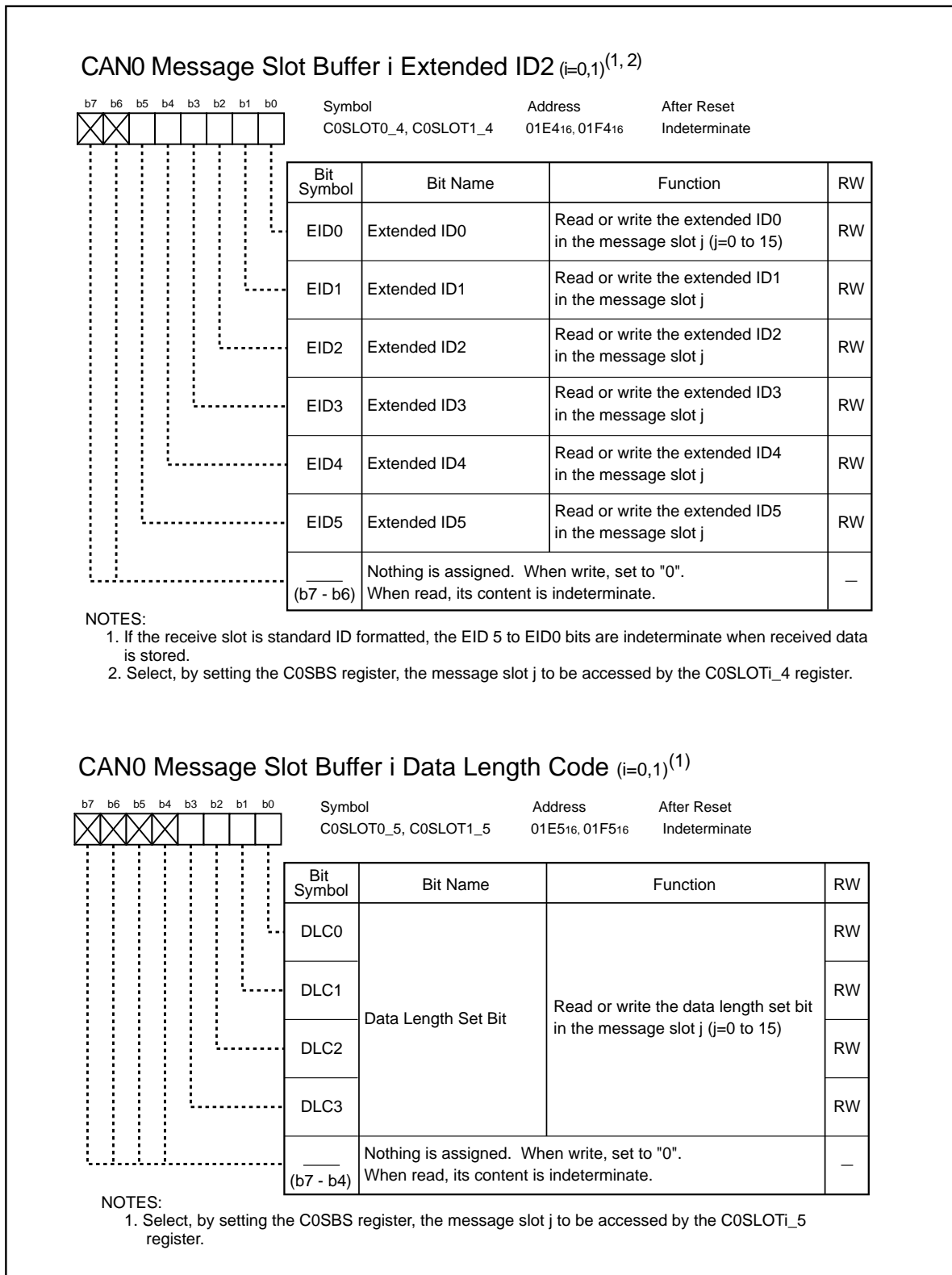


Figure 22.24 C0SLOT0_4, C0SLOT1_4 Registers and C0SLOT0_5 and C0SLOT1_5 Registers

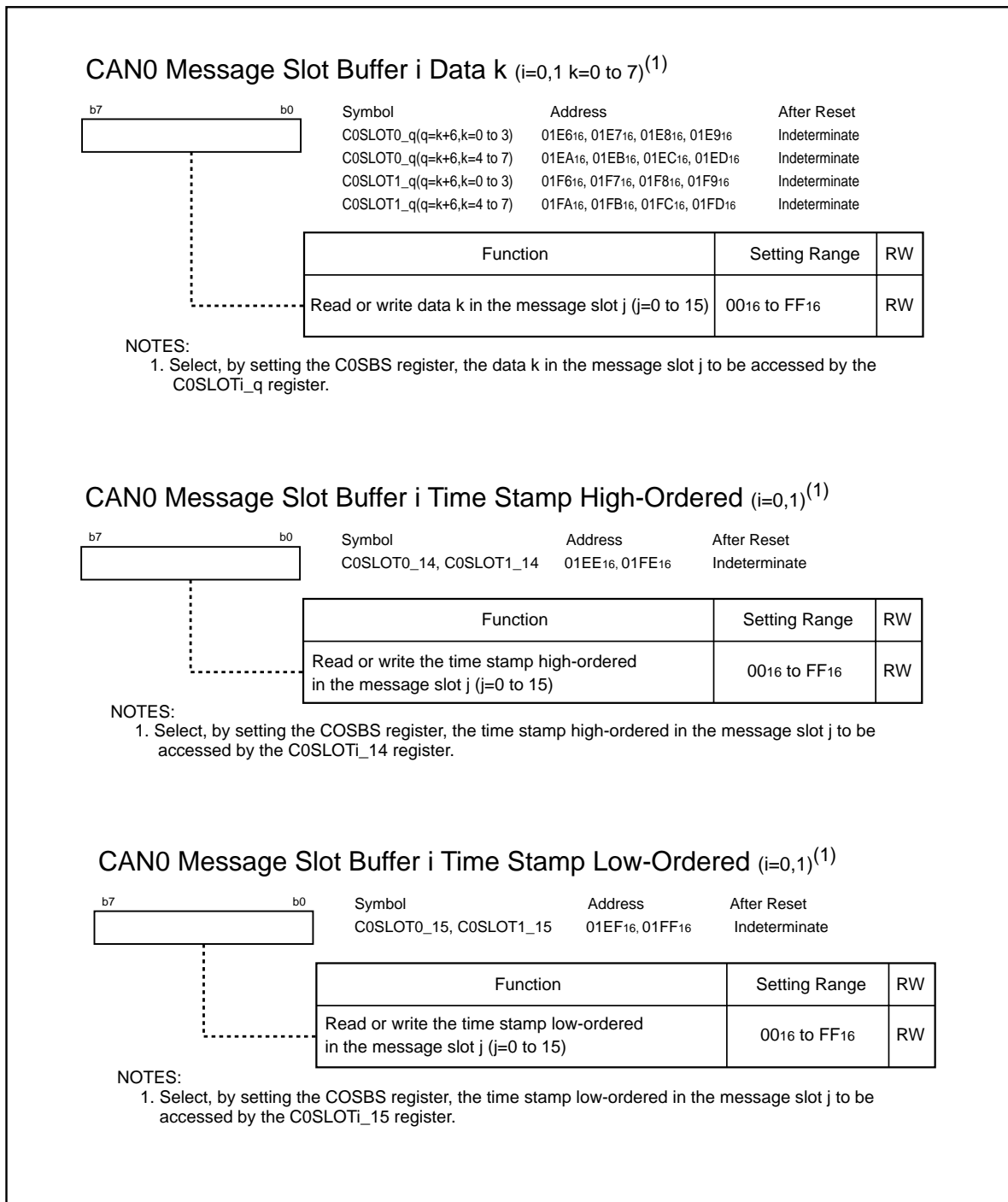


Figure 22.25 COSLOT0_6 to COSLOT0_13, COSLOT1_6 to COSLOT1_13, COSLOT0_14, COSLOT1_14, COSLOT0_15 and COSLOT1_15 Registers

22.2 Timing with CAN-Associated Registers

22.2.1 CAN Module Reset Timing

Figure 22.27 shows an operation example of when the CAN module is reset.

- (1) The CAN module can be reset when the STATE_RESET bit in the C0STR register is set to "1" (CAN module reset completed) after the RESET0 and RESET1 bits in the C0CTRL0 register are set to "1" (CAN module reset).
- (2) Set necessary CAN-associated registers.
- (3) CAN communication can be established after the STATE_RESET bit is set to "0" (resetting) after the RESET0 and RESET1 bits are set to "0" (CAN module reset exited).

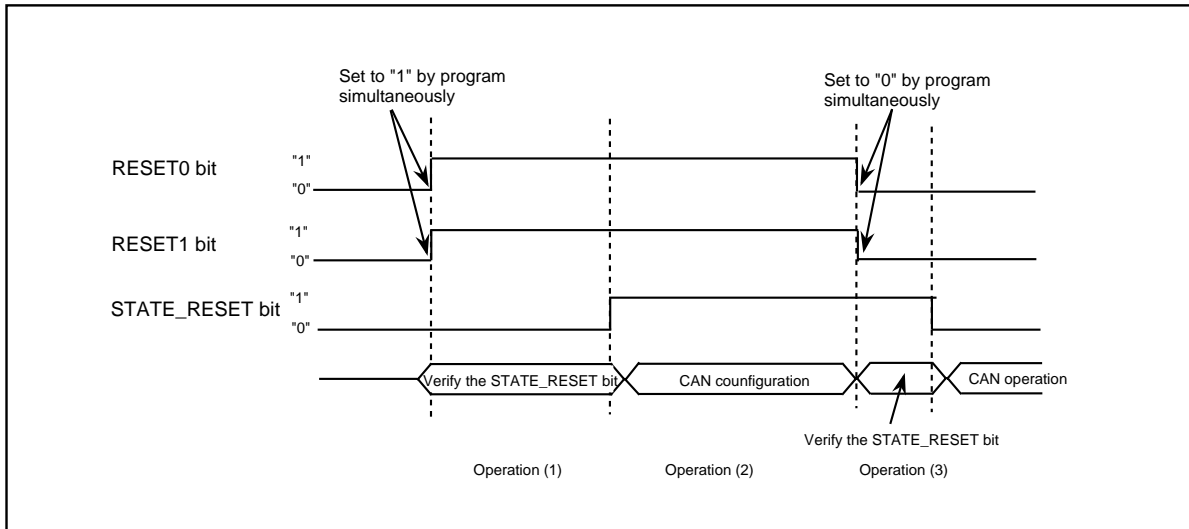


Figure 22.27 Example of CAN Module Reset Operation

22.2.2 CAN Transmit Timing

Figure 22.28 shows an operation example of when the CAN transmits a frame.

- (1) When the TRMREQ bit is set to "1" (request to transmit the data frame) while the CAN bus is in an idle state, the TRMACTIVE bit in the C0MCTLi register (i=0 to 15) is set to "1" (during transmission) and the TRMSTATE bit in the C0STR register is set to "1" (during transmission). The CAN starts transmitting the frame.
- (2) After a CAN frame transmission is completed, the SENTDATA bit in the C0MCTLi register is set to "1" (already transmitted), the TRMSUCC bit in the C0STR register to "1" (transmission completed) and the SISI bit in the C0SISTR register to "1" (interrupt requested). The MBOX3 to MBOX0 bits in the C0STR register store transmitted message slot numbers.

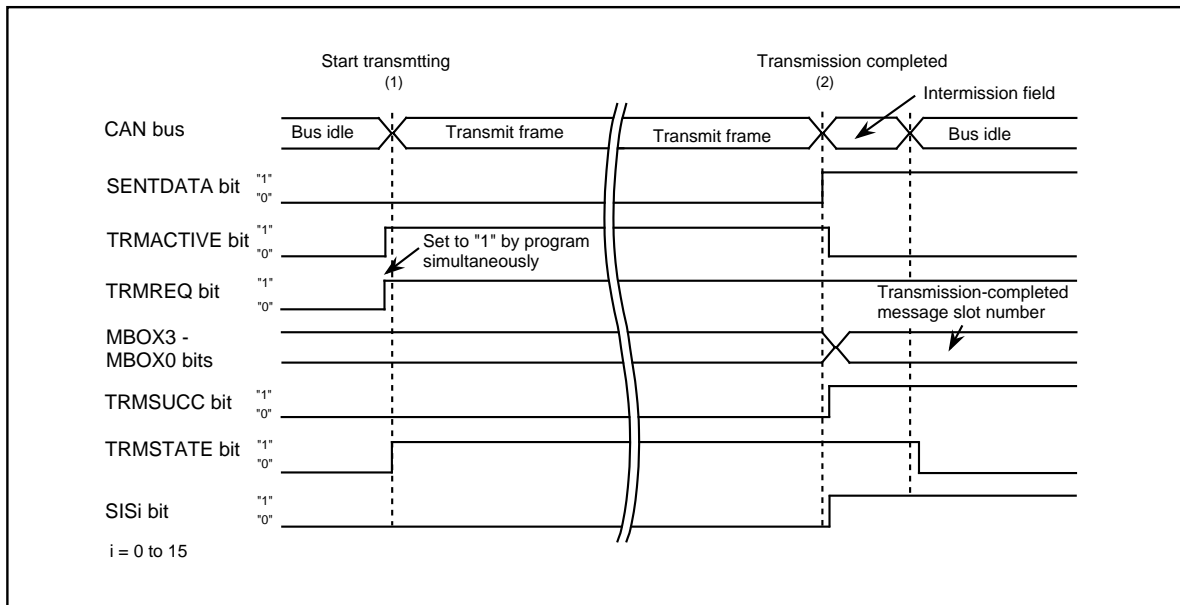


Figure 22.28 Example of CAN Data Frame Transmit Operation

22.2.3 CAN Receive Timing

Figure 22.29 shows an operation example of when the CAN receives a frame.

- (1) When the RECREQ bit in the C0MCTLi register ($i=0$ to 15) is set to "1" (receive requested), the CAN is ready to receive the frame at anytime.
- (2) When the CAN starts receiving the frame, the RECSTATE bit in the C0STR register is set to "1" (during reception).
- (3) After the CAN frame reception is completed, the INVALIDTA bit in the C0MCTLi register is set to "1" (storing received data), the NEWDATA bit in the C0MCTLi register is set to "1" (receive complete) and the RECSUCC bit in the C0STR register is set to "1" (reception completed).
- (4) After data is written to the message slot, the INVALIDDATA bit is set to "0" (stops receiving) and the SISI bit is set to "1" (interrupt requested). The MBOX3 to MBOX0 bits store received message slot numbers.

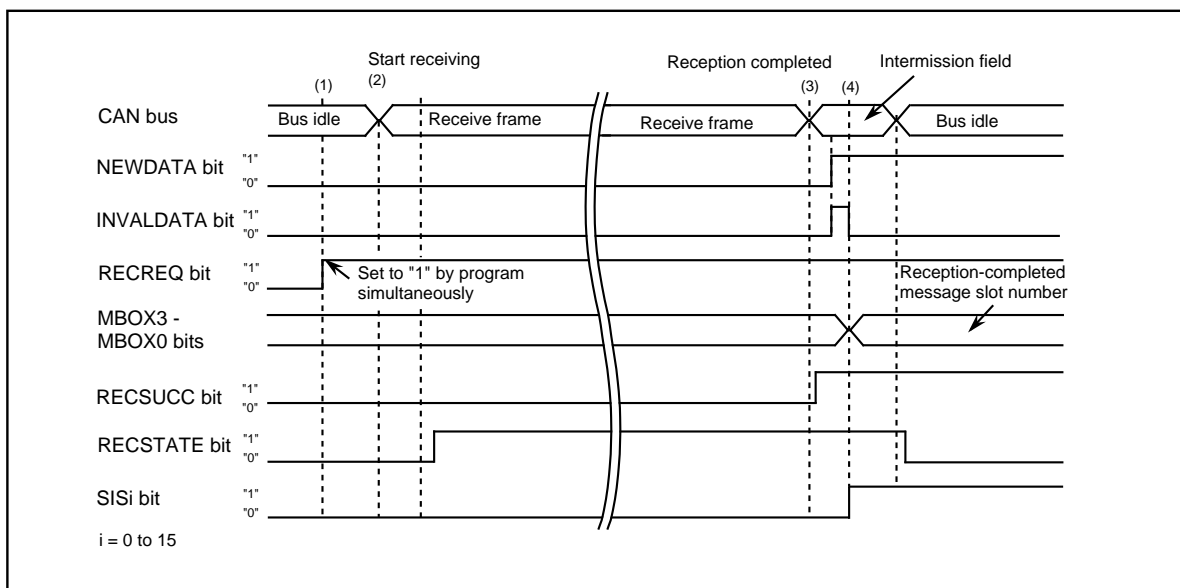


Figure 22.29 Example of CAN Data Frame Receive Operation

22.2.4 CAN Bus Error Timing

Figure 22.30 shows an operation example of when a CAN bus error occurs.

- (1) When a CAN bus error is detected, the STATE_BUSERROR bit in the CiSTR register is set to "1", (error occurred) and the BEIS bit in the CiEISTR register is set to "1" (interrupt requested). The CAN starts transmitting the error frame.

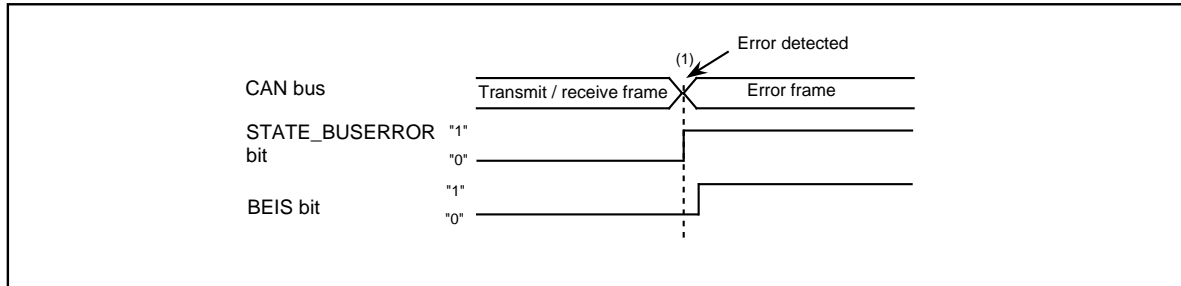


Figure 22.30 Operation Timing when CAN Bus Error Occurs

22.3 CAN Interrupts

The CAN_j interrupt (j=0 to 2) is provided as the CAN interrupt. Figure 22.31 shows a block diagram of the CAN interrupt.

The following factors cause the CAN-associated interrupt request to be generated.

- The CAN₀ slot i (i=0 to 15) completes a transmission
- The CAN₀ slot i completes a reception
- The CAN₀ module detects a bus error
- The CAN₀ module moves into an error-passive state
- The CAN₀ module moves into a bus-off state

The CAN_j interrupt, caused by one of the CAN_i interrupt request factors listed above, is generated via the OR circuit.

If an interrupt request factor is established, the corresponding bit in the C0SISTR register is set to "1" (interrupt requested) when the CAN₀ slot k completes a transmission or a reception. The corresponding bit in the C0EISTR register is set to "1" (interrupt requested) when the CAN_i module detects a bus error, moves into an error-passive state, or moves into a bus-off state.

The CAN₀ interrupt request signal is set to "1" when the corresponding bit in the C0SISTR or C0EISTR is set to "1" and the corresponding bit in the C0SIMKR or C0EIMKR is set to "1".

When the CAN₀ interrupt request signal changes from "0" to "1", all CAN_jR bits in the IIO9IR to IIO11IR registers are set to "1" (interrupt requested).

If at least one of the CAN_jE bits in the IIO9IE to IIO11IE registers is set to "1" (interrupt enabled), the IR bits in the corresponding CAN_jIC registers are set to "1" (interrupt requested). The CAN₀ interrupt request signal remains set to "1" if another interrupt request causes a corresponding bit in the C0SISTR or C0EISTR to be set to "1" and the corresponding bit in the C0SIMKR or C0EIMKR to be set to "1" after the CAN₀ interrupt request signal changes "0" to "1". The CAN_jR and IR bits also remain unchanged. Bits in the C0SISTR or C0EISTR register and CAN_jR bits (j=0 to 2) in the IIO9IR to IIO11IR registers are not set to "0" automatically, interrupt acknowledgment notwithstanding. Set these bits to "0" by program.

The CAN_i interrupts are acknowledged when the CAN_jR bit in the IIO9IR to IIO11IR register and the corresponding bit in the C0SISTR or C0EISTR register, which are set to enable interrupts though setting the C0SIMKR or C0EIMKR register, are set to "0". If these bits remain set to "1", all CAN-associated interrupt request factors become invalid.

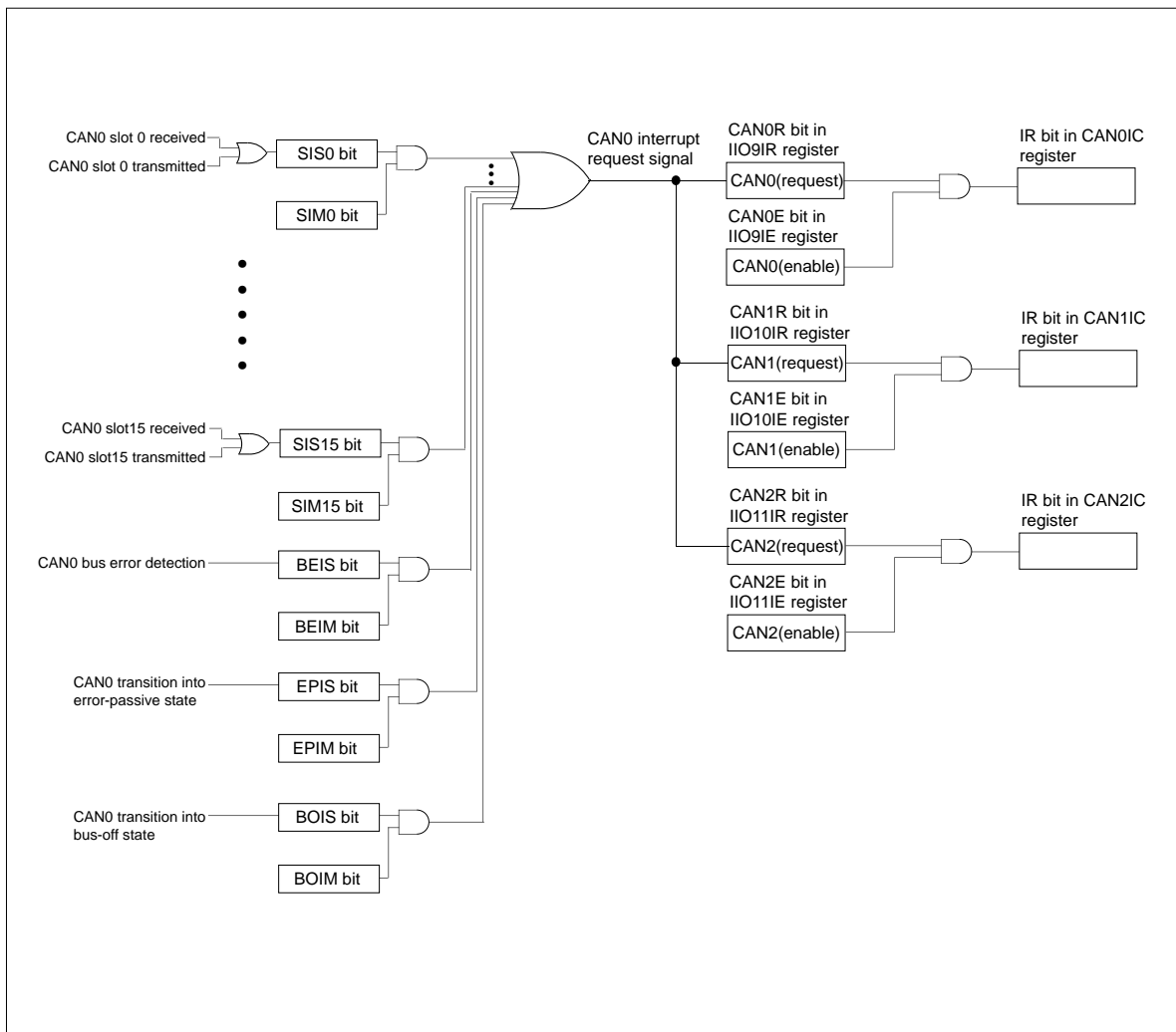


Figure 22.31 CAN Interrupts

23. DRAMC

The DRAM controller (DRAMC) controls the DRAM area, which ranges from 512 Kbytes to 8 Mbytes. Table 23.1 lists specifications of the DRAMC.

Table 23.1 DRAMC Specifications

Item	Specification
DRAM Area	512 KB, 1 MB, 2 MB, 4 MB, 8 MB
Bus Control	2CAS/1W
Refresh	CAS-before-RAS refresh, Self refresh
Supported Function Mode	EDO, fast page mode
Wait State Insertion	1-wait state, 2-wait state

Table 23.2 shows pins associated with DRAMC. Signals listed in Table 23.2 are output by setting the AR2 to AR0 bits in the DRAMCONT register for the DRAM area and accessing DRAM. See **Table 7.9** for $\overline{\text{RAS}}$, $\overline{\text{CASL}}$, $\overline{\text{CASH}}$ and $\overline{\text{DW}}$ signal operations. Figure 23.1 shows the DRAMCONT register and REFCNT register.

Table 23.2 DRAMC-associated Pins

Port	Bus for Device Access except DRAM ⁽¹⁾	Bus for DRAM Access
P0	D0 to D7	D0 to D7
P1	D8 to D15	D8 to D15 ⁽²⁾
P3	A8 to D15	MA0 to MA7
P40 to P44	A16 to A20	MA8 to MA12
P50	WRL / WR	$\overline{\text{CASL}}$
P51	WRH / BHE	$\overline{\text{CASH}}$
P52	RD	$\overline{\text{DW}}$
P56	ALE	$\overline{\text{RAS}}$

NOTES:

1. This is an example of the separate bus and 16-bit data bus.
2. This bus is available when the DS2 bit in the DS register is set to "1" (16-bit data bus) and the PM02 bit in the PM0 register is set to "1" (RD/WRL/WRH in R/W mode).

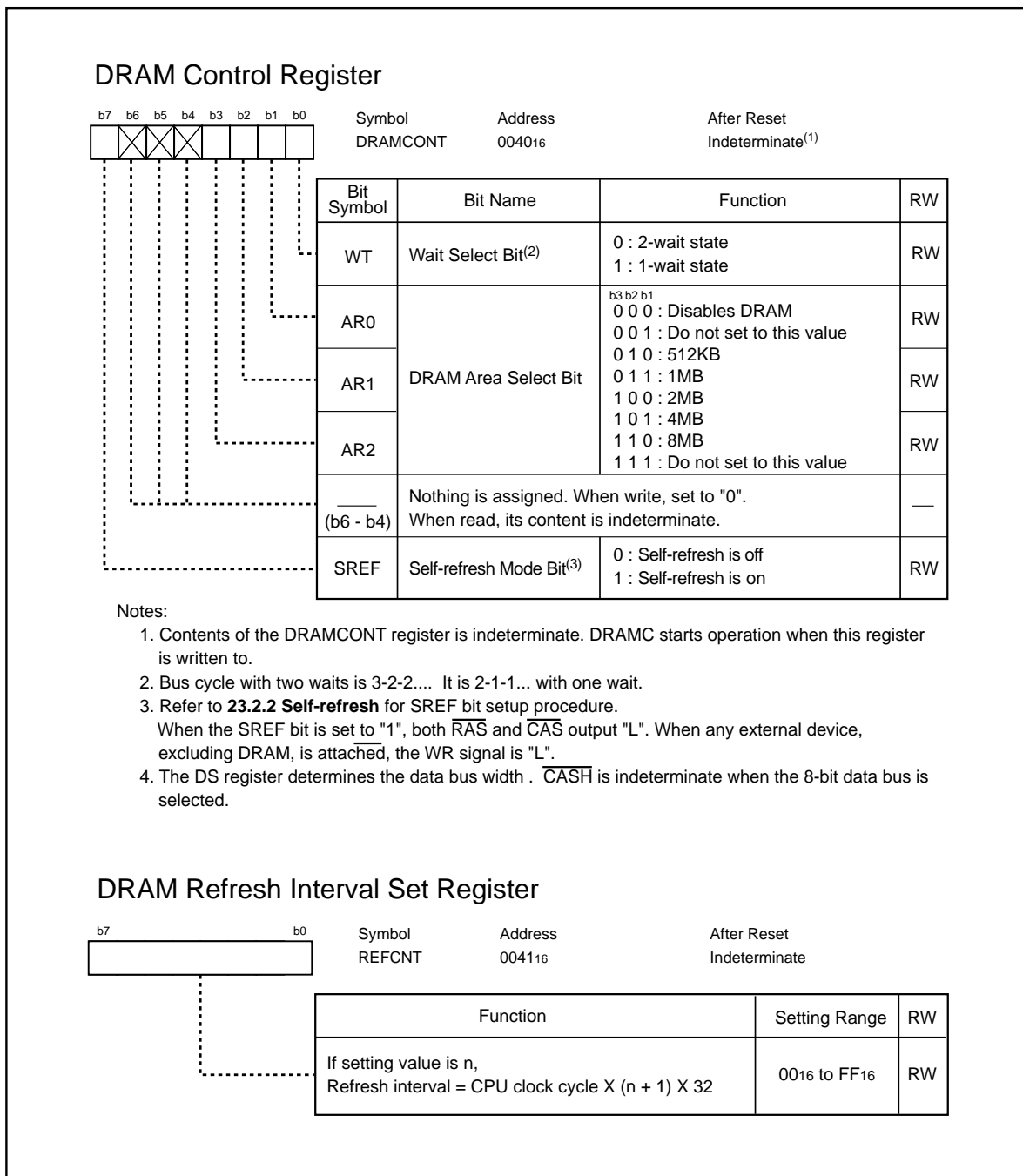


Figure 23.1 DRAMCONT Register and REFCNT Register

DRAMC is not available when the PM11 to PM10 bits in the PM1 register are set to "112" (mode 3). Set the PM11 to PM10 bits to "002," "012" or "102" (mode 0 to 2). When the 16-bit DRAM data bus is selected, set the PM02 bit in the PM0 register to "1" (RD/WRH/WRL).

Required wait time between DRAM power-on and memory operation, and necessary processing of dummy cycle for refresh varies with externally attached DRAM specifications.

23.1 DRAMC Multiplexed Address Output

DRAMC outputs signals, which are multiplexed row addresses and column addresses, to address bus A8 to A20. Figure 23.2 shows an output format for multiplexed addresses.

23.2 Refresh

23.2.1 Refresh

Refresh method is the $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh. The REFCNT register controls the refresh interval. Refresh signals are not output in a hold state.

The setting value of the REFCNT register is obtained as follows:

The value of the REFCNT register (00₁₆ to FF₁₆) = refresh interval time / (CPU clock frequency X 32) - 1

23.2.2 Self-Refresh

The refresh signal described in 23.2.1 stops while the CPU stops in stop mode, etc. The DRAM self-refresh function can be activated by setting the self-refresh before the CPU stops. Setting and cancellation procedures for the self-refresh are as follows:

(1) Setting self-refresh (with 1 wait state, 4 Mbytes)

```

...
mov.b #00000001b,DRAMCONT ;Set the AR2 to AR0 bits to "0002" (DRAM disabled)
mov.b #10001011b,DRAMCONT ;Set the AR2 to AR0 bits again and the SREF bit to "1"
                               (self-refresh on) simultaneously

nop ;Execute the nop instruction twice
nop ;
...

```

(2) Cancellation of self-refresh (with 1 wait state, 4M bytes)

```

...
mov.b #00000001b,DRAMCONT ;Set the AR2 to 0 bits to "0002" (self-refresh cancellation)
                               and the SREF bit to "0" (DRAM disabled) simultaneously
mov.b #00001011b,DRAMCONT ;Set the AR2 to AR0 bits again
mov.b 400h, 400h           ;DRAM access is disabled immediately after cancellation.
                               This is an example of a dummy read operation.
...

```

Both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are held "L" during self-refresh. When devices other than DRAM are attached, the $\overline{\text{WR}}$ signal is held "L". Take procedures such as applying an "H" signal to the $\overline{\text{CS}}$.

Figures 23.3 to 23.5 show bus timings during DRAM access.

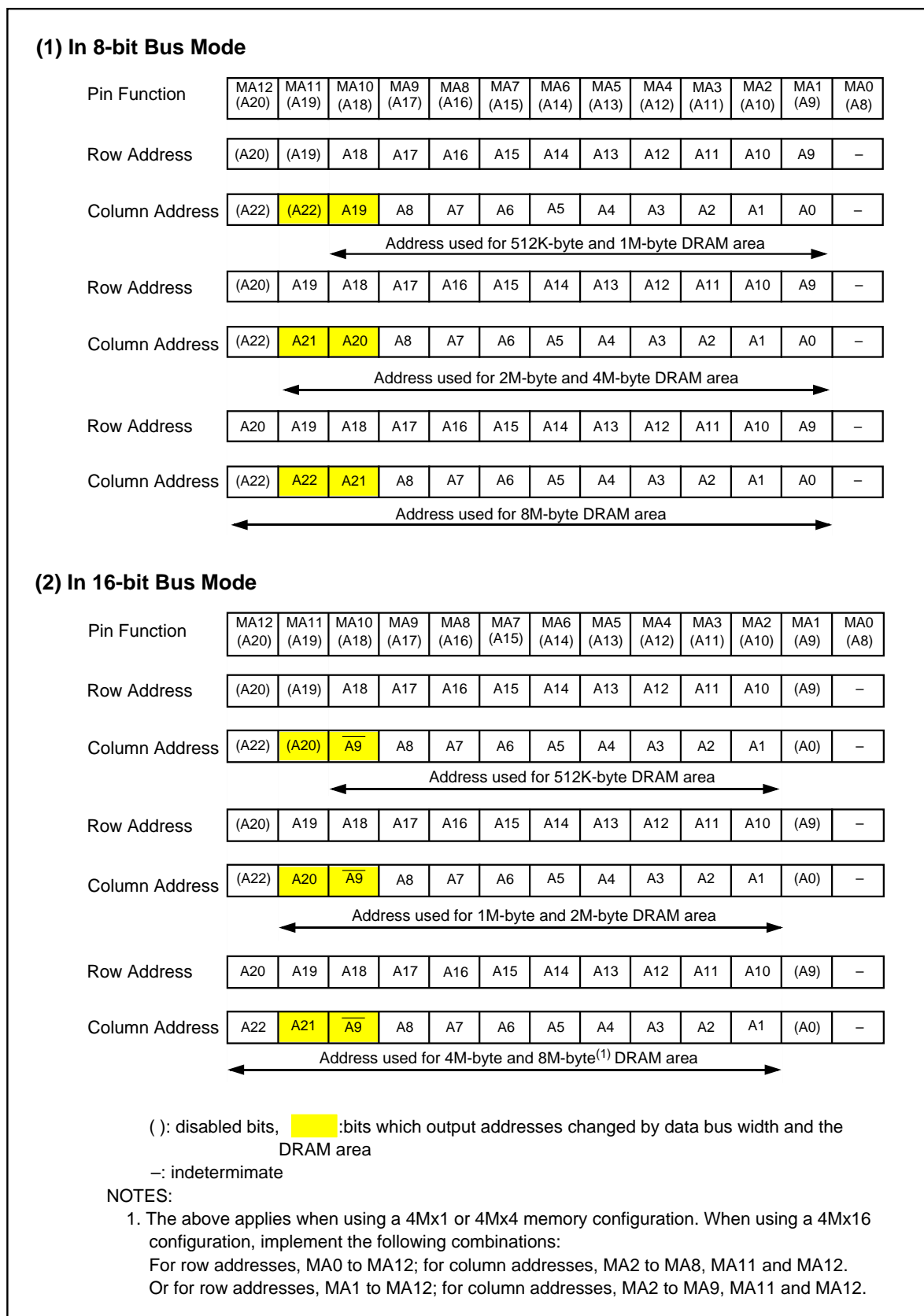


Figure 23.2 Multiplexed Address Output Pattern

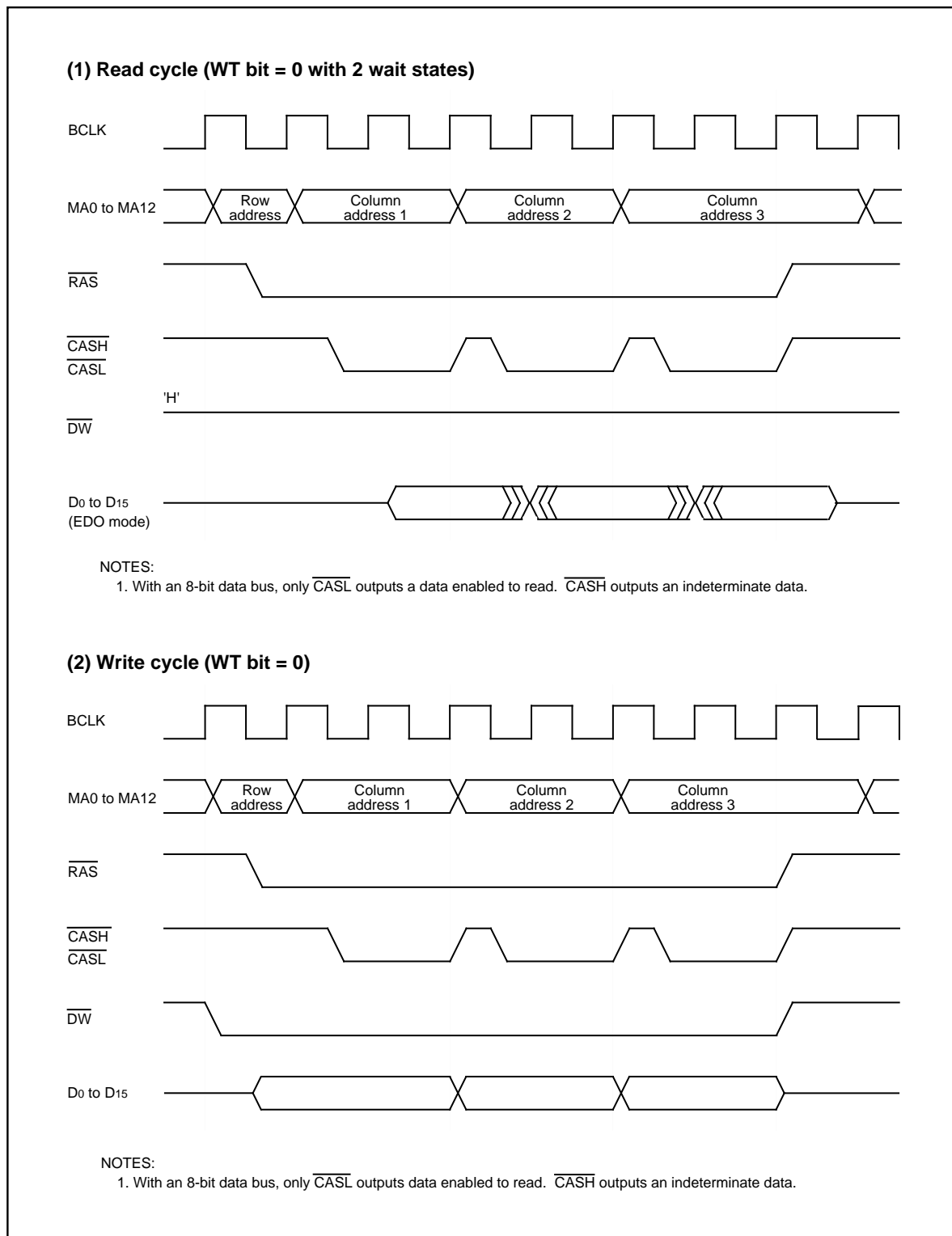


Figure 23.3 Bus Timing during DRAM Access (1)

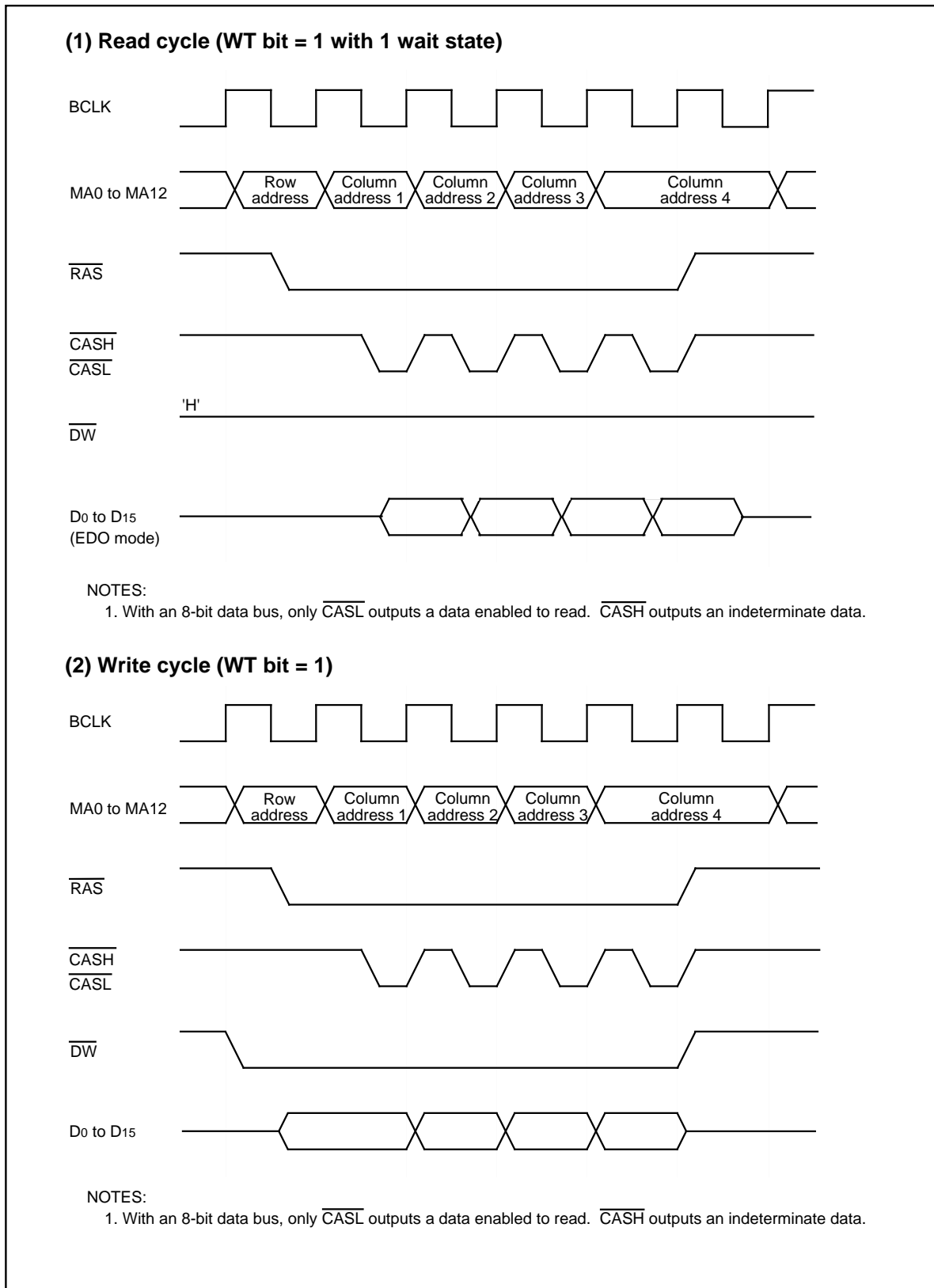


Figure 23.4 Bus Timing during DRAM Access (2)

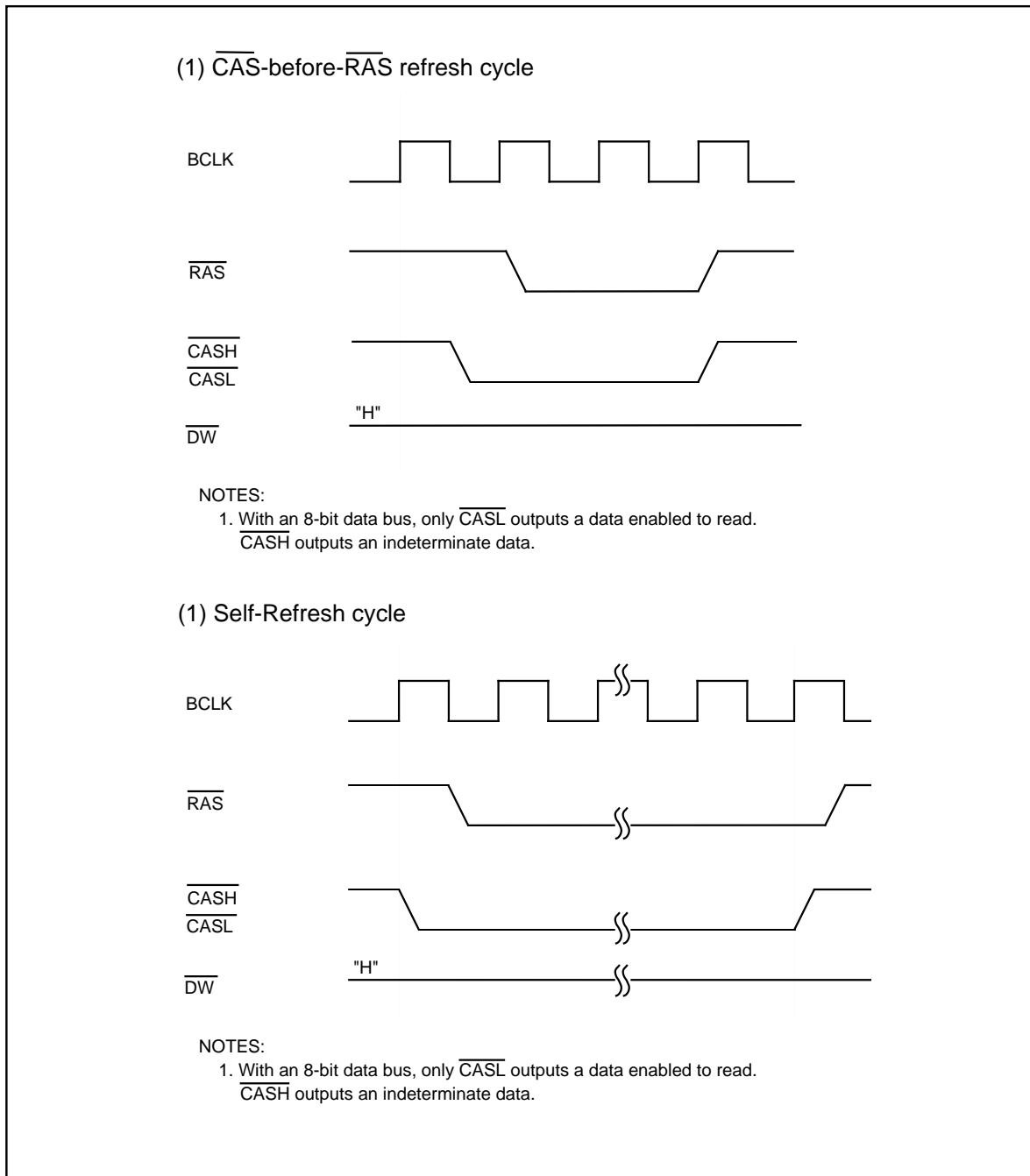


Figure 23.5 Bus Timing during DRAM Access (3)

24. Programmable I/O Ports

87 programmable I/O ports from P0 to P10 (excluding P85) are available in the 100-pin package and 123 programmable I/O ports from P0 to P15 (excluding P85) are in the 144-pin package. The direction registers determine each port status, input or output. The pull-up control registers determine whether the ports, divided into groups of four ports, are pulled up or not. P85 is an input port and no pull-up for this port is allowed. The P8_5 bit in the P8 register indicates an $\overline{\text{NMI}}$ input level since P85 shares pins with $\overline{\text{NMI}}$. Figures 24.1 to 24.4 show programmable I/O port configurations.

Each pin functions as the programmable I/O port, an I/O pin for internal peripheral functions or the bus control pin.

To use the pins as input or output pins for internal peripheral functions, refer to the explanations for each function. Refer to **7. Bus** when used as the bus control pin.

The registers, described below, are associated with the programmable I/O ports.

24.1 Port Pi Direction Register (PDi Register, i=0 to 15)

Figure 24.5 shows the PDi register.

The PDi register selects input or output status of a programmable I/O port. Each bit in the PDi register corresponds to a port.

In memory expansion and microprocessor mode, pins being used as bus control pins (A0 to A22, $\overline{\text{A23}}$, D0 to D15, MA0 to MA12, $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$, $\overline{\text{WRL/WR/CASL}}$, $\overline{\text{WRH/BHE}}$, $\overline{\text{RD/DW}}$, BCLK/ALE/CLKOUT, $\overline{\text{HLDA/ALE}}$, $\overline{\text{HOLD}}$, ALE/RAS, and $\overline{\text{RDY}}$) cannot be controlled by the PDi register. No bits controlling P85 are provided in the direction registers.

24.2 Port Pi Register (Pi Register, i=0 to 15)

Figure 24.6 shows the Pi register.

The Pi register writes and reads data to communicate with external devices. The Pi register consists of a port latch to hold output data and a circuit to read pin states. Each bit in the Pi register corresponds to a port.

In memory expansion and microprocessor mode, pins being used as bus control pins (A0 to A22, $\overline{\text{A23}}$, D0 to D15, MA0 to MA12, $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$, $\overline{\text{WRL/WR/CASL}}$, $\overline{\text{WRH/BHE}}$, $\overline{\text{RD/DW}}$, BCLK/ALE/CLKOUT, $\overline{\text{HLDA/ALE}}$, $\overline{\text{HOLD}}$, ALE/RAS, and $\overline{\text{RDY}}$) cannot be controlled by the Pi register.

24.3 Function Select Register Aj (PSj Register) (j=0 to 3, 5 to 9)

Figures 24.7 to 24.11 show the PSj registers.

The PSj register selects either I/O port or peripheral function output if an I/O port shares pins with a peripheral function output (excluding DA0 and DA1.)

Tables 24.3 to 24.12 list peripheral function output control settings for each pin.

When multiple peripheral function outputs are assigned to a pin, set the PSLk (k=0 to 3) and PSC registers to select which function is used.

24.4 Function Select Register Bk (PSLk Register) (k=0 to 3)

Figures 24.12 and 24.13 show the PSL0 to PSL3 registers.

When multiple peripheral function outputs are assigned to a pin, the PSL0 to PSL3 registers select which peripheral function output is used.

Refer to **24.9 Analog Input and Other Peripheral Function Input** for the PSL3_3 to PSL3_6 bits in the PSL3 register.

24.5 Function Select Register C (PSC Register)

Figure 24.14 show the PSC register.

When multiple peripheral function outputs are assigned to a pin, the PSC register select which peripheral function output is used.

Refer to **24.9 Analog Input and Other Peripheral Function Input** for the PSC_7 bit in the PSC register.

24.6 Pull-up Control Register 0 to 4 (PUR0 to PUR4 Registers)

Figures 24.15 to 24.16 show the PUR0 to PUR4 registers.

The PUR0 to PUR4 registers select whether the ports, divided into groups of four ports, are pulled up or not. Ports with bits in the PUR0 to PUR4 registers set to "1" (pull-up) and the direction registers set to "0" (input mode) are pulled up.

Set bits in the PUR0 and PUR1 registers which control P0 to P5, running as bus, to "0" (no pull-up) in memory expansion and microprocessor mode. P0, P1, P40 to P43 can be pulled up when they are used as input ports in memory expansion mode and microprocessor mode.

24.7 Port Control Register (PCR Register)

Figure 24.17 shows the PCR register.

The PCR register selects either CMOS output or N-channel open drain output as the P1 output format. If the PCR0 bits is set to "1" (N-channel open drain output), N-channel open drain output is selected because the P-channel in the CMOS port is turned off. This is, however, not a perfect open drain. Therefore, the absolute maximum rating of the input voltage is from -0.3V to $V_{cc} + 0.3V$.

If P1 is used as the data bus in memory expansion and microprocessor mode, set the PCR0 bit to "0" (CMOS output). If P1 is used as a port in memory expansion and microprocessor mode, the PCR0 bit determines the output format.

24.8 Input Function Select Register (IPS Register)

Figure 24.18 shows the IPS registers.

The IPS0 to IPS1 and IPS3 bits in the IPS register and the IPSA_0 and IPSA_3 bits in the IPSA register select which pin is assigned the intelligent I/O or CAN input functions.

Refer to **24.9 Analog Input and Other Peripheral Function Input** for the IPS2 bit.

24.9 Analog Input and Other Peripheral Function Input

The PSL3_3 to PSL3_6 bits in the PSL3 register, the PSC_7 bit in the PSC register and the IPS2 bit in the IPS register each separate analog I/O ports from other peripheral functions. Setting the corresponding bit to "1" (analog I/O) to use the analog I/O port (DA0, DA1, ANEX0, ANEX1, AN4 to AN7 or AN150 to AN157) prevents an intermediate potential from being impressed to other peripheral functions. The impressed intermediate potential may cause increase in power consumption.

Set the corresponding bit to "0" (except analog I/O) when analog I/O is not used. All peripheral function inputs except the analog I/O port are available when the corresponding bit is set to "0". These inputs are indeterminate when the bit is set to "1". When the PSC_7 bit is set to "1", key input interrupt request remains unchanged regardless of $\overline{KI0}$ to $\overline{KI3}$ pin input level change.

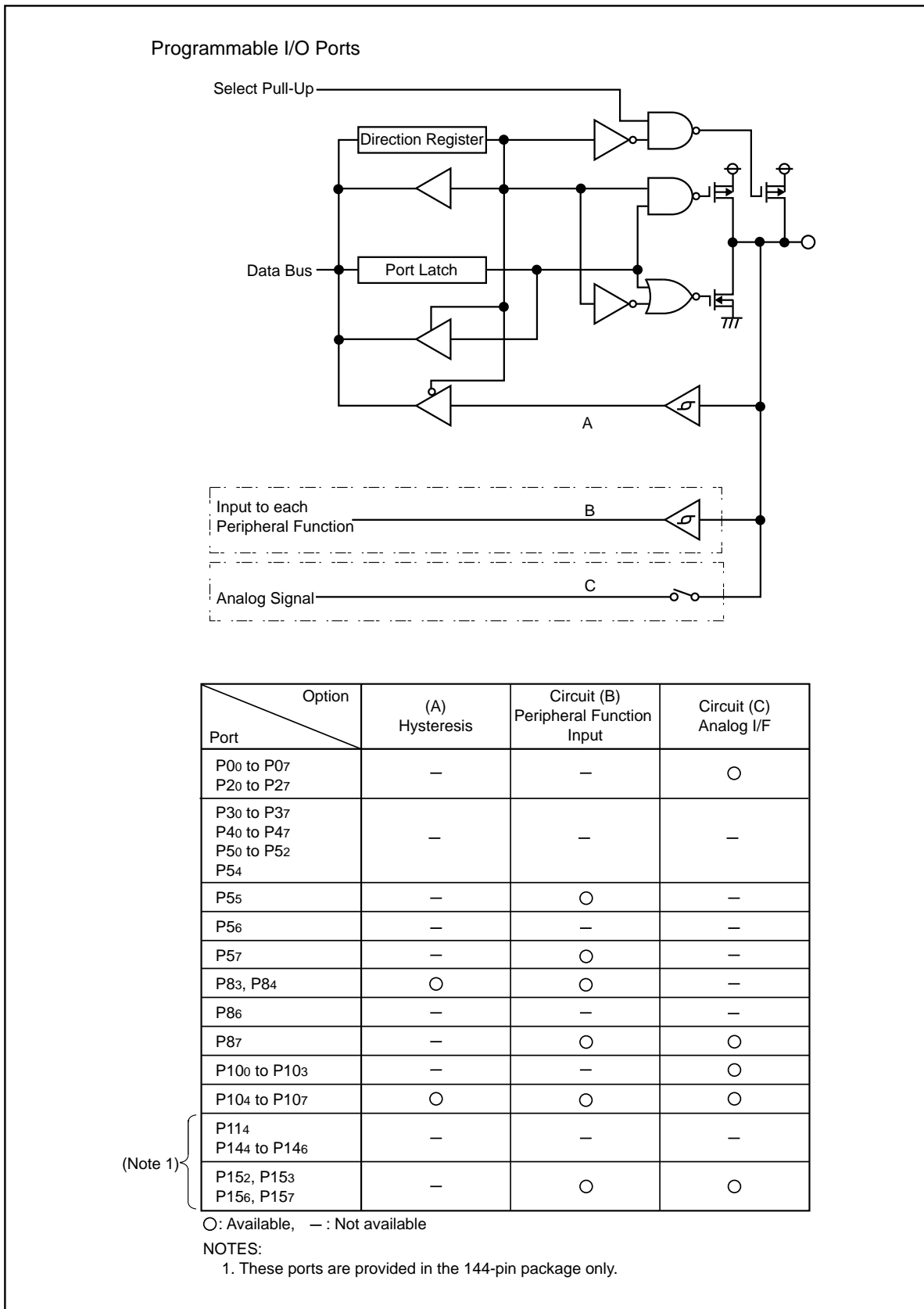


Figure 24.1 Programmable I/O Ports (1)

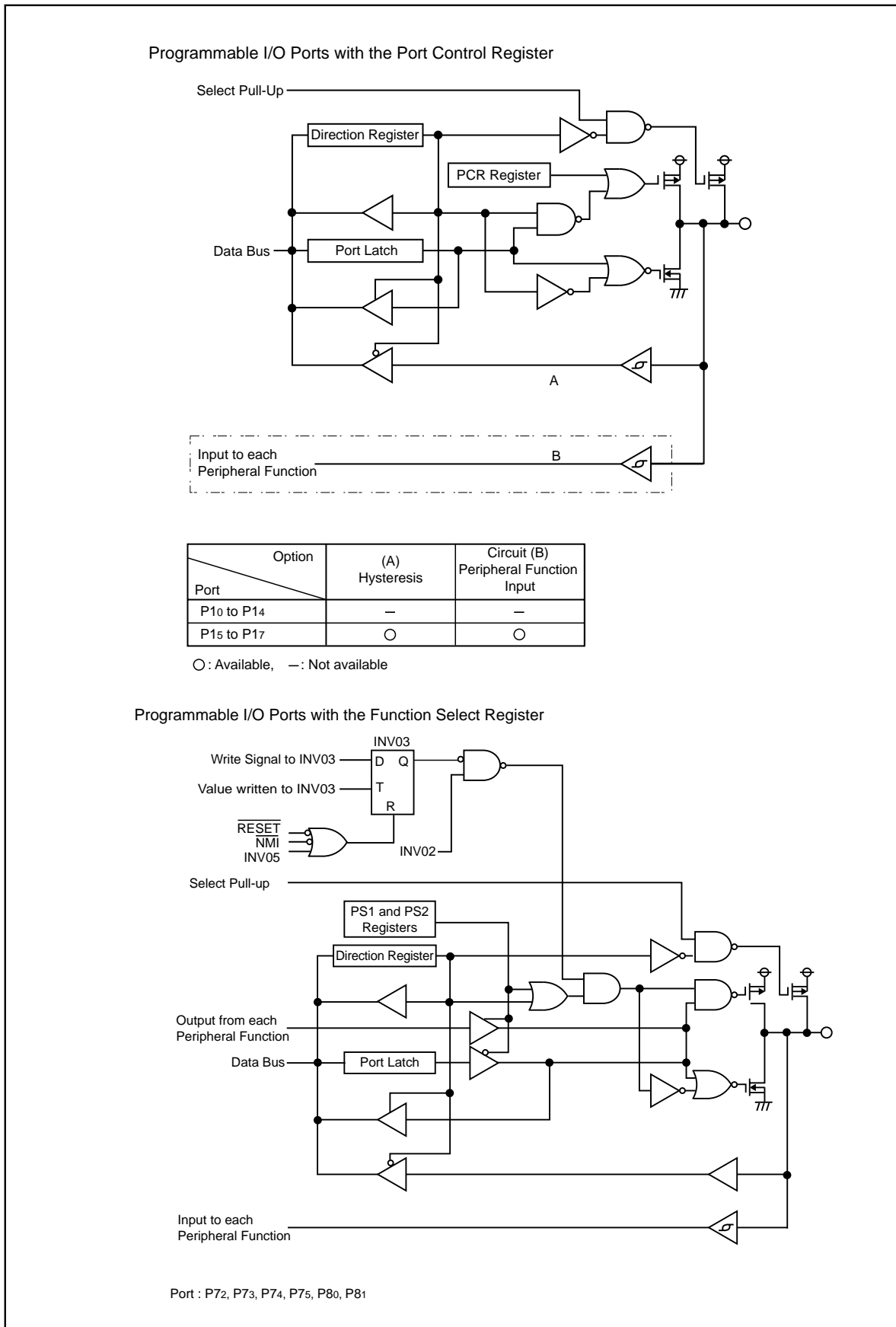


Figure 24.2 Programmable I/O Ports (2)

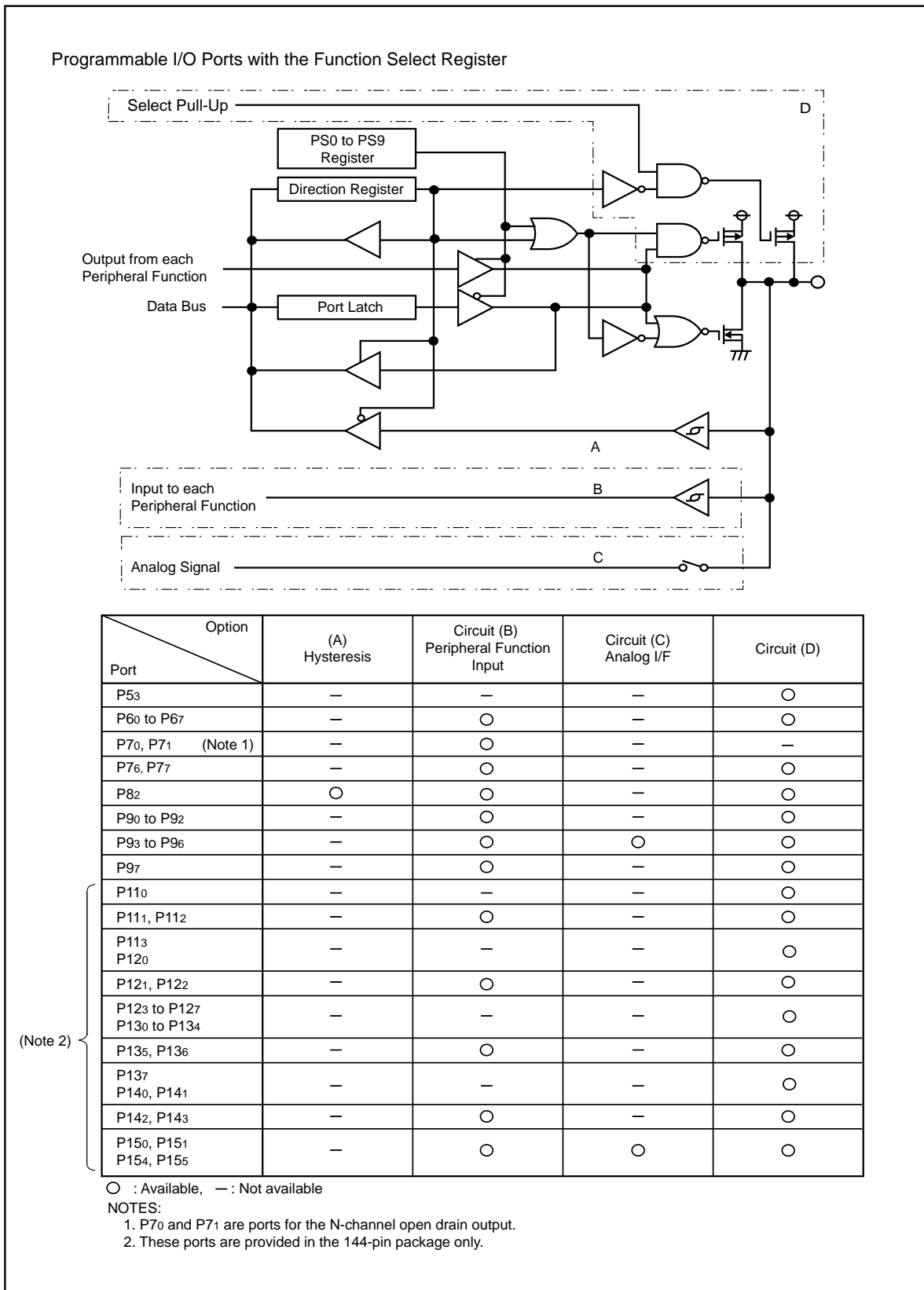


Figure 24.3 Programmable I/O Ports (3)

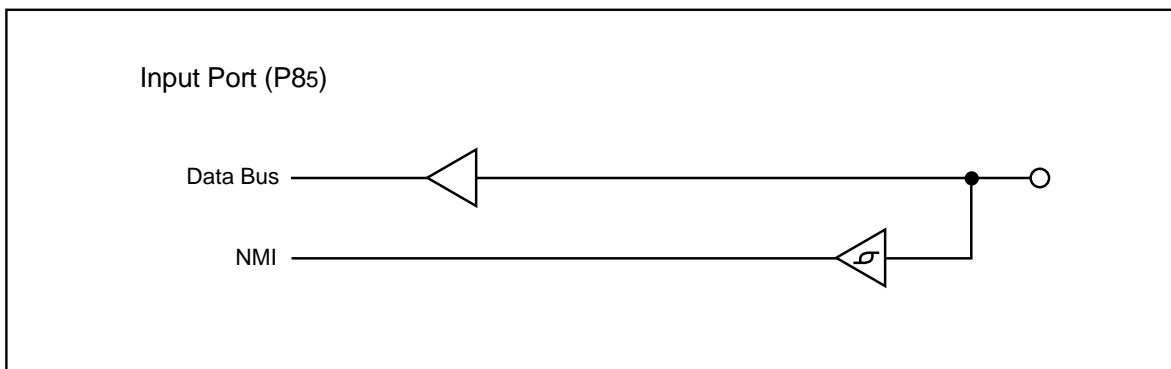


Figure 24.4 Programmable I/O Ports (4)

Port Pi Direction Register (i=0 to 15)⁽²⁾

Bit	Symbol	Bit Name	Function	RW
b7				
b6				
b5				
b4				
b3				
b2				
b1				
b0				

Symbol	Address	After Reset
PD0 to PD3	03E2 ₁₆ , 03E3 ₁₆ , 03E6 ₁₆ , 03E7 ₁₆	00 ₁₆
PD4 to PD7	03EA ₁₆ , 03EB ₁₆ , 03C2 ₁₆ , 03C3 ₁₆	00 ₁₆
PD8	03C6 ₁₆ ⁽⁴⁾	00X0 0000 ₂
PD9 to PD10	03C7 ₁₆ ⁽¹⁾ , 03CA ₁₆	00 ₁₆
PD11	03CB ₁₆ ^(3,4)	XXX0 0000 ₂
PD12 to PD13	03CE, 03CF ₁₆	00 ₁₆
PD14	03D2 ₁₆ ^(3,4)	X000 0000 ₂
PD15	03D3 ₁₆ ⁽³⁾	00 ₁₆

Bit Symbol	Bit Name	Function	RW
PDi_0	Port Pi0 Direction Register	0 : Input mode (Functions as input port) 1 : Output mode (Functions as output port)	RW
PDi_1	Port Pi1 Direction Register	0 : Input mode (Functions as input port) 1 : Output mode (Functions as output port)	RW
PDi_2	Port Pi2 Direction Register	0 : Input mode (Functions as input port) 1 : Output mode (Functions as output port)	RW
PDi_3	Port Pi3 Direction Register	0 : Input mode (Functions as input port) 1 : Output mode (Functions as output port)	RW
PDi_4	Port Pi4 Direction Register	0 : Input mode (Functions as input port) 1 : Output mode (Functions as output port)	RW
PDi_5	Port Pi5 Direction Register	0 : Input mode (Functions as input port) 1 : Output mode (Functions as output port)	RW
PDi_6	Port Pi6 Direction Register	0 : Input mode (Functions as input port) 1 : Output mode (Functions as output port)	RW
PDi_7	Port Pi7 Direction Register	0 : Input mode (Functions as input port) 1 : Output mode (Functions as output port)	RW

NOTES:

- Set the PD9 register immediately after the PRC2 bit in the PRCR register is set to "1" (write enable). Do not generate an interrupt or a DMA transfer between the instruction to set to the PRC2 bit to "1" and the instruction to set the PD9 register.
- In memory expansion and microprocessor mode, the direction register of pins being used as bus control pins (A0 to A22, A23, D0 to D15, MA0 to MA12, CS0 to CS3, WRL/WR/CASL, WRH/BHE/CASH, RD/DW, BCLK/ALE/CLKout, HLDA/ALE, HOLD, ALE/RAS and RDY) cannot be changed.
- Set the PD11 to PD15 registers to "FF₁₆" in the 100-pin package.
- Nothing is assigned to the PD8_5 bit in the PD8 register, the PD11_5 to PD11_7 bits in the PD11 register and the P14_7 bit in the PD14 register. If write, set these bits to "0". When read, their contents are indeterminate.

Figure 24.5 PD0 to PD15 Registers

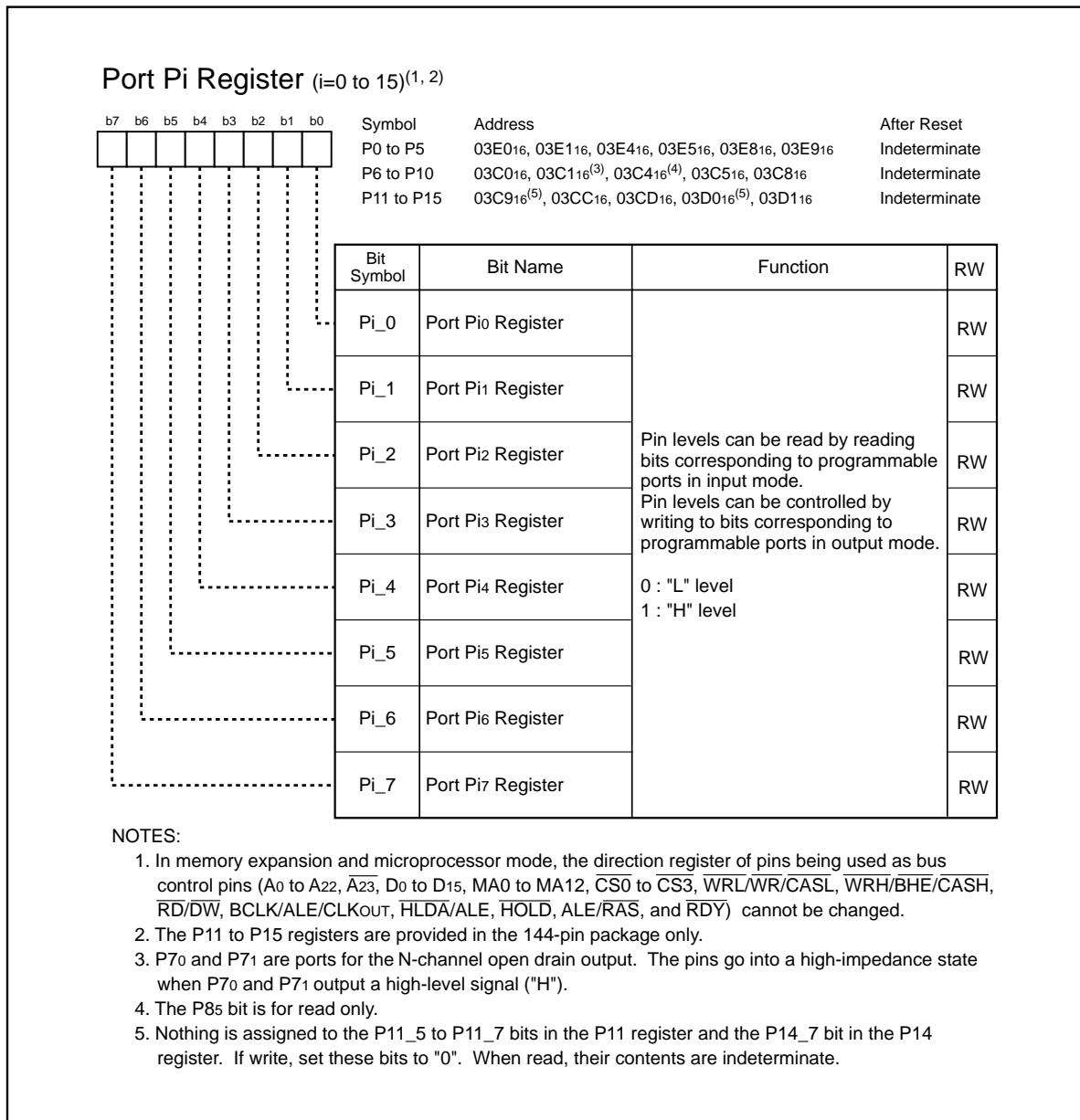


Figure 24.6 P0 to P15 Registers

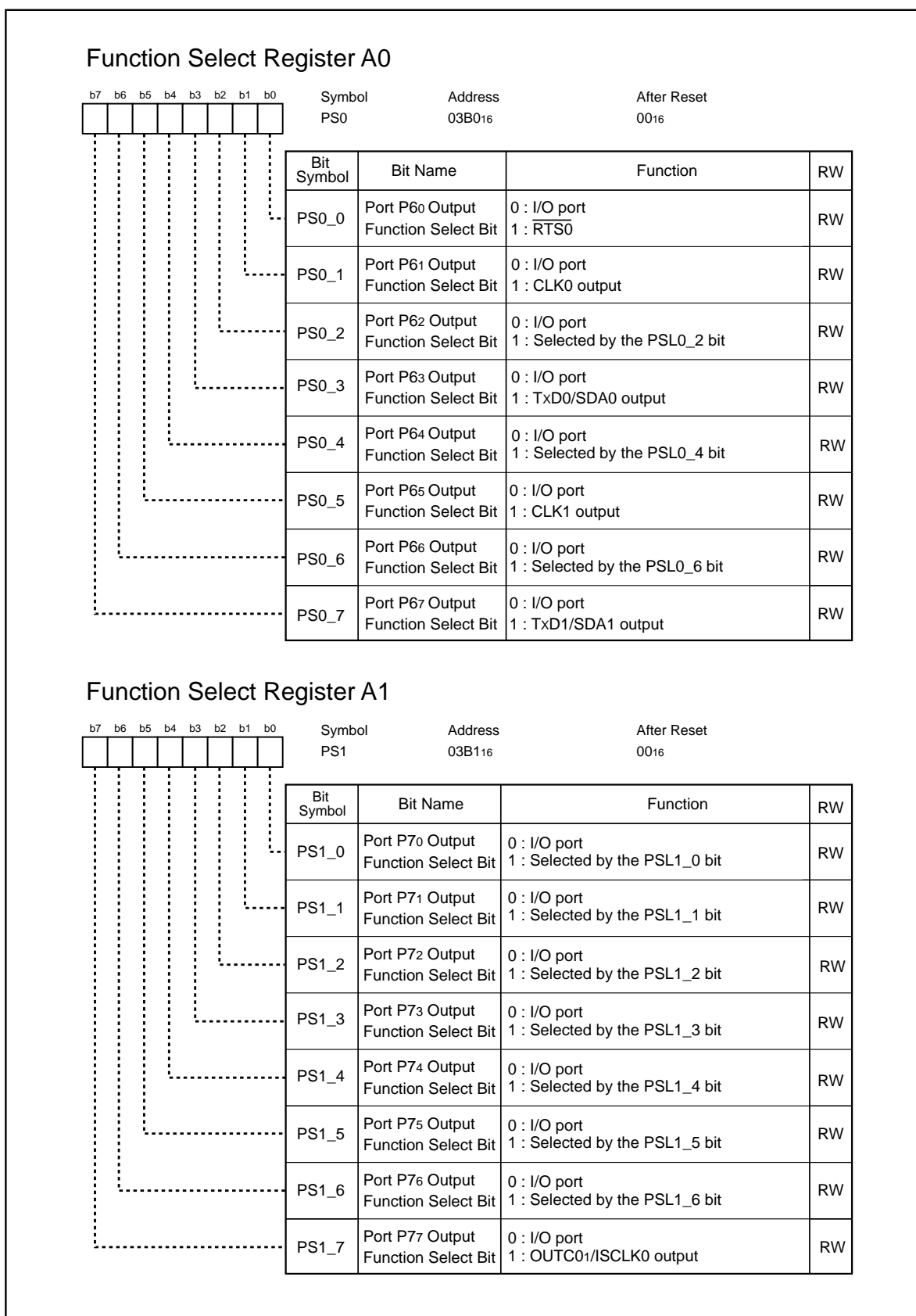


Figure 24.7 PS0 Register and PS1 Register

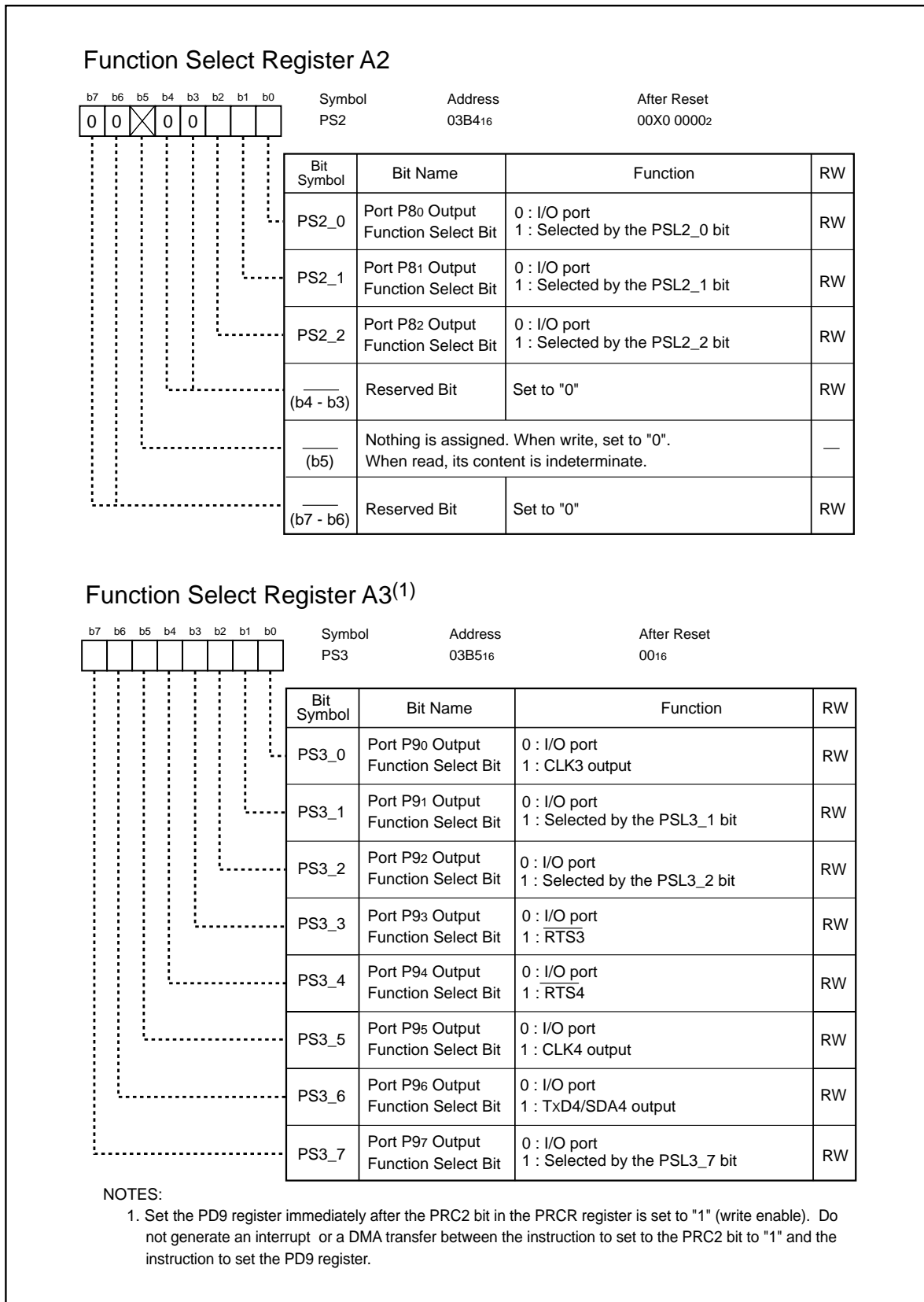


Figure 24.8 PS2 Register and PS3 Register

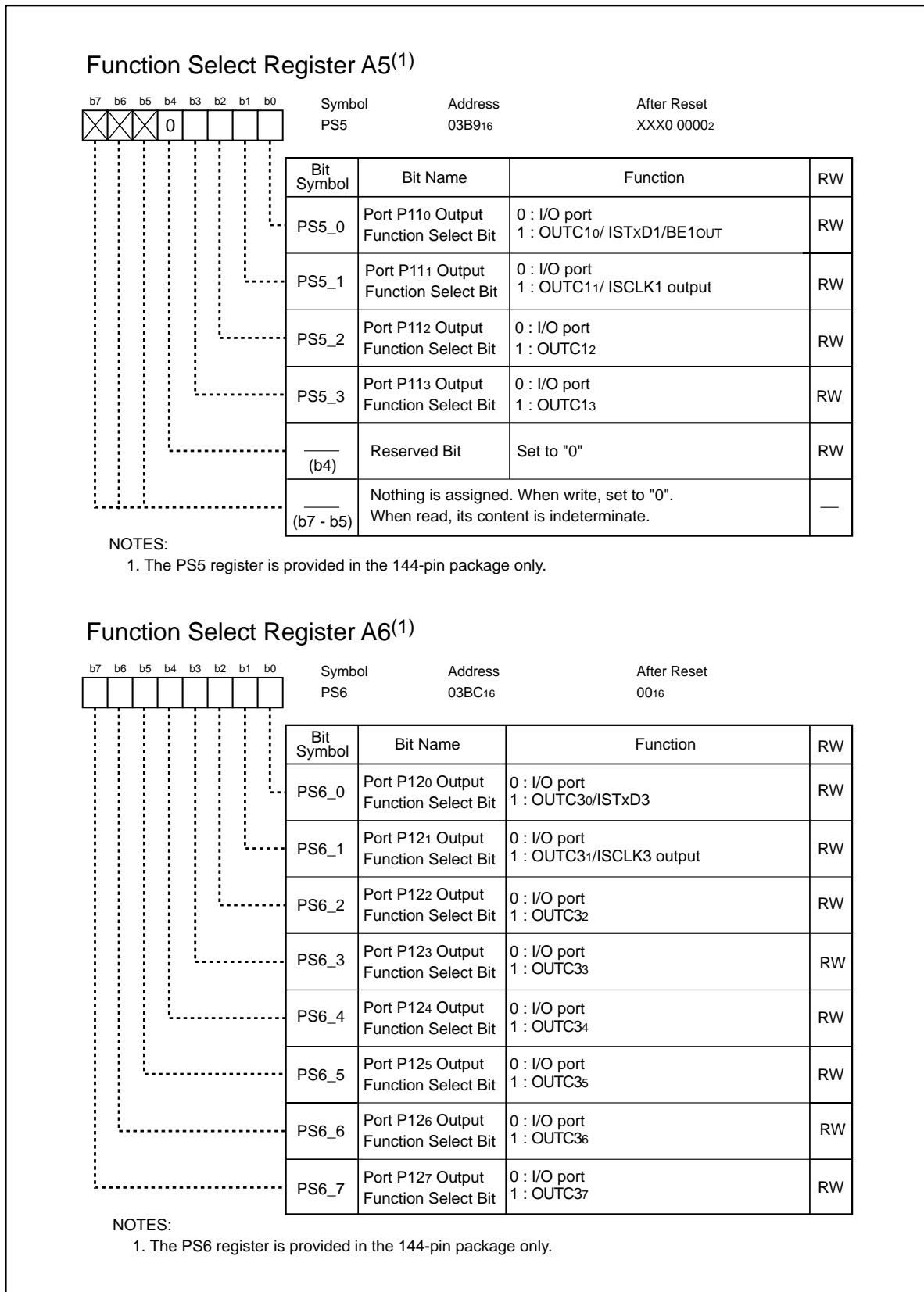
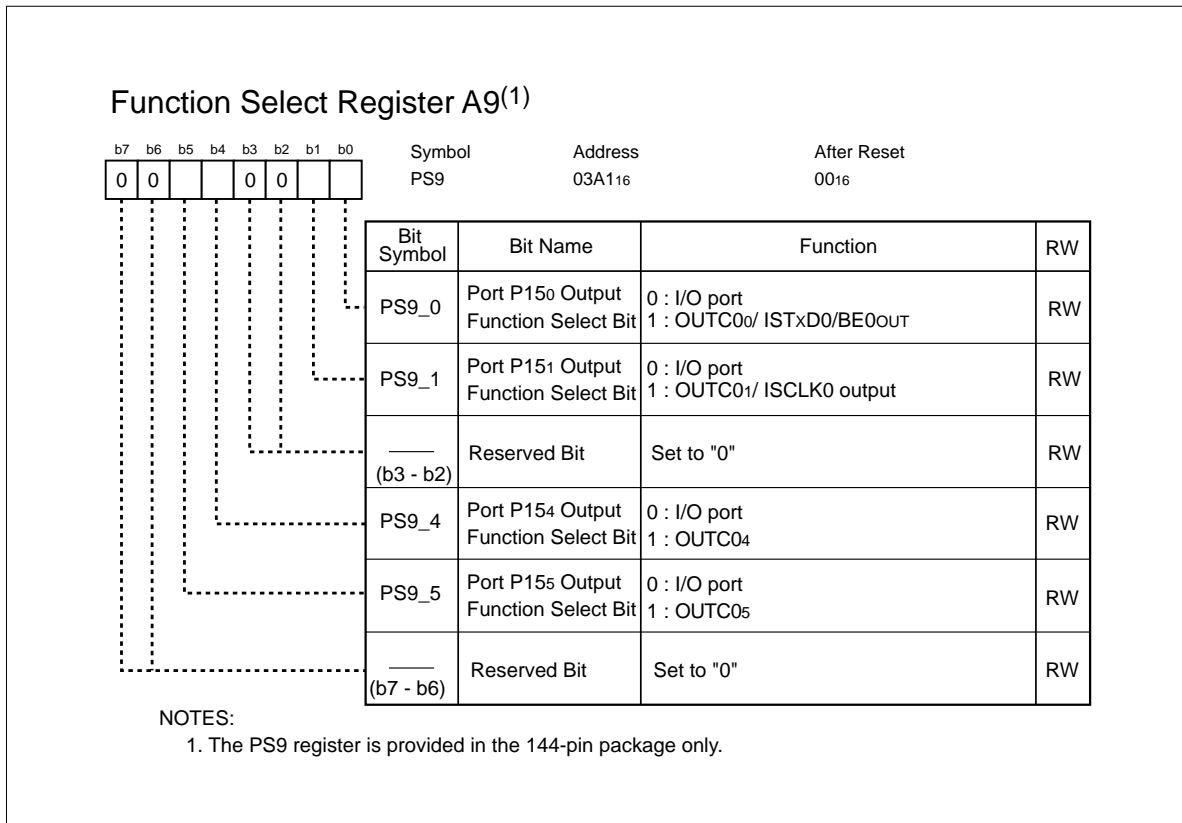


Figure 24.9 PS5 Register and PS6 Register

**Figure 24.11 PS9 Register**

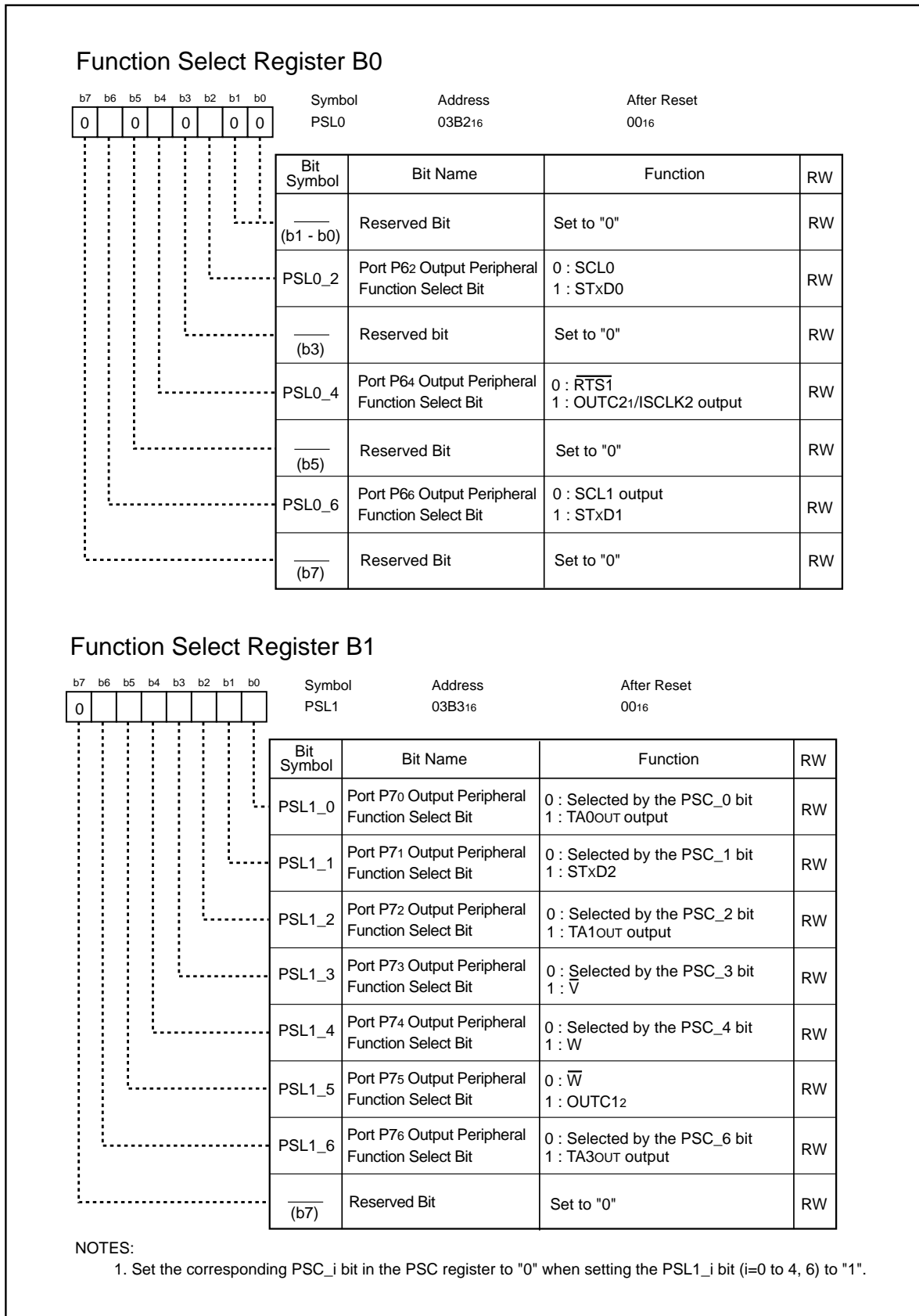


Figure 24.12 PSL0 Register and PSL1 Register

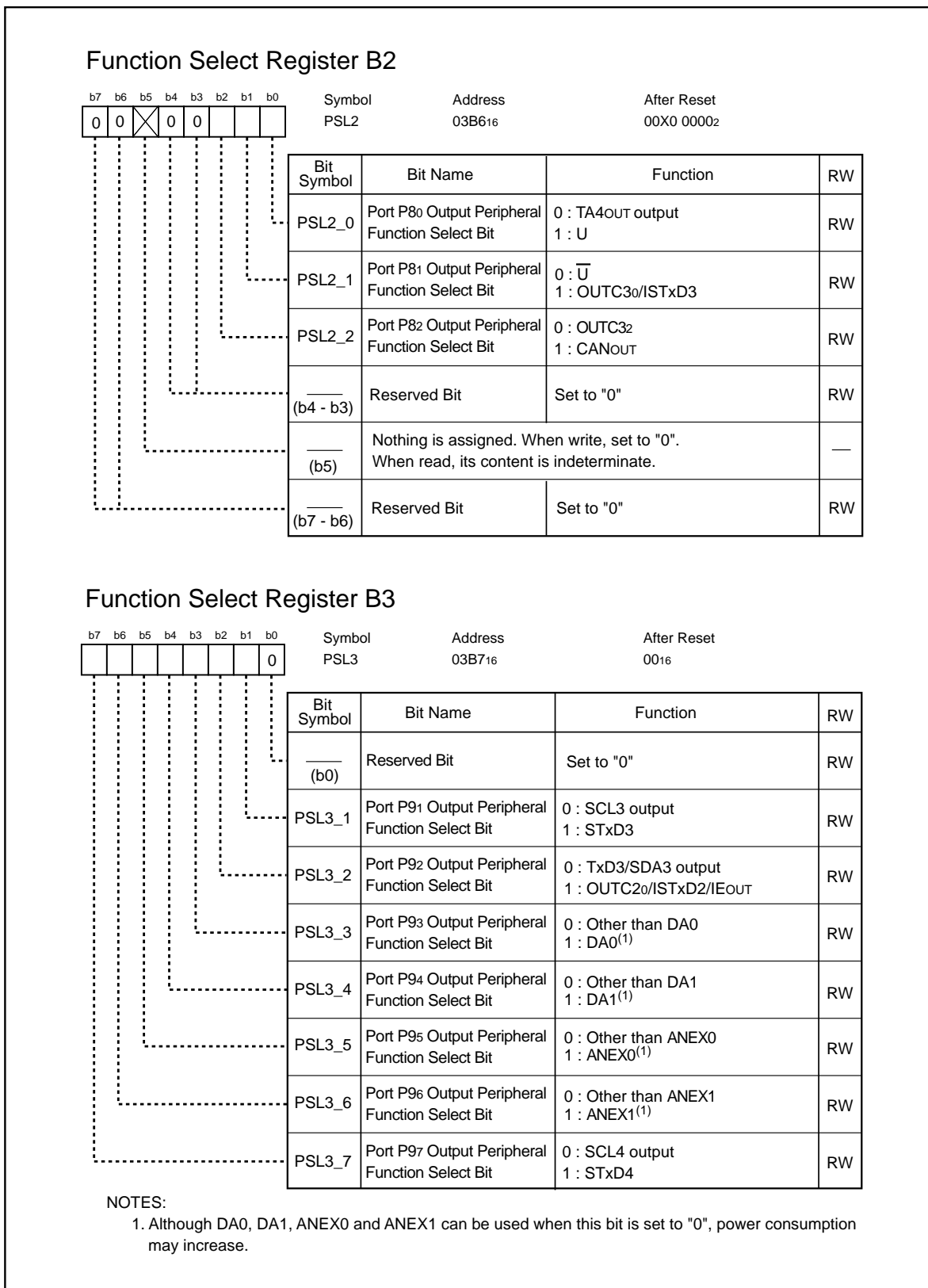


Figure 24.13 PSL2 Register and PSL3 Register

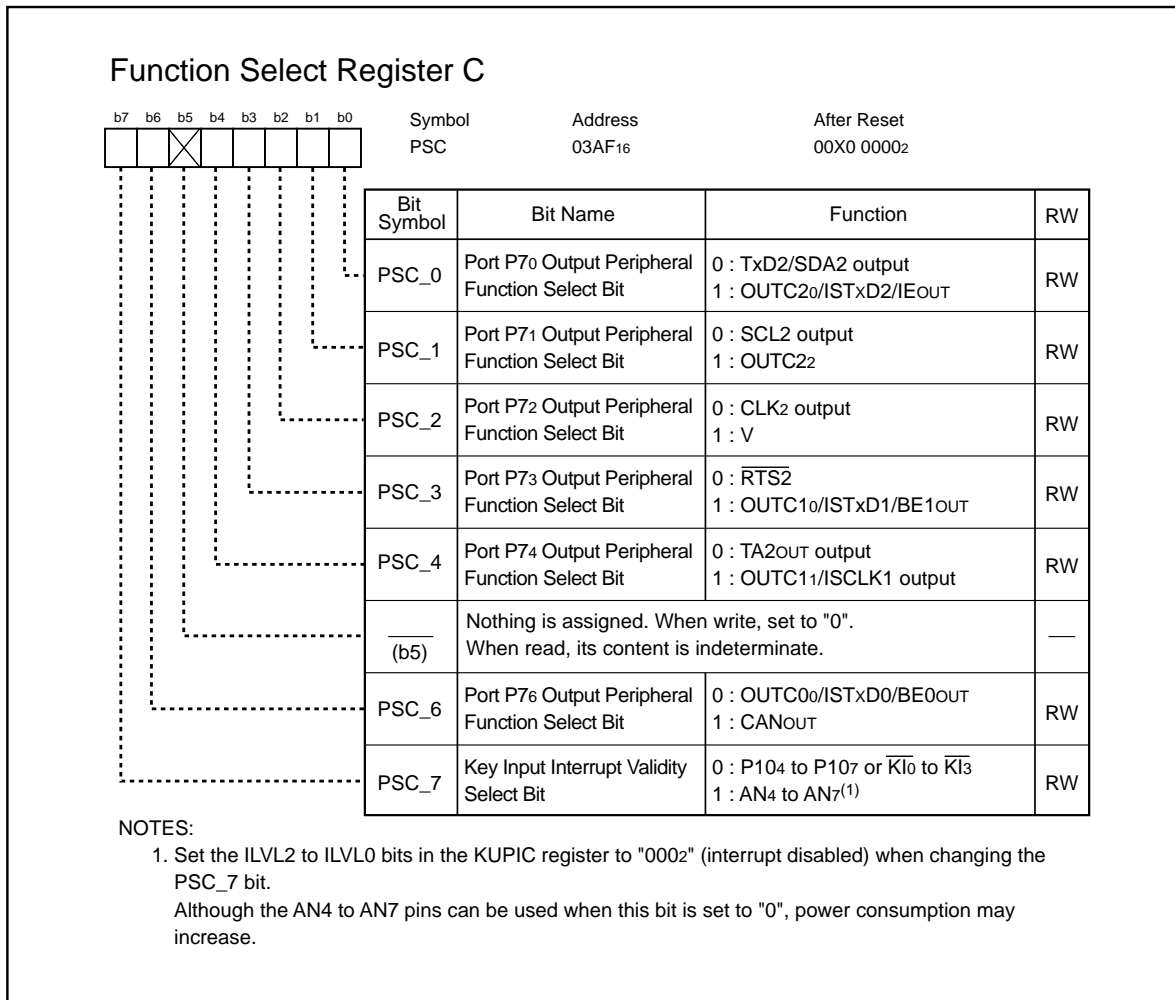


Figure 24.14 PSC Register

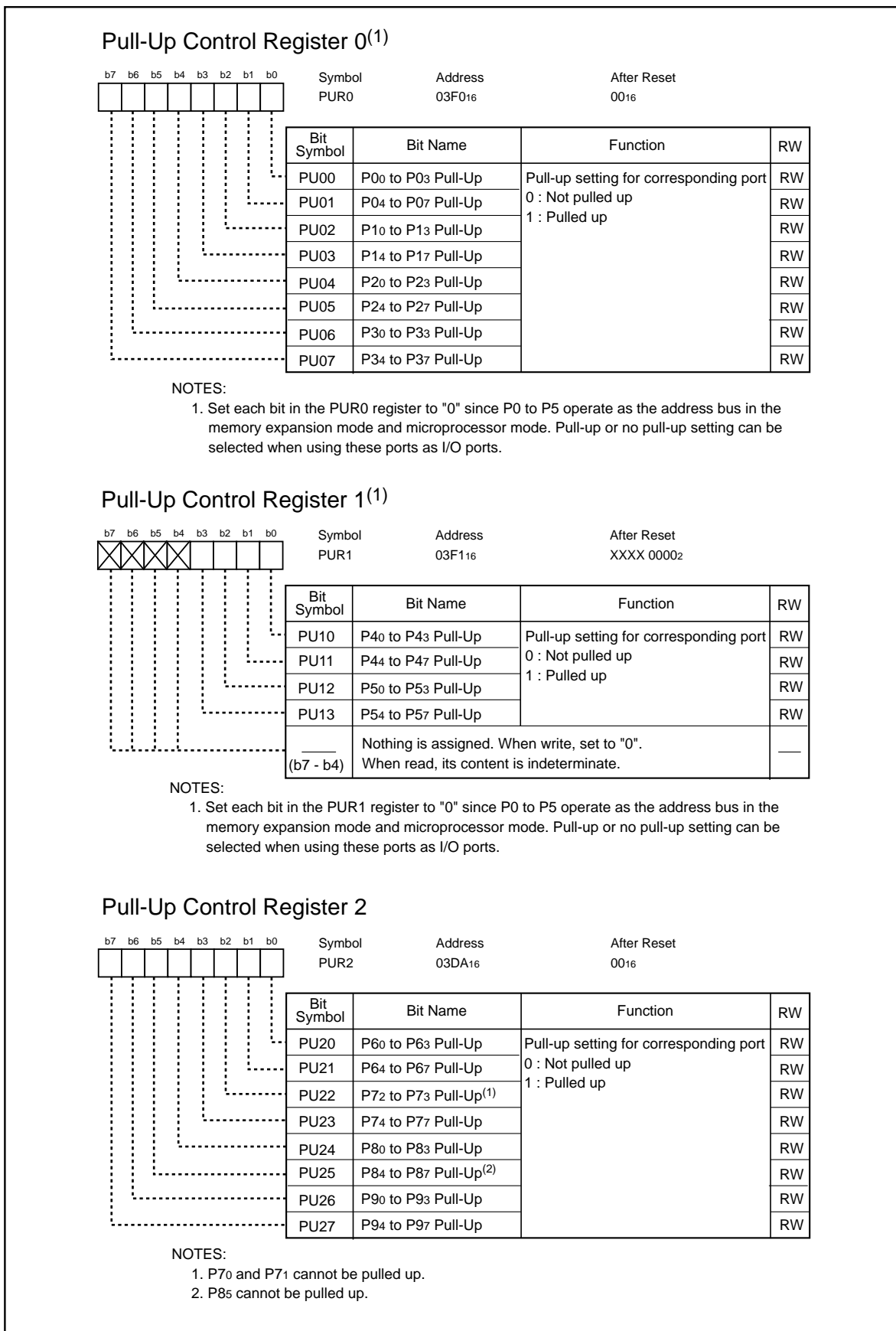


Figure 24.15 PUR0 Register, PUR1 Register and PUR2 Register

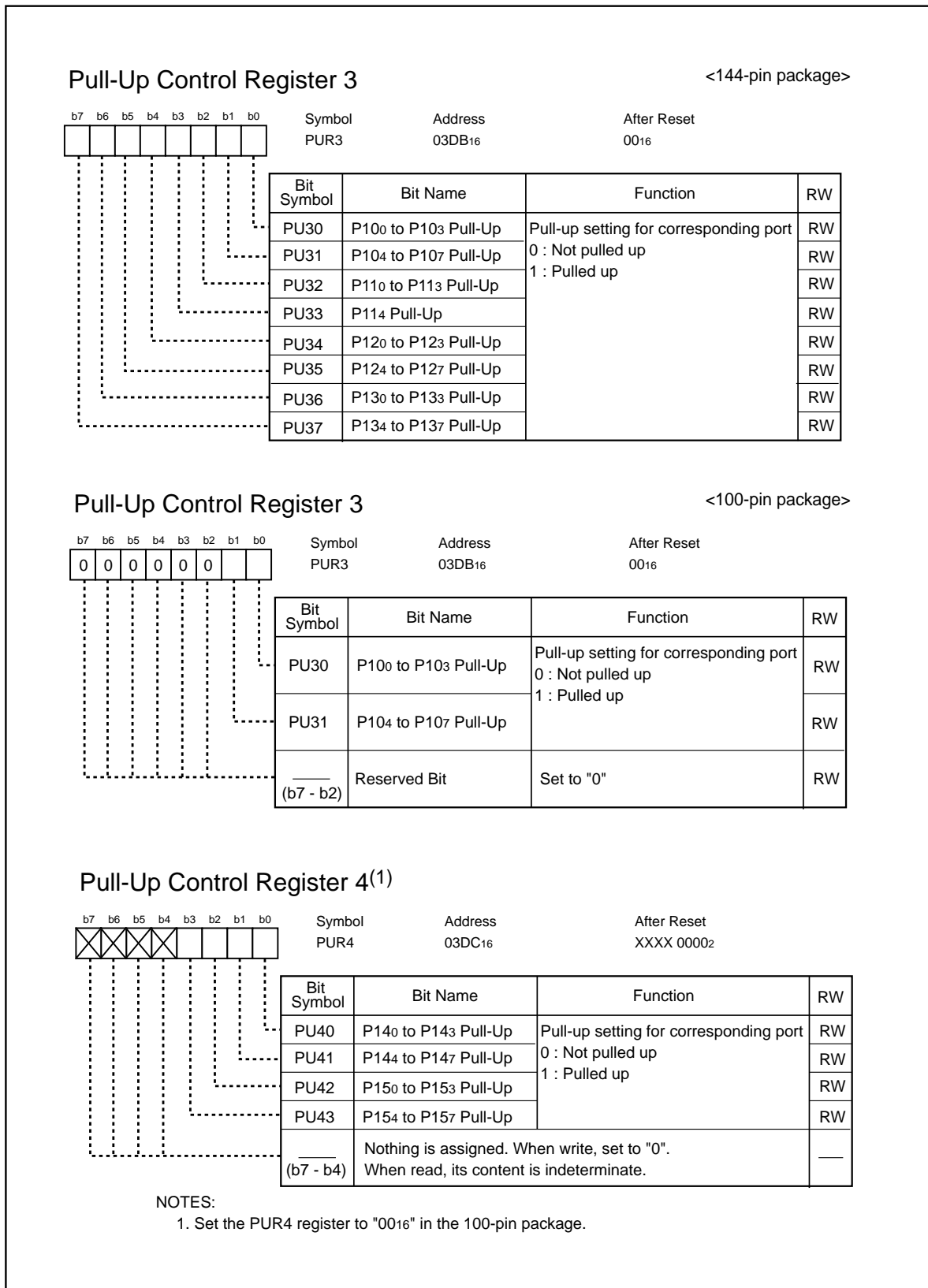


Figure 24.16 PUR3 Register and PUR4 Register

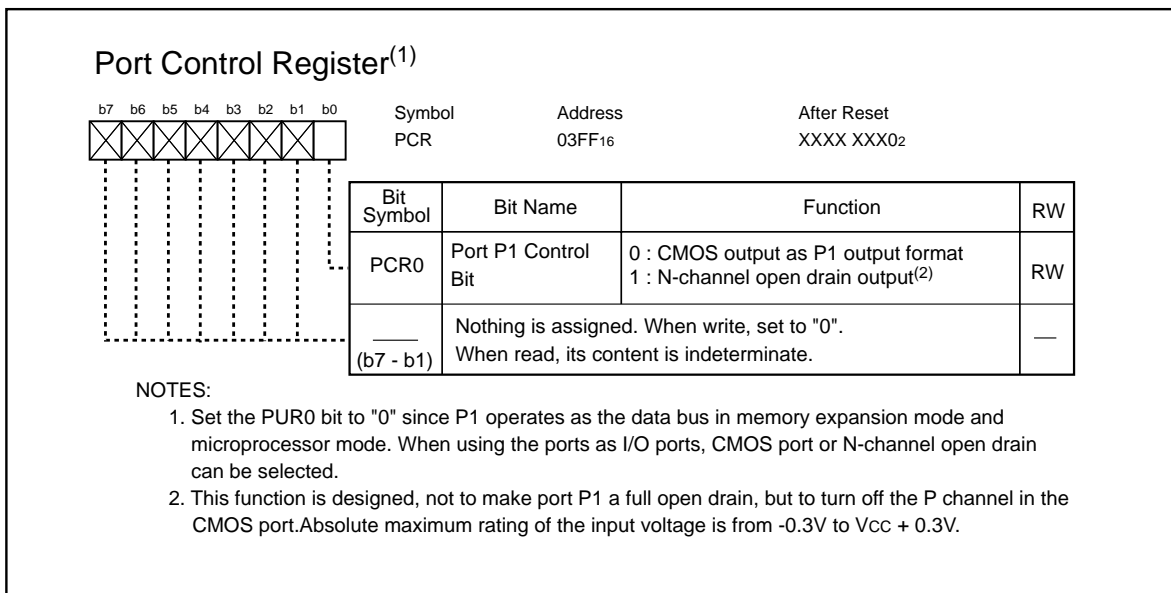


Figure 23.17 PCR Register

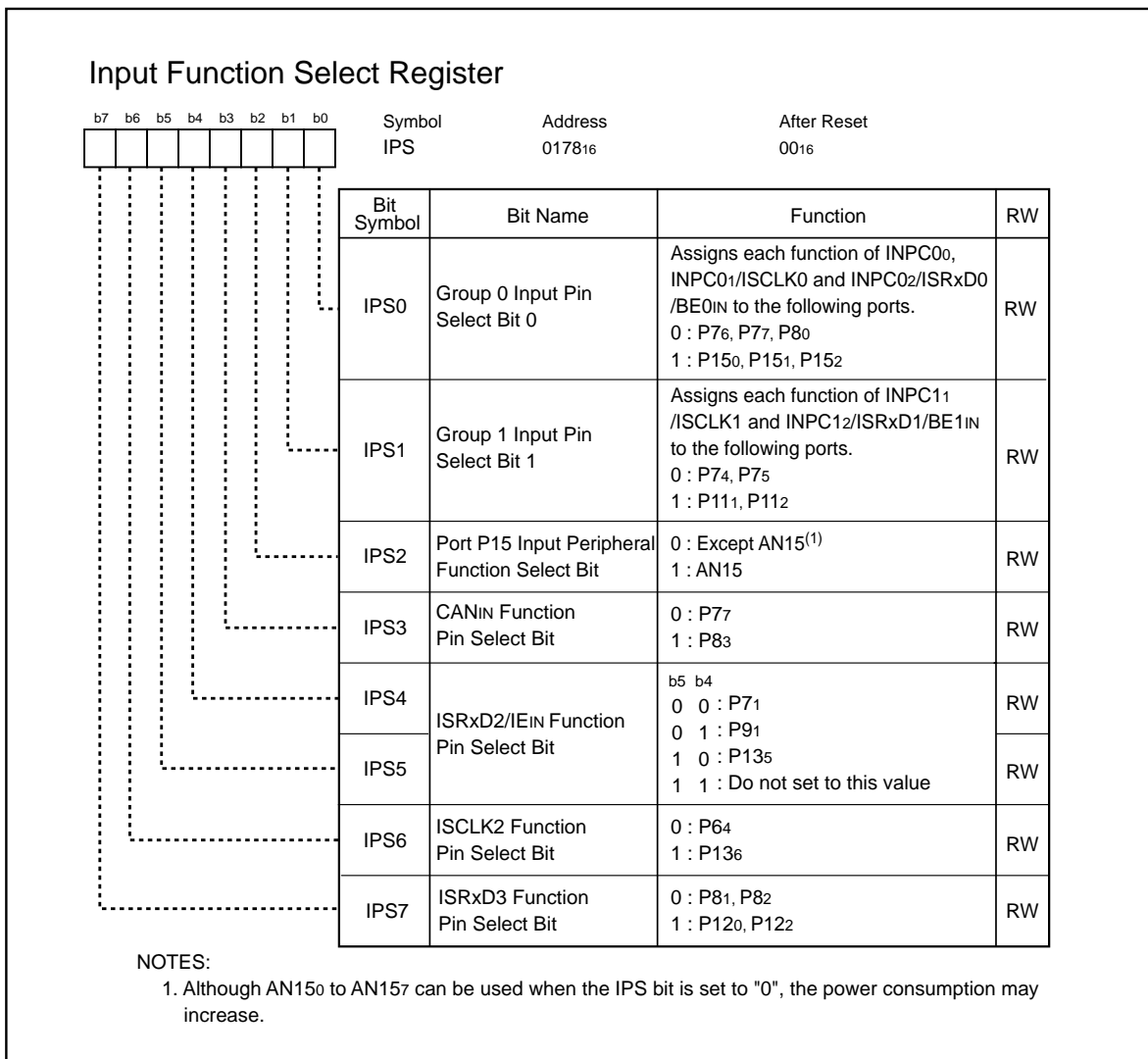


Figure 24.18 IPS Register

Table 24.1 Unassigned Pin Settings in Single-chip Mode

Pin Name	Setting
P0 to P15 (excluding P85) ^(1,2,3,4,6)	Enter input mode and connect each pin to Vss via a resistor (pull-down); or enter output mode and leave pins open
XOUT ⁽⁵⁾	Leave pin open
NMI(P85)	Connect pin to Vcc via a resistor (pull-up)
AVCC	Connect pin to VCC
AVSS, VREF, BYTE	Connect pins to VSS

NOTES:

- P11 to P15 are provided in the 144-pin package only.
- If the port enters output mode and is left open, it is in input mode before output mode is entered by program after reset. While the port is in input mode, voltage level on the pins is indeterminate and power consumption may increase.
Direction register settings may be changed by noise or failure caused by noise. Configure direction register settings regularly to increase the reliability of the program.
- Use the shortest possible wiring to connect the microcomputer pins to unassigned pins (within 2 cm).
- P70 and P71 must output low-level ("L") signals if they are in output mode. They are ports for the N-channel open drain outputs.
- When the external clock is applied to the XIN pin, set the pin as written above.
- In the 100-pin package, set "FF16" in the following addresses, in addition to the above settings:
Addresses 0003CB16, 0003CE16, 0003CF16, 0003D216, 0003D316

Table 24.2 Unassigned Pin Setting in Memory Expansion Mode and Microprocessor Mode

Pin Name	Setting
P6 to P15 (excluding P85) ^(1,2,3,4,6)	Enter input mode and connect each pin to Vss via a resistor (pull-down); or enter output mode and leave pins open
BHE, ALE, HLDA, XOUT ⁽⁵⁾ , BCLK	Leave pin open
NMI(P85), RDY, HOLD	Connect pin to Vcc via a resistor (pull-up)
AVCC	Connect pin to VCC
AVSS, VREF	Connect pins to VSS

NOTES:

- P11 to P15 are provided in the 144-pin package only.
- If the port enters output mode and is left open, it is in input mode before output mode is entered by program after reset. While the port is in input mode, voltage level on the pins is indeterminate and power consumption may increase.
Direction register settings may be changed by noise or failure caused by noise. Configure direction register settings regularly to increase the reliability of the program.
- Use the shortest possible wiring to connect the microcomputer pins to unassigned pins (within 2 cm).
- P70 and P71 must output low-level ("L") signals if they are in output mode. They are ports for the N-channel open drain outputs.
- When the external clock is applied to the XIN pin, set the pin as written above.
- In the 100-pin package, set "FF16" in the following addresses, in addition to the above settings:
Addresses 0003CB16, 0003CE16, 0003CF16, 0003D216, 0003D316

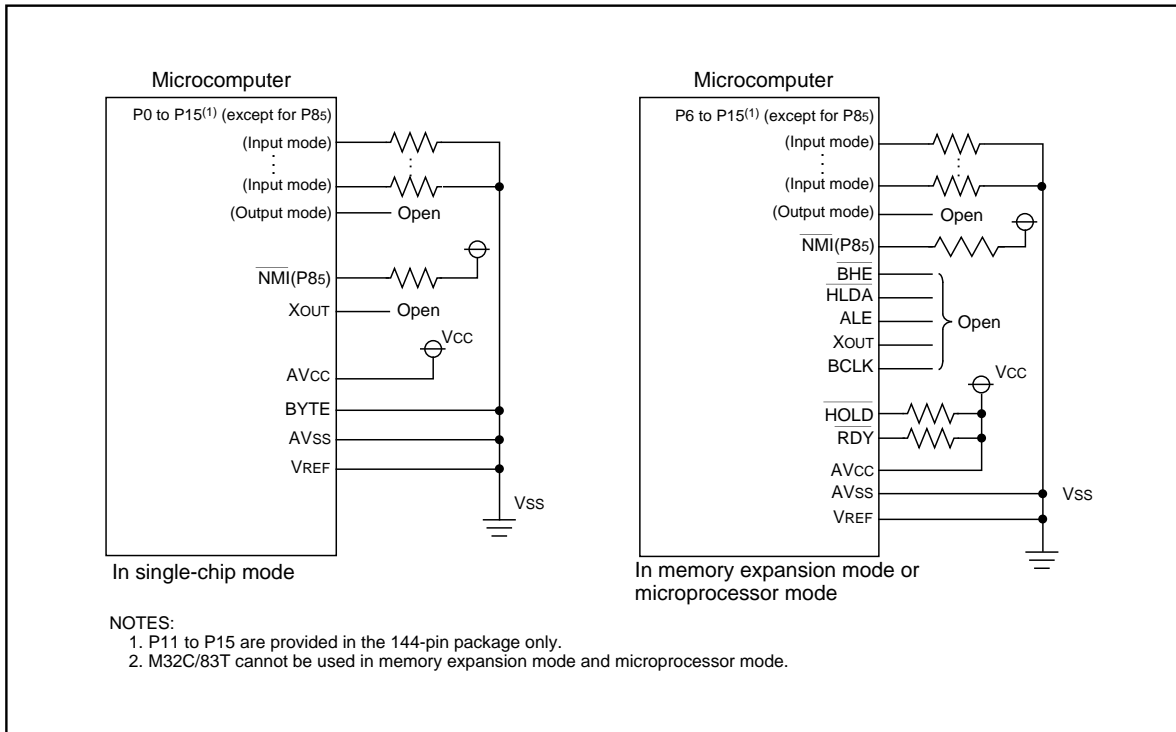


Figure 24.19 Unassigned Pin Handling

Table 24.3 Port P6 Peripheral Function Output Control

	PS0 Register	PSL0 Register
Bit 0	0: P60/CTS0/SS0 1: RTS0	Set to "0"
Bit 1	0: P61/CLK0 (input) 1: CLK0 (output)	Set to "0"
Bit 2	0: P62/RxD0/SCL0 (input) 1: Selected by the PSL0 register	0: SCL0 (output) 1: STxD0
Bit 3	0: P63/SRxD0/SDA0 (input) 1: TxD0/SDA0 (output)	Set to "0"
Bit 4	0: P64/CTS1/SS1/ISCLK2 (input) 1: Selected by the PSL0 register	0: RTS1 1: OUT21/ISCLK2(output)
Bit 5	0: P65/CLK1(input) 1: CLK1(output)	Set to "0"
Bit 6	0: P66/RxD1/SCL1 (input) 1: Selected by the PSL0 register	0: SCL1(output) 1: STxD1
Bit 7	0: P67/SRxD1/SDA1 (input) 1: TxD1/SDA1 (output)	Set to "0"

Table 24.4 Port P7 Peripheral Function Output Control

	PS1 Register	PSL1 Register	PSC Register ⁽¹⁾
Bit 0	0: P70/SRxD2/TA0OUT(input)/ SDA2(input) 1: Selected by the PSL1 register	0: Selected by the PSC register 1: TA0OUT(output)	0: TxD2/SDA2(output) 1: OUTC20/ISTxD2/IEOUT
Bit 1	0: P71/TB5IN/TA0IN/RxD2/ISRxD2/IEIN/ SCL2(input) 1: Selected by the PSL1 register	0: Selected by the PSC register 1: STxD2	0: SCL2(output) 1: OUTC22
Bit 2	0: P72/TA1OUT(input)/CLK2(input) 1: Selected by the PSL1 register	0: Selected by the PSC register 1: TA1OUT(output)	0: CLK2(output) 1: V
Bit 3	0: P73/TA1IN/CTS2/SS2 1: Selected by the PSL1 register	0: Selected by the PSC register 1: V	0: RTS2 1: OUTC10/ISTxD1/BE1OUT
Bit 4	0: P74/INPC11/ISCLK1(input)/TA2OUT(input) 1: Selected by the PSL1 register	0: Selected by the PSC register 1: W	0: TA2OUT(output) 1: OUTC11/ISCLK1(output)
Bit 5	0: P75/TA2IN/INPC12/ISRxD1/BE1IN 1: Selected by the PSL1 register	0: W 1: OUTC12	Set to "0"
Bit 6	0: P76/INPC00/TA3OUT(input) 1: Selected by the PSL1 register	0: Selected by the PSC register 1: TA3OUT(output)	0: OUTC00/ISTxD0/BE0OUT 1: CAN0OUT
Bit 7	0: P77/TA3IN/CANIN/ISCLK0(input)/INPC01 1: OUTC01/ISCLK0(output)	Set to "0"	0: P104 to P107 or K10 to K13 1: AN4 to AN7 (No relation to P77)

NOTES:

1. Set the corresponding PSC_i bit to "0" when setting the PSL1_i bit (i=0 to 4, 6) to "1".

Table 24.5 Port P8 Peripheral Function Output Control

	PS2 Register	PSL2 Register
Bit 0	0: P8 ₀ /INPC0 ₂ /ISRxD0/BE0 _{OUT} /TA4 _{OUT} (input) 1: Selected by the PSL2 register	0: TA4 _{OUT} (output) 1: U
Bit 1	0: P8 ₁ /TA4 _{IN} 1: Selected by the PSL2 register	0: U 1: OUTC3 ₂ /ISTxD3
Bit 2	0: P8 ₂ /INT0/ISRxD3 1: Selected by the PSL2 register	0: OUTC3 ₂ 1: CAN _{OUT}
Bit 3 to 7	Set to "0"	

Table 24.6 Port P9 Peripheral Function Output Control

	PS3 Register	PSL3 Register
Bit 0	0: P9 ₀ /TB0 _{IN} /CLK3(input) 1: CLK3(output)	Set to "0"
Bit 1	0: P9 ₁ /TB1 _{IN} /RxD3/ISRxD2/SCL3(input)/IE _{IN} 1: Selected by the PSL3 register	0: SCL3(output) 1: STxD3
Bit 2	0: P9 ₂ /TB2 _{IN} /SRxD3/SDA3(input) 1: Selected by the PSL3 register	0: TxD3/SDA3(output) 1: OUTC2 ₀ /ISTxD2/IE _{IN}
Bit 3	0: P9 ₃ /TB3 _{IN} /CTS3/SS3/DA0(output) 1: RTS3	0: Except DA0 1: DA0
Bit 4	0: P9 ₄ /TB4 _{IN} /CTS4/SS4/DA1(output) 1: RTS4	0: Except DA1 1: DA1
Bit 5	0: P9 ₅ /ANEX0/CLK4(input) 1: CLK4(output)	0: Except ANEX0 1: ANEX0
Bit 6	0: P9 ₆ /SRxD4/ANEX1/SDA4(input) 1: TxD4/SDA4(output)	0: Except ANEX1 1: ANEX1
Bit 7	0: P9 ₇ /RxD4/ADTRG/SCL4(input) 1: Selected by the PSL3 register	0: SCL4(output) 1: STxD4

Table 24.7 Port P10 Peripheral Function Output Control

	PSC Register
Bit 7	0: P10 ₄ to P10 ₇ or KI ₀ to KI ₃ 1: AN ₄ to AN ₇

Table 24.8 Port P11 Peripheral Function Output Control

	PS5 Register
Bit 0	0: P110 1: OUTC10/ISTxD1/BE1OUT
Bit 1	0: P111/INPC11/ISCLK1(input) 1: OUTC11/ISCLK1(output)
Bit 2	0: P112/INPC12/ISRxD1/BE1IN 1: OUTC12
Bit 3	0: P113 1: OUTC13
Bit 4 to 7	Set to "0"

Table 24.9 Port P12 Peripheral Function Output Control

	PS6 Register
Bit 0	0: P120 1: OUTC30/ISTxD3
Bit 1	0: P121/ISCLK3(input) 1: OUTC31/ISCLK3(output)
Bit 2	0: P122/ISRxD3 1: OUTC32
Bit 3	0: P123 1: OUTC33
Bit 4	0: P124 1: OUTC34
Bit 5	0: P125 1: OUTC35
Bit 6	0: P126 1: OUTC36
Bit 7	0: P127 1: OUTC37

Table 24.10 Port P13 Peripheral Function Output Control

	PS7 Register
Bit 0	0: P130 1: OUTC24
Bit 1	0: P131 1: OUTC25
Bit 2	0: P132 1: OUTC26
Bit 3	0: P133 1: OUTC23
Bit 4	0: P134 1: OUTC20/ISTxD2/IEOUT
Bit 5	0: P135/ISRxD2/IEIN 1: OUTC22
Bit 6	0: P136/ISCLK2(input) 1: OUTC21/ISCLK2(output)
Bit 7	0: P137 1: OUTC27

Table 24.11 Port P14 Peripheral Function Output Control

	PS8 Register
Bit 0	0: P140 1: OUTC14
Bit 1	0: P141 1: OUTC15
Bit 2	0: P142/INPC16 1: OUTC16
Bit 3	0: P143/INPC17 1: OUTC17
Bit 4 to 7	Set to "0"

Table 24.12 Port P15 Peripheral Function Output Control

	PS9 Register
Bit 0	0: P150/INPC00/AN150 1: OUTC00/ISTxD0/BE0OUT
Bit 1	0: P151/INPC01/AN151/ISCLK0(input) 1: OUTC01/ISCLK0(output)
Bit 2 to 3	Set to "0"
Bit 4	0: P154/INPC04/AN154 1: OUTC04
Bit 4	0: P155/INPC05/AN155 1: OUTC05
Bit 6 to 7	Set to "0"

25. Flash Memory Version

Aside from the built-in flash memory, the flash memory version microcomputer has the same functions as the masked ROM version.

In the flash memory version, rewrite operations to the flash memory can be performed in three modes: CPU rewrite mode, standard serial I/O mode and parallel I/O mode.

Table 25.1 lists specifications of the flash memory version. See **Tables 1.1 and 1.2** for the items not listed in Table 25.1.

Table 25.1 Flash Memory Version Specifications

Item		Specification
Supply Voltage		4.2V to 5.5V (f(XIN) = 32MHz, no wait) 3.0V to 5.5V (f(XIN) = 20MHz, no wait)
Program and Erase Voltage		4.2V to 5.5V (through VDC), 3.0V to 3.6V (not through VDC) CPU clock=12.5MHz (1 wait state), CPU clock=6.25MHz (no wait)
Flash Memory Rewrite Mode		3 modes (CPU rewrite, standard serial I/O, parallel I/O)
Erase Block	User ROM Area	See Figure 25.1
	Boot ROM Area	1 block (8 Kbytes) ⁽¹⁾
Program Method		Per page (256 bytes)
Erase Method		All block erase, erase per block
Program and Erase Control Method		Software commands control programming and erasing on the flash memory
Protect Method		The lock bit protects each block in the flash memory
Number of Commands		8 commands
Program and Erase Endurance		100 cycles ⁽³⁾
Data Retention		10 years
ROM Code Protection		Standard serial I/O mode and parallel I/O mode supported

NOTES:

1. The rewrite control program for standard serial I/O mode is stored in the boot ROM area before shipment. This space can be rewritten in parallel I/O mode only.

Table 25.2 Flash Memory Rewrite Mode Overview

Flash Memory Rewrite Mode	CPU Rewrite Mode	Standard Serial I/O Mode	Parallel I/O Mode
Function	Software command execution by CPU rewrites the user ROM area.	A dedicated serial programmer rewrites the user ROM area. Standard serial I/O mode 1: Clock synchronous serial I/O Standard serial I/O mode 2: UART	A dedicated parallel programmer rewrites the boot ROM area and user ROM area.
Space which can be Rewritten	User ROM area	User ROM area	User ROM area Boot ROM area
Operating Mode	Single-chip mode Memory expansion mode Boot mode	Boot mode	Parallel I/O mode
Programmer	None	Serial programmer	Parallel programmer

25.1 Memory Map

The flash memory contains a user ROM area, with space to store microcomputer operating programs in single-chip mode or memory expansion mode, and a separate 8-Kbyte boot ROM area. Figure 25.1 shows a block diagram of the flash memory.

The user ROM area is divided into several blocks, each of which can be protected (locked) from program and erase. The user ROM area can be rewritten in CPU rewrite, standard serial I/O and parallel I/O modes. The boot ROM area is allocated in the same addresses as the user ROM area. It can only be rewritten in parallel I/O mode (refer to **25.5 Parallel I/O Mode**). A program in the boot ROM area is executed after a hardware reset occurs while an "H" signal is applied to the CNVss and P50 pins and an "L" signal is applied to the P55 pin (refer to **25.1.1 Boot Mode**). A program in the user ROM area is executed after a hardware reset occurs while an "L" signal is applied to the CNVss pin. Consequently, the boot ROM area cannot be read.

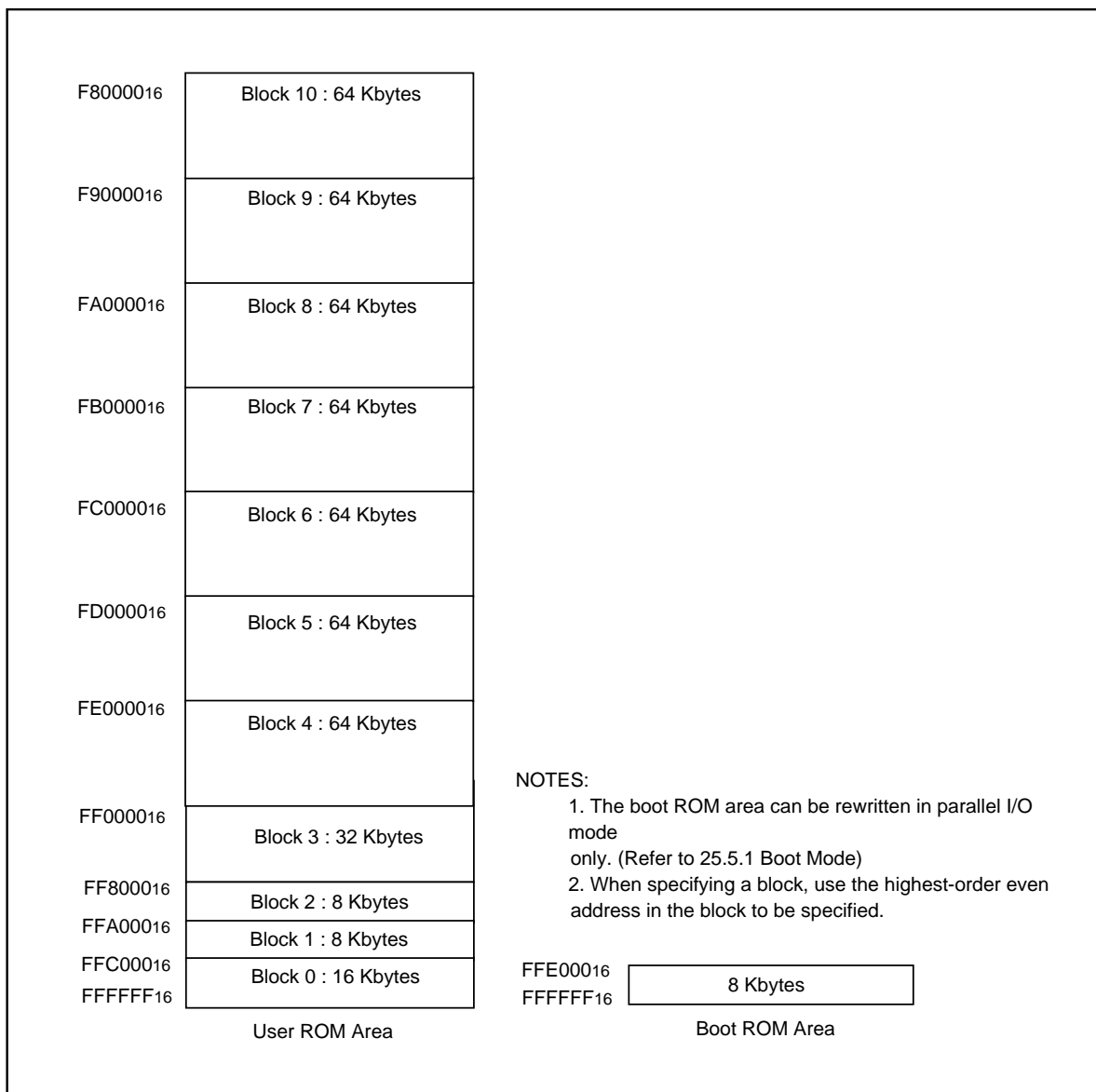


Figure 25.1 Flash Memory Block Diagram

25.1.1 Boot Mode

The microcomputer enters boot mode when a hardware reset is performed while an "H" signal is applied to the CNVss and P50 pins and an "L" signal is applied to the P55 pin. The program in the boot ROM area is executed.

In boot mode, the FMR05 bit in the FMR0 register selects access to either the boot ROM area or the user ROM area.

The rewrite control program for standard serial I/O mode (refer to **25.4 Standard Serial I/O Mode**) is stored in the boot ROM area before shipment.

The boot ROM area can be rewritten in parallel I/O mode only. If any rewrite control program using erase-write mode is written in the boot ROM area, the flash memory can be rewritten according to the system implemented.

25.2 Functions to Prevent the Flash Memory from Rewriting

The flash memory has the ROM code protect function for parallel I/O mode and the ID code verify function for standard I/O mode to prevent the flash memory from reading or rewriting.

25.2.1 ROM Code Protect Function

The ROM code protect function prevents the flash memory from reading and rewriting in parallel I/O mode. Figure 25.2 shows the ROMCP register. The ROMCP register is located in the user ROM area.

The ROM code protect function is enabled when the ROMCP1 bit is set to "002". The ROM code protect function is disabled when the ROMCR bit is set to "002", regardless of the ROMCP1 bit setting.

Therefore, set the ROMCR bit to "112" and the ROMCP1 bit to "002" when setting up the ROM code protect function.

Once the ROM code protect function is enabled, the ROMCR bit cannot be changed in parallel I/O mode. Rewrite the ROMCR bit to "002" in standard serial I/O mode or CPU rewrite mode when disabling the ROM code protect function.

25.2.2 ID Code Verify Function

Use the ID code verify function in standard serial I/O mode. The ID code sent from the serial programmer is compared with the ID code written in the flash memory for a match. If the ID codes do not match, commands sent from the serial programmer are not accepted. However, if the four bytes of the reset vector are "FFFFFFFF₁₆", ID codes are not compared, and all commands are accepted.

The ID codes are 7-byte data stored consecutively, starting with the first byte, into addresses 0FFFFFFD₁₆, 0FFFFFFE3₁₆, 0FFFFFFEB₁₆, 0FFFFFFEF₁₆, 0FFFFFFF3₁₆, 0FFFFFFF7₁₆ and 0FFFFFFFB₁₆. The flash memory must have a program with the ID codes set in these addresses.

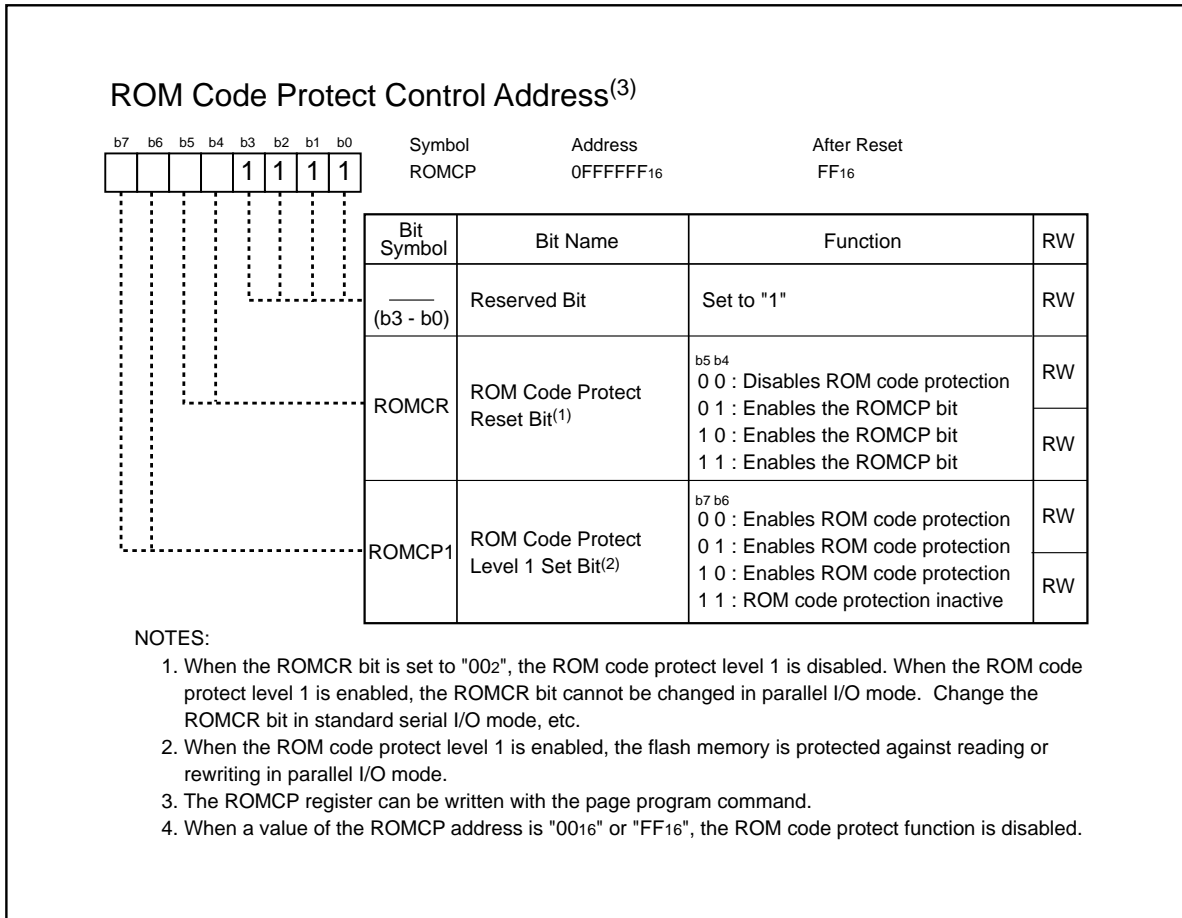


Figure 25.2 ROMCP Register

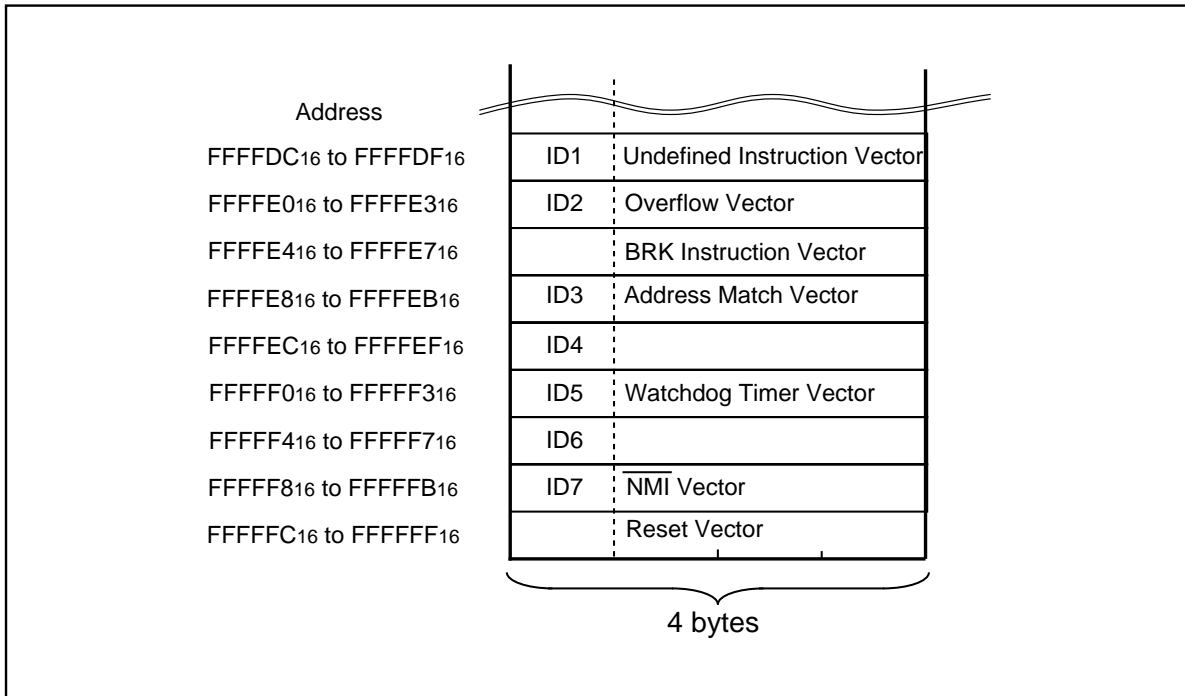


Figure 25.3 Address to Store ID Code

25.3 CPU Rewrite Mode

In CPU rewrite mode, the user ROM area can be rewritten when the CPU executes software commands. The user ROM area can be rewritten with the microcomputer mounted on a board, without using a parallel or serial programmer.

Write the rewrite control program to either the user ROM area or the boot ROM area, beforehand. No program in the flash memory can be executed in CPU rewrite mode. Therefore, transfer rewrite control program to an area other than flash memory (internal RAM, etc.), and execute.

CPU rewrite mode can be entered when the microcomputer is in single-chip, memory expansion, and boot mode.

Software commands, listed in Table 25.3, can be used in CPU rewrite mode. Refer to **25.3.3 Software Command** for details of each command.

Read or write commands and data from or to even addresses in the user ROM area, in 16-bit units. The 8 high-order bits (D₁₅ to D₈) are ignored when writing command codes.

Table 25.3 Software Commands

Software Command	First Bus Cycle			Second Bus Cycle			Third Bus Cycle		
	Mode	Address	Data (D ₁₅ to D ₀)	Mode	Address	Data (D ₁₅ to D ₀)	Mode	Address	Data (D ₁₅ to D ₀)
Read Array	Write	X	xxFF ₁₆						
Read Status Register	Write	X	xx70 ₁₆	Read	X	SRD			
Clear Status Register	Write	X	xx50 ₁₆						
Page Program	Write	X	xx41 ₁₆	Write	WA	WD	Write	WA+2	WD
Block Erase	Write	X	xx20 ₁₆	Write	BA	xxD0 ₁₆			
Erase All Unlocked Block	Write	X	xxA7 ₁₆	Write	X	xxD0 ₁₆			
Lock Bit Program	Write	X	xx77 ₁₆	Write	BA	xxD0 ₁₆			
Read Lock Bit Status	Write	X	xx71 ₁₆	Read	BA	D ₆			

SRD: Data in the SRD register (D₇ to D₀)

WA: Address to be written (Increment A₇ to A₀ by 2 from "00₁₆" to "FE₁₆".)

WD: 16-bit write data

BA: Highest-order block address (A₀ = 0)

D₆: Lock bit (D₆=1: unlock, D₆=0: locked)

X: Any even address in the user ROM area (A₀ = 0)

xx: 8 high-order bits of command code (ignored)

25.3.1 Flash Memory Control Register 0 (FMR0 Register)

Figure 25.4 shows the FMR0 register.

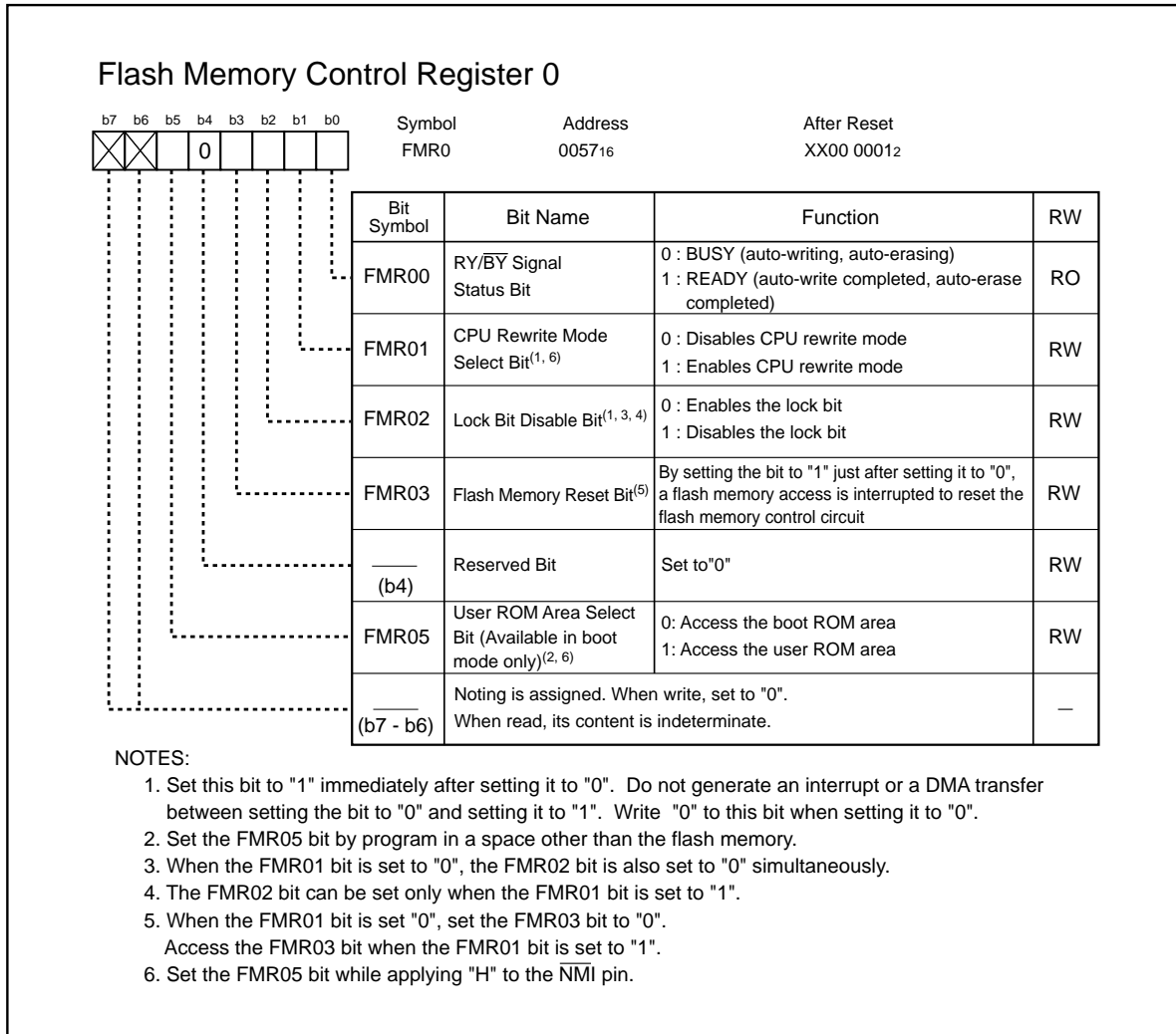


Figure 25.4 FMR0 Register

25.3.1.1 FMR00 Bit

The FMR00 bit indicates the write status machine (WSM) operation state during an auto write and auto erase operation. The FMR00 bit is set to "0" during an auto write or auto erase operation and is set to "1" when an auto write or auto erase operation is completed. The FMR00 bit changes while executing the page program, block erase, erase all unlocked block or lock bit program command. Determine whether the auto write or erase operation is completed by reading the FMR00 bit. The FMR00 bit is changed by the above commands only.

25.3.1.2 FMR01 Bit

Commands can be accepted when the FMR01 bit is set to "1" (CPU rewrite mode). To set the FMR01 bit to "1", set to "1" immediately after setting it to "0". To set the FMR01 bit to "0", set it to "0".

CPU rewrite mode is entered by setting the FMR01 bit to "1" and programs in the flash memory cannot be executed. Execute an instruction written to this bit in a space (internal RAM, etc.) other than the flash memory.

If a command for CPU rewrite mode is executed in boot mode, set the FMR05 bit to "1" (user ROM area access).

25.3.1.3 FMR02 Bit

The lock bit set for each block can be disabled by setting the FMR02 bit to "1" (lock bit disabled). (Refer to **25.3.3 Data Protect Function.**) The lock bit is enabled by setting the FMR02 bit to "0" (lock bit enabled). The FMR02 bit can be set when the FMR01 bit is set to "1". To set the FMR02 bit to "1", set it to "1" immediately after setting it to "0". To set the FMR02 bit to "0", set it to "0".

The FMR02 bit does not change the lock bit state, but disables the lock bit function. If the block erase or erase all unlocked block command is executed while the FMR02 bit is set to "1", the lock bit state changes "0" (locked) to "1" (unlocked) after command execution is completed.

25.3.1.4 FMR03 Bit

By setting the FMR03 bit to "0" following "1", access to the user ROM area is interrupted to reset the flash memory control circuit. The flash memory enters read array mode after reset. The FMR00 bit is set to "1" (READY) and the Status register is set to "8016". (Refer to **25.3.2 Status Register.**)

When the FMR03 bit resets the flash memory control circuit during an auto write or auto erase operation, an auto write or auto erase operation is interrupted. Data in the block is invalid.

To set the FMR03 bit to "0", set it to "0" immediately after setting it to "1".

25.3.1.5 FMR05 Bit

The FMR05 bit selects the boot ROM or user ROM area in boot mode. Set to "0" to access (read) the boot ROM area or to "1" (user ROM access) to access (read, write or erase) the user ROM area. Execute an instruction written to the FMR05 bit in a space (internal RAM, etc.) other than the flash memory.

In modes other than boot mode, the user ROM area is accessed (read) regardless of the FMR05 bit setting.

25.3.2 Status Register

The write state machine (WSM) in the flash memory controls programming and erasing of the flash memory. The status register indicates whether or not the WSM is operating as expected, and whether or not a program or erase operation is completed as expected. Refer to **25.3.6 Full Status Check** for details on each error.

Table 25.4 lists the status register.

The status register can be read by the read status command (Refer to **25.3.5 Software Command**).

Table 25.4 Status Register

Symbol	Status Name	Definition	
		0	1
SR0 (D0)	Reserved bit	-	-
SR1 (D1)	Reserved bit	-	-
SR2 (D2)	Reserved bit	-	-
SR3 (D3)	Block status after program	Completed as expected	Error (excessive write error)
SR4 (D4)	Program status	Completed as expected	Error (program error)
SR5 (D5)	Erase status	Completed as expected	Error (erase error)
SR6 (D6)	Reserved bit	-	-
SR7 (D7)	Write state machine (WSM) status	BUSY	READY

D7 to D0 : These data bus are read when the read status register command is executed.

25.3.2.1 Block Status After Program (SR3)

The SR3 bit is set to "1" when a page program command execution is completed with an excessive write error. The SR3 bit is set to "0" when the clear status command is executed.

The SR3 bit is set to "0" after reset or after setting the FMR03 bit to "0" following "1".

25.3.2.2 Program Status (SR4)

The SR4 bit is set to "1" when a program error occurs while the page program or lock bit program command is being executed. The SR4 bit is set to "0" when the clear status command is executed.

The SR4 bit is set to "0" after reset or after setting the FMR03 bit to "0" following "1".

25.3.2.3 Erase Status (SR5)

The SR5 bit is set to "1" when an erase error occurs while the block erase or erase all unlocked block command is being executed. The SR5 bit is set to "0" when the clear status command is executed.

The SR5 bit is set to "0" after reset or after setting the FMR03 bit to "0" following "1".

25.3.2.4 Write State Machine (WSM) Status (SR7)

The SR7 bit indicates the WSM operation state. The SR7 bit is set to "0" during auto write or auto erase and to "1" when an auto write or auto erase operation is completed. The SR7 bit changes while the page program, block erase, erase all unlocked block or lock bit program command is being executed. The SR7 bit changes with the above commands only. The SR7 bit is set to "1" after reset or after setting the FMR03 bit to "0" following "1".

The FMR00 bit indicates the WSM status. Read the FMR00 bit to determine whether the auto write or erase operation is completed.

25.3.3 Data Protect Function

Each block in the flash memory has a nonvolatile lock bit. The lock bit is enabled by setting the FMR02 bit to "0" (lock bit enabled). The lock bit individually protects (locks) each block against program and erase. This prevents data from being inadvertently written to or erased from the flash memory.

- When the lock bit status is set to "0", the block is locked (block is protected against program and erase).
- When the lock bit status is set to "1", the block is not locked (block can be programmed or erased).

The lock bit status is set to "0" (locked) by executing the lock bit program command and to "1" (unlocked) by erasing the block. The lock bit status cannot be set to "1" by any commands.

The lock bit status can be read by the read lock bit status command.

The lock bit function is disabled by setting the FMR02 bit to "1". All blocks are unlocked. However, individual lock bit status remains unchanged. The lock bit function is enabled by setting the FMR02 bit to "0". Lock bit status is retained.

If the block erase or erase all unlocked block command is executed while the FMR02 bit is set to "1", the target block or all blocks are erased regardless of lock bit status. The lock bit status of each block is set to "1" after an erase operation has been completed.

Refer to **25.3.5 Software Commands** for details on each command.

25.3.4 How to Enter and Exit CPU Rewrite Mode

Figure 25.5 shows how to enter and exit CPU rewrite mode.

No program in the flash memory can be executed in CPU rewrite mode. Execute rewrite control program in a space other than the flash memory (internal RAM, etc.) after transferring the program to that space.

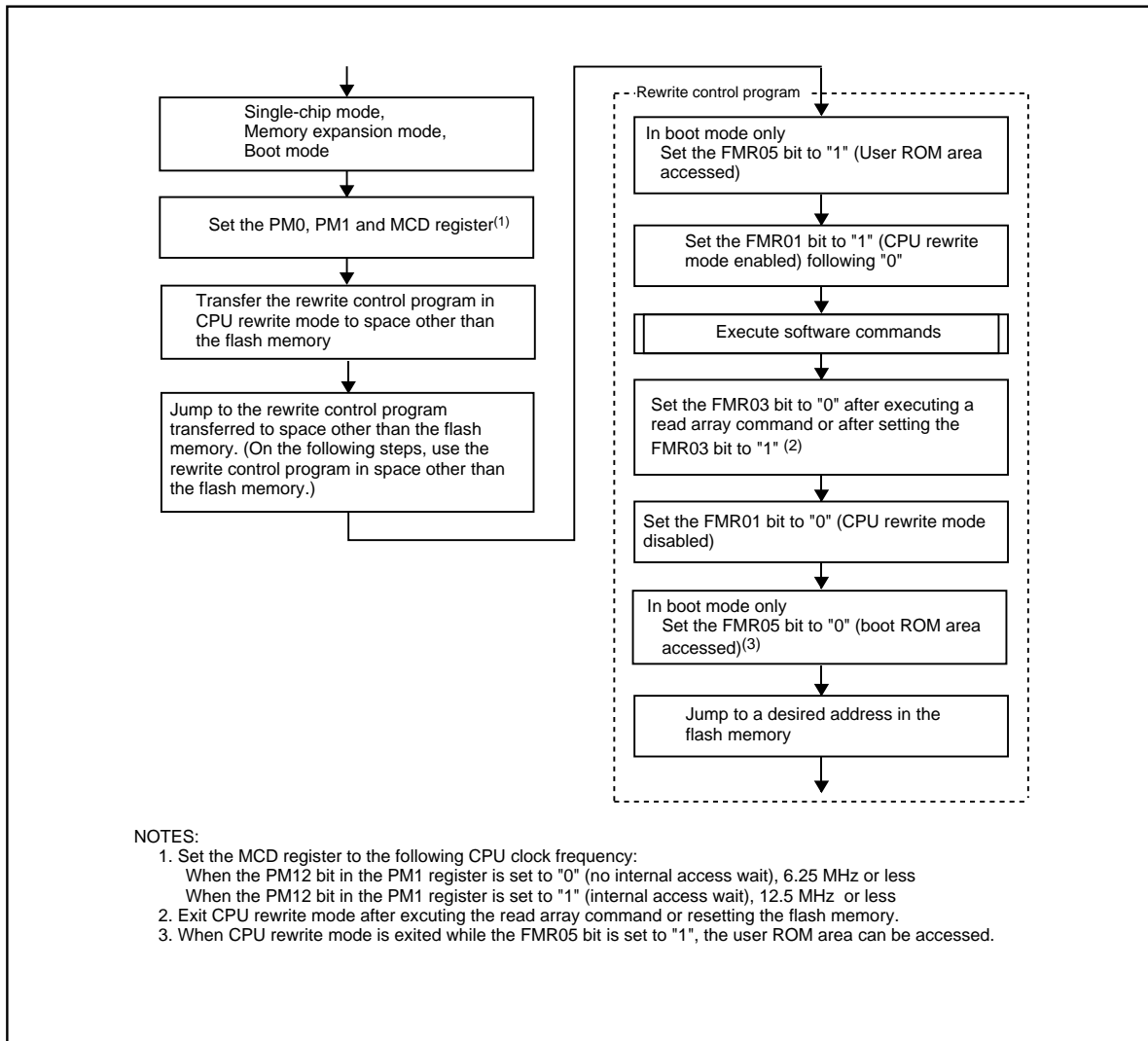


Figure 25.5 How to Enter and Exit CPU Rewrite Mode

25.3.5 Software Commands

Read or write commands and data from or to even addresses in the user ROM area, in 16-bit units. When writing a command code, 8 high-order bits (D15 to D8) are ignored.

25.3.5.1 Read Array Command

The read array command reads the flash memory.

Read array mode is entered by writing command code "xxFF16" in the first bus cycle. Content of a specified address can be read after the next bus cycle.

The microcomputer remains in read array mode until another command is written. Therefore, contents from multiple addresses can be read consecutively.

25.3.5.2 Read Status Register Command

The read status register command reads the status register (refer to **25.3.7 Status Register** for details).

By writing command code "xx7016" in the first bus cycle, the status register can be read in the second bus cycle. Read an even address in the user ROM area.

25.3.5.3 Clear Status Register Command

The clear status register command clears the status register. By writing "xx5016" in the first bus cycle, the SR5 to SR3 bits in the status register (see Table 25.4) are set to "0".

25.3.5.4 Page Program Command

The page program command executes programs in 128-word (256-byte) units.

After writing command code "xx4116" in the first bus cycle, write data to the 2nd through 129th bus cycles in 16-bit units. Increment by two, from "0016" to "FE16", the 8 low-order bits of the write address. Auto write, programming and verification of data, is performed when 128 word data has been written. Do not access the flash memory or execute the next command during auto write operation.

The FMR00 bit in the FMR0 register indicates whether an auto program operation is completed.

After an auto write operation is completed, the Status register indicates whether the auto write operation is completed as expected or not. (Refer to **25.3.6 Full Status Check**.)

Figure 25.6 shows a flow chart of the page program command programming. When programming a space which is already programmed, execute erase (block erase) before programming. If the page program command is executed to a space already programmed, no program error occurs but the page is indeterminate.

The lock bit can protect blocks from being programmed. (Refer to **25.3.3 Data Protect Function**.)

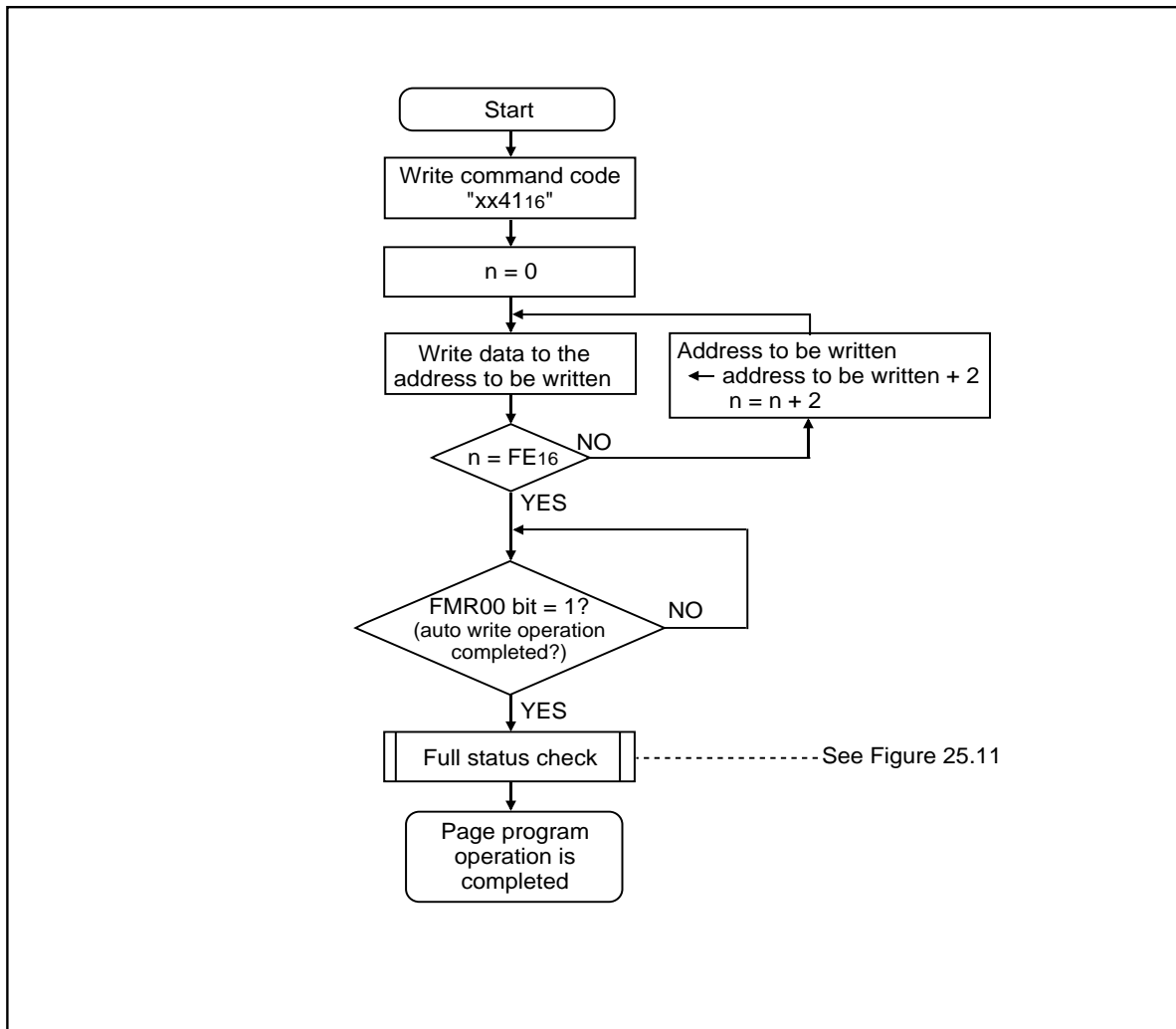


Figure 25.6 Program Command

25.3.5.5 Block Erase Command

The block erase command erases each block.

By writing command code "xx2016" in the first bus cycle and "xxD016" to the highest-order even address of a block in the second bus cycle, an auto erase operation (erase and verify) starts in the specified block. Do not access the flash memory or execute the next command during auto erase operations.

The FMR00 bit in the FMR0 register indicates whether an auto erase operation has been completed. After the completion of an auto erase operation, the Status register indicates whether or not the auto erase operation has been completed as expected. (Refer to **25.3.6 Full Status Check.**)

Figure 25.7 shows a flow chart of the block erase command programming.

The lock bit can protect blocks from being erased. (Refer to **25.3.6 Data Protect Function.**)

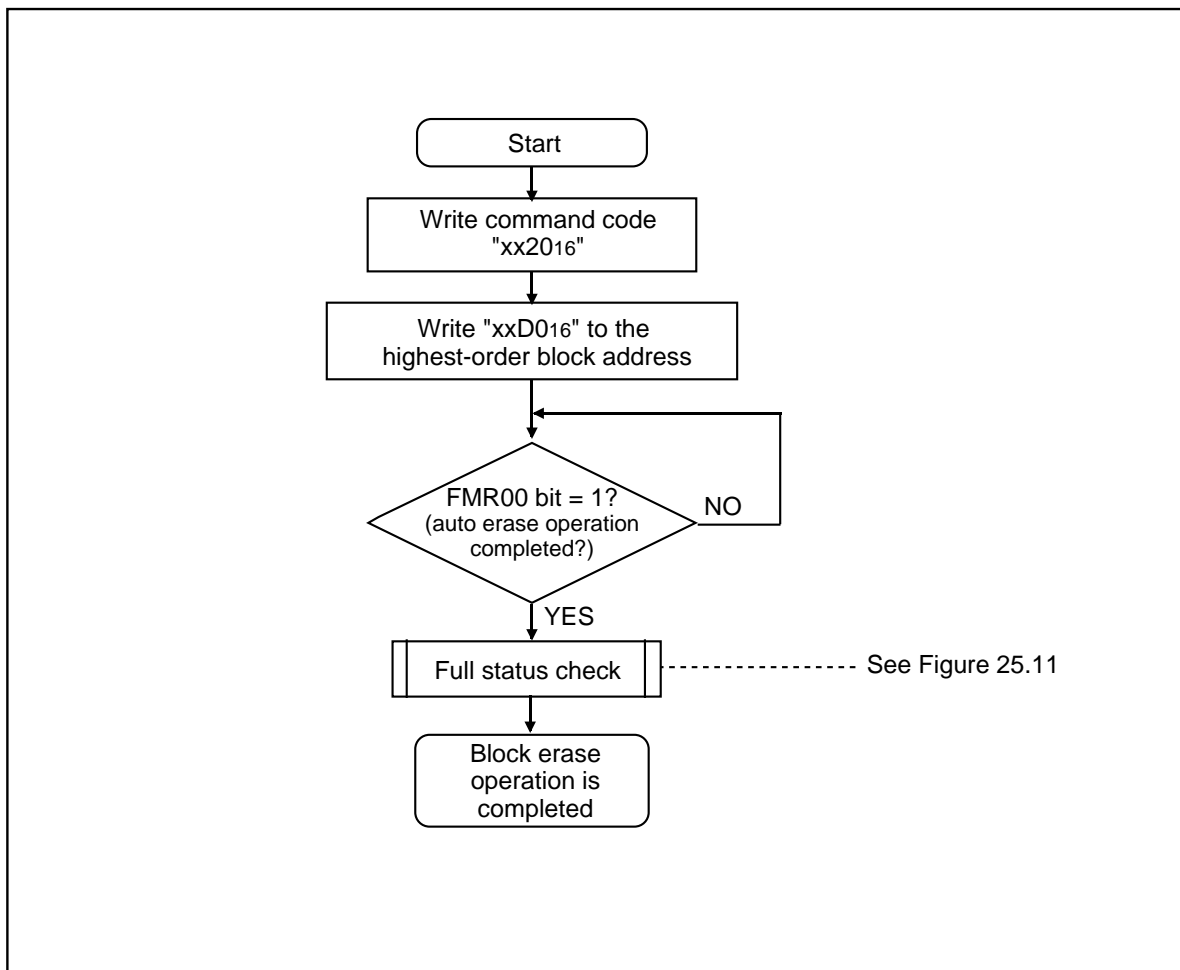


Figure 25.7 Block Erase Command

25.3.5.6 Erase All Unlocked Block Command

By writing command code "xxA716" in the first bus cycle and "xxD016" in the second bus cycle, an auto erase (erase and verify) operation will run in all blocks. Do not access the flash memory or execute the next command during auto erase operations.

The FMR00 bit in the FMR0 register indicates whether an auto erase operation is completed.

After the completion of an auto erase operation, the Status register indicates whether or not the auto erase operation is completed as expected.

Figure 25.8 shows a flow chart of the erase all unlocked block command programming.

The lock bit can protect each block from being erased. (Refer to **25.3.6 Data Protect Function.**)

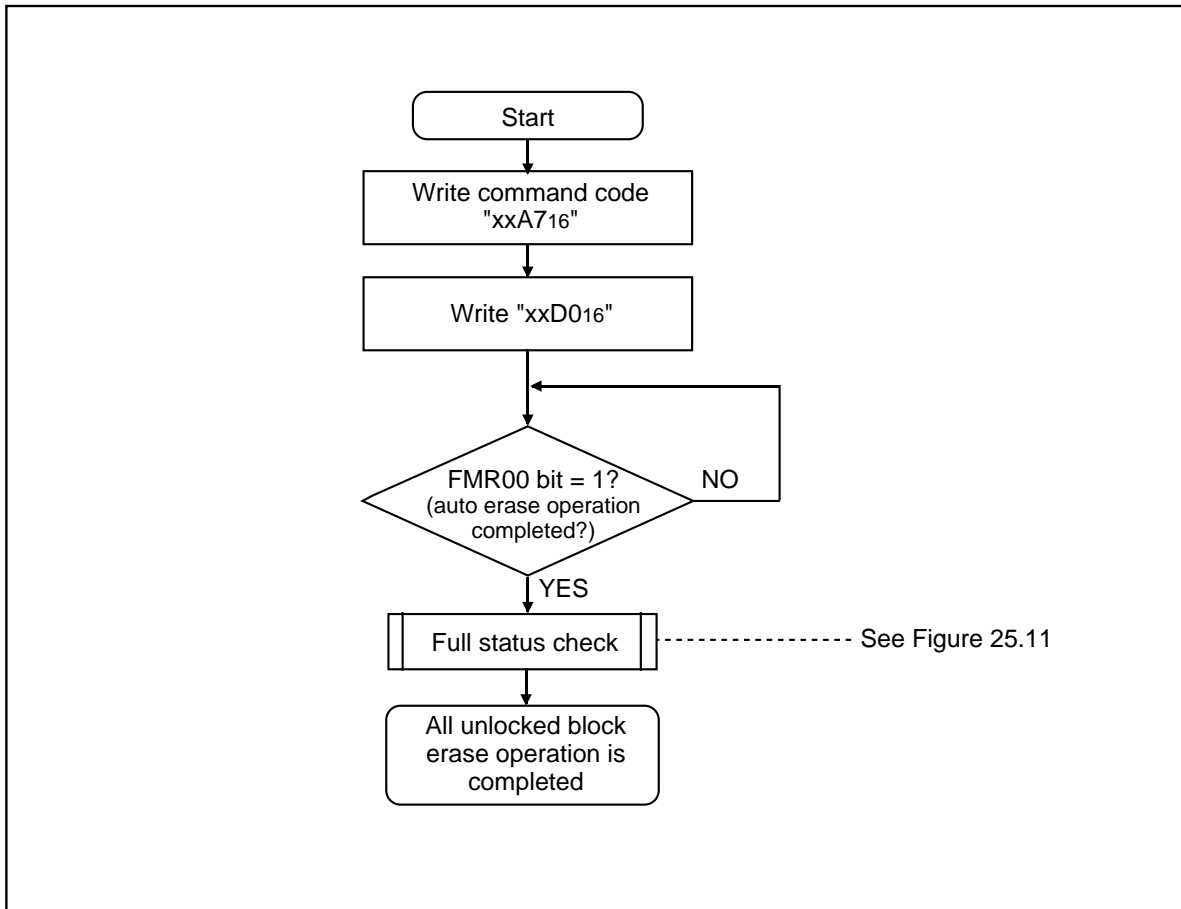


Figure 25.8 Erase All Unlocked Block Command

25.3.5.7 Lock Bit Program Command

The lock bit program command sets the lock bit for a specified block to "0" (locked).

By writing command code "xx7716" in the first bus cycle and "xxD016" to the highest-order even address of a block in the second bus cycle, auto write operation starts, and the lock bit for the specified block is set to "0". Do not access the flash memory or execute the next instructions during the lock bit program operation.

The FMR00 bit in the FMR0 register indicates whether or not the lock bit program operation has been completed. After the completion of a lock bit program operation, the Status register indicates whether or not the operation has been completed as expected. (Refer to **25.3.6 Full Status Check.**)

Figure 25.9 shows a flow chart of the lock bit program command programming.

Refer to **25.3.6 Data Protect Function** for details on how to set the lock bit function to "0" (unlocked).

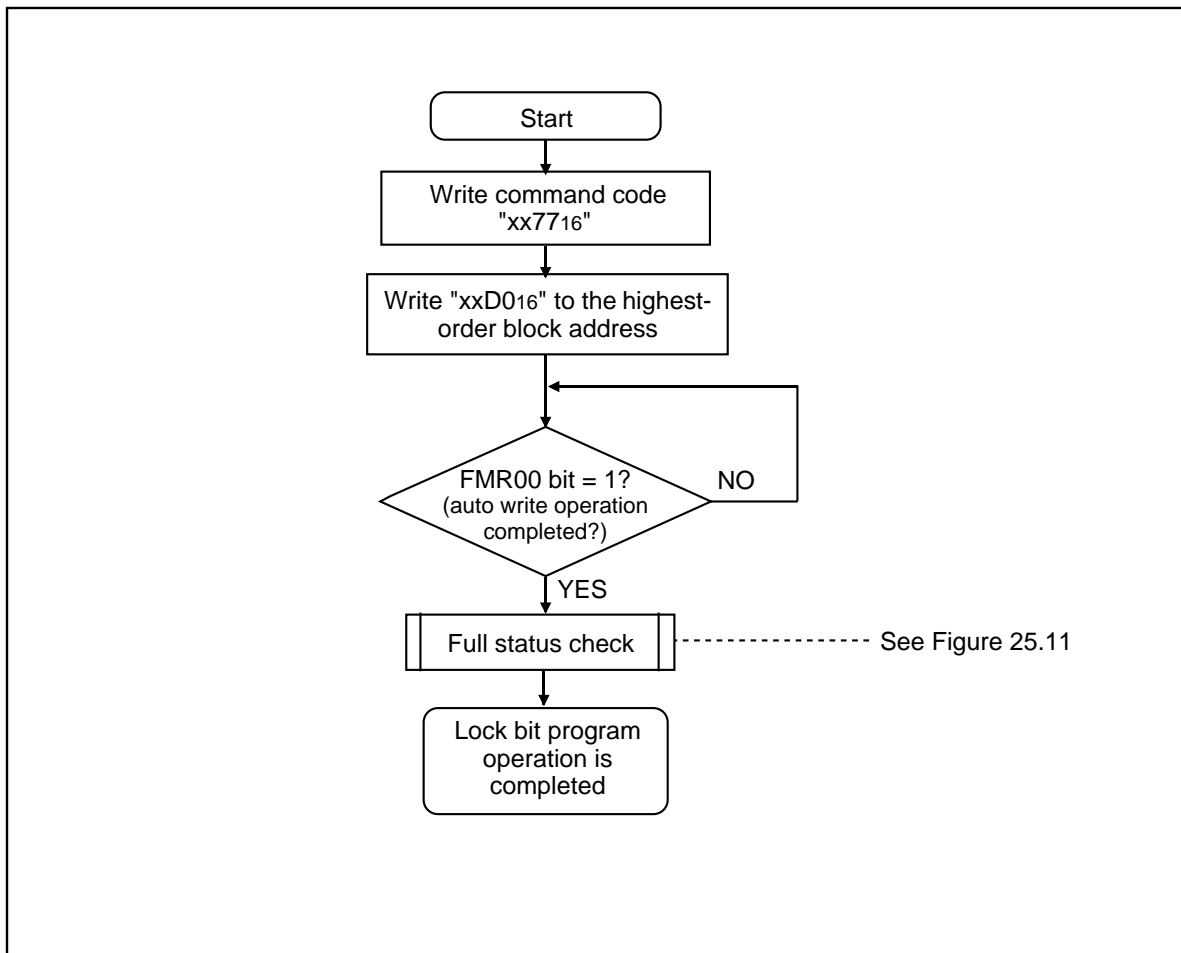


Figure 25.9 Lock Bit Program Command

25.3.5.8 Read Lock Bit Status Command

The read lock bit status command reads the lock bit state of a specified block.

By writing command code "xx7116" in the first bus cycle and reading the highest-order address (however, A0=0) of a block in the second bus cycle, the lock bit state information of a specified block is read out to the data bus (D6).

Figure 25.10 shows a flow chart of the read lock bit status command programming.

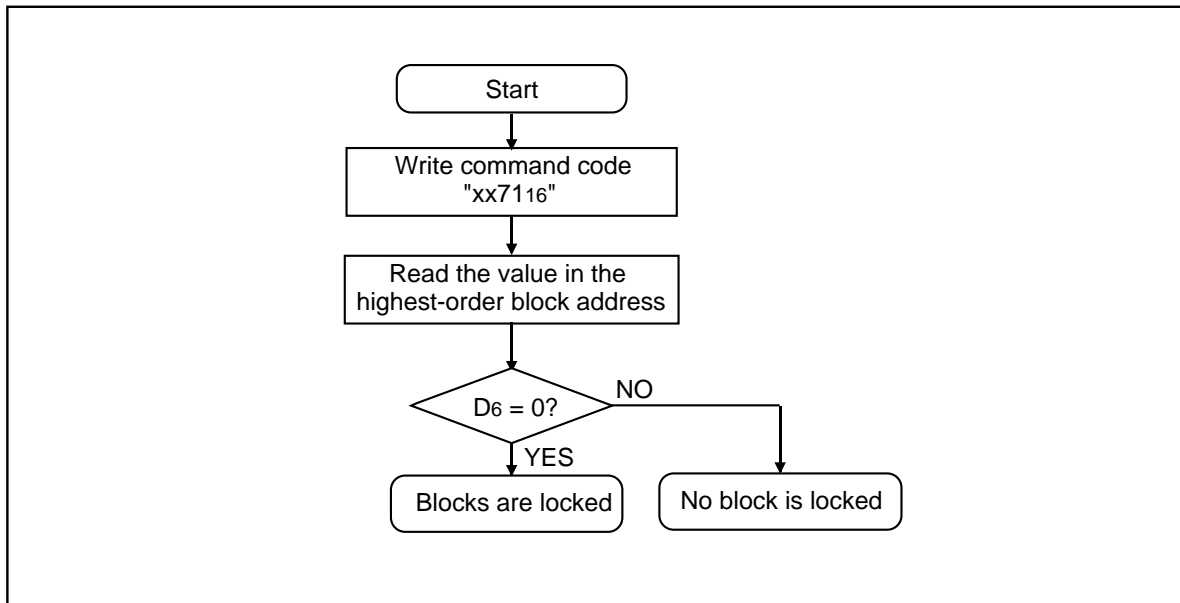


Figure 25.10 Read Lock Bit Status Command

25.3.6 Full Status Check

If an error occurs when a program or erase operation is completed, the SR3 to SR5 bits in the status register are set to "1", indicating a specific error. Therefore, execution results can be confirmed by verifying these bits (full status check).

Table 25.5 lists errors and status register state. Figure 25.12 shows a flow chart of the full status check and handling procedure for each error.

Table 25.5 Errors and Status Register State

Status Register			Error	Error Occurrence Conditions
SR5	SR4	SR3		
1	1	0	Command sequence error	<ul style="list-style-type: none"> An incorrect command is written A value other than "xD016" or "xFF16" is written in the second bus cycle of the lock bit program, block erase or erase all unlocked block command⁽¹⁾
1	0	0	Erase error	<ul style="list-style-type: none"> The block erase command is executed on a locked block² The block erase or erase all unlocked block command is executed on an unlock block but the erase operation is not completed as expected
0	1	0	Program error	<ul style="list-style-type: none"> The page program command is executed on a locked block⁽²⁾ The page program command is executed in an unlocked block but the program operation is not completed as expected The lock bit program command is executed but the program operation is not completed as expected
0	0	1	Excessive write error	Excessive write occurs after the page program command is executed

NOTES:

- The flash memory enters read array mode when command code "xFF16" is written in the second bus cycle of these commands. The command code written in the first bus cycle becomes invalid.
- If the FMR02 bit is set to "1" (lock bit disabled), no error occurs even under the conditions listed above.

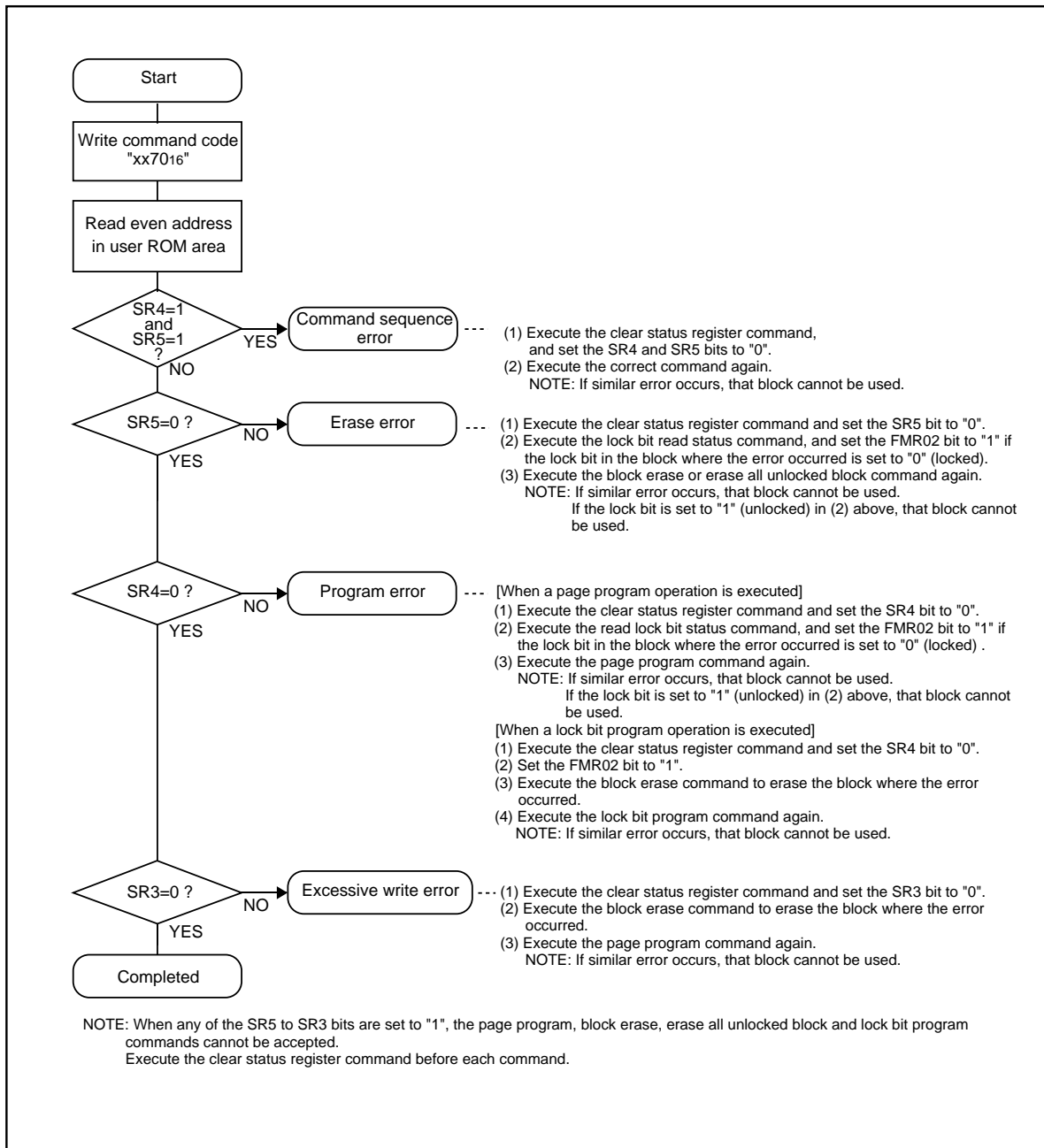


Figure 25.11 Full Status Check and Handling Procedure for Each Error

25.3.7 Precautions in CPU Rewrite Mode

25.3.7.1 Operating Speed

Set the MCD register to the following CPU clock before entering CPU rewrite mode .

When the PM12 bit in the PM register is set to "0" (no wait state), 6.25MHz or less

When the PM12 bit in the PM register is set to "1" (wait state), 12.5MHz or less

25.3.7.2 Prohibited Instructions

In CPU rewrite mode, programs cannot be executed, nor can interrupt vectors be read in the flash memory. Execute the rewrite control program after the program is transferred to a space other than the flash memory. (See **Figure 25.5**.)

The following instructions cannot be used because the CPU tries to read data in the flash memory: the UND instruction, INTO instruction, JMPS instruction, JSRS instruction and BRK instruction.

25.3.7.3 Interrupts

- To use interrupts having vectors in a relocatable vector table, the vectors must be relocated to the RAM area.
- The $\overline{\text{NMI}}$ and watchdog timer interrupts are available since the FMR01 is forcibly reset when either interrupt occurs. Allocate the jump addresses for each interrupt service routine and write to the fixed vector table. Flash memory rewrite operation is aborted when the $\overline{\text{NMI}}$ or watchdog timer interrupt occurs. Execute the rewrite program again after exiting the interrupt routine.
- The address match interrupt is not available since the CPU tries to read data in the flash memory.

25.3.7.4 Reading and Writing Commands and Data

Read or write 16-bit commands and data from or to even addresses in the user ROM area.

25.3.7.5 Reset

Reset is always enabled.

25.3.7.6 Access Prohibited

Write the FMR01 bit and FMR05 bit in a space other than the flash memory.

25.3.7.7 How to Access

To set the FMR01 bit and FMR02 bits to "1", set to "1" immediately after setting to "0". Do not generate an interrupt or a DMA transfer between the instruction to set the bits to "1" and the instruction to set the bits to "0". Set the FMR01 bit to "1" after an "H" signal is applied to the P85/NMI pin.

25.3.7.8 Rewriting in the User ROM Area

If the supply voltage drops while in CPU rewrite mode, when rewriting the block where the rewrite control program is stored, the flash memory cannot be rewritten because the rewrite control program is not correctly rewritten. If this error occurs, rewrite the user ROM area while in standard serial I/O mode or parallel I/O mode.

25.4 Standard Serial I/O Mode

In standard serial I/O mode, the serial programmer supporting the M32C/83 group can be used to rewrite the flash memory user ROM area, while the microcomputer is mounted on a board. For more information about the serial programmer, contact your serial programmer manufacturer. Refer to the user's manual included with your serial programmer for instructions.

Standard serial I/O mode includes:

- Standard serial I/O mode 1 (clock synchronous)
- Standard serial I/O mode 2 (clock asynchronous)

25.4.1 Pin Function

Table 25.6 lists pin descriptions (flash memory standard serial I/O mode). Figures 2.12 to 25.14 show pin connections in serial I/O mode.

25.4.2 ID Code Verify Function

The ID code verify function determines whether the ID codes sent from the serial programmer matches those written in the flash memory. (Refer to **25.2 Functions to Prevent Flash Memory from Rewriting.**)

Table 25.6 Pin Description (Flash Memory Standard Serial I/O Mode)

Symbol	Function	I/O Type	Description
VCC	Power Supply	I	Apply 4.2 V to 5.5 V to the VCC pin
VSS	Input		Apply 0 V to the VSS pin
CNVSS	CNVSS	I	Connect this pin to VCC
RESET	Reset Input	I	Reset input pin. Apply 20 or more clock cycles to the XIN pin while "L" is applied to the RESET pin.
XIN	Clock Input	I	Connect a ceramic resonator or crystal oscillator between XIN and XOUT. To use the external clock, input the clock from XIN and leave XOUT open.
XOUT	Clock Output	O	
BYTE	BYTE Input	I	Connect this pin to VSS or VCC
AVCC	Analog Power	I	Connect AVCC to VCC
AVSS	Supply Input	I	Connect AVSS to VSS
VREF	Reference Voltage Input	I	Reference voltage input pin for the A/D converter.
P00 to P07	Input Port P0	I	Apply "H" or "L" to this pin, or leave open
P10 to P17	Input Port P1	I	Apply "H" or "L" to this pin, or leave open
P20 to P27	Input Port P2	I	Apply "H" or "L" to this pin, or leave open
P30 to P37	Input Port P3	I	Apply "H" or "L" to this pin, or leave open
P40 to P47	Input port P4	I	Apply "H" or "L" to this pin, or leave open
P50	CE Input	I	Apply "H" to this pin.
P55	EPM Input	I	Apply "L" to this pin.
P51 to P54 P56, P57	Input Port P5	I	Apply "H" or "L" to this pin, or leave open
P60 to P63	Input Port P6	I	Apply "H" or "L" to this pin, or leave open
P64	BUSY Output	O	Standard serial I/O mode 1: BUSY signal output pin Standard serial I/O mode 2: Program running verify monitor
P65	SCLK Input	I	Standard serial I/O mode 1: Serial clock input pin Standard serial I/O mode 2: Apply "L" to this pin
P66	RxD	I	Serial data input pin
P67	TxD	O	Serial data output pin ⁽¹⁾
P70 to P77	Input Port P7	I	Apply "H" or "L" to this pin, or leave open
P80 to P84 P86, P87	Input Port P8	I	Apply "H" or "L" to this pin, or leave open
P85	NMI Input	I	Connect this pin to VCC
P90 to P97	Input Port P9	I	Apply "H" or "L" to this pin, or leave open
P100 to P107	Input Port P10	I	Apply "H" or "L" to this pin, or leave open
P110 to P114 ⁽²⁾	Input Port P11	I	Apply "H" or "L" to this pin, or leave open
P120 to P127 ⁽²⁾	Input Port P12	I	Apply "H" or "L" to this pin, or leave open
P130 to P137 ⁽²⁾	Input Port P13	I	Apply "H" or "L" to this pin, or leave open
P140 to P146 ⁽²⁾	Input Port P14	I	Apply "H" or "L" to this pin, or leave open
P150 to P157 ⁽²⁾	Input Port P15	I	Apply "H" or "L" to this pin, or leave open

NOTES:

1. In standard serial I/O mode 1, apply an "L" signal to the TxD pin while applying "L" to the RESET pin. Connect P67 to VSS via a resistor. P67 becomes a data output pin after reset. Adjust the value of the pull-down resistor on your system so as not to affect data transfer.
2. These pins are provided in the 144-pin package only.

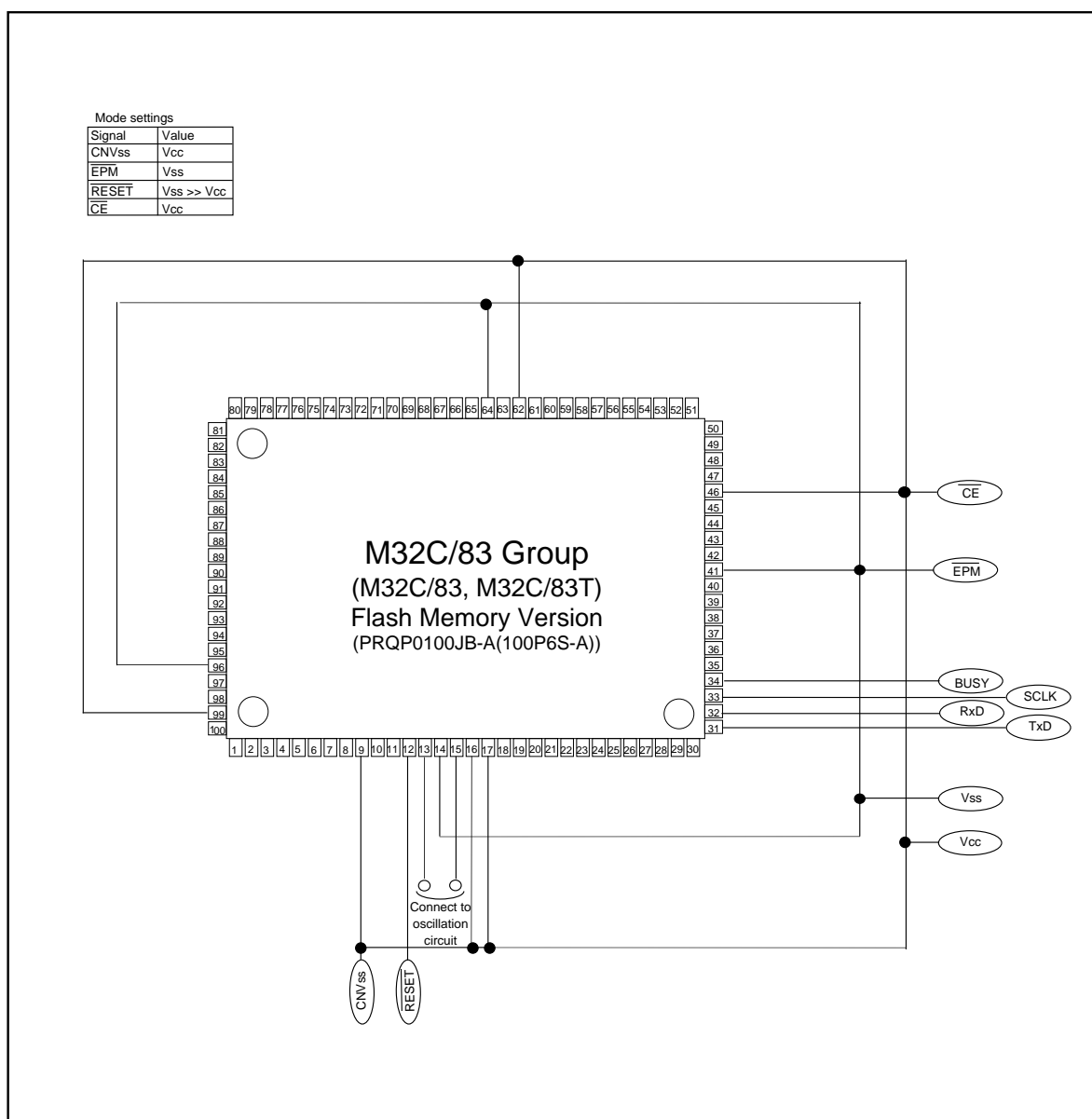


Figure 25.12 Pin Connections in Standard Serial I/O Mode (1)

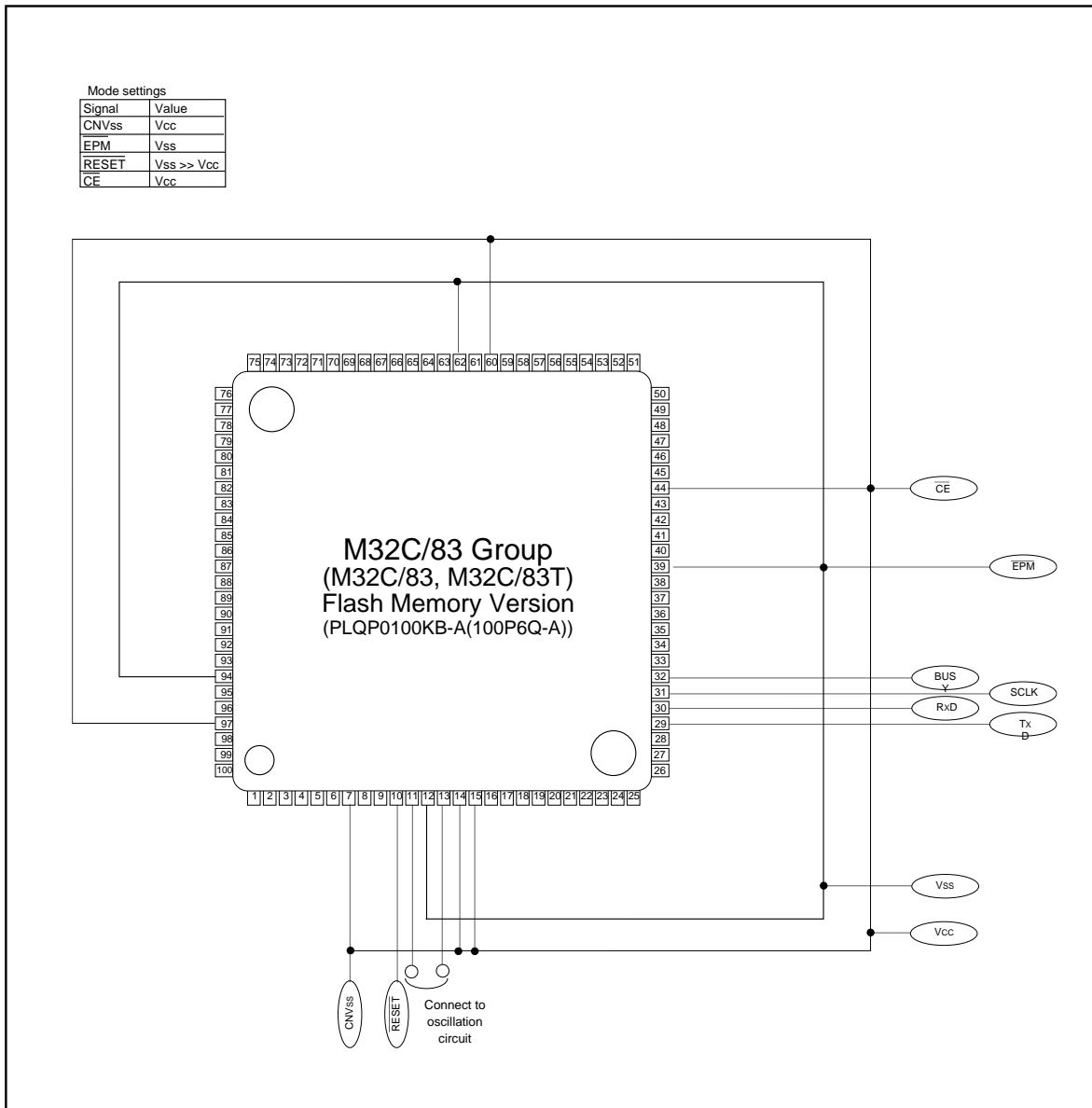


Figure 25.13 Pin Connections in Standard Serial I/O Mode (2)

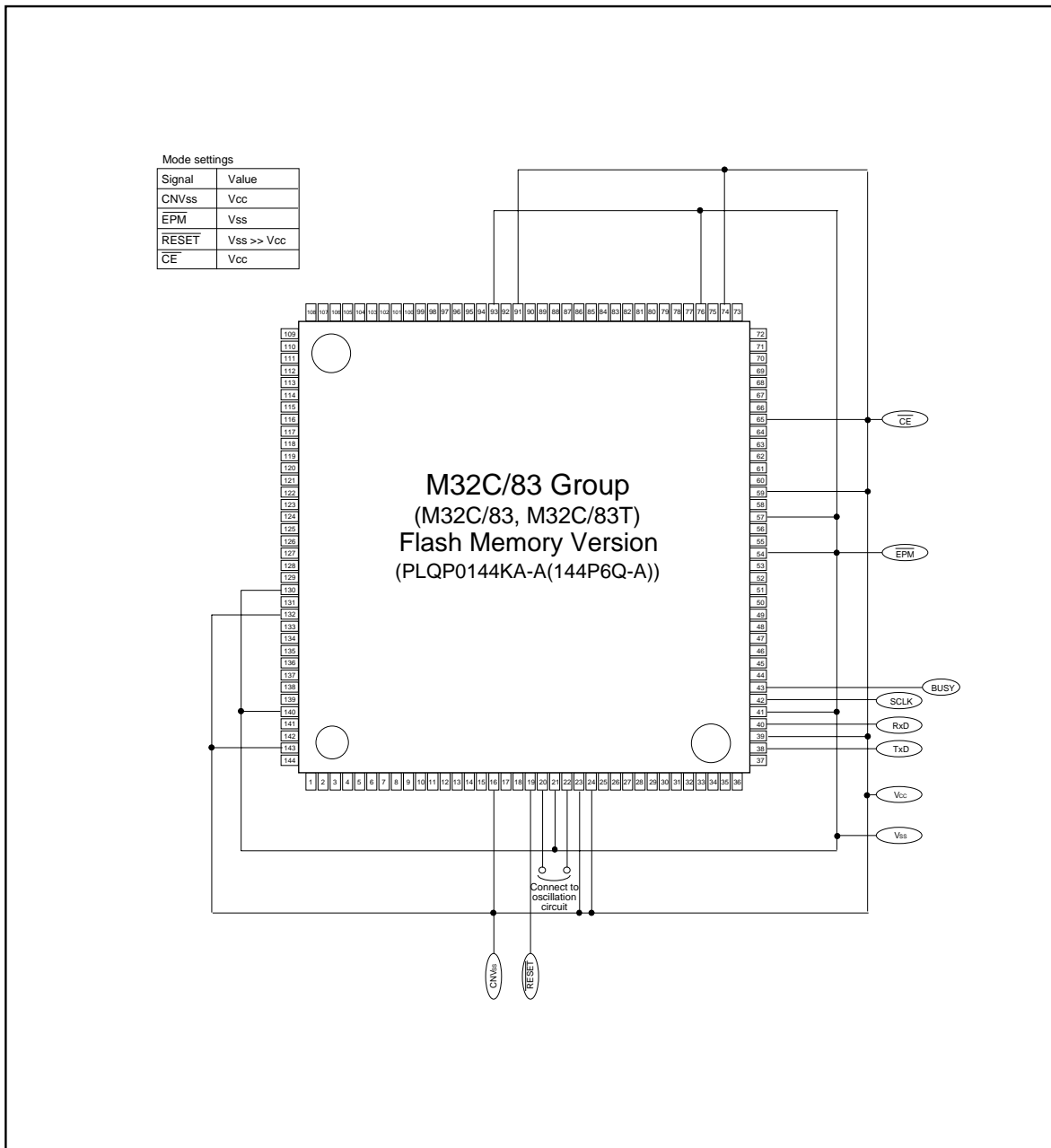


Figure 25.14 Pin Connections in Standard Serial I/O Mode (3)

25.4.3 Precautions in Standard Serial I/O Mode

- Serial I/O mode cannot be used after boot ROM area is written in parallel I/O mode.
- If an user reset signal becomes "L" in serial I/O mode, break connection between the user reset signal and the $\overline{\text{RESET}}$ pin by using, for example, a jumper selector.

25.4.4 Circuit Application in Standard Serial I/O Mode

Figure 25.15 shows an example of a circuit application in standard serial I/O mode 1. Figure 25.16 shows an example of a circuit application in serial I/O mode 2. Refer to the user's manual of your serial programmer to handle pins controlled by the serial programmer.

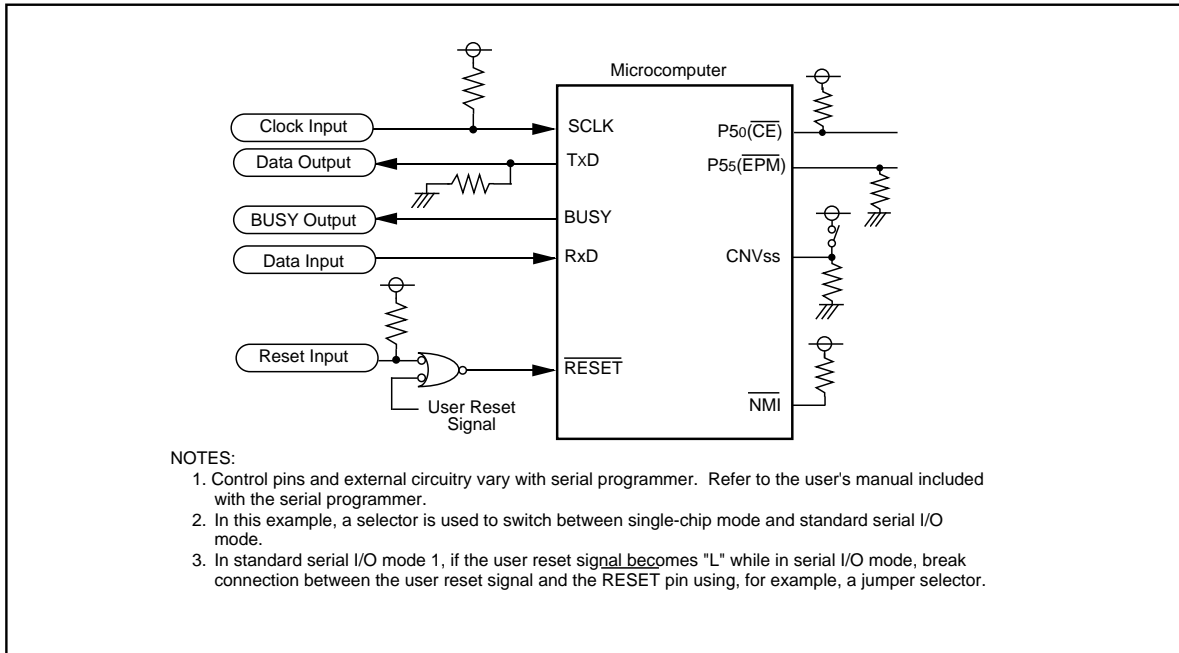


Figure 25.15 Circuit Application in Standard Serial I/O Mode 1

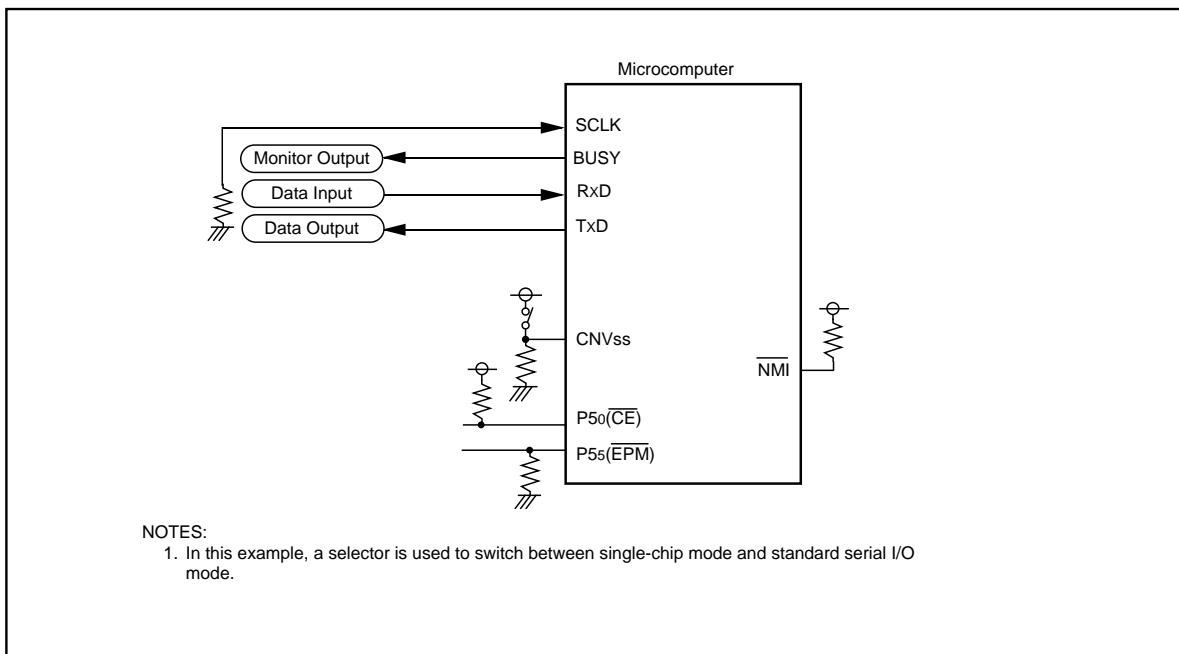


Figure 25.16 Circuit Application in Standard Serial I/O Mode 2

25.5 Parallel I/O Mode

In parallel I/O mode, the user ROM area and the boot ROM area (see Figure 25.1) can be rewritten by a parallel programmer supporting the M32C/83 Group. Contact your parallel programmer manufacturer for more information on the parallel programmer. Refer to the user's manual included with your parallel programmer for instructions.

25.5.1 Boot ROM Area

Within the boot ROM area, 8K bytes equal one block.

The rewrite control program in standard serial I/O mode is written in the boot ROM area before shipment. Do not rewrite the boot ROM area if using a serial programmer.

In parallel I/O mode, the boot ROM area is allocated to addresses 0FFE000₁₆ to 0FFFFFF₁₆. Rewrite only this address range when rewriting the boot ROM area. (Do not access addresses other than addresses 0FFE000₁₆ to 0FFFFFF₁₆.)

25.5.2 ROM Code Protect Function

The ROM code protect function prevents the flash memory from being read and rewritten in parallel I/O mode. (Refer to **25.2 Functions to Prevent Flash Memory from Rewriting.**)

25.5.3 Precautions on Parallel I/O Mode

Standard serial I/O mode cannot be used if rewriting the boot ROM area in parallel I/O mode. (Refer to **25.4 Standard Serial I/O Mode.**)

26. Electrical Characteristics

26.1 Electrical Characteristics (M32C/83)

Table 26.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Value	Unit
V _{CC}	Supply Voltage	V _{CC} =AV _{CC}	-0.3 to 6.0	V
AV _{CC}	Analog Supply Voltage	V _{CC} =AV _{CC}	-0.3 to 6.0	V
V _I	Input Voltage	RESET, CNV _{SS} , BYTE, P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₇ , P4 ₀ -P4 ₇ , P5 ₀ -P5 ₇ , P6 ₀ -P6 ₇ , P7 ₂ -P7 ₇ , P8 ₀ - P8 ₇ , P9 ₀ -P9 ₇ , P10 ₀ -P10 ₇ , P11 ₀ -P11 ₄ , P12 ₀ -P12 ₇ , P13 ₀ -P13 ₇ , P14 ₀ -P14 ₆ , P15 ₀ -P15 ₇ ⁽¹⁾ , V _{REF} , X _{IN}	-0.3 to V _{CC} +0.3	V
		P7 ₀ , P7 ₁	-0.3 to 6.0	V
V _O	Output Voltage	P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₇ , P4 ₀ -P4 ₇ , P5 ₀ - P5 ₇ , P6 ₀ -P6 ₇ , P7 ₂ -P7 ₇ , P8 ₀ -P8 ₄ , P8 ₆ , P8 ₇ , P9 ₀ -P9 ₇ , P10 ₀ -P10 ₇ , P11 ₀ -P11 ₄ , P12 ₀ -P12 ₇ , P13 ₀ -P13 ₇ , P14 ₀ - P14 ₆ , P15 ₀ -P15 ₇ ⁽¹⁾ , X _{OUT}	-0.3 to V _{CC} +0.3	V
P _d	Power Dissipation	T _{opr} =25° C	500	mW
T _{opr}	Operating Ambient Temperature		-20 to 85	° C
T _{stg}	Storage Temperature		-65 to 150	° C

NOTES:

1. P11 to P15 are provided in the 144-pin package.

Table 26.2 Recommended Operating Conditions ($V_{CC} = 3.0V$ to $5.5V$ at $T_{opr} = -20$ to $85^{\circ}C$)

Symbol	Parameter		Standard			Unit
			Min	Typ	Max	
V_{CC}	Supply Voltage (Through VDC)		3.0	5.0	5.5	V
	Supply Voltage (Not through VDC)		3.0	3.3	3.6	V
A_{VCC}	Analog Supply Voltage			V_{CC}		V
V_{SS}	Supply Voltage			0		V
A_{VSS}	Analog Supply Voltage			0		V
V_{IH}	Input High ("H") Voltage	P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P87 ⁽³⁾ , P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽⁴⁾ , X_{IN} , \overline{RESET} , CNV_{SS} , BYTE	0.8 V_{CC}		V_{CC}	V
		P70, P71	0.8 V_{CC}		6.0	
		P00-P07, P10-P17 (in single-chip mode)	0.8 V_{CC}		V_{CC}	V
		P00-P07, P10-P17 (in memory expansion mode and microprocessor mode)	0.5 V_{CC}		V_{CC}	V
V_{IL}	Input Low ("L") Voltage	P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87 ⁽³⁾ , P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽⁴⁾ , X_{IN} , \overline{RESET} , CNV_{SS} , BYTE	0		0.2 V_{CC}	V
		P00-P07, P10-P17 (in single-chip mode)	0		0.2 V_{CC}	V
		P00-P07, P10-P17 (in memory expansion mode and microprocessor mode)	0		0.16 V_{CC}	V
$I_{OH(peak)}$	Peak Output High ("H") Current ⁽²⁾	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽⁴⁾			-10.0	mA
$I_{OH(avg)}$	Average Output High ("H") Current ⁽¹⁾	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽⁴⁾			-5.0	mA
$I_{OL(peak)}$	Peak Output Low ("L") Current ⁽²⁾	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽⁴⁾			10.0	mA
$I_{OL(avg)}$	Average Output Low ("L") Current ⁽¹⁾	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽⁴⁾			5.0	mA
$f(X_{IN})$	Main Clock Input Frequency	Through VDC	$V_{CC}=4.2$ to $5.5V$	0	32	MHz
			$V_{CC}=3.0$ to $4.3V$	0	20	MHz
		Not through VDC	$V_{CC}=3.0$ to 3.6	0	20	MHz
$f(X_{CIN})$	Sub Clock Oscillation Frequency			32.768	50	kHz

NOTES:

- Typical values when average output current is 100ms.
- Total $I_{OL(peak)}$ for P0, P1, P2, P86, P87, P9, P10, P11, P14 and P15 must be 80mA or less.
Total $I_{OH(peak)}$ for P0, P1, P2, P86, P87, P9, P10, P11, P14 and P15 must be -80mA or less.
Total $I_{OL(peak)}$ for P3, P4, P5, P6, P7, P80 to P84, P12 and P13 must be 80mA or less.
Total $I_{OH(peak)}$ for P3, P4, P5, P6, P72 to P77, P80 to P84, P12 and P13 must be -80mA or less.
- V_{IH} and V_{IL} reference for P87 applies when P87 is used as a programmable input port.
It does not apply to P87 used as X_{CIN} .
- P11 to P15 are provided in the 144-pin package only.

**Table 26.3 Electrical Characteristics (V_{CC}=4.2 to 5.5V, V_{SS}=0V
at Topr= -20 to 85°C, f(X_{IN})=32MHz unless otherwise specified)**

Symbol	Parameter		Condition	Standard			Unit
				Min	Typ	Max	
V _{OH}	Output High ("H") Voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	I _{OH} =-5mA	V _{CC} - 2.0			V
		P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	I _{OH} =-200μA	V _{CC} - 0.3			
		X _{OUT}	I _{OH} =-1mA	3.0			V
		X _{COU} T	No load applied		3.3		V
V _{OL}	Output Low ("L") Voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	I _{OL} =5mA			2.0	V
		P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	I _{OL} =200μA			0.45	
		X _{OUT}	I _{OL} =1mA			2.0	V
		X _{COU} T	No load applied		0		V
V _{TH} -V _{TL}	Hysteresis	HOLD, RDY, TA0IN-TA4IN, TB0IN-TB5IN, INT0-INT5, AD _{TRG} , CTS0-CTS4, CLK0-CLK4, TA0 _{OUT} -TA4 _{OUT} , NMI, KI0-KI3, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4			0.2	1.0	V
		RESET			0.2	1.8	
I _{IH}	Input High ("H") Current	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾ , X _{IN} , RESET, CNV _{SS} , BYTE	V _I =5V			5.0	μA
I _{IL}	Input Low ("L") Current	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾ , X _{IN} , RESET, CNV _{SS} , BYTE	V _I =0V			-5.0	μA
R _{PULLUP}	Pull-up Resistance	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	V _I =0V	30	50	167	kΩ
R _{FXIN}	Feedback Resistance	X _{IN}			1.5		MΩ
R _{FXCN}	Feedback Resistance	X _{CN}			10		MΩ
V _{RAM}	RAM Standby Voltage	Through VDC		2.5			V
I _{CC}	Power Supply Current	Measurement conditions: In single-chip mode, output pins are left open and other pins are connected to V _{SS} .	f(X _{IN})=32 MHz, square wave, no division		40	54	mA
			f(X _{CN})=32 kHz, with a wait state, Topr=25° C		470		
			Topr=25° C when the clock stops		0.4	20	μA

NOTES:

1. P11 to P15 are provided in the 144-pin package only.

$V_{CC}=5V$

Table 26.4 A/D Conversion Characteristics ($V_{CC} = AV_{CC} = V_{REF} = 4.2$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$ at $T_{opr} = -20$ to $85^{\circ}C$, $f(X_{IN}) = 32MHz$ unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit	
			Min	Typ	Max		
-	Resolution	$V_{REF}=V_{CC}$			10	Bits	
INL	Integral Nonlinearity Error	$V_{REF}=V_{CC}=5V$	AN ₀ to AN ₇			±3	LSB
			AN _{EX0} , AN _{EX1}				LSB
			External op-amp connection mode			±7	LSB
DNL	Differential Nonlinearity Error				±1	LSB	
-	Offset Error				±3	LSB	
-	Gain Error				±3	LSB	
R _{LADDER}	Resistor Ladder	$V_{REF}=V_{CC}$	8		40	kΩ	
t _{CONV}	10-bit Conversion Time		2.1			μs	
t _{CONV}	8-bit Conversion Time		1.8			μs	
t _{SAMP}	Sample Time		0.2			μs	
V _{REF}	Reference Voltage		2		V _{CC}	V	
V _{IA}	Analog Input Voltage		0		V _{REF}	V	

NOTES:

1. Divide $f(X_{IN})$, if exceeding 16 MHz, to keep ϕ_{AD} frequency at 16 MHz or less.

Table 26.5 D/A Conversion Characteristics ($V_{CC} = V_{REF} = 4.2$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$ at $T_{opr} = -20$ to $85^{\circ}C$, $f(X_{IN}) = 32MHz$ unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min	Typ	Max	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
t _{SU}	Setup Time				3	μs
R _O	Output Resistance		4	10	20	kΩ
I _{VREF}	Reference Power Supply Input Current	(Note 1)			1.5	mA

NOTES:

1. Measurement results when using one D/A converter. The DA_i register (i=0, 1) of the D/A converter not being used is set to "00₁₆". The resistor ladder in the A/D converter is excluded. I_{VREF} flows even if the VCUT bit in the ADiCON1 register is set to "0" (no V_{REF} connection).

Table 26.6 Flash Memory Version Electrical Characteristics

Parameter	Standard			Unit
	Min	Typ	Max	
Program Time (per page)		8	120	ms
Block Erase Time (per block)		50	600	ms

NOTES:

1. V_{CC}= 4.2 to 5.5V (through VDC), 3.0 to 3.6V (not through VDC) at T_{opr}= 0 to 60° C, unless otherwise specified

$V_{CC}=5V$

Timing Requirements ($V_{CC} = 4.2$ to $5.5V$, $V_{SS} = 0V$ at $T_{opr} = -20$ to $85^{\circ}C$ unless otherwise specified)**Table 26.7 External Clock Input**

Symbol	Parameter	Standard		Unit
		Min	Max	
t_c	External Clock Input Cycle Time	33		ns
$t_{w(H)}$	External Clock Input High ("H") Pulse Width	13		ns
$t_{w(L)}$	External Clock Input Low ("L") Pulse Width	13		ns
t_r	External Clock Rise Time		5	ns
t_f	External Clock Fall Time		5	ns

Table 26.8 Memory Expansion and Microprocessor Modes

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{ac1(RD-DB)}$	Data Input Access Time (RD standard, with no wait state)		(Note 1)	ns
$t_{ac1(AD-DB)}$	Data Input Access Time (AD standard, CS standard, with no wait state)		(Note 1)	ns
$t_{ac2(RD-DB)}$	Data Input Access Time (RD standard, with a wait state)		(Note 1)	ns
$t_{ac2(AD-DB)}$	Data Input Access Time (AD standard, CS standard, with a wait state)		(Note 1)	ns
$t_{ac3(RD-DB)}$	Data Input Access Time (RD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
$t_{ac3(AD-DB)}$	Data Input Access Time (AD standard, CS standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
$t_{ac4(RAS-DB)}$	Data Input Access Time (RAS standard, when accessing a DRAM space)		(Note 1)	ns
$t_{ac4(CAS-DB)}$	Data Input Access Time (CAS standard, when accessing a DRAM space)		(Note 1)	ns
$t_{ac4(CAD-DB)}$	Data Input Access Time (CAD standard, when accessing a DRAM space)		(Note 1)	ns
$t_{su(DB-BCLK)}$	Data Input Setup Time	26		ns
$t_{su(RDY-BCLK)}$	RDY Input Setup Time	26		ns
$t_{su(HOLD-BCLK)}$	HOLD Input Setup Time	30		ns
$t_{h(RD-DB)}$	Data Input Hold Time	0		ns
$t_{h(CAS-DB)}$	Data Input Hold Time	0		ns
$t_{h(BCLK-RDY)}$	RDY Input Hold Time	0		ns
$t_{h(BCLK-HOLD)}$	HOLD Input Hold Time	0		ns
$t_{d(BCLK-HLDA)}$	HLDA Output Delay Time		25	ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency. Insert a wait state or lower the operation frequency, $f_{(BCLK)}$, if the calculated value is negative.

$$t_{ac1(RD-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}]$$

$$t_{ac1(AD-DB)} = \frac{10^9}{f_{(BCLK)}} - 35 \quad [\text{ns}]$$

$$t_{ac2(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \quad (m=3 \text{ with 1 wait state, } m=5 \text{ with 2 wait states and } m=7 \text{ with 3 wait states})$$

$$t_{ac2(AD-DB)} = \frac{10^9 \times n}{f_{(BCLK)}} - 35 \quad [\text{ns}] \quad (n=2 \text{ with 1 wait state, } n=3 \text{ with 2 wait states and } n=4 \text{ with 3 wait states})$$

$$t_{ac3(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \quad (m=3 \text{ with 2 wait states and } m=5 \text{ with 3 wait states})$$

$$t_{ac3(AD-DB)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \quad (n=5 \text{ with 2 wait states and } n=7 \text{ with 3 wait states})$$

$$t_{ac4(RAS-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \quad (m=3 \text{ with 1 wait state and } m=5 \text{ with 2 wait states})$$

$$t_{ac4(CAS-DB)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \quad (n=1 \text{ with 1 wait state and } n=3 \text{ when 2 wait states})$$

$$t_{ac4(CAD-DB)} = \frac{10^9 \times l}{f_{(BCLK)}} - 35 \quad [\text{ns}] \quad (l=1 \text{ with 1 wait state and } l=2 \text{ with 2 wait states})$$

Timing Requirements(V_{CC} = 4.2 to 5.5V, V_{SS} = 0V at Topr = -20 to 85°C unless otherwise specified)**Table 26.9 Timer A Input (Count Source Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{C(TA)}	TA _{in} Input Cycle Time	100		ns
t _{w(TAH)}	TA _{in} Input High ("H") Pulse Width	40		ns
t _{w(TAL)}	TA _{in} Input Low ("L") Pulse Width	40		ns

Table 26.10 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{C(TA)}	TA _{in} Input Cycle Time	400		ns
t _{w(TAH)}	TA _{in} Input High ("H") Pulse Width	200		ns
t _{w(TAL)}	TA _{in} Input Low ("L") Pulse Width	200		ns

Table 26.11 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{C(TA)}	TA _{in} Input Cycle Time	200		ns
t _{w(TAH)}	TA _{in} Input High ("H") Pulse Width	100		ns
t _{w(TAL)}	TA _{in} Input Low ("L") Pulse Width	100		ns

Table 26.12 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{w(TAH)}	TA _{in} Input High ("H") Pulse Width	100		ns
t _{w(TAL)}	TA _{in} Input Low ("L") Pulse Width	100		ns

Table 26.13 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{C(UP)}	TA _{IOU_T} Input Cycle Time	2000		ns
t _{w(UPH)}	TA _{IOU_T} Input High ("H") Pulse Width	1000		ns
t _{w(UPL)}	TA _{IOU_T} Input Low ("L") Pulse Width	1000		ns
t _{SU(UP-TIN)}	TA _{IOU_T} Input Setup Time	400		ns
t _{H(TIN-UP)}	TA _{IOU_T} Input Hold Time	400		ns

Timing Requirements**(V_{CC} = 4.2 to 5.5V, V_{SS} = 0V at Topr = -20 to 85°C unless otherwise specified)****Table 26.14 Timer B Input (Count Source Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{C(TB)}	TBin Input Cycle Time (counted on one edge)	100		ns
t _{w(TBH)}	TBin Input High ("H") Pulse Width (counted on one edge)	40		ns
t _{w(TBL)}	TBin Input Low ("L") Pulse Width (counted on one edge)	40		ns
t _{C(TB)}	TBin Input Cycle Time (counted on both edges)	200		ns
t _{w(TBH)}	TBin Input High ("H") Pulse Width (counted on both edges)	80		ns
t _{w(TBL)}	TBin Input Low ("L") Pulse Width (counted on both edges)	80		ns

Table 26.15 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{C(TB)}	TBin Input Cycle Time	400		ns
t _{w(TBH)}	TBin Input High ("H") Pulse Width	200		ns
t _{w(TBL)}	TBin Input Low ("L") Pulse Width	200		ns

Table 26.16 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{C(TB)}	TBin Input Cycle Time	400		ns
t _{w(TBH)}	TBin Input High ("H") Pulse Width	200		ns
t _{w(TBL)}	TBin Input Low ("L") Pulse Width	200		ns

Table 26.17 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{C(AD)}	AD _{TRG} Input Cycle Time (required for re-trigger)	1000		ns
t _{w(ADL)}	AD _{TRG} Input Low ("L") Pulse Width	125		ns

Table 26.18 Serial I/O

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{C(CLK)}	CLKi Input Cycle Time	200		ns
t _{w(CLKH)}	CLKi Input High ("H") Pulse Width	100		ns
t _{w(CLKL)}	CLKi Input Low ("L") Pulse Width	100		ns
t _{d(C-Q)}	TxDi Output Delay Time		80	ns
t _{h(C-Q)}	TxDi Hold Time	0		ns
t _{su(D-Q)}	RxDi Input Set Up Time	30		ns
t _{h(C-Q)}	RxDi Input Hold Time	90		ns

Table 26.19 External Interrupt INTi Input

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{w(INH)}	INTi Input High ("H") Pulse Width	250		ns
t _{w(INL)}	INTi Input Low ("L") Pulse Width	250		ns

Switching Characteristics(V_{CC} = 4.2 to 5.5V, V_{SS} = 0V at Topr = -20 to 85°C unless otherwise specified)**Table 26.20 Memory Expansion Mode and Microprocessor Mode (with No Wait State)**

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min	Max	
t _{d(BCLK-AD)}	Address Output Delay Time	See Figure 26.1		18	ns
t _{h(BCLK-AD)}	Address Output Hold Time (BCLK standard)		-3		ns
t _{h(RD-AD)}	Address Output Hold Time (RD standard)		0		ns
t _{h(WR-AD)}	Address Output Hold Time (WR standard)		(Note 1)		ns
t _{d(BCLK-CS)}	Chip-select Signal Output Delay Time			18	ns
t _{h(BCLK-CS)}	Chip-select Signal Output Hold Time (BCLK standard)		-3		ns
t _{h(RD-CS)}	Chip-select Signal Output Hold Time (RD standard)		0		ns
t _{h(WR-CS)}	Chip-select Signal Output Hold Time (WR standard)		(Note 1)		ns
t _{d(BCLK-ALE)}	ALE Signal Output Delay Time			18	ns
t _{h(BCLK-ALE)}	ALE Signal Output Hold Time		-2		ns
t _{d(BCLK-RD)}	RD Signal Output Delay Time			18	ns
t _{h(BCLK-RD)}	RD Signal Output Hold Time		-5		ns
t _{d(BCLK-WR)}	WR Signal Output Delay Time			18	ns
t _{h(BCLK-WR)}	WR Signal Output Hold Time		-3		ns
t _{d(DB-WR)}	Data Output Delay Time (WR standard)		(Note 1)		ns
t _{h(WR-DB)}	Data Output Hold Time (WR standard)		(Note 1)		ns
t _{w(WR)}	WR Output Width		(Note 1)		ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$t_{d(DB-WR)} = \frac{10^9}{f_{(BCLK)}} - 20 \quad [\text{ns}]$$

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

$$t_{w(WR)} = \frac{10^9}{f_{(BCLK)} \times 2} - 15 \quad [\text{ns}]$$

Switching Characteristics(V_{CC} = 4.2 to 5.5V, V_{SS} = 0V at Topr = -20 to 85°C unless otherwise specified)**Table 26.21 Memory Expansion Mode and Microprocessor Mode
(With a Wait State, Accessing an External Memory)**

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min	Max	
t _{d(BCLK-AD)}	Address Output Delay Time	See Figure 26.1		18	ns
t _{h(BCLK-AD)}	Address Output Hold Time (BCLK standard)		-3		ns
t _{h(RD-AD)}	Address Output Hold Time (RD standard)		0		ns
t _{h(WR-AD)}	Address Output Hold Time (WR standard)		(Note 1)		ns
t _{d(BCLK-CS)}	Chip-select Signal Output Delay Time			18	ns
t _{h(BCLK-CS)}	Chip-select Signal Output Hold Time (BCLK standard)		-3		ns
t _{h(RD-CS)}	Chip-select Signal Output Hold Time (RD standard)		0		ns
t _{h(WR-CS)}	Chip-select Signal Output Hold Time (WR standard)		(Note 1)		ns
t _{d(BCLK-ALE)}	ALE Signal Output Delay Time			18	ns
t _{h(BCLK-ALE)}	ALE Signal Output Hold Time		-2		ns
t _{d(BCLK-RD)}	RD Signal Output Delay Time			18	ns
t _{h(BCLK-RD)}	RD Signal Output Hold Time		-5		ns
t _{d(BCLK-WR)}	WR Signal Output Delay Time			18	ns
t _{h(BCLK-WR)}	WR Signal Output Hold Time		-3		ns
t _{d(DB-WR)}	Data Output Delay Time (WR standard)		(Note 1)		ns
t _{h(WR-DB)}	Data Output Hold Time (WR standard)		(Note 1)		ns
t _{w(WR)}	WR Output Width		(Note 1)		ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$t_{d(DB-WR)} = \frac{10^9 \times n}{f_{(BCLK)}} - 20 \quad [\text{ns}] \quad (n=1 \text{ with 1 wait state, } n=2 \text{ with 2 wait states} \\ \text{and } n=3 \text{ with 3 wait states})$$

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

$$t_{w(WR)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 15 \quad [\text{ns}] \quad (n=1 \text{ with 1 wait state, } n=3 \text{ with 2 wait states} \\ \text{and } n=5 \text{ with 3 wait states})$$

Switching Characteristics(V_{CC} = 4.2 to 5.5V, V_{SS} = 0V at Topr = -20 to 85°C unless otherwise specified)**Table 26.22 Memory Expansion Mode and Microprocessor Mode
(With a Wait State, Accessing an External Memory and Selecting a Space with the Multiplexed Bus)**

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min	Max	
t _{d(BCLK-AD)}	Address Output Delay Time	See Figure 26.1		18	ns
t _{h(BCLK-AD)}	Address Output Hold Time (BCLK standard)		-3		ns
t _{h(RD-AD)}	Address Output Hold Time (RD standard)		(Note 1)		ns
t _{h(WR-AD)}	Address Output Hold Time (WR standard)		(Note 1)		ns
t _{d(BCLK-CS)}	Chip-select Signal Output Delay Time			18	ns
t _{h(BCLK-CS)}	Chip-select Signal Output Hold Time (BCLK standard)		-3		ns
t _{h(RD-CS)}	Chip-select Signal Output Hold Time (RD standard)		(Note 1)		ns
t _{h(WR-CS)}	Chip-select Signal Output Hold Time (WR standard)		(Note 1)		ns
t _{d(BCLK-RD)}	RD Signal Output Delay Time			18	ns
t _{h(BCLK-AD)}	RD Signal Output Hold Time		-5		ns
t _{d(BCLK-WR)}	WR Signal Output Delay Time			18	ns
t _{h(BCLK-WR)}	WR Signal Output Hold Time		-3		ns
t _{d(DB-WR)}	Data Output Delay Time (WR standard)		(Note 1)		ns
t _{h(WR-DB)}	Data Output Hold Time (WR standard)		(Note 1)		ns
t _{d(BCLK-ALE)}	ALE Signal Output Delay Time (BCLK standard)			18	ns
t _{h(BCLK-ALE)}	ALE Signal Output Hold Time (BCLK standard)		-2		ns
t _{d(AD-ALE)}	ALE Signal Output Delay Time (address standard)		(Note 1)		ns
t _{h(ALE-AD)}	ALE Signal Output Hold Time (address standard)		(Note 1)		ns
t _{dz(RD-AD)}	Address Output High-Impedance Time			8	ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$t_{h(RD-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

$$t_{h(RD-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

$$t_{d(DB-WR)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 25 \quad [\text{ns}] \quad (m=3 \text{ with 2 wait states and } m=5 \text{ with 3 wait states})$$

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

$$t_{d(AD-ALE)} = \frac{10^9}{f_{(BCLK)} \times 2} - 20 \quad [\text{ns}]$$

$$t_{h(ALE-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

Switching Characteristics(V_{CC} = 4.2 to 5.5V, V_{SS} = 0V at Topr = -20 to 85°C unless otherwise specified)**Table 26.23 Memory Expansion Mode and Microprocessor Mode
(With a Wait State, Accessing an External Memory and Selecting the DRAM Space)**

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min	Max	
t _{d(BCLK-RAD)}	Row Address Output Delay Time	See Figure 26.1		18	ns
t _{h(BCLK-RAD)}	Row Address Output Hold Time (BCLK standard)		-3		ns
t _{d(BCLK-CAD)}	Column Address Output Delay Time			18	ns
t _{h(BCLK-CAD)}	Column Address Output Hold Time (BCLK standard)		-3		ns
t _{h(RAS-RAD)}	Row Address Output Hold Time after RAS Output		(Note 1)		ns
t _{d(BCLK-RAS)}	RAS Output Delay Time (BCLK standard)			18	ns
t _{h(BCLK-RAS)}	RAS Output Hold Time (BCLK standard)		-3		ns
t _{RP}	RAS High ("H") Hold Time		(Note 1)		ns
t _{d(BCLK-CAS)}	CAS Output Delay Time (BCLK standard)			18	ns
t _{h(BCLK-CAS)}	CAS Output Hold Time (BCLK standard)		-3		ns
t _{d(BCLK-DW)}	DW Output Delay Time (BCLK standard)			18	ns
t _{h(BCLK-DW)}	DW Output Hold Time (BCLK standard)		-5		ns
t _{SU(DB-CAS)}	CAS Output Setup Time after DB Output		(Note 1)		ns
t _{h(BCLK-DB)}	DB Signal Output Hold Time (BCLK standard)		-7		ns
t _{SU(CAS-RAS)}	CAS Output Setup Time before RAS Output (refresh)		(Note 1)		ns

NOTES:

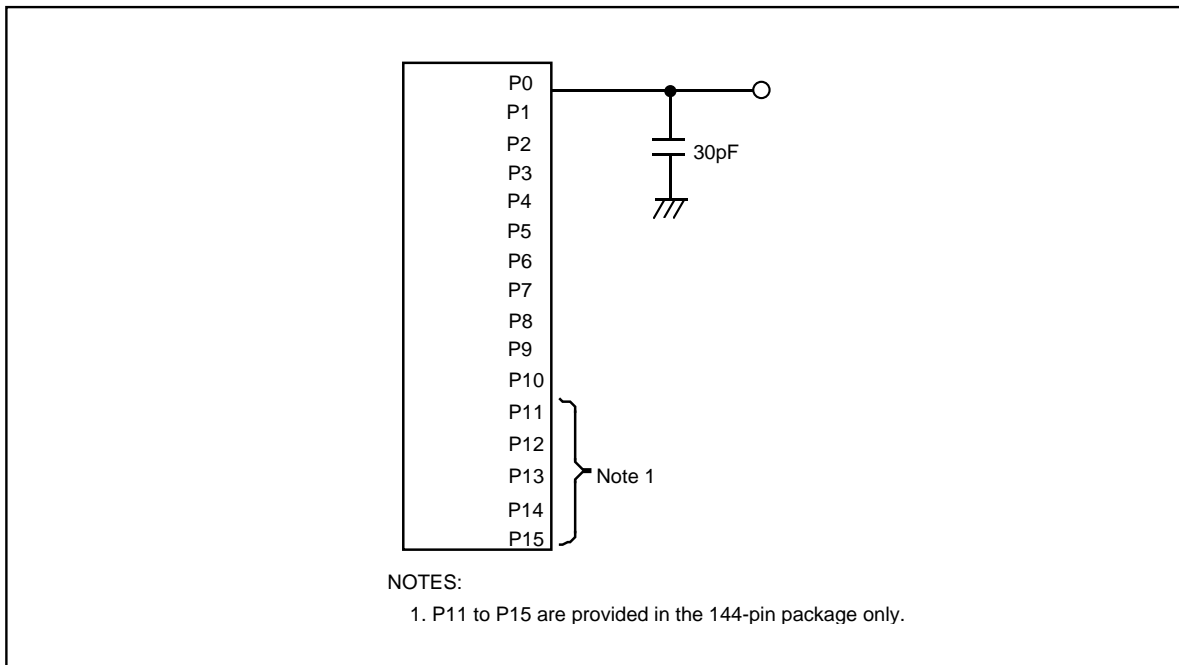
1. Values can be obtained from the following equation, according to BCLK frequency.

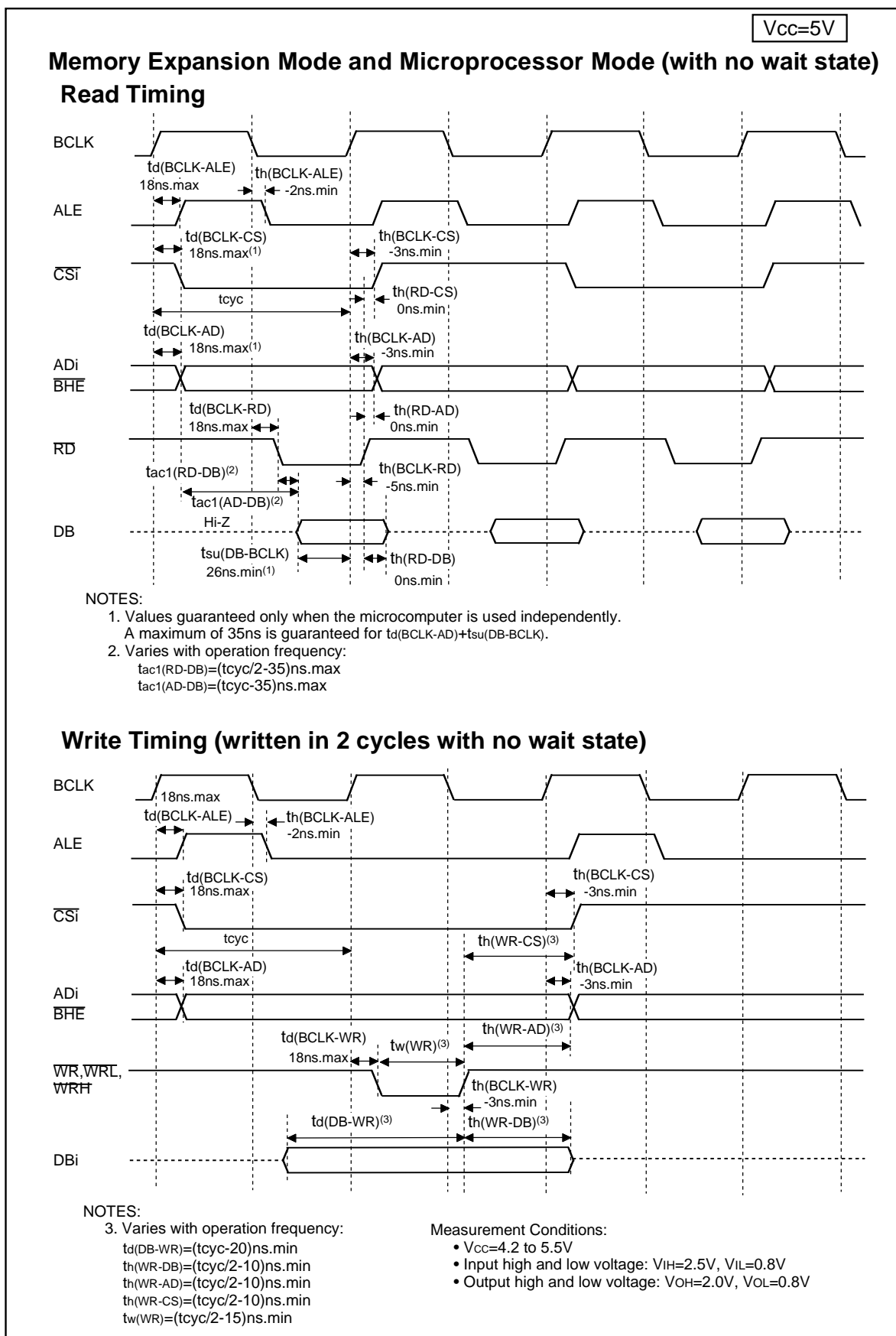
$$t_{h(RAS - RAD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 13 \quad [\text{ns}]$$

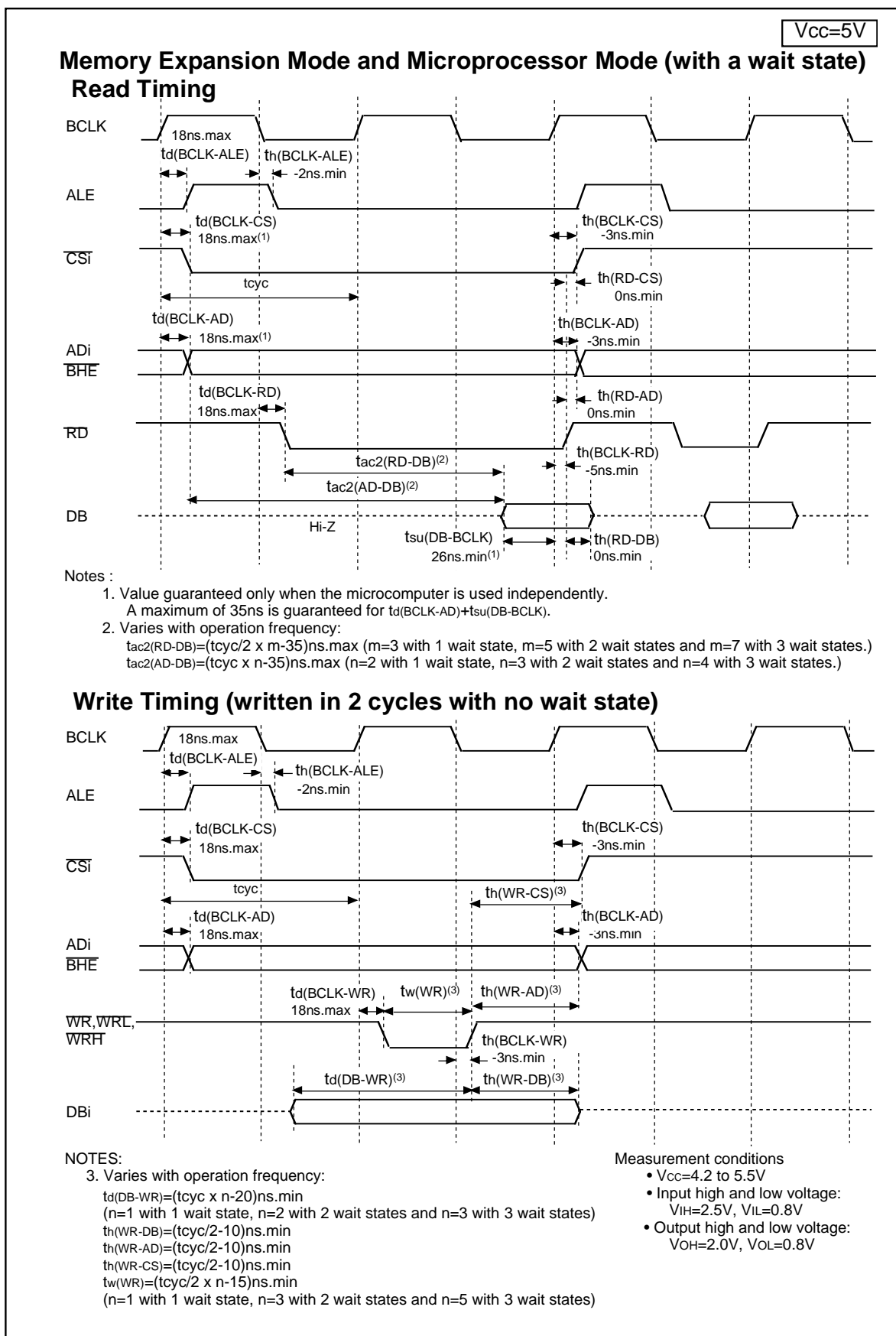
$$t_{RP} = \frac{10^9 \times 3}{f_{(BCLK)} \times 2} - 20 \quad [\text{ns}]$$

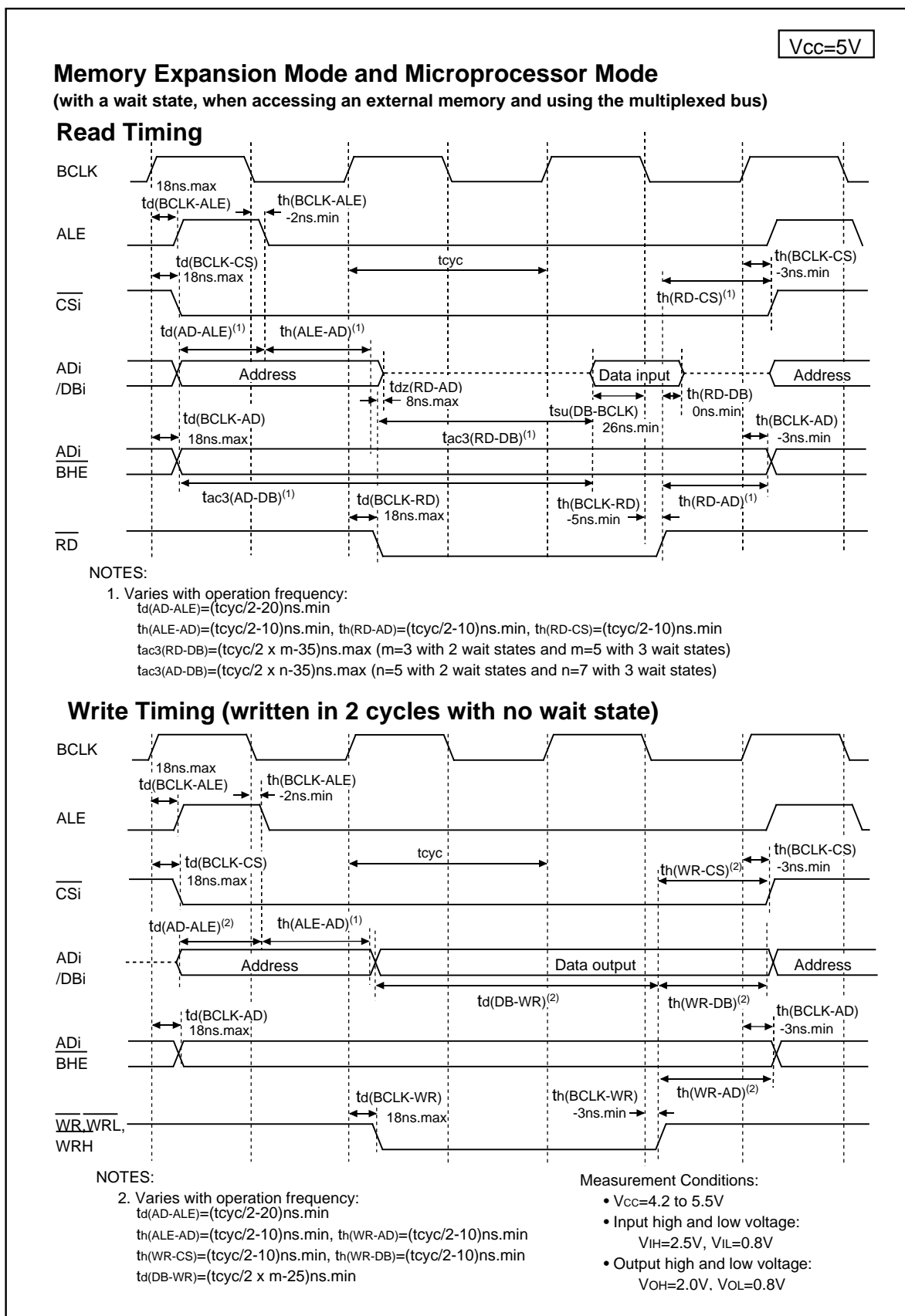
$$t_{SU(DB - CAS)} = \frac{10^9}{f_{(BCLK)}} - 20 \quad [\text{ns}]$$

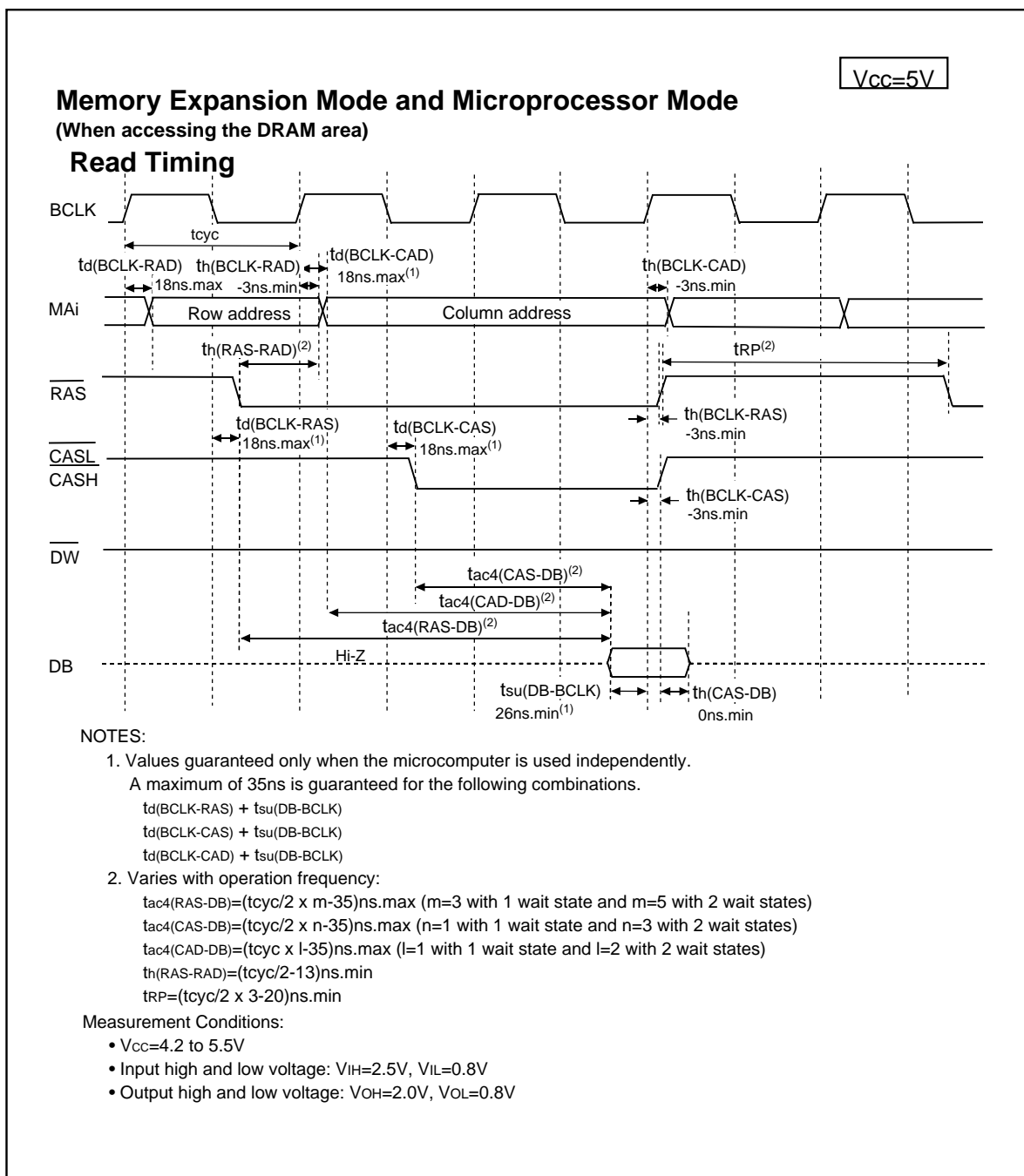
$$t_{SU(CAS - RAS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 13 \quad [\text{ns}]$$

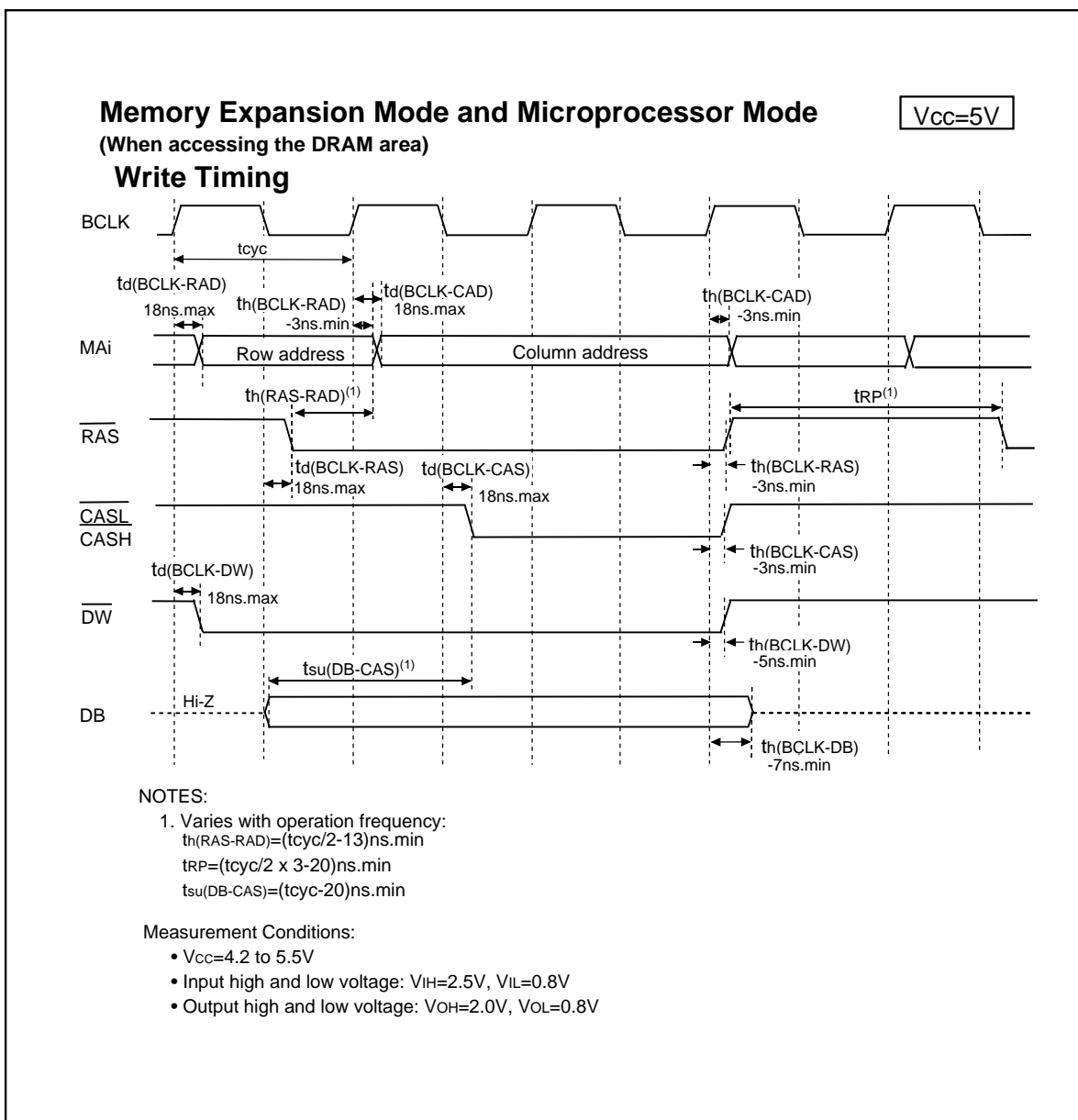
**Figure 26.1 P0 to P15 Measurement Circuit**

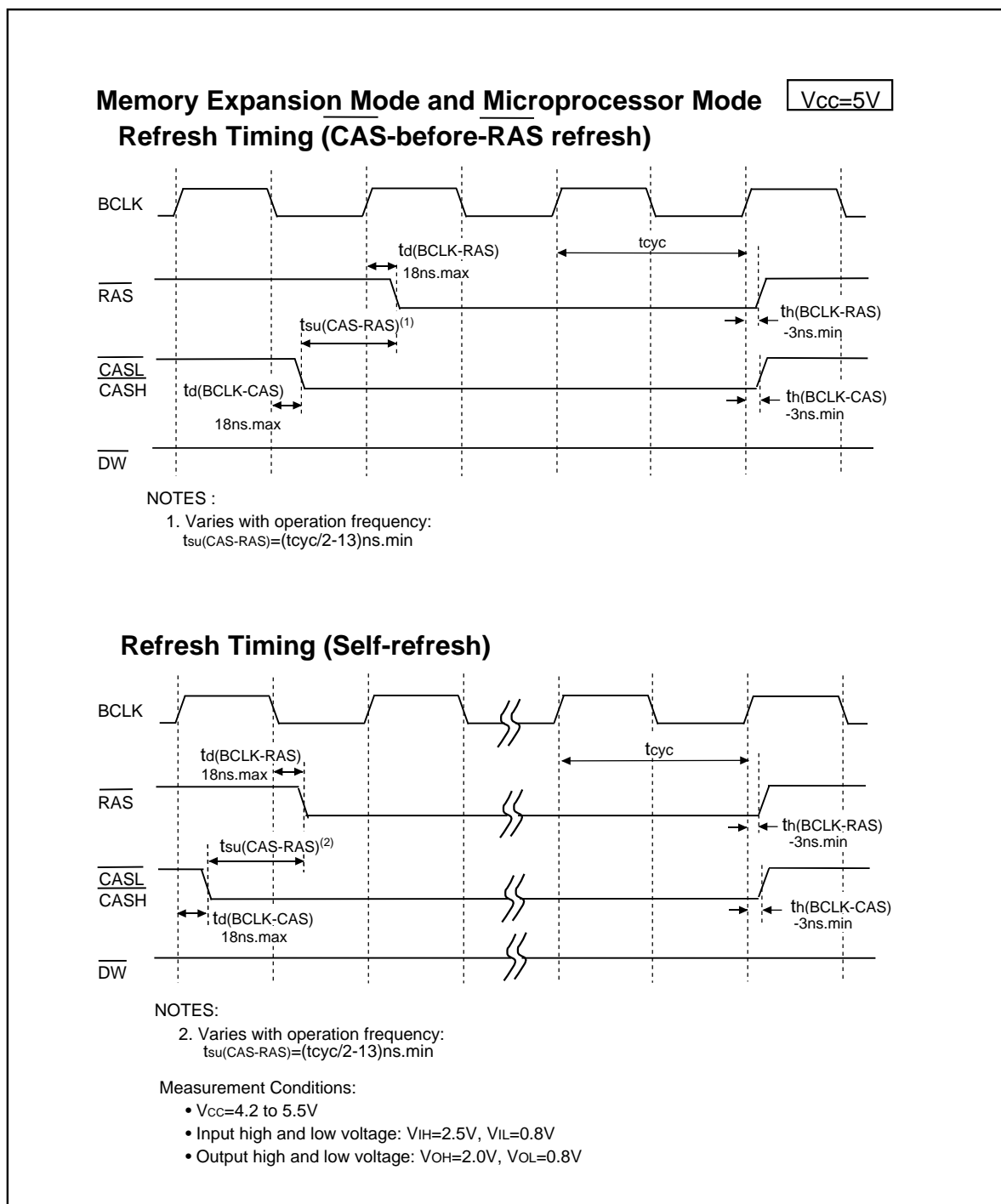
Figure 26.2 V_{CC}=5V Timing Diagram (1)

Figure 26.3 V_{CC}=5V Timing Diagram (2)

Figure 26.4 V_{CC}=5V Timing Diagram (3)

Figure 26.5 $V_{CC}=5V$ Timing Diagram (4)

Figure 26.6 V_{CC}=5V Timing Diagram (5)

Figure 26.7 V_{CC}=5V Timing Diagram (6)

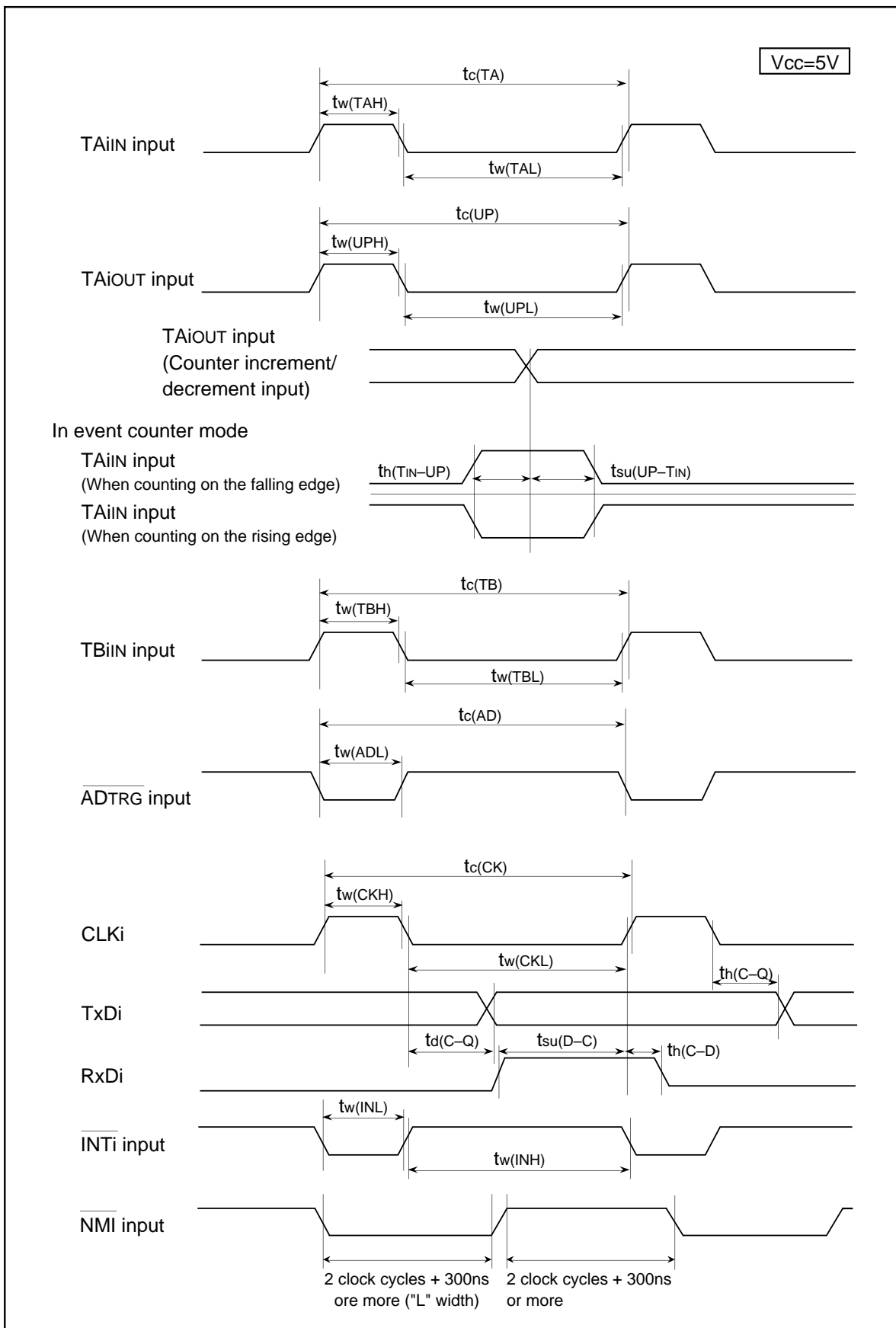


Figure 26.8 $V_{CC}=5V$ Timing Diagram (7)

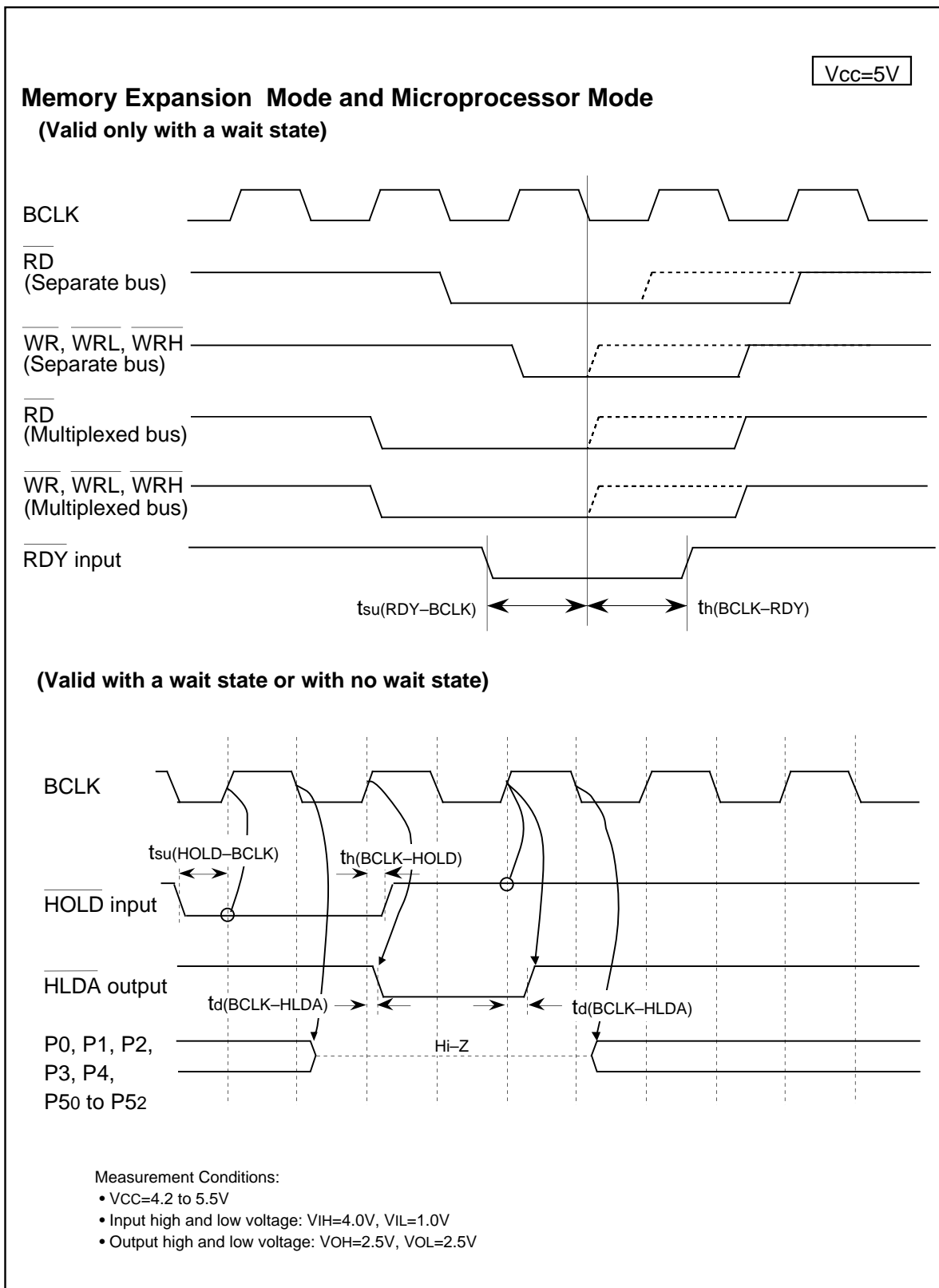


Figure 26.9 V_{CC}=5V Timing Diagram (8)

$V_{CC}=3.3V$

Table 26.24 Electrical Characteristics ($V_{CC}=3.0$ to $3.6V$, $V_{SS}=0V$ at $T_{opr} = -20$ to $85^{\circ}C$, $f(X_{IN})=20MHz$ unless otherwise specified)

Symbol	Parameter		Condition	Standard			Unit
				Min	Typ	Max	
V_{OH}	Output High ("H") Voltage	P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₇ , P4 ₀ -P4 ₇ , P5 ₀ -P5 ₇ , P6 ₀ -P6 ₇ , P7 ₂ -P7 ₇ , P8 ₀ -P8 ₄ , P8 ₆ , P8 ₇ , P9 ₀ -P9 ₇ , P10 ₀ -P10 ₇ , P11 ₀ -P11 ₄ , P12 ₀ -P12 ₇ , P13 ₀ -P13 ₇ , P14 ₀ -P14 ₆ , P15 ₀ -P15 ₇ ⁽¹⁾	$I_{OH}=-1mA$	$V_{CC}-0.6$			V
		X _{OUT}	$I_{OH}=-0.1mA$	2.7		V	
		X _{COUT}	No load applied		3.3		V
V_{OL}	Output Low ("L") Voltage	P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₇ , P4 ₀ -P4 ₇ , P5 ₀ -P5 ₇ , P6 ₀ -P6 ₇ , P7 ₀ -P7 ₇ , P8 ₀ -P8 ₄ , P8 ₆ , P8 ₇ , P9 ₀ -P9 ₇ , P10 ₀ -P10 ₇ , P11 ₀ -P11 ₄ , P12 ₀ -P12 ₇ , P13 ₀ -P13 ₇ , P14 ₀ -P14 ₆ , P15 ₀ -P15 ₇ ⁽¹⁾	$I_{OL}=1mA$			0.5	V
		X _{OUT}	$I_{OL}=0.1mA$			0.5	V
		X _{COUT}	No load applied		0		V
$V_{T+}-V_{T-}$	Hysteresis	HOLD, RDY, TA0 _{IN} -TA4 _{IN} , TB0 _{IN} -TB5 _{IN} , INT0-INT5, AD _{TRG} , CTS0-CTS4, CLK0-CLK4, TA0 _{OUT} -TA4 _{OUT} , \overline{NMI} , $\overline{KI0}$ - $\overline{KI3}$, Rx _{D0} -Rx _{D4} , SCL0-SCL4, SDA0-SDA4		0.2		1.0	V
		RESET		0.2		1.8	V
I_{IH}	Input High ("H") Current	P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₇ , P4 ₀ -P4 ₇ , P5 ₀ -P5 ₇ , P6 ₀ -P6 ₇ , P7 ₀ -P7 ₇ , P8 ₀ -P8 ₇ , P9 ₀ -P9 ₇ , P10 ₀ -P10 ₇ , P11 ₀ -P11 ₄ , P12 ₀ -P12 ₇ , P13 ₀ -P13 ₇ , P14 ₀ -P14 ₆ , P15 ₀ -P15 ₇ ⁽¹⁾ , X _{IN} , \overline{RESET} , CNV _{SS} , BYTE	$V_I=3V$			4.0	μA
I_{IL}	Input Low ("L") Current	P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₇ , P4 ₀ -P4 ₇ , P5 ₀ -P5 ₇ , P6 ₀ -P6 ₇ , P7 ₀ -P7 ₇ , P8 ₀ -P8 ₇ , P9 ₀ -P9 ₇ , P10 ₀ -P10 ₇ , P11 ₀ -P11 ₄ , P12 ₀ -P12 ₇ , P13 ₀ -P13 ₇ , P14 ₀ -P14 ₆ , P15 ₀ -P15 ₇ ⁽¹⁾ , X _{IN} , \overline{RESET} , CNV _{SS} , BYTE	$V_I=0V$			-4.0	μA
R_{PULLUP}	Pull-up Resistance	P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₇ , P4 ₀ -P4 ₇ , P5 ₀ -P5 ₇ , P6 ₀ -P6 ₇ , P7 ₂ -P7 ₇ , P8 ₀ -P8 ₄ , P8 ₆ , P8 ₇ , P9 ₀ -P9 ₇ , P10 ₀ -P10 ₇ , P11 ₀ -P11 ₄ , P12 ₀ -P12 ₇ , P13 ₀ -P13 ₇ , P14 ₀ -P14 ₆ , P15 ₀ -P15 ₇ ⁽¹⁾	$V_I=0V$	66	120	500	k Ω
R_{fXIN}	Feedback Resistance	X _{IN}			3.0		M Ω
R_{fXCIN}	Feedback Resistance	X _{CIN}			20.0		M Ω
V_{RAM}	RAM Standby Voltage	Through VDC		2.5			V
		Not through VDC		2.0			V
I_{CC}	Power Supply Current	Measurement condition: In single-chip mode, output pins are left open and other pins are connected to V _{SS} .	f(X _{IN})=20 MHz, square wave, no division		26	38	mA
			f(X _{CIN})=32 kHz, with a wait state, not through VDC, T _{opr} =25° C		5.0		μA
			f(X _{CIN})=32 kHz, with a wait state, through VDC, T _{opr} =25° C		340		μA
			T _{opr} =25° C when the clock stops		0.4	20	μA

NOTES:

1. P11 to P15 are provided in the 144-pin package only.

$V_{CC}=3.3V$

Table 26.25 A/D Conversion Characteristics ($V_{CC} = AV_{CC} = V_{REF} = 3.0$ to $3.6V$, $V_{SS} = AV_{SS} = 0V$ at $T_{opr} = -20$ to $85^{\circ}C$, $f(X_{IN}) = 20MHz$ unless otherwise specified)

Symbol	Parameter		Measurement Condition	Standard			Unit
				Min	Typ	Max	
-	Resolution		$V_{REF}=V_{CC}$			10	Bits
INL	Integral Nonlinearity Error	No S&H function (8-bit)	$V_{CC}=V_{REF}=3.3V$			± 2	LSB
DNL	Differential Nonlinearity Error	No S&H function (8-bit)				± 1	LSB
-	Offset Error	No S&H function (8-bit)				± 2	LSB
-	Gain Error	No S&H function (8-bit)				± 2	LSB
R _{LADDER}	Resistor Ladder		$V_{REF}=V_{CC}$	8		40	k Ω
t _{CONV}	8-bit Conversion Time			4.9			μs
V _{REF}	Reference Voltage			3.0		V _{CC}	V
V _{IA}	Analog Input Voltage			0		V _{REF}	V

S&H: Sample and hold

NOTES:

1. Divide $f(X_{IN})$, if exceeding 10 MHz, to keep ϕ_{AD} frequency at 10 MHz or less.

Table 26.26 D/A Conversion Characteristics ($V_{CC} = V_{REF} = 3.0$ to $3.6V$, $V_{SS} = AV_{SS} = 0V$ at $T_{opr} = -20$ to $85^{\circ}C$, $f(X_{IN}) = 20MHz$ unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min	Typ	Max	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
t _{SU}	Setup Time				3	μs
R _O	Output Resistance		4	10	20	k Ω
I _{VREF}	Reference Power Supply Input Current	(Note 1)			1.0	mA

NOTES:

1. Measurement results when using one D/A converter. The D_{Ai} register (i=0, 1) of the D/A converter not being used is set to "00₁₆". The resistor ladder in the A/D converter is excluded.
I_{VREF} flows even if the VCUT bit in the ADICON1 register is set to "0" (no V_{REF} connection).

Table 26.27 Flash Memory Version Electrical Characteristics

Parameter	Standard			Unit
	Min	Typ	Max	
Program Time (per page)		8	120	ms
Block Erase Time (per block)		50	600	ms

NOTES:

1. V_{CC}= 4.2 to 5.5V (through VDC), 3.0 to 3.6V (not through VDC) at $T_{opr} = 0$ to $60^{\circ}C$, unless otherwise specified

$V_{CC}=3.3V$

Timing Requirements ($V_{CC} = 3.0$ to $3.6V$, $V_{SS} = 0V$ at $T_{op} = -20$ to $85^{\circ}C$ unless otherwise specified)**Table 26.28 External Clock Input**

Symbol	Parameter	Standard		Unit
		Min	Max	
t_c	External Clock Input Cycle Time	50		ns
$t_{w(H)}$	External Clock Input High ("H") Pulse Width	22		ns
$t_{w(L)}$	External Clock Input Low ("L") Pulse Width	22		ns
t_r	External Clock Rise Time		5	ns
t_f	External Clock Fall Time		5	ns

Table 26.29 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{ac1(RD-DB)}$	Data Input Access Time (RD standard, with no wait state)		(Note 1)	ns
$t_{ac1(AD-DB)}$	Data Input Access Time (AD standard, CS standard, with no wait state)		(Note 1)	ns
$t_{ac2(RD-DB)}$	Data Input Access Time (RD standard, with a wait state)		(Note 1)	ns
$t_{ac2(AD-DB)}$	Data Input Access Time (AD standard, CS standard, with a wait state)		(Note 1)	ns
$t_{ac3(RD-DB)}$	Data Input Access Time (RD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
$t_{ac3(AD-DB)}$	Data Input Access Time (AD standard, CS standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
$t_{ac4(RAS-DB)}$	Data Input Access Time (RAS standard, when accessing a DRAM space)		(Note 1)	ns
$t_{ac4(CAS-DB)}$	Data Input Access Time (CAS standard, when accessing a DRAM space)		(Note 1)	ns
$t_{ac4(CAD-DB)}$	Data Input Access Time (CAD standard, when accessing a DRAM space)		(Note 1)	ns
$t_{su(DB-BCLK)}$	Data Input Setup Time	30		ns
$t_{su(RDY-BCLK)}$	RDY Input Setup Time	40		ns
$t_{su(HOLD-BCLK)}$	HOLD Input Setup Time	60		ns
$t_h(RD-DB)$	Data Input Hold Time	0		ns
$t_h(CAS-DB)$	Data Input Hold Time	0		ns
$t_h(BCLK-RDY)$	RDY Input Hold Time	0		ns
$t_h(BCLK-HOLD)$	HOLD Input Hold Time	0		ns
$t_d(BCLK-HLDA)$	HLDA Output Delay Time		25	ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency. Insert a wait state or lower operation frequency, $f_{(BCLK)}$, if the calculated value is negative.

$$t_{ac1(RD-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 35 \quad [ns]$$

$$t_{ac1(AD-DB)} = \frac{10^9}{f_{(BCLK)}} - 35 \quad [ns]$$

$$t_{ac2(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35 \quad [ns] \quad (m=3 \text{ with 1 wait state, } m=5 \text{ with 2 wait states and } m=7 \text{ with 3 wait states})$$

$$t_{ac2(AD-DB)} = \frac{10^9 \times n}{f_{(BCLK)}} - 35 \quad [ns] \quad (n=2 \text{ with 1 wait state, } n=3 \text{ with 2 wait states and } n=4 \text{ with 3 wait states})$$

$$t_{ac3(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35 \quad [ns] \quad (m=3 \text{ with 2 wait states and } m=5 \text{ with 3 wait states})$$

$$t_{ac3(AD-DB)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 35 \quad [ns] \quad (n=5 \text{ with 2 wait states and } n=7 \text{ with 3 wait states})$$

$$t_{ac4(RAS-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35 \quad [ns] \quad (m=3 \text{ with 1 wait state and } m=5 \text{ with 2 wait states})$$

$$t_{ac4(CAS-DB)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 35 \quad [ns] \quad (n=1 \text{ with 1 wait state and } n=3 \text{ when 2 wait states})$$

$$t_{ac4(CAD-DB)} = \frac{10^9 \times l}{f_{(BCLK)}} - 35 \quad [ns] \quad (l=1 \text{ with 1 wait state and } l=2 \text{ with 2 wait states})$$

V_{CC}=3.3V**Timing Requirements**(V_{CC} = 3.0 to 3.6V, V_{SS} = 0V at Topr = –20 to 85°C unless otherwise specified)**Table 26.30 Timer A Input (Count Source Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{C(TA)}	TAiIn Input Cycle Time	100		ns
t _{w(TAH)}	TAiIn Input High ("H") Pulse Width	40		ns
t _{w(TAL)}	TAiIn Input Low ("L") Pulse Width	40		ns

Table 26.31 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{C(TA)}	TAiIn Input Cycle Time	400		ns
t _{w(TAH)}	TAiIn Input High ("H") Pulse Width	200		ns
t _{w(TAL)}	TAiIn Input Low ("L") Pulse Width	200		ns

Table 26.32 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{C(TA)}	TAiIn Input Cycle Time	200		ns
t _{w(TAH)}	TAiIn Input High ("H") Pulse Width	100		ns
t _{w(TAL)}	TAiIn Input Low ("L") Pulse Width	100		ns

Table 26.33 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{w(TAH)}	TAiIn Input High ("H") Pulse Width	100		ns
t _{w(TAL)}	TAiIn Input Low ("L") Pulse Width	100		ns

Table 26.34 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{C(UP)}	TAiout Input Cycle Time	2000		ns
t _{w(UPH)}	TAiout Input High ("H") Pulse Width	1000		ns
t _{w(UPL)}	TAiout Input Low ("L") Pulse Width	1000		ns
t _{SU(UP-TIN)}	TAiout Input Setup Time	400		ns
t _{H(MINUP)}	TAiout Input Hold Time	400		ns

Timing Requirements(V_{CC} = 3.0 to 3.6V, V_{SS} = 0V at Topr = -20 to 85°C unless otherwise specified)**Table 26.35 Timer B input (Count Source Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{C(TB)}	TBin Input Cycle Time (counted on one edge)	100		ns
t _{w(TBH)}	TBin Input High ("H") Pulse Width (counted on one edge)	40		ns
t _{w(TBL)}	TBin Input Low ("L") Pulse Width (counted on one edge)	40		ns
t _{C(TB)}	TBin Input Cycle Time (counted on both edges)	200		ns
t _{w(TBH)}	TBin Input High ("H") Pulse Width (counted on both edges)	80		ns
t _{w(TBL)}	TBin Input Low ("L") Pulse Width (counted on both edges)	80		ns

Table 26.36 Timer B input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{C(TB)}	TBin Input Cycle Time	400		ns
t _{w(TBH)}	TBin Input High ("H") Pulse Width	200		ns
t _{w(TBL)}	TBin Input Low ("L") Pulse Width	200		ns

Table 26.37 Timer B input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{C(TB)}	TBin Input Cycle Time	400		ns
t _{w(TBH)}	TBin Input High ("H") Pulse Width	200		ns
t _{w(TBL)}	TBin Input Low ("L") Pulse Width	200		ns

Table 26.38 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{C(AD)}	AD _{TRG} Input High ("H") Pulse Width (required for re-trigger)	1000		ns
t _{w(ADL)}	AD _{TRG} Input Low ("L") Pulse Width	125		ns

Table 26.39 Serial I/O

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{C(CLK)}	CLKi Input Cycle Time	200		ns
t _{w(CLKH)}	CLKi Input High ("H") Pulse Width	100		ns
t _{w(CLKL)}	CLKi Input Low ("L") Pulse Width	100		ns
t _{d(C-Q)}	TxDi Output Delay Time		80	ns
t _{h(C-Q)}	TxDi Hold Time	0		ns
t _{su(D-C)}	RxDi Input Set Up Time	30		ns
t _{h(C-Q)}	RxDi Input Hold Time	90		ns

Table 26.40 External Interrupt INTi input

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{w(INH)}	INTi Input High ("H") Pulse Width	250		ns
t _{w(INL)}	INTi Input Low ("L") Pulse Width	250		ns

Switching Characteristics(V_{CC} = 3.0 to 3.6V, V_{SS} = 0V at Topr = –20 to 85°C, unless otherwise specified)**Table 26.41 Memory Expansion Mode and Microprocessor Mode (with No Wait State)**

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min	Max	
t _{d(BCLK-AD)}	Address Output Delay Time	See Figure 26.1		18	ns
t _{h(BCLK-AD)}	Address Output Hold Time (BCLK standard)		0		ns
t _{h(RD-AD)}	Address Output Hold Time (RD standard)		0		ns
t _{h(WR-AD)}	Address Output Hold Time (WR standard)		(Note 1)		ns
t _{d(BCLK-CS)}	Chip-select Signal Output Delay Time			18	ns
t _{h(BCLK-CS)}	Chip-select Signal Output Hold Time (BCLK standard)		0		ns
t _{h(RD-CS)}	Chip-select Signal Output Hold Time (RD standard)		0		ns
t _{h(WR-CS)}	Chip-select Signal Output Hold Time (WR standard)		(Note 1)		ns
t _{d(BCLK-ALE)}	ALE Signal Output Delay Time			18	ns
t _{h(BCLK-ALE)}	ALE Signal Output Hold Time		-2		ns
t _{d(BCLK-RD)}	RD Signal Output Delay Time			18	ns
t _{h(BCLK-RD)}	RD Signal Output Hold Time		-3		ns
t _{d(BCLK-WR)}	WR Signal Output Delay Time			18	ns
t _{h(BCLK-WR)}	WR Signal Output Hold Time		0		ns
t _{d(DB-WR)}	Data Output Delay Time (WR standard)		(Note 1)		ns
t _{h(WR-DB)}	Data Output Hold Time (WR standard)		(Note 1)		ns
t _{w(WR)}	WR Output Width		(Note 1)		ns

NOTES:

1. Values can be obtained from the following equations according to the BCLK frequency.

$$t_{d(DB-WR)} = \frac{10^9}{f_{(BCLK)}} - 20 \quad [\text{ns}]$$

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

$$t_{w(WR)} = \frac{10^9}{f_{(BCLK)} \times 2} - 15 \quad [\text{ns}]$$

Switching Characteristics(V_{CC} = 3.0 to 3.6V, V_{SS} = 0V at Topr = –20 to 85°C unless otherwise specified)**Table 26.42 Memory Expansion Mode and Microprocessor Mode
(With a Wait State, Accessing an External Memory)**

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min	Max	
t _{d(BCLK-AD)}	Address Output Delay Time	See Figure 26.1		18	ns
t _{h(BCLK-AD)}	Address Output Hold Time (BCLK standard)		0		ns
t _{h(RD-AD)}	Address Output Hold Time (RD standard)		0		ns
t _{h(WR-AD)}	Address Output Hold Time (WR standard)		(Note 1)		ns
t _{d(BCLK-CS)}	Chip-select Signal Output Delay Time			18	ns
t _{h(BCLK-CS)}	Chip-select Signal Output Hold Time (BCLK standard)		0		ns
t _{h(RD-CS)}	Chip-select Signal Output Hold Time (RD standard)		0		ns
t _{h(WR-CS)}	Chip-select Signal Output Hold Time (WR standard)		(Note 1)		ns
t _{d(BCLK-ALE)}	ALE Signal Output Delay Time			18	ns
t _{h(BCLK-ALE)}	ALE Signal Output Hold Time		-2		ns
t _{d(BCLK-RD)}	RD Signal Output Delay Time			18	ns
t _{h(BCLK-RD)}	RD Signal Output Hold Time		-3		ns
t _{d(BCLK-WR)}	WR Signal Output Delay Time			18	ns
t _{h(BCLK-WR)}	WR Signal Output Hold Time		0		ns
t _{d(DB-WR)}	Data Output Delay Time (WR standard)		(Note 1)		ns
t _{h(WR-DB)}	Data Output Hold Time (WR standard)		(Note 1)		ns
t _{w(WR)}	WR Output Width		(Note 1)		ns

NOTES:

- Values can be obtained from the following equations, according to BCLK frequency.

$$t_{d(DB-WR)} = \frac{10^9 \times n}{f_{(BCLK)}} - 20 \quad [\text{ns}] \quad (n=1 \text{ with 1 wait state, } n=2 \text{ with 2 wait states} \\ \text{and } n=3 \text{ with 3 wait states})$$

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

$$t_{w(WR)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 15 \quad [\text{ns}] \quad (n=1 \text{ with 1 wait state, } n=3 \text{ with 2 wait states} \\ \text{and } n=5 \text{ with 3 wait states})$$

Switching Characteristics(V_{CC} = 3.0 to 3.6V, V_{SS} = 0V at Topr = -20 to 85°C unless otherwise specified)**Table 26.43 Memory Expansion Mode and Microprocessor Mode
(With a Wait State, Accessing an External Memory and Selecting a Space with the Multiplexed Bus)**

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min	Max	
t _{d(BCLK-AD)}	Address Output Delay Time	See Figure 26.1		18	ns
t _{h(BCLK-AD)}	Address Output Hold Time (BCLK standard)		0		ns
t _{h(RD-AD)}	Address Output Hold Time (RD standard)		(Note 1)		ns
t _{h(WR-AD)}	Address Output Hold Time (WR standard)		(Note 1)		ns
t _{d(BCLK-CS)}	Chip-select Signal Output Delay Time			18	ns
t _{h(BCLK-CS)}	Chip-select Signal Output Hold Time (BCLK standard)		0		ns
t _{h(RD-CS)}	Chip-select Signal Output Hold Time (RD standard)		(Note 1)		ns
t _{h(WR-CS)}	Chip-select Signal Output Hold Time (WR standard)		(Note 1)		ns
t _{d(BCLK-RD)}	RD Signal Output Delay Time			18	ns
t _{h(BCLK-AD)}	RD Signal Output Hold Time		-3		ns
t _{d(BCLK-WR)}	WR Signal Output Delay Time			18	ns
t _{h(BCLK-WR)}	WR Signal Output Hold Time		0		ns
t _{d(DB-WR)}	Data Output Delay Time (WR standard)		(Note 1)		ns
t _{h(WR-DB)}	Data Output Hold Time (WR standard)		(Note 1)		ns
t _{d(BCLK-ALE)}	ALE Signal Output Delay Time (BCLK standard)			18	ns
t _{h(BCLK-ALE)}	ALE Signal Output Hold Time (BCLK standard)		-2		ns
t _{d(AD-ALE)}	ALE Signal Output Delay Time (address standard)		(Note 1)		ns
t _{h(ALE-AD)}	ALE Signal Output Hold Time (address standard)		(Note 1)		ns
t _{dz(RD-AD)}	Address Output High-Impedance Time			8	ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$t_{h(RD-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

$$t_{h(RD-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

$$t_{d(DB-WR)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 25 \quad [\text{ns}] \quad (m=3 \text{ with 2 wait states and } m=5 \text{ with 3 wait states})$$

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

$$t_{d(AD-ALE)} = \frac{10^9}{f_{(BCLK)} \times 2} - 20 \quad [\text{ns}]$$

$$t_{h(ALE-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

Switching Characteristics(V_{CC} = 3.0 to 3.6V, V_{SS} = 0V at Topr = -20 to 85°C unless otherwise specified)**Table 26.44 Memory Expansion Mode and Microprocessor Mode
(With a Wait State, Accessing an External Memory and Selecting the DRAM Area)**

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min	Max	
t _{d(BCLK-RAD)}	Row Address Output Delay Time	See Figure 26.1		18	ns
t _{h(BCLK-RAD)}	Row Address Output Hold Time (BCLK standard)		0		ns
t _{d(BCLK-CAD)}	Column Address Output Delay Time			18	ns
t _{h(BCLK-CAD)}	Column Address Output Hold Time (BCLK standard)		0		ns
t _{h(RAS-RAD)}	Row Address Output Hold Time after RAS Output		(Note 1)		ns
t _{d(BCLK-RAS)}	RAS Output Delay Time (BCLK standard)			18	ns
t _{h(BCLK-RAS)}	RAS Output Hold Time (BCLK standard)		0		ns
t _{RP}	RAS High ("H") Hold Time		(Note 1)		ns
t _{d(BCLK-CAS)}	CAS Output Delay Time (BCLK standard)			18	ns
t _{h(BCLK-CAS)}	CAS Output Hold Time (BCLK standard)		0		ns
t _{d(BCLK-DW)}	DW Output Delay Time (BCLK standard)			18	ns
t _{h(BCLK-DW)}	DW Output Hold Time (BCLK standard)		-3		ns
t _{SU(DB-CAS)}	CAS Output Setup Time after DB output		(Note 1)		ns
t _{h(BCLK-DB)}	DB Signal Output Hold Time (BCLK standard)		-7		ns
t _{SU(CAS-RAS)}	CAS Output Setup Time before RAS Output (refresh)		(Note 1)		ns

NOTES:

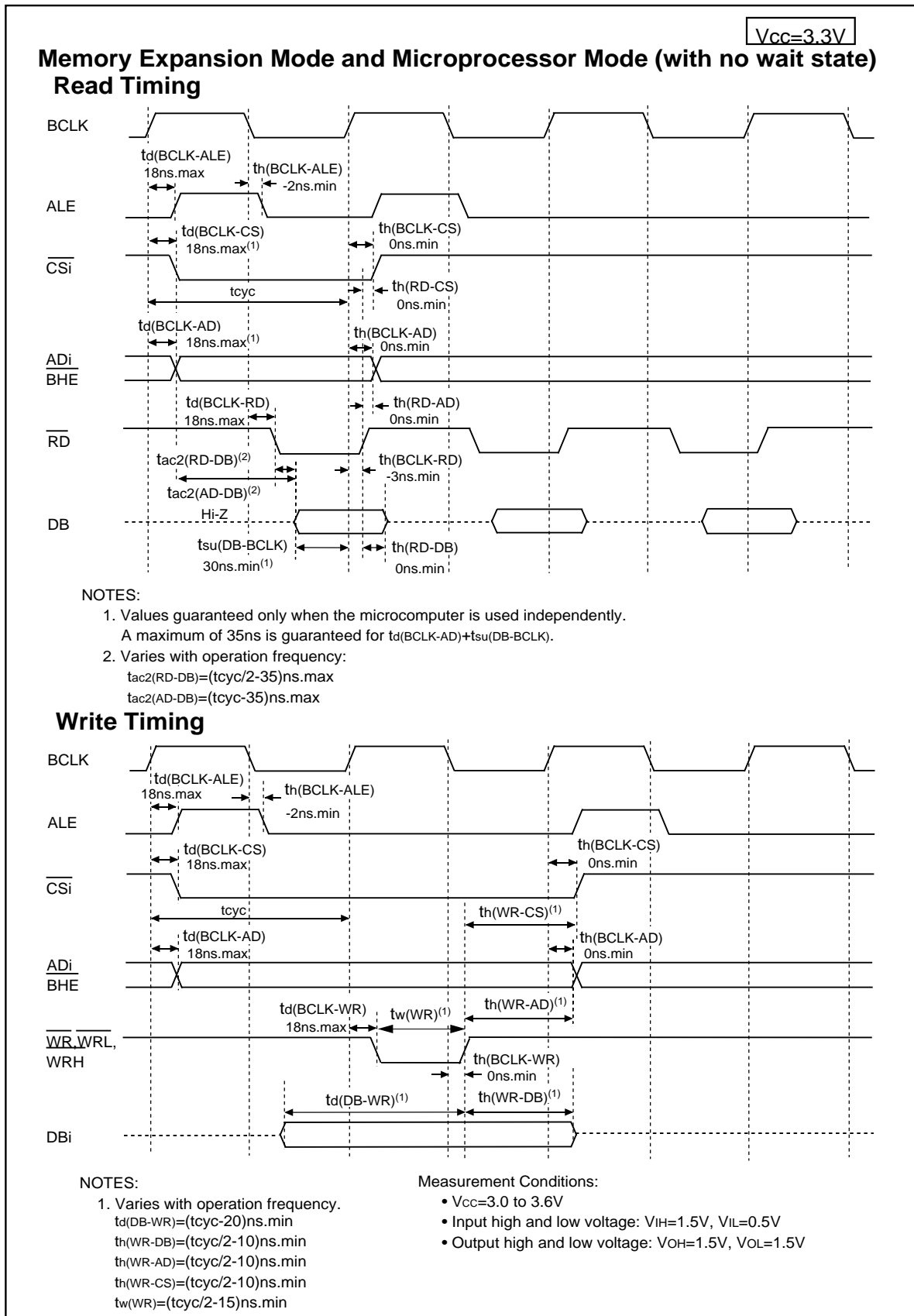
1. Values can be obtained from the following equations, according to the BCLK frequency.

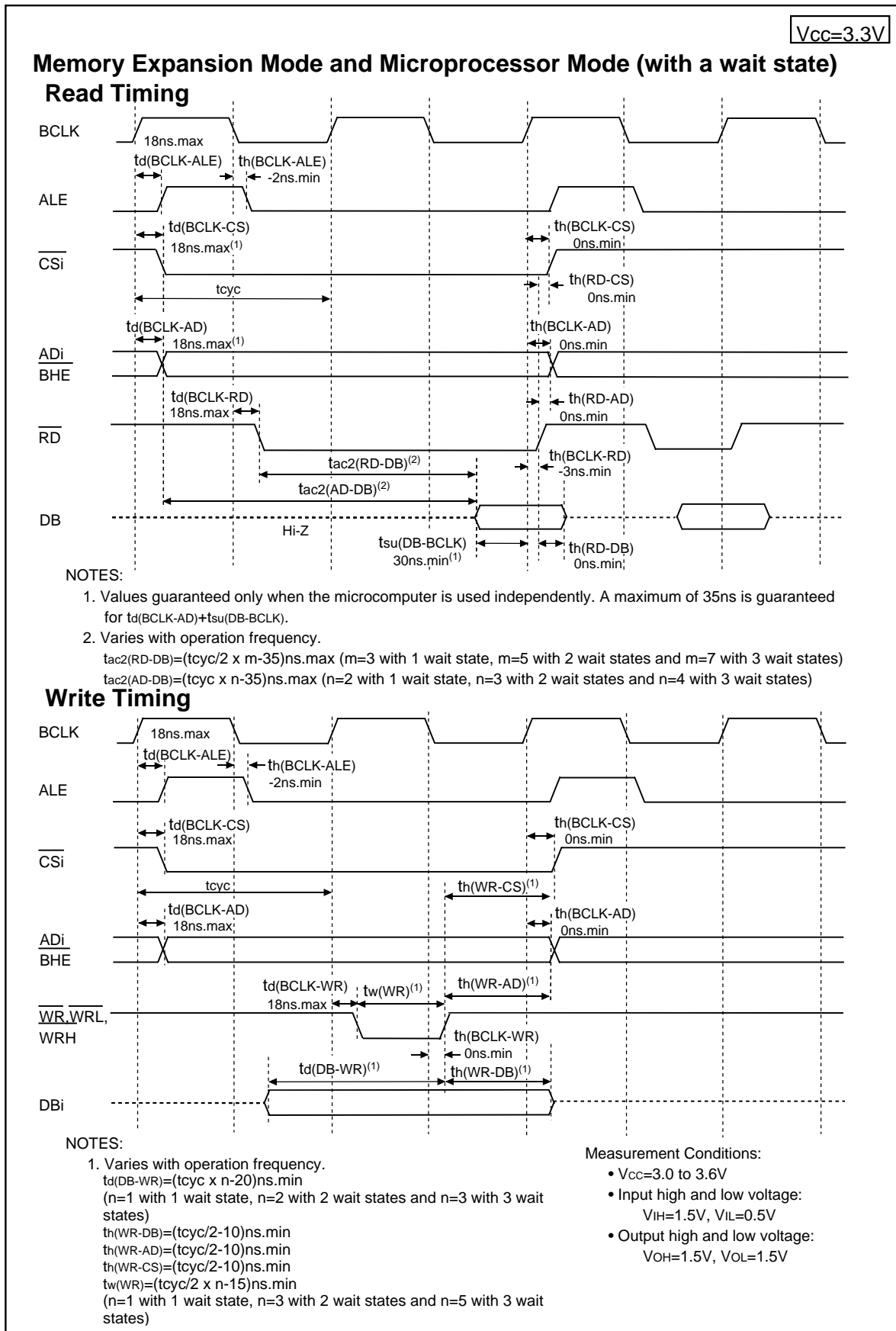
$$t_{h(RAS-RAD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 13 \quad [\text{ns}]$$

$$t_{RP} = \frac{10^9 \times 3}{f_{(BCLK)} \times 2} - 20 \quad [\text{ns}]$$

$$t_{SU(DB-CAS)} = \frac{10^9}{f_{(BCLK)}} - 20 \quad [\text{ns}]$$

$$t_{SU(CAS-RAS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 13 \quad [\text{ns}]$$

Figure 26.10 V_{CC}=3.3V Timing Diagram (1)

Figure 26.11 $V_{CC}=3.3V$ Timing Diagram (2)

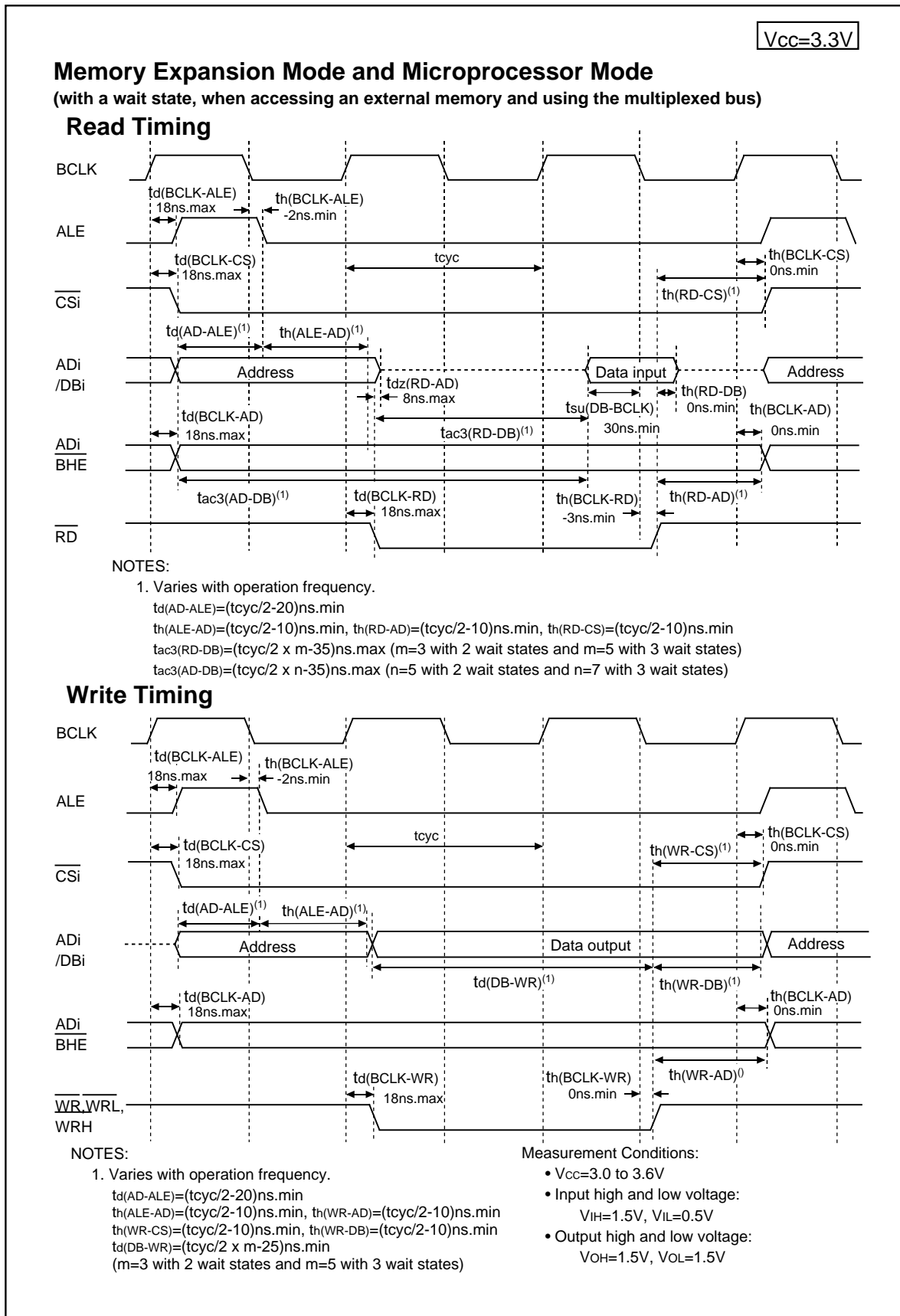
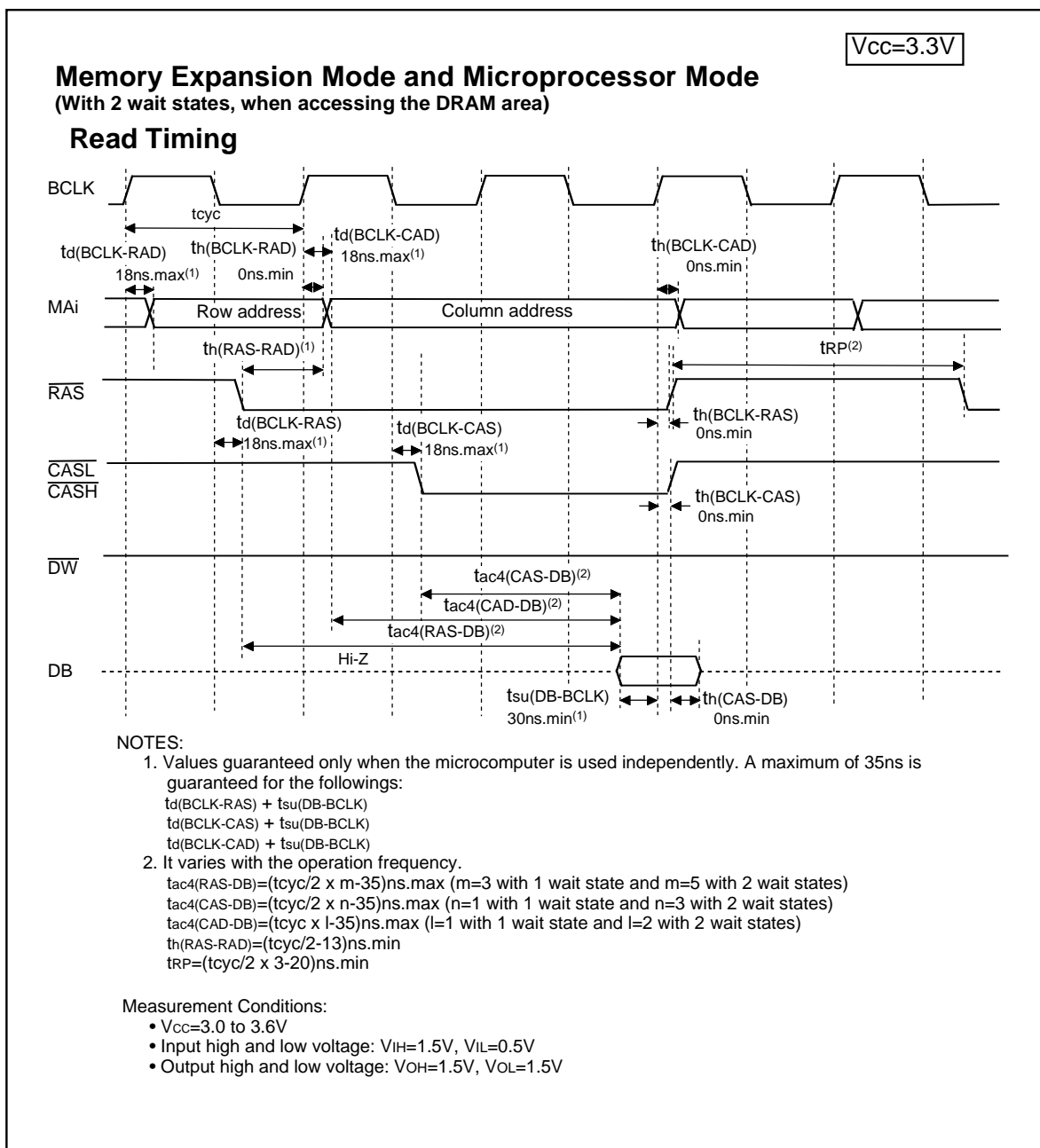
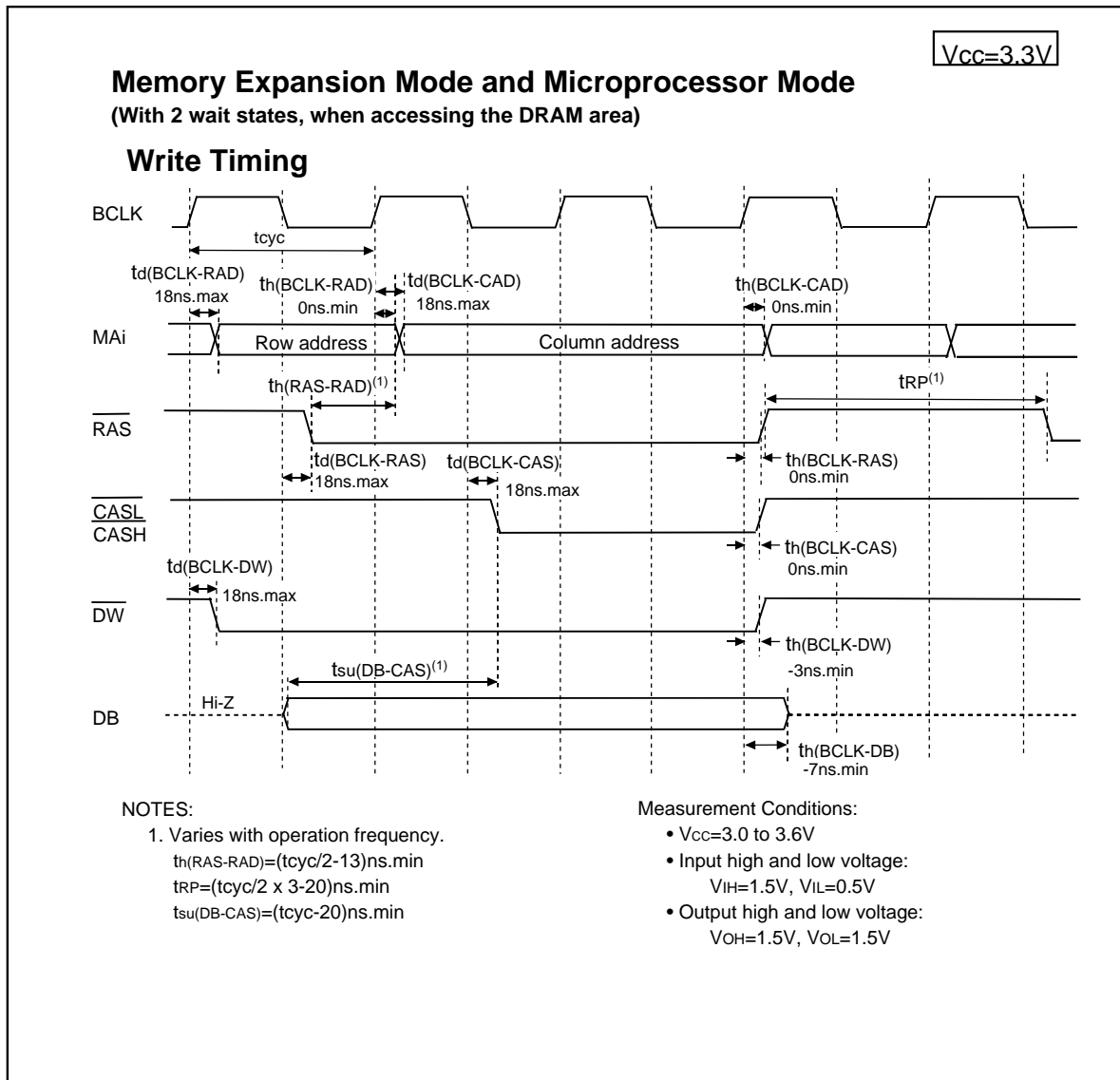
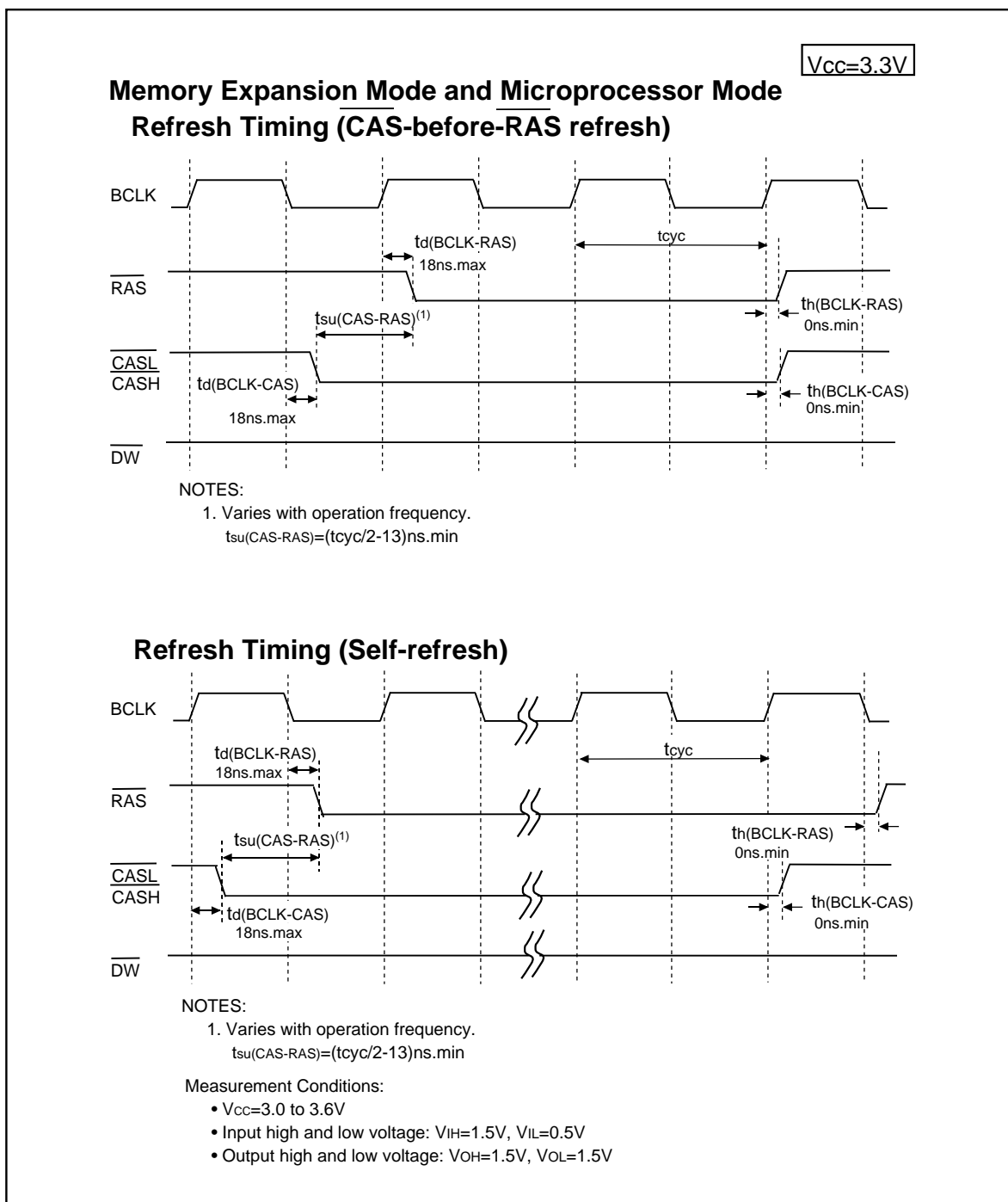


Figure 26.12 V_{CC}=3.3V Timing Diagram (3)

Figure 26.13 $V_{CC}=3.3V$ Timing Diagram (4)

Figure 26.14 $V_{CC}=3.3V$ Timing Diagram (5)

Figure 26.15 V_{CC}=3.3V Timing Diagram (6)

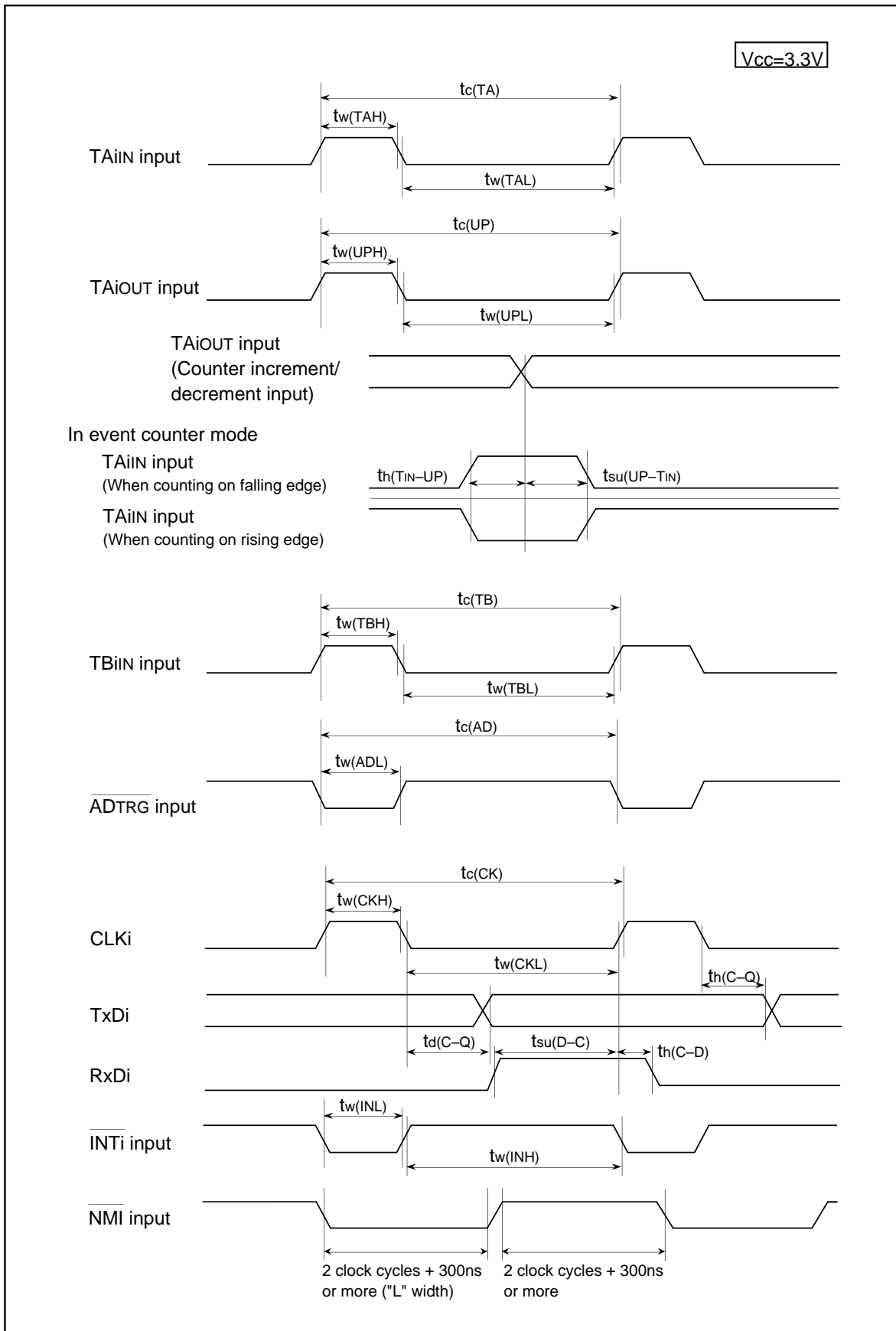
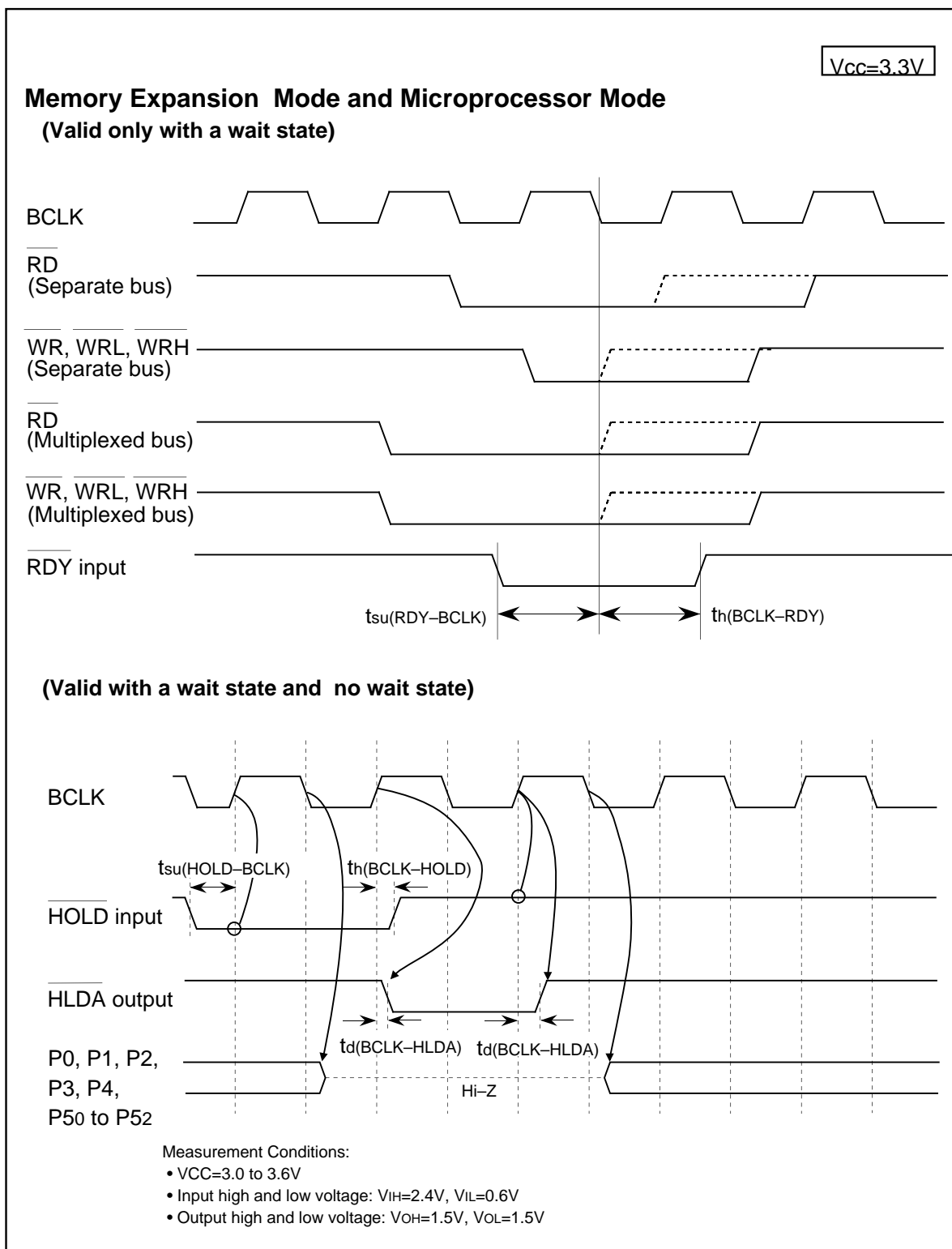


Figure 26.16 $V_{CC}=3.3V$ Timing Diagram (7)

Figure 26.17 V_{CC}=3.3V Timing Diagram (8)

26.2 Electrical Characteristics (M32C/83T)

Table 26.45 Absolute Maximum Ratings

Symbol	Parameter	Condition	Value	Unit
V _{CC}	Supply Voltage	V _{CC} =AV _{CC}	-0.3 to 6.0	V
AV _{CC}	Analog Supply Voltage	V _{CC} =AV _{CC}	-0.3 to 6.0	V
V _I	Input Voltage	RESET, CNV _{SS} , BYTE, P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₇ , P4 ₀ -P4 ₇ , P5 ₀ -P5 ₇ , P6 ₀ -P6 ₇ , P7 ₂ -P7 ₇ , P8 ₀ - P8 ₇ , P9 ₀ -P9 ₇ , P10 ₀ -P10 ₇ , P11 ₀ -P11 ₄ , P12 ₀ -P12 ₇ , P13 ₀ -P13 ₇ , P14 ₀ -P14 ₆ , P15 ₀ -P15 ₇ ⁽¹⁾ , V _{REF} , X _{IN}	-0.3 to V _{CC} +0.3	V
		P7 ₀ , P7 ₁	-0.3 to 6.0	V
V _O	Output Voltage	P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₇ , P4 ₀ -P4 ₇ , P5 ₀ - P5 ₇ , P6 ₀ -P6 ₇ , P7 ₂ -P7 ₇ , P8 ₀ -P8 ₄ , P8 ₆ , P8 ₇ , P9 ₀ -P9 ₇ , P10 ₀ -P10 ₇ , P11 ₀ -P11 ₄ , P12 ₀ -P12 ₇ , P13 ₀ -P13 ₇ , P14 ₀ - P14 ₆ , P15 ₀ -P15 ₇ ⁽¹⁾ , X _{OUT}	-0.3 to V _{CC} +0.3	V
P _d	Power Dissipation	Topr=25° C	400	mW
Topr	Operating Ambient Temperature	T version	-40 to 85	° C
Tstg	Storage Temperature		-65 to 150	° C

NOTES:

1. P11 to P15 are provided in the 144-pin package.

Table 26.46 Recommended Operating Conditions**(V_{CC}=4.2 to 5.5V, V_{SS}=0V at Topr = -40 to 85°C (T version) unless otherwise specified)**

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
V _{CC}	Supply Voltage		4.2	5.0	5.5	V
AV _{CC}	Analog Supply Voltage			V _{CC}		V
V _{SS}	Supply Voltage			0		V
AV _{SS}	Analog Supply Voltage			0		V
V _{IH}	Input High ("H") Voltage	P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₇ , P4 ₀ -P4 ₇ , P5 ₀ -P5 ₇ , P6 ₀ -P6 ₇ , P7 ₂ -P7 ₇ , P8 ₀ -P8 ₇ ⁽³⁾ , P9 ₀ -P9 ₇ , P10 ₀ -P10 ₇ , P11 ₀ -P11 ₄ , P12 ₀ -P12 ₇ , P13 ₀ -P13 ₇ , P14 ₀ -P14 ₆ , P15 ₀ -P15 ₇ ⁽⁴⁾ , X _{IN} , RESET, CNV _{SS} , BYTE P7 ₀ , P7 ₁	0.8V _{CC}		V _{CC}	V
V _{IL}	Input Low ("L") Voltage	P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₇ , P4 ₀ -P4 ₇ , P5 ₀ -P5 ₇ , P6 ₀ -P6 ₇ , P7 ₀ -P7 ₇ , P8 ₀ -P8 ₇ ⁽³⁾ , P9 ₀ -P9 ₇ , P10 ₀ -P10 ₇ , P11 ₀ -P11 ₄ , P12 ₀ -P12 ₇ , P13 ₀ -P13 ₇ , P14 ₀ -P14 ₆ , P15 ₀ -P15 ₇ ⁽⁴⁾ , X _{IN} , RESET, CNV _{SS} , BYTE	0		0.2V _{CC}	V
I _{OH(peak)}	Peak Output High ("H") Current ⁽²⁾	P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₇ , P4 ₀ -P4 ₇ , P5 ₀ -P5 ₇ , P6 ₀ -P6 ₇ , P7 ₂ -P7 ₇ , P8 ₀ -P8 ₄ , P8 ₆ , P8 ₇ , P9 ₀ -P9 ₇ , P10 ₀ -P10 ₇ , P11 ₀ -P11 ₄ , P12 ₀ -P12 ₇ , P13 ₀ -P13 ₇ , P14 ₀ -P14 ₆ , P15 ₀ -P15 ₇ ⁽⁴⁾			-10.0	mA
I _{OH(avg)}	Average Output High ("H") Current ⁽¹⁾	P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₇ , P4 ₀ -P4 ₇ , P5 ₀ -P5 ₇ , P6 ₀ -P6 ₇ , P7 ₂ -P7 ₇ , P8 ₀ -P8 ₄ , P8 ₆ , P8 ₇ , P9 ₀ -P9 ₇ , P10 ₀ -P10 ₇ , P11 ₀ -P11 ₄ , P12 ₀ -P12 ₇ , P13 ₀ -P13 ₇ , P14 ₀ -P14 ₆ , P15 ₀ -P15 ₇ ⁽⁴⁾			-5.0	mA
I _{OL(peak)}	Peak Output Low ("L") Current ⁽²⁾	P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₇ , P4 ₀ -P4 ₇ , P5 ₀ -P5 ₇ , P6 ₀ -P6 ₇ , P7 ₀ -P7 ₇ , P8 ₀ -P8 ₄ , P8 ₆ , P8 ₇ , P9 ₀ -P9 ₇ , P10 ₀ -P10 ₇ , P11 ₀ -P11 ₄ , P12 ₀ -P12 ₇ , P13 ₀ -P13 ₇ , P14 ₀ -P14 ₆ , P15 ₀ -P15 ₇ ⁽⁴⁾			10.0	mA
I _{OL(avg)}	Average Output Low ("L") Current ⁽¹⁾	P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₇ , P4 ₀ -P4 ₇ , P5 ₀ -P5 ₇ , P6 ₀ -P6 ₇ , P7 ₀ -P7 ₇ , P8 ₀ -P8 ₄ , P8 ₆ , P8 ₇ , P9 ₀ -P9 ₇ , P10 ₀ -P10 ₇ , P11 ₀ -P11 ₄ , P12 ₀ -P12 ₇ , P13 ₀ -P13 ₇ , P14 ₀ -P14 ₆ , P15 ₀ -P15 ₇ ⁽⁴⁾			5.0	mA
f(X _{IN})	Main Clock Input Frequency	V _{CC} =4.2 to 5.5V	0		32	MHz
f(X _{CIN})	Sub Clock Oscillation Frequency			32.768	50	kHz

NOTES:

1. Typical values when average output current is 100ms.
2. Total I_{OL(peak)} for P0, P1, P2, P8₆, P8₇, P9, P10, P11, P14 and P15 must be 80mA or less.
Total I_{OH(peak)} for P0, P1, P2, P8₆, P8₇, P9, P10, P11, P14 and P15 must be -80mA or less.
Total I_{OL(peak)} for P3, P4, P5, P6, P7, P8₀ to P8₄, P12 and P13 must be 80mA or less.
Total I_{OH(peak)} for P3, P4, P5, P6, P7₂ to P7₇, P8₀ to P8₄, P12 and P13 must be -80mA or less.
3. V_{IH} and V_{IL} reference for P8₇ applies when P8₇ is used as a programmable input port.
It does not apply when P8₇ is used as X_{CIN}.
4. P11 to P15 are provided in the 144-pin package only.

V_{CC}=5V

**Table 26.47 Electrical Characteristics (V_{CC} = 4.2 to 5.5 V, V_{SS} = 0V
at Topr = -40 to 85°C(T version), f(X_{IN})=32MHz unless otherwise specified)**

Symbol	Parameter	Condition	Standard			Unit		
			Min	Typ	Max			
V _{OH}	Output High ("H") Voltage	P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₇ , P4 ₀ -P4 ₇ , P5 ₀ -P5 ₇ , P6 ₀ -P6 ₇ , P7 ₂ -P7 ₇ , P8 ₀ -P8 ₄ , P8 ₆ , P8 ₇ , P9 ₀ -P9 ₇ , P10 ₀ -P10 ₇ , P11 ₀ -P11 ₄ , P12 ₀ -P12 ₇ , P13 ₀ -P13 ₇ , P14 ₀ -P14 ₆ , P15 ₀ -P15 ₇ ⁽¹⁾	I _{OH} =-5mA	V _{CC} -2.0			V	
		P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₇ , P4 ₀ -P4 ₇ , P5 ₀ -P5 ₇ , P6 ₀ -P6 ₇ , P7 ₂ -P7 ₇ , P8 ₀ -P8 ₄ , P8 ₆ , P8 ₇ , P9 ₀ -P9 ₇ , P10 ₀ -P10 ₇ , P11 ₀ -P11 ₄ , P12 ₀ -P12 ₇ , P13 ₀ -P13 ₇ , P14 ₀ -P14 ₆ , P15 ₀ -P15 ₇ ⁽¹⁾	I _{OH} =-200μA	V _{CC} -0.3				
		X _{OUT}	I _{OH} =-1mA	3.0			V	
		X _{COUT}	No load applied		3.3		V	
V _{OL}	Output Low ("L") Voltage	P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₇ , P4 ₀ -P4 ₇ , P5 ₀ -P5 ₇ , P6 ₀ -P6 ₇ , P7 ₀ -P7 ₇ , P8 ₀ -P8 ₄ , P8 ₆ , P8 ₇ , P9 ₀ -P9 ₇ , P10 ₀ -P10 ₇ , P11 ₀ -P11 ₄ , P12 ₀ -P12 ₇ , P13 ₀ -P13 ₇ , P14 ₀ -P14 ₆ , P15 ₀ -P15 ₇ ⁽¹⁾	I _{OL} =5mA			2.0	V	
		P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₇ , P4 ₀ -P4 ₇ , P5 ₀ -P5 ₇ , P6 ₀ -P6 ₇ , P7 ₀ -P7 ₇ , P8 ₀ -P8 ₄ , P8 ₆ , P8 ₇ , P9 ₀ -P9 ₇ , P10 ₀ -P10 ₇ , P11 ₀ -P11 ₄ , P12 ₀ -P12 ₇ , P13 ₀ -P13 ₇ , P14 ₀ -P14 ₆ , P15 ₀ -P15 ₇ ⁽¹⁾	I _{OL} =200μA			0.45	V	
		X _{OUT}	I _{OL} =1mA			2.0	V	
		X _{COUT}	No load applied		0		V	
V _{TH} -V _{TL}	Hysteresis	HOLD, RDY, TA0 _{IN} -TA4 _{IN} , TB0 _{IN} -TB5 _{IN} , INT0-INT5, AD _{TRG} , CTS0-CTS4, CLK0-CLK4, TA0 _{OUT} -TA4 _{OUT} , NMI, KI0-KI3, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4		0.2		1.0	V	
		RESET		0.2		1.8	V	
I _{IH}	Input High ("H") Current	P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₇ , P4 ₀ -P4 ₇ , P5 ₀ -P5 ₇ , P6 ₀ -P6 ₇ , P7 ₀ -P7 ₇ , P8 ₀ -P8 ₇ , P9 ₀ -P9 ₇ , P10 ₀ -P10 ₇ , P11 ₀ -P11 ₄ , P12 ₀ -P12 ₇ , P13 ₀ -P13 ₇ , P14 ₀ -P14 ₆ , P15 ₀ -P15 ₇ ⁽¹⁾ , X _{IN} , RESET, CNV _{SS} , BYTE	V _I =5V			5.0	μA	
I _{IL}	Input Low ("L") Current	P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₇ , P4 ₀ -P4 ₇ , P5 ₀ -P5 ₇ , P6 ₀ -P6 ₇ , P7 ₀ -P7 ₇ , P8 ₀ -P8 ₇ , P9 ₀ -P9 ₇ , P10 ₀ -P10 ₇ , P11 ₀ -P11 ₄ , P12 ₀ -P12 ₇ , P13 ₀ -P13 ₇ , P14 ₀ -P14 ₆ , P15 ₀ -P15 ₇ ⁽¹⁾ , X _{IN} , RESET, CNV _{SS} , BYTE	V _I =0V			-5.0	μA	
R _{PULLUP}	Pull-up Resistance	P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₇ , P4 ₀ -P4 ₇ , P5 ₀ -P5 ₇ , P6 ₀ -P6 ₇ , P7 ₂ -P7 ₇ , P8 ₀ -P8 ₄ , P8 ₆ , P8 ₇ , P9 ₀ -P9 ₇ , P10 ₀ -P10 ₇ , P11 ₀ -P11 ₄ , P12 ₀ -P12 ₇ , P13 ₀ -P13 ₇ , P14 ₀ -P14 ₆ , P15 ₀ -P15 ₇ ⁽¹⁾	V _I =0V	30	50	167	kΩ	
R _{fXIN}	Feedback Resistance	X _{IN}			1.5		MΩ	
R _{fXCIN}	Feedback Resistance	X _{CIN}			10		MΩ	
V _{RAM}	RAM Standby Voltage			2.5			V	
I _{CC}	Power Supply Current	Measurement conditions: In single-chip mode, output pins are left open and other pins are connected to V _{SS}	f(X _{IN})=32 MHz, square wave, no division		40	54	mA	
			f(X _{CIN})=32 kHz, with a wait state, Topr=25° C		470		μA	
			Topr=25° C when the clock stops		0.4	20	μA	

NOTES:

1. P11 to P15 are provided in the 144-pin package only.

$V_{CC}=5V$ **Table 26.48 A/D Conversion Characteristics ($V_{CC} = AV_{CC} = V_{REF} = 4.2$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$ at $T_{opr} = -40$ to $85^{\circ}C$ (T version), $f(X_{IN}) = 32MHz$ unless otherwise specified)**

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min	Typ	Max	
-	Resolution	$V_{REF}=V_{CC}$			10	Bits
INL	Integral Nonlinearity Error	$V_{REF}=V_{CC}=5V$	AN ₀ to AN ₇ ANEX ₀ , ANEX ₁		± 3	LSB
					± 7	LSB
	External op-amp connection mode					LSB
DNL	Differential Nonlinearity Error				± 1	LSB
-	Offset Error				± 3	LSB
-	Gain Error				± 3	LSB
RLADDER	Resistor Ladder	$V_{REF}=V_{CC}$	8		40	k Ω
tCONV	10-bit Conversion Time		2.1			μs
tCONV	8-bit Conversion Time		1.8			μs
tSAMP	Sample Time		0.2			μs
VREF	Reference Voltage		2		V_{CC}	V
VIA	Analog Input Voltage		0		V_{REF}	V

NOTES:

1. Divide $f(X_{IN})$, if exceeding 16 MHz, to keep ϕ_{AD} frequency at 16 MHz or less.

Table 26.49 D/A Conversion Characteristics ($V_{CC} = V_{REF} = 4.2$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$ at $T_{opr} = -40$ to $85^{\circ}C$ (T version), $f(X_{IN}) = 32MHz$ unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min	Typ	Max	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
tsu	Setup Time				3	μs
R _o	Output Resistance		4	10	20	k Ω
I _{VREF}	Reference Power Supply Input Current	(Note 1)			1.5	mA

NOTES:

1. Measurement results when using one D/A converter. The DA_i register (i=0, 1) of the D/A converter not being used is set to "00₁₆". The resistor ladder in the A/D converter is excluded. I_{VREF} flows even if the VCUT bit in the ADICON1 register is set to "0" (no VREF connection).

Table 26.50 Flash Memory Version Electrical Characteristics

Parameter	Standard			Unit
	Min	Typ	Max	
Program Time (per page)		8	120	ms
Block Erase Time (per block)		50	600	ms

NOTES:

1. $V_{CC}= 4.2$ to $5.5V$ at $T_{opr}= 0$ to $60^{\circ}C$, unless otherwise specified

Timing Requirements ($V_{CC} = 4.2$ to $5.5V$, $V_{SS} = 0V$ at $T_{opr} = -40$ to $85^{\circ}C$ (T version) unless otherwise specified)

$V_{CC}=5V$

Table 26.51 External Clock Input

Symbol	Parameter	Standard		Unit
		Min	Max	
tc	External Clock Input Cycle Time	33		ns
tw(H)	External Clock Input High ("H") Pulse Width	13		ns
tw(L)	External Clock Input Low ("L") Pulse Width	13		ns
tr	External Clock Rise Time		5	ns
tf	External Clock Fall Time		5	ns

V_{CC}=5V**Timing Requirements**(V_{CC} = 4.2 to 5.5V, V_{SS} = 0V at Topr = -40 to 85°C (T version) unless otherwise specified)**Table 26.52 Timer A Input (Count Source Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{C(TA)}	TA _{in} Input Cycle Time	100		ns
t _{w(TAH)}	TA _{in} Input High ("H") Pulse Width	40		ns
t _{w(TAL)}	TA _{in} Input Low ("L") Pulse Width	40		ns

Table 26.53 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{C(TA)}	TA _{in} Input Cycle Time	400		ns
t _{w(TAH)}	TA _{in} Input High ("H") Pulse Width	200		ns
t _{w(TAL)}	TA _{in} Input Low ("L") Pulse Width	200		ns

Table 26.54 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{C(TA)}	TA _{in} Input Cycle Time	200		ns
t _{w(TAH)}	TA _{in} Input High ("H") Pulse Width	100		ns
t _{w(TAL)}	TA _{in} Input Low ("L") Pulse Width	100		ns

Table 26.55 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{w(TAH)}	TA _{in} Input High ("H") Pulse Width	100		ns
t _{w(TAL)}	TA _{in} Input Low ("L") Pulse Width	100		ns

Table 26.56 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{C(U_P)}	TA _{IOU_T} Input Cycle Time	2000		ns
t _{w(U_{PH})}	TA _{IOU_T} Input High ("H") Pulse Width	1000		ns
t _{w(U_{PL})}	TA _{IOU_T} Input Low ("L") Pulse Width	1000		ns
t _{SU(U_{P-TIN})}	TA _{IOU_T} Input Setup Time	400		ns
t _{H(TIN-U_P)}	TA _{IOU_T} Input Hold Time	400		ns

VCC=5V

Timing Requirements

(VCC = 4.2 to 5.5V, VSS = 0V at Topr = -40 to 85°C (T version) unless otherwise specified)

Table 26.57 Timer B Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{C(TB)}	TB _{IN} Input Cycle Time (counted on one edge)	100		ns
t _{w(TBH)}	TB _{IN} Input High ("H") Pulse Width (counted on one edge)	40		ns
t _{w(TBL)}	TB _{IN} Input Low ("L") Pulse Width (counted on one edge)	40		ns
t _{C(TB)}	TB _{IN} Input Cycle Time (counted on both edges)	200		ns
t _{w(TBH)}	TB _{IN} Input High ("H") Pulse Width (counted on both edges)	80		ns
t _{w(TBL)}	TB _{IN} Input Low ("L") Pulse Width (counted on both edges)	80		ns

Table 26.58 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{C(TB)}	TB _{IN} Input Cycle Time	400		ns
t _{w(TBH)}	TB _{IN} Input High ("H") Pulse Width	200		ns
t _{w(TBL)}	TB _{IN} Input Low ("L") Pulse Width	200		ns

Table 26.59 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{C(TB)}	TB _{IN} Input Cycle Time	400		ns
t _{w(TBH)}	TB _{IN} Input High ("H") Pulse Width	200		ns
t _{w(TBL)}	TB _{IN} Input Low ("L") Pulse Width	200		ns

Table 26.60 A/D Trigger Input

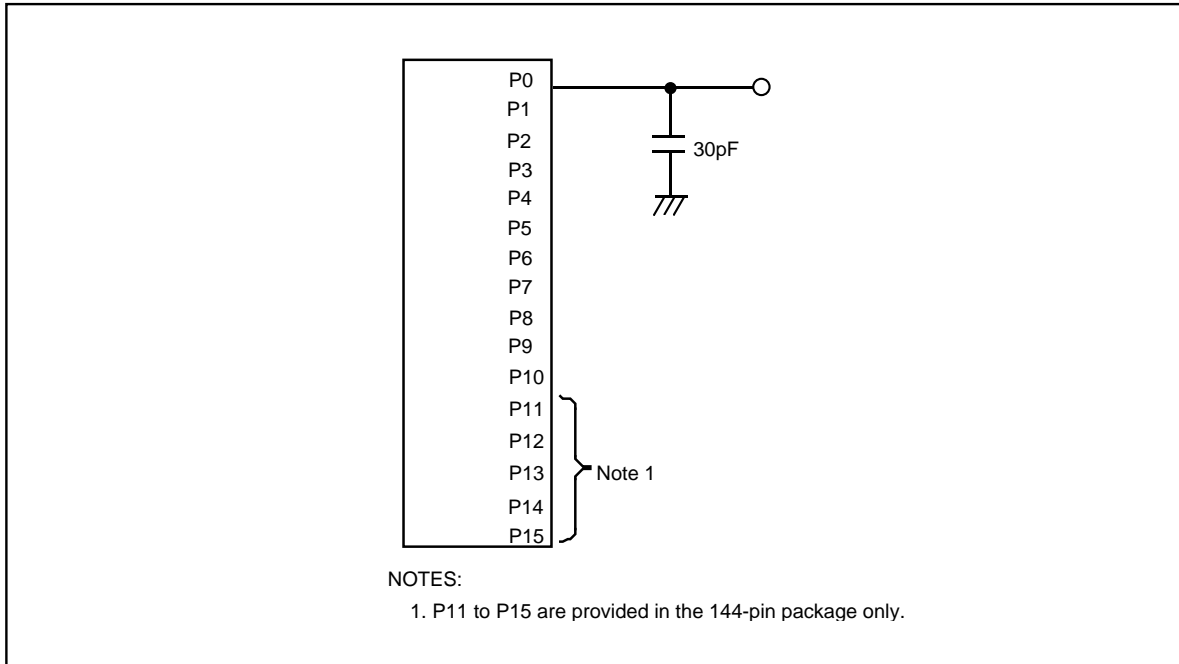
Symbol	Parameter	Standard		Unit
		Min	Max	
t _{C(AD)}	AD _{TRG} Input Cycle Time (required for re-trigger)	1000		ns
t _{w(ADL)}	AD _{TRG} Input Low ("L") Pulse Width	125		ns

Table 26.61 Serial I/O

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{C(CLK)}	CLK _I Input Cycle Time	200		ns
t _{w(CLKH)}	CLK _I Input High ("H") Pulse Width	100		ns
t _{w(CLKL)}	CLK _I Input Low ("L") Pulse Width	100		ns
t _{d(C-Q)}	TxD _I Output Delay Time		80	ns
t _{h(C-Q)}	TxD _I Hold Time	0		ns
t _{SU(D-Q)}	RxD _I Input Set Up Time	30		ns
t _{h(C-Q)}	RxD _I Input Hold Time	90		ns

Table 26.62 External Interrupt INT_I Input

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{w(INH)}	INT _I Input High ("H") Pulse Width	250		ns
t _{w(INL)}	INT _I Input Low ("L") Pulse Width	250		ns

**Figure 26.18 P0 to P15 Measurement Circuit**

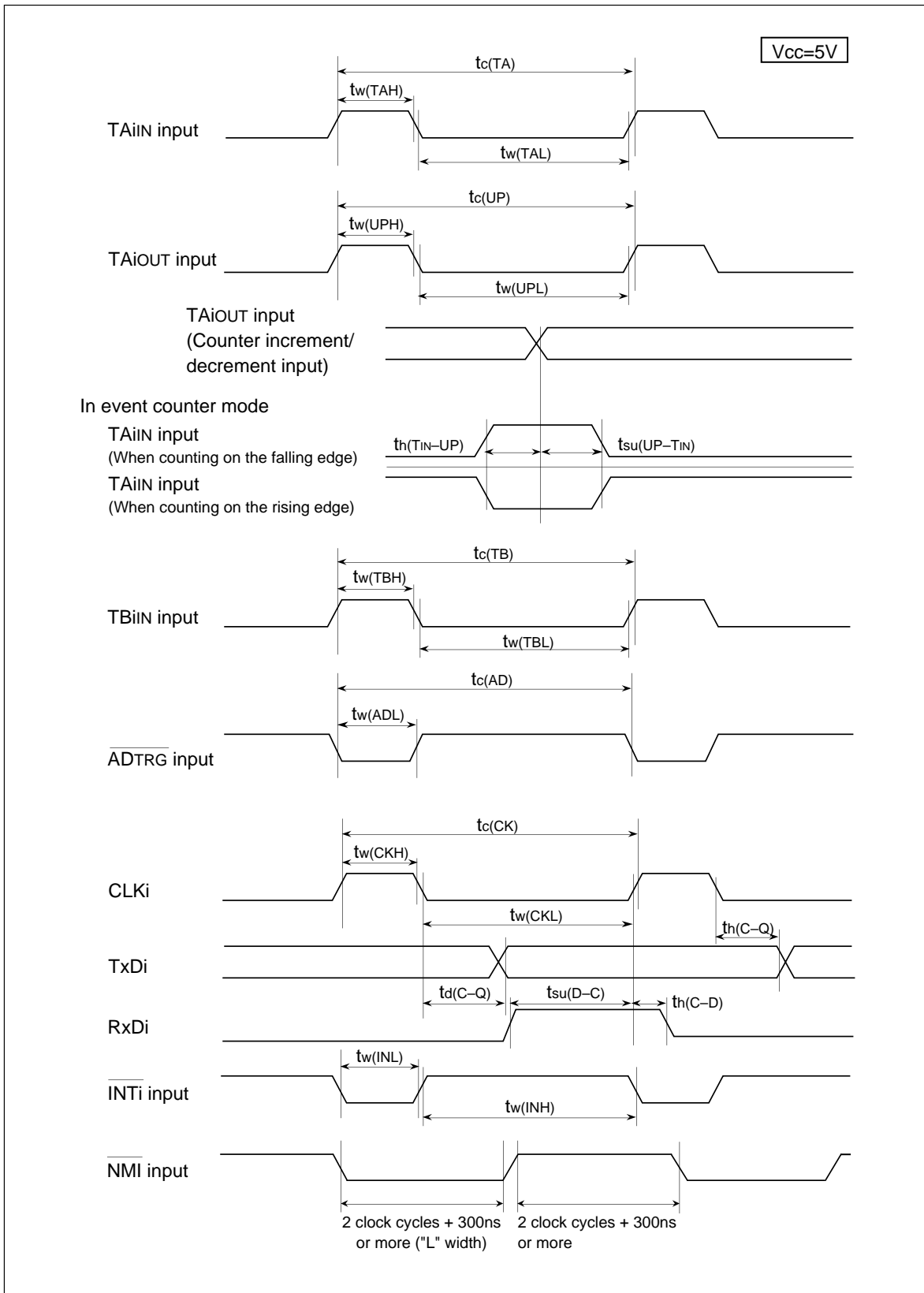


Figure 26.19 VCC = 5 V Timing Diagram(1)

27. Precautions

27.1 Processor Mode

27.1.1 Microprocessor Mode

SFR, internal RAM and external space can be accessed when in microprocessor mode. The internal ROM cannot be accessed.

The internal ROM cannot be accessed, despite entering memory expansion mode or single-chip mode, if the microcomputer begins operation in microprocessor mode while the CNVss is held high ("H") after reset.

27.2 Bus

27.2.1 HOLD Signal

When entering microprocessor mode or memory expansion mode from single-chip mode and using $\overline{\text{HOLD}}$ input, set the PM01 to PM00 bits to "112" (microprocessor mode) or to "102" (memory expansion mode) after setting the PD4_0 to PD4_7 bits in the PD4 register and the PD5_0 to PD5_2 bits in the PD5 register to "0" (input mode).

P40 to P47 (A_{16} to A_{22} , \overline{A}_{23} , $\overline{\text{CS}}_0$ to $\overline{\text{CS}}_3$, MA8 to MA12) and P50 to P52 ($\overline{\text{RD}}/\overline{\text{WR}}/\overline{\text{BHE}}$, $\overline{\text{RD}}/\overline{\text{WRL}}$, $\overline{\text{WRH}}$) do not enter a high-impedance state even when an "L" signal is applied to the $\overline{\text{HOLD}}$ pin, if the PM01 to PM00 bits are set to "112" (microprocessor mode) or to "102" (memory expansion mode) after setting the PD4_0 to PD4_7 bits in the PD4 register and the PD5_0 to PD5_2 bits in the PD5 register to "1" (output mode) in single-chip mode.

27.2.2 External Bus

The internal ROM cannot be read when an "H" signal is applied to the CNVss pin and the hardware reset (hardware reset 1 or hardware reset 2) occurs.

27.3 SFR

27.3.1 100-Pin Package

Set address space for 03CB₁₆, 03CE₁₆, 03CF₁₆, 03D2₁₆, 03D3₁₆ to "FF₁₆" after reset when using the 100-pin package. 03DC₁₆ must be set to "00₁₆" after reset.

27.3.2 Register Settings

Table 27.1 lists registers containing bits which can only be written to. Set these registers with immediate values. When establishing the next value by altering the present value, write the present value to the RAM as well as to the register. Transfer the next value to the register after making changes in the RAM.

Table 27.1 Registers with Write-only Bits

Register	Address	Register	Address
WDTS register	000E ₁₆	U2BRG register	0339 ₁₆
G0RI register	00EC ₁₆	U2TB register	033B ₁₆ , 033A ₁₆
G1RI register	012C ₁₆	UDF register	0344 ₁₆
G2TB register	016D ₁₆ , 016C ₁₆	TA0 register ⁽¹⁾	0347 ₁₆ , 0346 ₁₆
G3TB register	017D ₁₆ , 017C ₁₆	TA1 register ⁽¹⁾	0349 ₁₆ , 0348 ₁₆
U4BRG register	02F9 ₁₆	TA2 register ⁽¹⁾	034B ₁₆ , 034A ₁₆
U4TB register	02FB ₁₆ , 02FA ₁₆	TA3 register ⁽¹⁾	034D ₁₆ , 034C ₁₆
TA11 register	0303 ₁₆ , 0302 ₁₆	TA4 register ⁽¹⁾	034F ₁₆ , 034E ₁₆
TA21 register	0305 ₁₆ , 0304 ₁₆	U0BRG register	0369 ₁₆
TA41 register	0307 ₁₆ , 0306 ₁₆	U0TB register	036B ₁₆ , 036A ₁₆
DTT register	030C ₁₆	U1BRG register	02E9 ₁₆
ICTB2 register	030D ₁₆	U1TB register	02EB ₁₆ , 02EA ₁₆
U3BRG register	0329 ₁₆	AD0CON2 register	0394 ₁₆
U3TB register	032B ₁₆ , 032A ₁₆		

NOTES :

1. In one-shot timer mode and pulse width modulation mode only.

27.4 Clock Generation Circuit

27.4.1 PLL Frequency Synthesizer

Stabilize supply voltage when using the PLL frequency synthesizer. The ripple of supply voltage at 5V must be less than 10kHz in frequency, 0.5V (peak to peak) in voltage fluctuation range, and 1V/ms in voltage fluctuation rate. The ripple of supply voltage at 3.3V must be less than 100Hz in frequency, 0.2V (peak to peak) in voltage fluctuation range, and 0.1V/ms in voltage fluctuation rate.

27.4.2 Power Consumption Control

- When resetting the microcomputer to exit stop mode, apply an "L" signal to the $\overline{\text{RESET}}$ pin until the main clock oscillation stabilizes.
- Write at least 4 NOP instructions after the WAIT instruction or instructions to set the CM10 bit in the CM1 register to "1" (all clocks stop). When entering wait mode or stop mode, the instruction queue reads ahead to instructions following the WAIT instruction and instructions to set the CM10 bit to "1", and the program stops. The next instruction may be executed before entering wait mode or stop mode, depending on the combination of instructions and their execution timing.
- The followings are suggestions for reducing power consumption when programming or designing systems:
 - Ports:** I/O ports maintains the same state despite the microcomputer entering wait mode or stop mode. Current flows through active output ports. Feedthrough current flows through input ports in a high-impedance state. Set unused ports as input ports and stabilize electrical potential before entering wait mode or stop mode.
 - A/D Converter:** If the A/D conversion is not performed, set the VCUT bit in the AD0CON1 register to "0" (no VREF connection). Set the VCUT bit to "1" (VREF connection) and wait at least 1 μ s before starting the A/D conversion.
 - D/A Converter:** Set the DAi bit (i=0 to 1) in the DACON register to "0" (output disabled) and set the DAi register to "0016" when the D/A conversion is not performed.
 - Peripheral Function Stop:** Set the CM02 bit in the CM0 register while in wait mode to stop unnecessary peripheral functions. However, this does not reduce power consumption because the peripheral function clock (fc32) generating from the sub clock does not stop. When in low-speed mode and low-power consumption mode, do not enter wait mode when the CM02 bit is set to "1" (peripheral clock stops in wait mode).
 - External Clock:** When an external clock is selected as the CPU clock, set the CM05 bit in the CM0 register to "1" (main clock stops). This disables the XOUT pin and reduces power consumption. (When using an external clock input, the clock is applied regardless of the CM05 bit setting.)

27.4.3 Wait Mode

When entering wait mode, the instruction queue reads ahead to instructions following the WAIT instruction, and the program stops. Write at least 4 NOP instructions after WAIT instruction.

27.4.4 Stop Mode

- If stop mode is exited by any reset, apply an "L" signal to the RESET pin until a main clock oscillation is stabilized enough.
- When entering stop mode, the instruction queue reads ahead to instructions following the instruction setting the CM10 bit in the CM1 register to "1" (all clocks stopped), and the program stops. When the microcomputer exits stop mode, the instruction lined in the instruction queue is executed before the interrupt routine for recovery is done.

Write the JMP.B instruction as follows, after the instruction setting the CM10 bit to "1".

```
e.g., bset 0, prcr      ; protection removed
      fset  I          ; I flag set
      bset 0, cm1      ; all clocks stopped (stop mode)
      jmp.b LABEL_001 ; jmp.b instruction executed (no instruction between jmp.b and LABEL)
LABEL_001;
      nop              ; nop (1)
      nop              ; nop (2)
      nop              ; nop (3)
      nop              ; nop (4)
      mov.b #0, prcr   ; Protection set
      •
      •
      •
```

27.5 Protection

The PRC2 bit in the PRCR register is changed to "0" (write disable) when an instruction is written to any address after the PRC2 bit is set to "1" (write enable). Write instruction immediately after setting the PRC2 bit to "1" to change registers protected by the PRC2 bit. Do not generate an interrupt or a DMA transfer between the instruction to set the PRC2 bit to "1" and the following instruction.

27.6 Interrupts

27.6.1 ISP Setting

After reset, the ISP is set to "00000016". The program runs out of control if an interrupt is acknowledged before the ISP is set. Therefore, the ISP must be set before an interrupt request is acknowledged. Set the ISP to an even address, which allows interrupt sequences to be executed at a higher speed.

To use $\overline{\text{NMI}}$ interrupt, set the ISP at the beginning of the program. The $\overline{\text{NMI}}$ interrupt can be acknowledged after the first instruction has been executed after reset.

27.6.2 $\overline{\text{NMI}}$ Interrupt

- $\overline{\text{NMI}}$ interrupt cannot be denied. Connect the $\overline{\text{NMI}}$ pin to VCC via a resistor (pull-up) when not in use.
- The P8_5 bit in the P8 register indicates the $\overline{\text{NMI}}$ pin value. Read the P8_5 bit only to determine the pin level after a $\overline{\text{NMI}}$ interrupt occurs.
- "H" and "L" of a signal applied to the $\overline{\text{NMI}}$ pin must be over 2 CPU clock cycles + 300 ns wide.

27.6.3 $\overline{\text{INT}}$ Interrupt

- Edge sensitive
"H" and "L" of a signal applied to the $\overline{\text{INT}}0$ to $\overline{\text{INT}}5$ pins must be at least 250 ns wide, regardless of the CPU clock.
- Level sensitive
"H" and "L" of a signal applied to the $\overline{\text{INT}}0$ to $\overline{\text{INT}}5$ pins must be at least 1 CPU clock cycle + 200 ns wide. For example, "H" and "L" must be at least 234ns wide if $X_{IN}=30\text{MHz}$ with no division.
- The IR bit may change to "1" (interrupt requested) when switching the polarity of the $\overline{\text{INT}}0$ to $\overline{\text{INT}}5$ pins. Set the IR bit to "0" (no interrupt requested) after selecting the polarity. Figure 27.1 shows an example of the switching procedure for the $\overline{\text{INT}}$ interrupt.

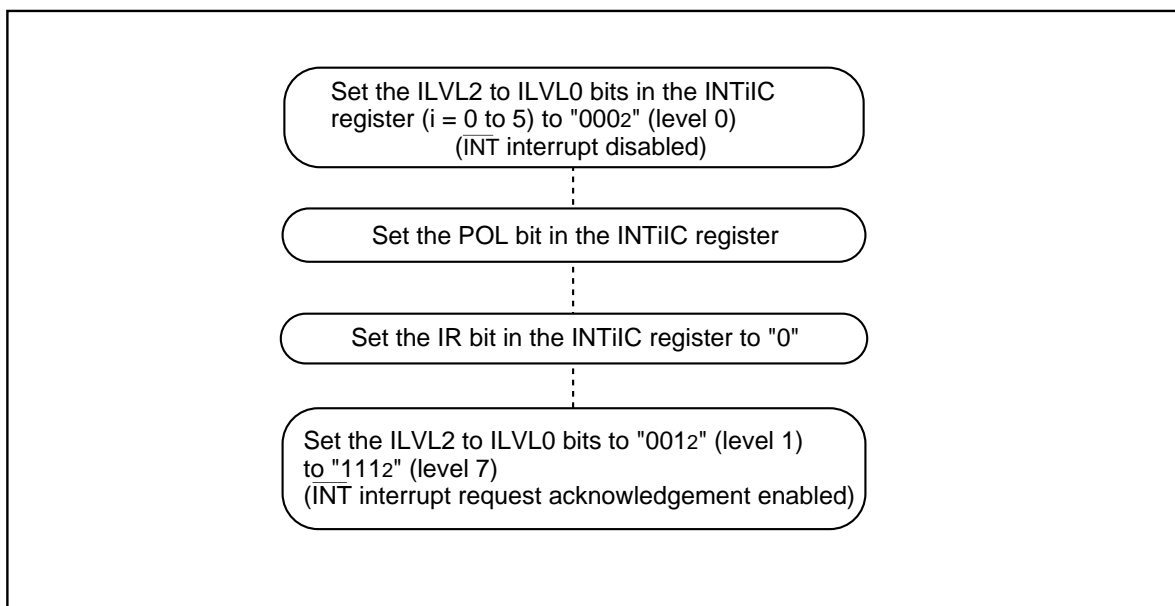


Figure 27.1 Switching Procedure for $\overline{\text{INT}}$ Interrupt

27.6.4 Watchdog Timer Interrupt

Reset the watchdog timer after a watchdog timer interrupt occurs.

27.6.5 Changing Interrupt Control Register

To change the interrupt control register while the interrupt request is disabled, follow the instructions below.

Changing Bits Except IR Bit

When an interrupt request occurs while executing an instruction, the IR bit may not be set to "1" (interrupt requested) and the interrupt may be ignored. If this is a problem, use the following instructions to change the register: AND, OR, BCLR, BSET

Changing IR bit

The IR bit may not change to "0" (no interrupt requested) depending on the instructions written. If this is a problem, use the following instruction to change the register: MOV

27.6.6 Changing IIOiIR Register (i = 0 to 11)

Use the following instructions to set bits 1 to 7 in the IIOiIR register to "0" (no interrupt requested).
AND, BCLR

27.6.7 Changing RLVL Register

The DMAII bit is indeterminate after reset. When using the DMAII bit to generate an interrupt, set the interrupt control register after setting the DMACII bit to "0" (interrupt priority level 7 available for interrupts).

27.7 DMAC

- Set DMAC-associated registers while the MDi1 to MDi0 bits (i=0 to 3) in the channel to be used are set to "002" (DMA disabled). Set the MDi1 to MDi0 bits to "012" (single transfer) or "112" (repeat transfer) at the end of the setup procedure to start DMA requests.
- Do not set the DRQ bit in the DMiSL register to "0" (no request).
When a DMA request is generated but the receiving channel is not ready to receive⁽¹⁾, the DMA transfer does not occur and the DRQ bit is set to "0".

NOTES:

1. The MDi1 to MDi0 bits are set to "002" or the DCTi register is set to "000016" (transferred 0 times).
- To start a DMA transfer by a software trigger, set the DSR bit and DRQ bit in the DMiSL register to "1" simultaneously.
e.g.,
OR.B #0A0h,DMiSL Set the DSR and DRQ bits to "1" simultaneously.
 - Do not generate a channel i DMA request when setting the MDi1 to MDi0 bits in the DMDj register (j=0,1) corresponding to channel i to "012" (single transfer) or "112" (repeat transfer), if the DCTi register of channel i is set to "1".
 - Select the peripheral function which causes the DMA request after setting the DMA-associated registers. If none of the conditions above (setting \overline{INT} interrupt as DMA request source) apply, do not write "1" to the DCTi register.
 - Enable DMA⁽²⁾ after setting the DMiSL register (i=0 to 3) and waiting 6 BCLK cycles or more by program.

NOTES:

2. DMA is enabled when the values set in the MDi1 to MDi0 bits in the DMDj register are changed from "002" (DMA disabled) to "012" (single transfer) or "112" (repeat transfer).

27.8 Timer

27.8.1 Timers A and B

The timers stop after reset. Set the TAI*S*(*i*=0 to 4) bit or TB*S*(*j*=0 to 5) bit in the TABSR register or TBSR register to "1" (starts counting) after setting operation mode, count source and counter.

Set the following registers and bits while the TAI*S* bit or TB*S* bit is set to "0" (stops counting).

- TAI*M*R, TB*j*M*R* register
- TAI, TB*j* register
- UDF register
- TAZIE, TA0TGL, TA0TGH bits in the ONFS register
- TRGSR register

27.8.2 Timer A

27.8.2.1 Timer A (Timer Mode)

- (a) The TAI*S* bit (*i*=0 to 4) in the TABSR register is set to "0" (stops counting) after reset. Set the TAI*S* bit to "1" (starts counting) after selecting operation mode and setting the TAI register.
- (b) The TAI register indicates the counter value during counting at any given time. However, the counter will read "FFFF16" when reloading. The setting value can be read after setting the TAI register while the counter is stopped and before the counter starts counting.
- (c) TA1OUT, TA2OUT and TA4OUT pins are placed in high-impedance states when an "L" signal is applied to the $\overline{\text{NMI}}$ pin while INV03 to INV02 bits in the INVC0 register are set to "112" (forced cutoff of the three-phase output by an "L" signal applied to the $\overline{\text{NMI}}$ pin)

27.8.2.2 Timer A (Event Counter Mode)

- (a) TAI*S* (*i*=0 to 4) bit in the TABSR register is set to "0" (stops counting) after reset. Set the TAI*S* bit to "1" (starts counting) after selecting operation mode and setting the TAI register.
- (b) The TAI register indicates the counter values during counting at any given time. However, the counter will read "FFFF16" during underflow and "000016" during overflow, when reloading. The setting value can be read after setting the TAI register while the counter is stopped and before the counter starts counting.
- (c) The TA1OUT, TA2OUT and TA4OUT pins are placed in high-impedance states when an "L" signal is applied to the $\overline{\text{NMI}}$ pin while the INV03 to INV02 bit in the INVC0 register are set to "112" (forced cutoff of the three-phase output by an "L" signal applied to the $\overline{\text{NMI}}$ pin).

27.8.2.3 Timer A (One-shot Timer Mode)

- (a) TAI*S* (*i*=0 to 4) bit in the TABSR register is set to "0" (stops counting) after reset. Set TAI*S* bit to "1" (starts counting) after selecting operation mode and setting the TAI register.
- (b) The followings occur when setting the TABSR register to "0" (stops counting) while counting:
 - The counter stops counting and the microcomputer reloads contents of the reload register.
 - The TAIOUT pin becomes low ("L").
 - The IR bit in the TAI*I*C register is set to "1" (interrupt requested) after 1 CPU clock cycle.
- (c) The output of the one-shot timer is synchronized with an internal count source. When set to an external trigger, there is a delay of 1 count source cycle maximum, from trigger input to the TAIIN pin to the one-shot timer output.

- (d) The IR bit is set to "1" when the timer operation mode is selected as follows:
- one-shot timer mode is selected after reset.
 - timer mode is switched to one-shot timer mode.
 - event counter mode is switched to one-shot timer mode.
- Therefore, set the IR bit to "0" by program when generating a timer Ai interrupt (IR bit), if the timer operation mode is selected as is described above.
- (e) When a trigger is generated while counting, the reload register reloads and continues counting after the counter has downcounted once following a re-trigger. To generate a trigger while counting, wait at least 1 count source cycle after the previous trigger has been generated and generate a re-trigger.
- (f) The TA1OUT, TA2OUT and TA4OUT pins are placed in high-impedance states when an "L" signal is applied to the $\overline{\text{NMI}}$ pin while the INV03 to INV02 bits in the INVC0 register is set to "112" (forced cutoff of the three-phase output by an "L" signal applied to the $\overline{\text{NMI}}$ pin).
- (g) If an external trigger input is selected to start counting in timer A one-shot timer mode, do not provide another external trigger input again for 300 ns before the timer A counter value reaches "000016". One-shot timer may stop counting.

27.8.2.4 Timer A (Pulse Width Modulation Mode)

- (a) TAI*S*(*i*=0 to 4) bit in the TABSR register is set to "0" (stops counting) after reset. Set TAI*S* bit to "1" (starts counting) after selecting an operating mode and setting the TAI register.
- (b) The IR bit is set to "1" when the timer operation mode is selected as follows:
- PWM mode is selected after reset.
 - timer mode is switched to PWM mode.
 - event counter mode is switched to PWM mode.
- Therefore, set the IR bit to "0" by program when generating a timer Ai interrupt (IR bit), if the timer operation mode is selected as is described above.
- (c) The followings occur when the TAI*S* bit is set to "0" (stops counting) while PWM pulse is output:
- The counter stops counting.
 - The IR bit changes to "1" and the output level changes to low ("L") when TAIOUT pin is held high ("H").
 - The IR bit and the output level remain unchanged when TAIOUT pin is held low ("L").
- (d) The TA1OUT, TA2OUT and TA4OUT pins are placed in high-impedance states when an "L" signal is applied to the $\overline{\text{NMI}}$ pin while the INV03 to INV02 bits in the INVC0 register are set to "1" (three-phase output forced cutoff enabled).

27.8.3 Timer B

27.8.3.1 Timer B (Timer Mode, Event Counter Mode)

(a) TBiS (i=0 to 5) bit is set to "0" (stops counting) after reset. Set TBiS bit to "1" (starts counting) after selecting an operation mode and setting the TBi register.

The TB0S to TB2S bits are the bits 5 to 7 in the TABSR register. The TB3S to TB5S bits are bits 5 to 7 in the TBSR register.

(b) The TBi register indicates the counter value during counting at any given time. However, the counter will read "FFFF₁₆" when reloading. The setting value can be read after setting the TBi register while the counter stops and before the counter starts counting.

27.8.3.2 Timer B (Pulse Period/Pulse Width Measurement Mode)

(a) The IR bit in the TBiIC register is set to "1" (overflow) when the valid edge of a pulse to be measured is input and when the timer Bi counter overflows. The MR3 bit in the TBiMR register determines the interrupt source within an interrupt service routine.

(b) Count overflow on a different timer if an interrupt source cannot be determined by the MR3 bit, such as when a pulse to be measured is input at the same time the timer overflows.

(c) To set the MR3 bit in the TBiMR register to "0" (no overflow), set when the TBiS bit is set to "1" (count starts) and at least one count is counted after the MR3 bit is set to "1" (overflow).

(d) The IR bit in the TBiIC register is used to detect overflow only. Use the MR3 bit only to determine interrupt source within an interrupt service routine.

(e) Indeterminate values are transferred to the reload register during the first valid edge input following the start of the count. Timer B interrupt request is not acknowledged at this time.

(f) The counter value is indeterminate at the start of a count. Therefore, the MR3 bit may change to "1" (overflow) and cause timer B interrupt requests to be generated, until a valid edge is input after the count begins.

(g) The IR bit may be set to "1" (interrupt requested) if the MR1 to MR0 bits in the TBiMR register are set to a different value after a count begins. If the MR1 to MR0 bits are rewritten, but to the same value as before, the IR bit remains unchanged.

(h) Pulse width measurement measures pulse width continuously. Use program to determine whether measurement results are high ("H") or low ("L").

27.9 Three-Phase Motor Control Timer Functions

27.9.1 Changing TAI and TAI1 (i=1, 2, 4) Registers

Do not write to the TAI and TAI1 registers at the same time timer B2 underflows. Follow the procedure below when rewriting the TAI1 register.

- (1) Write value to the TAI1 register
- (2) Wait 1 timer Ai count source cycle
- (3) Write the same value to the TAI1 register again

27.10 Serial I/O

27.10.1 Clock Synchronous Serial I/O Mode

27.10.1.1 Transmission / Reception

When the $\overline{\text{RTS}}$ function is used while an external clock is selected, the output level of the $\overline{\text{RTSi}}$ pin is held low ("L") indicating that the microcomputer is ready for reception. The transmitting microcomputer is notified that reception is possible. The output level of the $\overline{\text{RTSi}}$ pin becomes high ("H") when reception begins. Therefore, connecting the $\overline{\text{RTSi}}$ pin to the $\overline{\text{CTS}}$ pin of the transmitting microcomputer synchronizes transmission and reception. The $\overline{\text{RTS}}$ function is disabled if an internal clock is selected.

The $\overline{\text{RTS}}_2$ pin and CLK₂ pin are placed in high-impedance states when an "L" signal is applied to the $\overline{\text{NMI}}$ pin while the INV02 to INV01 bits in the INVC0 register are set to "112" (forced cutoff of the three-phase output by low-level signal ("L") applied to $\overline{\text{NMI}}$ pin).

27.10.1.2 Transmission

When an external clock is selected while the CKPOL bit in the UiC0 register is set to "0" (data is transmitted on the falling edge of the transfer clock and received on the rising edge) and the external clock is held high ("H") or when the CKPOL bit is set to "1" (data is transmitted on the rising edge of the transfer clock and received on the falling edge) and the external clock is held low ("L"), meet the following conditions:

- Set the TE bit in the UiC1 register to "1" (transmit enabled)
- Set the TI bit in the UiC1 register to "0" (data in the UiBT register)
- Apply "L" signal to the $\overline{\text{CTS}}$ pin if the $\overline{\text{CTS}}$ function is selected

27.10.1.3 Reception

Activating the transmitter in clock synchronous serial I/O mode generates the shift clock. Therefore, set for transmission even if the microcomputer is used for reception only. Dummy data is output from the TxDi pin while receiving.

If an internal clock is selected, the shift clock is generated when the TE bit in the UiC1(i=0 to 2) registers is set to "1" (receive enable) and dummy data is set in the UiTB register. If an external clock is selected, the shift clock is generated when the external clock is input into CLK_i pin while the TE bit is set to "1" (receive enable) and dummy data is set in the UiTB register.

When receiving data consecutively while the RE bit in the UiC1(i=0 to 2) register is set to "1" (data in the UiRB register) and the next data is received by the UART_i reception register, an overrun error occurs and the OER bit in the UiRB register becomes "1" (overrun error). In this case, the UiRB register is indeterminate. When overrun error occurs, program both reception and transmission registers to retransmit earlier data. The IR bit in the SiRIC does not change when an overrun error occurs.

When receiving data consecutively, feed dummy data to the low-order byte in the UiTB register every time a reception is made.

When an external clock is selected while the CKPOL bit in the UiC0 register is set to "0" (data is transmitted on the falling edge of the transfer clock and received on the rising edge) and the external clock is held high ("H") or when the CKPOL bit is set to "1" (data is transmitted on the rising edge of the transfer clock and received on the falling edge) and the external clock is held low ("L"), meet the following conditions:

- Set the RE bit in the UiC1 register to "1" (receive enabled)
- Set the TE bit in the UiC1 register to "1" (transmit enabled)
- Set the TI bit in the UiC1 register to "0" (data in the UiTB register)

27.10.2 UART Mode

- Set the UiERE bit in the UiC1 register after setting the UiMR register.
- The $\overline{\text{RTS}}_2$ and CLK₂ pins will enter a high-impedance state when an "L" signal is applied to the $\overline{\text{NMI}}$ pin while the INV03 to INV02 bits in the INVC0 register are set to "112" (forced cutoff of the three-phase output by an "L" signal applied to the $\overline{\text{NMI}}$ pin).

27.10.3 Special Mode 2

The $\overline{\text{RTS}}_2$ and CLK₂ pins will enter high-impedance states when an "L" signal is applied to the $\overline{\text{NMI}}$ pin while the INV03 to INV02 bits in the INVC0 register are set to "112" (forced cutoff of the three-phase output by an "L" signal applied to the $\overline{\text{NMI}}$ pin).

27.11 A/D Converter

- Set the ADiCON0 (i=0,1) (bit 6 excluded), ADiCON1, and ADiCON2 registers while the A/D conversion is stopped (before trigger is generated).
- Wait a minimum of 1 μ s before starting the A/D conversion when changing the VCUT bit in the ADiCON1 register from "0" (VREF no connection) to "1" (VREF connection). Change the VCUT bit from "1" to "0" after the A/D conversion is completed.
- Insert capacitors between pins AVCC, VREF, analog input pin ANjk (j=none, 0, 2, 15; k=0 to 7) and AVSS to prevent latch-ups and malfunctions due to noise and to minimize conversion errors. The same applies to pins Vcc and Vss. Figure 27.2 shows the procedure.

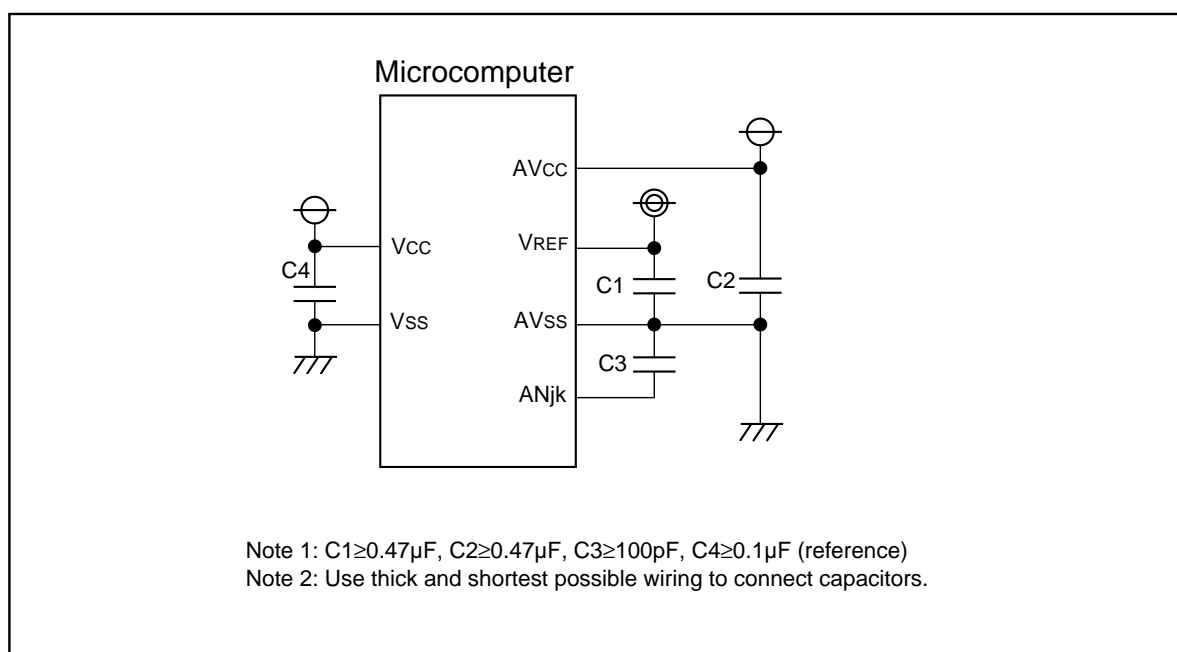


Figure 27.2 Use of Capacitors to Reduce Noise

- Set the bit in the port direction register, which corresponds to the pin being used as the analog input, to "0" (input mode). Set the bit in the port direction register, which corresponds to the $\overline{\text{ADTRG}}$ pin, to "0" (input mode) if the TRG1 to TRG0 bits in the ADiCON2 register are set to "002" ($\overline{\text{ADTRG}}$).
- When generating a key input interrupt, do not use the AN4 to AN7 pins as analog input pins (key input interrupt request is generated when the A/D input voltage becomes "L").
- When the sample and hold function is not activated, \emptyset_{AD} frequency must be 250kHz or more. If the sample and hold function is activated, \emptyset_{AD} frequency must be 1MHz or more.
- Set the CH2 to CH0 bits in the ADiCON0 register or the SCAN1 to SCAN0 bits in the ADiCON1 register to select analog input pins again when changing A/D conversion mode.

- Wrong values are stored in the AD_{ij} register (i=0,1; j=0 to 7) if the CPU reads the AD_{ij} register while the AD_{ij} register is storing results from a completed A/D conversion. This occurs when the CPU clock is set to a divided main clock or a sub clock.

In one-shot mode or single sweep mode, read the corresponding AD_{ij} register after verifying that the A/D conversion has been completed. The IR bit in the AD_iIC register can determine the completion of the A/D conversion.

In repeat mode, repeat sweep mode 0 and repeat sweep mode 1, use an undivided main clock as the CPU clock.

- Conversion results of the A/D_i is indeterminate if the ADST bit in the AD_iCON0 register (i=0,1) is set to "0" (A/D conversion stopped) and the conversion is forcibly terminated by program. The AD_{ij} register (j=0 to 7) not performing an A/D conversion may also be indeterminate.

If A/D_i is forcibly terminated, do not use any values obtained from the AD_{ij} registers.

If either A/D0 or A/D1 is forcibly terminated while the ADS bit in the AD_iCON2 register is set to "0" (channel replacement disabled), the other A/D converter, A/D_i, will perform normally. The values of AD_{ij} registers not performing an A/D conversion remain unchanged.

27.12 Intelligent I/O

27.12.1 Register Setting

Operations controlled by the values written to the GiBT (i=0 to 3), GiBCR1, B TSR, GjTMCR0 to GjTMCR7 (j=0,1), GiTPR6, GiTPR7, GjTM0 to GjTM7, GiPOCR0 to GiPOCR7, GiPO0 to GiPO7, G3MK4 to G3MK7, GjFS, GiFE, G2RTP, and G3RTP registers are affected by the count source (fBTi) set in the BCK1 to BCK0 bits in the GiBCR0 register.

Set the BCK1 to BCK0 bits before setting the GiBT, GiBCR1, B TSR, GjTMCR0 to GjTMCR7, GiTPR6, GiTPR7, GjTM0 to GjTM7, GiPOCR0 to GiPOCR7, GiPO0 to GiPO7, G3MK4 to G3MK7, GjFS, GiFE, G2RTP, and G3RTP registers.

Operations controlled by the values written to the GjRI, GjTO, GiCR, GiRB, GiMR, GjEMR, GjETC, GjERC, GjIRF, GiTB, GjCMP0 to GjCMP3, GjMSK0, GjMSK1, GjTCRC, GjRCRC, IECR, IEAR, IETIF, IERIF, and G3FLG registers are affected by the transfer clock. Set transfer clock before setting the GjRI, GjTO, GiCR, GiRB, GiMR, GjEMR, GjETC, GjERC, GjIRF, GiTB, GjCMP0 to GjCMP3, GjMSK0, GjMSK1, GjTCRC, GjRCRC, IECR, IEAR, IETIF, IERIF, and G3FLG registers.

27.12.2 B TSR Register Setting

The B TSR register is located in the intelligent I/O group 2. When starting the base timer using the BTiS bit in the B TSR register, set the BTiS bit to "1" (base timer starts counting) after selecting the count source for the intelligent I/O group 2. If the BTiS bit is not being used, set the BTiS bit to "0" (base timer reset) after selecting the count source for the intelligent I/O group 2.

Set only either the BTiS bit or the B TS bit in the GiBCR1 register to "1" when starting the base timer. If both BTiS bit and the B TS bit are set to "0", both bits must be set "0" when stopping the base timer.

27.13 Programmable I/O Port

Because ports P72 to P75, P80, and P81 have the three-phase PWM output forced cutoff function, they are affected by the three-phase motor control timer function and the $\overline{\text{NMI}}$ pin when these ports are set for output functions (port output, timer output, three-phase PWM output, serial I/O output, intelligent I/O output).

Table 27.2 shows the relationship between the INVC0 register setting, the $\overline{\text{NMI}}$ pin input level and the state of output ports.

Table 27.2 INVC0 Register and the $\overline{\text{NMI}}$ Pin

Setting Value of INVC0 Register		Input Level to $\overline{\text{NMI}}$ Pin	States of P72 to P75, P80, and P81 Pins (when setting an output pin)
INV02 bit	INV03 bit		
0 (not using three-phase motor control function)	-	-	Output functions selected in the PS1, PSL1, PSC, PS2, and PSL2, registers
1 (using three-phase motor control timer function)	0 (three-phase PWM output disabled)	-	High-impedance
	1 (three-phase PWM output enabled) ⁽¹⁾	H	Output functions selected in the PS1, PSL1, PSC, PS2, and PSL2, registers
		L (forcibly terminated)	High-impedance

NOTES :

1. The INV03 bit is set to "0" after an "L" signal is applied to the $\overline{\text{NMI}}$ pin.

The input threshold voltage differs with programmable I/O ports and peripheral functions. Therefore, if the level of the voltage applied to a pin shared by both programmable I/O ports and peripheral functions is not within the recommended operating condition, V_{IH} and V_{IL} (neither "H" nor "L"), the level determined will differ with the programmable I/O ports and peripheral functions.

27.14 Flash Memory Version

27.14.1 Differences Between Flash Memory Version and Masked ROM Version

Due to differences in internal ROM and layout pattern, flash memory version and mask ROM version have varying electrical characteristics such as attributes, performance margins, noise endurance capacity, and noise radiation. When switching to masked ROM version, administer system evaluation tests equal to those held on the flash memory version.

27.15 Noise

Connect a bypass capacitor (approx. 0.1 μ F) between Vcc and Vss by shortest path, using thick wires.

27.16 Low Voltage Operations

The voltage down converter (VDC) is a circuit used to step down external supply voltage to the internal operation voltage of 3.3V. Disconnect the VDC when applying a 3.3V supply voltage to reduce power consumption.

Figure 27.3 shows the procedure for disconnecting the VDC.

Perform these settings immediately after reset, while the CPU clock is divided by 8. Do not set the VDC0 register (001B₁₆) to other values. Furthermore, do not write to the VDC0 register when applying a supply voltage of 3.3V or more.

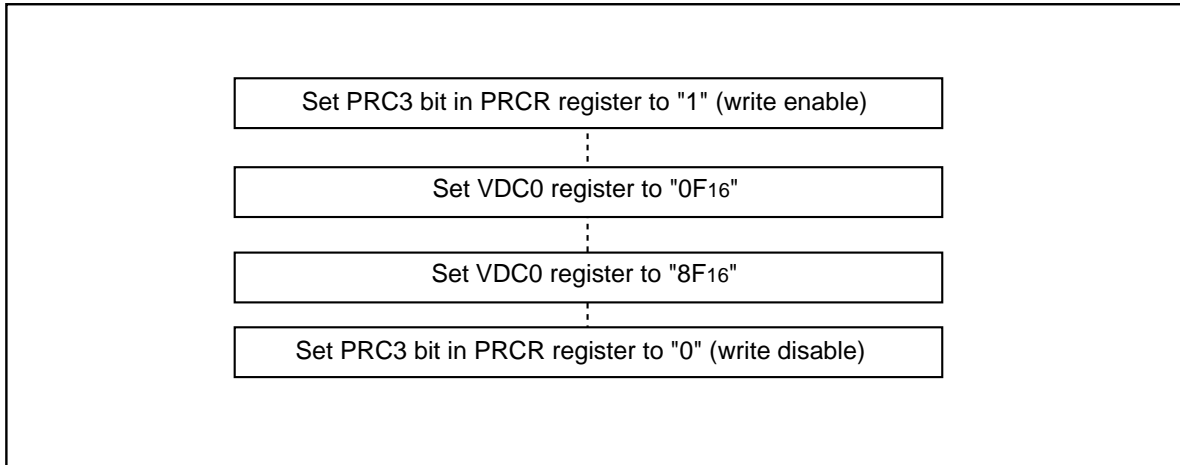


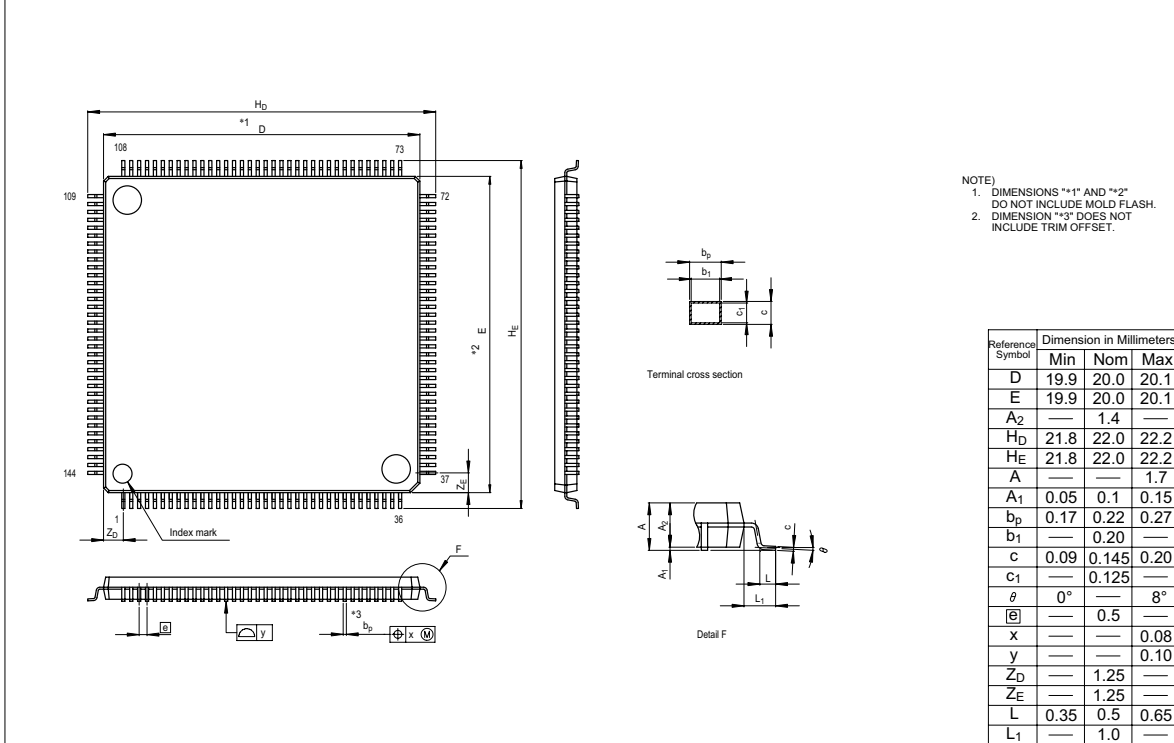
Figure 27.3 VDC Disconnection Procedure

Package Dimensions

PLQ0144KA-A (144P6Q-A)

Plastic 144pin 20 X 20 mm body LQFP

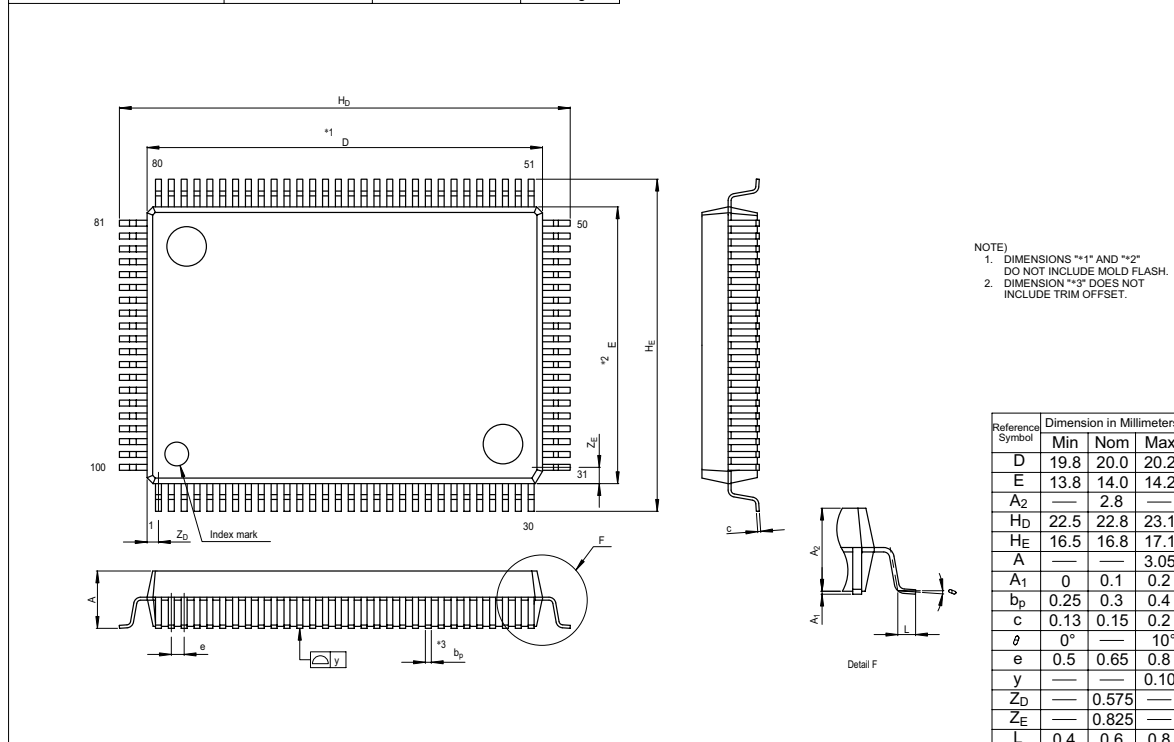
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP144-20x20-0.50	PLQP0144KA-A	144P6Q-A / FP-144L / FP-144LV	1.2g



PRQP0100JB-A (100P6S-A)

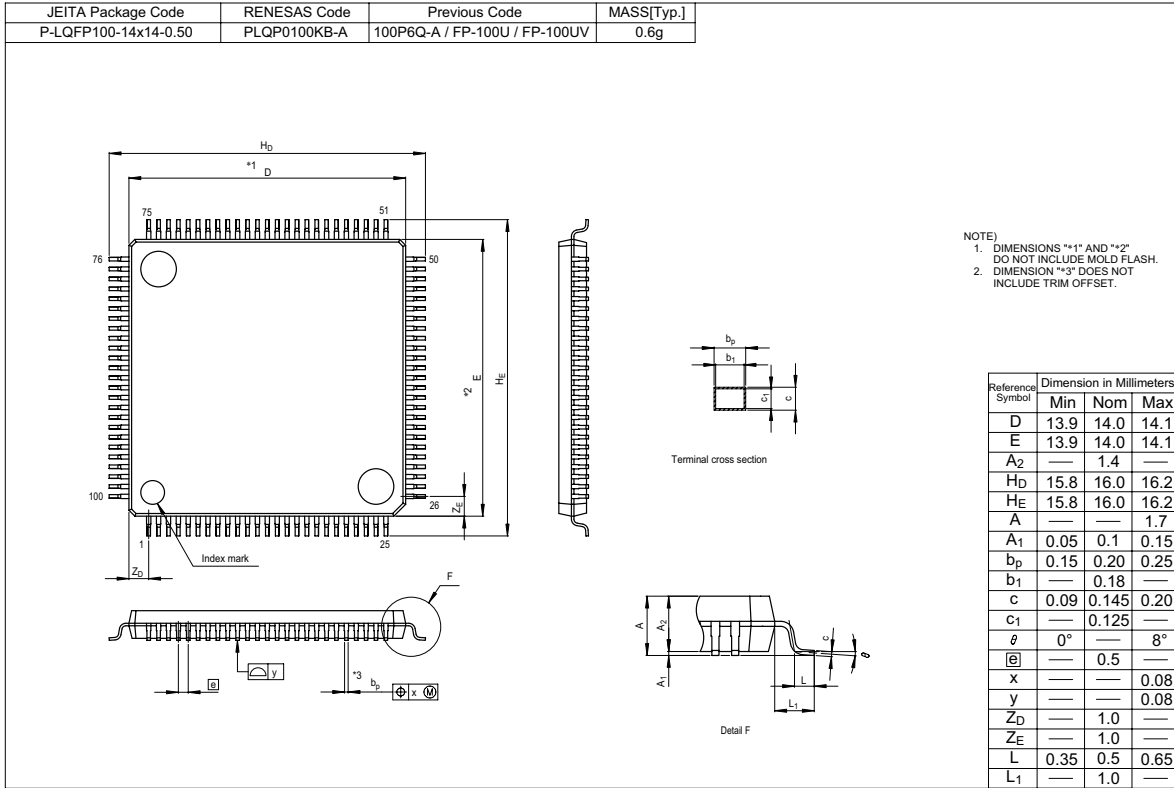
Plastic 100pin 14 X 20 mm body LQFP

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-QFP100-14x20-0.65	PRQP0100JB-A	100P6S-A	1.6g



PLQP0100KB-A (100P6Q-A)

Plastic 100pin 14 X 14 mm body LQFP



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REVISION HISTORY

M32C/83 GROUP (M32C/83, M32C/83T) Hardware Manual

Rev.	Date	Description	
		Page	Summary
1.01	2002-12	All	Full-fledged revision <ul style="list-style-type: none"> • Modify the notation system of registers and bits
		23	Reset <ul style="list-style-type: none"> • Delete the figure “Device’s internal status after a reset is cleared”.
		65	System Clock <ul style="list-style-type: none"> • Modify the figure “Clock Generation Circuit”. • Add descriptions about the ‘PLL clock’. • Modify the figure “Status Transition”.
		88	Interrupt <ul style="list-style-type: none"> • Modify the figure “Intelligent I/O Interrupt and CAN Interrupt”. • Add tables ‘registers to be used and settings’. • Change symbols of the bits in the interrupt request register. • Change symbols of the bits in the interrupt enable register.
		137	Timer A <ul style="list-style-type: none"> • Modify the figure “Timer A Configuration”. • Add tables ‘registers to be used and settings’.
		154	Timer B <ul style="list-style-type: none"> • Modify the figure “Timer B Configuration”. • Add tables ‘registers to be used and settings’.
		163	Three-Phase Control Timer Function <ul style="list-style-type: none"> • Change the bit name, the ‘INV17bit’ in the INVC1 register to reserved bit.
		174	Serial I/O <ul style="list-style-type: none"> • Modify the figure “UARTi Block Diagram”. • Add the table ‘registers to be used and settings’ in each mode. • Add distributions about the ‘clock-divided synchronous function (GCI mode)’. • Add descriptions about the ‘bus conflict detect function (IE mode)’.
		264	Intelligent I/O <ul style="list-style-type: none"> • Modify the figure “Intelligent I/O Group 0 Block Diagram”. • Modify the figure “Intelligent I/O Group 1 Block Diagram”. • Modify the figure “Intelligent I/O Group 2 Block Diagram”. • Modify the figure “Intelligent I/O Group 3 Block Diagram”. • Add the table ‘registers and settings’ associated with each function and mode. • Add a bit function of ‘the BCK0 to BCK1 bit in the G0BCR0 to G3BCR0 register’. <ul style="list-style-type: none"> -Group 0 and 1 • Add descriptions about the ‘HDLC data processing mode’. -Group 0 and 1 • Add distributions about the ‘IEBus mode’. -Group2 • Add descriptions about the ‘8-bit and 16-bit clock synchronous serial I/O function’. -Group3

REVISION HISTORY

M32C/83 GROUP (M32C/83, M32C/83T) Hardware Manual

Rev.	Date	Description	
		Page	Summary
		338	A/D Convertor <ul style="list-style-type: none"> • Modify the figure "A/D Convertor Block Diagram". • Add the table 'pin settings'.
		355	D/A Convertor <ul style="list-style-type: none"> • Add the table 'pin settings'.
		394	Usage Precaution <ul style="list-style-type: none"> • Add descriptions about the 'PLL synthesizer'. • Add descriptions about the 'Timer A' and 'Timer B'. • Add descriptions about the 'Low-Voltage Operation'.
1.02	2003-1	2-3	Overview <ul style="list-style-type: none"> • Add -40 to 85°C to 'Operating ambient temperature' row in Table 1.1.1 and 1.1.2. • Delete 8-bit or 16-bit clock synchronous serial I/O:1 channel (group3) on 'Peripheral function' row in Table 1.1.2.
		3	
		33	SFR <ul style="list-style-type: none"> • Modify 00?0 X0002 to 0000 X0002 on 'value after RESET' column on '017B16' row.
		78	System Clock <ul style="list-style-type: none"> • Modify 0 to 1 on 'PLC00' column and '10MHz' row in Table 1.8.2. • Modify the PLC02 to PLC0 bits and the PLC05 to PLC04 bits to the PLC0 register in the third step in Figure 1.8.13. • Modify 1 to 0 on 'CM00' column and 'BCLK output' row in Table 1.8.5.
		78	
		80	
		117	DMAC <ul style="list-style-type: none"> • Add the note 3 in Figure 1.11.2.
		141	Timer <ul style="list-style-type: none"> • Modify TA4 and TA1 to TA0 and TA2 on the TA1TGL and TA1TGH in the top figure of Table 1.14.5. • Modify TA4 and TA1 to TA1 and TA3 on the TA2TGL and TA2TGH in the top figure of Table 1.14.5. • Modify TA4 and TA1 to TA2 and TA4 on the TA3TGL and TA3TGH in the top figure of Table 1.14.5. • Modify TA4 and TA1 to TA3 and TA0 on the TA4TGL and TA4TGH in the top figure of Table 1.14.5.
186	Serial I/O <ul style="list-style-type: none"> • Modify PD7_0=0 to PD7_2=0 on 'PD7 register' column and 'CLK2 input' row in Table 1.18.4. • Modify PD7_0=0 to PD7_2=0 on 'PD7 register' column and 'CLK2 input' row in Table 1.19.4. • Modify a function description on 'UiRRM' row in Table 1.20.9. 		
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REVISION HISTORY

M32C/83 GROUP (M32C/83, M32C/83T) Hardware Manual

Rev.	Date	Description	
		Page	Summary
		207	<ul style="list-style-type: none"> • Modify PD7_2=0 to PD7_0=0 on 'PD7 register' column and 'SRxD2 input' row in Table 1.20.11. • Modify PD7_0=0 to PD7_2=0 on 'PD7 register' column and 'CLK2 input' row in Table 1.20.11.
		216	<ul style="list-style-type: none"> • Modify PS3_4=0 to PS3_5=0 on 'PS3 register' column and 'CLK4 input' row in Table 1.20.23.
		226	<p>CAN Module</p> <ul style="list-style-type: none"> • Modify PSL2_2=0 to PSL2_1=0 on 'PSL1 and PSL2 registers' column and 'P82' row in Table 1.21.2.
		296	<p>Intelligent I/O</p> <ul style="list-style-type: none"> • Modify Setting value of the GiPO0 register to Setting value of the GiPOk register as n and m on the second figure in Figure 1.22.26.
		304	<ul style="list-style-type: none"> • Modify RxD to ISRxD on 'IPOL' row and TxD to ISTxD on 'OPOL' row in Figure 1.22.33.
		315	<ul style="list-style-type: none"> • Modify IPS=1 to IPS1=1 on IPS registers column and 'P112' row in Table 1.22.26.
		317	<ul style="list-style-type: none"> • Modify TCRCRC to TCRCE on 'CRC' row in Table 1.22.28. • Delete SIOiTR and SIOiRR and add SRTiR in note 3 in Table 1.22.28.
		320	<ul style="list-style-type: none"> • Modify IER to OER in note 1 in the second figure of Figure 1.22.42.
		324	<ul style="list-style-type: none"> • Modify SIOiTR to SIO2TR and SIO5RR to SIO2RR in Table 1.22.30 and 1.22.36.
		334	<ul style="list-style-type: none"> • Modify GiCR to G3CR in Table 1.22.41.
		364	<p>DRAMC</p> <ul style="list-style-type: none"> • Modify SRDF to SREF in note 3 in Figure 1.27.1.
		385	<ul style="list-style-type: none"> • Modify IOUTC10 to OUTC10 on 'PSC_3' row in Figure 1.28.14.
		388	<ul style="list-style-type: none"> • Modify P0 to P5 to P1 in note 1 in Table 1.28.17.
		390	<p>Programable I/O Port</p> <ul style="list-style-type: none"> • Modify INPC1 to INPC11 on 'PS1 register' column and 'Bit 4' row in Table 1.28.4.
		391	<ul style="list-style-type: none"> • Modify INPC0 to INPC02 on 'PS2 register' column and 'Bit 0' row in table 1.28.5.
		393	<ul style="list-style-type: none"> • Modify ISCLK input to ISCLK0 input on 'Bit 1' row in table 1.28.12.
		394	<p>Usage Precaution</p> <ul style="list-style-type: none"> • Modify PM0 to PM00 in "HOLD Signal" • Modify all SP to ISP in (1) SP Setting of "Interrupts".
		398	<ul style="list-style-type: none"> • Modify all TAI to TBI in 1. Timer Mode and Event Counter Mode of "Timer B".
		400	<ul style="list-style-type: none"> • Modify the CAN module to the microcomputer in "Resetting CNVSS Pin with H". • Delete a discription of 'Difference between Flash Memory version and Masked ROM'
		429	<p>Electric Characteristics</p> <ul style="list-style-type: none"> • Modify IOH=5mA to IOL=5mA on 'VOL' row and 'Mesurement Condition' column in Table 1.31.3.

Rev.	Date	Description	
		Page	Summary
1.10	2004-3	All Pages	Chapter numbers, section numbers, etc., added; Table and Figure numbers modified; Chapter sequence modified; Word Phrasing in Revision History changed
		2, 3	Overview <ul style="list-style-type: none"> • Tables 1.1 and 1.2 M32C/83 Group Performance Shortest Instruction Execution Time modified: 31.3ns(f(BCLK)=30MHz changed to 31.3ns(f(BCLK)=32MHz, 50ns(f(BCLK)=20MHz added; Performance details of Multifunction Timer, Intelligent I/O, Clock Generating Circuit, and Electrical Characteristics revised; Oscillator Stop Detect Function added; 32MHz added to Supply Voltage and Power Consumption Note 3 added
		4	• Figure 1.1 M32C/83 Block Diagram modified
		5	• Table 1.3 M32C/83 Group Product deleted
		9, 13	• Tables 1.4 and 1.5 Pin Characteristics VREF pin changed from “analog pin” to “control pin”
		15 to 18	• Table 1.6 Pin Description SDA0 to SDA4 changed from “output” to “input”; Descriptions of A/D-related pin functions revised
		20	Central Processing Unit <ul style="list-style-type: none"> • Figure 2.1 CPU Register modified
		23	Memory <ul style="list-style-type: none"> • Figure 3.1 Memory Map Product deleted; Diagram modified
24 to 45	SFR Value after reset and listing sequence modified <ul style="list-style-type: none"> • “? : Indetermination” changed to “X : Indeterminate” • Notation “Users cannot use any symbols with *” deleted • Register names, symbols, and Values after RESET of addresses 001F₁₆ to 0025₁₆, 0030₁₆ to 0035₁₆, 0055₁₆ to 0056₁₆, 01AC₁₆, and 01AE₁₆ to 01BF₁₆ deleted • Notations added to PM0 and TCSPR registers • Value after reset in the RLVL register modified 		
46	Reset <ul style="list-style-type: none"> • Figure 5.1 Reset Circuit modified 		
47	• Figure 5.2 Reset Sequence Diagram modified; Note 1 added		
48	• 5.3 Watchdog Timer Reset added		
49	• Figure 5.3 CPU Register after Reset modified		
50	Processor Mode <ul style="list-style-type: none"> • 6.2.2 Applying Vcc to CNVss Pin Contents added 		

Rev.	Date	Description	
		Page	Summary
		55	Bus
		60	• 7.1.3.2 Multiplexed Bus revised
		64	• 7.2.4 Bus Timing revised
		65	• 7.6 $\overline{\text{RDY}}$ Signal revised
		65	• Figure 7.7 $\overline{\text{RD}}$ Signal Output Extended by $\overline{\text{RDY}}$ Signal modified
		67	Clock Generating Circuit Chapter name changed from "System Clock " to "Clock Generating Circuit"
		67	• Table 8.1 Clock Generation Circuit Specifications Main clock clock frequency modified; "Ceramic oscillator" changed to "Ceramic resonator"; Reference point added to PLL Frequency Synthesizer
		68	• Figure 8.1 Clock Generation Circuit revised
		69	• Figure 8.2 CM0 Register Bit 3 function changed from "Nothing is assigned" to "Reserved Bit"
		72	• Figure 8.5 CM2 Register CM21 bit function modified; Note 5 revised
		75	• Figure 8.8 PLC1 Register Note 3 revised; Note 4 added
		77	• 8.1.2 Sub Clock revised
		79	• Figure 8.11 Switching Procedure form On-chip Oscillator Clock to Main Clock modified
			• 8.1.4 PLL Clock revised
			• Table 8.2 Bit Settings to Use PLL Clock as CPU Clock Source Setting added for when $f(\text{XIN})$ is 8MHz
		80	• Figure 8.13 Procedure to Use PLL Clock as CPU Clock Source modified
		81	• 8.2 CPU Clock and BCLK revised
		84	• 8.5.2.2 Before Entering Wait Mode revised
		85	• 8.5.2.5 Entering Wait Mode added
		86	• 8.5.3 Stop Mode revised
			• 8.5.3.1 Before Entering Stop Mode revised
			• 8.5.3.3 Exiting Stop Mode revised
		87	• 8.5.3.4 Entering Stop Mode added
		88	• Figure 8.15 Status Transition modified
		93	Interrupts
		95	• Table 10.1 Fixed Vector Table Point of reference changed
		99	• Table 10.2 Relocatable Vector Tables Reserved Space added
		99	• Figure 10.5 RLVL Register Value after reset changed; Note 3 revised; Note 4 added
			• 10.6.2.3 RLVL2 to RLVL0 Bits revised
		103	• Figure 10.8 Interrupt Priority "Oscillation Stop Detect" added
		104	• Figure 10.9 Interrupt Priority Level Select Circuit modified
		106	• 10.8 NMI Interrupt revised

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		108	<ul style="list-style-type: none"> • “10.11 Intelligent I/O and CAN Interrupt” changed to “10.11 Intelligent I/O Interrupt and CAN Interrupt” • Precautions pertaining to Interrupts are compiled into one chapter, “27. Precaution”
		111	<p>Watchdog Timer Contents revised</p>
		115	<ul style="list-style-type: none"> • 12. DMAC revised
		114	<ul style="list-style-type: none"> • Table 12.1 DMAC Specifications CAN interrupt added to DNA Request Factors; Note 1 revised • Precautions pertaining to DMAC are compiled into one chapter, “27. Precaution”
		125	<p>DMAC II</p> <ul style="list-style-type: none"> • Table 13.1 DMAC II Specifications Note 2 added
		126	<ul style="list-style-type: none"> • Figure 13.1 RLVL Register Values after reset modified; Note 3 revised; Note 4 added
		129	<ul style="list-style-type: none"> • 13.3 Transfer Data Contents added
		130	<ul style="list-style-type: none"> • 13.4.2 Burst Transfer revised • 13.4.4 Chain Transfer revised
		132	<ul style="list-style-type: none"> • 13.5 Execution Time revised
		135	<p>Timer</p> <ul style="list-style-type: none"> • 14.1 Timer A Contents added
		140	<ul style="list-style-type: none"> • Table 14.1 Pin Settings for Output from TAIout Pin (i= 0 to 4) modified
		149	<ul style="list-style-type: none"> • 14.1.4 Pulse Width Modulation Mode Settings changed for 16-bit PWM and 8-bit PWM
		152	<ul style="list-style-type: none"> • 14.2 Timer B Contents added
		159	<ul style="list-style-type: none"> • Figure 14.22 TB0MR to TB5MR Registers (Pulse Period/ Pulse Width Measurement Mode) Values after reset modified <p>Three-Phase Motor Control Timer Function</p>
		161	<ul style="list-style-type: none"> • Table 15.1 Three-Phase Motor Control Timer Functions Specification modified
		162	<ul style="list-style-type: none"> • Figure 15.1 Three-Phase Motor Control Function Block Diagram modified
		163	<ul style="list-style-type: none"> • Figure 15.2 INVC0 Register modified
		164	<ul style="list-style-type: none"> • Figure 15.3 INVC1 Register modified
		166	<ul style="list-style-type: none"> • Figure 15.5 ICTB2 Register, TA1, TA2, TA4, TA11, TA21 and TA41 Registers and TB2SC Register Notes 2 and 3 added to ICTB2 register; Note 7 added to TAI and TAI1 registers
		168	<ul style="list-style-type: none"> • Figure 15.7 TAI MR Register (i=1, 2, 4) MR1 bit function modified

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		169	• Figure 15.8 Triangular Wave Modulation Operation modified
		170	• Figure 15.9 Sawtooth Wave Modulation Operation modified
		173	Serial I/O • Figure 16.2 U0TB to U4TB Registers and U0RB to U4RB Registers Note 3 added to U0RB to U4RB registers
		175	• Figure 16.4 UiC0 Register Note 3 added to UFORM bit
		176	• Figure 16.5 UiC1 Register Note 2 added to UiLCH bit; Note 1 added to SCLKSTPB (UiERE) bit
		181	• Table 16.1 Clock Synchronous Serial I/O Mode Specifications Explanation of CLK Polarity in Selectable Functions revised
		182 to 219	• Tables 16.2, 16.7, 16.12, 16.19, 16.24, and 16.34 Registers to be Used and Settings Points of reference deleted
		183	• Table 16.3 Pin Settings in Clock Synchronous Serial I/O Mode (1) revised
		184	• Figure 16.10 Transmit and Receive Operation modified
		188	• Table 16.7 Registers to be Used and Settings in UART Mode Function of the UiERE bit in the UiC1 register modified
		189	• Table 16.8 Pin Settings in UART (1) revised
		190	• Figure 16.14 Transmit Operation modified
		192	• Figure 16.17 Serial Data Logic Inverse modified
		195	• Table 16.12 Registers to be Used and Settings (I²C Mode) Setting values for master and slave indicated separately
		196	• Table 16.13 I²C Mode Functions "P61, P65, P72, P90, P75 Pin Functions" changed to "P61, P65, P72, P90, P95 Pin Functions"
		197, 198	• Tables 16.14 to 16.16 Pin Settings in I²C Mode modified
		200	• 16.3.4 Transfer Clock revised
		203	• Table 16.19 Registers to be Used and Settings in Special Mode 2 Functions of the UFORM bit in the UiC0 register and the UiRRM bit in the UiC1 register modified
		204	• Table 16.20 Pin Settings in Special Mode 2 (1) revised • Table 16.21 Pin Settings in Special Mode 2 (2) revised • Table 16.22 Pin Settings in Special Mode 2 (3) revised
		208	• Table 16.23 GCI Mode Specifications Explanations of Transmit/Receive Start Conditions revised
		210	• Table 16.25 Pin Settings in GCI Mode (1) revised • Table 16.26 Pin Settings in GCI Mode (2) revised • Table 16.27 Pin Settings in GCI Mode (3) revised
		213	• Table 16.31 Pin Settings in IE Mode (2) revised • Table 16.32 Pin Settings in IE Mode (3) revised
		219	• Figure 16.29 SIM Interface Operation modified

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		221	• Figure 16.32 SIM Interface Format modified
		223	A/D Converter Sequence of content modified
		226, 227	• Table 17.1 A/D Converter Specifications Explanation of A/D Conversion Start Conditions revised; ϕ A/D frequency modified
		229, 230	• Figure 17.2 AD0CON0 Register, Figure 17.3 AD0CON1 Register ϕ A/D frequency modified
		232	• Figure 17.5 AD1CON0 Register, Figure 17.6 AD1CON1 Register ϕ A/D frequency modified
		235	• Table 17.4 One-shot Mode Specifications Explanation of Start Condition revised
		237	• Table 17.9 Trigger Select Function Settings Table modified; Note 2 added
		238 to 247	• Figure 17.9 Analog Input Pin and External Sensor Equivalent Circuit Capacitance of the capacitor modified Sequence of the following Chapters have been changed: D/A Converter, CRC Calculation, XY Conversion
		248	Intelligent I/O • Figure 21.2 Intelligent I/O Group 1 Block Diagram modified
		251	• Figure 21.5 G0BT to G3BT Registers and G0BCR0 to G3BCR0 Registers Note 2 added to G0BT to G3BT registers, Note 3 deleted from G0BCR0 to G3BCR0 registers
		252	• Table 21.2 Base Timer Specifications Explanation of Counter increment/decrement mode in Selectable Function modified
		263	• Tables 21.3, 21.6, 21.8, 21.17, 21.23, 21.29, 21.31, 21.37, and 21.42 Associated Register Settings Point of reference deleted
		266	• Figure 21.18 Counter Increment Mode (Group 0 and 1) modified
		265	• Figure 21.19 Counter Increment/Decrement Mode (Group 0 and 1) modified
		266	• Figure 21.20 Base Timer Operation in Two-Phase Pulse Signal Processing Mode Note 1 revised
		267	• 21.2 Time Measurement Function (Group 0 and 1) Contents added
		270	• Figure 21.22 Time Measurement Function (2) modified
		271	• Figure 21.23 Prescaler Function and Gate Function Diagram modified; Note 2 of Gate Function deleted
		272	• Table 21.7 Pin Settings for Waveform Generation Function modified
		273	• Table 21.8 Waveform Generation Function Associated Register Settings Note 1 added
		274	• 21.3.1 Single-Phase Waveform Output Mode (Group 0 to 3) revised
		275	• Table 21.9 Single-Phase Waveform Output Mode Specifications revised • Figure 21.24 Single-Phase Waveform Output Mode modified

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		276	• Table 21.10 Phase-Delayed Waveform Output Mode Specifications revised
		277	• Figure 21.25 Phase-Delayed Waveform Output Mode modified
		278	• 21.3.3 Set/Reset Waveform Output (SR Waveform Output) Mode revised
			• Table 21.11 SR Waveform Output Mode Specifications revised
		280	• Figure 21.26 SR Waveform Output Mode modified
		281	• 21.3.4 Bit-Modulation PWM Output Mode revised
			• Table 21.12 Bit Modulation PWM Output Mode revised
			• Figure 21.27 Bit Modulation PWM Mode Pulse numbering added
		283	• 21.3.5 Real-Time Port (RTP) Output Mode (Group 2 and 3) revised
			• Table 21.14 RTP Output Mode Specifications Note 1 added
		284	• Figure 21.29 Real-Time Port Output Mode modified
		285	• 21.3.6 Parallel Real-Time Port Output Mode (Group 2 and 3) revised
			• Table 21.15 Parallel RTP Output Mode Note 1 added
		286	• Figure 21.31 Parallel RTP Output Mode modified
		290	• Figure 21.35 G0EMR to G1EMR Registers and G0ETC to G1ETC Registers Note 1 added
		291	• Figure 21.36 G0ERC to G1ERC Registers Note 1 added
		292	• Figure 21.37 G0IRF to G1IRF Registers and G0TB to G1TB Registers Notes 1 and 2 in G0IRF to G1IRF registers revised; Note 1 added to G0TB to G1TB registers
		293	• Figure 21. 38 G0CMP0 to G0CMP3 Registers, G1CMP0 to G1CMP3 Registers, G0MSK0 to G0MSK1 Registers, G1MSK0 to G1MSK1 Registers, G0TCRC to G1TCRC Registers, and G0RCRC to G1RCRC Registers Note 1 revised and Note 2 added to G0TCRC to G1TCRC registers; Note 3 in G0RCRC to G1RCRC registers revised
		294	• Table 21.16 Clock Synchronous Serial I/O Mode Specifications (Group 0 and 1) Explanation of transfer clock revised
		297	• Table 21.22 UART Mode Specifications (Group 0 and 1) Explanation of transfer clock and Note 2 revised
		301	• Table 21.28 HDLC Processing Mode Specifications (Group 0 and 1) Explanation of transfer clock revised
		308	• Table 21.30 Variable Clock Synchronous Serial I/O Mode Specifications (Group 2) Explanation of transfer clock revised
		312	• Table 21.36 IE Bus Mode Specification Explanation of transfer clock revised
		318	• Table 21.41 Clock Synchronous Serial I/O Mode (Group 3) Explanation of transfer clock revised
		322	CAN Bit symbols of each register are now capitalized (e.g. Reset0 is changed to RESET0)

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		325	• 22.1.1.3 BASICCAN Bit revised
		344	• 22.1.16 CANi Message Slotj Control Register (CiMCTLj Register) (i=0, 1; j=0 to 15) Funtion of the INVALIDDATA/TRMACTIVE bit when set to “1” changed to “Transmits”; Note 4 in REMACTIVE deleted; RW modified to RO
			• Table 22.4 C0MCTLi Register (i=0 to 15) Setting and Transmit/Receive Mode Hyphens (-) changed to “0”
		345	• 22.1.16.4 REMACTIVE Bit revised
		346	• 22.1.16.5 RSPLOCK Bit revised
			Programmable I/O Port
		364	• 24.4 Function Select Register Bk (PSLk Register) (k=0 to 3) revised
		365	• 24.5 Function Select Register C (PSC Register) revised
			• 24.7 Port Control Register (PCR Register) revised
		367	• Figure 24.2 Programmable I/O Ports (2) modified
		369	• Figure 24.5 PD0 to PD15 Registers Note 4 added
		371	• Figure 24.7 PS0 Register and PS1 Register PS0 register revised
		372	• Figure 24.8 PS2 Register and PS3 Register PS3 register revised
		376	• Figure 24.12 PSL0 Register and PSL1 Register Note 1 added to PSL1 register
		377	• Figure 24.13 PSL2 Register and PSL3 Register PSL3 register revised
		378	• Figure 24.14 PSC Register revised
		379	• Figure 24.15 PUR0 Register, PUR1 Register and PUR2 Register Note 1 revised
		383	• Table 24.3 Port P6 Peripheral Function Output Control Bits 3 and 7 modified
			• Table 24.4 Port P7 Peripheral Function Output Control Note 1 added to PSC register; Bit 0 modified
		384	• Table 24.6 Port P9 Peripheral Function Output Control Bit 2 and 6 modified
			Flash Memory Version
		387	• Table 25.1 Flash Memory Version Specifications Supply voltage modified
		389	• 25.2.1 ROM Code Protect Function revised
			• 25.2.2 ID Code Check Function revised
		393	• 25.3.1.3 FMR02 Bit revised
		395	• 25.3.3 Data Protect Function revised
		397	• 25.3.5.3 Clear status Register revised
		405	• 25.3.7.8 Rewriting the User ROM Area
		406	• 25.4.2 ID Code Check Function revised
		412	• 25.5.2 ROM Code Protect Function revised

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		413	Electrical Characteristics • Table 26.1 Absolute Maximum Ratings VREF, XIN P70 and P71 deleted and XOUT added to Output Voltage
		414	• Table 26.2 Recommended Operation Conditions (Vcc= 3.0V to 5.5V at Topr= -20 to 85°C) Maximum value of 50MHz added to f(XCIN) Sub Clock Oscillation Frequency
		416	• Table 26.4 A/D Conversion Characteristics φAD frequency modified
		416, 434	• Tables 26.6 Flash Memory Version Electrical Characteristics added
		450 to 472	Precautions • Overall structure modified
1.20	2004-6	All pages	Words standardized: On-chip oscillator, A/D converter and D/A converter
		111	Interrupts • Figure 10.15 IIO0IE to IIO11IE Registers Note 2 added
		112	Watchdog Timer • Figure 11.1 Watchdog Timer Block Diagram modified
		432 449	Electrical Characteristics • Figure 26.8 Vcc=5V Timing Diagram (7) Figure modified • Figure 26.16 Vcc=3.3V Timing Diagram (7) Figure modified
1.31	2006-1	All Pages	M32C/83T version added; Package code changed: 144P6Q-A to PLQP0144KA-A, 100P6Q-A to PLQP0100KB-A, 100P6S-A to PRQP0100JB-A
		All Pages	Word standardized: Clock Generation Circuit , On-chip Oscillator, A/D Converter, D/A Converter, XY Conversion, Low -power consumption
		1 2, 3 5	Overview • 1.1 Applications Automobile added • Tables 1.1 and 1.2 M32C/83 Group (M32C/83, M32C/83T) Performance • Table 1.3 M32C/83 Group (1) (M32C/83) Information updated • Table 1.3 M32C/83 Group (2) (M32C/83T) M32C/83T product information added • Figure 1.2 Product Numbering System Classification modified • Table 1.4 Pin Characteristics for 144-Pin Package Note 1 added • Table 1.5 Pin Characteristics for 100-Pin Package Note 1 added • Table 1.6 Pin Description modified, notes added
		21	Memory • Figure 3.1 Memory Map modified; Note 2 modified, notes 3 and 4 added
		22 to 23	Special Function Registers (SFR) • Note 2 added
		45	Reset • Figure 5.2 Reset Sequence Note 2 added

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			Processor Mode
		48	• Chapter Note added
		49	• Figure 6.1 PM0 Register Note 9 added
		50	• Figure 6.2 PM1 Register Note 6 added
			Bus
		52	• Chapter note added
			• Figure 7.1 DS Register Note 2 added
		54	• Table 7.2 Processor Mode and Port Function Note 3 modified
		58	• Table 7.3 WCR Register Note 3 added
			Clock Generation Circuit
		67	• Figure 8.2 CM0 Register Function of the CM07 bit modified
		68	• Figure 8.3 CM1 Register Note mark position changed
		71	• Figure 8.6 TCSPR and CPSRF Register Note 2 added for TCSPR register
		74	• Figure 8.9 Main Clock Circuit Connection modified
		75	• Figure 8.10 Sub Clock Connection Circuit modified
		76	• 8.1.3.2 How to Use Oscillation Stop Detect Function partially modified
		78	• Figure 8.12 External Circuit with PLL Frequency Synthesizer modified
		80	• Table 8.5 BLCK/CLKOUT Pin in Memory Expansion Mode and Microprocessor Mode Note 4 added
		81	• 8.5.1 Normal Operation Mode Description partially modified
		82	• 8.5.2 Wait Mode modified
		83	• Table 8.6 Pin States in Wait Mode Note 2 added
		84-85	• 8.5.3 Stop Mode modified
		85	• Table 8.8 Pin Status in Stop Mode Note 2 added
		86	• Figure 8.14 Status Transition in Wait Mode and Stop Mode The mode between stop mode and low-speed mode, low-power consumption mode changed; Note 2 deleted
			Interrupts
		97	• Figure 10.4 Interrupt Control Register (2) Note mark position changed
		98	• Figure 10.5 RLVL Register Note 3 modified
		109	• Figure 10.14 IIO0IR to IIO11IR Registers partially modified
		110	• Figure 10.15 IIO0IE to IIO11IE Registers partially modified
			Watchdog Timer
		113	• Figure 11.3 CM0 Register Function of the CM07 bit modified
			DMAC
		115	• Table 12.1 DMAC Specifications Specification of DMA Transfer Cycles partially modified
		119	• Figure 12.4 DCT0 to DCT3 Registers Notes 3 and 4 modified; DRC0 to DRC3 Registers Notes 2 and 4 modified

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		120	<ul style="list-style-type: none"> • Figure 12.5 DMA0 to DMA Registers Notes 3 and 4 modified; DSA0 to DSA3 Registers Notes 3 and 4 modified
		126 140	<p>DMACII</p> <ul style="list-style-type: none"> • Figure 13.1 RLV L Register Note 3 modified • 13.4.2 Burst Transfer partially added
		139 141-156	<p>Timer</p> <ul style="list-style-type: none"> • Figure 14.7 TCSPR Register Note 2 added • Table 14.4 Specification in Event Counter Mode (when not processing two-phase pulse signal) to Table 14.7 Specifications in Pulse Width Modulation Mode; Table 14.9 Specifications in Timer Mode and Table 14.10 Specifications in Event Counter Mode Condition for "Write to Timer" modified
		173 175 176 177 191 192 204 221	<p>Serial I/O</p> <ul style="list-style-type: none"> • Figure 16.1 UARTi Block Diagram modified between transmit control circuit and CTSi/RTSi pins • Figure 16.3 U0BRG to U4BRG Registers Note 3 added • Figure 16.4 U0C0 to U4C0 Registers Note 4 added • Figure 16.5 U0C1 to U4C1 Register and U0SMR to U4SMR Registers RI bit revised • Figure 16.14 Transmit Operation Timing modified • 16.2.1 Bit Rate added • Table 16.19 Special Mode 2 Specifications Transmit Start Condition modified; Specification for Error Detection partially added • Figure 16.29 SIM Interface Operation Timing modified
		225	<p>A/D Converter</p> <ul style="list-style-type: none"> • Table 17.1 A/D Converter Specifications Note 3 added
		242	<p>D/A Converter</p> <ul style="list-style-type: none"> • Figure 18.3 D/A Converter Equivalent Circuit modified
		250 274, 275 296 297 299 304	<p>Intelligent I/O</p> <ul style="list-style-type: none"> • Figure 21.2 Intelligent I/O Group 1 Block Diagram modified • Table 21.7 Pin Settings for Waveform Generation Function PSL3 register added • Table 21.16 Clock Synchronous Serial I/O Mode Specifications (Groups 0 and 1) Specification for interrupt request modified • Table 21.19 Pin Settings (2) Bit and Setting modified for the PD8 register • Table 21.22 UART Mode Specifications Specification for interrupt request modified • Table 21.28 HDLC Processing Mode Specifications Specification for interrupt request modified

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		314	<ul style="list-style-type: none"> • Table 21.36 IEBus Mode Specifications Specification for interrupt request modified
		315	<ul style="list-style-type: none"> • Table 21.37 Registers to be Used and Settings Description for the IPOL bit in the G2CR register is modified
		369	<p>Programmable I/O Ports</p> <ul style="list-style-type: none"> • Figure 24.2 Programmable I/O Ports (2) Figure modified
		384	<ul style="list-style-type: none"> • Table 24.1 Unassigned Pin Settings in Single-chip Mode Notes 2, 3, 4, and 6 added • Table 24.2 Unassigned Pin Settings in Memory Expansion Mode and Microprocessor Mode Notes 2, 3, 4, and 6 added
		385	<ul style="list-style-type: none"> • Figure 24.19 Unassigned Pin Handling Note 2 added
		387	<ul style="list-style-type: none"> • Table 24.7 Port P10 Peripheral Function Output Control Title modified
		393	<p>Flash Memory Version</p> <ul style="list-style-type: none"> • Figure 25.2 ROMCP Register Note 4 added
		453-461	<p>Electrical Characteristics</p> <ul style="list-style-type: none"> • 26.2 Electrical Characteristics (M32C/83T) Newly added
		418	<ul style="list-style-type: none"> • Table 26.3 Electrical Characteristics Minimum standard values for V_{OH} revised, values for I_{CC} when f(XIN)=32 MHz, square wave, no division revised, one condition of “f(XIN)=32 MHz, square wave, no division” deleted
		426	<ul style="list-style-type: none"> • Table 26.23 Memory Expansion Mode and Microprocessor Mode Symbols for Row Address Output Delay Time and for Row Address Output Hold Time (BCLK standard) modified
		434	<ul style="list-style-type: none"> • Figure 26.8 V_{CC}=5 V Timing Diagram (7) Timing for $\overline{\text{NMI}}$ input added
		436	<ul style="list-style-type: none"> • Table 26.24 Electrical Characteristics Minimum standard value for V_{OH} revised
		444	<ul style="list-style-type: none"> • Table 26.44 Memory Expansion Mode and Microprocessor Mode Symbols for Row Address Output Delay Time and for Row Address Output Hold Time (BCLK standard) modified
		451	<ul style="list-style-type: none"> • Figure 26.8 V_{CC}=3.3 V Timing Diagram (7) Timing for $\overline{\text{NMI}}$ input added
		453-461	<ul style="list-style-type: none"> • 26.2 Electrical Characteristics (M32C/83T) Newly added
		476	<p>Precautions</p> <ul style="list-style-type: none"> • 27.4.3 Wait Mode modified • 27.4.4 Stop Mode modified
		472	<ul style="list-style-type: none"> • 27.8.2.3 Timer A (One-shot Timer Mode) Information (g) newly added

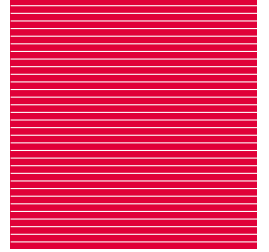
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