Freescale Semiconductor
Data Sheet: Technical Data

Document Number: MC9S08QA4
Rev. 2, 2/2008

MC9S08QA4


8-Pin DFN
Case 1452-02


8-Pin NB-SOIC
Case 751-07


8-Pin PDIP
Case 626-06

MC9S08QA4 Series

Covers: MC9S08QA4

Features:

- 8-bit HCS08 Central Processor Unit (CPU)
  - Up to 20 MHz CPU at 3.6 V to 1.8 V across temperature range of –40°C to 85°C
  - HC08 instruction set with added BGND instruction
  - Support for up to 32 interrupt/reset sources
- On-Chip Memory
  - Flash read/program/erase over full operating voltage and temperature
  - Random-access memory (RAM)
  - Security circuitry to prevent unauthorized access to RAM and flash contents
- Power-Saving Modes
  - Two very low power stop modes
  - Peripheral clock enable register can disable clocks to unused modules, thereby reducing currents
  - Very low power real time counter for use in run, wait, and stop modes with internal clock sources
- Clock Source Options
  - Internal Clock Source (ICS) — Internal clock source module containing a frequency-locked-loop (FLL) controlled by internal reference; precision trimming of internal reference allows 0.2% resolution and 2% deviation over temperature and voltage; supports bus frequencies from 1 MHz to 10 MHz
- System Protection
  - Watchdog computer operating properly (COP) reset with option to run from dedicated 1 kHz internal clock source or bus clock
  - Low-voltage detection with reset or interrupt
  - Selectable trip points
  - Illegal opcode detection with reset
  - Illegal address detection with reset
  - Flash block protection
- Development Support
  - Single-wire background debug interface
  - Breakpoint capability to allow single breakpoint setting during in-circuit debugging
- Peripherals
  - ADC — 4-channel, 10-bit resolution; 1.7 mV/°C temperature sensor; automatic compare function; internal bandgap reference channel; operation in stop3; fully functional from 3.6 V to 1.8 V
  - ACMP — Analog comparator with selectable interrupt on rising, falling, or either edge of comparator output; compare option to fixed internal bandgap reference voltage; output can be tied internally to TPM input capture
  - TPM — One 1-channel timer/pulse-width modulator (TPM) module; selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel; ACMP output can be tied internally to input capture
  - MTIM — 8-bit modulo timer module with 8-bit prescaler
  - KBI — 4-pin keyboard interrupt module with software selectable polarity on edge or edge/level modes
- Input/Output
  - Four GPIOs, one input-only pin and one output-only pin.
  - Hysteresis and configurable pullup device on all input pins; configurable slew rate and drive strength on all output pins except PTA5
- Package Options
  - 8-pin SOIC, PDIP, and DFN

This document contains information on a product under development. Freescale reserves the right to change or discontinue this product without notice.

Table of Contents

Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com/

The following revision history table summarizes changes contained in this document.

Revision	Date	Description of Changes
1	1/2008	Initial public release
2	2/2008	Changed the designator of the device in Table 15.

Related Documentation

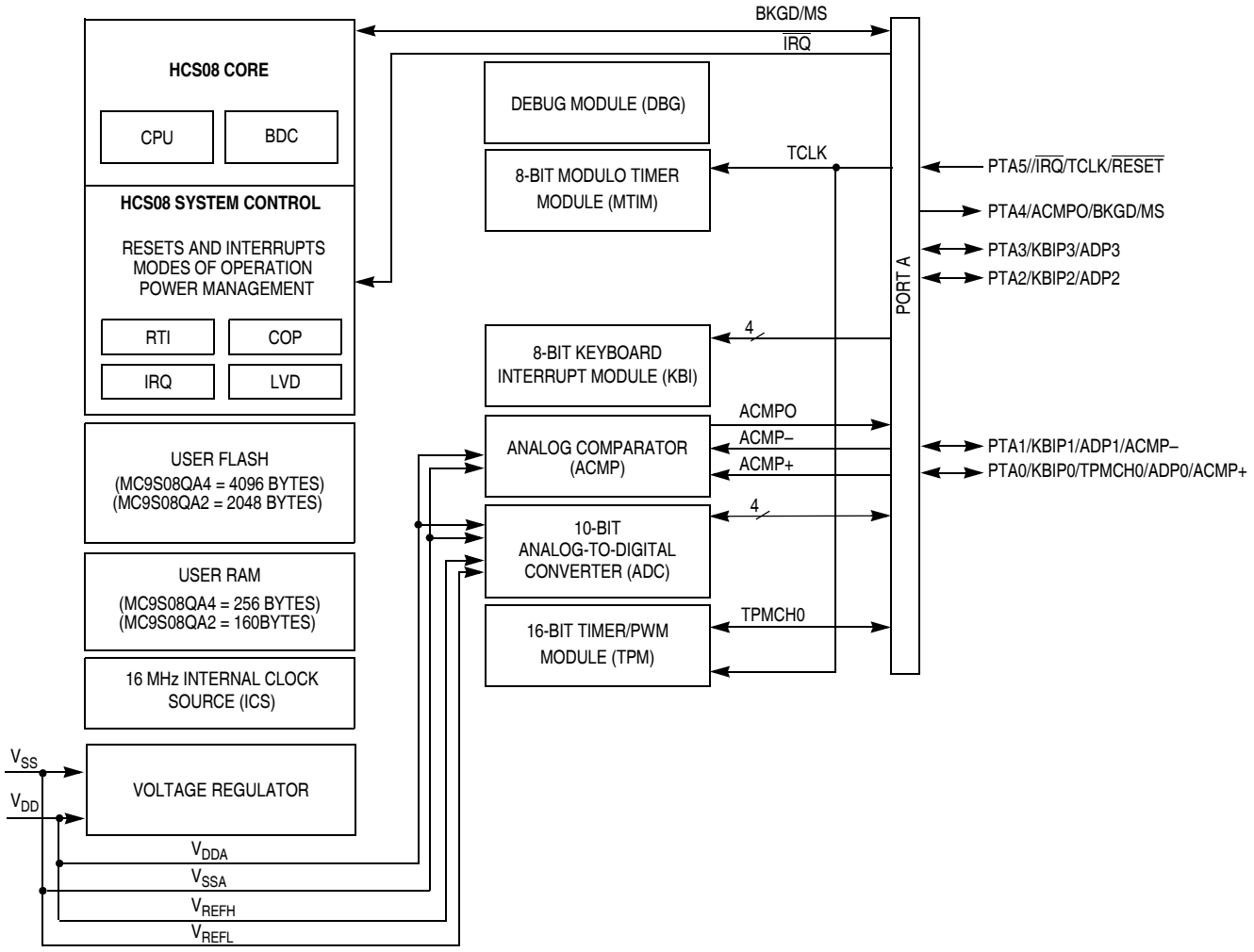
Find the most current versions of all documents at: http://www.freescale.com

Reference Manual (MC9S08QA4RM)

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

1 MCU Block Diagram

The block diagram, Figure 1, shows the structure of the MC9S08QA4 MCU.



NOTES:

1. Port pins are software configurable with pullup device if input port.
2. Port pins are software configurable for output drive strength.
3. Port pins are software configurable for output slew rate control.
4. $\overline{IRQ}$ contains a software configurable (IRQPDD) pullup device if PTA5 enabled as $\overline{IRQ}$ pin function (IRQPE = 1).
5. $\overline{RESET}$ contains integrated pullup device if PTA5 enabled as reset pin function (RSTPE = 1).
6. PTA4 contains integrated pullup device if BKGD enabled (BKGDPE = 1).
7. When pin functions as KBI (KBIPEn = 1) and associated pin is configured to enable the pullup device, KBEDGn can be used to reconfigure the pullup as a pulldown device.

Figure 1. MC9S08QA4 Series Block Diagram

2 Pin Assignments

This section shows the pin assignments in the packages available for the MC9S08QA4 series.

Table 2-1. Pin Sharing Priority

PIN	Priority (Lowest → Highest)				
8-Pin	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**	**Alt 4**
1	PTA5[1]	$\overline{\text{IRQ}}$	TCLK		$\overline{\text{RESET}}$
2	PTA4		ACMPO	BKGD	MS
3					V_{DD}
4					V_{SS}
5	PTA3	KBIP3	ADP3		
6	PTA2	KBIP2	ADP2		
7	PTA1	KBIP1		ADP1[2]	ACMP–[2]
8	PTA0	KBIP0	TPMCH0	ADP0[2]	ACMP+[2]

1 Pin does not contain a clamp diode to V_{DD} and must not be driven above V_{DD}. The voltage measured on the internally pulled-up $\overline{\text{RESET}}$ pin will not be pulled to V_{DD}. The internal gates connected to this pin are pulled to V_{DD}.

2 If ACMP and ADC are both enabled, both will have access to the pin.

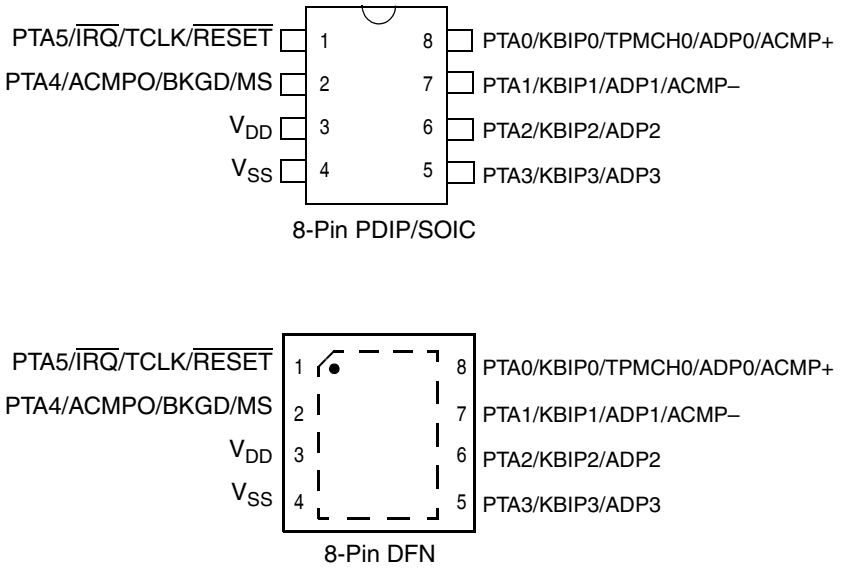


Figure 2. MC9S08QA4 Series in 8-Pin Packages

3 Electrical Characteristics

3.1 Introduction

This chapter contains electrical and timing specifications for the MC9S08QA4 series of microcontrollers available at the time of publication.

3.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 2 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pullup resistor associated with the pin is enabled.

Table 2. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to 3.8	V
Maximum current into V_{DD}	I_{DD}	120	mA
Digital input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	±25	mA
Storage temperature range	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

3.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 3. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	T_L to T_H –40 to 85	°C
Thermal resistance Single-layer board			
8-pin PDIP	θ_{JA}	113	°C/W
8-pin NB SOIC		150	
8-pin DFN		179	
Thermal resistance Four-layer board			
8-pin PDIP	θ_{JA}	72	°C/W
8-pin NB SOIC		87	
8-pin DFN		41	

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \textit{Eqn. 1}$$

where:

- T_A = Ambient temperature, °C
- θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
- $P_D = P_{int} + P_{I/O}$
- $P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
- $P_{I/O}$ = Power dissipation on input and output pins — user-determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

3.4 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 4. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulses per pin		3	
Machine	Series resistance	R1	0	Ω
	Storage capacitance	C	200	pF
	Number of pulses per pin		3	
Latch-up	Minimum input voltage limit		–2.5	V
	Maximum input voltage limit		7.5	V

Table 5. ESD and Latch-Up Protection Characteristics

No.	Rating[1]	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	±2000	—	V
2	Machine model (MM)	V_{MM}	±200	—	V
3	Charge device model (CDM)	V_{CDM}	±500	—	V
4	Latch-up current at T_A = 85°C	I_{LAT}	±100	—	mA

1 Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

3.5 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 6. DC Characteristics (Temperature Range = –40 to 85°C Ambient)

Parameter	Symbol	Min	Typical	Max	Unit
Supply voltage (run, wait, and stop modes) (V_{DD} falling)	V_{DD}	1.8	—	3.6	V
(V_{DD} rising)		V_{LVDL} (rising)	—	3.6	
Minimum RAM retention supply voltage applied to V_{DD}	V_{RAM}	V_{por}[1,2]	—	—	V
Low-voltage detection threshold (V_{DD} falling)	V_{LVD}	1.80	1.82	1.91	V
(V_{DD} rising)		1.88	1.90	1.99	
Low-voltage warning threshold (V_{DD} falling)	V_{LVW}	2.08	2.1	2.2	V

Table 6. DC Characteristics (Temperature Range = –40 to 85°C Ambient) (continued)

Parameter	Symbol	Min	Typical	Max	Unit
(V_{DD} rising)		2.16	2.19	2.27	
Power on reset (POR) re-arm voltage	V_{por}	—	1.4	—	V
Bandgap voltage reference	V_{BG}	1.18	1.20	1.21	V
Input high voltage (V_{DD} > 2.3 V) (all digital inputs)	V_{IH}	0.70 × V_{DD}	—	—	V
Input high voltage (1.8 V ≤ V_{DD} ≤ 2.3 V) (all digital inputs)		0.85 × V_{DD}	—	—	
Input low voltage (V_{DD} > 2.3 V) (all digital inputs)	V_{IL}	—	—	0.35 × V_{DD}	V
Input low voltage (1.8 V ≤ V_{DD} ≤ 2.3 V) (all digital inputs)		—	—	0.30 × V_{DD}	
Input hysteresis (all digital inputs)	V_{hys}	0.06 × V_{DD}	—	—	V
Input leakage current (per pin) V_{In} = V_{DD} or V_{SS}, all input-only pins	$\lvert I_{In}\rvert$	—	0.025	1.0	μA
High impedance (off-state) leakage current (per pin) V_{In} = V_{DD} or V_{SS}, all input/output	$\lvert I_{OZ}\rvert$	—	0.025	1.0	μA
Internal pullup resistors[3,4]	R_{PU}	17.5	—	52.5	kΩ
Internal pulldown resistor (KBI)	R_{PD}	17.5	—	52.5	kΩ
Output high voltage — low drive (PTxDSn = 0) I_{OH} = –2 mA (V_{DD} ≥ 1.8 V)	V_{OH}	V_{DD} – 0.5	—	—	V
Output high voltage — high drive (PTxDSn = 1) I_{OH} = –10 mA (V_{DD} ≥ 2.7 V) I_{OH} = –6 mA (V_{DD} ≥ 2.3 V) I_{OH} = –3 mA (V_{DD} ≥ 1.8 V)		V_{DD} – 0.5	— — —	— — —	
Maximum total I_{OH} for all port pins	$\lvert I_{OHT}\rvert$	—	—	60	mA
Output low voltage — low drive (PTxDSn = 0) I_{OL} = 2.0 mA (V_{DD} ≥ 1.8 V)	V_{OL}	—	—	0.5	V
Output low voltage — high drive (PTxDSn = 1) I_{OL} = 10.0 mA (V_{DD} ≥ 2.7 V) I_{OL} = 6 mA (V_{DD} ≥ 2.3 V) I_{OL} = 3 mA (V_{DD} ≥ 1.8 V)		— — —	— — —	0.5 0.5 0.5	
Maximum total I_{OL} for all port pins	I_{OLT}	—	—	60	mA
DC injection current [2, 5, 6, 7] V_{In} < V_{SS}, V_{In} > V_{DD} Single pin limit Total MCU limit, includes sum of all stressed pins	I_{IC}	 –0.2 –5	 — —	 0.2 5	 mA mA
Input capacitance (all non-supply pins)	C_{In}	—	—	7	pF

1 RAM will retain data down to POR voltage. RAM data not guaranteed to be valid following a POR.

2 This parameter is characterized and not tested on each device.

3 Measurement condition for pull resistors: V_{In} = V_{SS} for pullup and V_{In} = V_{DD} for pulldown.

4 PTA5/$\overline{\text{IRQ}}$/TCLK/$\overline{\text{RESET}}$ pullup resistor may not pull up to the specified minimum V_{IH}. However, all ports are functionally tested to guarantee that a logic 1 will be read on any port input when the pullup is enabled and no DC load is present on the pin.

5 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

6 Input must be current-limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

7 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

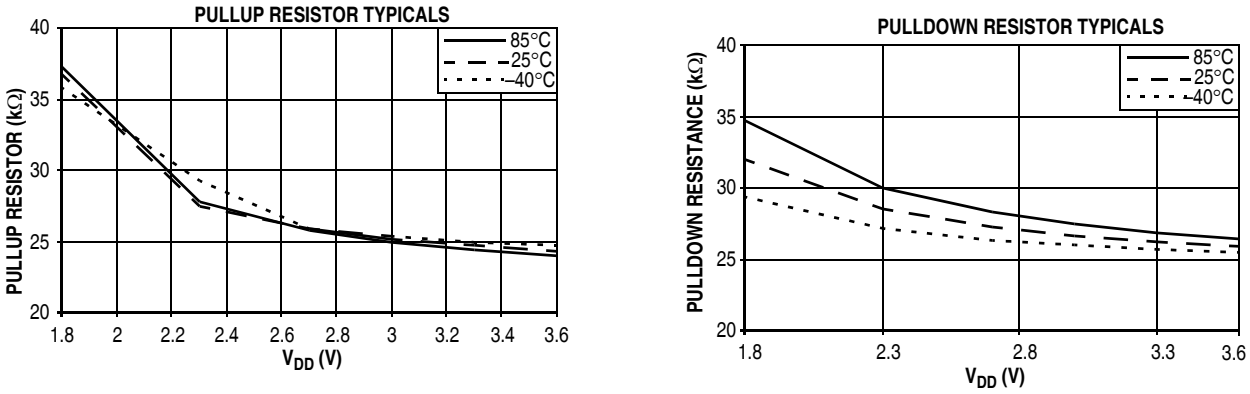


Figure 3. Pullup and Pulldown Typical Resistor Values (V_{DD} = 3.0 V)

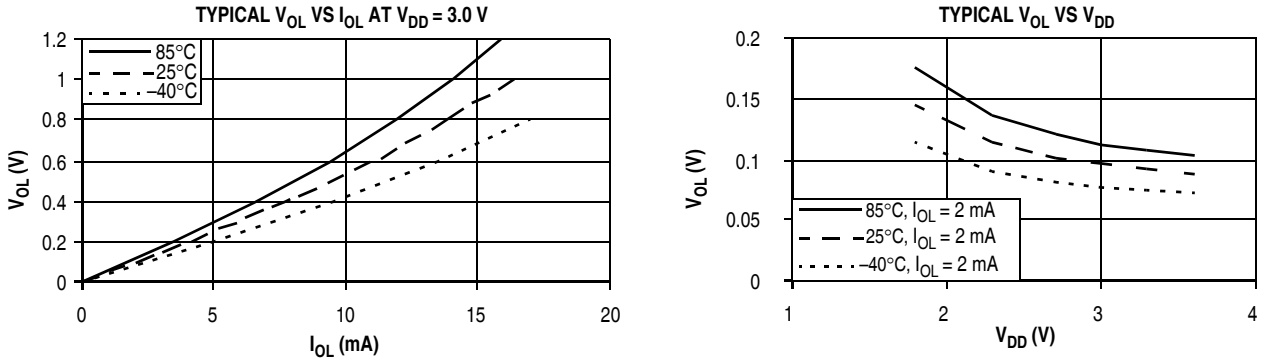


Figure 4. Typical Low-Side Driver (Sink) Characteristics — Low Drive (PTxDSn = 0)

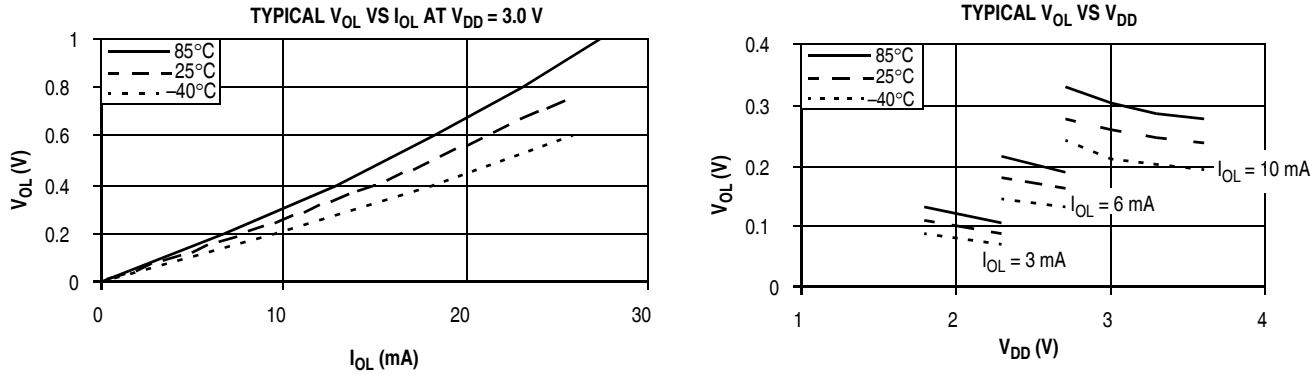


Figure 5. Typical Low-Side Driver (Sink) Characteristics — High Drive (PTxDSn = 1)

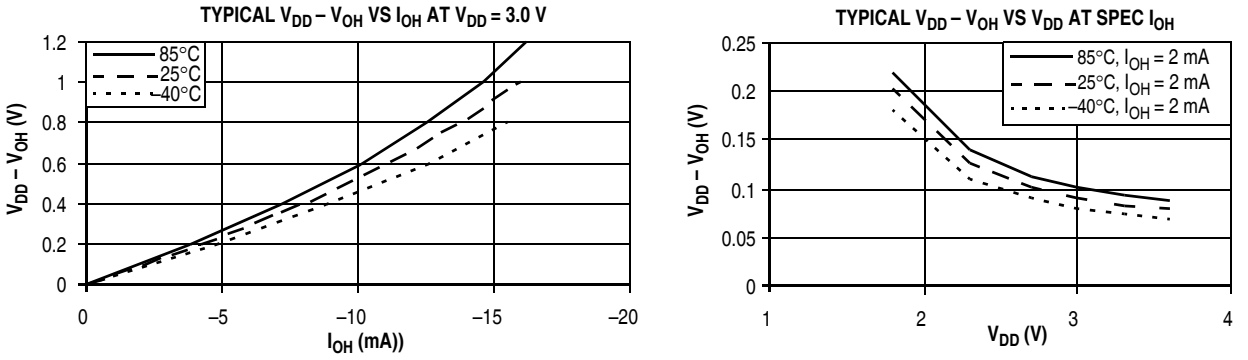


Figure 6. Typical High-Side (Source) Characteristics — Low Drive (PTxDSn = 0)

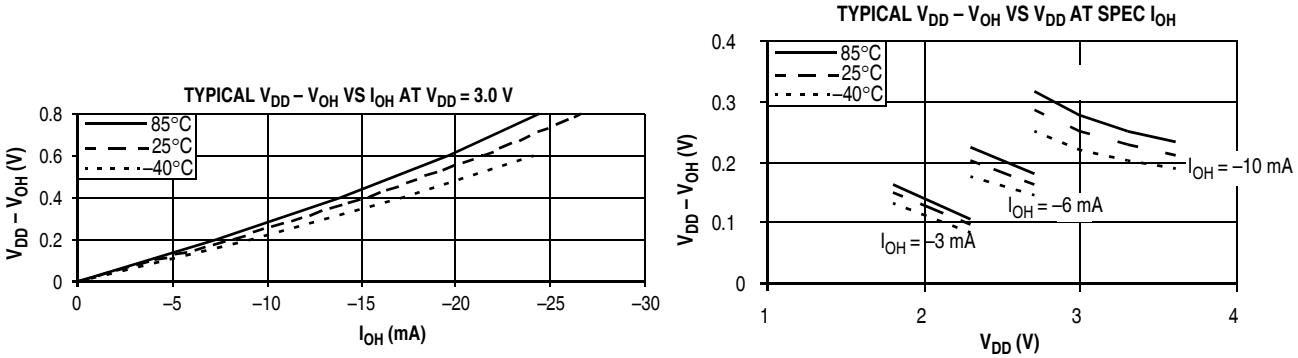


Figure 7. Typical High-Side (Source) Characteristics — High Drive (PTxDSn = 1)

3.6 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 7. Supply Current Characteristics

Parameter	Symbol	V_{DD} (V)[1]	Typical[2]	Max	T (°C)
Run supply current[3] measured in FBE mode at f_{Bus} = 8 MHz	RI_{DD}	3	3.5 mA	5 mA	85
		2	2.6 mA	—	85
Run supply current[3] measured in FBE mode at f_{Bus} = 8 MHz	RI_{DD}	3	490 μA	1 mA	85
		2	370 μA	—	85
Wait mode supply current[4] measured in FBE at 8 MHz	WI_{DD}	3	1 mA	1.5 mA	85
Stop1 mode supply current	$S1I_{DD}$	3	475 nA	1.2 μA	85
		2	470 nA	—	85
Stop2 mode supply current	$S2I_{DD}$	3	600 nA	2 μA	85
		2	550 nA	—	85
Stop3 mode supply current	$S3I_{DD}$	3	750 nA	6 μA	85
		2	680 nA	—	85
RTI adder to stop1, stop2, or stop3[4]	—	3	300 nA	—	85
		2	300 nA	—	85
LVD adder to stop3 (LVDE = LVDSE = 1)[4]	—	3	70 μA	—	85
		2	60 μA	—	85

1 3 V values are 100% tested; 2 V values are characterized but not tested.
2 Typicals are measured at 25°C.
3 Does not include any DC loads on port pins.
4 Most customers are expected to find that auto-wakeup from a stop mode can be used instead of the higher current wait mode.

3.7 Internal Clock Source (ICS) Characteristics

Table 8. ICS Specifications (Temperature Range = –40 to 85°C Ambient)

Characteristic	Symbol	Min	Typical[1]	Max	Unit
Internal reference start-up time	t_{IRST}	—	60	100	µs
Average internal reference frequency — untrimmed	f_{int_ut}	25	32.7	41.66	kHz
Average internal reference frequency — trimmed	f_{int_t}	31.25	—	39.06	kHz
DCO output frequency range — untrimmed	f_{dco_ut}	12.8	16.8	21.33	MHz
DCO output frequency range — trimmed	f_{dco_t}	16	—	20	MHz
Resolution of trimmed DCO output frequency at fixed voltage and temperature[2]	$\Delta f_{dco\_res\_t}$	—	±0.1	±0.2	$\%f_{dco}$
Total deviation of DCO output from trimmed frequency[2] At 8 MHz over full voltage and temperature range At 8 MHz and 3.6 V from 0 to 70°C	Δf_{dco_t}	—	–1.0 to +0.5 ±0.5	±2 ±1	$\%f_{dco}$
FLL acquisition time [2,3]	$t_{Acquire}$	—	—	1.5	ms
Long term jitter of DCO output clock (averaged over 2 ms interval)	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

1 Data in Typical column was characterized at 3.0 V, 25°C, or is typical recommended value.
2 This parameter is characterized and not tested on each device.
3 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed.

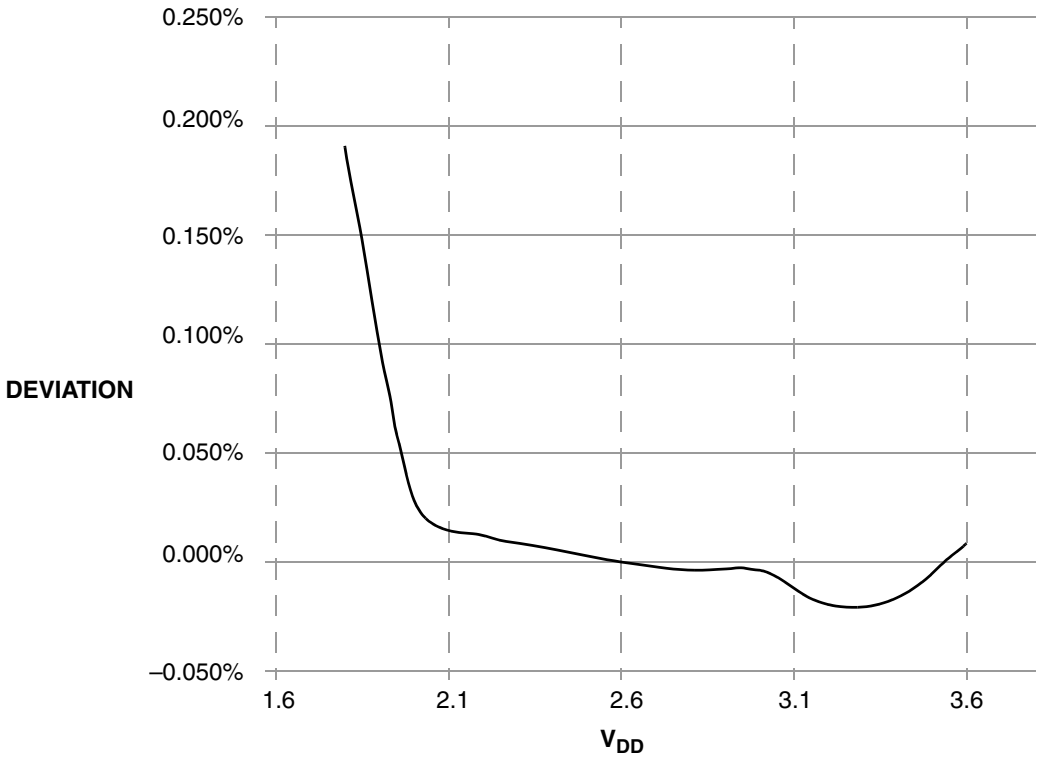


Figure 8. Deviation of DCO Output from Trimmed Frequency (8 MHz, 25°C)

3.8 AC Characteristics

This section describes timing characteristics for each peripheral system.

3.8.1 Control Timing

Table 9. Control Timing

Parameter	Symbol	Min	Typical[1]	Max	Unit
Bus frequency (t_{cyc} = 1/f_{Bus})	f_{Bus}	0	—	10	MHz
Real-time interrupt internal oscillator period (see Table 9)	t_{RTI}	700	1000	1300	µs
External reset pulse width[2]	t_{extrst}	100	—	—	ns
$\overline{IRQ}$ pulse width Asynchronous path[2] Synchronous path[3]	t_{ILIH}	 100 1.5 t_{cyc}	—	—	ns
KBIPx pulse width Asynchronous path[2] Synchronous path[3]	t_{ILIH}, t_{IHIL}	 100 1.5 t_{cyc}	—	—	ns
Port rise and fall time (load = 50 pF)[4] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 3 30	 — —	ns
BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes	t_{MSSU}	500	—	—	ns
BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes[5]	t_{MSH}	100	—	—	µs

1 Data in Typical column was characterized at 3.0 V, 25°C.

2 This is the shortest pulse that is guaranteed to be recognized.

3 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

4 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40°C to 85°C.

5 To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD}.

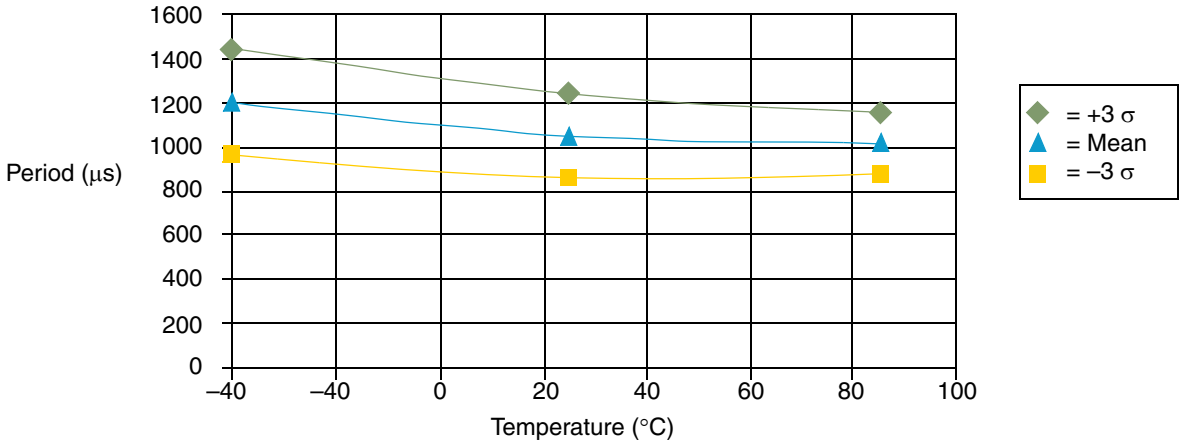


Figure 9. Typical RTI Clock Period vs. Temperature

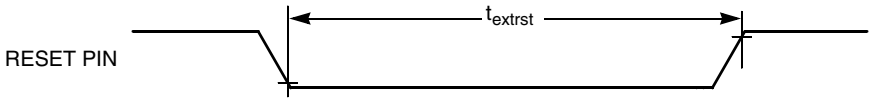


Figure 10. Reset Timing

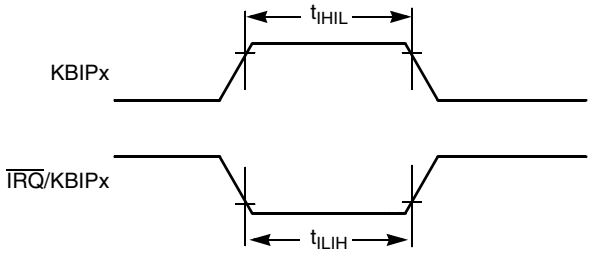


Figure 11. IRQ/KBIPx Timing

3.8.2 TPM/MTIM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 10. TPM/MTIM Input Timing

Function	Symbol	Min	Max	Unit
External clock frequency	f_{TCLK}	0	$f_{Bus}/4$	Hz
External clock period	t_{TCLK}	4	—	t_{cyc}
External clock high time	t_{clkh}	1.5	—	t_{cyc}
External clock low time	t_{clkl}	1.5	—	t_{cyc}
Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

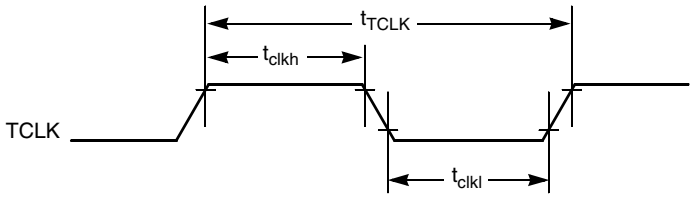


Figure 12. Timer External Clock

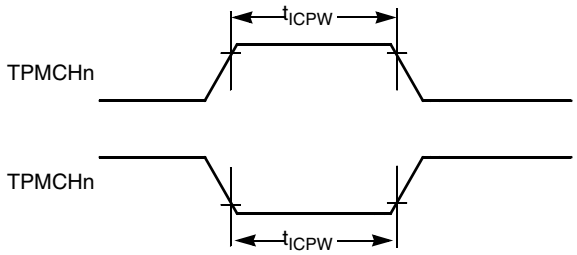


Figure 13. Timer Input Capture Pulse

3.9 Analog Comparator (ACMP) Electricals

Table 11. Analog Comparator Electrical Specifications

Characteristic	Symbol	Min	Typical	Max	Unit
Supply voltage	V_{DD}	1.80	—	3.60	V
Supply current (active)	I_{DDAC}	—	20	—	μA
Analog input voltage	V_{AIN}	V_{SS} – 0.3	—	V_{DD}	V
Analog input offset voltage	V_{AIO}	—	20	40	mV
Analog comparator hysteresis	V_H	3.0	9.0	15.0	mV
Analog input leakage current	I_{ALKG}	—	—	1.0	μA
Analog comparator initialization delay	t_{AINIT}	—	—	1.0	μs

3.10 ADC Characteristics

Table 12. 3 V 10-Bit ADC Operating Conditions

Characteristic	Conditions	Symbol	Min	Typical[1]	Max	Unit	Comment
Supply voltage	Absolute	V_{DD}	1.8	—	3.6	V	
Input voltage		V_{ADIN}	V_{SS}	—	V_{DD}	V	
Input capacitance		C_{ADIN}	—	4.5	5.5	pF	
Input resistance		R_{ADIN}	—	5	7	kΩ	
Analog source resistance	10 bit mode f_{ADCK} > 4 MHz f_{ADCK} < 4 MHz	R_{AS}	 — —	 — —	 5 10	kΩ	External to MCU
	8 bit mode (all valid f_{ADCK})		—	—	10		
ADC conversion clock frequency	High Speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz	
	Low Power (ADLPC=1)		0.4	—	4.0		

[1] Typical values assume V_{DD} = 3.0 V, Temp = 25°C, f_{ADCK} =1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

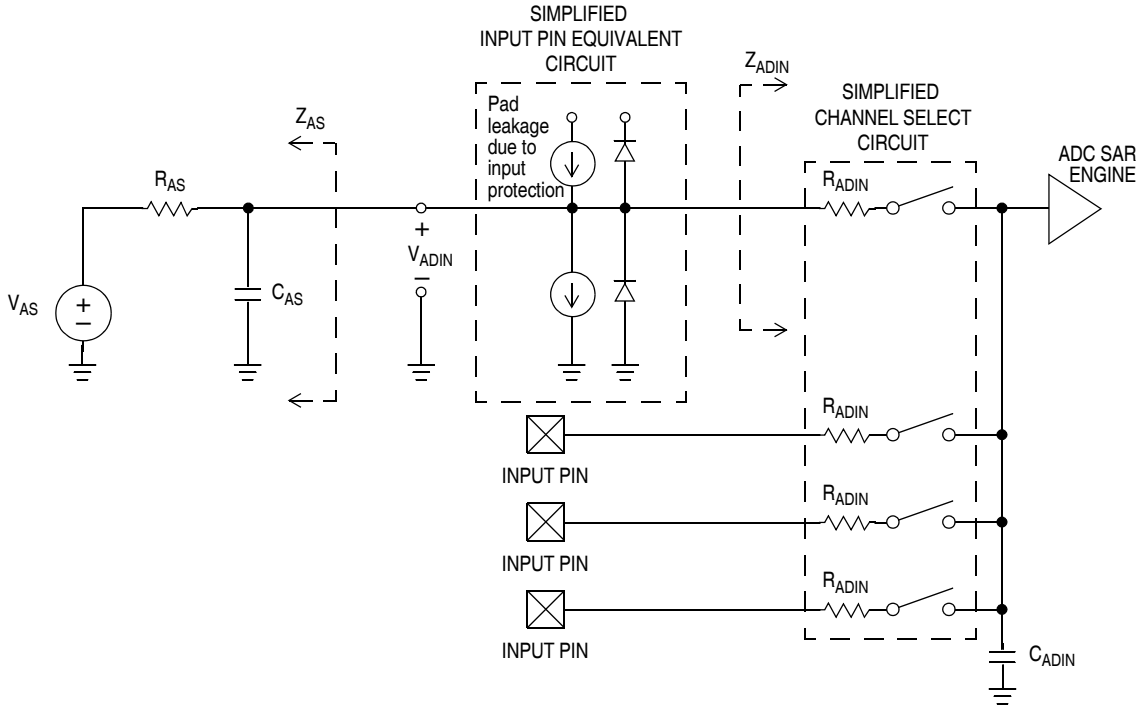


Figure 14. ADC Input Impedance Equivalency Diagram

Table 13. 3 V 10-Bit ADC Characteristics

Characteristic	Conditions	Symbol	Min	Typical[1]	Max	Unit	Comment
Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1		I_{DDAD}	—	120	—	μA	
Supply current ADLPC = 1 ADLSMP = 0 ADCO = 1		I_{DDAD}	—	202	—	μA	
Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1		I_{DDAD}	—	288	—	μA	
Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1		I_{DDAD}	—	532	646	μA	
ADC asynchronous clock source	High speed (ADLPC=0)	f_{ADACK}	2	3.3	5	MHz	$t_{ADACK} = 1/f_{ADACK}$
	Low power (ADLPC=1)		1.25	2	3.3		

Table 13. 3 V 10-Bit ADC Characteristics (continued)

Characteristic	Conditions	Symbol	Min	Typical[1]	Max	Unit	Comment
Conversion time (including sample time)	Short sample (ADLSMP=0)	t_{ADC}	—	20	—	ADCK cycles	See *MC9S08QA4 Series Reference Manual* for conversion time variances
	Long sample (ADLSMP=1)		—	40	—		
Sample time	Short sample (ADLSMP=0)	t_{ADS}	—	3.5	—	ADCK cycles	
	Long sample (ADLSMP=1)		—	23.5	—		
Total unadjusted error	10-bit mode	E_{TUE}	—	±1.5	±3.5	LSB[2]	Includes quantization
	8-bit mode		—	±0.7	±1.5		
Differential non-linearity	10-bit mode	DNL	—	±0.5	±1.0	LSB[2]	Monotonicity and no missing codes guaranteed
	8-bit mode		—	±0.3	±0.5		
Integral non-linearity	10-bit mode	INL	—	±0.5	±1.0	LSB[2]	
	8-bit mode		—	±0.3	±0.5		
Zero-scale error	10-bit mode	E_{ZS}	—	±1.5	±2.1	LSB[2]	$V_{ADIN} = V_{SS}$
	8-bit mode		—	±0.5	±0.7		
Full-scale error	10-bit mode	E_{FS}	0	±1.0	±1.5	LSB[2]	$V_{ADIN} = V_{DD}$
	8-bit mode		0	±0.5	±0.5		
Quantization error	10-bit mode	E_Q	—	—	±0.5	LSB[2]	
	8-bit mode		—	—	±0.5		
Input leakage error	10-bit mode	E_{IL}	0	±0.2	±4	LSB[2]	Pad leakage[3] * R_{AS}
	8-bit mode		0	±0.1	±1.2		
Temp sensor slope	–40°C – 25°C	m	—	1.646	—	mV/°C	
	25°C – 85°C		—	1.769	—		
Temp sensor voltage	25°C	V_{TEMP25}	—	701.2	—	mV	

1 Typical values assume V_{DD} = 3.0 V, Temp = 25°C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

3 Based on input pad leakage current. Refer to pad electricals.

3.11 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see *MC9S08QA4 Series Reference Manual*.

Table 14. Flash Characteristics

Characteristic	Symbol	Min	Typical	Max	Unit
Supply voltage for program/erase –40°C to 85°C	$V_{prog/erase}$	1.8	—	3.6	V
Supply voltage for read operation	V_{Read}	1.8	—	3.6	V
Internal FCLK frequency[1]	f_{FCLK}	150	—	200	kHz
Internal FCLK period (1/FCLK)	t_{Fcyc}	5	—	6.67	μs
Byte program time (random location)[2]	t_{prog}	9			t_{Fcyc}
Byte program time (burst mode)[2]	t_{Burst}	4			t_{Fcyc}
Page erase time[2]	t_{Page}	4000			t_{Fcyc}
Mass erase time[2]	t_{Mass}	20,000			t_{Fcyc}
Program/erase endurance[3] T_L to T_H = –40°C to + 85°C T = 25°C		10,000	— 100,000	— —	cycles
Data retention[4]	t_{D_ret}	15	100	—	years

1 The frequency of this clock is controlled by a software setting.

2 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

3 **Typical endurance for flash** was evaluated for this product family on the 9S12Dx64. For additional information on how Motorola defines typical endurance, please refer to Engineering Bulletin EB619/D, *Typical Endurance for Nonvolatile Memory.*

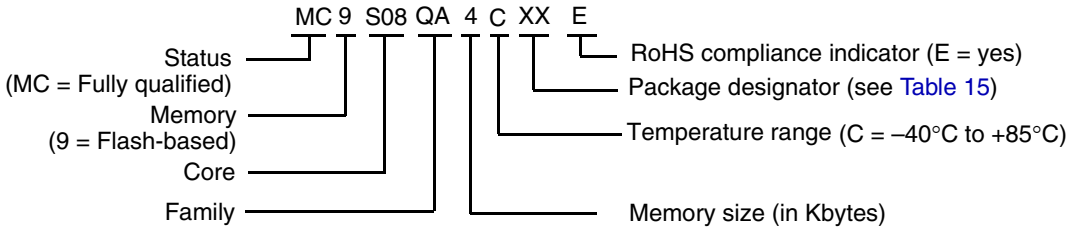
4 **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618/D, *Typical Data Retention for Nonvolatile Memory.*

4 Ordering Information

This section contains ordering numbers for MC9S08QA4 series devices. See below for an example of the device numbering system.

Table 15. Device Numbering System

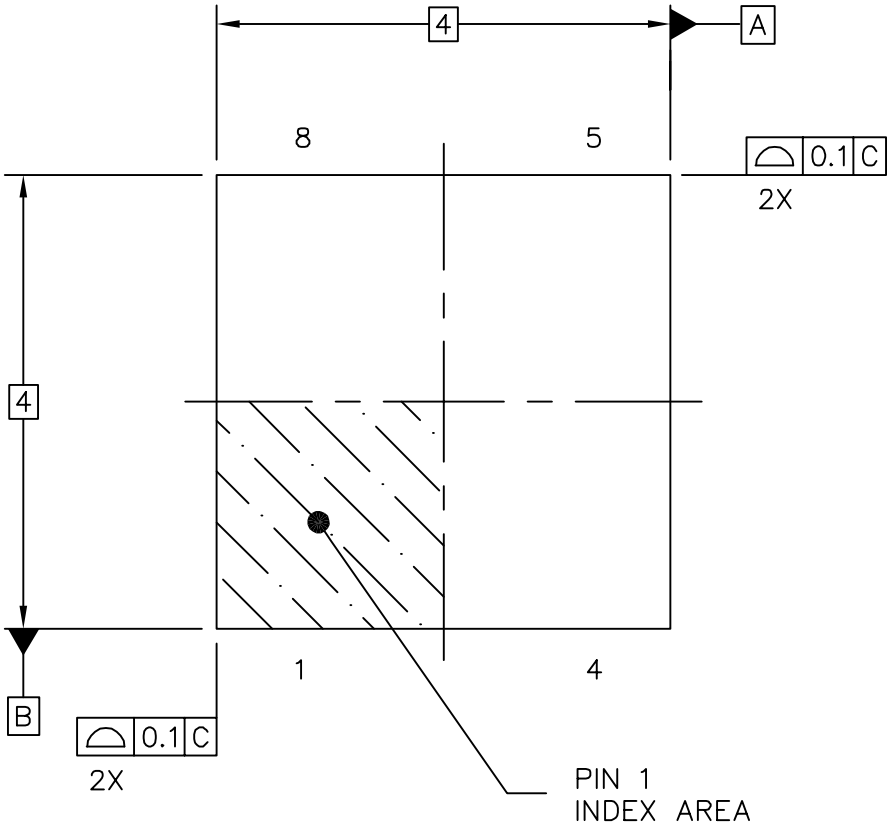
Device Number	Memory		Package		
	Flash	RAM	Type	Designator	Document No.
MC9S08QA4	4 Kbytes	256 bytes	8 DFN 8 PDIP 8 NB SOIC	FQ PA DN	98ARL10557D 98ASB42420B 98ASB42564B
MC9S08QA2	2 Kbytes	160 bytes			

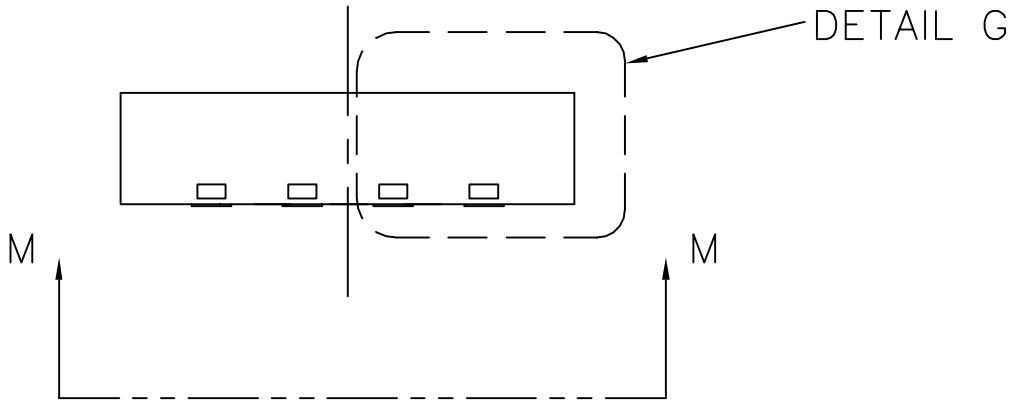


5 Mechanical Drawings

The following pages contain mechanical specifications for MC9S08QA4 series package options.

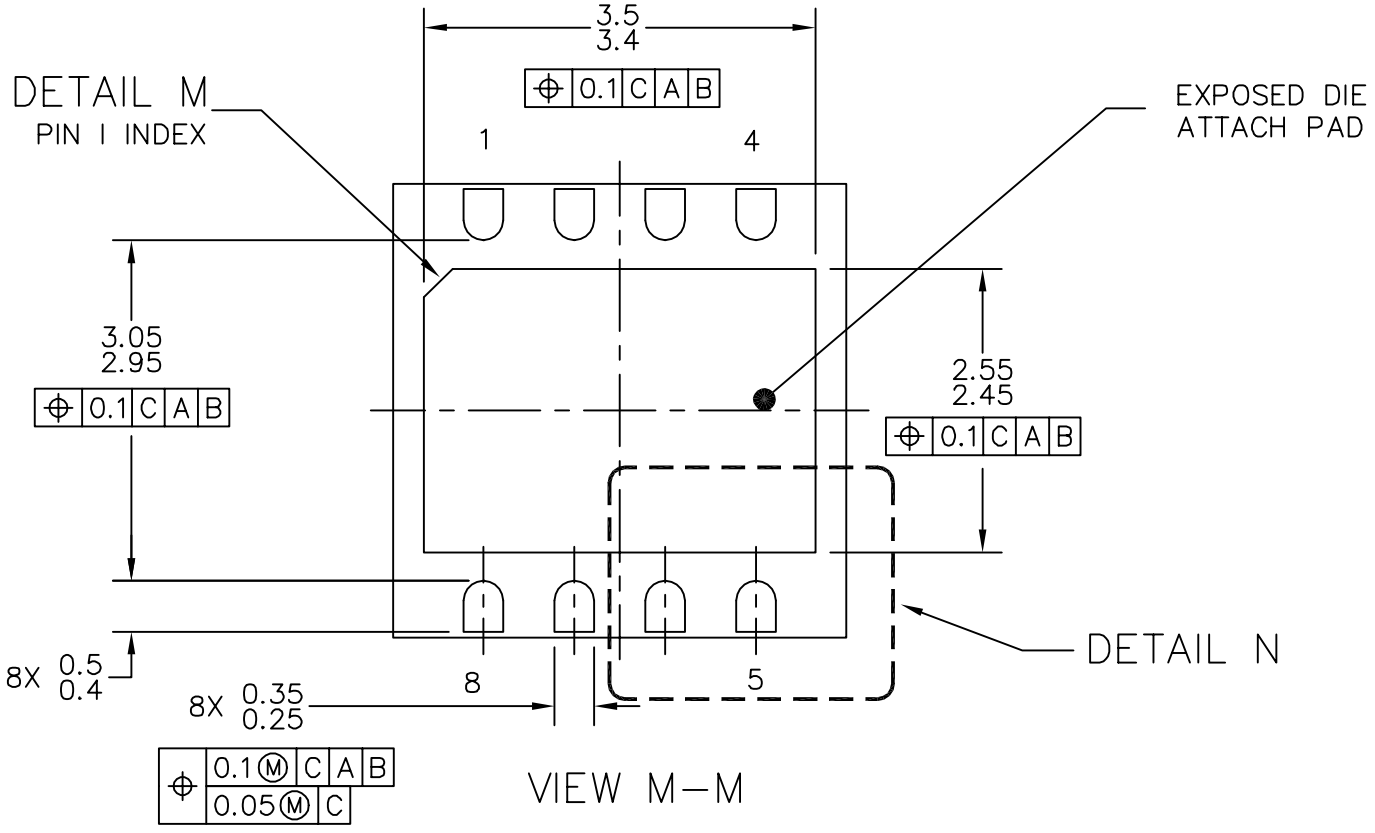
- 8-pin DFN (plastic dual in-line pin)
- 8-pin NB SOIC (narrow body small outline integrated circuit)
- 8-pin PDIP (plastic dual in-line pin)

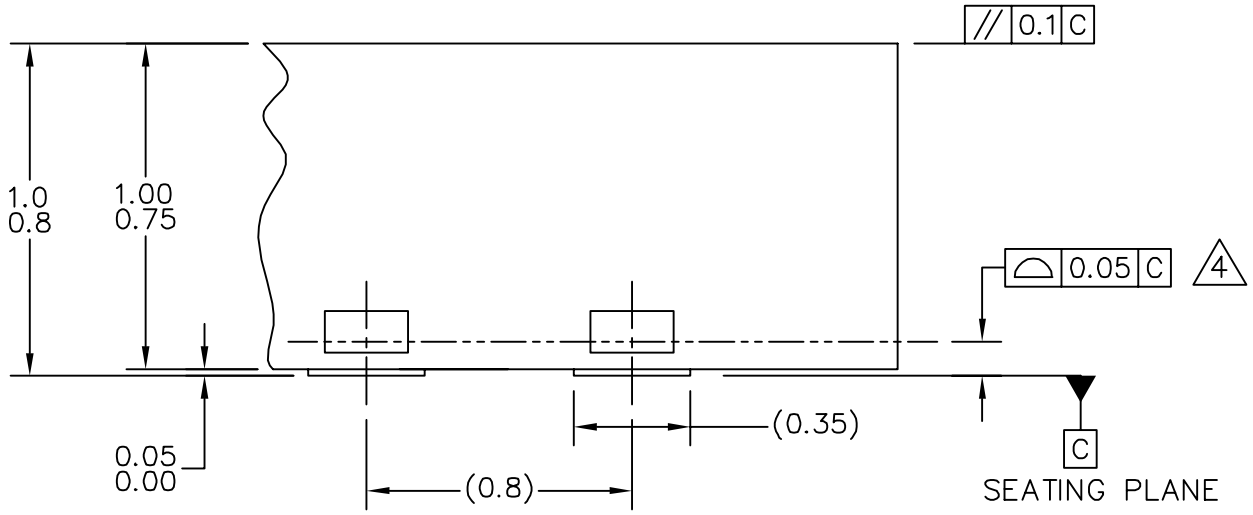




MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE: THERMALLY ENHANCED DUAL FLAT NO LEAD PACKAGE (DFN) 8 TERMINAL, 0.8 PITCH (4 X 4 X 1)	DOCUMENT NO: 98ARL10557D	REV: B
	CASE NUMBER: 1452-02	28 DEC 2005
	STANDARD: NON-JEDEC	





DETAIL G

MECHANICAL OUTLINE

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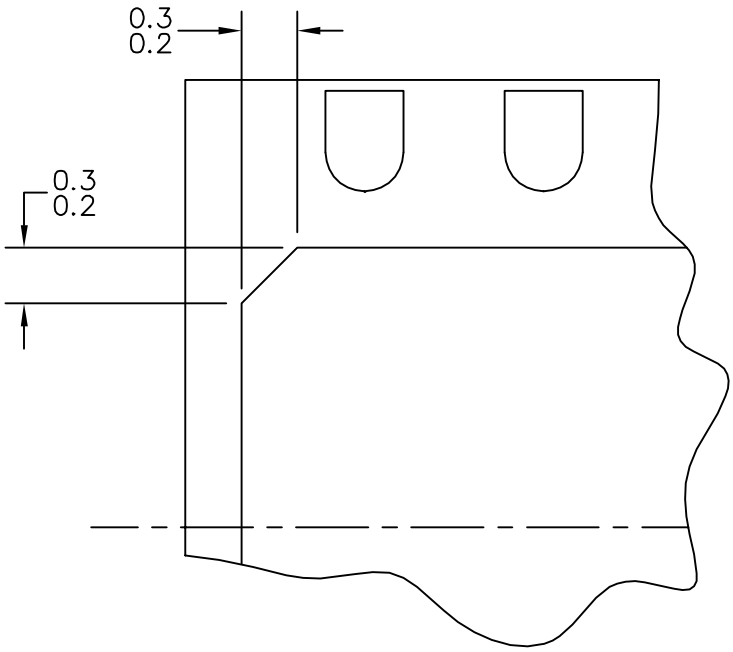
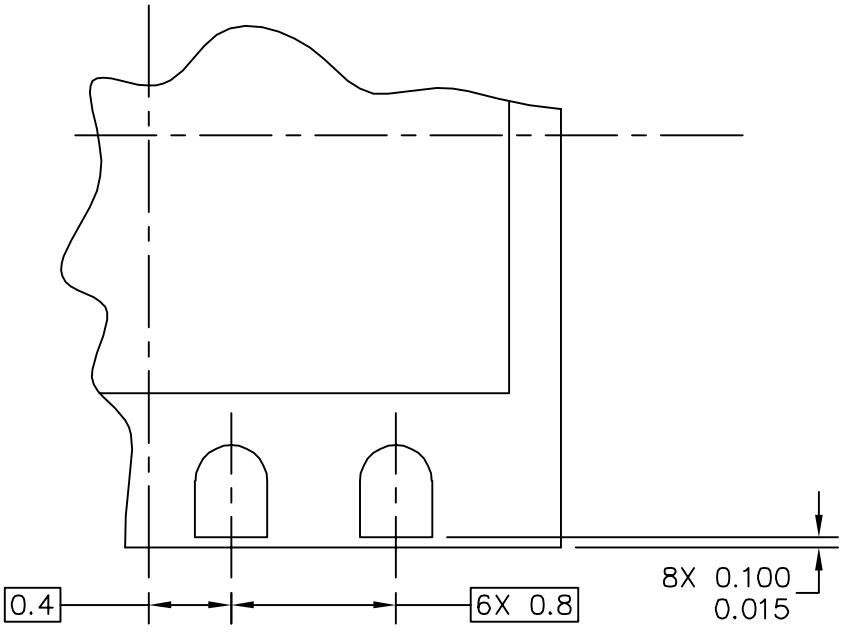
	CASE NUMBER: 1452–02	28 DEC 2005
	STANDARD: NON–JEDEC	



DETAIL M
BACKSIDE PIN 1 INDEX



DETAIL N

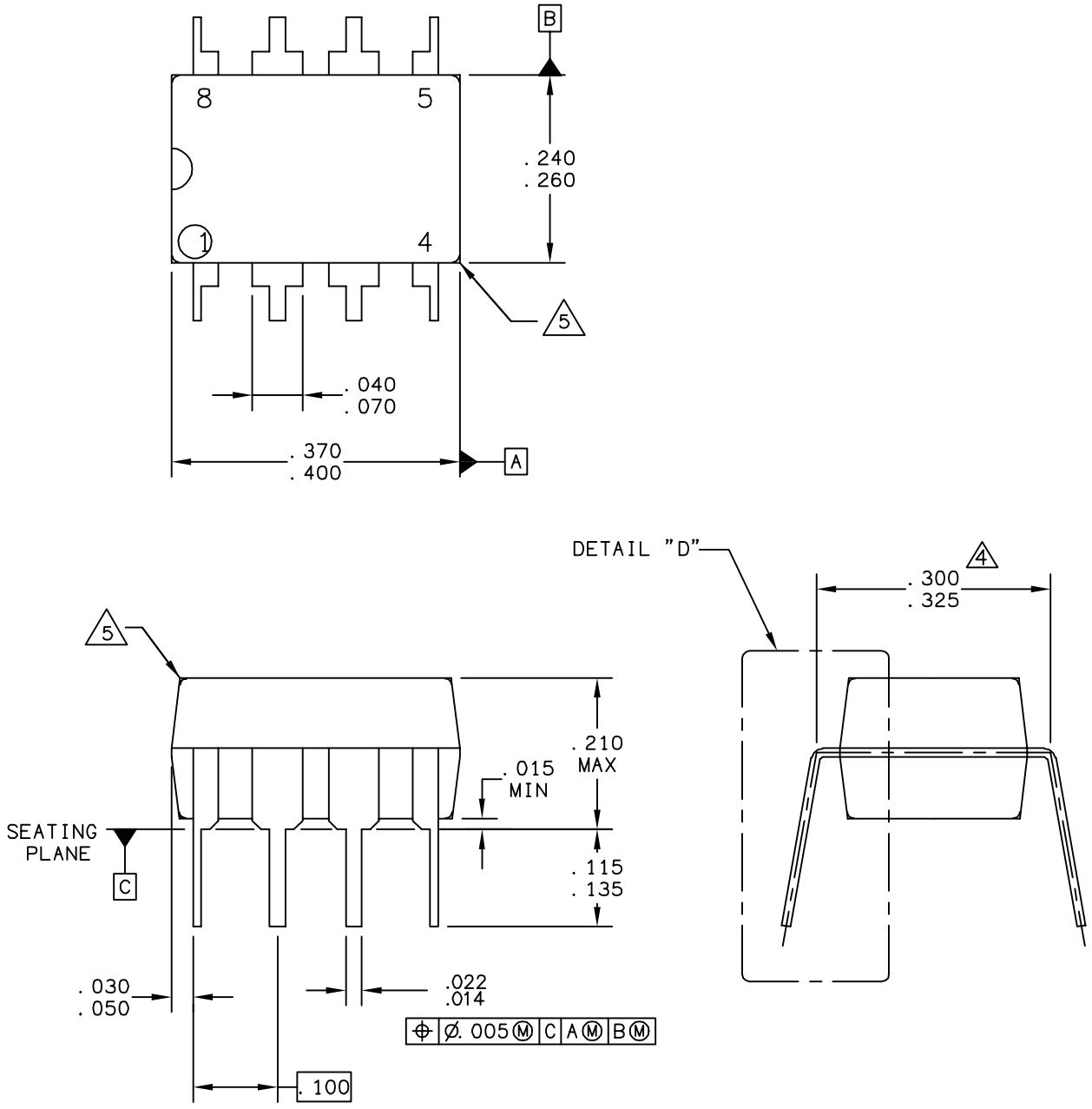
MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE: THERMALLY ENHANCED DUAL FLAT NO LEAD PACKAGE (DFN) 8 TERMINAL, 0.8 PITCH (4 X 4 X 1)	DOCUMENT NO: 98ARL10557D	REV: B
	CASE NUMBER: 1452-02	28 DEC 2005
	STANDARD: NON-JEDEC	

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HP-VFDFP-N.
4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH PAD.
5. MIN. METAL GAP SHOULD BE 0.2MM.

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: THERMALLY ENHANCED DUAL FLAT NO LEAD PACKAGE (DFN) 8 TERMINAL, 0.8 PITCH (4 X 4 X 1)	DOCUMENT NO: 98ARL10557D	REV: B
	CASE NUMBER: 1452-02	28 DEC 2005
	STANDARD: NON-JEDEC	



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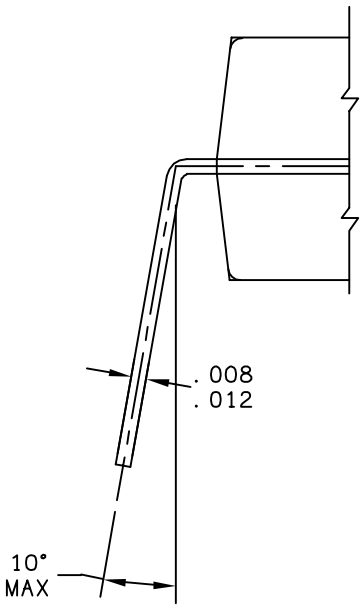
TITLE: 8 LD PDIP	DOCUMENT NO: 98ASB42420B	REV: N
	CASE NUMBER: 626-06	19 MAY 2005
	STANDARD: NON-JEDEC	



DETAIL "D"

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 8 LD PDIP	DOCUMENT NO: 98ASB42420B	REV: N
	CASE NUMBER: 626-06	19 MAY 2005
	STANDARD: NON-JEDEC	

NOTES:

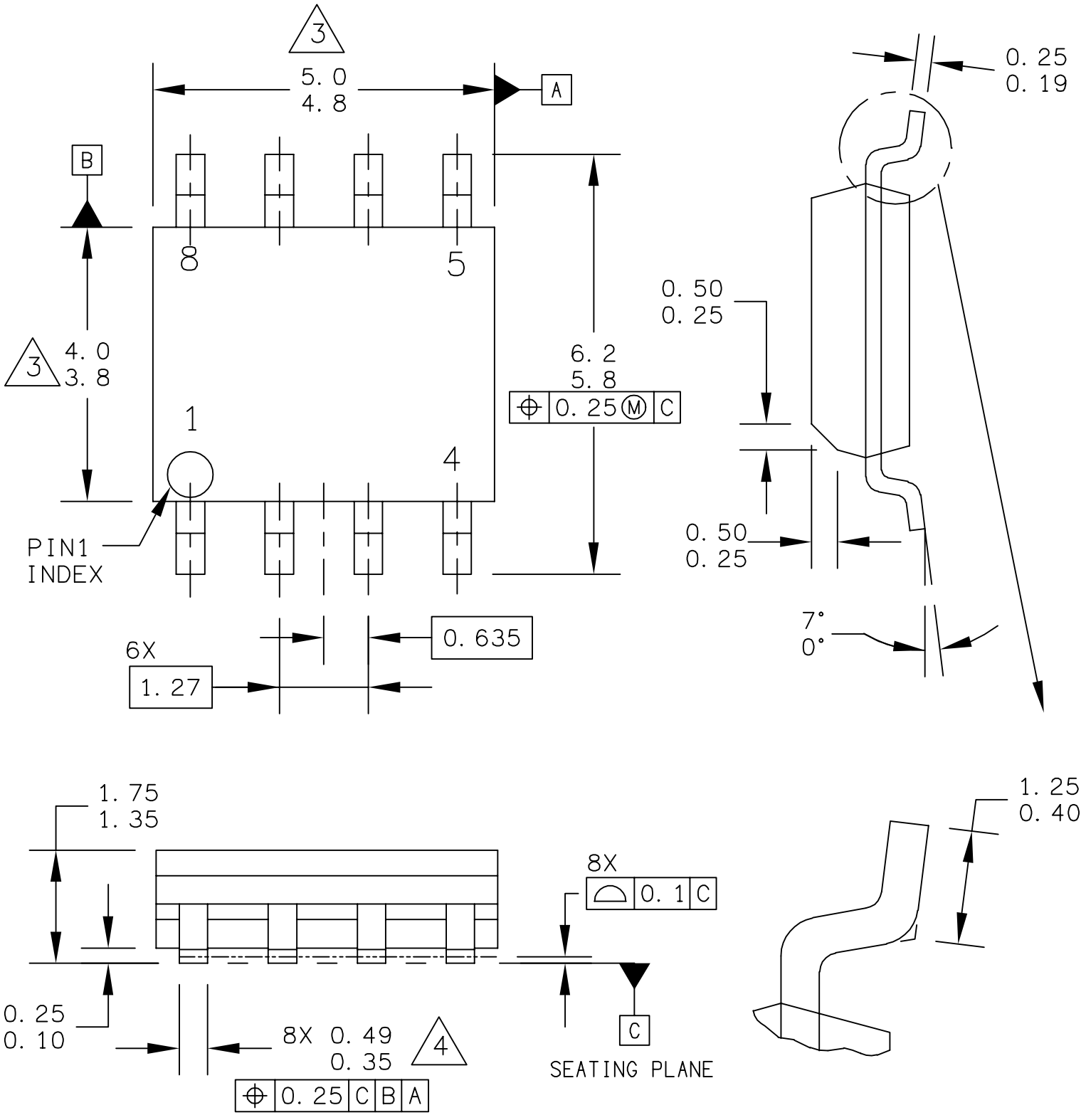
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M – 1994.
2. ALL DIMENSIONS ARE IN INCHES.
3. 626-03 TO 626-06 OBSOLETE. NEW STANDARD 626-07.
4. DIMENSION TO CENTER OF LEAD WHEN FORMED PARALLEL.
5. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CONERS).

STYLE 1:

PIN	1.	AC IN	5.	GROUND
	2.	DC + IN	6.	OUTPUT
	3.	DC – IN	7.	AUXILIARY
	4.	AC IN	8.	VCC

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASB42420B	REV: N
8 LD PDIP	CASE NUMBER: 626-06	19 MAY 2005
	STANDARD: NON-JEDEC	



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TITLE: 8LD SOIC NARROW BODY	DOCUMENT NO: 98ASB42564B	REV: U
	CASE NUMBER: 751-07	07 APR 2005
	STANDARD: JEDEC MS-012AA	

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N-SOURCE
2. N-GATE
3. P-SOURCE
4. P-GATE
5. P-DRAIN
6. P-DRAIN
7. N-DRAIN
8. N-DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

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	STANDARD: JEDEC MS-012AA	

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

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NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.

3. DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

4. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

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