FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-13607-5E

*16-bit Proprietary Microcontrollers*

**CMOS**

# F²MC-16L MB90650A Series

# MB90652A/653A/654A/F654A/V650A

## ■ DESCRIPTION

The MB90650A series are 16-bit microcontrollers designed for high speed real-time processing in consumer product applications such as controlling cellular phones, CD-ROMs, or VTRs. Based on the F²MC*1-16L CPU core, an F²MC-16L is used as the CPU. This CPU includes high-level language-support instructions and robust task switching instructions, and additional addressing modes. In order to reduce the consumption current, dual-clock (main/sub) is used. Furthermore, low consumption power supply is achieved by using stop mode, sleep mode, watch mode, pseudo-watch mode, CPU intermittent operation mode.

Microcontrollers in this series have built-in peripheral resources including 10-bit A/D converter, 8-bit D/A converter, UART, 8/16-bit PPG, 8/16-bit up/down counter/timer, I²C interface*2, 8/16-bit I/O timer (input capture, output compare, and 16-bit free-run timer).

*1:F²MC stands for FUJITSU Flexible Microcontroller.

*2:Purchase of Fujitsu I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

## ■ FEATURES

**F²MC-16L CPU**

- Minimum execution time: 83.3 ns/3 MHz oscillation (Uses PLL clock multiplication) maximum multiplier = 4
- Instruction set optimized for controller applications
  Object code compatibility with F²MC-16(H)

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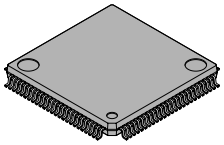
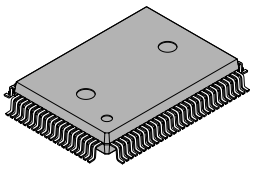
## ■ PACKAGES

| 100-pin plastic LQFP | 100-pin plastic QFP |
|---|---|
|  |  |
| (FPT-100P-M05) | (FPT-100P-M06) |

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Wide range of data Types (bit, byte, word, and long word)
Improved instruction cycles provide increased speed
Additional addressing modes: 23 modes
High code efficiency
Access methods (bank access, linear pointer)
High precision operations are enhanced by use of a 32-bit accumulator
Extended intelligent I/O service (access area extended to 64 Kbytes)
Maximum memory space: 16 Mbytes

- Enhanced high level language (C) and multitasking support instructions
  Use of a system stack pointer
  Enhanced pointer indirect instructions
  Barrel shift instructions
- Improved execution speed: Four byte instruction queue
- Powerful interrupt function
- Automatic data transfer function that does not use instruction (extended $I^2OS$)

## ■ PRODUCT LINEUP

| Item \ Part number | MB90652A | MB90653A | MB90654A | MB90F654A | MB90V650A* |
|---|---|---|---|---|---|
| Classification | Mask ROM product | | Mask ROM product | FLASH product | For evaluation |
| ROM size | 64 Kbytes | 128 Kbytes | 256 Kbytes | | — |
| RAM size | 3 Kbytes | 5 Kbytes | 8 Kbytes | | 6 Kbytes |
| Power supply voltage | 2.2 V to 3.6 V | | 2.2 V to 3.6 V | 2.4 V to 3.6 V | 2.7 V to 5.5 V |
| CPU functions | The number of instructions : 340<br>Instruction bit length : 8/16 bits<br>Instruction length : 1 to 7 bytes<br>Data bit length : 1/4/8/16/32 bits<br>Minimum execution time : 83.3 ns/3 MHz (PLL multiplier = 4)<br>Interrupt processing time : 2 µs/12 MHz (minimum) | | | | |
| Ports | I/O ports (N-channel open-drain) : 4<br>I/O ports (CMOS) : 75 (Input pull-up resistors available: 24/ Can be set as N-channel open-drain: 8)<br>Total : 79 | | | | |
| A/D converter | Analog inputs: 8 channels<br>10-bit resolution<br>Conversion time: minimum 8.17 µs/12 MHz | | | | Analog inputs: 8 channels<br>10-bit resolution<br>Conversion time: minimum 8.17 µs/12 MHz |
| D/A converter | 2 channels (independent),<br>8-bit resolution, R-2R type | | | | |
| 8/16-bit up/down counter/timer | 16 bits × 1 channel/8 bits × 2 channels selectable<br>Includes reload and compare functions. | | | | |
| $I^2C$ interface | 1 channel<br>Master mode/slave mode available | | | | |
| UART | 1 channel<br>Clock synchronous communication<br>Clock asynchronous communication | | | | |
| I/O extended serial interface | 8 bits × 2 channels<br>LSB-first or MSB-first operation selectable | | | | |
| 8/16-bit PPG | 8 bits × 2 channels/16 bits × 1 channel selectable | | | | |
| 16-bit I/O timer | 1 channel<br>(Input capture × 2 channels, output compare × 4 channels, and free-run timer × 1 channel) | | | | |
| DTP/external interrupt | 8 inputs | | | | |
| Timer functions | Timebase timer (18-bit)/watchdog timer (18-bit)/watch timer (15-bit) | | | | |
| DTMF generator | Supports every ITU-T (CCITT) tone for output (Internal 12 MHz shall be used for DTMF generator). | | | | |
| Low-power consumption modes | CPU intermittent operation mode, sub clock mode, stop mode, sleep mode, watch mode, pseudo-watch mode | | | | |

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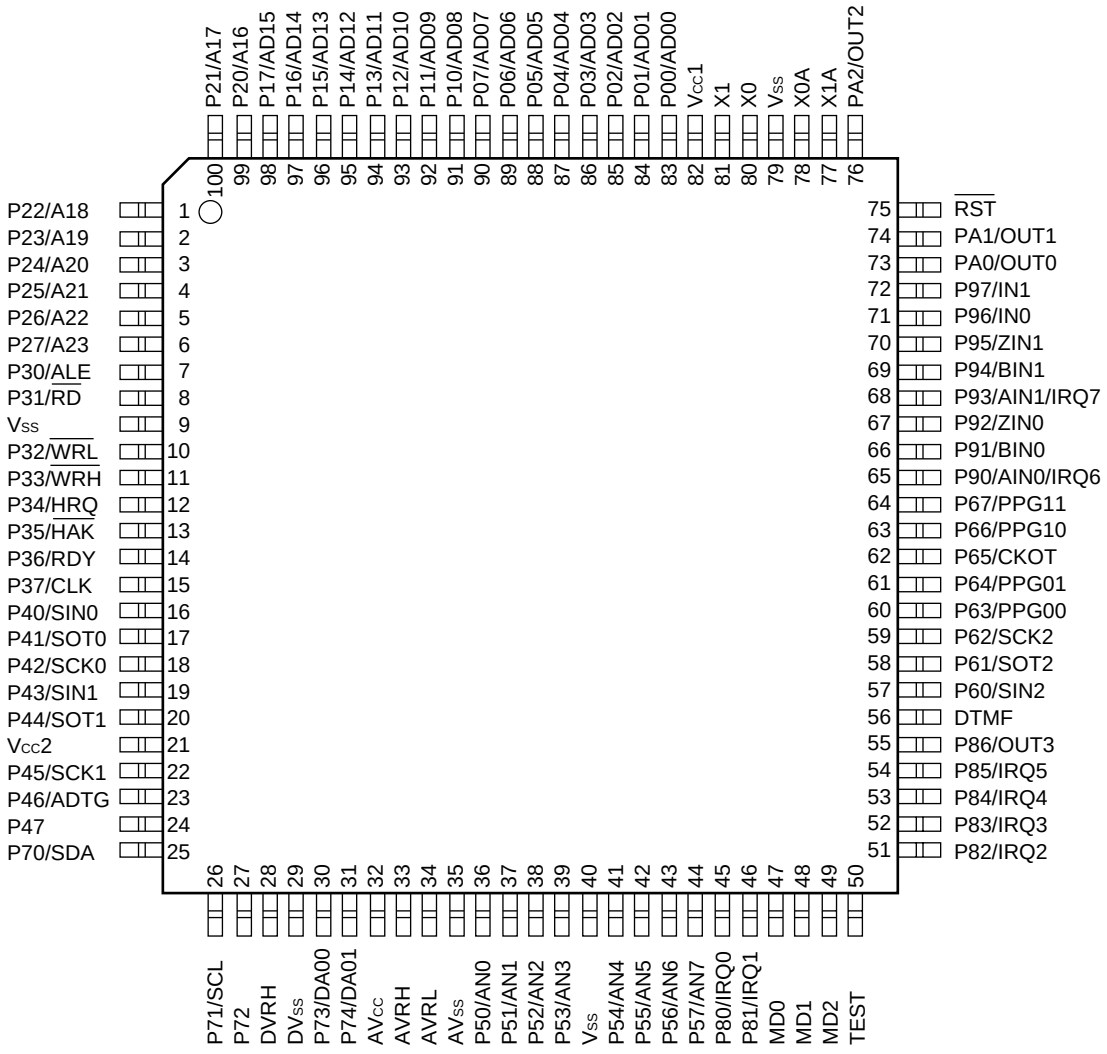
| Item \ Part number | MB90652A | MB90653A | MB90654A | MB90F654A | MB90V650A* |
|---|---|---|---|---|---|
| PLL function | Selectable multiplier: 1/2/3/4<br>(Set a multiplier that does not exceed the assured operation frequency range.) | | | | |
| Other | — | | | | |
| Package | FPT-100P-M05,<br>FPT-100P-M06 | | | | PGA-256C-A02 |

* : MB90V650A has products of single clock power supply and dual clock power supply.
Model : Single clock system MB90V650ACR-ES
Dual clock system MB90V650ACR-ES-H

Note : MB90V650A device is assured only when operate with the tools, under the condition of power supply voltage : 2.7 V to 3.3 V, operating temperature: 0°C to 70°C and operating frequency: 1.5 MHz to 12 MHz
For more information about each package, see section “PACKAGE DIMENSIONS”.

## ■ PIN ASSIGNMENTS

(Top view)




(FPT-100P-M05)

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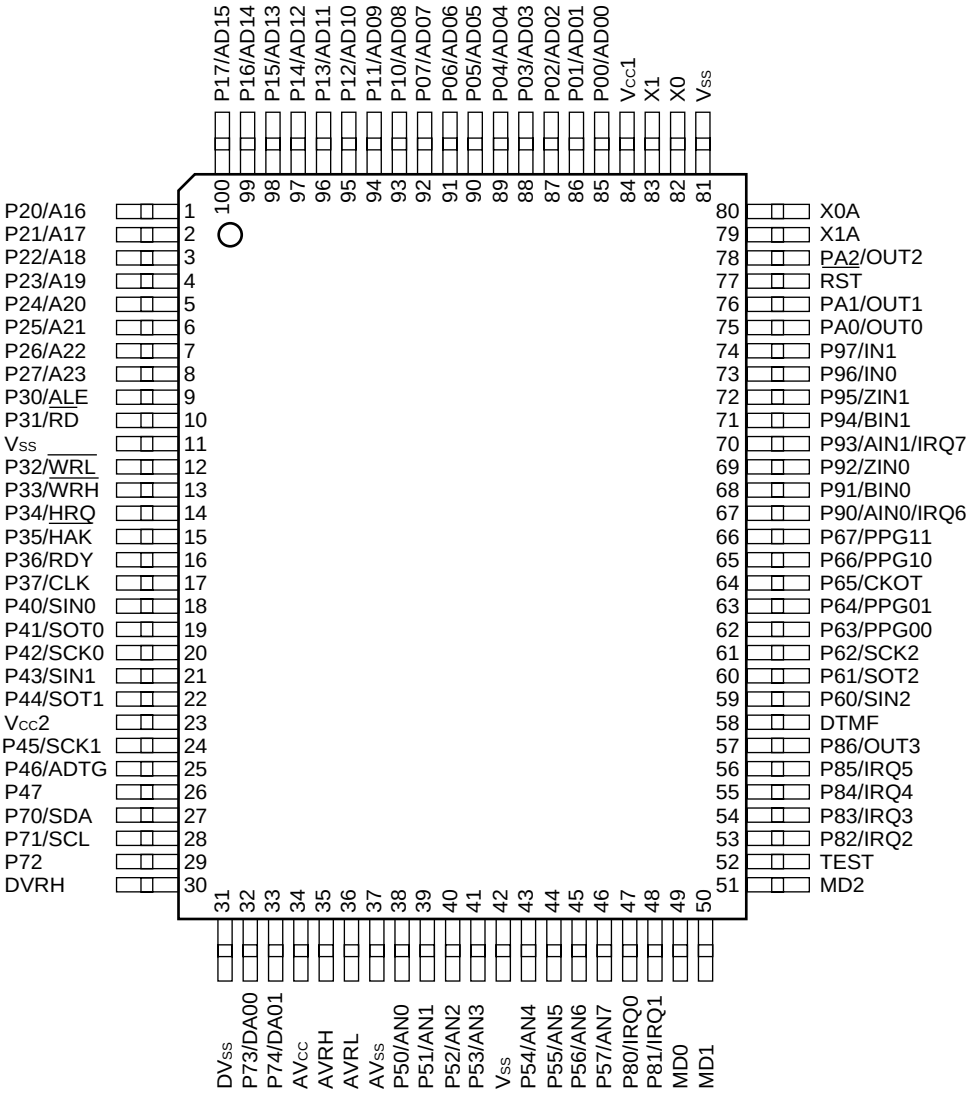
(Top view)




(FPT-100P-M06)

## ■ PIN DESCRIPTION

| Pin no. | | Pin name | Circuit type | Function |
|---|---|---|---|---|
| LQFP*1 | QFP*2 | | | |
| 80 | 82 | X0 | A | Crystal oscillator pin |
| 81 | 83 | X1 | A | Crystal oscillator pin |
| 77 | 79 | X1A | B | Crystal oscillator pins (32 kHz) |
| 78 | 80 | X0A | B | Crystal oscillator pins (32 kHz) |
| 47 to 49 | 49 to 51 | MD0 to MD2 | D | Operating mode selection pins<br>Connect directly to $V_{CC}$ or $V_{SS}$. |
| 50 | 52 | TEST | D | Test input pin<br>This pin must always be fixed to “H”. |
| 75 | 77 | $\overline{RST}$ | C | Reset input pin |
| 83 to 90 | 85 to 92 | P00 to P07 | E (STBC) | General-purpose I/O ports<br>Pull-up resistors can be set (RD07 to RD00 = “1”) using the pull-up resistor setting register (RDR0).<br>The setting does not apply for ports set as outputs (D07 to D00 = “1”: invalid at the output setting). |
| | | AD00 to AD07 | | In external bus mode, the pins function as the lower data I/O or lower address outputs (AD00 to AD07). |
| 91 to 98 | 93 to 100 | P10 to P17 | E (STBC) | General-purpose I/O ports<br>Pull-up resistors can be set (RD17 to RD10 = “1”) using the pull-up resistor setting register (RDR1).<br>The setting does not apply for ports set as outputs (D17 to D10 = “1”: invalid at the output setting). |
| | | AD08 to AD15 | | In 16-bit external bus mode, the pins function as the upper data I/O or middle address outputs (AD08 to AD15). |
| 99, 100, 1 to 6 | 1, 2, 3 to 8 | P20, P21, P22 to P27 | I (STBC) | General-purpose I/O ports<br>In external bus mode, pins for which the corresponding bit in the external address output control register (HACR) is “1” function as the general-purpose I/O pots. |
| | | A16, A17, A18 to A23 | | External address bus output pins (A16 to A23)<br>In external bus mode, pins for which the corresponding bit in the external address output control register (HACR) is “0” function as the upper address output pins (A16 to A23). |
| 7 | 9 | P30 | I (STBC) | General-purpose I/O port<br>Functions as the ALE pin in external bus mode. |
| | | ALE | | Functions as the address latch enable signal. |
| 8 | 10 | P31 | I (STBC) | General-purpose I/O port<br>Functions as the $\overline{RD}$ pin in external bus mode. |
| | | $\overline{RD}$ | | Functions as the read strobe output ($\overline{RD}$). |
| 10 | 12 | P32 | I (STBC) | General-purpose I/O port<br>Functions as the $\overline{WRL}$ pin in external bus mode if the WRE bit in the ECSR register is “1”. |
| | | $\overline{WRL}$ | | Functions as the lower data write strobe output ($\overline{WRL}$). |

*(Continued)*

| Pin no. | | Pin name | Circuit type | Function |
|---|---|---|---|---|
| LQFP*1 | QFP*2 | | | |
| 11 | 13 | P33 | I (STBC) | General-purpose I/O port<br>Functions as the $\overline{WRH}$ pin in 16-bit external bus mode if the WRE bit in the ECSR register is “1”. |
| | | $\overline{WRH}$ | | Functions as the upper data write strobe output ($\overline{WRH}$). |
| 12 | 14 | P34 | I (STBC) | General-purpose I/O port<br>Functions as the HRQ pin in external bus mode if the HDE bit in the ECSR register is “1”. |
| | | HRQ | | Functions as the hold request input pin (HRQ). |
| 13 | 15 | P35 | I (STBC) | General-purpose I/O port<br>Functions as the $\overline{HAK}$ pin in external bus mode if the HDE bit in the ECSR register is “1”. |
| | | $\overline{HAK}$ | | Functions as the hold acknowledge output ($\overline{HAK}$) pin. |
| 14 | 16 | P36 | I (STBC) | General-purpose I/O port<br>Functions as the RDY pin in external bus mode if the RYE bit in the ECSR register is “1”. |
| | | RDY | | Functions as the external ready input (RDY) pin. |
| 15 | 17 | P37 | I (STBC) | General-purpose I/O port<br>Functions as the CLK pin in external bus mode if the CKE bit in the ECSR register is “1”. |
| | | CLK | | Functions as the machine cycle clock output (CLK) pin. |
| 16 | 18 | P40 | H (STBC) | General-purpose I/O port<br>When UART0 is operating, the data at the pin is used as the serial input (SIN0).<br>Can be set as an open-drain output port (OD40 = “1”) by the open-drain control register (ODR4).<br>The setting does not apply for ports set as inputs (D40 = “0”: invalid at the input setting). |
| | | SIN0 | | Functions as the UART0 serial input (SIN0). |
| 17 | 19 | P41 | G (STBC) | General-purpose I/O port<br>Functions as the SOT0 pin if the SOE bit in the UMC register is “1”.<br>Can be set as an open-drain output port (OD41 = “1”) by the open-drain control register (ODR4).<br>The setting does not apply for ports set as inputs (D41 = “0”: invalid at the input setting). |
| | | SOT0 | | Functions as the UART0 serial data output pin (SOT0). |

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| Pin no. | | Pin name | Circuit type | Function |
|---|---|---|---|---|
| LQFP*1 | QFP*2 | | | |
| 18 | 20 | P42 | H (STBC) | General-purpose I/O port<br>When UART0 is operating in external shift clock mode, the data at the pin is used as the clock input (SCK0).<br>Also, functions as the SCK0 pin if the SOE bit in the UMC register is “1”.<br>Can be set as an open-drain output port (OD42 = “1”) by the open-drain control register (ODR4).<br>The setting does not apply for ports set as inputs (D42 = “0”: invalid at the input setting). |
| | | SCK0 | | Functions as the UART0 serial clock I/O pin (SCK0). |
| 19 | 21 | P43 | H (STBC) | General-purpose I/O port<br>When I/O extended serial is operating, the data at the pin is used as the serial input (SIN1).<br>Can be set as an open-drain output port (OD43 = “1”) by the open-drain control register (ODR4).<br>The setting does not apply for ports set as inputs (D43 = “0”: invalid at the input setting). |
| | | SIN1 | | Functions as the serial input for I/O extended serial data. |
| 20 | 22 | P44 | G (STBC) | General-purpose I/O port<br>Functions as the SOT1 pin if the SOE bit in the UMC register is “1”.<br>Can be set as an open-drain output port (OD44 = “1”) by the open-drain control register (ODR4).<br>The setting does not apply for ports set as inputs (D44 = “0”: invalid at the input setting). |
| | | SOT1 | | Functions as the output pin (SOT1) for I/O extended serial data. |
| 22 | 24 | P45 | H (STBC) | General-purpose I/O port<br>When I/O extended serial is operating in external shift clock mode, the data at the pin is used as the clock input (SCK1).<br>Also, functions as the SCK1 pin if the SOE bit in the UMC register is “1”.<br>Can be set as an open-drain output port (OD45 = “1”) by the open-drain control register (ODR4).<br>The setting does not apply for ports set as inputs (D45 = “0”: invalid at the input setting). |
| | | SCK1 | | Functions as the I/O extended serial clock I/O pin (SCK1). |
| 23 | 25 | P46 | G (STBC) | General-purpose I/O port<br>Can be set as an open-drain output port (OD46 = “1”) by the open-drain control register (ODR4).<br>The setting does not apply for ports set as inputs (D46 = “0”: invalid at the input setting). |
| | | ADTG | | Functions as the external trigger input pin for the A/D converter. |
| 24 | 26 | P47 | K (NMOS/H) (STBC) | Open-drain type general-purpose I/O port |

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| Pin no. | | Pin name | Circuit type | Function |
|---|---|---|---|---|
| LQFP*1 | QFP*2 | | | |
| 36 to 39, 41 to 44 | 38 to 41, 43 to 46 | P50 to P53, P54 to P57 | L (STBC) | General-purpose I/O ports |
| | | AN0 to AN3, AN4 to AN7 | | The pins are used as analog inputs (AN0 to AN7) when the A/D converter is operating. |
| 57 | 59 | P60 | F (STBC) | General-purpose I/O port<br>A pull-up resistor can be set (RD60 = “1”) using the pull-up resistor setting register (RDR6).<br>The setting does not apply for ports set as outputs (D60 = “1”: invalid at the output setting). |
| | | SIN2 | | Functions as a data input pin (SIN2) for I/O extended serial. |
| 58 | 60 | P61 | E (STBC) | General-purpose I/O port<br>Function as the SOT2 pin if the SOE bit in the UMC register is “1”.<br>A pull-up resistor can be set (RD61 = “1”) using the pull-up resistor setting register (RDR6).<br>The setting does not apply for ports set as outputs (D61 = “1”: invalid at the output setting). |
| | | SOT2 | | Functions as an output pin (SOT2) for I/O extended serial data. |
| 59 | 61 | P62 | F (STBC) | General-purpose I/O port<br>When I/O extended serial is operating in external shift clock mode, the data at the pin is used as the clock input (SCK2). Also, functions as the SCK2 pin if the SOE bit in the UMC register is “1”.<br>A pull-up resistor can be set (RD62 = “1”) using the pull-up resistor setting register (RDR6).<br>The setting does not apply for ports set as outputs (D62 = “1”: invalid at the output setting). |
| | | SCK2 | | Functions as the I/O extended serial clock I/O pin (SCK2). |
| 60 | 62 | P63 | E (STBC) | General-purpose I/O port<br>A pull-up resistor can be set (RD63 = “1”) using the pull-up resistor setting register (RDR6).<br>The setting does not apply for ports set as outputs (D63 = “1”: invalid at the output setting). |
| | | PPG00 | | Functions as the PPG00 output when PPG output is enabled. |
| 61 | 63 | P64 | E (STBC) | General-purpose I/O port<br>A pull-up resistor can be set (RD64 = “1”) using the pull-up resistor setting register (RDR6).<br>The setting does not apply for ports set as outputs (D64 = “1”: invalid at the output setting). |
| | | PPG01 | | Functions as the PPG01 output when PPG output is enabled. |

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| Pin no. | | Pin name | Circuit type | Function |
|---|---|---|---|---|
| LQFP*1 | QFP*2 | | | |
| 62 | 64 | P65 | E (STBC) | General-purpose I/O port<br>A pull-up resistor can be set (RD65 = “1”) using the pull-up resistor setting register (RDR6).<br>The setting does not apply for ports set as outputs (D65 = “1”: invalid at the output setting). |
| | | CKOT | | Functions as the CKOT output when CKOT is operating. |
| 63 | 65 | P66 | E (STBC) | General-purpose I/O port<br>A pull-up resistor can be set (RD66 = “1”) using the pull-up resistor setting register (RDR6).<br>The setting does not apply for ports set as outputs (D66 = “1”: invalid at the output setting). |
| | | PPG10 | | Functions as the PPG10 output when PPG output is enabled. |
| 64 | 66 | P67 | E (STBC) | General-purpose I/O port<br>A pull-up resistor can be set (RD67 = “1”) using the pull-up resistor setting register (RDR6).<br>The setting does not apply for ports set as outputs (D67 = “1”: invalid at the output setting). |
| | | PPG11 | | Functions as the PPG11 output when PPG output is enabled. |
| 25 | 27 | P70 | K (NMOS/H) (STBC) | Open-drain type I/O port |
| | | SDA | | $I^2C$ interface data I/O pin<br>This function is valid when $I^2C$ interface operations are enabled.<br>Set port output to Hi-Z (PDR = 1) during $I^2C$ interface operations. |
| 26 | 28 | P71 | K (NMOS/H) (STBC) | Open-drain type I/O port |
| | | SCL | | $I^2C$ interface clock I/O pin<br>This function is valid when $I^2C$ interface operations are enabled.<br>Set port output to Hi-Z (PDR = 1) during $I^2C$ interface operations. |
| 27 | 29 | P72 | K (STBC) | Open-drain type I/O port |
| 30 | 32 | P73 | M (STBC) | Open-drain type I/O port<br>Functions as a D/A output pin when DAE0 = “1” in the D/A control register (DACR). |
| | | DA00 | | Functions as D/A output 0 when the D/A converter is operating. |
| 31 | 33 | P74 | M (STBC) | General-purpose I/O port<br>Functions as a D/A output pin when DAE1 = “1” in the D/A control register (DACR). |
| | | DA01 | | Functions as D/A output 1 when the D/A converter is operating. |
| 45 | 47 | P80 | J | General-purpose I/O port |
| | | IRQ0 | | Functions as external interrupt request I/O 0. |

*(Continued)*

| Pin no. | | Pin name | Circuit type | Function |
|---|---|---|---|---|
| LQFP*1 | QFP*2 | | | |
| 46 | 48 | P81 | J | General-purpose I/O port |
| | | IRQ1 | | Functions as external interrupt request I/O 1. |
| 51 | 53 | P82 | J | General-purpose I/O port |
| | | IRQ2 | | Functions as external interrupt request I/O 2. |
| 52 | 54 | P83 | J | General-purpose I/O port |
| | | IRQ3 | | Functions as external interrupt request I/O 3. |
| 53 | 55 | P84 | J | General-purpose I/O port |
| | | IRQ4 | | Functions as external interrupt request I/O 4. |
| 54 | 56 | P85 | J | General-purpose I/O port |
| | | IRQ5 | | Functions as external interrupt request I/O 5. |
| 55 | 57 | P86 | I (STBC) | General-purpose I/O port<br>This applies in all cases. |
| | | OUT3 | | Event output for channel 3 of the output compare |
| 65 | 67 | P90 | J | General-purpose I/O port |
| | | AIN0 | | Input to channel 0 of the 8/16-bit up/down counter/timer |
| | | IRQ6 | | Functions as an interrupt request input. |
| 66 | 68 | P91 | J (STBC) | General-purpose I/O port |
| | | BIN0 | | Input to channel 0 of the 8/16-bit up/down counter/timer |
| 67 | 69 | P92 | J (STBC) | General-purpose I/O port |
| | | ZIN0 | | Input to channel 0 of the 8/16-bit up/down counter/timer |
| 68 | 70 | P93 | J | General-purpose I/O port |
| | | AIN1 | | Input to channel 1 of the 8/16-bit up/down counter/timer |
| | | IRQ7 | | Functions as an interrupt request input. |
| 69 | 71 | P94 | J (STBC) | General-purpose I/O port |
| | | BIN1 | | Input to channel 1 of the 8/16-bit up/down counter/timer |
| 70 | 72 | P95 | J (STBC) | General-purpose I/O port |
| | | ZIN1 | | Input to channel 1 of the 8/16-bit up/down counter/timer |
| 71 | 73 | P96 | J (STBC) | General-purpose I/O port |
| | | IN0 | | Trigger input for channel 0 of the input capture |
| 72 | 74 | P97 | J (STBC) | General-purpose I/O port |
| | | IN1 | | Trigger input for channel 1 of the input capture |
| 73 | 75 | PA0 | I (STBC) | General-purpose I/O port |
| | | OUT0 | | Event output for channel 0 of the output compare |

*(Continued)*

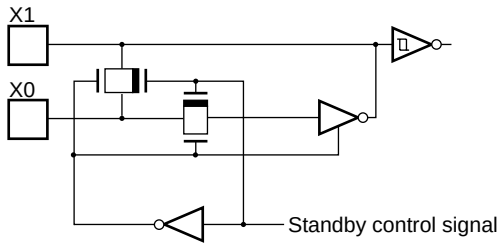
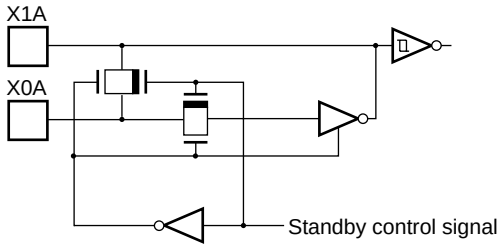
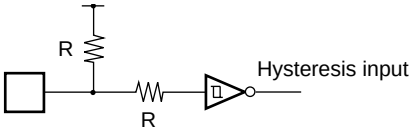
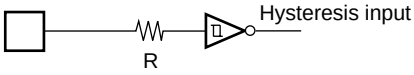
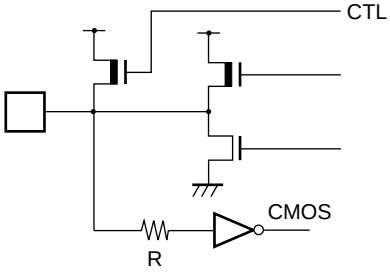
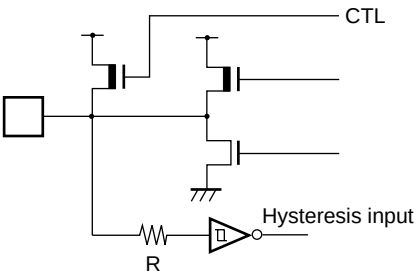
*(Continued)*

| Pin no. | | Pin name | Circuit type | Function |
|---|---|---|---|---|
| LQFP*1 | QFP*2 | | | |
| 74 | 76 | PA1 | I (STBC) | General-purpose I/O port |
| | | OUT1 | | Event output for channel 1 of the output compare |
| 76 | 78 | PA2 | I (STBC) | General-purpose I/O port |
| | | OUT2 | | Event output for channel 2 of the output compare |
| 82 | 84 | $V_{CC}1$ | — | Power supply (3.0 V) input pin |
| 21 | 23 | $V_{CC}2$ | — | Power supply (3.0 V/5.0 V) input pin |
| 9, 40, 79 | 11, 42, 81 | $V_{SS}$ | — | Power supply (0.0 V) input pin |
| 32 | 34 | $AV_{CC}$ | — | A/D converter power supply pin |
| 33 | 35 | AVRH | — | A/D converter external reference power supply pin |
| 34 | 36 | AVRL | — | A/D converter external reference power supply pin |
| 35 | 37 | $AV_{SS}$ | — | A/D converter power supply pin |
| 28 | 30 | DVRH | — | D/A converter external reference power supply pin |
| 29 | 31 | $DV_{SS}$ | — | D/A converter power supply pin |
| 56 | 58 | DTMF | N | DTMF output pin |

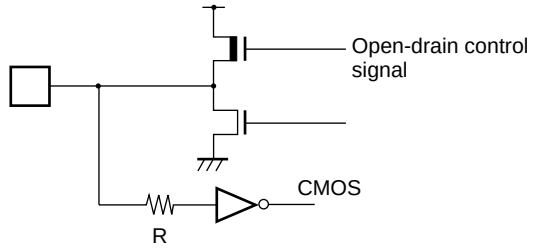
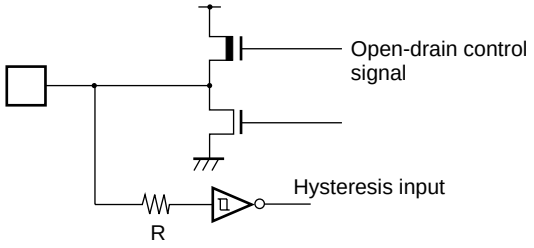
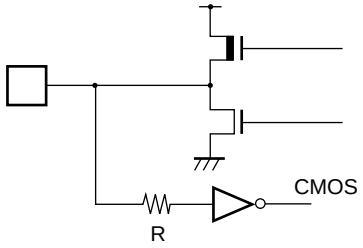
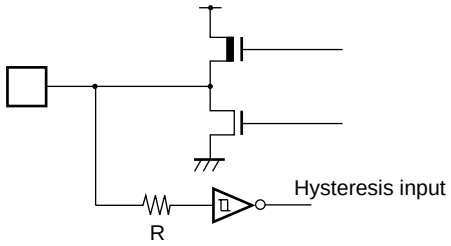
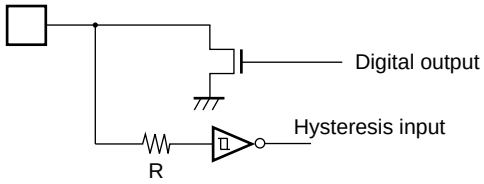
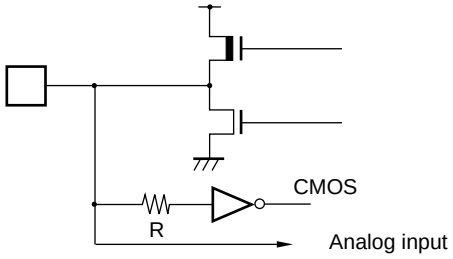
*1: FPT-100P-M05
*2: FPT-100P-M06

Note : STBC = Incorporates standby control
NMOS = N-ch open-drain output

## ■ I/O CIRCUIT TYPE

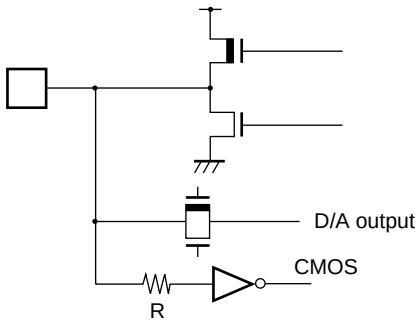
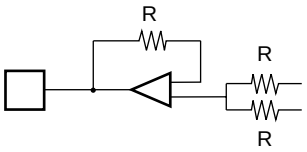
| Type | Circuit | Remarks |
|---|---|---|
| A |  | • Oscillation feedback resistance: Approx. 1 MΩ |
| B |  | • Oscillation feedback resistance: Approx. 10 MΩ |
| C |  | • Hysteresis input with pull-up Resistance approx. 50 kΩ |
| D |  | • Hysteresis input port |
| E |  | • Incorporates pull-up resistor control (for input)<br>• CMOS level I/O<br>Resistance approx. 50 kΩ |
| F |  | • Incorporates pull-up resistor control (for input)<br>• CMOS level output<br>• Hysteresis input<br>Resistance approx. 50 kΩ |

*(Continued)*

| Type | Circuit | Remarks |
|---|---|---|
| G |  | • CMOS level I/O<br>• Incorporates open-drain control |
| H |  | • CMOS level output<br>• Hysteresis input<br>• Incorporates open-drain control |
| I |  | • CMOS level I/O |
| J |  | • CMOS level output<br>• Hysteresis input |
| K |  | • Hysteresis input<br>• N-ch open-drain output |
| L |  | • CMOS level I/O<br>• Analog input |

*(Continued)*

*(Continued)*

| Type | Circuit | Remarks |
|---|---|---|
| M |  | • CMOS level I/O<br>• Analog output<br>• Shared with D/A outputs |
| N |  | • DTMF analog output |

## ■ HANDLING DEVICES

### 1. Preventing Latch-up

Latch-up occurs in a CMOS IC if a voltage greater than $V_{CC}$ or less than $V_{SS}$ is applied to an input or output pin or if the voltage applied between $V_{CC}$ and $V_{SS}$ exceeds the rating.

If latch-up occurs, the power supply current increases rapidly resulting in thermal damage to circuit elements. Therefore, ensure that maximum ratings are not exceeded in circuit operation.

For the same reason, also ensure that the analog supply voltage does not exceed the digital supply voltage.

### 2. Treatment of Unused Pins

Leaving unused input pins unconnected can cause misoperation. Always pull-up or pull-down unused pins.

### 3. External Reset Input

To reliably reset the controller by inputting an “L” level to the $\overline{RST}$ pin, ensure that the “L” level is applied for at least five machine cycles. Take particular note when using an external clock input.

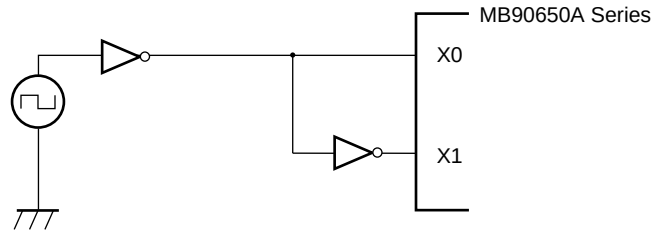
### 4. $V_{CC}$ and $V_{SS}$ Pins

Ensure that all $V_{CC}$ pins are at the same voltage. The same applies for the $V_{SS}$ pins.

### 5. Precautions when Using an External Clock

Drive the X0 pin only when using an external clock.

- **Using an external clock**




### 6. A/D Converter Power Supply and the Turn-on Sequence for Analog Inputs

Always turn off the A/D converter power supply ($AV_{CC}$, AVRH, AVRL) and analog inputs (AN0 to AN7) before turning off the digital power supply ($V_{CC}$).

When turning the power on or off, ensure that AVRH does not exceed $AV_{CC}$.

Also, when using the analog input pins as input ports, ensure that the input voltage does not exceed $AV_{CC}$.

### 7. Turn-on Sequence for D/A Converter Power Supply

Always turn on the D/A converter power supply (DVR), after turning off the digital power supply ($V_{CC}$).

And in the turning off the power supply sequence always turn off the digital power supply ($V_{CC}$) after turning off the D/A converter power supply (DVR).

## 8. Initializing

In this device there are some kinds of inner resisters which are initialized only by power on reset. It is possible to initialize these resisters by turning on the power supply again.

## 9. Power Supply Pins

When there are several $V_{CC}$ and $V_{SS}$ pins, those pins that should have the same electric potential are connected within the device when the device is designed in order to prevent misoperation, such as latchup. However, all of those pins must be connected to the power supply and ground externally in order to reduce unnecessary emissions, prevent misoperation of strobe signals due to an increase in the ground level, and to observe the total output current standards.

In addition, give a due consideration to the connection in that current supply be connected to $V_{CC}$ and $V_{SS}$ with the lowest possible impedance.

Finally, it is recommended to connect a capacitor of about 0.1 µF between $V_{CC}$ and $V_{SS}$ near this device as a bypass capacitor.

## 10. Crystal Oscillation Circuit

Noise in the vicinity of the X0 and X1 pins will cause this device to operate incorrectly. Design the printed circuit board so that the bypass capacitor connecting X0, X1 and the crystal oscillator (or ceramic oscillator) to ground is located as close to the device as possible, and that the wiring does not cross the other wirings.

In addition, because printed circuit board artwork in which the area around the X0 and X1 pins is surrounded by ground provides stable operation, such an arrangement is strongly recommended.

## 11. About 2 Power Supplies

The MB90650A series usually uses the 3-V power supply as the main power source. With Vcc1 = 3 V and Vcc2 = 5 V, however, it can interface with P20/A16 to P27/A23, P30/ALE to P37/CLK, P40/SIN0 to P47, and P70/SDA to P72 for the 5-V power supply separately from the 3-V power supply at all operation mode. Note, however, that the analog power supplies such as A/D and D/A can be used only as 3-V power supplies.

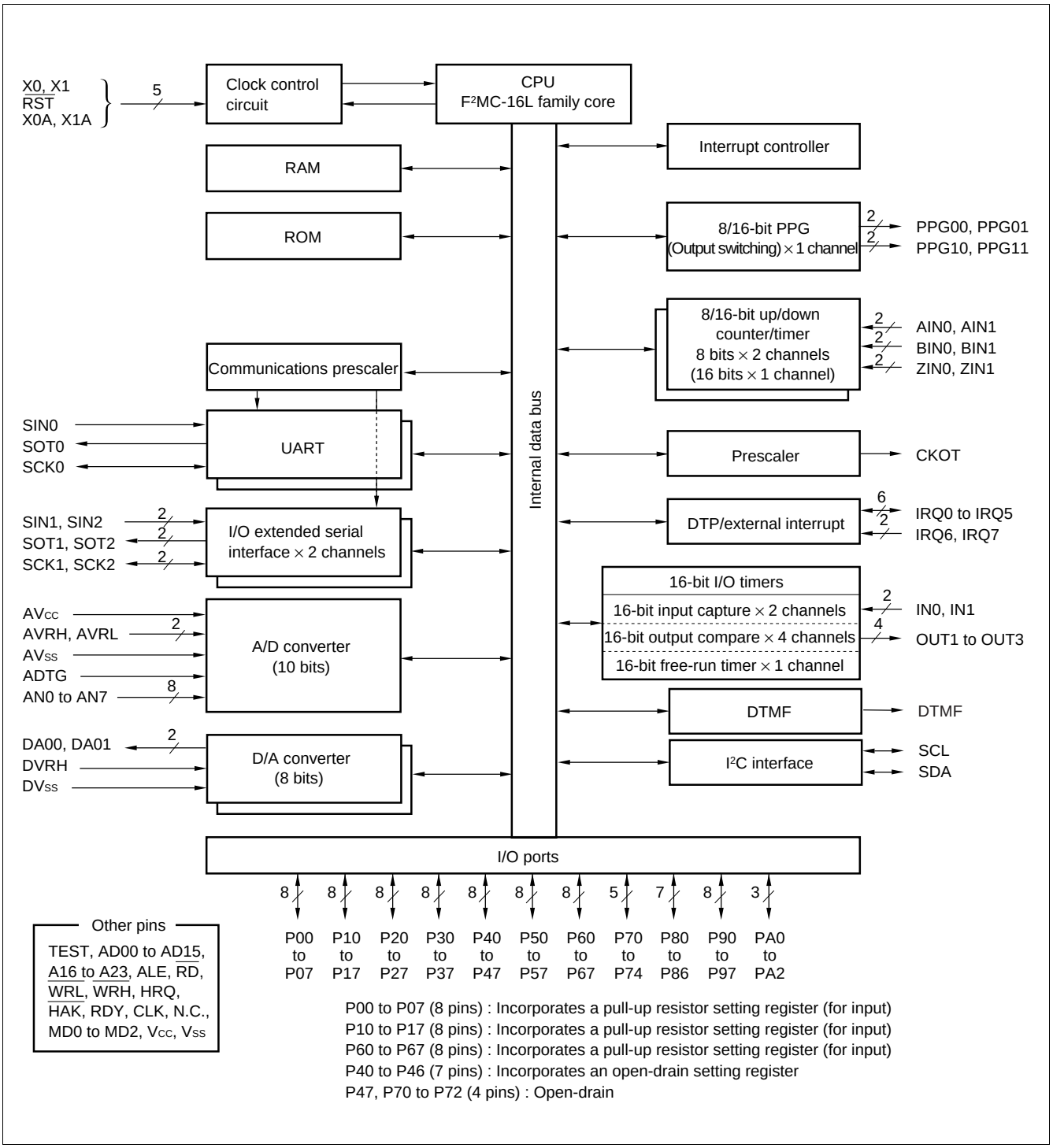
## 12. When not Using a Sub Clock Signal

Also when the sub-clock is not used, X0A and X1A pins should be connected to an oscillator.

## 13. Caution on Operations during PLL Clock Mode

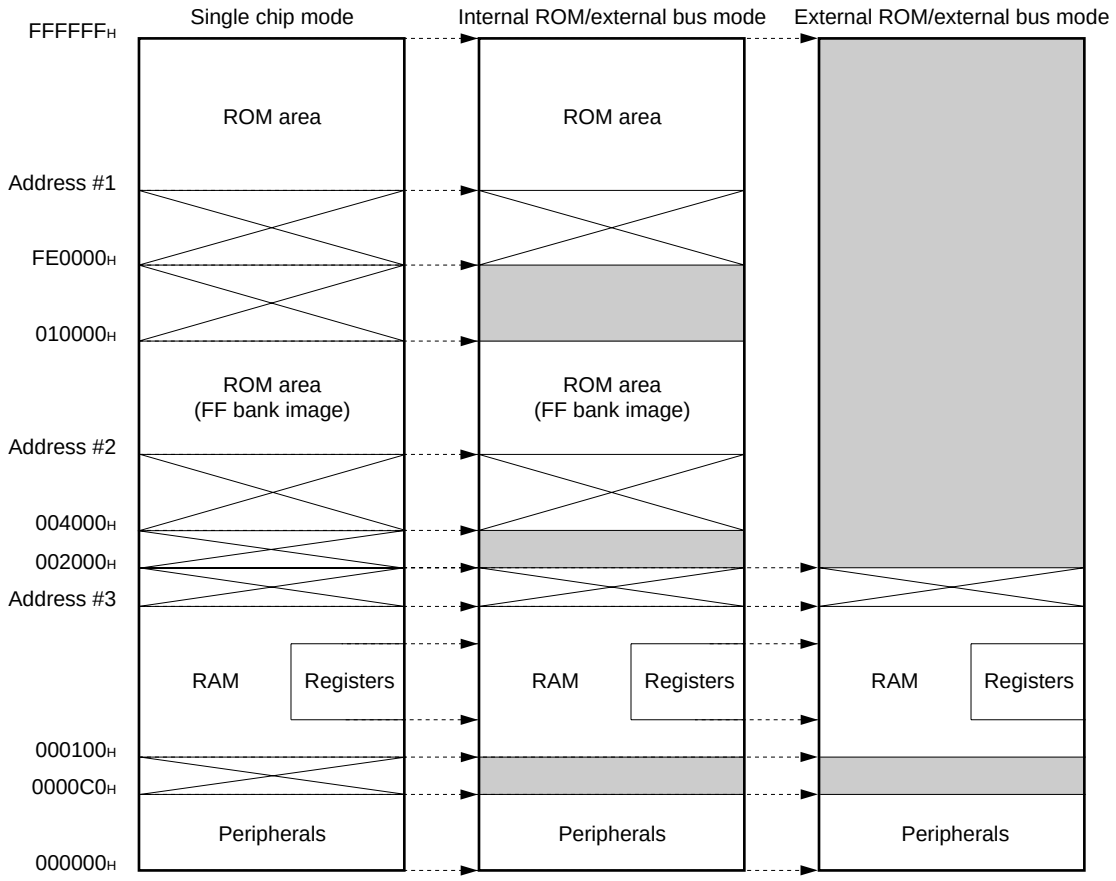
If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

## ■ BLOCK DIAGRAM



## ■ MEMORY MAP

- **MB90652A, MB90653A, MB90V650A**




| Type | Address #1 * | Address #2 * | Address #3 * |
|---|---|---|---|
| MB90652A | FF0000H | 004000H | 000CFFH |
| MB90653A | FE0000H | 004000H | 0014FFH |
| MB90V650A | (FE0000H) | 004000H | 0018FFH |

: Internal access memory

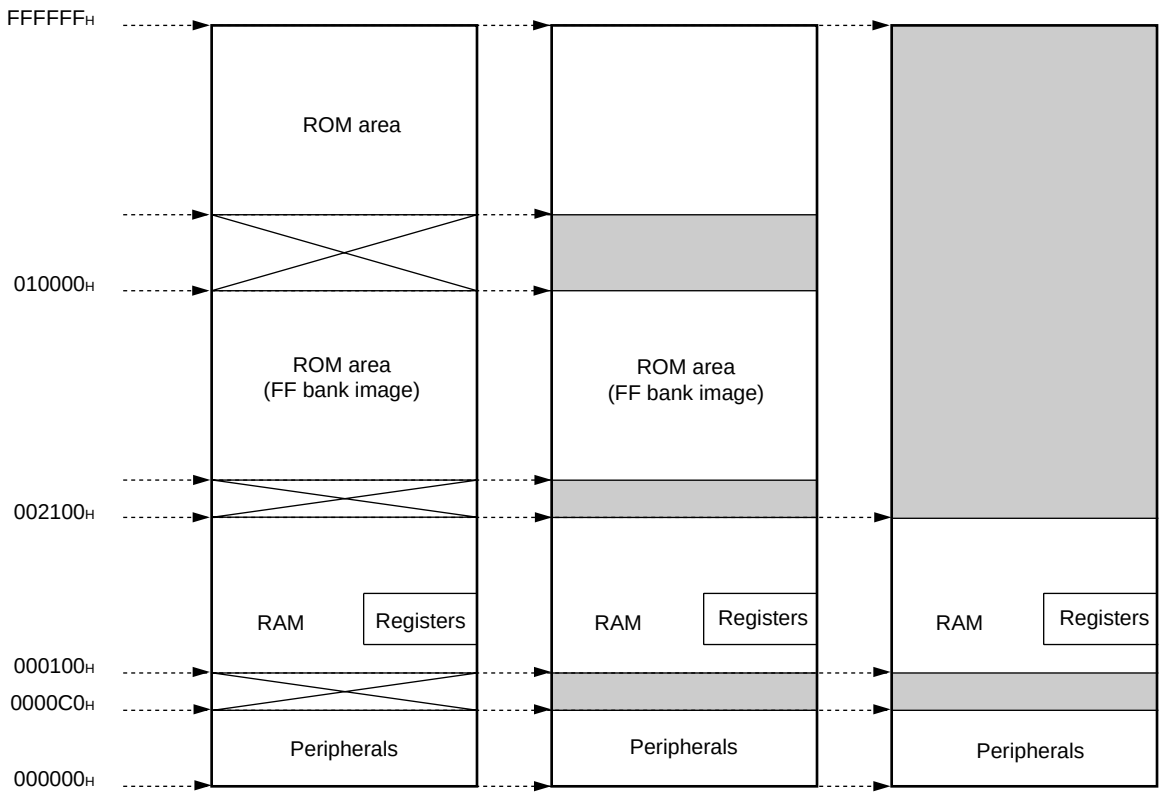
: External access memory

: No access

* : Address #1, #2, and #3 are different owing to their devices respectively.

Note : While the ROM data image of bank FF can be seen in the upper portion of bank 00, this is done only to permit effective use of the C compiler's small model. Because the lower 16 bits are the same, it is possible to reference tables in ROM without declaring the "far" specification in the pointer.
For example, to access to 00C000H is to access to the ROM content of FFC000H in practice.
Because the ROM area of FF bank exceeds 48 Kbytes, all the area can be seen in bank 00.
So, the image for FF4000H to FFFFFFH can be seen in bank 00, while FE0000H to FF3FFFH can only be seen in bank FF and FE.

- **MB90654A, MB90F654A**




| Type | Address #1 | Address #2 | Address #3 |
|---|---|---|---|
| MB90654A* | FC0000H | 004000H | 0020FFH |
| MB90F654A* | FC0000H | 004000H | 0020FFH |

: Internal access memory

: External access memory

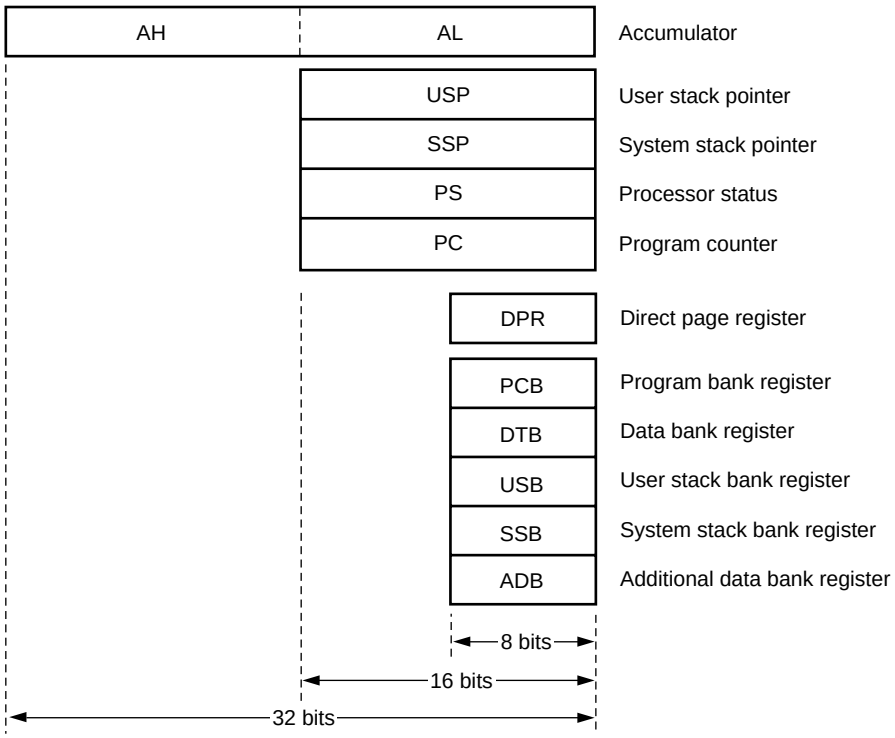
: No access

* : In the MB90654A and MB90F654A, RAM area 2000H is 2100H.

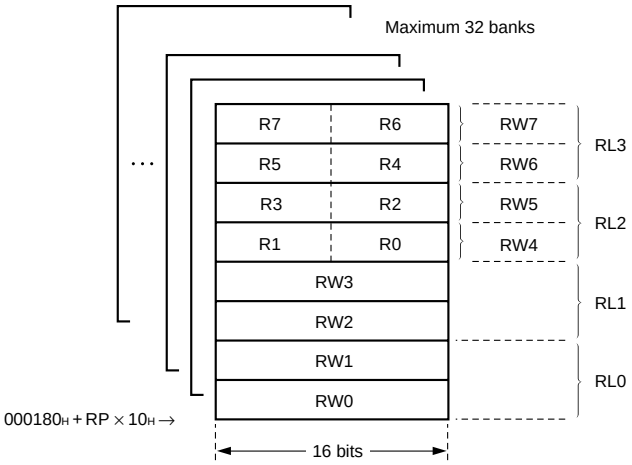
Note : While the ROM data image of bank FF can be seen in the upper portion of bank 00, this is done only to permit effective use of the C compiler's small model. Because the lower 16 bits are the same, it is possible to reference tables in ROM without declaring the "far" specification in the pointer.
For example, to access to 00C000H is to access to the ROM content of FFC000H in practice.
Because the ROM area of FF bank exceeds 48 Kbytes, all the area can be seen in bank 00.
So, the image for FF4000H to FFFFFFH can be seen in bank 00, while FE0000H to FF3FFFH can only be seen in bank FF and FE.

## ■ F²MC-16L CPU PROGRAMMING MODEL

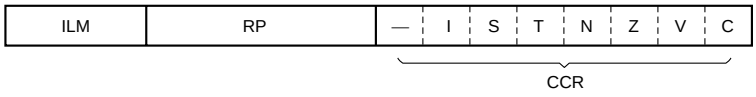
• **Dedicated registers**




• **General-purpose registers**




• **Processor status (PS)**



## ■ I/O MAP

| Address | Register | Register name | Read/ write | Resource name | Initial value |
|---|---|---|---|---|---|
| 00H | Port 0 data register | PDR0 | R/W | Port 0 | XXXXXXXXB |
| 01H | Port 1 data register | PDR1 | R/W | Port 1 | XXXXXXXXB |
| 02H | Port 2 data register | PDR2 | R/W | Port 2 | XXXXXXXXB |
| 03H | Port 3 data register | PDR3 | R/W | Port 3 | XXXXXXXXB |
| 04H | Port 4 data register | PDR4 | R/W | Port 4 | 1XXXXXXXB |
| 05H | Port 5 data register | PDR5 | R/W | Port 5 | XXXXXXXXB |
| 06H | Port 6 data register | PDR6 | R/W | Port 6 | XXXXXXXXB |
| 07H | Port 7 data register | PDR7 | R/W | Port 7 | ---XX111B |
| 08H | Port 8 data register | PDR8 | R/W | Port 8 | -XXXXXXXB |
| 09H | Port 9 data register | PDR9 | R/W | Port 9 | XXXXXXXXB |
| 0AH | Port A data register | PDRA | R/W | Port A | -----XXXB |
| 0BH to 0FH | (Reserved area) | | | | |
| 10H | Port 0 direction register | DDR0 | R/W | Port 0 | 00000000B |
| 11H | Port 1 direction register | DDR1 | R/W | Port 1 | 00000000B |
| 12H | Port 2 direction register | DDR2 | R/W | Port 2 | 00000000B |
| 13H | Port 3 direction register | DDR3 | R/W | Port 3 | 00000000B |
| 14H | Port 4 direction register | DDR4 | R/W | Port 4 | -0000000B |
| 15H | Port 5 direction register | DDR5 | R/W | Port 5 | 00000000B |
| 16H | Port 6 direction register | DDR6 | R/W | Port 6 | 00000000B |
| 17H | Port 7 direction register | DDR7 | R/W | Port 7 | ---00---B |
| 18H | Port 8 direction register | DDR8 | R/W | Port 8 | -0000000B |
| 19H | Port 9 direction register | DDR9 | R/W | Port 9 | 00000000B |
| 1AH | Port A direction register | DDRA | R/W | Port A | -----000B |
| 1BH | Port 4 pin register | ODR4 | R/W | Port 4 | -0000000B |
| 1CH | Port 0 resistance register | RDR0 | R/W | Port 0 | 00000000B |
| 1DH | Port 1 resistance register | RDR1 | R/W | Port 1 | 00000000B |
| 1EH | Port 6 resistance register | RDR6 | R/W | Port 6 | 00000000B |
| 1FH | Analog input enable register | ADER | R/W | Port 5, A/D | 11111111B |
| 20H | Serial mode register 0 | SMR0 | R/W | UART0 | 00000000B |
| 21H | Serial control register 0 | SCR0 | R/W | | 00000100B |
| 22H | Serial input register/ serial output register 0 | SIDR/ SODR0 | R/W | | XXXXXXXXB |

*(Continued)*

| Address | Register | Register name | Read/ write | Resource name | Initial value |
|---|---|---|---|---|---|
| 23H | Serial status register 0 | SSR0 | R/W | UART0 | 00001–00B |
| 24H | Serial mode control status register 0 | SMCS0 | R/W | I/O extended serial interface 0 | ––––0000B |
| 25H | Serial mode control status register 0 | SMCS0 | R/W | | 00000010B |
| 26H | Serial data register 0 | SDR0 | R/W | | XXXXXXXXB |
| 27H | Clock division control register | CDCR | R/W | Communications prescaler | 0–––1111B |
| 28H | Serial mode control status register 1 | SMCS1 | R/W | I/O extended serial interface 1 | ––––0000B |
| 29H | Serial mode control status register 1 | SMCS1 | R/W | | 00000010B |
| 2AH | Serial data register 1 | SDR1 | R/W | | XXXXXXXXB |
| 2BH to 2FH | (Reserved area) | | | | |
| 30H | Interrupt/DTP enable register | ENIR | R/W | DTP/external interrupts | 00000000B |
| 31H | Interrupt/DTP source register | EIRR | R/W | | 00000000B |
| 32H | Request level setting register | ELVR | R/W | | 00000000B |
| 33H | | | | | 00000000B |
| 34H to 35H | (Reserved area) | | | | |
| 36H | Control status register 1 | ADCS1 | R/W | A/D converter | 00000000B |
| 37H | Control status register 2 | ADCS2 | | | 00000000B |
| 38H | Data register 1 | ADCR1 | R | | XXXXXXXXB |
| 39H | Data register 2 | ADCR2 | | | XXXXXXXXB |
| 3AH | D/A converter data register 0 | DAT0 | R/W | D/A converter | XXXXXXXXB |
| 3BH | D/A converter data register 1 | DAT1 | R/W | | XXXXXXXXB |
| 3CH | D/A control register channel 0 | DACR0 | R/W | | –––––––0B |
| 3DH | D/A control register channel 1 | DACR1 | R/W | | –––––––0B |
| 3EH | Clock control register | CLKR | R/W | Clock output control register | ––––0000B |
| 3FH | (Reserved area) | | | | |
| 40H | Reload register lower channel 0 | PRLL0 | R/W | 8/16-bit PPG | XXXXXXXXB |
| 41H | Reload register upper channel 0 | PRLH0 | R/W | | XXXXXXXXB |
| 42H | Reload register lower channel 1 | PRLL1 | R/W | | XXXXXXXXB |
| 43H | Reload register upper channel 1 | PRLH1 | R/W | | XXXXXXXXB |
| 44H | PPG0 operation mode control register channel 0 | PPGC0 | R/W | | 0X000XX1B |
| 45H | PPG1 operation mode control register channel 1 | PPGC1 | R/W | | 0X000001B |
| 46H | PPG0, PPG1 output control register channel 0, channel 1 | PPGOE | R/W | | 00000000B |
| 47H to 4FH | (Reserved area) | | | | |
| 50H | Lower compare register channel 0 | OCCP0 | R/W | 16-bit I/O timer output compare (channel 0 to channel 3) | XXXXXXXXB |

*(Continued)*

| Address | Register | Register name | Read/ write | Resource name | Initial value |
|---|---|---|---|---|---|
| 51H | Upper compare register channel 0 | OCCP0 | R/W | 16-bit I/O timer Output compare (channel 0 to channel 3) | XXXXXXXXB |
| 52H | Lower compare register channel 1 | OCCP1 | R/W | | XXXXXXXXB |
| 53H | Upper compare register channel 1 | | | | XXXXXXXXB |
| 54H | Lower compare register channel 2 | OCCP2 | R/W | | XXXXXXXXB |
| 55H | Upper compare register channel 2 | | | | XXXXXXXXB |
| 56H | Lower compare register channel 3 | OCCP3 | R/W | | XXXXXXXXB |
| 57H | Upper compare register channel 3 | | | | XXXXXXXXB |
| 58H | Compare control status register channel 0 | OCS0 | R/W | | 0000––00B |
| 59H | Compare control status register channel 1 | OCS1 | R/W | | –––00000B |
| 5AH | Compare control status register channel 2 | OCS2 | R/W | | 0000––00B |
| 5BH | Compare control status register channel 3 | OCS3 | R/W | | –––00000B |
| 5CH to 5FH | (Reserved area) | | | | |
| 60H | Lower input capture register channel 0 | IPCP0 | R | 16-bit I/O timer Input capture (channel 0, channel 1) | XXXXXXXXB |
| 61H | Upper input capture register channel 0 | | R | | XXXXXXXXB |
| 62H | Lower input capture register channel 1 | IPCP1 | R | | XXXXXXXXB |
| 63H | Upper input capture register channel 1 | | R | | XXXXXXXXB |
| 64H | Input capture control status register | ICS0, 1 | R/W | | 00000000B |
| 65H | (Reserved area) | | | | |
| 66H | Lower timer data register | TCDTL | R/W | 16-bit I/O timer Free-run timer | 00000000B |
| 67H | Upper timer data register | TCDTH | R/W | | 00000000B |
| 68H | Timer control status register | TCCS | R/W | | 00000000B |
| 69H to 6FH | (Reserved area) | | | | |
| 70H | Up/down count register channel 0 | UDCR0 | R | 8/16-bit up/down counter/timer | 00000000B |
| 71H | Up/down count register channel 1 | UDCR1 | | | 00000000B |
| 72H | Reload compare register channel 0 | RCR0 | W | | 00000000B |
| 73H | Reload compare register channel 1 | RCR1 | | | 00000000B |
| 74H | Counter status register channel 0 | CSR0 | R/W | | 00000000B |
| 75H | (Reserved area) | | | | |
| 76H | Counter control register channel 0 | CCRL0 | R/W | 8/16-bit up/down counter/timer | 00001000B |
| 77H | | CCRH0 | | | 00000000B |
| 78H | Counter status register channel 1 | CSR1 | R/W | | 00000000B |
| 79H | (Reserved area) | | | | |
| 7AH | Counter control register channel 1 | CCRL1 | R/W | 8/16-bit up/down counter/timer | 00000000B |

*(Continued)*

| Address | Register | Register name | Read/ write | Resource name | Initial value |
|---|---|---|---|---|---|
| 7BH | Counter control register channel 1 | CCRH1 | R/W | 8/16-bit up/down counter/timer | X0001000B |
| 7CH to 7FH | (Reserved area) | | | | |
| 80H | I²C bus status register | IBSR | R | I²C interface | 00000000B |
| 81H | I²C bus control register | IBCR | R/W | | 00000000B |
| 82H | I²C bus clock control register | ICCR | R/W | | ––0XXXXXB |
| 83H | I²C bus address register | IADR | R/W | | –XXXXXXXB |
| 84H | I²C bus data register | IDAR | R/W | | XXXXXXXXB |
| 85H to 87H | (Reserved area) | | | | |
| 88H | DTMF control register | DTMC | — | — | 00000000B |
| 89H | DTMF data register | DTMD | — | — | 000X0000B |
| 8A to 9EH | (Reserved area) (Accessing 90H to 9EH is prohibited) | | | | |
| 9FH | Delayed interrupt generation/ release register | DIRR | R/W | Delayed interrupt generation module | –––––––0B |
| A0H | Low-power consumption mode control register | LPMCR | R/W | Low-power consumption mode | 00011000B |
| A1H | Clock selection register | CKSCR | R/W | Low-power consumption mode | 11111100B |
| A2H to A4H | (Reserved area) | | | | |
| A5H | Auto-ready function selection register | ARSR | W | External bus pin control circuit | 0011––00B |
| A6H | External address output control register | HACR | W | External bus pin control circuit | 00000000B |
| A7H | Bus control signal selection register | ECSR | W | External bus pin control circuit | 0000*00–B |
| A8H | Watchdog timer control register | WDTC | R/W | Watchdog timer | XXXXX111B |
| A9H | Timebase timer control register | TBTC | R/W | Timebase timer | 1––00000B |
| AAH | Watch timer control register | WTC | R/W | Watch timer | 1X–00000B |
| ABH to AFH | (Reserved area) | | | | |

*(Continued)*

*(Continued)*

| Address | Register | Register name | Read/ write | Resource name | Initial value |
|---|---|---|---|---|---|
| B0H | Interrupt control register 00 | ICR00 | R/W | Interrupt controller | 00000111B |
| B1H | Interrupt control register 01 | ICR01 | R/W | | 00000111B |
| B2H | Interrupt control register 02 | ICR02 | R/W | | 00000111B |
| B3H | Interrupt control register 03 | ICR03 | R/W | | 00000111B |
| B4H | Interrupt control register 04 | ICR04 | R/W | | 00000111B |
| B5H | Interrupt control register 05 | ICR05 | R/W | | 00000111B |
| B6H | Interrupt control register 06 | ICR06 | R/W | | 00000111B |
| B7H | Interrupt control register 07 | ICR07 | R/W | | 00000111B |
| B8H | Interrupt control register 08 | ICR08 | R/W | | 00000111B |
| B9H | Interrupt control register 09 | ICR09 | R/W | | 00000111B |
| BAH | Interrupt control register 10 | ICR10 | R/W | | 00000111B |
| BBH | Interrupt control register 11 | ICR11 | R/W | | 00000111B |
| BCH | Interrupt control register 12 | ICR12 | R/W | | 00000111B |
| BDH | Interrupt control register 13 | ICR13 | R/W | | 00000111B |
| BEH | Interrupt control register 14 | ICR14 | R/W | | 00000111B |
| BFH | Interrupt control register 15 | ICR15 | R/W | | 00000111B |
| C0H to FFH | (External area) | | | | |

About Programming

R/W : Readable and writable
R : Read only
W : Write only

Explanation of initial values

0: The initial value of this bit is “0”.
1: The initial value of this bit is “1”.
* : The initial value of this bit is “0” or “1”.
X: The initial value of this bit is undefined.
–: This bit is not used. The initial value is undefined.

Note : Areas below address 0000FFH not listed in the table are reserved areas. These addresses are accessed by internal access. No access signals are output on the external bus.

## ■ INTERRUPT VECTOR AND INTERRUPT CONTROL REGISTER ASSIGNMENTS TO INTERRUPT SOURCES

| Interrupt source | I²OS support | Interrupt vector | | Interrupt control register | |
|---|---|---|---|---|---|
| | | Number | Address | Number | Address |
| Reset | × | #08 | FFFFDC$_H$ | — | — |
| INT 9 instruction | × | #09 | FFFFD8$_H$ | — | — |
| Exception | × | #10 | FFFFD4$_H$ | — | — |
| A/D converter | ○ | #11 | FFFFD0$_H$ | ICR00 | 0000B0$_H$ |
| Timebase timer interval interrupt | × | #12 | FFFFCC$_H$ | | |
| DTP/external interrupt 0 (External interrupt 0) | ○ | #13 | FFFFC8$_H$ | ICR01 | 0000B1$_H$ |
| 16-bit free-run timer (I/O timer) overflow | ○ | #14 | FFFFC4$_H$ | | |
| I/O extended serial interface 1 | ○ | #15 | FFFFC0$_H$ | ICR02 | 0000B2$_H$ |
| DTP/external interrupt 1 (External interrupt 1) | ○ | #16 | FFFFBC$_H$ | | |
| I/O extended serial interface 2 | ○ | #17 | FFFFB8$_H$ | ICR03 | 0000B3$_H$ |
| DTP/external interrupt 2 (External interrupt 2) | ○ | #18 | FFFFB4$_H$ | | |
| DTP/external interrupt 3 (External interrupt 3) | ○ | #19 | FFFFB0$_H$ | ICR04 | 0000B4$_H$ |
| 8/16-bit PPG 0 counter borrow | ○ | #20 | FFFFAC$_H$ | | |
| 8/16-bit up/down counter/timer 0 compare | ○ | #21 | FFFFA8$_H$ | ICR05 | 0000B5$_H$ |
| 8/16-bit up/down counter/timer 0 underflow/overflow, up/down invert | ○ | #22 | FFFFA4$_H$ | | |
| 8/16-bit PPG 1 counter borrow | ○ | #23 | FFFFA0$_H$ | ICR06 | 0000B6$_H$ |
| DTP/external interrupt 4/5 (External interrupt 4/5) | ○ | #24 | FFFF9C$_H$ | | |
| Output compare (channel 2) match (I/O timer) | ○ | #25 | FFFF98$_H$ | ICR07 | 0000B7$_H$ |
| Output compare (channel 3) match (I/O timer) | ○ | #26 | FFFF94$_H$ | | |
| Watch prescaler | × | #27 | FFFF90$_H$ | ICR08 | 0000B8$_H$ |
| DTP/external interrupt 6 (External interrupt 6) | ○ | #28 | FFFF8C$_H$ | | |
| 8/16-bit up/down counter/timer 1 compare | ○ | #29 | FFFF88$_H$ | ICR09 | 0000B9$_H$ |
| 8/16-bit up/down counter/timer 1 underflow/overflow, up/down invert | ○ | #30 | FFFF84$_H$ | | |
| Input capture (channel 0) read (I/O timer) | ○ | #31 | FFFF80$_H$ | ICR10 | 0000BA$_H$ |
| Input capture (channel 1) read (I/O timer) | ○ | #32 | FFFF7C$_H$ | | |
| Output compare (channel 0) match (I/O timer) | ○ | #33 | FFFF78$_H$ | ICR11 | 0000BB$_H$ |
| Output compare (channel 1) match (I/O timer) | ○ | #34 | FFFF74$_H$ | | |
| Completion of flash memory write/erase | × | #35 | FFFF70$_H$ | ICR12 | 0000BC$_H$ |
| DTP/external interrupt 7 (External interrupt 7) | ○ | #36 | FFFF6C$_H$ | | |
| UART0 receive complete | ◎ | #37 | FFFF68$_H$ | ICR13 | 0000BD$_H$ |
| UART0 transmit complete | ◎ | #39 | FFFF60$_H$ | ICR14 | 0000BE$_H$ |
| I²C interface | × | #41 | FFFF58$_H$ | ICR15 | 0000BF$_H$ |
| Delayed interrupt generation module | × | #42 | FFFF54$_H$ | | |

○: Indicates that the interrupt request flag is cleared by the I²OS interrupt clear signal.
◎: Indicates that the interrupt request flag is cleared by the I²OS interrupt clear signal (stop request present).
×: Indicates that the interrupt request flag is not cleared by the I²OS interrupt clear signal.
Note: For resources in which two interrupt sources share the same interrupt number, the I²OS interrupt clear signal clears both interrupt request flags.

## ■ PERIPHERAL RESOURCES

### 1. Parallel Ports

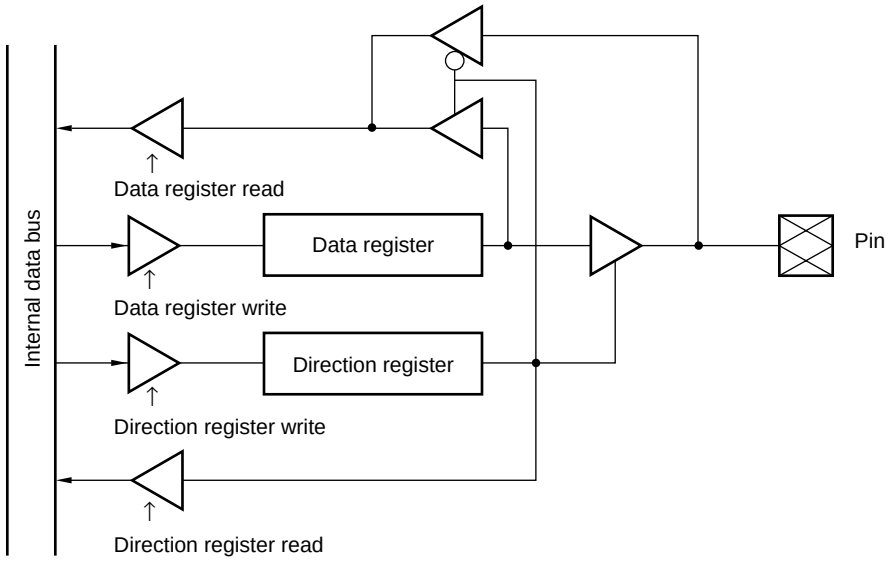
#### (1) I/O Ports

Each port pin can be specified as either an input or output by its corresponding direction register when the pin is not set for use by a peripheral. When a port is set as an input, reading the data register always reads the value corresponding to the pin level. When a port is set as an output, reading the data register reads the data register latch value. The same applies when reading using a read-modify-write instruction.

When used as control outputs, reading the data register reads the control output value, irrespective of the direction register value.

Note that if a read-modify-write instruction (set bit or similar instruction) is used to set output data in the data register before switching a pin from input to output, the instruction reads the input level at the pin and not the data register latch value.

- **Block diagram**



## (2) Port Direction Registers

**• Port 0 data register (PDR0)**

| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value | Access |
|---|---|---|---|---|---|---|---|---|---|---|
| Address : 000000H | P07 | P06 | P05 | P04 | P03 | P02 | P01 | P00 | XXXXXXXXB | R/W* |

**• Port 1 data register (PDR1)**

| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value | Access |
|---|---|---|---|---|---|---|---|---|---|---|
| Address : 000001H | P17 | P16 | P15 | P14 | P13 | P12 | P11 | P10 | XXXXXXXXB | R/W* |

**• Port 2 data register (PDR2)**

| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value | Access |
|---|---|---|---|---|---|---|---|---|---|---|
| Address : 000002H | P27 | P26 | P25 | P24 | P23 | P22 | P21 | P20 | XXXXXXXXB | R/W* |

**• Port 3 data register (PDR3)**

| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value | Access |
|---|---|---|---|---|---|---|---|---|---|---|
| Address : 000003H | P37 | P36 | P35 | P34 | P33 | P32 | P31 | P30 | XXXXXXXXB | R/W* |

**• Port 4 data register (PDR4)**

| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value | Access |
|---|---|---|---|---|---|---|---|---|---|---|
| Address : 000004H | P47 | P46 | P45 | P44 | P43 | P42 | P41 | P40 | 1XXXXXXXB | R/W* |

**• Port 5 data register (PDR5)**

| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value | Access |
|---|---|---|---|---|---|---|---|---|---|---|
| Address : 000005H | P57 | P56 | P55 | P54 | P53 | P52 | P51 | P50 | XXXXXXXXB | R/W* |

**• Port 6 data register (PDR6)**

| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value | Access |
|---|---|---|---|---|---|---|---|---|---|---|
| Address : 000006H | P67 | P66 | P65 | P64 | P63 | P62 | P61 | P60 | XXXXXXXXB | R/W* |

**• Port 7 data register (PDR7)**

| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value | Access |
|---|---|---|---|---|---|---|---|---|---|---|
| Address : 000007H | — | — | — | P74 | P73 | P72 | P71 | P70 | - - - XX111B | R/W* |

**• Port 8 data register (PDR8)**

| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value | Access |
|---|---|---|---|---|---|---|---|---|---|---|
| Address : 000008H | — | P86 | P85 | P84 | P83 | P82 | P81 | P80 | - XXXXXXXB | R/W* |

**• Port 9 data register (PDR9)**

| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value | Access |
|---|---|---|---|---|---|---|---|---|---|---|
| Address : 000009H | P97 | P96 | P95 | P94 | P93 | P92 | P91 | P90 | XXXXXXXXB | R/W* |

**• Port A data register (PDRA)**

| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value | Access |
|---|---|---|---|---|---|---|---|---|---|---|
| Address : 00000AH | — | — | — | — | — | PA2 | PA1 | PA0 | - - - - - XXXB | R/W* |

R/W : Readable and writable
— : Unused
X : Indeterminate

* : The operation of reading or writing to I/O ports is slightly different from reading or writing to memory, as follows.

- Input mode
  Read: Reads the corresponding pin level.
  Write: Writes to the output latch.
- Output mode
  Read: Reads the value of the data register latch.
  Write: The value is output from the corresponding pin.

## (3) Port Direction Registers

**• Port 0 direction register (DDR0)**

| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value | Access |
|---|---|---|---|---|---|---|---|---|---|---|
| Address : 000010H | D07 | D06 | D05 | D04 | D03 | D02 | D01 | D00 | 00000000B | R/W* |

**• Port 1 direction register (DDR1)**

| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value | Access |
|---|---|---|---|---|---|---|---|---|---|---|
| Address : 000011H | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | 00000000B | R/W* |

**• Port 2 direction register (DDR2)**

| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value | Access |
|---|---|---|---|---|---|---|---|---|---|---|
| Address : 000012H | D27 | D26 | D25 | D24 | D23 | D22 | D21 | D20 | 00000000B | R/W* |

**• Port 3 direction register (DDR3)**

| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value | Access |
|---|---|---|---|---|---|---|---|---|---|---|
| Address : 000013H | D37 | D36 | D35 | D34 | D33 | D32 | D31 | D30 | 00000000B | R/W* |

**• Port 4 direction register (DDR4)**

| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value | Access |
|---|---|---|---|---|---|---|---|---|---|---|
| Address : 000014H | — | D46 | D45 | D44 | D43 | D42 | D41 | D40 | -0000000B | R/W* |

**• Port 5 direction register (DDR5)**

| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value | Access |
|---|---|---|---|---|---|---|---|---|---|---|
| Address : 000015H | D57 | D56 | D55 | D54 | D53 | D52 | D51 | D50 | 00000000B | R/W* |

**• Port 6 direction register (DDR6)**

| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value | Access |
|---|---|---|---|---|---|---|---|---|---|---|
| Address : 000016H | D67 | D66 | D65 | D64 | D63 | D62 | D61 | D60 | 00000000B | R/W* |

**• Port 7 direction register (DDR7)**

| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value | Access |
|---|---|---|---|---|---|---|---|---|---|---|
| Address : 000017H | — | — | — | D74 | D73 | — | — | — | ---00---B | R/W* |

**• Port 8 direction register (DDR8)**

| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value | Access |
|---|---|---|---|---|---|---|---|---|---|---|
| Address : 000018H | — | D86 | D85 | D84 | D83 | D82 | D81 | D80 | -0000000B | R/W* |

**• Port 9 direction register (DDR9)**

| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value | Access |
|---|---|---|---|---|---|---|---|---|---|---|
| Address : 000019H | D97 | D96 | D95 | D94 | D93 | D92 | D91 | D90 | 00000000B | R/W* |

**• Port A direction register (DDRA)**

| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value | Access |
|---|---|---|---|---|---|---|---|---|---|---|
| Address : 00001AH | — | — | — | — | — | DA2 | DA1 | DA0 | -----000B | R/W* |

R/W : Readable and writable
— : Unused

*(Continued)*

*(Continued)*

* : The operation of reading or writing to I/O ports is slightly different from reading or writing to memory, as follows.

- Input mode
  Read: Reads the corresponding pin level.
  Write: Writes to the output latch.
- Output mode
  Read: Reads the value of the data register latch.
  Write: The value is output from the corresponding pin.

When pins are used as ports, the register bits control the corresponding pins as follows.

0: Input mode
1: Output mode
Bits are set to “0” by a reset.

- P47, P70 to P72
  No DDR for this port. Data is always available in this port, so when using P70 and P71 as $I^2C$ pin, set PDR value to “1”. (Otherwise when using P70 and P71 by themselves, turn off the $I^2C$.)

  As this port is open-drain output style, so when using this port as an input port, in order to turn off the output transistor, set the output data resister value to “1” and add the pull up resister to the external pin.

### (4) Port Resistance Registers

- **Register configuration**

**• Port 0 resistance register (RDR0)**

| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value | Access |
|---|---|---|---|---|---|---|---|---|---|---|
| Address : 00001C$_H$ | RD07 | RD06 | RD05 | RD04 | RD03 | RD02 | RD01 | RD00 | 00000000$_B$ | R/W |

**• Port 1 resistance register (RDR1)**

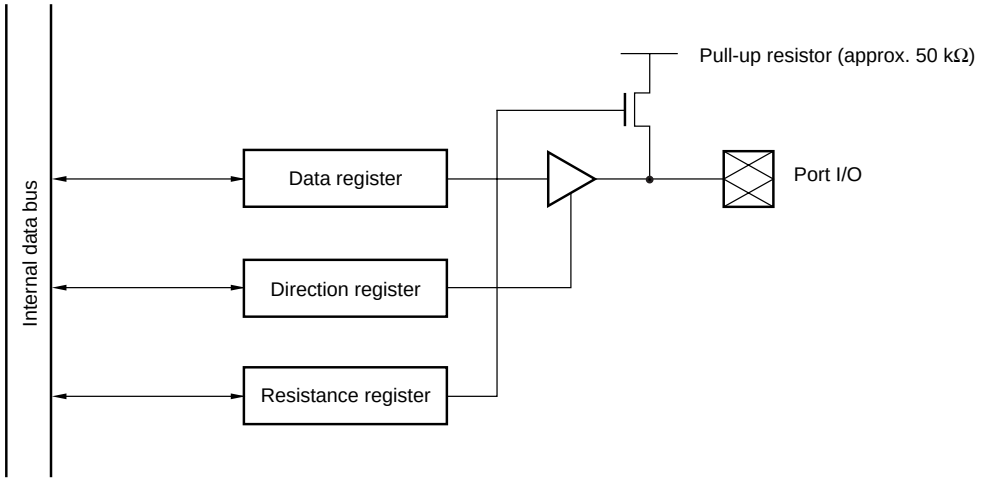
| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value | Access |
|---|---|---|---|---|---|---|---|---|---|---|
| Address : 00001D$_H$ | RD17 | RD16 | RD15 | RD14 | RD13 | RD12 | RD11 | RD10 | 00000000$_B$ | R/W |

**• Port 6 resistance register (RDR6)**

| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value | Access |
|---|---|---|---|---|---|---|---|---|---|---|
| Address : 00001E$_H$ | RD67 | RD66 | RD65 | RD64 | RD63 | RD62 | RD61 | RD60 | 00000000$_B$ | R/W |

R/W : Readable and writable

- **Block diagram**




Notes :
- Input resistance register R/W
  Controls the pull-up resistor in input mode.
  0: Pull-up resistor disconnected in input mode.
  1: Pull-up resistor connected in input mode.
  The setting has no meaning in output mode (pull-up resistor disconnected).
  The direction register (DDR) sets input or output mode.
- The pull-up resistor is disconnected in hardware standby or stop mode (SPL = 1) (high impedance).
- This function is disabled when using an external bus mode. In this case, do not write to this register.

### (5) Port Pin Register

- **Register configuration**

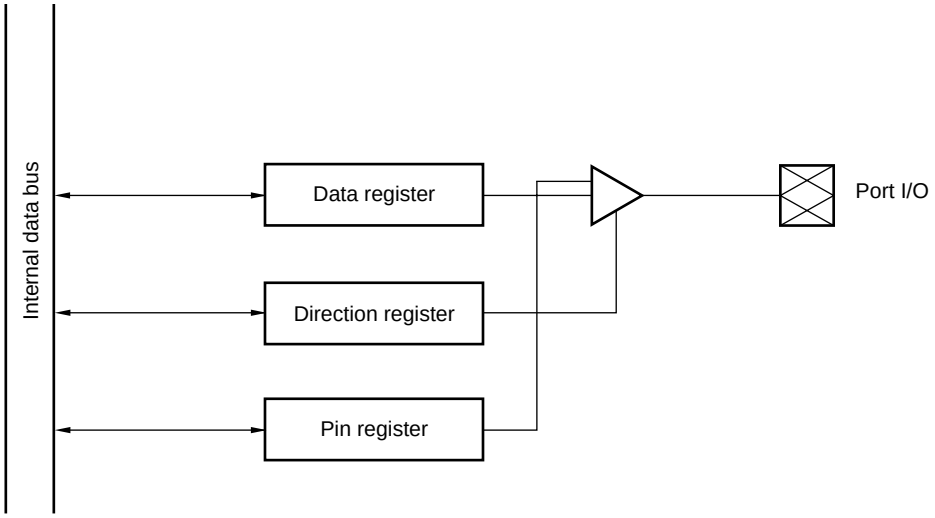
**• Port 4 pin register (ODR4)**

Address : 00001B$_H$

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value | Access |
|---|---|---|---|---|---|---|---|---|---|
| — | OD46 | OD45 | OD44 | OD43 | OD42 | OD41 | OD40 | -0000000$_B$ | R/W |

R/W : Readable and writable
— : Unused

- **Block diagram**




Notes: • Pin register R/W
Performs open-drain control in output mode.
0: Operate as a standard output port in output mode.
1: Operate as an open-drain output port in output mode.
The setting has no meaning in input mode (output Hi-z).
• The direction register (DDR) sets input or output mode.
• This function is disabled when using an external bus mode. In this case, do not write to this register.

### (6) Analog Input Enable Register

- **Register configuration**

**• Analog input enable register (ADER)**

Address : 00001F$_H$

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value | Access |
|---|---|---|---|---|---|---|---|---|---|
| ADE7 | ADE6 | ADE5 | ADE4 | ADE3 | ADE2 | ADE1 | ADE0 | 11111111$_B$ | R/W |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | | |

R/W : Readable and writable

Controls each port 5 pin as follows.
0: Port input mode
1: Analog input mode
Set to “1” by a reset.

## 2. UART

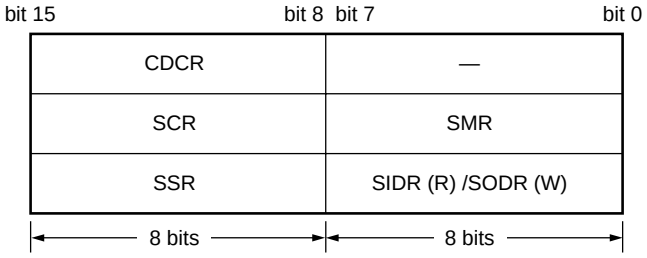
The UART is a serial I/O port that can be used for CLK asynchronous (start-stop synchronization) or CLK synchronous communications. The UART has the following features.

- Full duplex, double buffered
- Supports asynchronous (start-stop synchronization) and CLK synchronous data transfer
- Supports multi-processor mode
- Built-in dedicated baud rate generator

  Asynchronous: 9615 bps, 31250 bps, 4808 bps, 2404 bps and 1202 bps
  CLK synchronous : 1 Mbps, 500 Kbps, 250 Kbps, 125 Kbps and 62.5 Kbps
  } For a 6, 8, 10 or 12 MHz clock.

- Supports flexible baud rate setting using an external clock
- Error detect function (parity, framing, and overrun)
- NRZ type transmission signal
- Intelligent I/O service support

### (1) Register Configuration




**• Serial mode register 0 (SMR0)**

| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|
| Address : 000020H | MD1 | MD0 | CS2 | CS1 | CS0 | Reserved | SCKE | SOE | 00000000B |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

**• Serial control register 0 (SCR0)**

| | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | Initial value |
|---|---|---|---|---|---|---|---|---|---|
| Address : 000021H | PEN | P | SBL | CL | A/D | REC | RXE | TXE | 00000100B |
| | R/W | R/W | R/W | R/W | R/W | W | R/W | R/W | |

**• Serial input register/serial output register 0 (SIDR/SODR0)**

| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|
| Address : 000022H | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | XXXXXXXXB |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

**• Serial status register 0 (SSR0)**

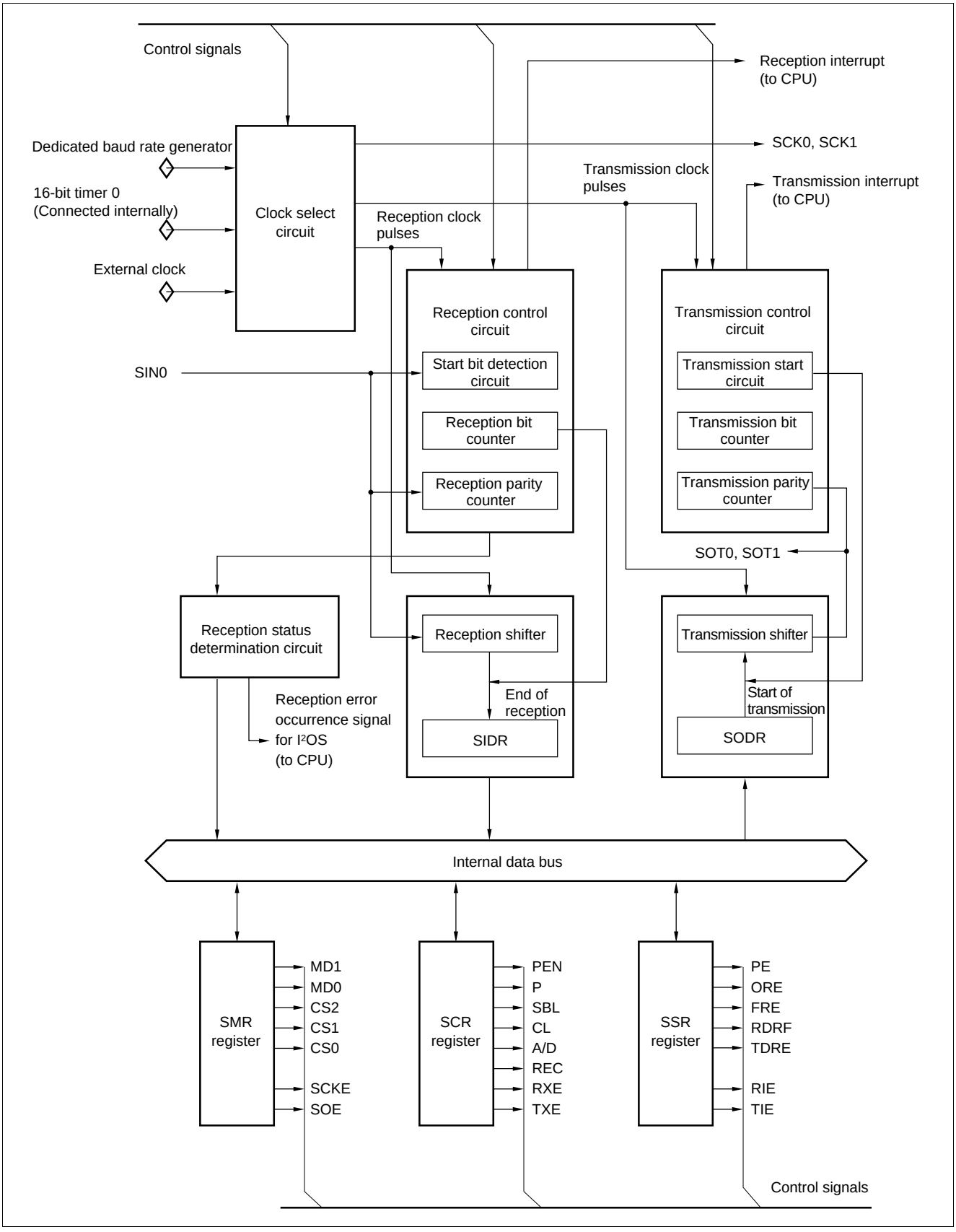
| | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | Initial value |
|---|---|---|---|---|---|---|---|---|---|
| Address : 000023H | PE | ORE | FRE | RDRF | TDRE | — | RIE | TIE | 00001-00B |
| | R | R | R | R | R | — | R/W | R/W | |

**• Clock division control register (CDCR)**

| | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | Initial value |
|---|---|---|---|---|---|---|---|---|---|
| Address : 000027H | MD | — | — | — | DIV3 | DIV2 | DIV1 | DIV0 | 0---1111B |
| | R/W | — | — | — | R/W | R/W | R/W | R/W | |

R/W : Readable and writable
R : Read only
W : Write only
— : Unused
X : Indeterminate

### (2) Block Diagram



## 3. I/O Extended Serial Interface

I/O extended serial interface consists of an 8-bit serial I/O interface that can perform clock synchronous data transfer. Either LSB-first or MSB-first data transfer can be selected.

The following two serial I/O operation modes are available.

- Internal shift clock mode: Data transfer is synchronized with the internal clock.
- External shift clock mode: Data transfer is synchronized with the clock input from the external pin (SCK). By manipulating the general-purpose port that shares the external pin (SCK), this mode also enables the data transfer operation to be driven by CPU instructions.

### (1) Register Details

**• Serial mode control status register 0, 1 (SMCS0, SMCS1)**

| | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | Initial value |
|---|---|---|---|---|---|---|---|---|---|
| Address : 000025H 000029H | SMD2 | SMD1 | SMD0 | SIE | SIR | BUSY | STOP | STRT | 00000010B |
| | R/W | R/W | R/W | R/W | R/W*1 | R | R/W | R/W*2 | |

| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|
| Address : 000024H 000028H | — | — | — | — | MODE | BDS | SOE | SCOE | ----0000B |
| | — | — | — | — | R/W | R/W | R/W | R/W | |

**• Serial data register 0, 1 (SDR0, SDR1)**

| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|
| Address : 000026H 00002AH | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | XXXXXXXXB |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

R/W : Readable and writable
R : Read only
— : Unused
X : Indeterminate

*1: Only “0” can be written.

*2: Only “1” can be written. Reading always returns “0”.

This register controls the transfer operation mode of the serial I/O. The following describes the function of each bit.

**bit 3: Serial mode selection bit (MODE)**

This bit selects the conditions for starting operation from the halted state. Changing the mode during operation is prohibited

| MODE | Operation |
|---|---|
| 0 | Start when STRT is set to “1”. [Initial value] |
| 1 | Start on reading from or writing to the serial data register. |

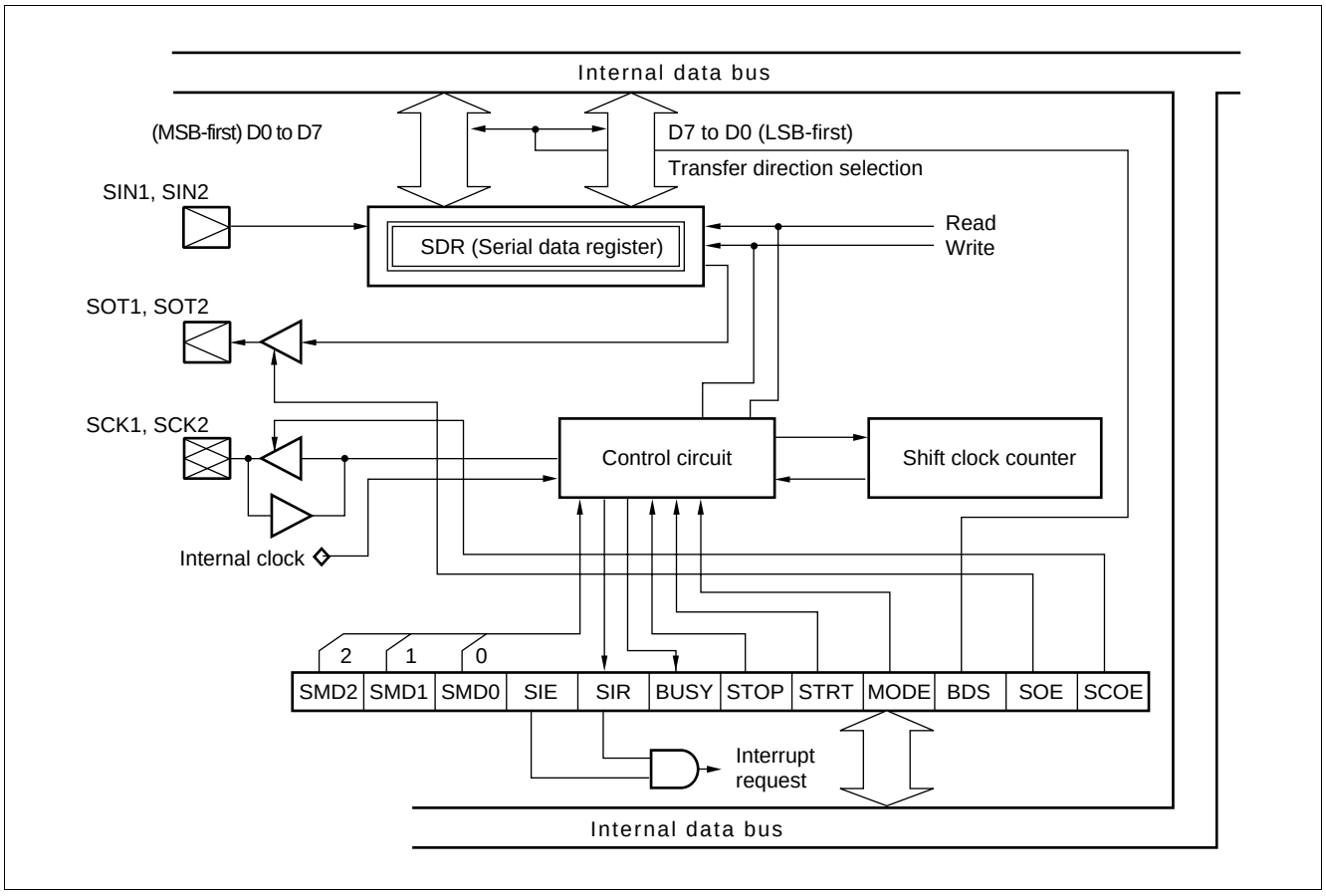
The bit is initialized to “0” by a reset. The bit is readable and writable. Set to “1” when using the intelligent I/O

**bit 2: Transfer direction selection bit (BDS: Bit Direction Select)**

Selects as follows at the time of serial data input and output whether the data are to be transferred in the order from LSB to MSB or vice versa.

| MODE | Operation |
|---|---|
| 0 | LSB-first [Initial value] |
| 1 | MSB-first |

**(2) Block Diagram**

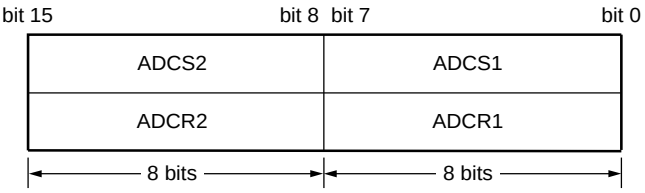


## 4. A/D Converter

The A/D converter converts analog input voltages to digital values. The A/D converter has the following features.

- Conversion time: Minimum of 8.167 µs per channel (for a 12 MHz machine clock)
- Uses RC-type successive approximation conversion with a sample and hold circuit.
- 10-bit resolution
- Eight program-selectable analog input channels
  - Single conversion mode: Selectively convert a one channel.
  - Scan conversion mode: Continuously convert multiple channels. Maximum of 8 program-selectable channels.
  - Continuous conversion mode: Repeatedly convert specified channels.
  - Stop conversion mode: Convert one channel then halt until the next activation. (Enables synchronization of the conversion start timing.)
- An A/D conversion completion interrupt request to the CPU can be generated on the completion of A/D conversion. This interrupt can activate I²OS to transfer the result of A/D conversion to memory and is suitable for continuous operation.
- Activation by software, external trigger (falling edge), or timer (rising edge) can be selected.

### (1) Register Configuration




**• Control status register 1 (ADCS1)**

| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|
| Address : 000036H | MD1 | MD0 | ANS2 | ANS1 | ANS0 | ANE2 | ANE1 | ANE0 | 00000000B |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

**• Control status register 2 (ADCS2)**

| | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | Initial value |
|---|---|---|---|---|---|---|---|---|---|
| Address : 000037H | BUSY | INT | INTE | PAUS | STS1 | STS0 | STRT | DA | 00000000B |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

**• Data register 1 (ADCR1)**

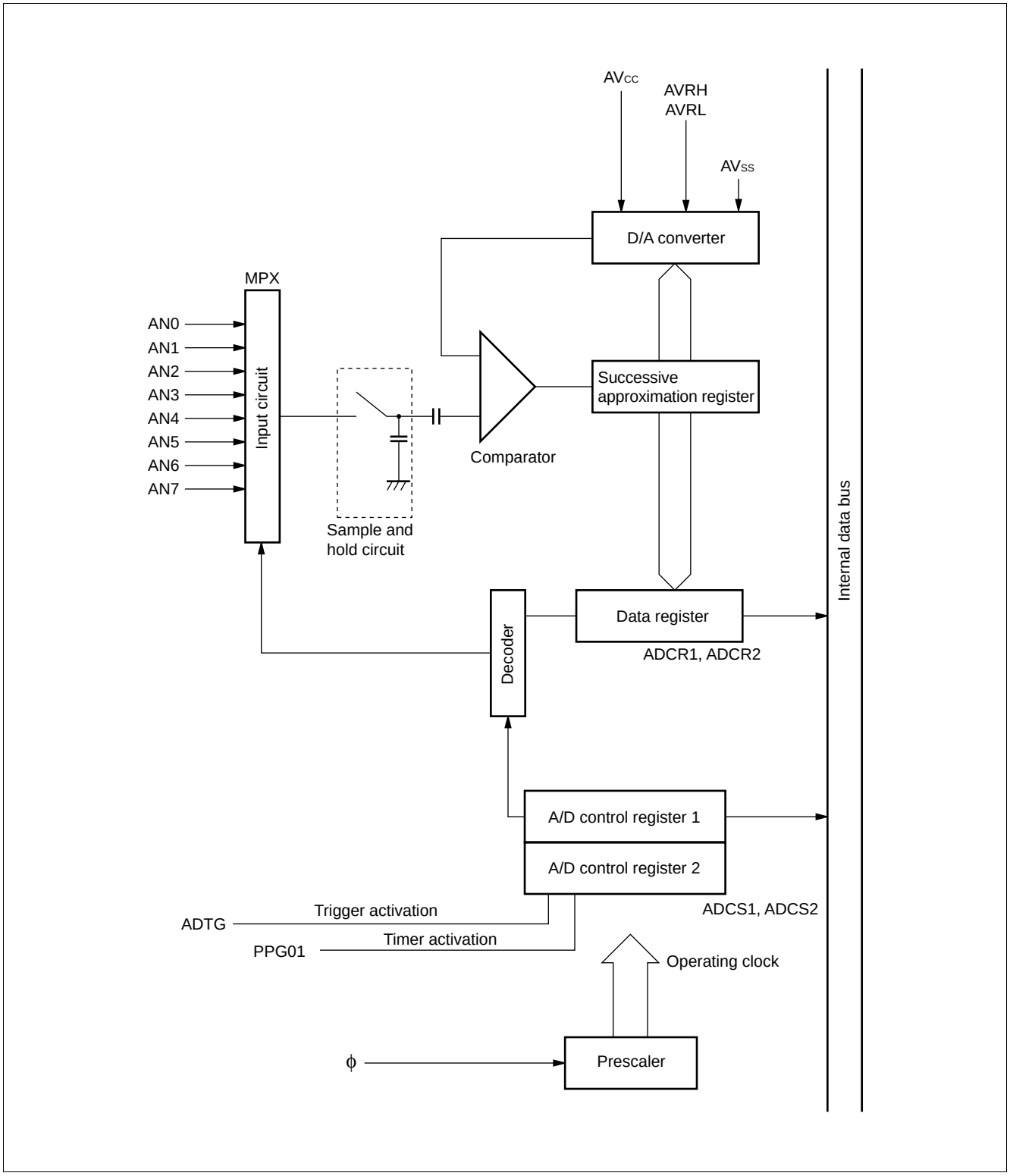
| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|
| Address : 000038H | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | XXXXXXXXB |
| | R | R | R | R | R | R | R | R | |

**• Data register 2 (ADCR2)**

| | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | Initial value |
|---|---|---|---|---|---|---|---|---|---|
| Address : 000039H | — | — | — | — | — | — | 9 | 8 | XXXXXXXXB |
| | R | R | R | R | R | R | R | R | |

R/W : Readable and writable
R : Read only
X : Indeterminate

**(2) Block Diagram**



## 5. D/A Converter

D/A converter is an R-2R type D/A converter with 8-bit resolution. The device contains two D/A converters. The D/A control register controls the output of the two D/A converters independently.

### (1) Register Configuration

**• D/A converter data register 0 (DAT0)**

| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|
| Address : 00003A$_H$ | DA07 | DA06 | DA05 | DA04 | DA03 | DA02 | DA01 | DA00 | XXXXXXXX$_B$ |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

**• D/A converter data register 1 (DAT1)**

| | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | Initial value |
|---|---|---|---|---|---|---|---|---|---|
| Address : 00003B$_H$ | DA17 | DA16 | DA15 | DA14 | DA13 | DA12 | DA11 | DA10 | XXXXXXXX$_B$ |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

**• D/A control register channel 0 (DACR0)**

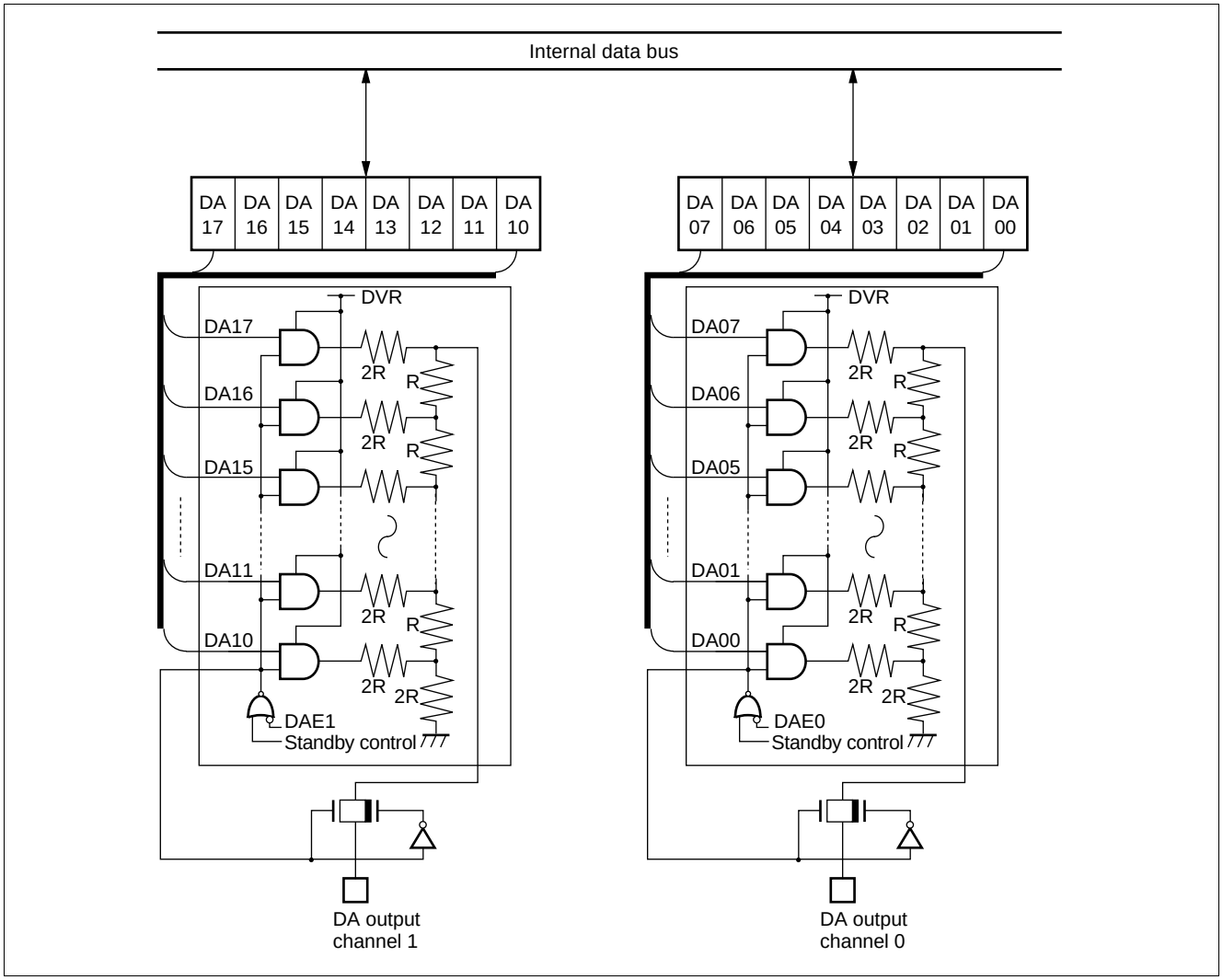
| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|
| Address : 00003C$_H$ | — | — | — | — | — | — | — | DAE0 | -------0$_B$ |
| | — | — | — | — | — | — | — | R/W | |

**• D/A control register channel 1 (DACR1)**

| | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | Initial value |
|---|---|---|---|---|---|---|---|---|---|
| Address : 00003D$_H$ | — | — | — | — | — | — | — | DAE1 | -------0$_B$ |
| | — | — | — | — | — | — | — | R/W | |

R/W : Readable and writable
— : Unused
X : Indeterminate

**(2) Block Diagram**



## 6. 8/16-bit PPG

8/16-bit PPG is an 8-bit reload timer module. The block performs PPG output in which the pulse output is controlled by the operation of the timer.

The hardware consists of two 8-bit down-counters, four 8-bit reload registers, one 16-bit control register, two external pulse output pins, and two interrupt outputs. The PPG has the following functions.

- 8-bit PPG output in two channels independent operation mode: Two independent PPG output channels are available.
- 16-bit PPG output operation mode: One 16-bit PPG output channel is available.
- 8 + 8-bit PPG output operation mode: Variable-period 8-bit PPG output operation is available by using the output of channel 0 as the clock input to channel 1.
- PPG output operation: Outputs pulse waveforms with variable period and duty ratio. Can be used as a D/A converter in conjunction with an external circuit.

### (1) Register Configuration

**• PPG0 operation mode control register channel 0 (PPGC0)**

Address : 000044H

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|
| PEN0 | — | PE00 | PIE0 | PUF0 | — | — | Reserved | 0X000XX1B |
| R/W | — | R/W | R/W | R/W | — | — | — | |

**• PPG1 operation mode control register channel 1 (PPGC1)**

Address : 000045H

| bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | Initial value |
|---|---|---|---|---|---|---|---|---|
| PEN1 | — | PE10 | PIE1 | PUF1 | MD1 | MD0 | Reserved | 0X000001B |
| R/W | — | R/W | R/W | R/W | R/W | R/W | — | |

**• PPG0, PPG1 output control register channel 0, channel 1 (PPGOE)**

Address : 000046H

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|
| PCS2 | PCS1 | PCS0 | PCM2 | PCM1 | PCM0 | PE11 | PE01 | 00000000B |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

**• Reload register upper channel 0, channel 1 (PRLH0, PRLH1)**

Address : 000041H, 000043H

| bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | Initial value |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | XXXXXXXXB |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

**• Reload register lower channel 0, channel 1 (PRLL0, PRLL1)**

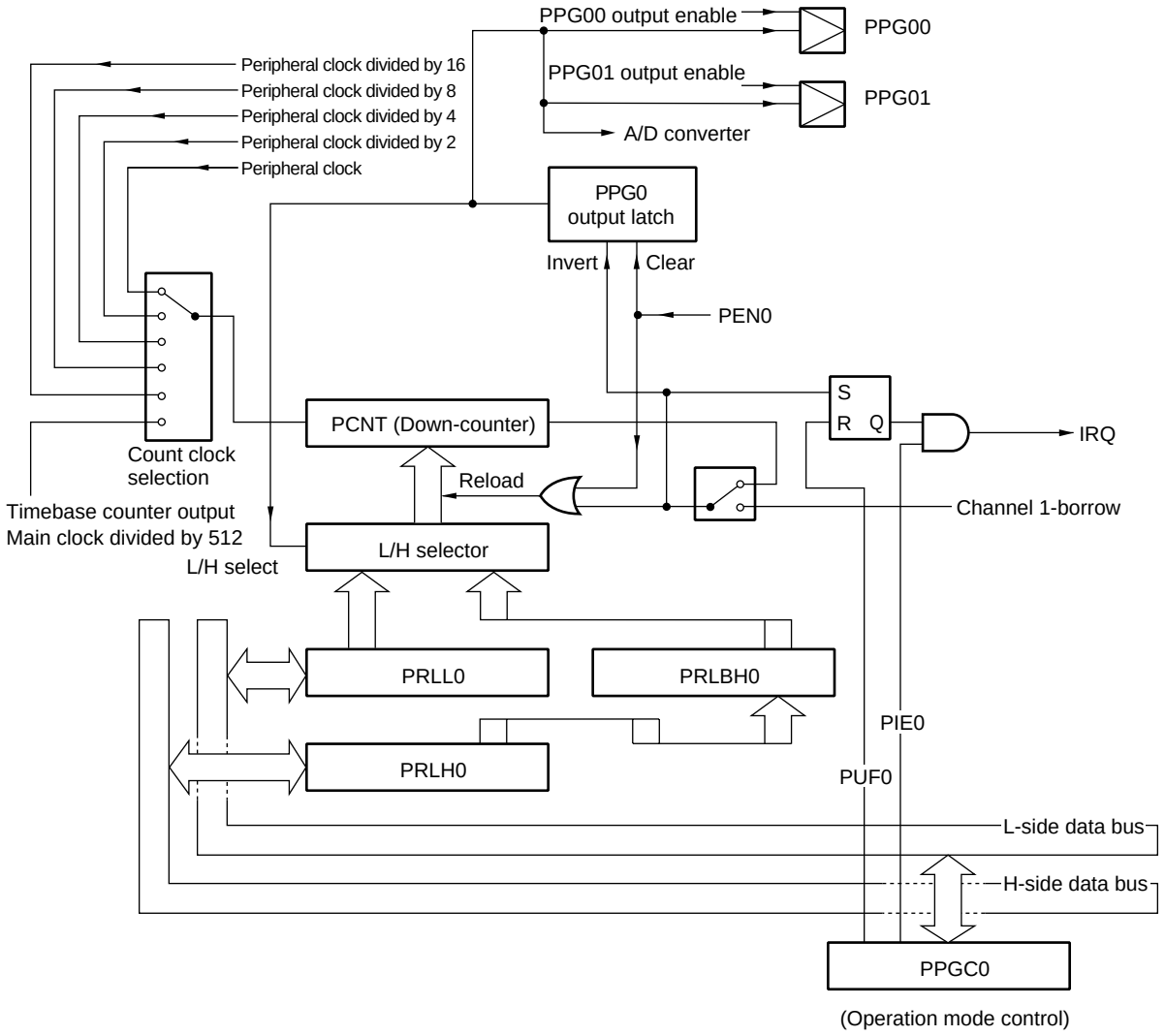
Address : 000040H, 000042H

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | XXXXXXXXB |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

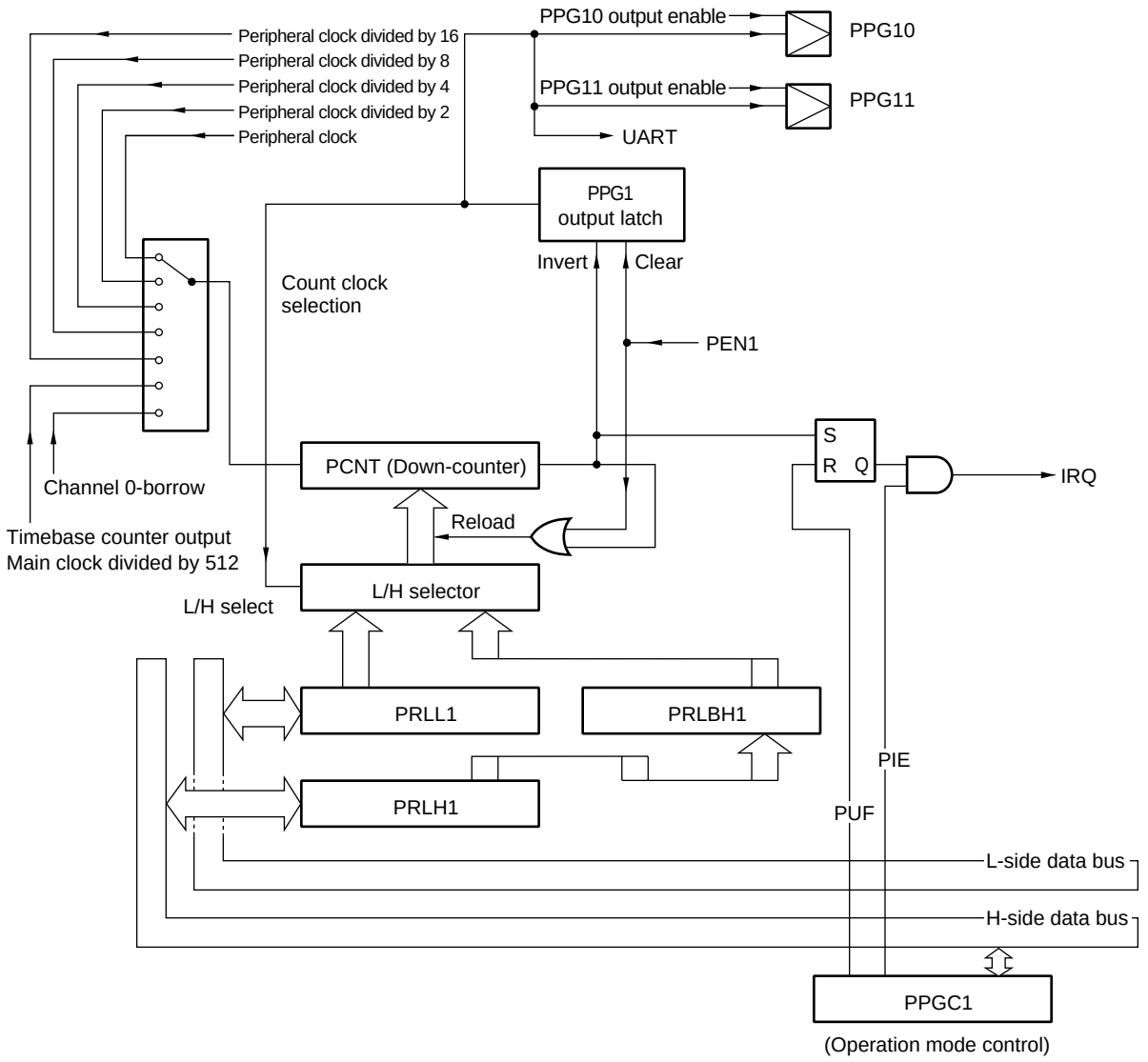
R/W : Readable and writable
X : Indeterminate

### (2) Block Diagram

- **8/16-bit PPG (channel 0)**



- **8/16-bit PPG (channel 1)**



## 7. 8/16-bit Up/Down Counter/Timer

8/16-bit up/down counter/timer is an up/down counter/timer and consists of six event input pins, two 8-bit up/down counters, two 8-bit reload/compare registers, and their control circuits.

### (1) Main Functions

- The 8-bit count register can count in the range 0 to 256 (or 0 to 65535 in 1 × 16-bit operation mode).
- The count clock selection can select between four different count modes.

  Count modes
  - Timer mode
  - Up/down counter mode
  - Phase difference count mode (× 2)
  - Phase difference count mode (× 8)

- Two different internal count clocks are available in timer mode.

  Count clock (at 12 MHz operation)
  - 166 ns (6 MHz: Divide by 2)
  - 0.67 µs (1.5 MHz: Divide by 8)

- In up/down count mode, you can select which edge to detect on the external pin input signal.

  Detected edge
  - Detect falling edges
  - Detect rising edges
  - Detect both rising and falling edges
  - Edge detection disabled

- Phase difference count mode is suitable for motor encoder counting. By inputting the A, B, and Z phase outputs from the encoder, a high-precision rotational angle, speed, or similar count can be implemented simply.
- Two different functions can be selected for the ZIN pin.

  ZIN pin
  - Counter clear function
  - Gate function

- Compare and reload functions are available and can be used either independently or together. A variable-width up/down count can be performed by activating both functions.

  Compare/reload function
  - Compare function (Output an interrupt when a compare occurs.)
  - Compare function (Output an interrupt and clear the counter when a compare occurs.)
  - Reload function (Output an interrupt and reload when an underflow occurs.)
  - Compare/reload function (Output an interrupt and clear the counter when a compare occurs. Output an interrupt and reload when an underflow occurs.)
  - Compare/reload disabled

- Whether or not to generate an interrupt when a compare, reload (underflow), or overflow occurs can be set independently.
- The previous count direction can be determined from the count direction flag.
- An interrupt can be generated when the count direction changes.

## (2) Register Configuration

| bit 15 | bit 8 bit 7 | bit 0 |
|---|---|---|
| UDCR1 | UDCR0 | |
| RCR1 | RCR0 | |
| (Reversed area) | CSR0 | |
| CCRH0 | CCRL0 | |
| (Reversed area) | CSR1 | |
| CCRH1 | CCRL1 | |
| 8 bits | 8 bits | |

**• Up/down count register channel 0 (UDCR0)**

| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|
| Address : 000070H | D07 | D06 | D05 | D04 | D03 | D02 | D01 | D00 | 00000000B |
| | R | R | R | R | R | R | R | R | |

**• Up/down count register channel 1 (UDCR1)**

| | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | Initial value |
|---|---|---|---|---|---|---|---|---|---|
| Address : 000071H | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | 00000000B |
| | R | R | R | R | R | R | R | R | |

**• Reload compare register channel 0 (RCR0)**

| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|
| Address : 000072H | D07 | D06 | D05 | D04 | D03 | D02 | D01 | D00 | 00000000B |
| | W | W | W | W | W | W | W | W | |

**• Reload compare register channel 1 (RCR1)**

| | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | Initial value |
|---|---|---|---|---|---|---|---|---|---|
| Address : 000073H | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | 00000000B |
| | W | W | W | W | W | W | W | W | |

**• Counter status register channel 0, channel 1 (CSR0, CSR1)**

| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|
| Address : 000074H<br>000078H | CSTR | CITE | UDIE | CMPF | OVFF | UDFF | UDF1 | UDF0 | 00000000B |
| | R/W | R/W | R/W | R/W | R/W | R/W | R | R | |

**• Counter control register channel 0, channel 1 (CCRL0, CCRL1)**

| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|
| Address : 000076H<br>00007AH | – | CTUT | UCRE | RLDE | UDCC | CGSC | CGE1 | CGE0 | 00001000B<br>00000000B |
| | – | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

**• Counter control register channel 0 (CCRH0)**

| | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | Initial value |
|---|---|---|---|---|---|---|---|---|---|
| Address : 000077H | M16E | CDCF | CFIE | CLKS | CMS1 | CMS0 | CES1 | CES0 | 00000000B |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

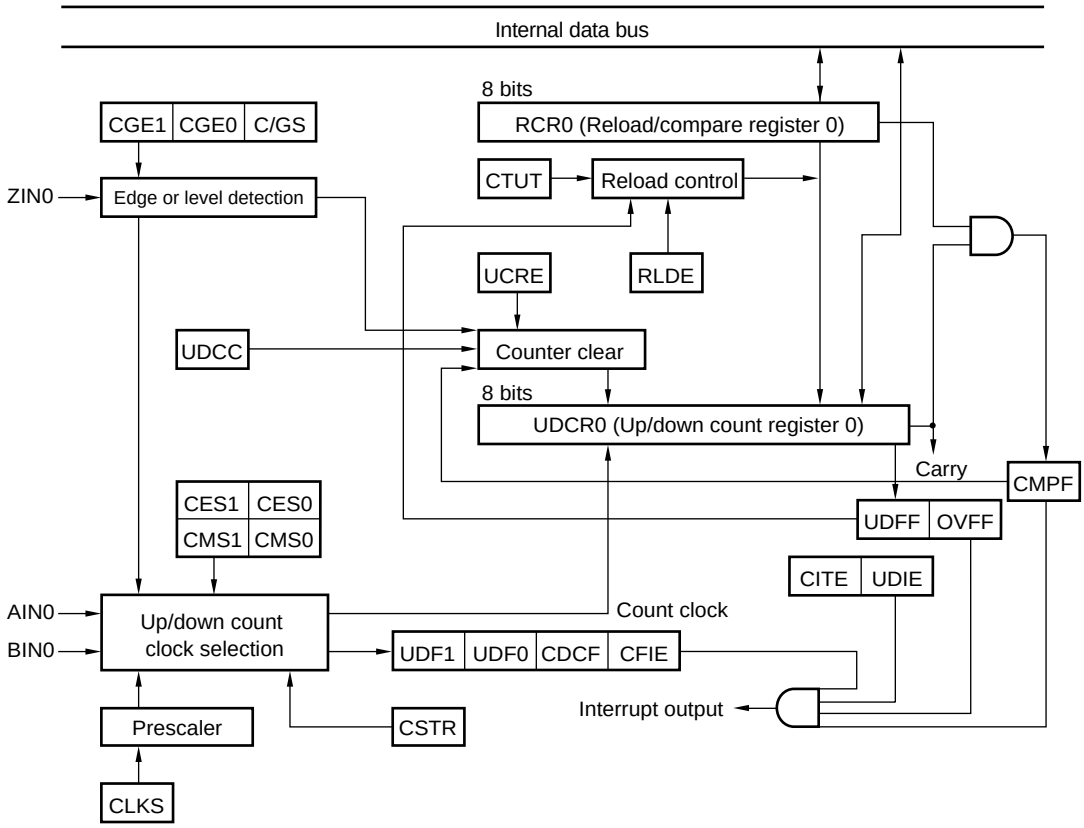
**• Counter control register channel 1 (CCRH1)**

| | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | Initial value |
|---|---|---|---|---|---|---|---|---|---|
| Address : 00007BH | – | CDCF | CFIE | CLKS | CMS1 | CMS0 | CES1 | CES0 | X0001000B |
| | – | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

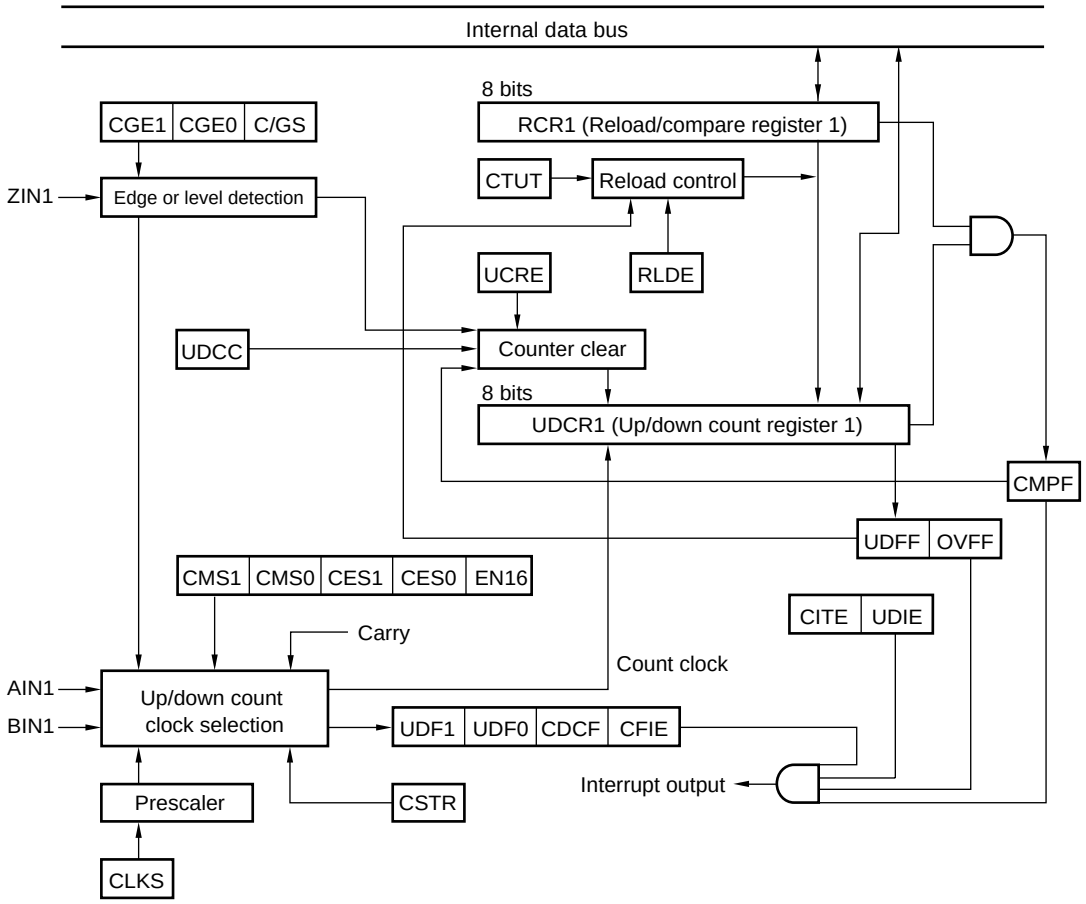
R/W : Readable and writable
R : Read only
W : Write only
– : Unused
X : Indeterminate

### (3) Block Diagram

- **8/16-bit up/down counter/timer (channel 0)**



- **8/16-bit up/down counter/timer (channel 1)**



## 8. Clock Output Control Register

Clock output control register outputs the divided machine clock.

### (1) Register Configuration

• **Clock control register (CLKR)**

| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|
| Address : 00003E$_H$ | — | — | — | — | CKEN | FRQ2 | FRQ1 | FRQ0 | ----0000$_B$ |
| | | | | | R/W | R/W | R/W | R/W | |

R/W : Readable and writable
— : Unused

**bit 3: Clock output enable bit (CKEN)**

| MODE | Operation |
|---|---|
| 0 | Operate as a standard port. |
| 1 | Operate as the clock output. |

**bit 2 to bit 0: Clock output frequency select bit (FRQ2 to FRQ0)**

| FRQ2 | FRQ1 | FRQ0 | Output clock | $\phi$ = 12 MHz | $\phi$ = 8 MHz | $\phi$ = 4 MHz |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | $\phi/2^1$ | 167 ns | 250 ns | 500 ns |
| 0 | 0 | 1 | $\phi/2^2$ | 333 ns | 500 ns | 1 µs |
| 0 | 1 | 0 | $\phi/2^3$ | 667 ns | 1 µs | 2 µs |
| 0 | 1 | 1 | $\phi/2^4$ | 1.33 µs | 2 µs | 4 µs |
| 1 | 0 | 0 | $\phi/2^5$ | 2.67 µs | 4 µs | 8 µs |
| 1 | 0 | 1 | $\phi/2^6$ | 5.33 µs | 8 µs | 16 µs |
| 1 | 1 | 0 | $\phi/2^7$ | 10.67 µs | 16 µs | 32 µs |
| 1 | 1 | 1 | $\phi/2^8$ | 21.33 µs | 32 µs | 64 µs |

## 9. DTP/External Interrupts

The DTP (Data Transfer Peripheral) is a peripheral block that interfaces external peripherals to the F²MC-16L CPU. The DTP receives DMA and interrupt processing requests from external peripherals and passes the requests to the F²MC-16L CPU to activate the intelligent I/O service or interrupt processing. Two request levels ("H" and "L") are provided for the intelligent I/O service. For external interrupt requests, generation of interrupts on a rising or falling edge as well as on "H" and "L" levels can be selected, giving a total of four types.

### (1) Register Configuration

**• Interrupt/DTP enable register (ENIR)**

| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|
| Address : 000030H | EN7 | EN6 | EN5 | EN4 | EN3 | EN2 | EN1 | EN0 | 00000000B |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

**• Interrupt/DTP source register (EIRR)**

| | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | Initial value |
|---|---|---|---|---|---|---|---|---|---|
| Address : 000031H | ER7 | ER6 | ER5 | ER4 | ER3 | ER2 | ER1 | ER0 | 00000000B |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

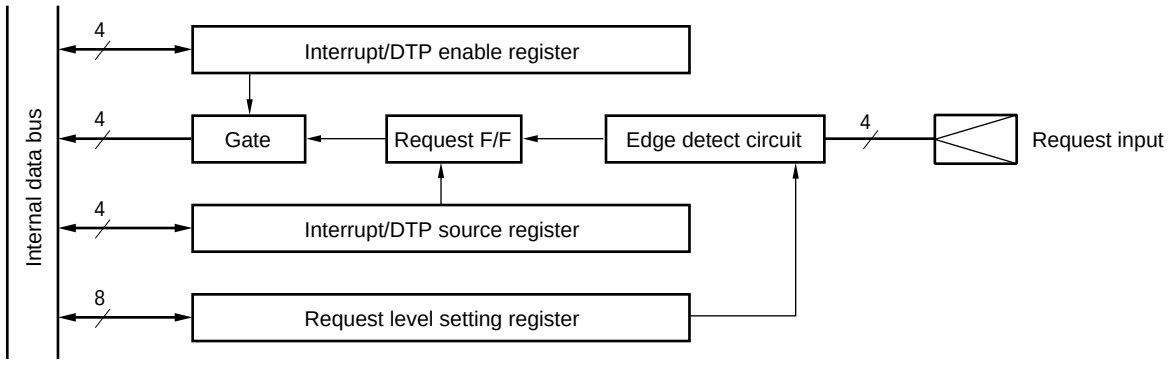
**• Request level setting register (ELVR)**

| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|
| Address : 000032H | LB3 | LA3 | LB2 | LA2 | LB1 | LA1 | LB0 | LA0 | 00000000B |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

| | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | Initial value |
|---|---|---|---|---|---|---|---|---|---|
| Address : 000033H | LB7 | LA7 | LB6 | LA6 | LB5 | LA5 | LB4 | LA4 | 00000000B |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

R/W : Readable and writable

### (2) Block Diagram



## 10. 16-bit I/O Timer

The 16-bit I/O timer consists of one 16-bit free-run timer, two output compare, and two input capture modules.

Based on the 16-bit free-run timer, these functions can be used to generate two independent waveform outputs and to measure input pulse widths and external clock periods.

- **Register configuration**

**• 16-bit free-run timer**

| | | |
|---|---|---|
| TCDTL : 000066H<br>TCDTH : 000067H | bit 15 … bit 0: TCDT | Timer data register lower, upper (TCDTL, TCDTH) |
| TCCS : 000068H | TCCS | Timer control status register (TCCS) |

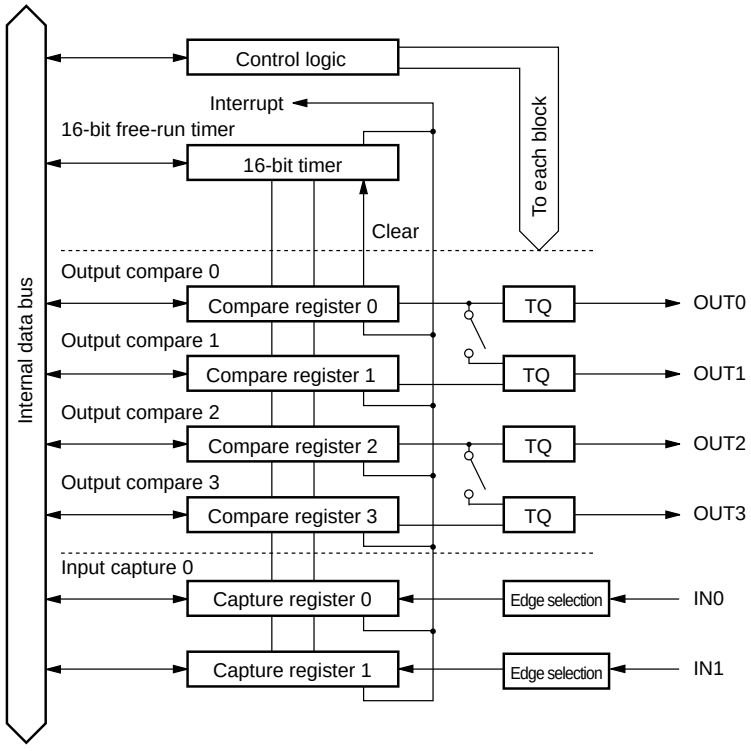
**• 16-bit output compare**

| | | |
|---|---|---|
| OCCP0 : 000050H, 51H<br>OCCP1 : 000052H, 53H<br>OCCP2 : 000054H, 55H<br>OCCP3 : 000056H, 57H | bit 15 … bit 0: OCCP | Compare register channel 0 to channel 3 lower, upper (OCCP0 to OCCP3) |
| OCS0 : 000058H<br>OCS1 : 000059H<br>OCS2 : 00005AH<br>OCS3 : 00005BH | OCS | Compare control status register channel 0 to channel 3 (OCS0 to OCS3) |

**• 16-bit input capture**

| | | |
|---|---|---|
| IPCP0 : 000060H, 61H<br>IPCP1 : 000062H, 63H | bit 15 … bit 0: IPCP | Input capture register channel 0, channel 1 lower, upper (IPCP0, IPCP1) |
| ICS0, 1 : 000064H | ICS | Input capture control status register (ICS0, 1) |

- **Block diagram**



### (1) 16-bit Free-run Timer

The 16-bit free-run timer consists of a 16-bit up-counter, a control register, and a prescaler. The output of the timer/counter is used as the base time for the input capture and output compare.

- The operating clock for the counter can be selected from four different clocks.
  Four internal clocks (ϕ/4, ϕ/16, ϕ/32, ϕ/64)
- Interrupts can be generated when a counter value overflow or compare match with compare register 0 occurs (the appropriate mode must be set for a compare match).
- The counter can be initialized to $0000_H$ by a reset, software clear, or compare match with compare register 0.

- **Register details**

**• Upper timer data register (TCDTH)**

Address : $000067_H$

| bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | Initial value |
|---|---|---|---|---|---|---|---|---|
| T15 | T14 | T13 | T12 | T11 | T10 | T09 | T08 | $00000000_B$ |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

**• Lower timer data register (TCDTL)**

Address : $000066_H$

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|
| T07 | T06 | T05 | T04 | T03 | T02 | T01 | T00 | $00000000_B$ |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

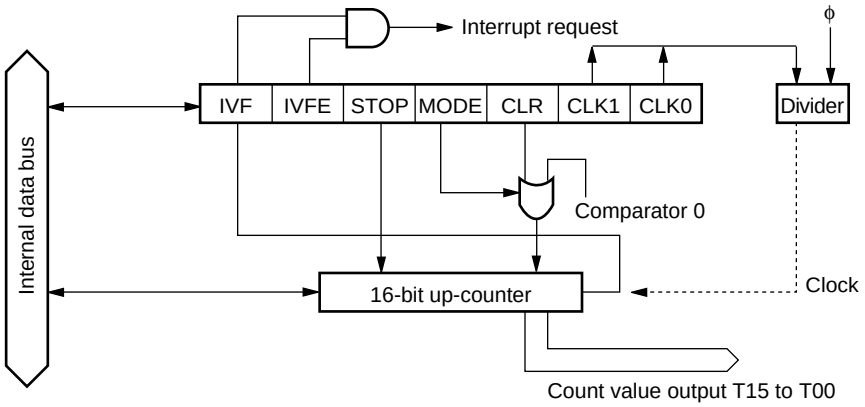
R/W : Readable and writable

The count value of the 16-bit free-run timer can be read from this register. The count is cleared to "$0000_B$" by a reset. Writing to this register sets the timer value. However, only write to the register when the timer is halted (STOP = "1"). Always use word access.

The 16-bit free-run timer is initialized by the following.

- Reset
- The clear bit (CLR) of the control status register
- A match between the timer/counter value and compare register 0 of the output compare (if the appropriate mode is set)

- **Block diagram**



### (2) Output Compare

The output compare consists of two 16-bit compare registers, compare output latches, and control registers. The modules can invert the output level and generate an interrupt when the 16-bit free-run timer value matches the compare register value.

- The four compare registers can be operated independently.
  Each compare register has a corresponding output pin and interrupt flag.
- The four compare registers can be paired to control the output pins.
  Invert the output pins using the four compare registers.
- Initial values can be set for the output pins.
- An interrupt can be generated when a compare match occurs.

- **Register configuration**

**• Upper compare register channel 0 to channel 3 (OCCP0 to OCCP3)**

OCCP0 : 000051H
OCCP1 : 000053H
OCCP2 : 000055H
OCCP3 : 000057H

| bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | Initial value |
|---|---|---|---|---|---|---|---|---|
| C15 | C14 | C13 | C12 | C11 | C10 | C09 | C08 | XXXXXXXXB |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

**• Lower compare register channel 0 to channel 3 (OCCP0 to OCCP3)**

OCCP0 : 000050H
OCCP1 : 000052H
OCCP2 : 000054H
OCCP3 : 000056H

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|
| C07 | C06 | C05 | C04 | C03 | C02 | C01 | C00 | XXXXXXXXB |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

**• Compare control status register channel 0 to channel 3 (OCS0 to OCS3)**

OCS1 : 000059H
OCS3 : 00005BH

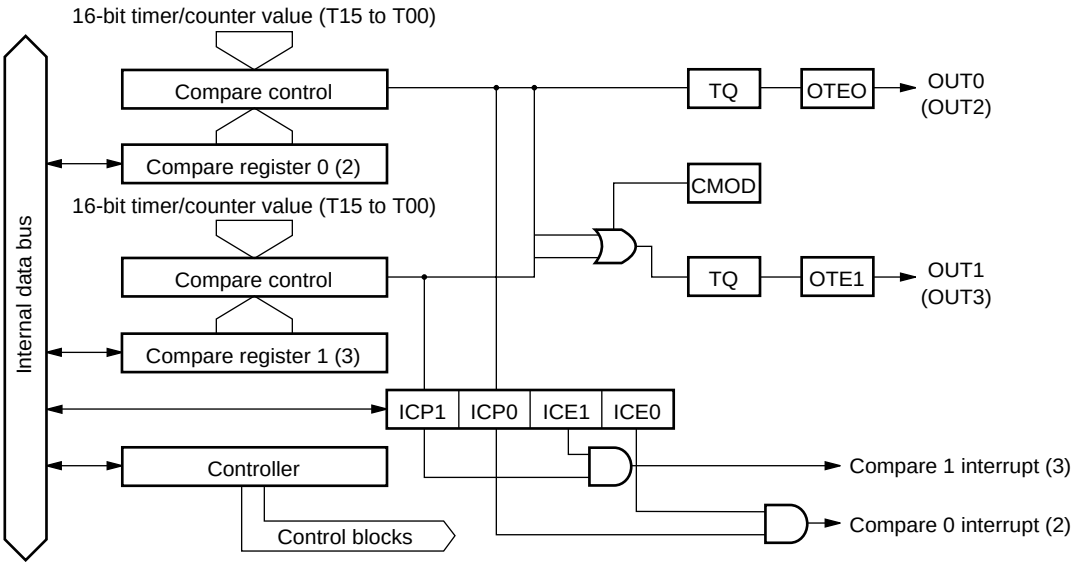
| bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | Initial value |
|---|---|---|---|---|---|---|---|---|
| — | — | — | CMOD | OTE1 | OTE0 | OTDI | OTD0 | ---00000B |
| — | — | — | R/W | R/W | R/W | R/W | R/W | |

OCS0 : 000058H
OCS2 : 00005AH

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|
| ICP1 | ICP0 | ICE1 | ICE0 | — | — | CST1 | CST0 | 0000--00B |
| R/W | R/W | R/W | R/W | — | — | R/W | R/W | |

R/W : Readable and writable
— : Unused
X : Indeterminate

- **Block diagram**



### (3) Input Capture

The input capture consists of two independent external input pins, their corresponding capture registers, and a control register. The value of the 16-bit free-run timer can be stored in the capture register and an interrupt generated when the specified edge is detected on the signal from the external input pin.

- The edge to detect on the external input signal is selectable.
  Detection of rising edges, falling edges, or either edge can be specified.
- The two input capture channels can operate independently.
- An interrupt can be generated on detection of the specified edge on the external input signal.

The input capture interrupt can activate the intelligent I/O service.

- **Register details**

**• Input capture register channel 0, channel 1 (IPCP0, IPCP1)**

| | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | Initial value |
|---|---|---|---|---|---|---|---|---|---|
| IPCP0 : $000061_H$<br>IPCP1 : $000063_H$ | CP15 | CP14 | CP13 | CP12 | CP11 | CP10 | CP09 | CP08 | $XXXXXXXX_B$ |
| | R | R | R | R | R | R | R | R | |

| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|
| IPCP0 : $000060_H$<br>IPCP1 : $000062_H$ | CP07 | CP06 | CP05 | CP04 | CP03 | CP02 | CP01 | CP00 | $XXXXXXXX_B$ |
| | R | R | R | R | R | R | R | R | |

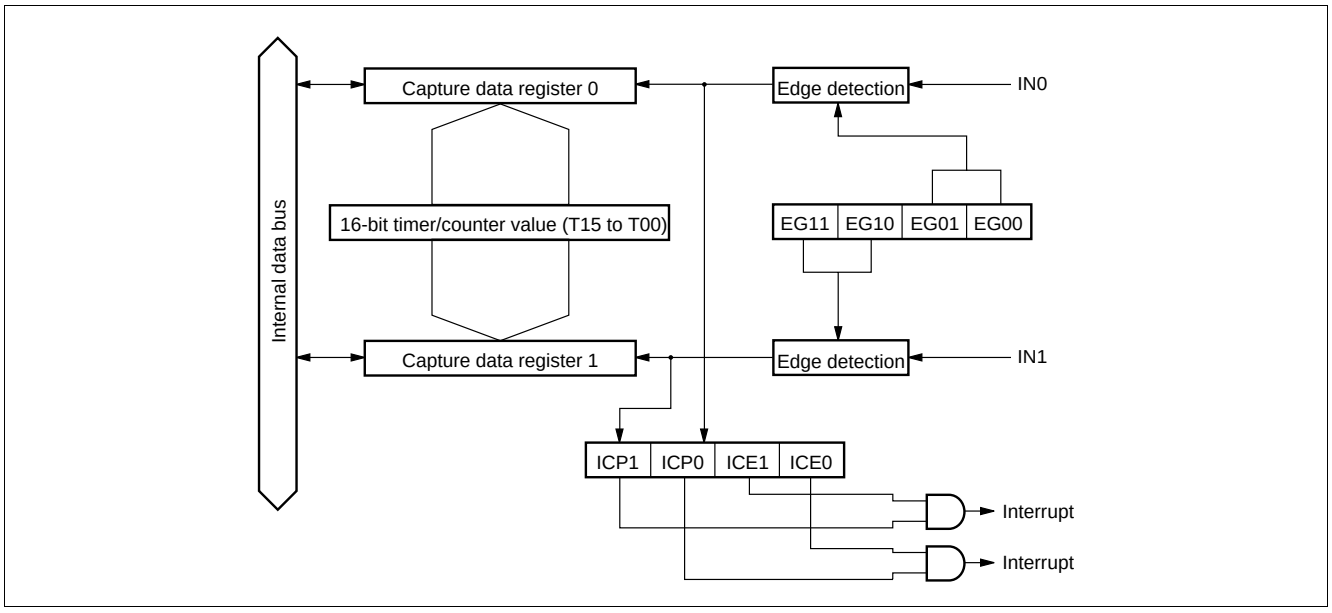
**• Input capture control status register (ICS0, 1)**

| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|
| $000064_H$ | ICP1 | ICP0 | ICE1 | ICE0 | EG11 | EG10 | EG01 | EG00 | $00000000_B$ |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

R/W : Readable and writable
R : Read only
X : Indeterminate

The 16-bit free-run timer value is stored in these registers when the specified edge is detected on the input waveform from the corresponding external pin. (Always use word access. Writing is prohibited.)

- **Block diagram**



## 11. Watchdog Timer, Timebase Timer, and Watch Timer

The watchdog timer consists of a 2-bit watchdog counter that uses the carry signal from the 18-bit timebase timer or the 15-bit watch timer as a clock source, a control register, and a watchdog reset controller.

The timebase timer consists of an 18-bit timer and a circuit that controls interval interrupts. Note that the timebase timer uses the main clock, regardless of the setting of the MCS bit and SCS bit in CKSCR.

The watch timer consists of a 15-bit timer and a circuit that controls interval interrupts. Note that the watch timer uses the sub clock, regardless of the setting of the MCS bit SCS bit in CKSCR.

### (1) Register Configuration

**• Watchdog timer control register (WDTC)**

| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|
| Address : 0000A8H | PONR | — | WRST | ERST | SRST | WTE | WT1 | WT0 | XXXXX111B |
| | R | — | R | R | R | W | W | W | |

**• Timebase timer control register (TBTC)**

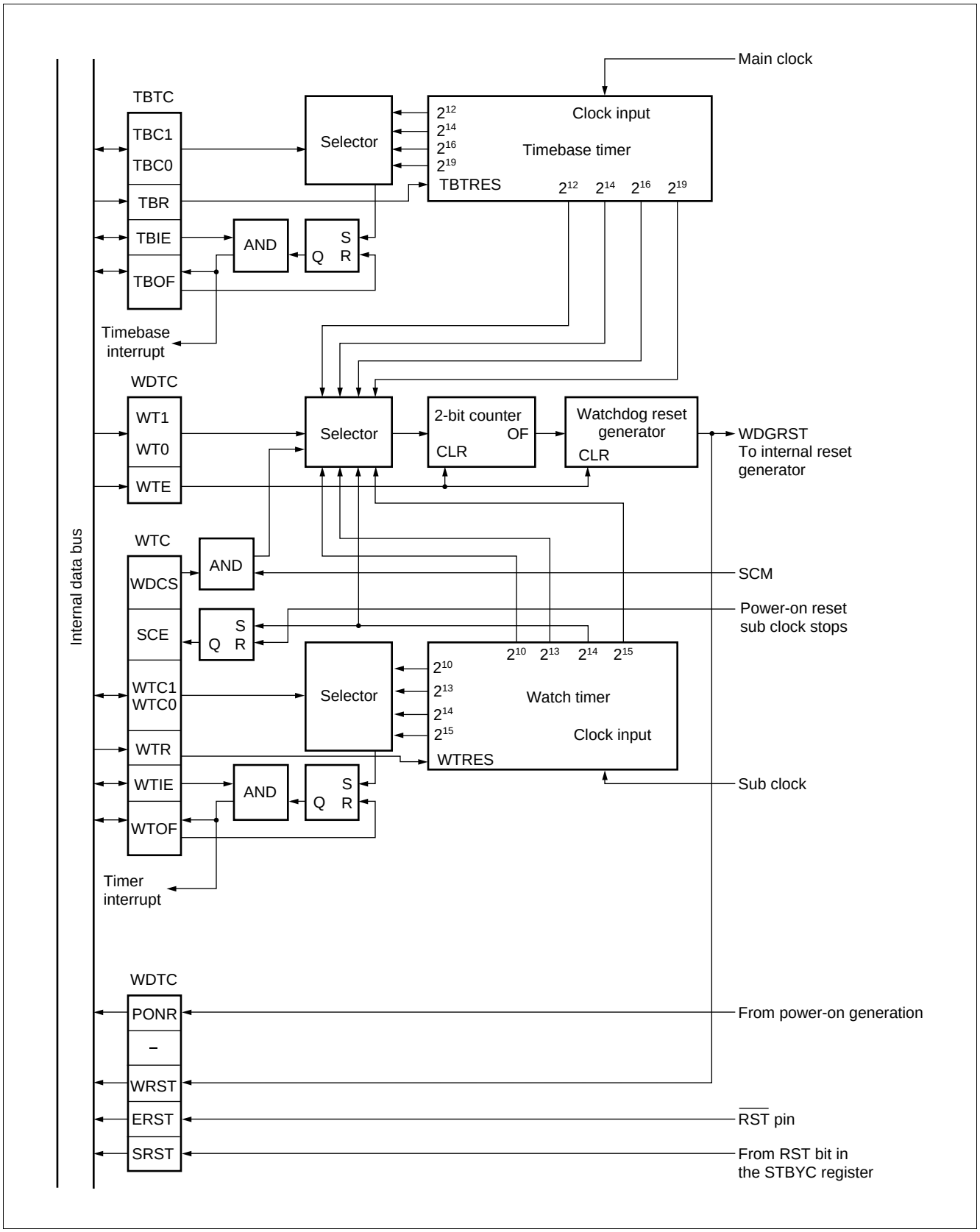
| | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | Initial value |
|---|---|---|---|---|---|---|---|---|---|
| Address : 0000A9H | Reserved | — | — | TBIE | TBOF | TBR | TBC1 | TBC0 | 1--00000B |
| | — | — | — | R/W | R/W | W | R/W | R/W | |

**• Watch timer control register (WTC)**

| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|
| Address : 0000AAH | WDCS | SCE | WTIE | WTOF | WTR | WTC2 | WTC1 | WTC0 | 1X000000B |
| | R/W | R | R/W | R/W | R | R/W | R/W | R/W | |

R/W : Readable and writable
R : Read only
W : Write only
— : Unused
X : Indeterminate

### (2) Block Diagram



## 12. I²C Interface

The I²C interface is a serial I/O port that supports the Inter-IC bus and operates as a master/slave device on the I²C bus. This module has the following features:

- Master/slave transmission/reception
- Arbitration function
- Clock synchronization function
- Slave address/general call address detection function
- Transfer direction detection function
- Start condition repeat generation and detection function
- Bus error detection function

### (1) Register Configuration

**• I²C bus status register (IBSR)**

Address : 000080H

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|
| BB | RSC | AL | LRB | TRX | AAS | GCA | FBT | 00000000B |
| R | R | R | R | R | R | R | R | |

**• I²C bus control register (IBCR)**

Address : 000081H

| bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | Initial value |
|---|---|---|---|---|---|---|---|---|
| BER | BEIE | SCC | MSS | ACK | GCAA | INTE | INT | 00000000B |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

**• I²C bus clock control register (ICCR)**

Address : 000082H

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|
| — | — | EN | CS4 | CS3 | CS2 | CS1 | CS0 | --0XXXXXB |
| — | — | R/W | R/W | R/W | R/W | R/W | R/W | |

**• I²C bus address register (IADR)**

Address : 000083H

| bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | Initial value |
|---|---|---|---|---|---|---|---|---|
| — | A6 | A5 | A4 | A3 | A2 | A1 | A0 | -XXXXXXXB |
| — | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

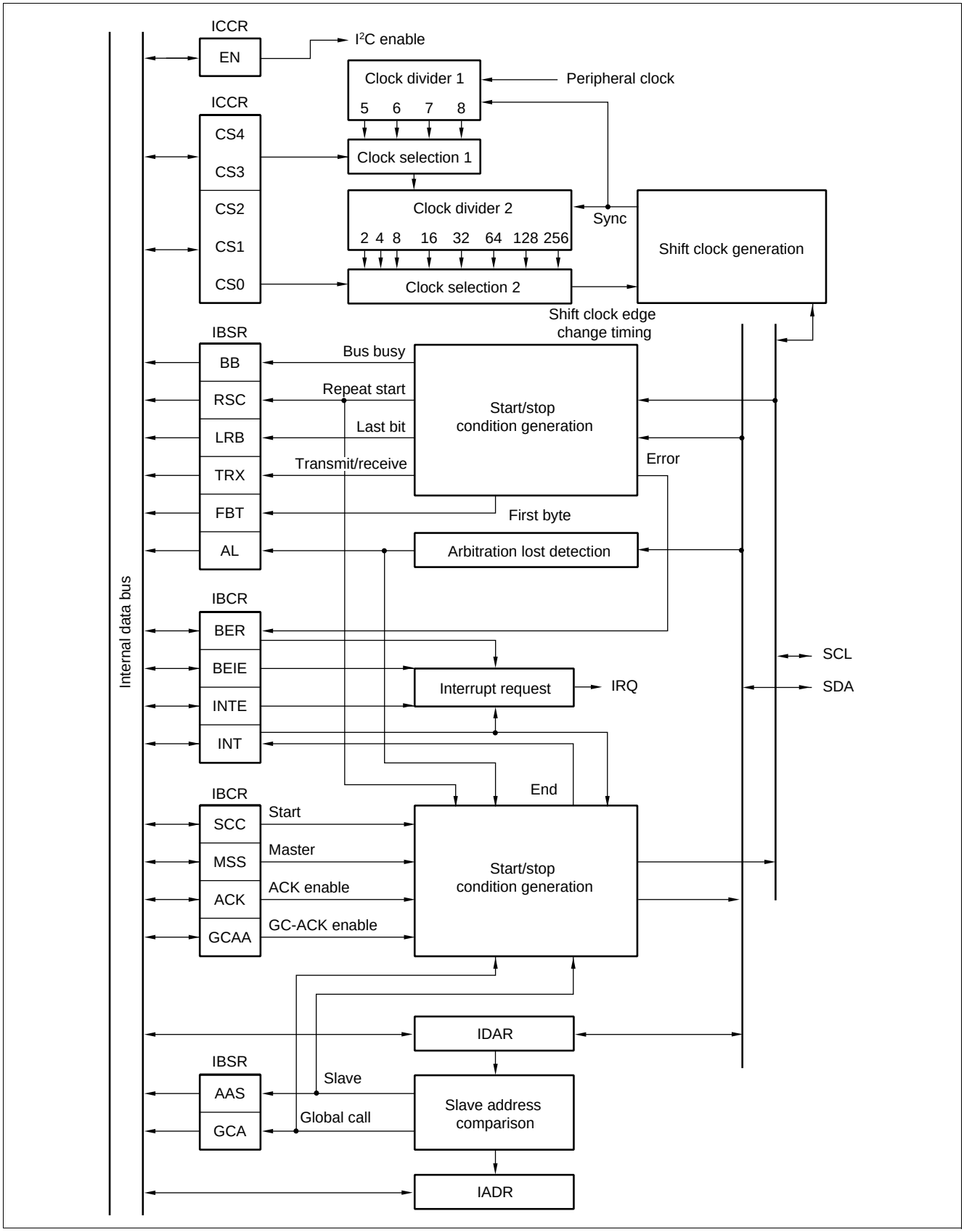
**• I²C bus data register (IDAR)**

Address : 000084H

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | XXXXXXXXB |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

R/W : Readable and writable
R : Read only
— : Unused
X : Indeterminate

### (2) Block Diagram



## 13. External Bus Pin Control Circuit

The external bus pin control circuit controls the external bus pins required to extend the CPU's address/data bus outside the device.

### (1) Register Configuration

• **Auto-ready function selection register (ARSR)**

Address : 0000A5H

| bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | Initial value |
|---|---|---|---|---|---|---|---|---|
| ICR1 | ICR0 | HMR1 | HMR0 | — | — | LMR1 | LMR0 | 0011--00B |
| W | W | W | W | — | — | W | W | |

• **External address output control register (HACR)**

Address : 0000A6H

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|
| E23 | E22 | E21 | E20 | E19 | E18 | E17 | E16 | 00000000B |
| W | W | W | W | W | W | W | W | |

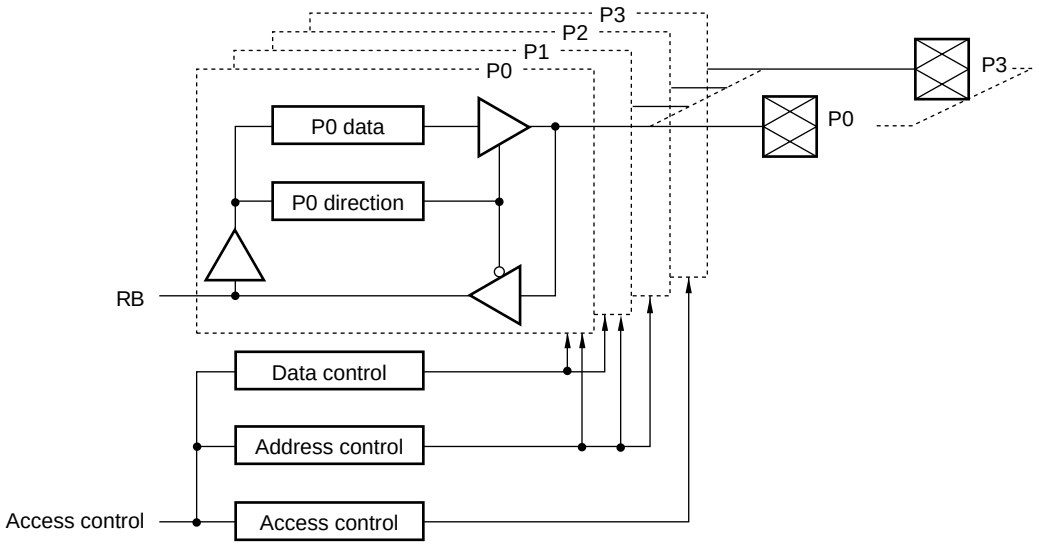
• **Bus control signal selection register (ECSR)**

Address : 0000A7H

| bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | Initial value |
|---|---|---|---|---|---|---|---|---|
| CKE | RYE | HDE | ICBS | HMBS | WRE | LMBS | — | 0000*00-B |
| W | W | W | W | W | W | W | — | |

W : Write only
— : Unused
* : "1" or "0"

### (2) Block Diagram



## 14. Low-power Consumption Mode (CPU Intermittent Operation Function, Oscillation Stabilization Delay Time, Clock Multiplier Function)

The following are the operating modes: PLL clock mode, PLL sleep mode, PLL watch mode, pseudo-watch mode, main clock mode, main sleep mode, main watch mode, main stop mode, sub clock mode, sub sleep mode, sub watch mode, and sub stop mode. Aside from the PLL clock mode, all of the other operating modes are low-power consumption modes.

In main clock mode and main sleep mode, the main clock (main OSC oscillation clock) and the sub clock (sub OSC oscillation clock) operate. In these modes, the main clock divided by 2 is used as the operation clock, the sub clock (sub OSC oscillation clock) is used as the timer clock, and the PLL clock (VCO oscillation clock) is stopped.

In sub clock mode and sub sleep mode, only the sub clock operates. In these modes, the sub clock is used as the operation clock, and the main clock and PLL clock are stopped.

In PLL sleep mode and main sleep mode, only the CPU's operation clock is stopped; all clocks other than the CPU clock operate.

In pseudo-watch mode, only the watch timer and timebase timer operate.

In PLL watch mode, main watch mode, and sub watch mode, only the watch timer operates. In this mode, only the sub clock is used for operation, while the main clock and the PLL clock are stopped (the difference between the PLL watch mode, the main watch mode and the sub watch mode is that it resumes operation after an interrupt in the PLL clock mode, the main clock mode, and the sub clock mode respectively, and there is no reference concerning about clock mode operation).

The main stop mode, sub stop mode, and hardware standby mode stop oscillation, making it possible to retain data while consuming the least amount of power. (The difference between the main stop mode and the sub stop mode is that it resumes operation in the main clock mode and the sub clock mode respectively, and there is no reference concerning about stop mode operation).

The CPU intermittent operation function intermittently runs the clock supplied to the CPU when accessing registers, on-chip memory, on-chip resources, and the external bus. Processing is possible with lower power consumption by reducing the execution speed of the CPU while supplying a high-speed clock and using on-chip resources.

The PLL clock multiplier can be selected as either 2, 4, 6, or 8 by setting the CS1 and CS0 bits. These clocks are divided by 2 to be used as a machine clock.

The WS1 and WS0 bits can be used to set the main clock oscillation stabilization delay time for when stop mode is woken up.

## (1) Register Configuration

• **Low-power consumption mode control register (LPMCR)**

Address : 0000A0H

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|
| STP | SLP | SPL | RST | TMD | CG1 | CG0 | Re-served | 00011000B |
| W | W | R/W | W | W | R/W | R/W | (—) | |

• **Clock selection register (CKSCR)**

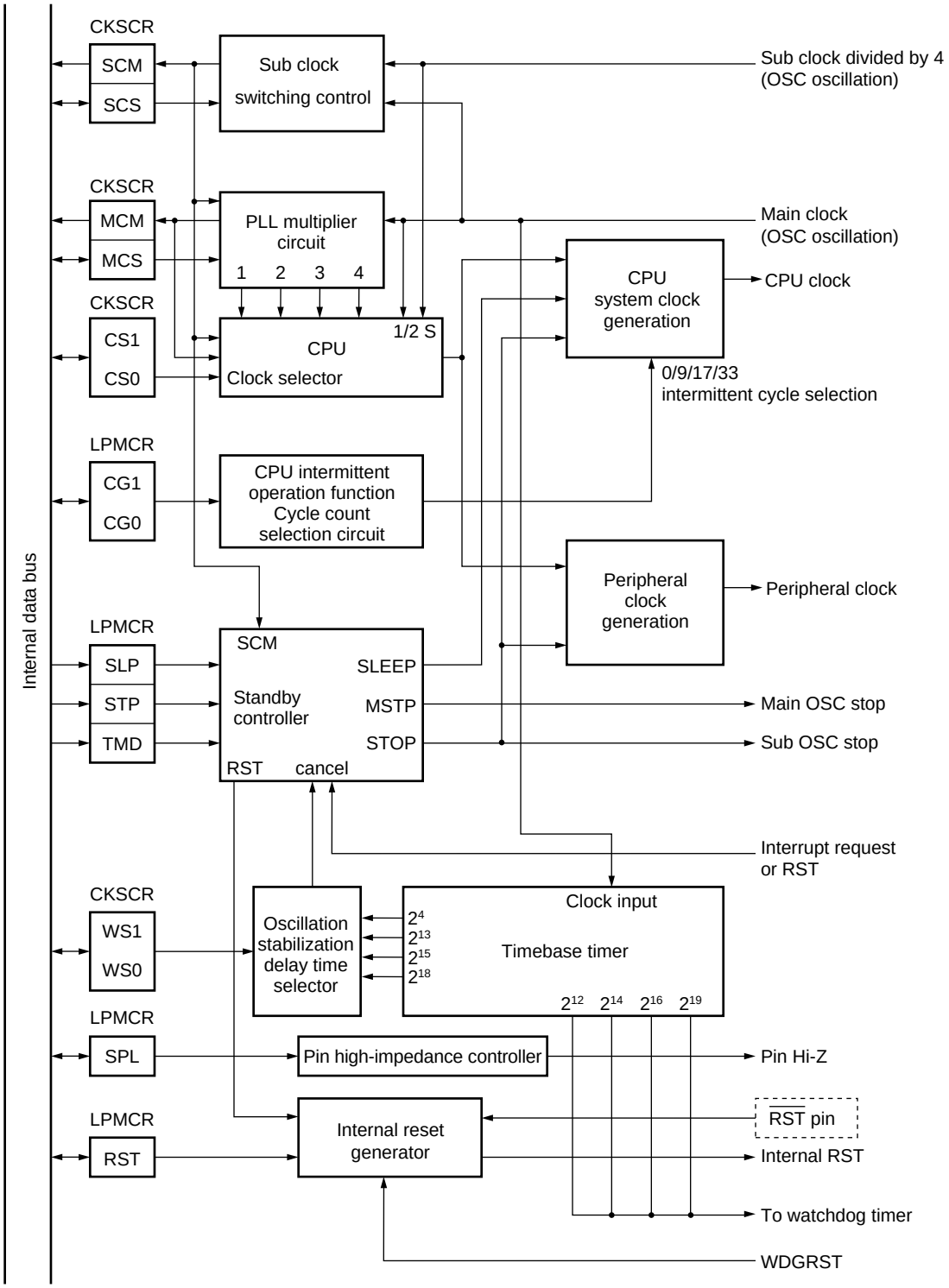
Address : 0000A1H

| bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | Initial value |
|---|---|---|---|---|---|---|---|---|
| SCM | MCM | WS1 | WS0 | SCS | MCS | CS1 | CS0 | 11111100B |
| R | R | R/W | R/W | R/W | R/W | R/W | R/W | |

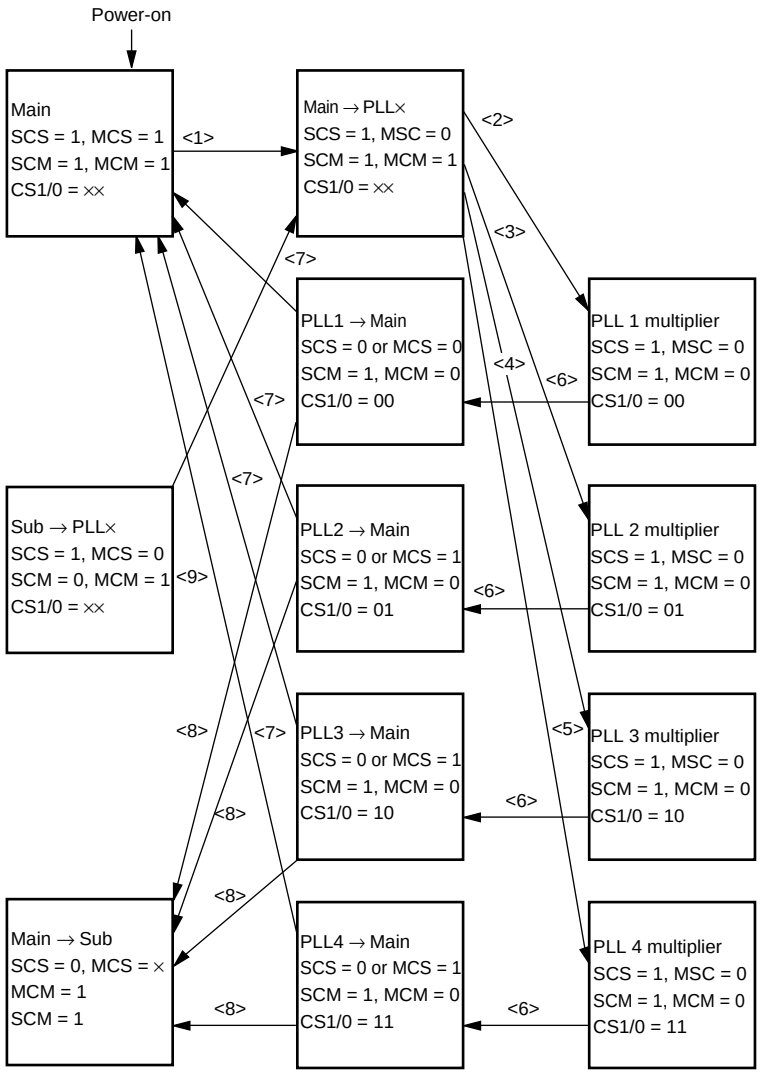
R/W : Readable and writable
R : Read only
W : Write only
Ñ : Unused

### (2) Block Diagram

- **Low-power consumption control circuit and clock generator**

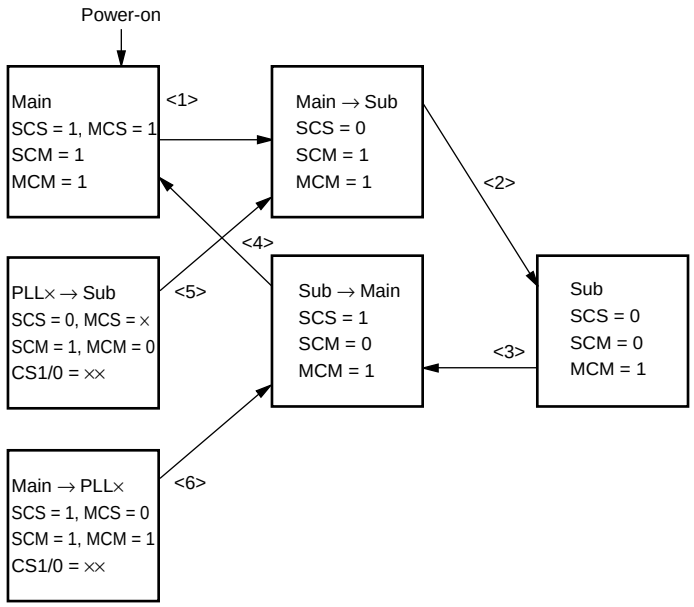


- **State transition diagram for clock selection (1)**




<1> MCS bit cleared and SCS bit set
<2> PLL clock oscillation stabilization delay complete and CS1/0 = 00
<3> PLL clock oscillation stabilization delay complete and CS1/0 = 01
<4> PLL clock oscillation stabilization delay complete and CS1/0 = 10
<5> PLL clock oscillation stabilization delay complete and CS1/0 = 11
<6> MCS bit set or SCS bit cleared
<7> PLL clock and main clock synchronized timing and SCS = 1
<8> PLL clock and main clock synchronized timing and SCS = 0
<9> Main clock oscillation stabilization delay complete and MCS = 0

- **State transition diagram for clock selection (2)**




<1> SCS bit cleared
<2> Sub clock edge detection timing
<3> SCS bit set
<4> Main clock oscillation stabilization delay complete and MCS = 1
<5> PLL clock and main clock synchronized timing and SCS = 0
<6> Main clock ascillation stabilization delay complete and MCS = 0

## 15. Delayed Interrupt Generation Module

The delayed interrupt generation module is used to generate the task switching interrupt. Interrupt requests to the F²MC-16L CPU can be generated and cleared by software using this module.

### (1) Register Details

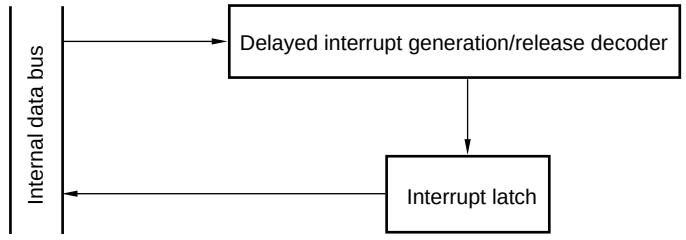
• **Delayed interrupt generation /release register (DIRR)**

| | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | Initial value |
|---|---|---|---|---|---|---|---|---|---|
| Address : 00009F$_H$ | — | — | — | — | — | — | — | R0 | -------0$_B$ |
| | | | | | | | | R/W | |

R/W : Readable and writable
— : Unused

The DIRR register controls generation and clearing of delayed interrupt requests. Writing “1” to the register generates a delayed interrupt request. Writing “0” to the register clears the delayed interrupt request. The register is set to the interrupt cleared state by a reset. Either “0” or “1” can be written to the reserved bits. However, considering possible future extensions, it is recommended that the set bit and clear bit instructions are used for register access.

### (2) Block Diagram



## 16. DTMF Generator

The DTMF (dual tone multifrequency) generator is a module that can generate a series of audio tones as heard from a push-button telephone or a radio transceiver with a keypad. It has the following features:

Capable of generating DTMF tones continuously (or even a single tone)

Capable of generating all CCITT tones: 0 to 9, *, #, A to D

### (1) Register list

**• DTMF control register (DTMC)**

Address : 000088H

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|
| — | CSL2 | CSL1 | CSL0 | CDIS | RDIS | OUTE | — | 00000000B |
| — | R/W | R/W | R/W | R/W | R/W | R/W | — | |

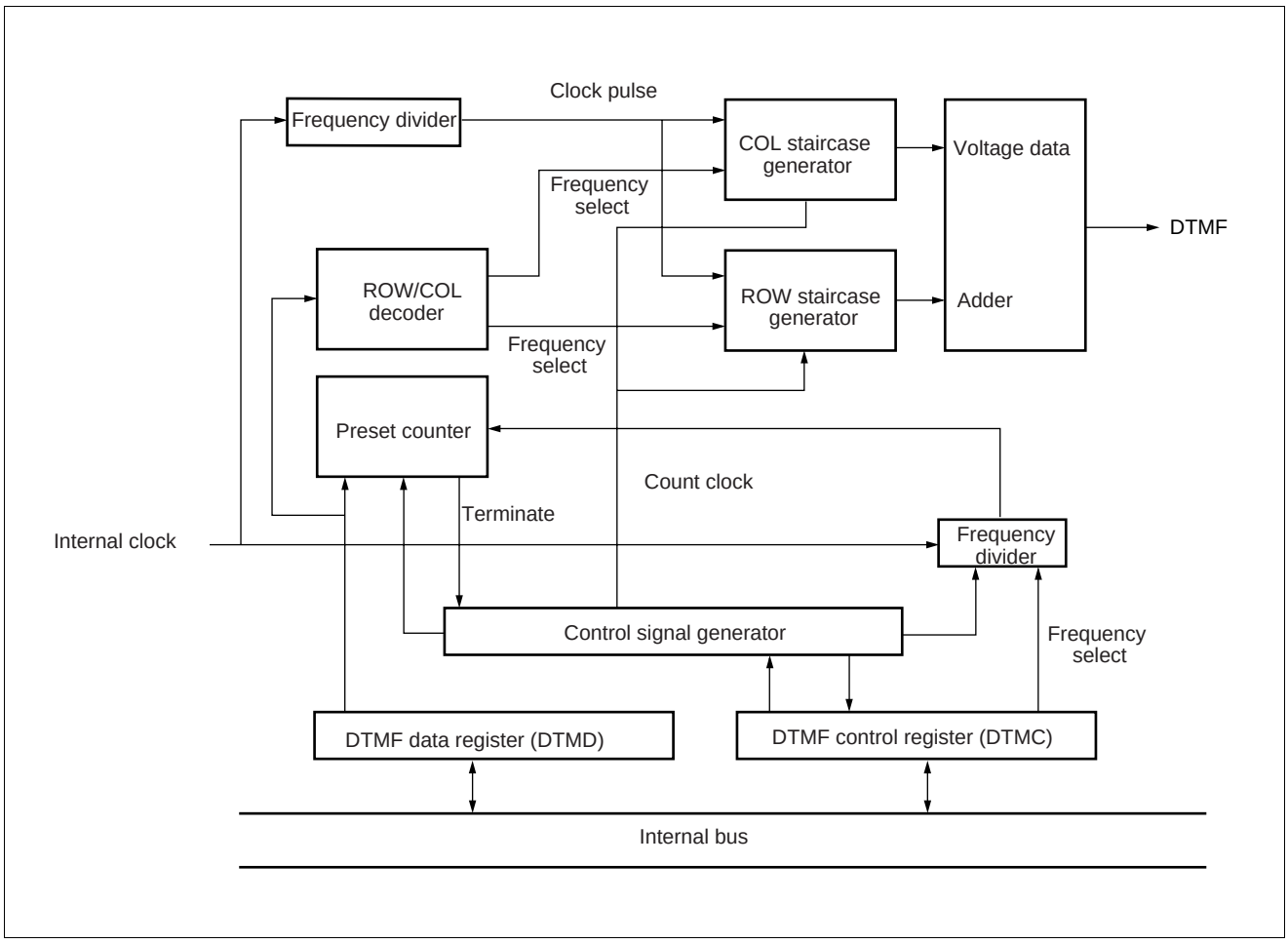
**• DTMF data register (DTMD)**

Address : 000089H

| bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | Initial value |
|---|---|---|---|---|---|---|---|---|
| — | — | — | — | DDAT3 | DDAT2 | DDAT1 | DDAT0 | 000X0000B |
| — | — | — | — | R/W | R/W | R/W | R/W | |

R/W : Read/write enabled
— : Unused
X : Undefined

### (2) Block diagram



## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

($V_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Rating | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Power supply voltage | $V_{CC}1$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 4.0 | V | without MB90V650A |
| | $V_{CC}2$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 7.0 | V | |
| | $AV_{CC}$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 4.0 | V | without MB90V650A *1 |
| | AVRH AVRL | $V_{SS}$ – 0.3 | $V_{SS}$ + 4.0 | V | without MB90V650A |
| | DVRH | $V_{SS}$ – 0.3 | $V_{SS}$ + 4.0 | V | without MB90V650A |
| Input voltage | $V_I$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 4.0 | V | without MB90V650A *2 |
| | $V_{IC}$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 7.0 | V | P47, P70/SDA, P71/SLC, P72 (N-ch open-drain pins) |
| Output voltage | $V_O$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 4.0 | V | without MB90V650A *2 |
| Maximum clamp current | $I_{CLAMP}$ | –2.0 | +2.0 | mA | *6 |
| Total maximum clamp current | $\sum \lvert I_{CLAMP} \rvert$ | — | +20 | mA | *6 |
| “L” level maximum output current | $I_{OL}$ | — | 10 | mA | without MB90V650A *3 |
| “L” level average output current | $I_{OLAV}$ | — | 3 | mA | without MB90V650A *4 |
| “L” level total maximum output current | $\Sigma I_{OL}$ | — | 60 | mA | without MB90V650A |
| “L” level total average output current | $\Sigma I_{OLAV}$ | — | 30 | mA | without MB90V650A *5 |
| “H” level maximum output current | $I_{OH}$ | — | –10 | mA | without MB90V650A *3 |
| “H” level average output current | $I_{OHAV}$ | — | –3 | mA | without MB90V650A *4 |
| “H” level total maximum output current | $\Sigma I_{OH}$ | — | –60 | mA | without MB90V650A |
| “H” level total average output current | $\Sigma I_{OHAV}$ | — | –30 | mA | *5 |
| Power consumption | $P_D$ | — | 200 | mW | |
| Operating temperature | $T_A$ | –40 | +85 | °C | |
| Storage temperature | Tstg | –55 | +150 | °C | |

*1 : $AV_{CC}$, AVRH, AVRL and DVRH shall never exceed $V_{CC}$ ($V_{CC}1$ and $V_{CC}2$ are contained). AVRH, AVRL shall never exceed $AV_{CC}$. Also, AVRL shall never exceed AVRH.

*2 : $V_I$ and $V_O$ must not exceed $V_{CC}$ ($V_{CC1}$ and $V_{CC2}$ are contained) + 0.3 V.

*3 : Maximum output current specifies the peak value or one corresponding pin.

*4 : The average output current is the rating for the current from an individual pin averaged over 100 ms.

*5 : The average total output current is the rating for the current from all pins averaged over 100 ms.

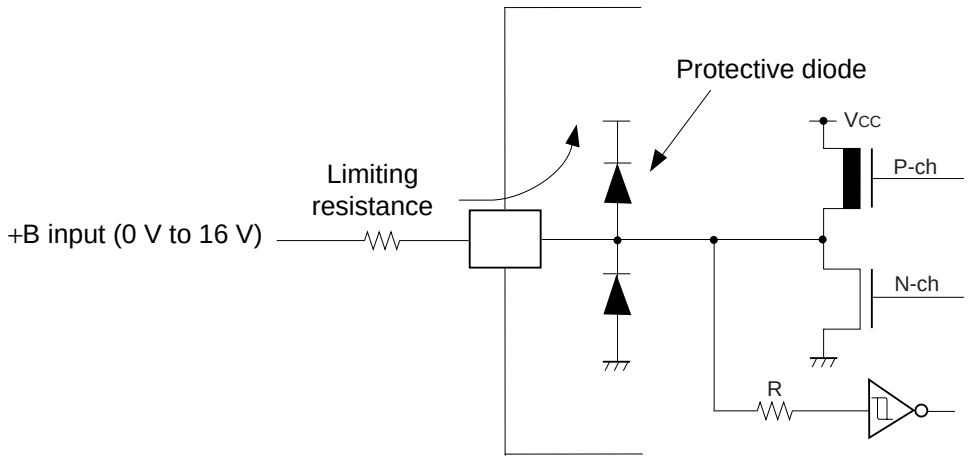
*(Continued)*

*(Continued)*

*6 : • Applicable to pins : P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P74, P80 to P86, P90 to P97, PA0 to PA2

- Use within recommended operating conditions.
- Use at DC voltage (current).
- The +B signal should always be applied with a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the $V_{CC}$ pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller current is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal input.
- Sample recommended circuits :

• Input/Output Equivalent circuits




WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## 2. Recommended Operating Conditions

($V_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Value | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Power supply voltage | $V_{CC}1$ | 2.2 | 3.6 | V | For normal operation (MB90652A/653A/654A) |
| | | 2.4 | 3.6 | V | For normal operation (MB90F654A) |
| | $V_{CC}2$ | 2.2 | 5.5 | V | For normal operation (MB90652A/653A/654A) |
| | | 2.4 | 5.5 | V | For normal operation (MB90F654A) |
| | $V_{CC}1$ | 1.8 | 3.6 | V | To maintain statuses in stop mode (MB90652A/653A/654A) |
| | | 1.8 | 3.6 | V | To maintain statuses in stop mode (MB90F654A) |
| | $V_{CC}2$ | 1.8 | 5.5 | V | To maintain statuses in stop mode (MB90652A/653A/654A) |
| | | 1.8 | 5.5 | V | To maintain statuses in stop mode (MB90F654A) |
| “H” level input voltage | $V_{IH}$ | 0.7 $V_{CC}$ | $V_{CC}$ + 0.3 | V | Pins other than $V_{IHS}$ and $V_{IHM}$ |
| | $V_{IH2}$ | 0.7 $V_{CC}$ | $V_{CC}$ + 0.3 | V | P70/SDA, P71/SLC (only $I^2C$ pin) |
| | $V_{IHS}$ | 0.8 $V_{CC}$ | $V_{CC}$ + 0.3 | V | Hysteresis input pins |
| | $V_{IHM}$ | $V_{CC}$ – 0.3 | $V_{CC}$ + 0.3 | V | MD pin input |
| | $V_{IHT}$ | 2.4 | $V_{CC}$ + 0.3 | V | TTL input pins |
| “L” level input voltage | $V_{IL}$ | $V_{SS}$ – 0.3 | 0.3 $V_{CC}$ | V | PIns other than $V_{ILS}$ and $V_{ILM}$ |
| | $V_{IL2}$ | $V_{SS}$ – 0.3 | 0.3 $V_{CC}$ | V | P70/SDA, P71/SLC (only $I^2C$ pin) |
| | $V_{ILS}$ | $V_{SS}$ – 0.3 | 0.2 $V_{CC}$ | V | Hysteresis input pins |
| | $V_{ILM}$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 0.3 | V | MD pin input |
| | $V_{ILT}$ | $V_{SS}$ – 0.3 | 0.8 | V | TTL input pins |
| Operating temperature | $T_A$ | –40 | +85 | °C | |

Note : $I^2C$ must be used at above 2.7 V.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

## 3. DC Characteristics

(MB90652A/653A/654A: $V_{CC}$ = 2.2 V to 3.6 V, $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)
(MB92F654A: $V_{CC}$ = 2.4 V to 3.6 V, $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| "H" level output voltage*2 | $V_{OH}$ | Pins except P47, P70 to P72 | $V_{CC}2$ = 4.5 V, $I_{OH}$ = –4.0 mA | $V_{CC}2$– 0.5 | — | — | V | When the 5-V power supply is used |
| | | | $V_{CC}$ = 2.7 V, $I_{OH}$ = –1.6 mA | $V_{CC}1$– 0.3 | — | — | V | When the 3-V power supply is used *1 |
| "L" level output voltage*2 | $V_{OL}$ | All output pins | $V_{CC}2$ = 4.5 V, $I_{OL}$ = 4.0 mA | — | — | 0.4 | V | When the 5-V power supply is used |
| | | | $V_{CC}$ = 2.7 V, $I_{OL}$ = 2.0 mA | — | — | 0.4 | V | When the 3-V power supply is used |
| Input leakage current | $I_{IL}$ | Except P50 to P57, P90, P91 | $V_{CC}$ = 3.3 V, $V_{SS} < V_I < V_{CC}$ | –10 | — | 10 | µA | |
| Pull-up resistor | RPULL | — | When $V_{CC}$ = 3.0 V, $T_A$ = +25°C | 20 | 65 | 200 | kΩ | without MB90V650A |
| Open-drain output leakage current | $I_{leak}$ | P40 to P47, P70 to P72 | — | — | 0.1 | 10 | µA | |
| Power supply current | $I_{CC}$ | — | When $V_{CC}$ = 3.0 V Internal 8 MHz operation | — | 10 | 20 | mA | MB90652A/653A/654A: During normal operation |
| | $I_{CC}$ | | | — | 17 | 24 | mA | MB90652A/653A/654A: In A/D operation |
| | $I_{CC}$ | | | — | 19 | 26 | mA | MB90652A/653A/654A: In D/A operation |
| | $I_{CCS}$ | | | — | 2.5 | 5 | mA | MB90652A/653A/654A: During sleep |
| | $I_{CC}$ | — | When $V_{CC}$ = 3.0 V Internal 12 MHz operation | — | 16 | 31 | mA | MB90652A/653A/654A: During normal operation |
| | $I_{CC}$ | | | — | 21 | 39 | mA | MB90F654A: During normal operation |
| | $I_{CC}$ | | | — | 37 | 44 | mA | MB90F654A: Flash write/erase |
| | $I_{CC}$ | | | — | 27 | 37 | mA | MB90652A/653A/654A: In A/D operation |
| | $I_{CC}$ | | | — | 32 | 42 | mA | MB90F654A: In A/D operation |
| | $I_{CC}$ | | | — | 30 | 38 | mA | MB90652A/653A/654A: In D/A operation |
| | $I_{CC}$ | | | — | 30 | 38 | mA | MB90F654A: In D/A operation |

*(Continued)*

*(Continued)*

(MB90652A/653A/654A: $V_{CC}$ = 2.2 V to 3.6 V, $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)
(MB90F654A: $V_{CC}$ = 2.4 V to 3.6 V, $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Power supply current | $I_{CCS}$ | — | When $V_{CC}$ = 3.0 V Internal 12 MHz operation | — | 3.5 | 9 | mA | MB90652A/653A/654A: During sleep |
| | $I_{CCS}$ | | | — | 4.8 | 10 | mA | MB90F654A: During sleep |
| | $I_{CCH}$ | — | $T_A$ = +25°C When $V_{CC}$ = 3.0 V | — | 0.1 | 20 | µA | MB90652A/653A/654A: During stop |
| | $I_{CCH}$ | | | — | 0.2 | 40 | µA | MB90F654A: During stop |
| | $I_{CCL}$ | — | $V_{CC}$ = 3.0 V, $T_A$ = +25°C External 32 kHz operation (Internal 8 MHz operation) | — | 16 | 140 | µA | without MB90V650A: In sub operation |
| | $I_{CCT}$ | — | $V_{CC}$ = 3.0 V, $T_A$ = +25°C External 32 kHz operation | — | 10 | 30 | µA | MB90652A/653A/654A: In watch mode |
| | $I_{CCT}$ | | | — | 15 | 30 | µA | MB90F654A: In watch mode |
| Input capacitance | $C_{IN}$ | Except $AV_{CC}$, $AV_{SS}$, $V_{CC}$, $V_{SS}$ | — | — | 5 | 15 | pF | |

* 1 : P40 to P46 are N-ch open-drain pins to be controlled and are usually used as CMOS devices.

* 2 : When the device is used with dual power supplies, the P20 to P27, P30 to P37, P40 to P47, and P70 to P72 are the 5 V pins and the rest are the 3 V pins.

Note : $V_{CC} = V_{CC}1 = V_{CC}2$

## 4. AC Characteristics

### (1) Clock Timing

($V_{CC}$ = 2.7 V to 3.6 V, $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

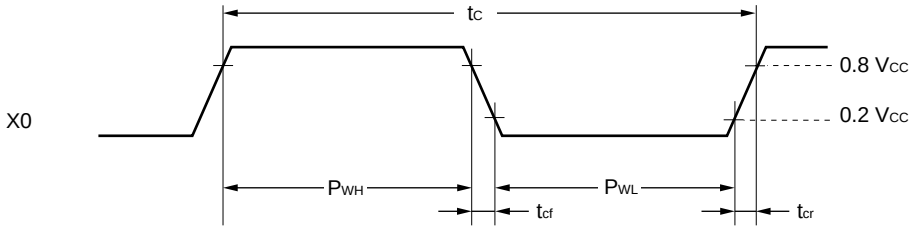
| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Clock frequency | $F_{CH}$ | X0, X1 | — | 3 | — | 24 | MHz | |
| | $F_{CL}$ | X0A, X1A | — | — | 32.768 | — | kHz | |
| Clock cycle time | $t_C$ | X0, X1 | — | 41.67 | — | 333 | ns | |
| | $t_{CL}$ | X0A, X1A | — | — | 30.5 | — | µs | |
| Input clock pulse width | $P_{WH}$ $P_{WL}$ | X0 | — | 5 | — | — | ns | * |
| | $P_{WLH}$ $P_{WLL}$ | X0A | — | — | 15.2 | — | µs | * |
| Input clock rise time and fall time | $t_{cr}$ $t_{cf}$ | X0 | — | — | — | 5 | ns | External clock |
| Internal operating clock frequency | $f_{CP}$ | — | — | 1.5 | — | 12 | MHz | |
| | $f_{CPL}$ | — | — | — | 8.192 | — | kHz | |
| Internal operating clock cycle time | $t_{CP}$ | — | — | 83.3 | — | 666 | ns | |
| | $t_{CPL}$ | — | — | — | 122.1 | — | µs | |

Because the PLL frequency fluctuates around the set frequency with a certain cycle [approximately CLK × (1 CYC to 50 CYC)], the worst value is not maintained for long. (The pulse, if featured with the long period, would produce practically no error.)

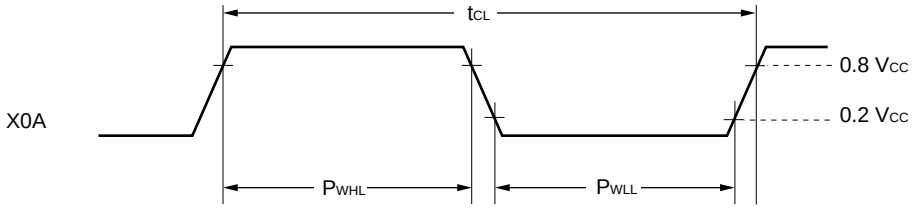
* : The duty ratio should be in the range 30% to 70%.

Note : $V_{CC}$ = $V_{CC}1$ = $V_{CC}2$

**•Main clock timing condition (X0, X1)**

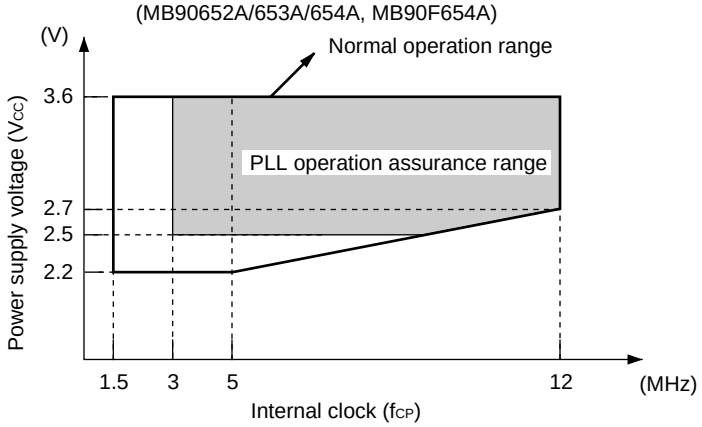



**• Subclock timing condition (X0A, X1A)**

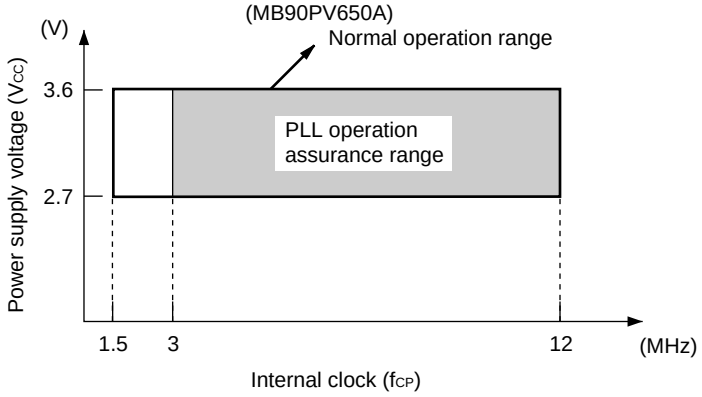


- **PLL operation assurance range**

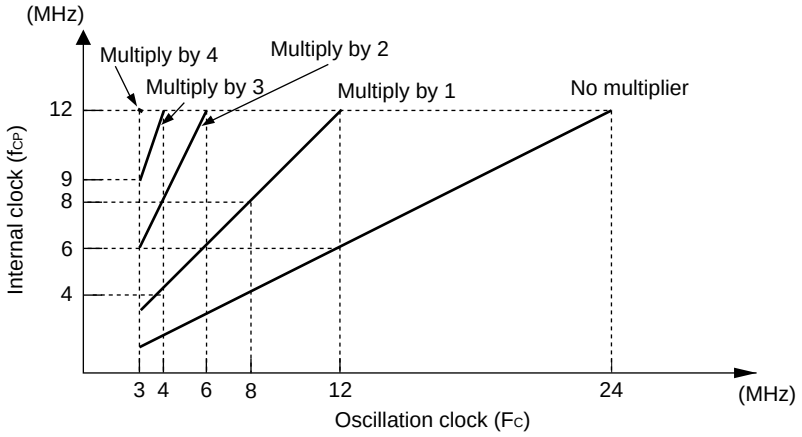
Relationship between the internal operating clock frequency and power supply voltage
(MB90652A/653A/654A, MB90F654A)




Relationship between the internal oprating clock frequency and power supply voltage
(MB90PV650A)



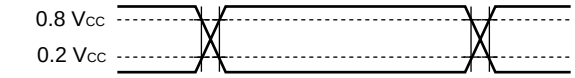

Relationship between the oscillation frequency and internal operating clock frequency



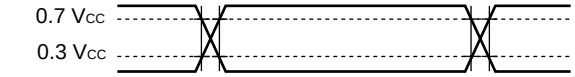
The AC characteristics are for the following measurement reference voltages.

- **Input signal waveform**

Hysteresis input pins




Other than hysteresis or MD input pins




- **Output signal waveform**

Output pins

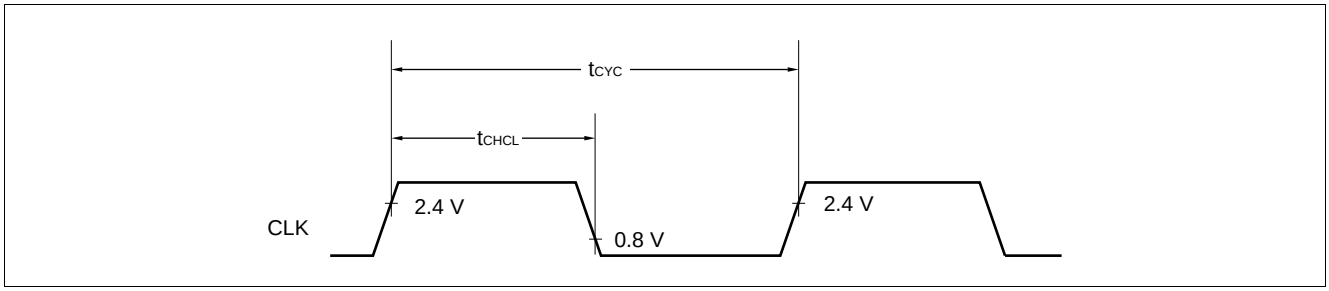
### (2) Clock Output Timing

($V_{CC}$ = 2.7 V to 3.6 V, $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Cycle time | $t_{CYC}$ | CLK | — | $t_{CP}$* | — | ns | |
| CLK ↑ → CLK↓ | $t_{CHCL}$ | CLK | $V_{CC}$ = 3.0 V ±10% | $t_{CP}$* / 2 – 20 | $t_{CP}$* / 2 + 20 | ns | |
| | | | | $t_{CP}$* / 2 – 64 | $t_{CP}$* / 2 + 64 | ns | In the external frequency of 5 MHz |

* : For $t_{CP}$ see “(1) Clock Timing.”

Note : $V_{CC}$ = $V_{CC}1$ = $V_{CC}2$



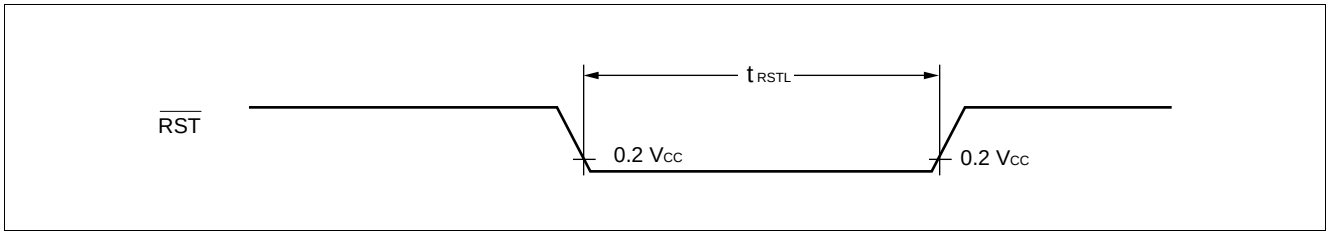

### (3) Reset Input Specifications

($V_{CC}$ = 2.7 V to 3.6 V, $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

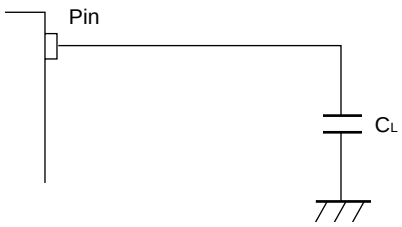
| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Reset input time | $t_{RSTL}$ | $\overline{RST}$ | — | 16 $t_{CP}$* | — | ns | |

* : For $t_{CP}$ see “(1) Clock Timing.”

Note : $V_{CC}$ = $V_{CC}1$ = $V_{CC}2$




- **AC characteristics measurement conditions**




$C_L$ : Load capacitance at testing

CLK, ALE: $C_L$ = 30 pF
AD15 to AD00 (address/data bus), $\overline{RD}$, $\overline{WR}$: $C_L$ = 80 pF

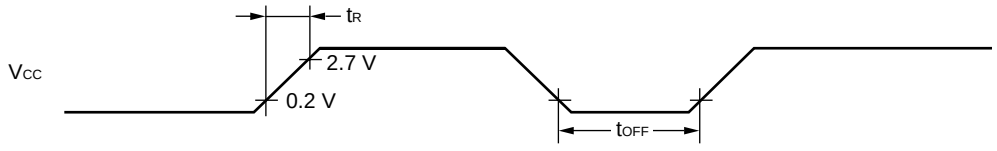
### (4) Power on Supply Specifications (Power-on Reset)

($V_{CC}$ = 2.7 V to 3.6 V, $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

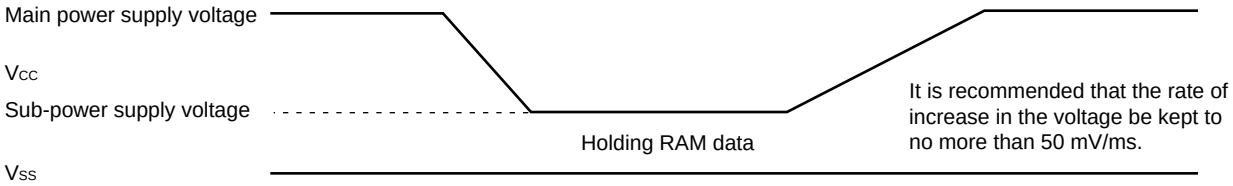
| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Power supply rising time | $t_R$ | $V_{CC}$ | — | — | 30 | ms | * |
| Power supply cut-off time | $t_{OFF}$ | $V_{CC}$ | — | 1 | — | ms | Due to repeat operation |

* : When the power rising, $V_{CC}$ must be less than 0.2 V.

Notes : • The above standards are the values needed in order to activate a power-on reset.
• Activate a power-on reset by turning on the power supply again this in device.
• $V_{CC}$ = $V_{CC}1$ = $V_{CC}2$




Abrupt changes in the power supply voltage may cause a power-on reset.
When changing the power supply voltage during operation, suppress variations in the voltage and ensure that the voltage rises smoothly, as shown in the following figure.



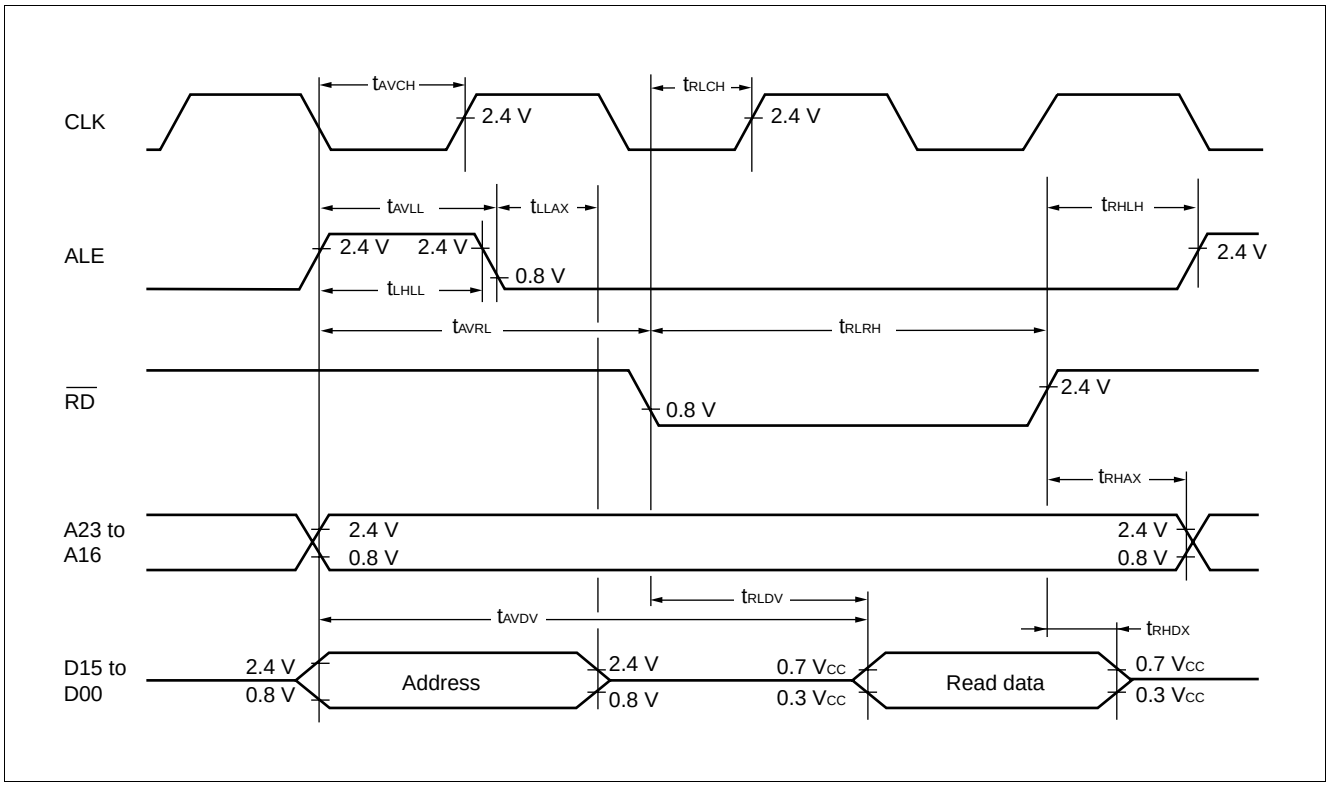
### (5) Bus Read Timing

($V_{CC}$ = 2.7 V to 3.6 V, $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| ALE pulse width | $t_{LHLL}$ | ALE | — | $t_{CP}$* /2 – 20 | — | ns | MASK/FLASH |
| Valid address → ALE ↓ time | $t_{AVLL}$ | Multiplexed address | — | $t_{CP}$* / 2 – 25 | — | ns | MASK/FLASH |
| ALE ↓ → address valid time | $t_{LLAX}$ | Multiplexed address | — | $t_{CP}$* / 2 – 15 | — | ns | |
| Valid address → $\overline{RD}$ ↓ time | $t_{AVRL}$ | Multiplexed address | — | $t_{CP}$* – 15 | — | ns | |
| Valid address → valid data input | $t_{AVDV}$ | Multiplexed address | — | — | 5 $t_{CP}$* / 2 – 60 | ns | MASK/FLASH |
| $\overline{RD}$ pulse width | $t_{RLRH}$ | $\overline{RD}$ | — | 3 $t_{CP}$* / 2 – 20 | — | ns | |
| $\overline{RD}$ ↓ → valid data input | $t_{RLDV}$ | D15 to D00 | — | — | 5 $t_{CP}$* / 2 – 60 | ns | MASK/FLASH |
| $\overline{RD}$ ↑ → data hold time | $t_{RHDX}$ | D15 to D00 | — | 0 | — | ns | |
| $\overline{RD}$ ↑ → ALE ↑ time | $t_{RHLH}$ | $\overline{RD}$, ALE | — | $t_{CP}$* / 2 – 15 | — | ns | |
| $\overline{RD}$ ↑ → address valid time | $t_{RHAX}$ | Address, $\overline{RD}$ | — | $t_{CP}$* / 2 – 10 | — | ns | |
| Valid address → CLK ↑ time | $t_{AVCH}$ | Address, CLK | — | $t_{CP}$* / 2 –20 | — | ns | |
| $\overline{RD}$ ↓ → CLK ↑ time | $t_{RLCH}$ | $\overline{RD}$, CLK | — | $t_{CP}$* / 2 – 20 | — | ns | |

* : For $t_{CP}$ see “(1) Clock Timing.”

Note : $V_{CC}$ = $V_{CC}1$ = $V_{CC}2$



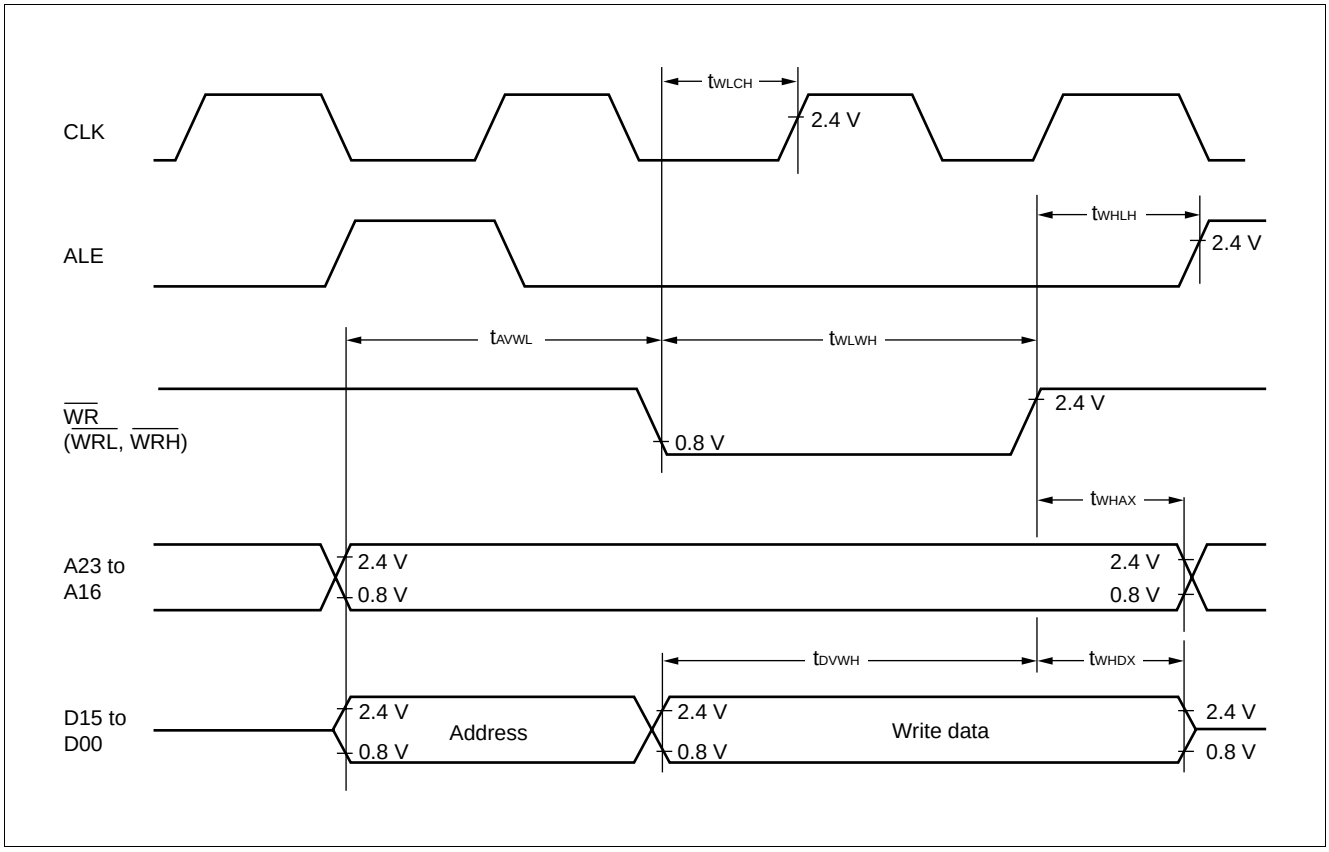
### (6) Bus Write Timing

($V_{CC}$ = 2.7 V to 3.6 V, $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Valid address → $\overline{WR}$ ↓ time | $t_{AVWL}$ | A23 to A00 | — | $t_{CP}$* – 15 | — | ns | |
| $\overline{WR}$ pulse width | $t_{WLWH}$ | $\overline{WR}$ | — | 3 $t_{CP}$* / 2 – 20 | — | ns | |
| Valid data output → $\overline{WR}$ ↑ time | $t_{DVWH}$ | D15 to D00 | — | 3 $t_{CP}$* / 2 – 20 | — | ns | |
| $\overline{WR}$ ↑ → data hold time | $t_{WHDX}$ | D15 to D00 | — | 20 | — | ns | MASK/FLASH |
| $\overline{WR}$ ↑ → address valid time | $t_{WHAX}$ | A23 to A00 | — | $t_{CP}$* / 2 – 10 | — | ns | |
| $\overline{WR}$ ↑ → ALE ↑ time | $t_{WHLH}$ | $\overline{WR}$, ALE | — | $t_{CP}$* / 2 – 15 | — | ns | |
| $\overline{WR}$ ↓ → CLK ↑ time | $t_{WLCH}$ | $\overline{WR}$, ALE | — | $t_{CP}$* / 2 – 20 | — | ns | |

* : For $t_{CP}$ see “(1) Clock Timing.”

Note : $V_{CC}$ = $V_{CC}1$ = $V_{CC}2$

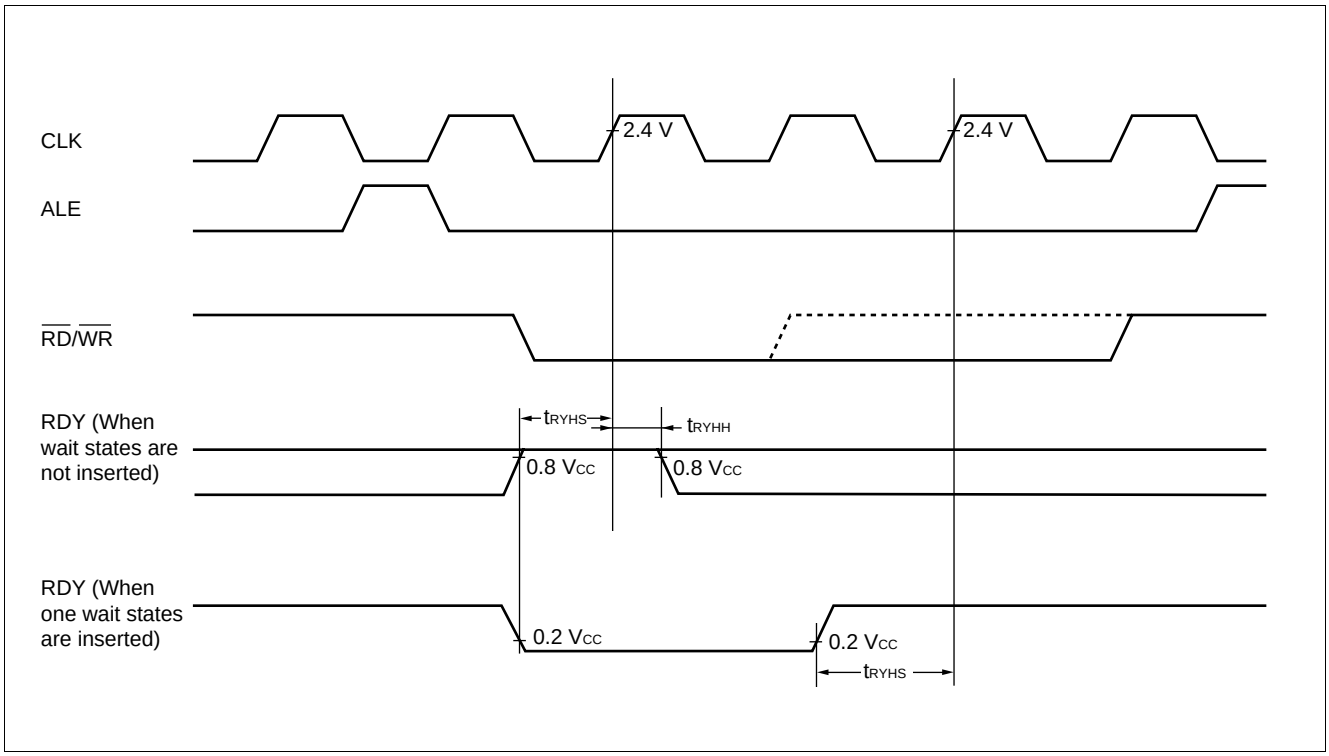


### (7) Ready Input Timing

($V_{CC}$ = 2.7 V to 3.6 V, $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| RDY setup time | $t_{RYHS}$ | RDY | — | 45 | — | ns | MASK/FLASH |
| RDY hold time | $t_{RYHH}$ | RDY | — | 0 | — | ns | |

Notes: • Use the auto-ready function if the RDY setup time is too short
• $V_{CC}$ = $V_{CC}1$ = $V_{CC}2$.



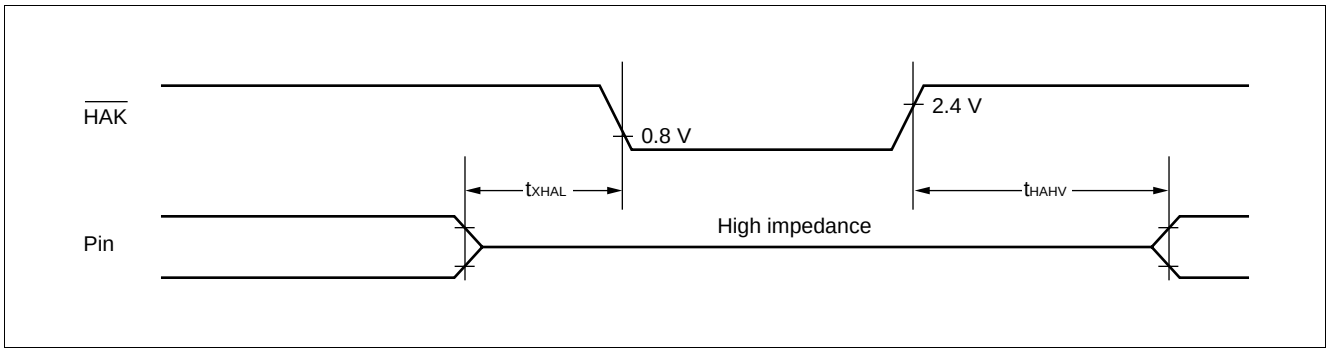
### (8) Hold Timing

($V_{CC}$ = 2.7 V to 3.6 V, $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Pin floating → $\overline{HAK}$ ↓ time | $t_{XHAL}$ | $\overline{HAK}$ | — | 30 | $t_{CP}$* | ns | |
| $\overline{HAK}$ ↑ → pin valid time | $t_{HAHV}$ | $\overline{HAK}$ | — | $t_{CP}$* | 2 $t_{CP}$* | ns | |

* : For $t_{CP}$ see “(1) Clock Timing.”

Notes: • After reading HRQ, more than one cycle is required before changing $\overline{HAK}$.
• $V_{CC}$ = $V_{CC}1$ = $V_{CC}2$



### (9) UART Timing

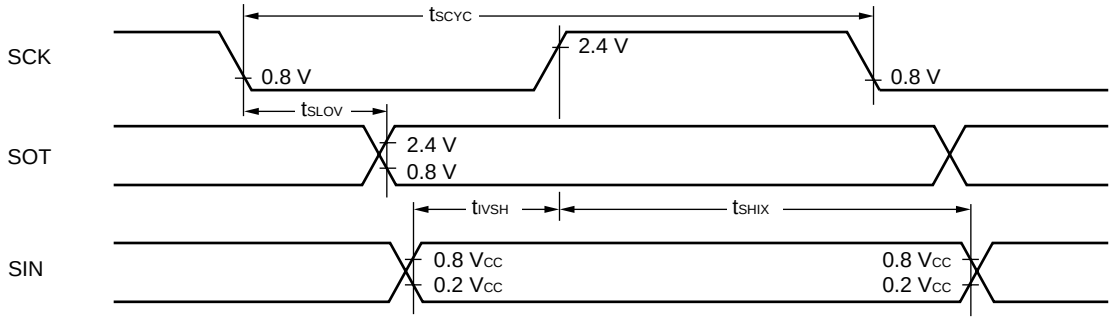
($V_{CC}$ = 2.7 V to 3.6 V, $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Serial clock cycle time | $t_{SCYC}$ | — | $C_L$ = 80 pF + 1 TTL for the internal shift clock mode output pin | 8 $t_{CP}$* | — | ns | |
| SCK ↓ → SOT delay time | $t_{SLOV}$ | — | | –80 | +80 | ns | MASK/FLASH |
| Valid SIN → SCK ↑ | $t_{IVSH}$ | — | | 100 | — | ns | MASK/FLASH |
| SCK ↑ → valid SIN hold time | $t_{SHIX}$ | — | | $t_{CP}$* | — | ns | |
| Serial clock “H” pulse width | $t_{SHSL}$ | — | $C_L$ = 80 pF + 1 TTL for the external shift clock mode output pin | 4 $t_{CP}$* | — | ns | |
| Serial clock “L” pulse width | $t_{SLSH}$ | — | | 4 $t_{CP}$* | — | ns | |
| SCK ↓ → SOT delay time | $t_{SLOV}$ | — | | — | 150 | ns | MASK/FLASH |
| Valid SIN → SCK ↑ | $t_{IVSH}$ | — | | 60 | — | ns | MASK/FLASH |
| SCK ↑ → valid SIN hold time | $t_{SHIX}$ | — | | 60 | — | ns | MASK/FLASH |

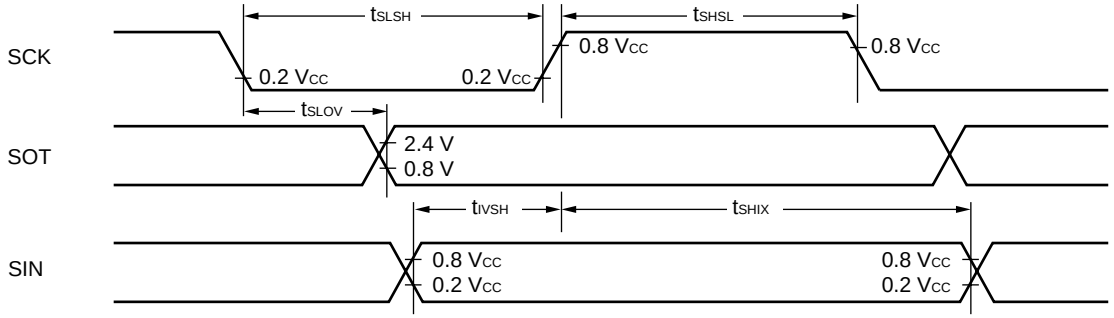
* : For $t_{CP}$ see “(1) Clock Timing.”

Notes: • These are the AC characteristics for CLK synchronous mode.
• $C_L$ is the load capacitance connected to the pin at testing.
• $V_{CC}$ = $V_{CC}1$ = $V_{CC}2$

• **Internal shift clock mode**




• **External shift clock mode**



### (10) I/O Extended Serial Timing

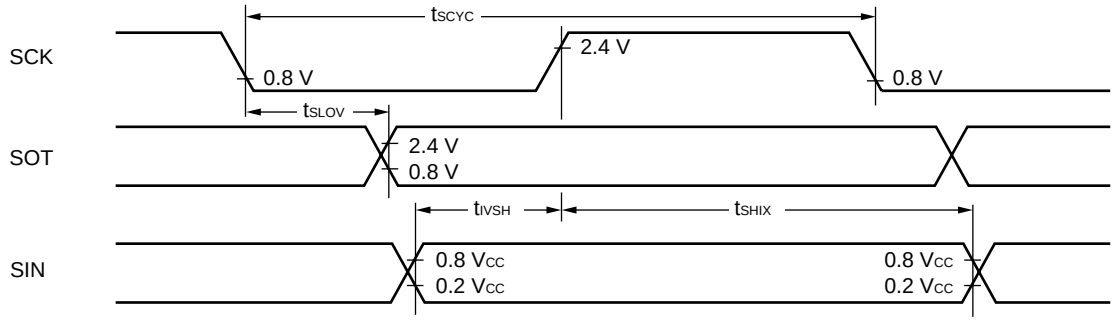
($V_{CC}$ = 2.7 V to 3.6 V, $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Serial clock cycle time | $t_{SCYC}$ | — | $C_L$ = 80 pF + 1 TTL for the internal shift clock mode output pin | 8 $t_{CP}$* | — | ns | |
| SCK ↓ → SOT delay time | $t_{SLOV}$ | — | | –80 | +80 | ns | MASK/FLASH |
| Valid SIN → SCK ↑ | $t_{IVSH}$ | — | | 100 | — | ns | MASK/FLASH |
| SCK ↑ → valid SIN hold time | $t_{SHIX}$ | — | | $t_{CP}$* | — | ns | |
| Serial clock “H” pulse width | $t_{SHSL}$ | — | $C_L$ = 80 pF + 1 TTL for the external shift clock mode output pin | 4 $t_{CP}$* | — | ns | |
| Serial clock “L” pulse width | $t_{SLSH}$ | — | | 4 $t_{CP}$* | — | ns | |
| SCK ↓ → SOT delay time | $t_{SLOV}$ | — | | — | 150 | ns | MASK/FLASH |
| Valid SIN → SCK ↑ | $t_{IVSH}$ | — | | 60 | — | ns | MASK/FLASH |
| SCK ↑ → valid SIN hold time | $t_{SHIX}$ | — | | 60 | — | ns | MASK/FLASH |

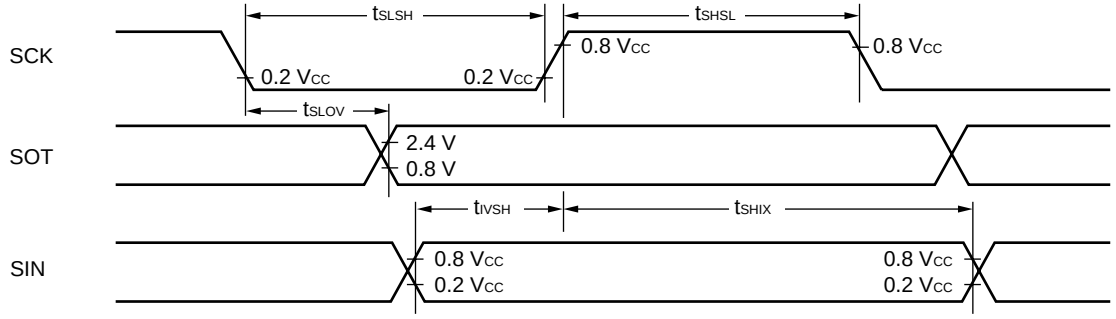
* : For $t_{CP}$ see “(1) Clock Timing.”

Notes: • These are the AC characteristics for CLK synchronous mode.
• $C_L$ is the load capacitance connected to the pin at testing.
• $V_{CC}$ = $V_{CC}1$ = $V_{CC}2$

• **Internal shift clock mode**




• **External shift clock mode**

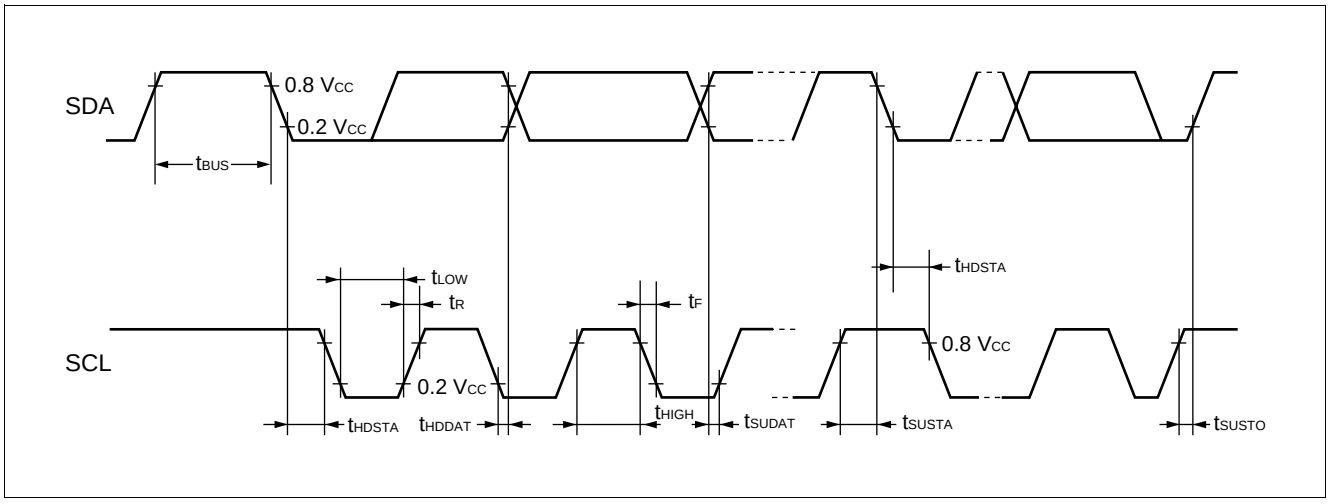


### (11) I²C Timing

($V_{CC}$ = 2.7 V to 3.6 V, $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| SCL clock frequency | $f_{SCL}$ | — | — | 0 | 100 | kHz | |
| Bus free time between stop and start conditions | $t_{BUS}$ | — | — | 4.7 | — | µs | |
| Hold time (re-send) start | $t_{HDSTA}$ | — | — | 4.0 | — | µs | The first clock pulse is generated after this period. |
| SCL clock L state hold time | $t_{LOW}$ | — | — | 4.7 | — | µs | |
| SCL clock H state hold time | $t_{HIGH}$ | — | — | 4.0 | — | µs | |
| Re-send start condition setup time | $t_{SUSTA}$ | — | — | 4.7 | — | µs | |
| Data hold time | $t_{HDDAT}$ | — | — | 0 | — | µs | |
| Data setup time | $t_{SUDAT}$ | — | — | 40 | — | ns | |
| SDA and SCL signal rising time | $t_R$ | — | — | — | 1000 | ns | |
| SDA and SCL signal falling time | $t_F$ | — | — | — | 300 | ns | |
| Stop condition setup time | $t_{SUSTO}$ | — | — | 4.0 | — | µs | |

Note : $V_{CC}$ = $V_{CC}1$ = $V_{CC}2$



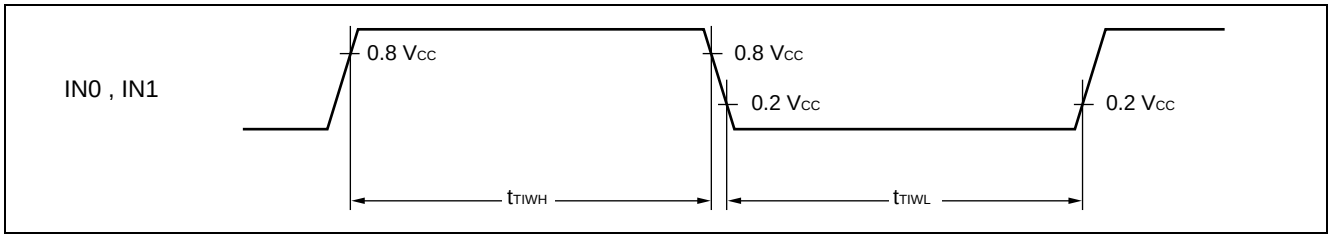
### (12) Timer Input Timing

($V_{CC}$ = 2.7 V to 3.6 V, $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Input pulse width | $t_{TIWH}$, $t_{TIWL}$ | IN0, IN1 | — | 4 $t_{CP}$* | — | ns | |

* : For $t_{CP}$ see “(1) Clock Timing.”

Note : $V_{CC}$ = $V_{CC}1$ = $V_{CC}2$

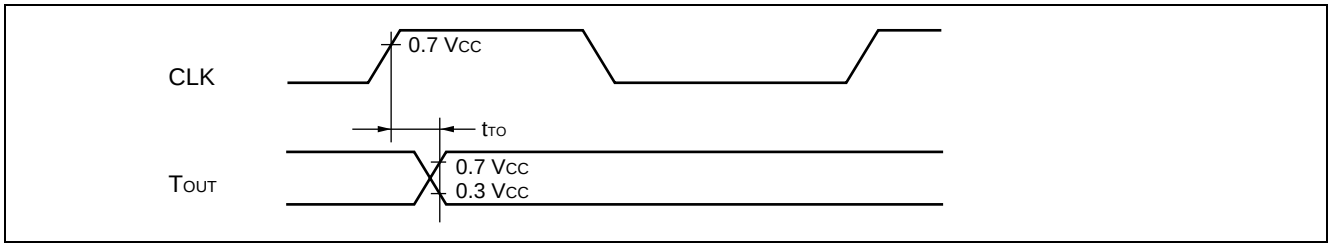



### (13) Timer Output Timing

($V_{CC}$ = 2.7 V to 3.6 V, $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| CLK↑ → $T_{OUT}$ change time | $t_{TO}$ | PPG00 to PPG11<br>OUT0 to OUT3 | 80 pF load | 30 | — | ns | |

Note : $V_{CC}$ = $V_{CC}1$ = $V_{CC}2$



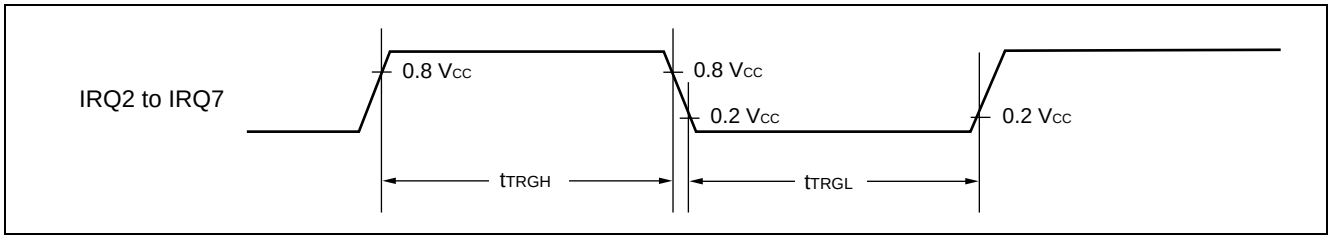

### (14) Trigger Input Timing

($V_{CC}$ = 2.7 V to 3.6 V, $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Input pulse width | $t_{TRGH}$<br>$t_{TRGL}$ | ADTG,<br>IRQ0 to IRQ7 | — | 5 $t_{CP}$* | — | ns | During normal operation |
| | | | | 1 | — | ms | During stop |

* : For $t_{CP}$ see “(1) Clock Timing.”

Note : $V_{CC}$ = $V_{CC}1$ = $V_{CC}2$



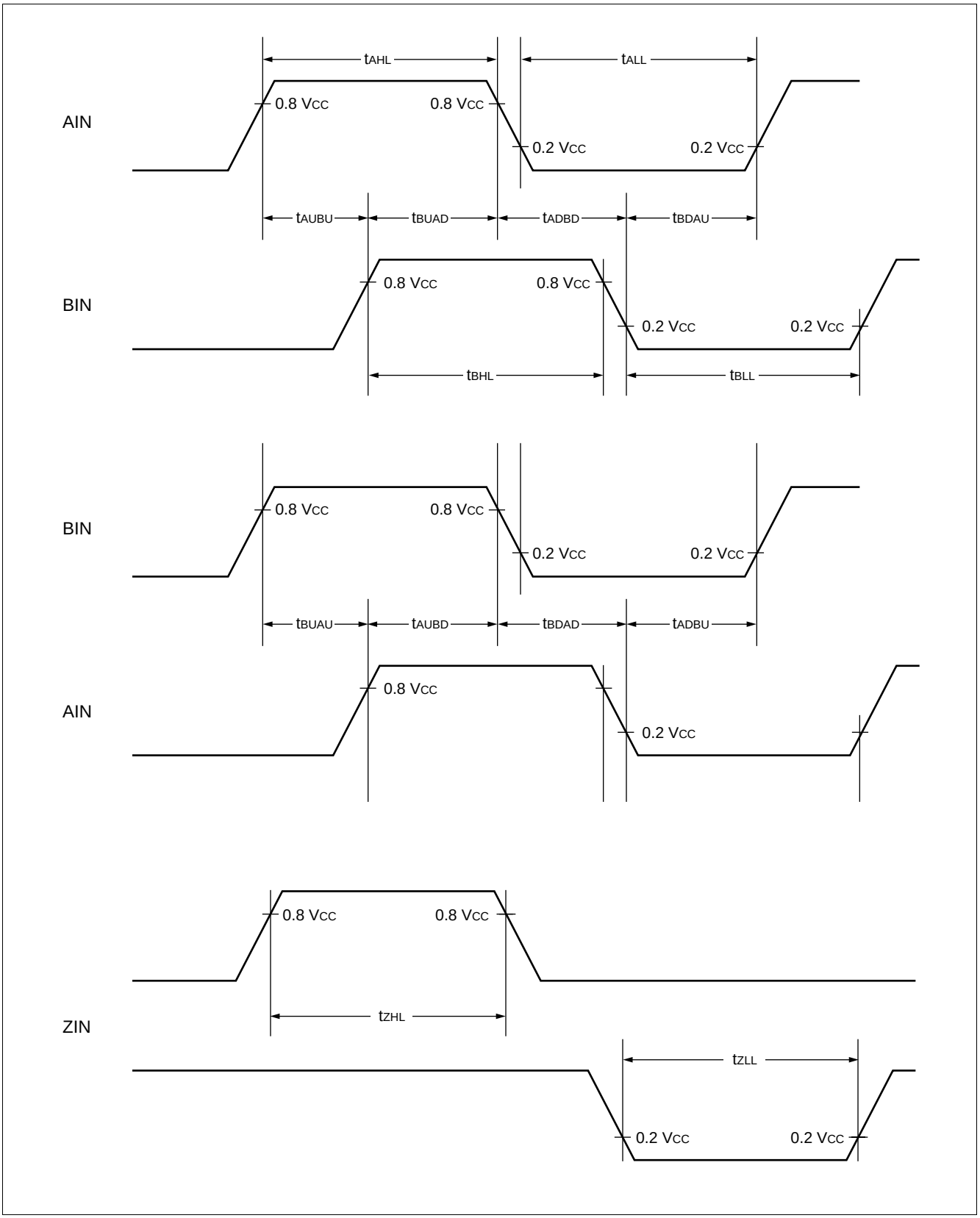
### (15) Up/down Counter Timing

($V_{CC}$ = 2.7 V to 3.6 V, $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| AIN input “H” pulse width | $t_{AHL}$ | AIN0, AIN1<br>BIN0, BIN1 | 80 pF load | 8 $t_{CP}$* | — | ns | |
| AIN input “L” pulse width | $t_{ALL}$ | | | 8 $t_{CP}$* | — | ns | |
| BIN input “H” pulse width | $t_{BHL}$ | | | 8 $t_{CP}$* | — | ns | |
| BIN input “L” pulse width | $t_{BLL}$ | | | 8 $t_{CP}$* | — | ns | |
| AIN↑ → BIN↑ time | $t_{AUBU}$ | | | 4 $t_{CP}$* | — | ns | |
| BIN↑ → AIN↓ time | $t_{BUAD}$ | | | 4 $t_{CP}$* | — | ns | |
| AIN↓ → BIN↑ time | $t_{ADBD}$ | | | 4 $t_{CP}$* | — | ns | |
| BIN↓ → AIN↑ time | $t_{BDAU}$ | | | 4 $t_{CP}$* | — | ns | |
| BIN↑ → AIN↑ time | $t_{BUAU}$ | | | 4 $t_{CP}$* | — | ns | |
| AIN↑ → BIN↓ time | $t_{AUBD}$ | | | 4 $t_{CP}$* | — | ns | |
| BIN↓ → AIN↑ time | $t_{BDAD}$ | | | 4 $t_{CP}$* | — | ns | |
| AIN↓ → BIN↑ time | $t_{ADBU}$ | | | 4 $t_{CP}$* | — | ns | |
| ZIN input “H” pulse width | $t_{ZHL}$ | ZIN0, ZIN1 | | 4 $t_{CP}$* | — | ns | |
| ZIN input “L” pulse width | $t_{ZLL}$ | | | 4 $t_{CP}$* | — | ns | |

* : For $t_{CP}$ see “(1) Clock Timing.”

Note : $V_{CC}$ = $V_{CC}1$ = $V_{CC}2$



## 5. A/D Converter Electrical Characteristics

(MB90652A/653A/654A: $V_{CC}$ = 2.2 V to 3.6 V, $V_{SS}$ = $AV_{SS}$ =0.0V, 2.7 V ≤ AVRH – AVRL, $T_A$ = –40°C to +85°C)
(MB90F654A: $V_{CC}$ = 2.4 V to 3.6 V, $V_{SS}$ = $AV_{SS}$ = 0.0 V, 2.7 V ≤ AVRH – AVRL, $T_A$ = –40°C to +85°C)

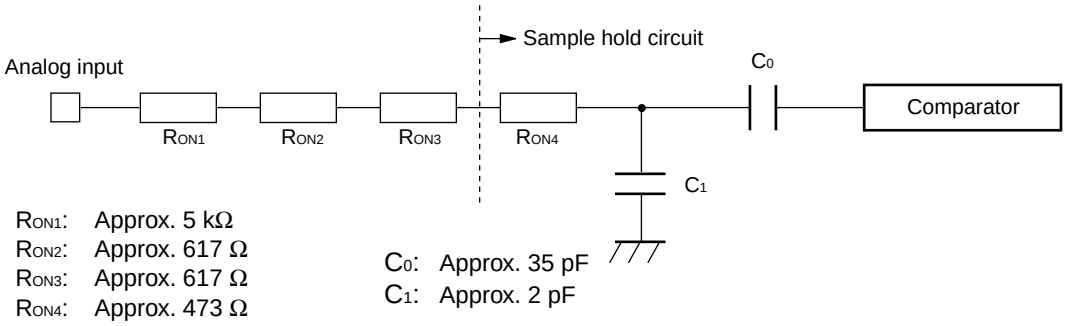
| Parameter | Symbol | Pin name | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Resolution | — | — | — | 10 | 10 | bit | |
| Total error | — | — | — | — | ±3.0 | LSB | |
| Linearity error | — | — | — | — | ±2.0 | LSB | |
| Differential linearity error | — | — | — | — | ±1.9 | LSB | MASK/FLASH |
| Zero transition voltage | $V_{OT}$ | AN0 to AN7 | AVRL – 1.5 LSB | AVRL + 0.5 LSB | AVRL + 2.5 LSB | mV | |
| Full scale transition voltage | $V_{FST}$ | AN0 to AN7 | AVRH – 4.5 LSB | AVRH – 1.5 LSB | AVRH + 0.5 LSB | mV | |
| Conversion time | — | — | 8.167*1 | — | — | µs | MASK/FLASH |
| Analog port input current | $I_{AIN}$ | AN0 to AN7 | — | 0.1 | 10 | µA | |
| Analog input voltage | $V_{AIN}$ | AN0 to AN7 | AVRL | — | AVRH | V | |
| Reference voltage | — | AVRH | AVRL + 2.7 | — | $AV_{CC}$ | V | |
| | | AVRL | 0 | — | AVRH – 2.7 | V | |
| Power supply current | $I_A$ | $AV_{CC}$ | — | 3 | — | mA | |
| | $I_{AH}$ | $AV_{CC}$ | — | — | 5*2 | µA | |
| Reference voltage supply current | $I_R$ | AVRH | — | 200 | — | µA | |
| | $I_{RH}$ | AVRH | — | — | 5*2 | µA | |
| Variation between channels | — | AN0 to AN7 | — | — | 4 | LSB | |

*1: For a 12 MHz machine clock

*2: The current when the A/D converter is not operating or the CPU is in stop mode (for $V_{CC}$ = $AV_{CC}$ = AVRH = 3.0 V).

Notes:
- The error increases proportionally as |AVRH – AVRL| decreases.
- The output impedance of the external circuits connected to the analog inputs should be in the following range.
  The output impedance of the external circuit should be less than approximately 7 kΩ.
  When using an external capacitor, it is recommended to have several thousand times the capacitance of the internal capacitor as a guide, if one takes into consideration the effect of the divided capacitance between the external capacitor and the internal capacitor.
- If the output impedance of the external circuit is too high, the sampling time might be insufficient (sampling time = 3.75 µs at a machine clock of 16 MHz).
- $V_{CC}$ = $V_{CC}1$ = $V_{CC}2$

• **Analog input circuit model diagram**




$R_{ON1}$: Approx. 5 kΩ
$R_{ON2}$: Approx. 617 Ω
$R_{ON3}$: Approx. 617 Ω
$R_{ON4}$: Approx. 473 Ω

$C_0$: Approx. 35 pF
$C_1$: Approx. 2 pF

Note : Use the values shown as guides only.

## 6. D/A Converter Electrical Characteristics

(MB90652A/653A: $V_{CC}$ = 2.2 V to 3.6 V, $V_{SS}$ = $DV_{SS}$ = 0.0 V, 2.2 V ≤ DVRH – $DV_{SS}$, $T_A$ = –40°C to +85°C)

(MB90F654A: $V_{CC}$ = 2.4 V to 3.6 V, $V_{SS}$ = $DV_{SS}$ = 0.0 V, 2.4 V ≤ DVRH – $DV_{SS}$, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin name | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Resolution | — | — | — | 8 | 8 | bit | |
| Differential linearity error | — | — | — | — | ±0.9 | LSB | |
| Absolute accuracy | — | — | — | — | 1 | % | |
| Linearity error | — | — | — | — | ±1.5 | LSB | |
| Conversion time | — | — | — | 10.0 | 20.0 | µs | *1 |
| Analog reference power supply voltage | — | DVRH | 2.2 | — | $V_{CC}$ | V | MB90652A/653A/654A*2 |
| | | | 2.4 | — | $V_{CC}$ | V | MB90F654A *2 |
| Reference voltage supply current | $I_{DVR}$ | DVRH | — | 100 | — | µA | *3 |
| | $I_{DVRS}$ | | — | — | 5 | µA | *4 |
| Analog output impedance | — | — | — | 28 | — | kΩ | |

*1: Conversion time is the value at the load capacitance = 20 pF.

*2: DVRH – $DV_{SS}$ ($AV_{SS}$)

*3: Current value at conversion

*4: Current value when stopped

Note : $V_{CC}$ = $V_{CC}1$ = $V_{CC}2$

## 7. DTMF Electrical characteristics

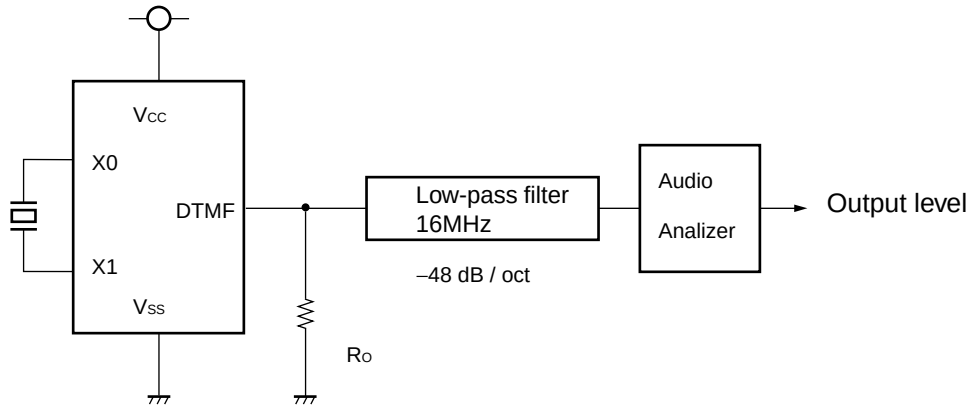
(MB90652A/653A: $V_{CC}$ = 2.2 V to 3.6 V, $V_{SS}$ = $DV_{SS}$ = 0.0 V, 2.2 V ≤ DVRH – $DV_{SS}$, $T_A$ = –40°C to +85°C)

(MB90F654A: $V_{CC}$ = 2.4 V to 3.6 V, $V_{SS}$ = $DV_{SS}$ = 0.0 V, 2.4 V ≤ DVRH – $DV_{SS}$, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Output load condition | $R_O$ | $V_{CC}$ = 3 V<br>$T_A$ = +25°C<br>Machine clock<br>f = 12 MHz | 30 k | — | — | Ω | To be specified with DTMF pin pull-down resistor |
| DTMF output offset voltage (At signal output) | $V_{MOF}$ | | — | 0.4 | — | V | When DTMF terminal is opened<br>$R_O$ = 200 kΩ |
| DTMF output amplitude (COL single tone) | $V_{MFC}$ | | 450 | 530 | 600 | $mV_{P-P}$ | |
| DTMF output amplitude (ROW single tone) | $V_{MFOR}$ | | 330 | 440 | 500 | $mV_{P-P}$ | |
| COL/ROW level difference | $R_{MF}$ | | 1.6 | 2.0 | 2.4 | dB | |

Note : $V_{CC}$ =$V_{CC}$1 = $V_{CC}$2

• Output level measurement circuit

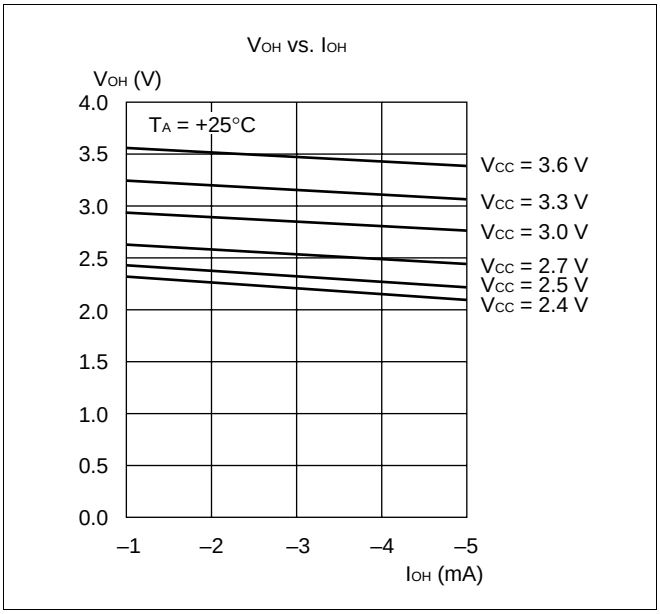


## 8. Flash Memory Programming/Erase Characteristics

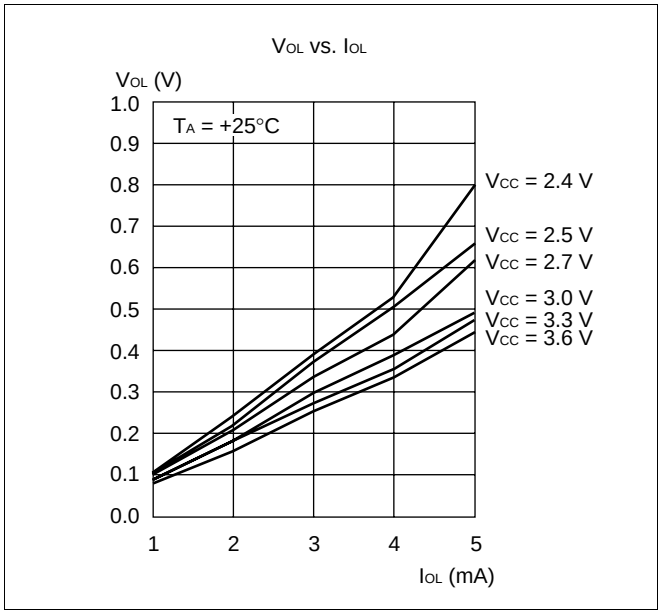
| Parameter | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Sector erase time | $T_A$ = +25 °C<br>$V_{CC}$ = 3.0 V | — | 1 | 15 | s | Excludes $00_H$ programming prior erasure |
| Chip erase time | | — | 7 | — | s | Excludes $00_H$ programming prior erasure |
| Word (16-bit width) programming time | | — | 16 | 3600 | µs | Excludes system-level overhead |
| Program/Erase cycle | — | 10,000 | — | — | cycle | |
| Data holding time | — | 100,000 | — | — | h | |

## ■ EXAMPLE CHARACTERISTICS

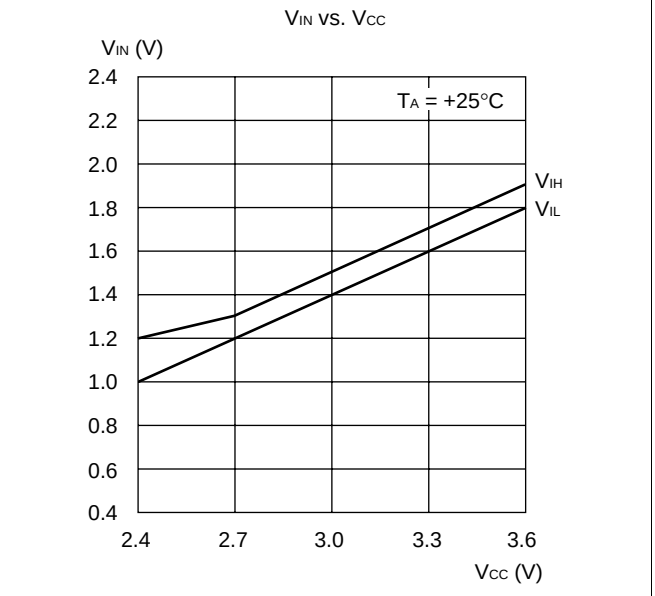
### (1) “H” Level Output Voltage




### (2) “L” Level Output Voltage



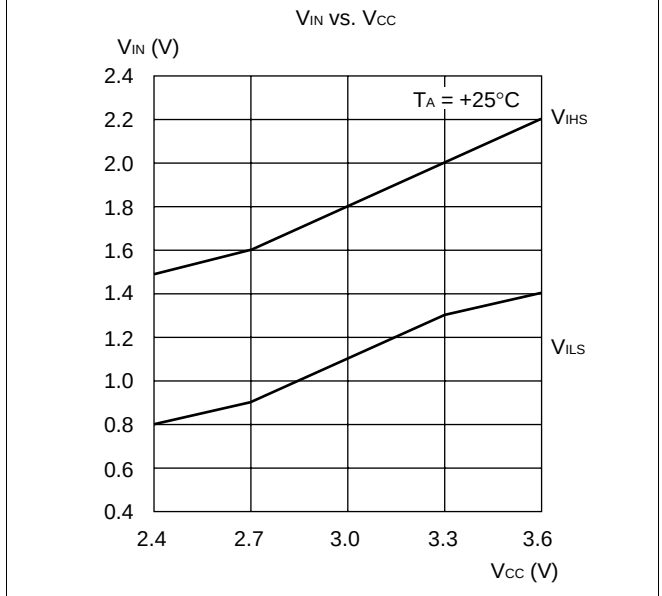

### (3) “H” Level Input Voltage/“L” Level Input Voltage (COMS Input)




$V_{IH}$: Threshold when input voltage is set to “H” level

$V_{IL}$: Threshold when input voltage is set to “L” level

### (4) “H” Level Input Voltage/“L” Level Input Voltage (Hysteresis Input)

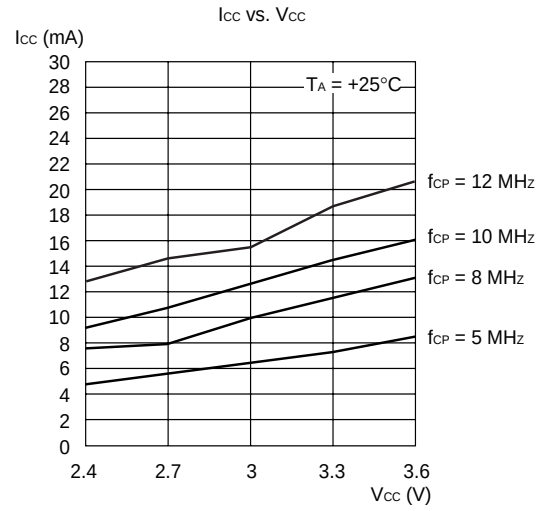


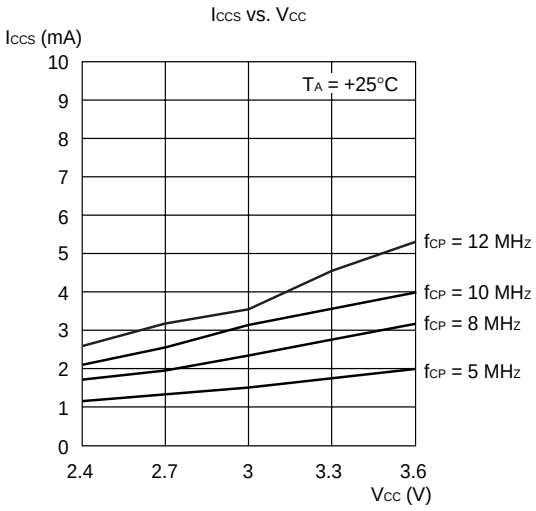

$V_{IHS}$: Threshold when input voltage in hysteresis characteristics is set to “H” level

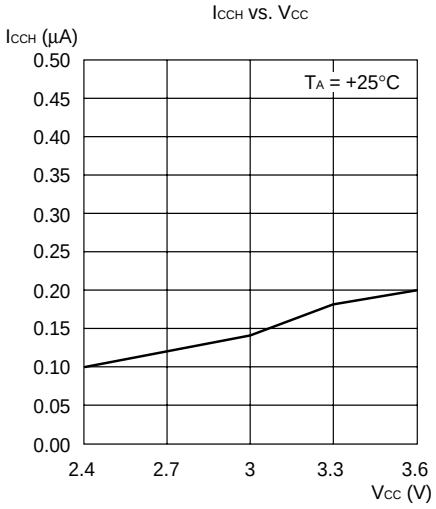
$V_{ILS}$: Threshold when input voltage in hysteresis characteristics is set to “L” level

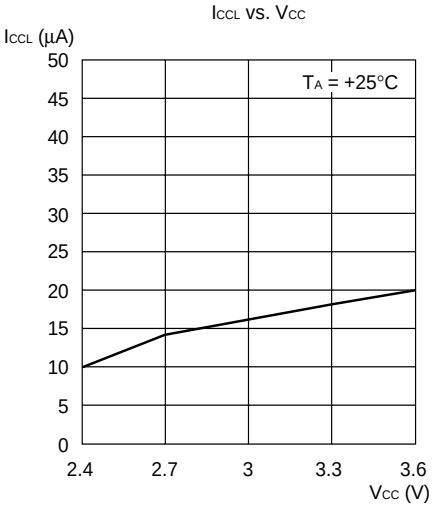
### (5) Power Supply Current ($f_{CP}$ = Internal Operating Clock Frequency)

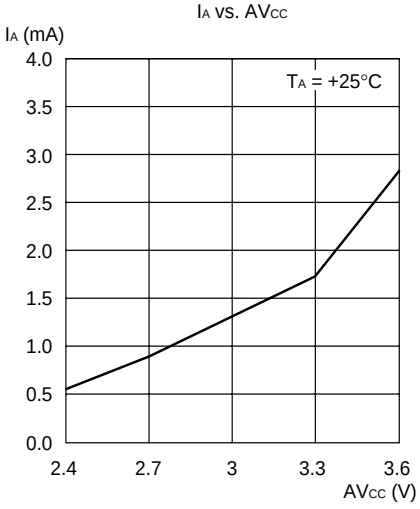
- **Mask ROM products**

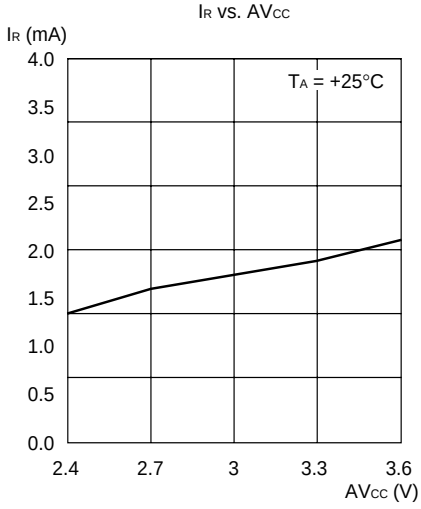


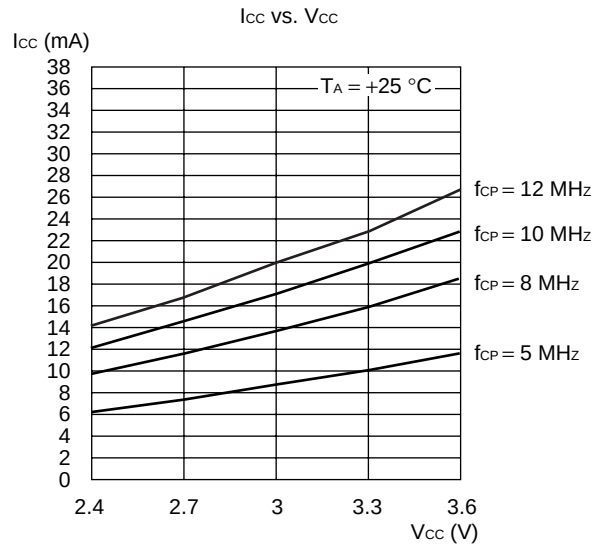



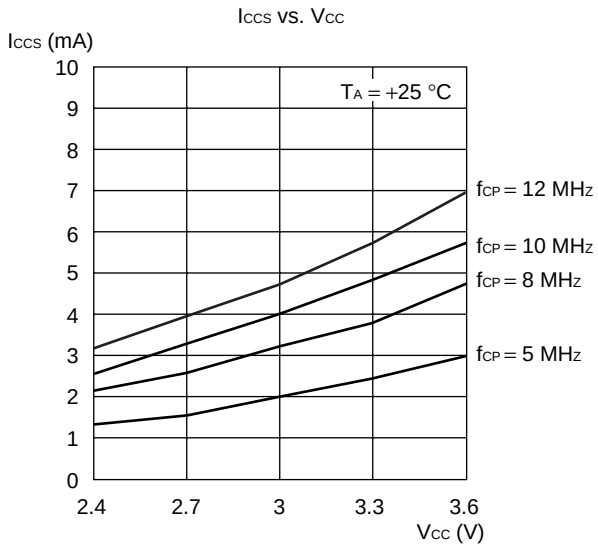



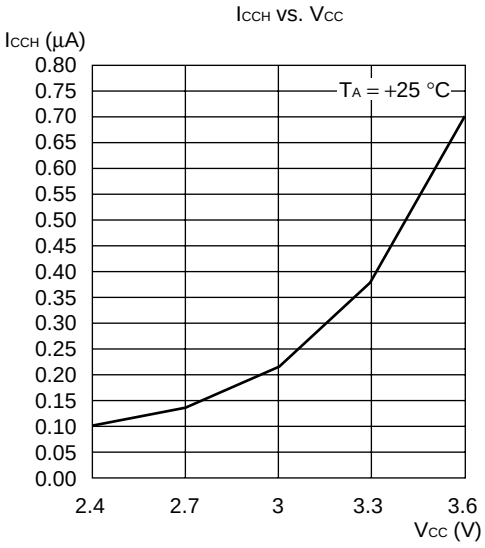



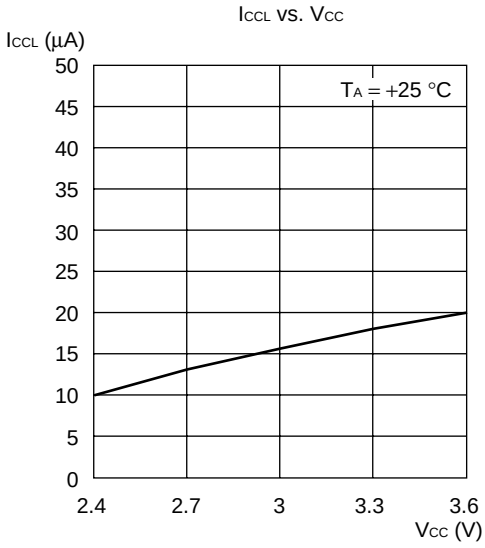



- **FLASH products**



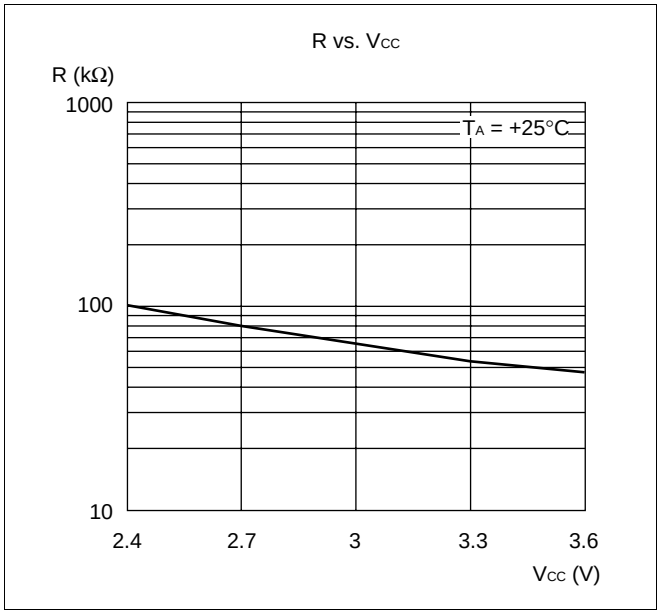



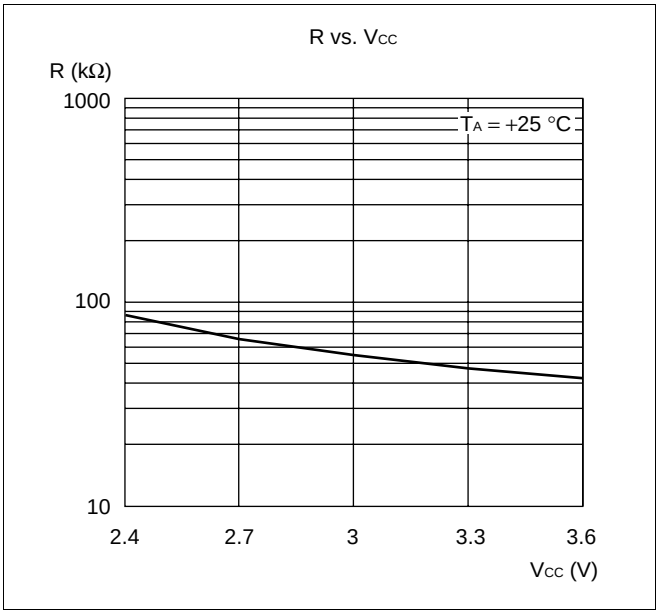



### (6) Pull-up Resistance

- **Mask ROM products**




- **FLASH products**

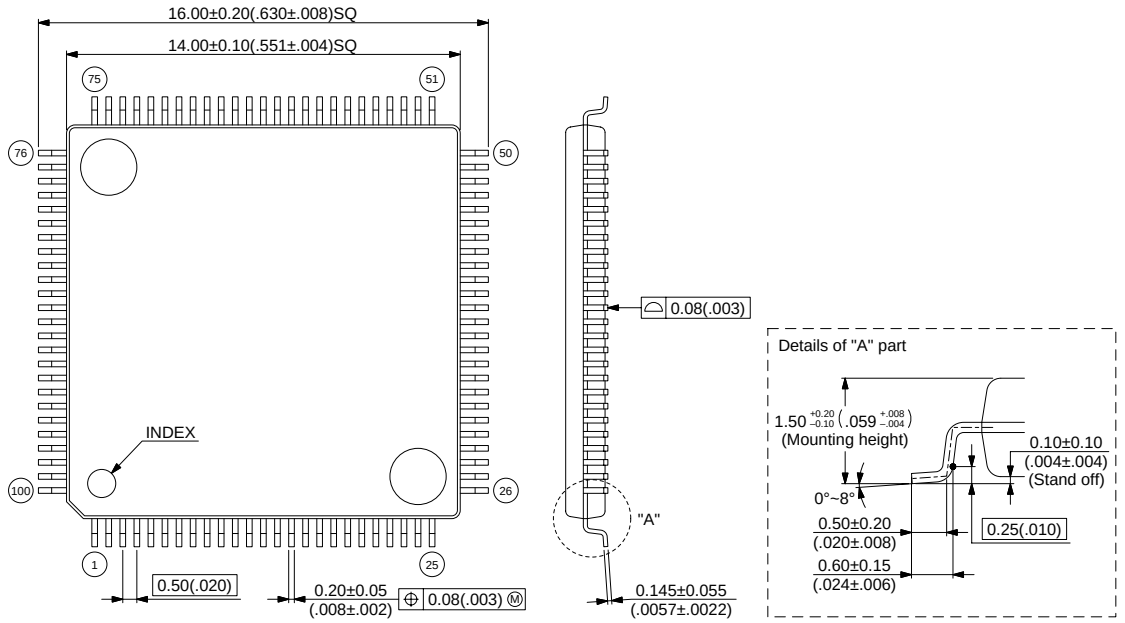


## ■ ORDERING INFORMATION

| Part number | Package | Remarks |
|---|---|---|
| MB90652APFV<br>MB90653APFV<br>MB90654APFV<br>MB90F654APFV | 100-pin plastic LQFP<br>(FPT-100P-M05) | |
| MB90652APF<br>MB90653APF<br>MB90654APF<br>MB90F654APF | 100-pin plastic QFP<br>(FPT-100P-M06) | |

## ■ PACKAGE DIMENSIONS

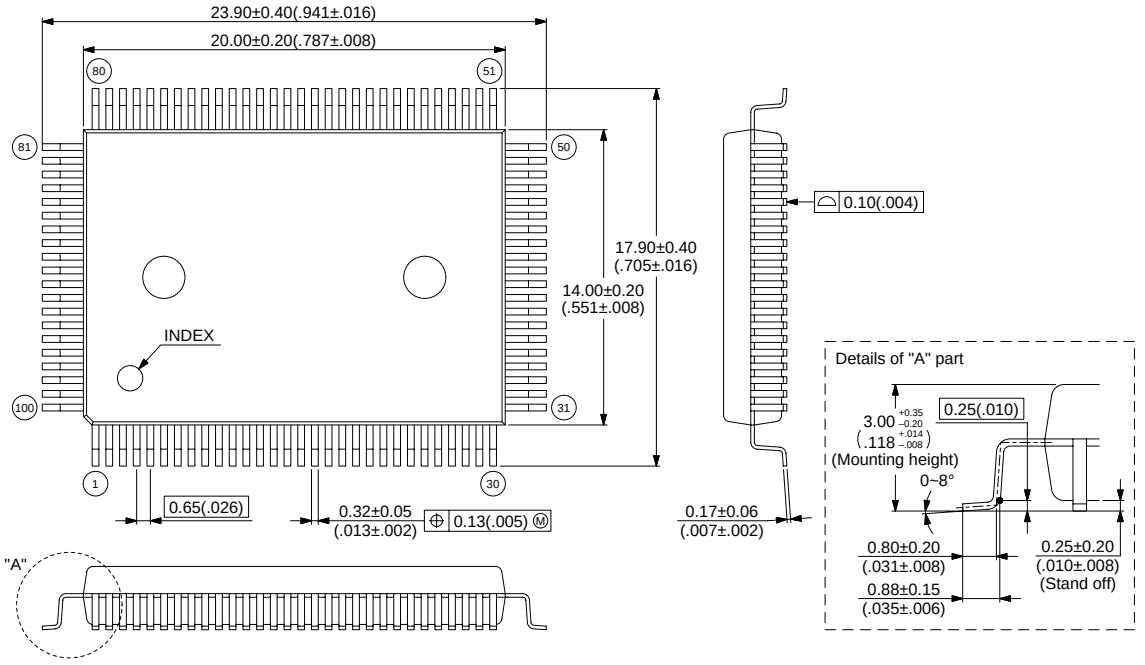
100-pin plastic LQFP
(FPT-100P-M05)




Dimensions in mm (inches)



100-pin plastic QFP
(FPT-100P-M06)




Dimensions in mm (inches)

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