FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-12630-1E

8-bit Proprietary Microcontrollers

CMOS

F²MC-8FX MB95R203A

MB95R203A

■ DESCRIPTION

The MB95R203A is general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers contain a variety of peripheral functions.

Note : F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

■ FEATURES

- F²MC-8FX CPU core
  Instruction set optimized for controllers
  - Multiplication and division instructions
  - 16-bit arithmetic operations
  - Bit test branch instruction
  - Bit manipulation instructions etc.
- Clock
  - Selectable Main clock source
    Main OSC clock (Up to 10 MHz, Maximum Machine clock frequency is 5 MHz)
    External clock (Up to 20 MHz, Maximum Machine clock frequency is 10 MHz)
    Internal main CR clock (Typ 1/8 MHz, Maximum Machine clock frequency is 8 MHz)
  - Selectable Sub clock source
    Sub OSC clock (32 kHz)
    Sub internal CR clock (Typ : 100 kHz, Min : 50 kHz, Max : 200 kHz)

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- Timer
  - 8/16-bit compound timer
  - Time-base timer
  - Watch prescaler
- UART/SIO
  - Offers clock asynchronous (UART) or clock synchronous (SIO) serial data transfer
  - Full duplex double buffer
- I^2C
  - Built-in wake-up function
- External interrupt
  - Interrupt by the edge detection (Select rising edge/falling edge/both edges)
  - Can be used to recover from low-power consumption modes (also called standby mode)
- 8/10-bit A/D converter
  - 8-bit or 10-bit resolutions can be selected
- Low-power consumption (standby) mode
  - Stop mode
  - Sleep mode
  - Watch mode
  - Time-base timer mode
- I/O port : 16
  - General-purpose I/O ports :
    CMOS I/O : 12, N-ch open drain : 4
- On-chip debug
  - 1 wire serial control
  - Support serial writing. (Asynchronous mode)
- Hardware/Software watch dog timer
  - Built-in Hardware watchdog timer
- Low voltage detection circuit (LVD)
  - Low voltage detection reset circuit
  - Low voltage detection interrupt circuit
  - Circuit to monitor FRAM power supply
- Clock supervisor counter (CSV)
  - Built-in Clock supervise function
- Programmable input voltage levels of port
  - CMOS input level / hysteresis input level
- FRAM
  - Non-volatile memory
  - 8 Kbytes of FRAM integrated on-chip
- FRAM memory security function
  - Protects the content of FRAM memory

■ PRODUCT OVERVIEW

Part number / Parameter	MB95R203A
ROM (FRAM) capacity	8 Kbytes
RAM capacity	496 bytes
Reset output	Yes
Low voltage detection reset	Yes
CPU function	Number of basic instructions : 136 instructions Instruction bit length : 8 bits Instruction length : 1 to 3 bytes Data bit length : 1, 8, and 16 bits Minimum instruction execution time : 100 ns (at machine clock 10 MHz) Interrupt processing time : 0.9 µs (at machine clock 10 MHz)
Port	General-purpose I/O ports : 16 CMOS I/O : 12, N-ch open drain : 4
Time-base timer	Interrupt cycle : 0.256 ms to 8.3 s (at external 4 MHz)
Hardware/software Watchdog timer	Reset generation cycle Main clock at 10 MHz : 105 ms (Min) Subclock CR can be used as the Watch dog source clock.
Wild registers	It can be used to replace three bytes of data.
UART/SIO	Able to transfer data using UART/SIO Variable data length (5/6/7/8-bit) , built-in baud rate generator Transfer rate (2400 bps to 125000 bps at 10 MHz) , full-duplex transfers with built-in double buffers NRZ type transfer format, error detection function LSB-first or MSB-first can be selected Capable of clock synchronous (SIO) or clock asynchronous (UART) serial data transfer
I^2C bus	Transmit and receive master/slave Bus function, arbitration function, transfer direction detection function Start condition repeated generation and detection functions Built-in timeout detection function
8/10-bit A/D converter	6 ch
	8-bit or 10-bit resolution can be selected
8/16-bit compound timer	2 ch
	Can be configured as a 2 ch × 8-bit timer or 1 ch × 16-bit timer Built-in timer function, PWC function, PWM function and capture function Count clock : available from internal clocks (7 types) or external clocks With square wave output
External interrupt	6 ch
	Interrupt by edge detection (Select rising edge/falling edge/both edges) Can be used to recover from standby modes
Low voltage interrupt	Selectable from 4 kinds of low voltage detection levels Usable as a release function from standby mode

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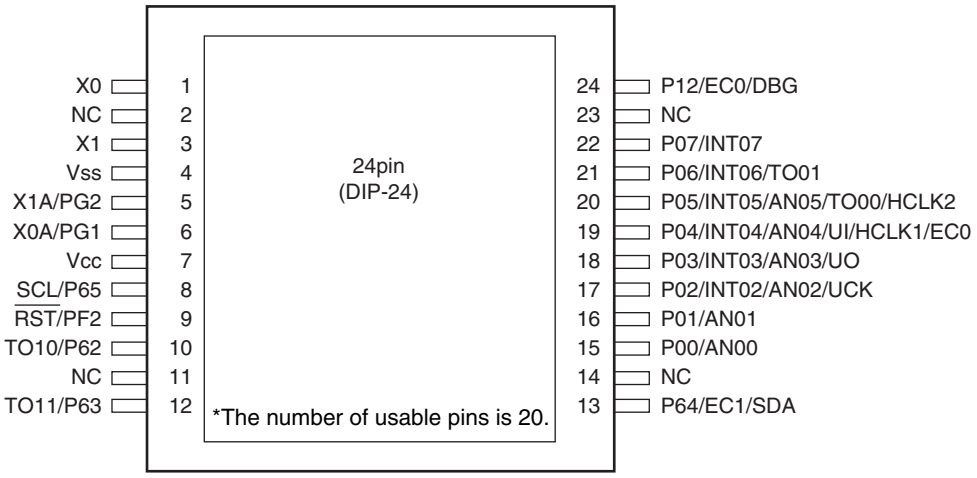
Part number / Parameter	MB95R203A
On-chip debug	1 wire serial control Support serial writing. (Asynchronous mode)
Watch prescaler	Eight different time intervals can be selected.
FRAM	Non-volatile memory Number of read/write cycles : 10^{15} times Data retention characteristics : 10 years (+ 55 °C) Read security function Function to monitor FRAM power supply
Standby Mode	Sleep mode, Stop mode, Watch mode, time-base timer mode
Package	DIP-24, SOP-20

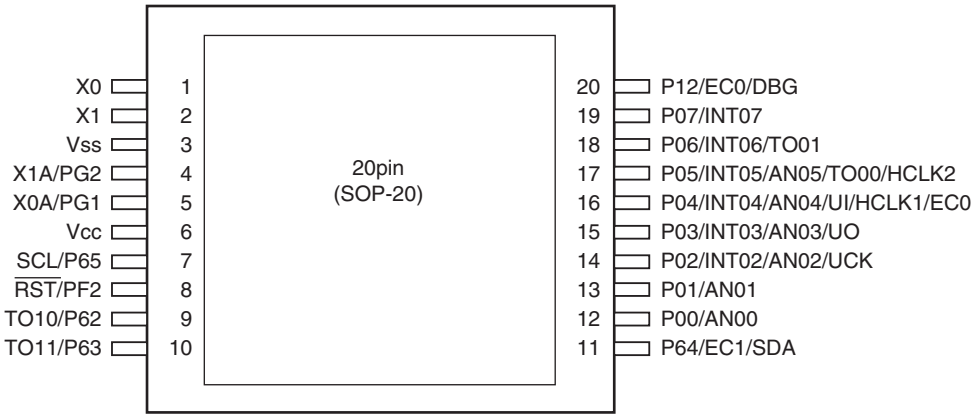
■ PIN ASSIGNMENT

(TOP VIEW)



(DIP-24P-M07)

(TOP VIEW)



(FPT-20P-M09)

■ PIN DESCRIPTION

Pin no.		Pin name	I/O Circuit type*	Function
DIP24	SOP20			
1	1	X0	B	Main clock input oscillation pin
3	2	X1	B	Main clock input/output oscillation pin
4	3	Vss	—	Power supply pin (GND)
5	4	PG2/X1A	C	General-purpose I/O port This pin is also used as Sub clock input/output oscillation pin.
6	5	PG1/X0A	C	General-purpose I/O port This pin is also used as Sub clock input oscillation pin.
7	6	Vcc	—	Power supply pin
8	7	P65/SCL	I	General-purpose I/O port This pin is also used as I²C clock I/O.
9	8	PF2/$\overline{\text{RST}}$	A	General-purpose I/O port This pin is also used as reset pin
10	9	P62/TO10	D	General-purpose I/O port High current port This pin is also used as 8/16-bit compound timer ch.1 output.
12	10	P63/TO11	D	General-purpose I/O port High current port This pin is also used as 8/16-bit compound timer ch.1 output.
13	11	P64/SDA/EC1	I	General-purpose I/O port This pin is also used as I²C data I/O. This pin is also used as 8/16-bit compound timer ch.1 clock input.
15	12	P00/AN00	E	General-purpose I/O port This pin is also used as A/D converter analog input.
16	13	P01/AN01	E	General-purpose I/O port This pin is also used as A/D converter analog input.
17	14	P02/INT02/AN02/ UCK	E	General-purpose I/O port This pin is also used as external interrupt input. This pin is also used as A/D converter analog input. This pin is also used as UART/SIO clock I/O.
18	15	P03/INT03/AN03/ UO	E	General-purpose I/O port This pin is also used as external interrupt input. This pin is also used as A/D converter analog input. This pin is also used as UART/SIO data output.
19	16	P04/INT04/AN04/ UI/HCLK1/EC0	F	General-purpose I/O port This pin is also used as external interrupt input. This pin is also used as A/D converter analog input. This pin is also used as UART/SIO data input. This pin is also used as 8/16-bit compound timer ch.0 clock input.

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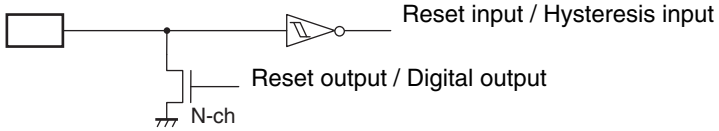
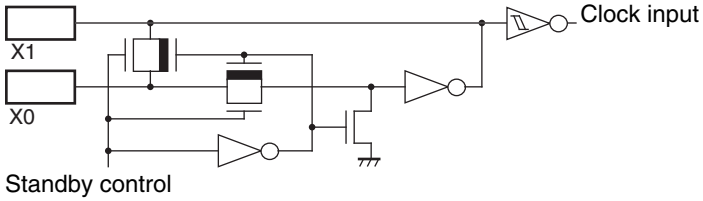
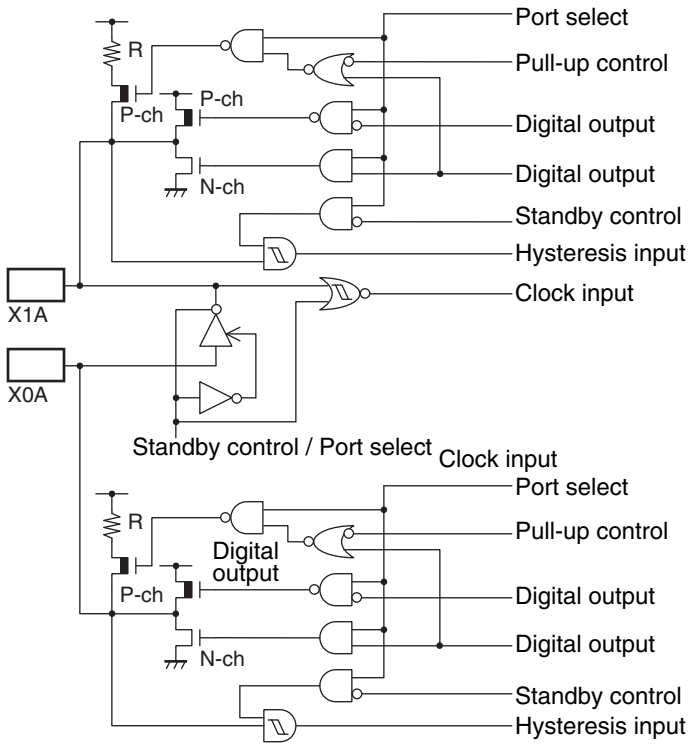
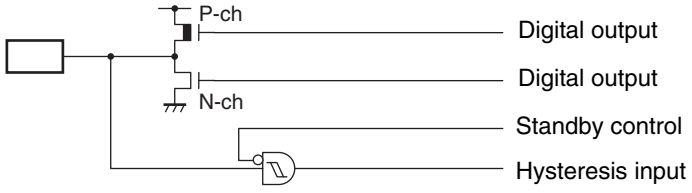
Pin no.		Pin name	I/O Circuit type*	Function
DIP24	SOP20			
20	17	P05/INT05/AN05/ TO00/HCLK2	E	General-purpose I/O port High current port This pin is also used as external interrupt input. This pin is also used as A/D converter analog input. The pins are also used as 8/16-bit compound timer ch.0 output. This pin is also used as the external clock input.
21	18	P06/INT06/TO01	G	General-purpose I/O port High current port This pin is also used as external interrupt input. This pin is also used as 8/16-bit compound timer ch.0 output.
22	19	P07/INT07	G	General-purpose I/O port This pin is also used as external interrupt input.
24	20	P12/EC0/DBG	H	General-purpose I/O port This pin is also used as DBG input pin. This pin is also used as 8/16-bit compound timer ch.0 clock input.
2, 11, 14, 23	—	NC	—	Internal connect pin. Be sure this pin is left open.

* : For the I/O circuit type, refer to “■ I/O CIRCUIT TYPE”.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• N-ch open drain output • Hysteresis input • Reset output
B		• Oscillation circuit • High-speed side Feedback resistance : approx. 1 MΩ • Hysteresis input
C		• Oscillation circuit • Low-speed side Feedback resistance : approx. 10 MΩ • CMOS output • Hysteresis input • With pull-up control
D		• CMOS output • Hysteresis input

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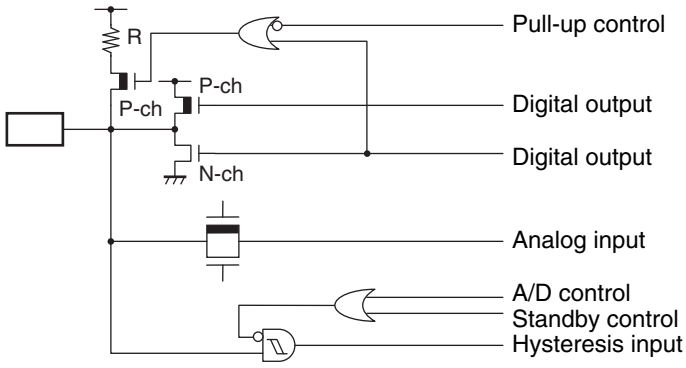
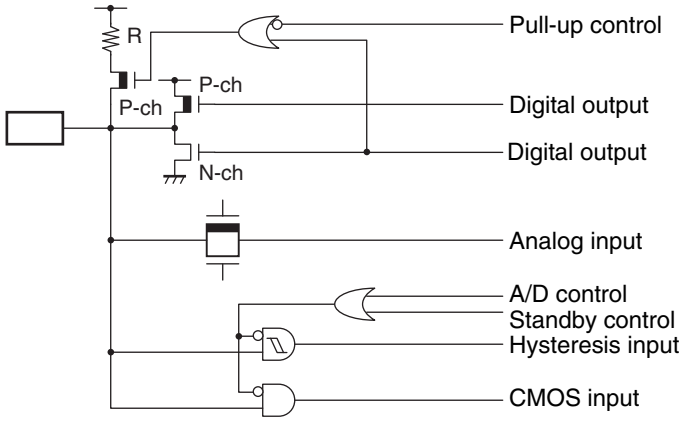
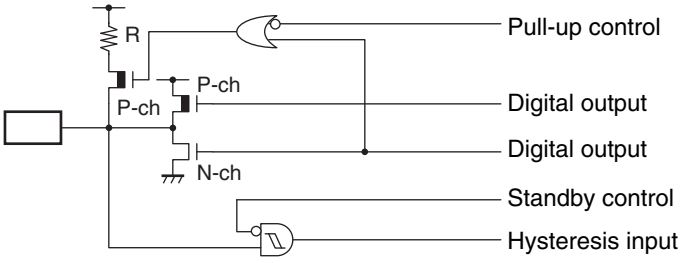
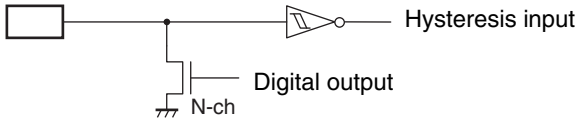
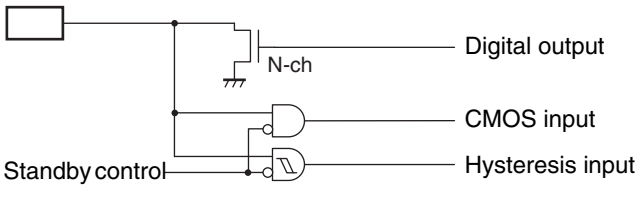
Type	Circuit	Remarks
E		• CMOS output • Hysteresis input • With pull-up control
F		• CMOS output • Hysteresis input • CMOS input • With pull-up control
G		• CMOS output • Hysteresis input • With pull-up control
H		• N-ch open drain output • Hysteresis input
I		• N-ch open drain output • CMOS input • Hysteresis input

■ NOTES ON DEVICE HANDLING

• Preventing Latch-up

Care must be taken to ensure that maximum voltage ratings are not exceeded when they are used.
Latch-up may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- and high-withstand voltage pins or if higher than the rating voltage is applied between V_{CC} pin and V_{SS} pin.
When latch-up occurs, power supply current increases rapidly and might thermally damage elements.

• Stable Supply Voltage

Supply voltage should be stabilized.
A sudden change in power-supply voltage may cause a malfunction even within the guaranteed operating range of the Vcc power-supply voltage.
For stabilization, in principle, keep the variation in Vcc ripple (p-p value) in a commercial frequency range (50 Hz / 60 Hz) not to exceed 10% of the standard Vcc value and suppress the voltage variation so that the transient variation rate does not exceed 0.1 V/ms during a momentary change such as when the power supply is switched.

• Precautions for Use of External Clock

Even when an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from sub clock mode or stop mode.

• Do not use a sample used in program development as mass-produced product.

■ PIN CONNECTION

• Treatment of Unused Input Pin

Leaving unused input pins unconnected can cause abnormal operation or latch-up, leaving to permanent damage. Unused input pins should always be pulled up or down through resistance of at least 2 kΩ. Any unused input/output pins may be set to output mode and left open, or set to input mode and treated the same as unused input pins. If there is unused output pin, make it to open.

• Power Supply Pins

In products with multiple V_{CC} or V_{SS} pins, the pins of the same potential are internally connected in the device to avoid abnormal operations including latch-up. However, you must connect the pins to external power supply and a ground line to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with the V_{CC} and V_{SS} pins of this device at the low impedance. It is also advisable to connect a ceramic bypass capacitor of approximately 0.1 μF between V_{CC} and V_{SS} near this device.

• DBG Pin

Connect the DBG pin directly to external Pull-up.

To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the DBG pin to V_{CC} or V_{SS} pins.

The DBG pin should not stay at “L” level after power-on until the reset output is released.

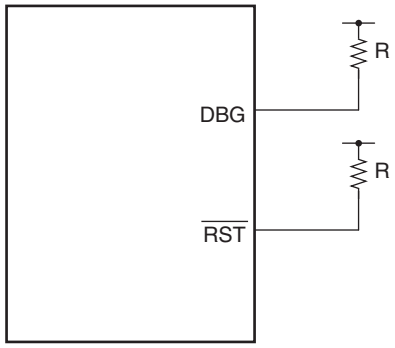
• $\overline{\text{RST}}$ Pin

Connect the $\overline{\text{RST}}$ pin directly to Pull-up.

To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the $\overline{\text{RST}}$ pin to V_{CC} or V_{SS} pins.

The $\overline{\text{RST}}$/PF2 pin functions as the reset input/output pin after power-on. In addition, the reset output can be enabled by the RSTOE bit of the SYSC register, and the reset input function or the general purpose I/O function can be selected by the RSTEN bit of the SYSC register.

• Example of DBG / $\overline{\text{RST}}$ connection diagram



Pull-up resistor recommended resistance
For DBG pin : R = 4.7 kΩ
For $\overline{\text{RST}}$ pin : R = 10 kΩ

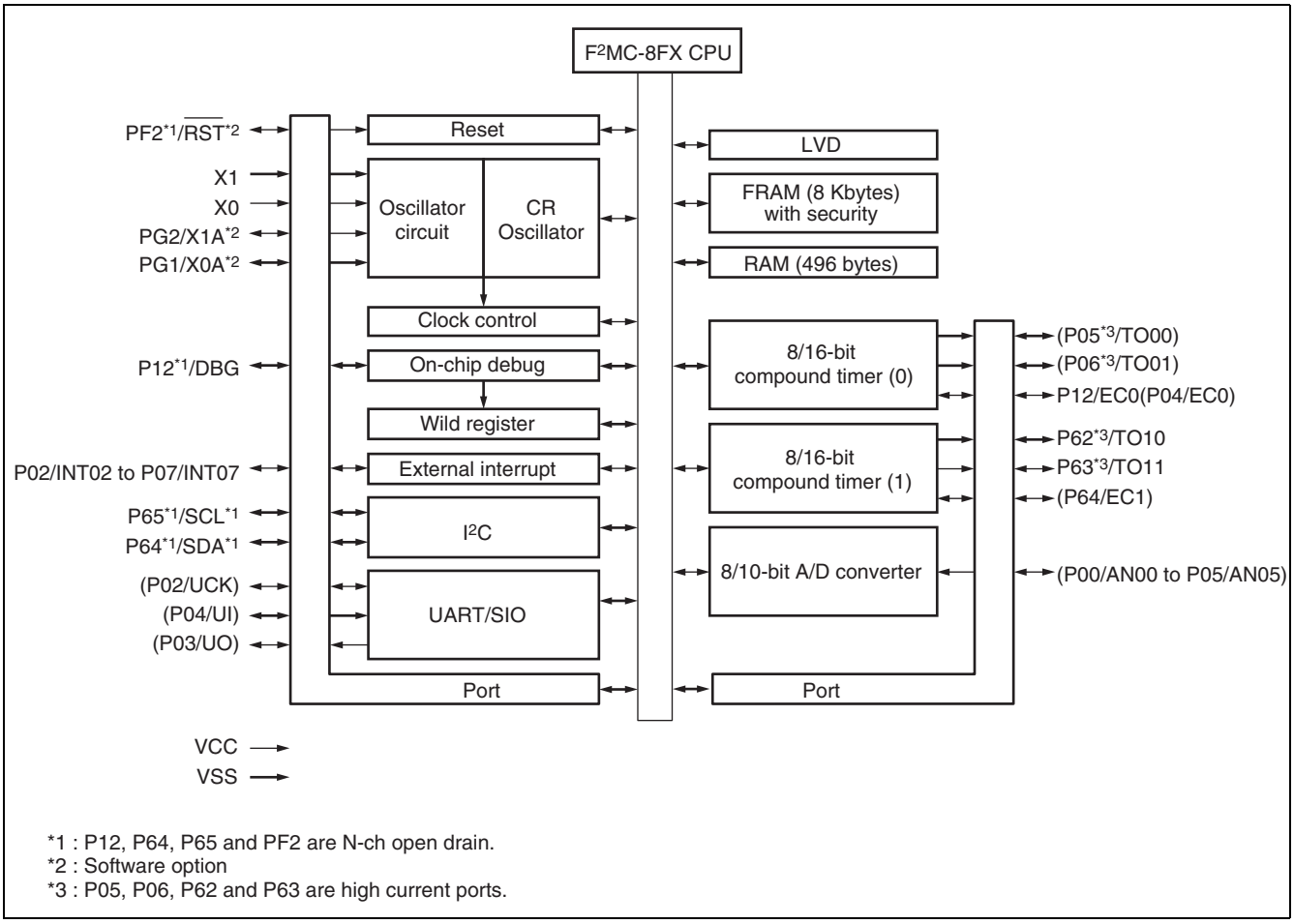
■ NOTES ON DEBUG

- Although the [Upload Flash Memory] button on SOFTUNE Workbench is enabled, clicking it does not start the actual processing.
- When you click on the [Erase Flash Memory] button on SOFTUNE Workbench, data is overwritten into the FRAM area, as shown below.

Address	Data to be overwritten
F554H	55H
FAAAH	A0H
FFBCH	Indeterminate
FFBDH	Indeterminate
Entire FRAM except the above	FFH

- Be very careful not to apply voltages to the pins PF2/$\overline{\text{RST}}$ in excess of the absolute maximum ratings. Especially when handling devices in the environment compatible to the package, such as MB95200H/210H and so on, the voltage may be erroneously applied to the pins PF2/$\overline{\text{RST}}$ in excess of the maximum rating and it may cause thermal breakdown of the device.

■ BLOCK DIAGRAM



*1 : P12, P64, P65 and PF2 are N-ch open drain.
*2 : Software option
*3 : P05, P06, P62 and P63 are high current ports.

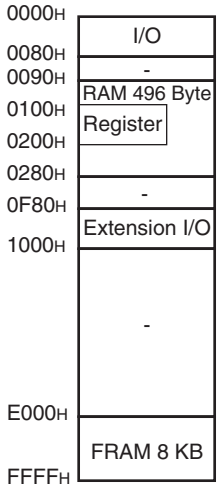
■ CPU CORE

1. Memory space

Memory space of the MB95R203A is 64 Kbytes and consists of I/O area, data area, and program area. The memory space includes special-purpose areas such as the general-purpose registers and vector table. Memory map of the MB95R203A shown below.

• Memory Map

MB95R203A



■ I/O MAP

Address	Register abbreviation	Register name	R/W	Initial value
0000H	PDR0	Port 0 data register	R/W	00000000B
0001H	DDR0	Port 0 direction register	R/W	00000000B
0002H	PDR1	Port 1 data register	R/W	00000000B
0003H	DDR1	Port 1 direction register	R/W	00000000B
0004H	—	(disabled)	—	—
0005H	WATR	Oscillation stabilization wait time setting register	R/W	11111111B
0006H	—	(disabled)	—	—
0007H	SYCC	System clock control register	R/W	XXXXXX11B
0008H	STBC	Standby control register	R/W	00000XXXB
0009H	RSRR	Reset source register	R	XXXXXXXXB
000AH	TBTC	Time-base timer control register	R/W	00000000B
000BH	WPCR	Watch timer control register	R/W	00000000B
000CH	WDTC	Watchdog timer control register	R/W	00000000B
000DH	SYCC2	System clock control register 2	R/W	XX100011B
000EH to 0015H	—	(disabled)	—	—
0016H	PDR6	Port 6 data register	R/W	00000000B
0017H	DDR6	Port 6 direction register	R/W	00000000B
0018H to 0027H	—	(disabled)	—	—
0028H	PDRF	Port F data register	R/W	00000000B
0029H	DDRF	Port F direction register	R/W	00000000B
002AH	PDRG	Port G data register	R/W	00000000B
002BH	DDRG	Port G direction register	R/W	00000000B
002CH	PUL0	Port 0 pull-up register	R/W	00000000B
002DH to 0034H	—	(disabled)	—	—
0035H	PULG	Port G pull-up register	R/W	00000000B
0036H	T01CR1	8/16-bit compound timer 01 control status register 1 ch.0	R/W	00000000B
0037H	T00CR1	8/16-bit compound timer 00 control status register 1 ch.0	R/W	00000000B
0038H	T11CR1	8/16-bit compound timer 11 control status register 1 ch.1	R/W	00000000B
0039H	T10CR1	8/16-bit compound timer 10 control status register 1 ch.1	R/W	00000000B

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Address	Register abbreviation	Register name	R/W	Initial value
003A$_H$ to 0046$_H$	—	(disabled)	—	—
0047$_H$	LVDCR	Low voltage detection interrupt control register	R/W	00000000$_B$
0048$_H$	—	(disabled)	—	—
0049$_H$	EIC10	External interrupt circuit control register ch.2/ch.3	R/W	00000000$_B$
004A$_H$	EIC20	External interrupt circuit control register ch.4/ch.5	R/W	00000000$_B$
004B$_H$	EIC30	External interrupt circuit control register ch.6/ch.7	R/W	00000000$_B$
004C$_H$ to 0055$_H$	—	(disabled)	—	—
0056$_H$	SMC10	UART/SIO serial mode control register 1	R/W	00000000$_B$
0057$_H$	SMC20	UART/SIO serial mode control register 2	R/W	00100000$_B$
0058$_H$	SSR0	UART/SIO serial status and data register	R/W	00000001$_B$
0059$_H$	TDR0	UART/SIO serial output data register	R/W	00000000$_B$
005A$_H$	TDR0	UART/SIO serial input data register	R/W	00000000$_B$
005B$_H$ to 005F$_H$	—	(disabled)	—	—
0060$_H$	IBCR00	I^{2}C bus control register 0	R/W	00000000$_B$
0061$_H$	IBCR10	I^{2}C bus control register 1	R/W	00000000$_B$
0062$_H$	IBSR0	I^{2}C bus status register	R/W	00000000$_B$
0063$_H$	IDDR0	I^{2}C data register	R/W	00000000$_B$
0064$_H$	IAAR0	I^{2}C address register	R/W	00000000$_B$
0065$_H$	ICCR0	I^{2}C clock control register	R/W	00000000$_B$
0066$_H$	FSCR	FRAM status/control register	R/W	00000000$_B$
0067$_H$	FRAC	FRAM register access control register	R/W	00000000$_B$
0068$_H$	FABH	FRAM write permit start address register (H)	R/W	11111111$_B$
0069$_H$	FABL	FRAM write permit start address register (L)	R/W	11111111$_B$
006A$_H$	FASH	FRAM write permit area size register (H)	R/W	00000000$_B$
006B$_H$	FASL	FRAM write permit area size register (L)	R/W	00000000$_B$
006C$_H$	ADC1	8/10-bit A/D converter control register 1	R/W	00000000$_B$
006D$_H$	ADC2	8/10-bit A/D converter control register 2	R/W	00000000$_B$
006E$_H$	ADDH	8/10-bit A/D converter data register (upper byte)	R/W	00000000$_B$
006F$_H$	ADDL	8/10-bit A/D converter data register (lower byte)	R/W	00000000$_B$
0070$_H$	FVAH	FRAM violation address register (H)	R	XXXXXXXX$_B$
0071$_H$	FVAL	FRAM violation address register (L)	R	XXXXXXXX$_B$

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0072H to 0075H	—	(disabled)	—	—
0076H	WREN	Wild register address compare enable register	R/W	00000000B
0077H	WROR	Wild register data test setting register	R/W	00000000B
0078H	—	Register bank pointer (RP) , Mirror of direct bank pointer (DP)	—	—
0079H	ILR0	Interrupt level setting register 0	R/W	11111111B
007AH	ILR1	Interrupt level setting register 1	R/W	11111111B
007BH	ILR2	Interrupt level setting register 2	R/W	11111111B
007CH	ILR3	Interrupt level setting register 3	R/W	11111111B
007DH	ILR4	Interrupt level setting register 4	R/W	11111111B
007EH	ILR5	Interrupt level setting register 5	R/W	11111111B
007FH	—	(disabled)	—	—
0F80H	WRARH0	Wild register address setting register (upper byte) ch.0	R/W	00000000B
0F81H	WRARL0	Wild register address setting register (lower byte) ch.0	R/W	00000000B
0F82H	WRDR0	Wild register data setting register ch.0	R/W	00000000B
0F83H	WRARH1	Wild register address setting register (upper byte) ch.1	R/W	00000000B
0F84H	WRARL1	Wild register address setting register (lower byte) ch.1	R/W	00000000B
0F85H	WRDR1	Wild register data setting register ch.1	R/W	00000000B
0F86H	WRARH2	Wild register address setting register (upper byte) ch.2	R/W	00000000B
0F87H	WRARL2	Wild register address setting register (lower byte) ch.2	R/W	00000000B
0F88H	WRDR2	Wild register data setting register ch.2	R/W	00000000B
0F89H to 0F91H	—	(disabled)	—	—
0F92H	T01CR0	8/16-bit compound timer 01 control status register 0 ch.0	R/W	00000000B
0F93H	T00CR0	8/16-bit compound timer 00 control status register 0 ch.0	R/W	00000000B
0F94H	T01DR	8/16-bit compound timer 01 data register ch.0	R/W	00000000B
0F95H	T00DR	8/16-bit compound timer 00 data register ch.0	R/W	00000000B
0F96H	TMCR0	8/16-bit compound timer 00/01 timer mode control register ch.0	R/W	00000000B
0F97H	T11CR0	8/16-bit compound timer 11 control status register 0 ch.1	R/W	00000000B
0F98H	T10CR0	8/16-bit compound timer 10 control status register 0 ch.1	R/W	00000000B

(Continued)

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0F99H	T11DR	8/16-bit compound timer 11 data register ch.1	R/W	00000000B
0F9AH	T10DR	8/16-bit compound timer 10 data register ch.1	R/W	00000000B
0F9BH	TMCR1	8/16-bit compound timer 10/11 timer mode control register ch.1	R/W	00000000B
0F9CH to 0FBDH	—	(disabled)	—	—
0FBEH	PSSR0	UART/SIO prescaler select register	R/W	00000000B
0FBFH	BRSR0	UART/SIO baud rate setting register	R/W	00000000B
0FC0H to 0FC2H	—	(disabled)	—	—
0FC3H	AIDRL	A/D input disable register lower	R/W	00000000B
0FC4H to 0FE3H	—	(disabled)	—	—
0FE4H	CRTH	CR-trimming register upper	R/W	1XXXXXXXB
0FE5H	CRTL	CR-trimming register lower	R/W	000XXXXXB
0FE6H	LVDCR2	Low voltage detection control register	R/W	00000010B
0FE7H	—	(disabled)	—	—
0FE8H	SYSC	System control register	R/W	11000-11B
0FE9H	CMCR	Clock monitor control register	R/W	--000000B
0FEAH	CMDR	Clock monitor data register	R/W	00000000B
0FEBH	WDTH	Watchdog ID register upper	R/W	XXXXXXXXB
0FECH	WDTL	Watchdog ID register lower	R/W	XXXXXXXXB
0FEDH	—	(disabled)	—	—
0FEEH	ILSR	Input level select register	R/W	--00-0--B
0FEFH to 0FFFH	—	(disabled)	—	—

- R/W access symbols
  - R/W : Readable / Writable
  - R : Read only
  - W : Write only

- Initial value symbols
  - 0 : The initial value of this bit is “0”.
  - 1 : The initial value of this bit is “1”.
  - X : The initial value of this bit is undefined.

Note : Do not write to the “ (Disabled) ”. Reading the “ (Disabled) ” returns an undefined value.

■ INTERRUPT SOURCE TABLE

Interrupt source	Interrupt request number	Vector table address		Bit name of interrupt level setting register	Priority order of interrupt sources of the same level (occurring simultaneously)
		Upper	Lower		
External interrupt ch.4	IRQ00	FFFA$_H$	FFFB$_H$	L00 [1 : 0]	High ↑
External interrupt ch.5	IRQ01	FFF8$_H$	FFF9$_H$	L01 [1 : 0]	
External interrupt ch.2	IRQ02	FFF6$_H$	FFF7$_H$	L02 [1 : 0]	
External interrupt ch.6					
External interrupt ch.3	IRQ03	FFF4$_H$	FFF5$_H$	L03 [1 : 0]	
External interrupt ch.7					
UART/SIO (transmit)	IRQ04	FFF2$_H$	FFF3$_H$	L04 [1 : 0]	
UART/SIO (receive)					
8/16-bit compound timer ch.0 (Lower)	IRQ05	FFF0$_H$	FFF1$_H$	L05 [1 : 0]	
8/16-bit compound timer ch.0 (Upper)	IRQ06	FFEE$_H$	FFEF$_H$	L06 [1 : 0]	
—	IRQ07	FFEC$_H$	FFED$_H$	L07 [1 : 0]	
—	RQ08	FFEA$_H$	FFEB$_H$	L08 [1 : 0]	
FRAM (UDEF, PROT)	IRQ09	FFE8$_H$	FFE9$_H$	L09 [1 : 0]	
—	IRQ10	FFE6$_H$	FFE7$_H$	L10 [1 : 0]	
—	IRQ11	FFE4$_H$	FFE5$_H$	L11 [1 : 0]	
—	IRQ12	FFE2$_H$	FFE3$_H$	L12 [1 : 0]	
—	IRQ13	FFE0$_H$	FFE1$_H$	L13 [1 : 0]	
8/16-bit compound timer ch.1 (Upper)	IRQ14	FFDE$_H$	FFDF$_H$	L14 [1 : 0]	
—	IRQ15	FFDC$_H$	FFDD$_H$	L15 [1 : 0]	
I^{2}C complete/error	IRQ16	FFDA$_H$	FFDB$_H$	L16 [1 : 0]	
I^{2}C stop/AL/wakeup					
Low voltage detection interrupt	IRQ17	FFD8$_H$	FFD9$_H$	L17 [1 : 0]	
8/10-bit A/D converter	IRQ18	FFD6$_H$	FFD7$_H$	L18 [1 : 0]	
Time-base timer	IRQ19	FFD4$_H$	FFD5$_H$	L19 [1 : 0]	
Watch prescaler	IRQ20	FFD2$_H$	FFD3$_H$	L20 [1 : 0]	
—	IRQ21	FFD0$_H$	FFD1$_H$	L21 [1 : 0]	
8/16-bit compound timer ch.1 (Lower)	IRQ22	FFCE$_H$	FFCF$_H$	L22 [1 : 0]	
FRAM (AREA)	IRQ23	FFCC$_H$	FFCD$_H$	L23 [1 : 0]	Low ↓

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	Vcc	Vss − 0.3	Vss + 4.0	V	
Input voltage*1	V_I	Vss − 0.3	Vss + 4.0	V	*2
Output voltage*1	V_O	Vss − 0.3	Vss + 4.0	V	*2
"L" level maximum output current	I_{OL1}	—	15	mA	Other than P05, P06, P62 and P63
	I_{OL2}		15		P05, P06, P62 and P63
"L" level average current	I_{OLAV1}	—	4	mA	Other than P05, P06, P62 and P63 Average output current = operating current × operating ratio (1pin)
	I_{OLAV2}		12		P05, P06, P62 and P63 Average output current = operating current × operating ratio (1pin)
"L" level total maximum output current	ΣI_{OL}	—	100	mA	
"L" level total average output current	ΣI_{OLAV}	—	50	mA	Total average output current = operating current × operating ratio (Total of pins)
"H" level maximum output current	I_{OH1}	—	−15	mA	Other than P05, P06, P62 and P63
	I_{OH2}		−15		P05, P06, P62 and P63
"H" level average current	I_{OHAV1}	—	−4	mA	Other than P05, P06, P62 and P63 Average output current = operating current × operating ratio (1 pin)
	I_{OHAV2}		−8		P05, P06, P62 and P63 Average output current = operating current × operating ratio (1pin)
"H" level total maximum output current	ΣI_{OH}	—	−100	mA	
"H" level total average output current	ΣI_{OHAV}	—	−50	mA	Total average output current = operating current × operating ratio (Total of pins)
Power consumption	Pd	—	320	mW	
Operating temperature	T_A	−40	+ 85	°C	
Storage temperature	Tstg	−40	+ 85	°C	

(Continued)

(Continued)

*1 : The parameter is based on V_{SS} = 0.0 V.

*2 : V_I and Vo should not exceed V_{CC} + 0.3 V. V_I must not exceed the rating voltage.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS} = 0.0 V)

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage	Vcc	1.8*	3.6	V	In normal operating
		2.7	3.6		In A/D converter operating
		2.7	3.6		On-chip debug mode
Operating temperature	T_A	–40	+85	°C	Other than on-chip debug mode
		+5	+35	°C	On-chip debug mode

* : The normal operation is performed from 1.8 V to the low voltage detection of the FRAM power supply monitor, or from the release voltage of the FRAM power supply monitor to 1.8 V. Reset is generated during the period that the low voltage detection reset has been detected. As for the low voltage detection, see “(8) Low Voltage Detection” in “4. AC Characteristics”.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

3. DC Characteristics

(Vcc = 3.3 V, Vss = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH1}	P04	*1	0.7 V_{CC}	—	V_{CC} + 0.3	V	When CMOS input level (Hysteresis input) is selected
	V_{IH2}	P64, P65	*1	0.7 V_{CC}	—	V_{CC} + 0.3	V	When CMOS input level (Hysteresis input) is selected
	V_{IHS1}	P00 to P07, P12, P62, P63, PG1, PG2	*1	0.8 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
	V_{IHS2}	P64, P65	*1	0.8 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
	V_{IHM}	PF2	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
"L" level input voltage	V_{IL}	P04, P64, P65	*1	V_{SS} – 0.3	—	0.3 V_{CC}	V	When CMOS input level (Hysteresis input) is selected
	V_{ILS}	P00 to P07, P12, P62 to P65, PG1, PG2	*1	V_{SS} – 0.3	—	0.2 V_{CC}	V	Hysteresis input
	V_{ILM}	PF2	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	Hysteresis input
Open-drain output application voltage	V_D	P12, P64, P65, PF2	—	V_{SS} – 0.3	—	V_{CC} + 0.3	V	
"H" level output voltage	V_{OH1}	Output pins other than P05, P06, P62 to P65, PF2, P12	I_{OH} = –4.0 mA	2.4	—	—	V	
	V_{OH2}	P05, P06, P62, P63	I_{OH} = –8.0 mA	2.4	—	—	V	
"L" level output voltage	V_{OL1}	Output pins other than P05, P06, P62, P63	I_{OL} = 4.0 mA	—	—	0.4	V	
	V_{OL2}	P05, P06, P62, P63	I_{OL} = 12.0 mA	—	—	0.4	V	

(Continued)

(Vcc = 3.3 V, Vss = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input leak current (Hi-Z output leak current)	I_{LI}	Other than ports P64, P65	0.0 V < V_I < V_{CC}	–5	—	+ 5	µA	When pull-up resistance is disabled
Open-drain output leak current	I_{LIOD}	P64, P65	0.0 V < V_I < V_{SS} + 5.5 V	—	—	+ 5	µA	
Pull-up resistance	R_{PULL}	P00 to P07, PG1, PG2	V_I = 0.0 V	16.5	33	66	kΩ	When pull-up resistance is enabled
Input capacitance	C_{IN}	Other than Vcc, Vss	f = 1 MHz	—	5	15	pF	
Power supply current*2	I_{CC}	Vcc (External clock operation)	F_{CH} = 20 MHz, F_{MP} = 10 MHz Main clock mode (divided by 2)	—	2.1 (TBD)	(TBD)	mA	
				—	(TBD)	(TBD)	mA	At A/D conversion
	I_{CCS}*3		F_{CH} = 20 MHz, F_{MP} = 10 MHz Main sleep mode (divided by 2) T_A = +25 °C	—	1	(TBD)	mA	
	I_{CCL}		F_{CL} = 32 kHz, F_{MPL} = 16 kHz Sub clock mode (divided by 2) T_A = +25 °C	—	52 (TBD)	(TBD)	µA	
	I_{CCLS}*3		F_{CL} = 32 kHz, F_{MPL} = 16 kHz Sub sleep mode (divided by 2) T_A = +25 °C	—	8 (TBD)	(TBD)	µA	
	I_{CCT}*3		F_{CL} = 32 kHz, Watch mode Main stop mode T_A = +25 °C	—	8 (TBD)	(TBD)	µA	
	I_{CCMCR}	Vcc	F_{CRH} = 1 MHz, F_{MP} = 1 MHz Main CR clock mode	—	0.4	—	mA	
	I_{CCSCR}		Sub CR clock mode (divided by 2) T_A = +25 °C	—	67	(TBD)	µA	

(Continued)

(Continued)

(Vcc = 3.3 V, Vss = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*2	I_{CCTS}*3	Vcc (External clock operation)	F_{CH} = 10 MHz, Time-base timer mode T_A = +25 °C	—	0.2	(TBD)	mA	
	I_{CCH}*3		Sub stop mode T_A = +25 °C	—	8 (TBD)	(TBD)	µA	
	I_{LVD1}	V_{CC}	Consumption current using a low voltage interrupt circuit only	—	5	10	µA	
	I_{LVD2}		Current consumption using a low voltage detection reset circuit and an FRAM power supply monitor circuit only	—	25	50	µA	
	I_{CRH}		Current consumption of internal main CR oscillator	—	70	100	µA	
	I_{CRL}		At oscillating 100 kHz current consumption of internal sub CR oscillator	—	9	20	µA	

*1 : P04, P64, P65 can switch the input level to either the “CMOS input level” or “hysteresis input level”. The switching of the input level can be set by the input level selection register (ILSR) .

*2 : • The power-supply current is determined by the external clock. when Internal CR are selected, the power-supply current will be a value of adding current consumption of internal CR oscillator (I_{CRH}, I_{CRL}) to the specified value. In on-chip debug mode, the CR oscillator (I_{CRH}) and the low-voltage detection circuit are always enabled, and current consumption therefore increases accordingly.
• Refer to “(1) Clock Timing” in “4. AC Characteristics” for F_{CH} and F_{CL}.
• Refer to “(2) Source Clock/Machine Clock” in “4. AC Characteristics” for F_{MP} and F_{MPL}.

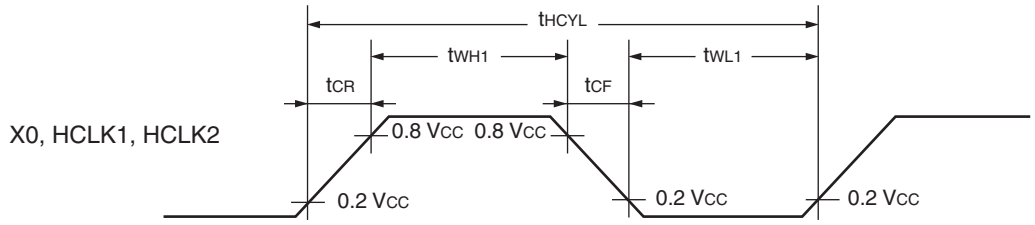
*3 : When a low voltage detection circuit stop bit (LVDCR2: LVDSTP set) is not set to “1”, the power supply current will be the sum of the current consumption value for a low voltage detection circuit (I_{LVD2}) and the specified value.

4. AC Characteristics

(1) Clock Timing

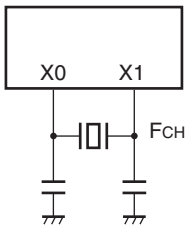
(Vcc = 3.3 V, Vss = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_{CH}	X0, X1	—	1	—	10	MHz	When the main oscillation circuit is used
		X0, X1, HCLK1, HCLK2		1	—	20	MHz	When the main external clock is used
	F_{CRH}	—		0.96	1	1.04	MHz	When the main internal CR clock is used (+ 5 °C ≤ T_A ≤ + 35 °C)
				7.2 (TBD)	—	8.8 (TBD)		
	F_{CL}	X0A, X1A		—	32.768	—	MHz	When the sub oscillation circuit is used
				—	32.768	—	kHz	When the sub external clock is used
	F_{CRL}	—		50	100	200	kHz	When the sub internal CR clock is used
Clock cycle time	t_{HCYL}	X0, X1	—	100	—	1000	ns	When the main oscillation circuit is used
		X0, X1, HCLK1, HCLK2		50	—	1000	ns	When the main external clock is used
	t_{LCYL}	X0A, X1A		—	30.5	—	µs	When using sub clock
Input clock pulse width	t_{WH1}	X0, HCLK1, HCLK2		20	—	—	ns	When the external clock is used, the duty ratio should range between 40% and 60%
	t_{WL1}							
	t_{WH2}	X0A		—	15.2	—	µs	
	t_{WL2}							
Input clock rise time and fall time	t_{CR}	X0, X0A, HCLK1, HCLK2		—	—	5	ns	When the external clock is used
	t_{CF}							
Internal CR oscillation start time	t_{CRHWK}	—		—	—	10	µs	When the main-internal CR clock is used
	t_{CRLWK}	—		—	—	50	µs	When the sub-internal CR clock is used

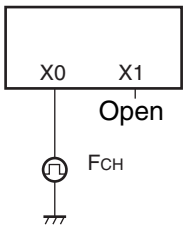


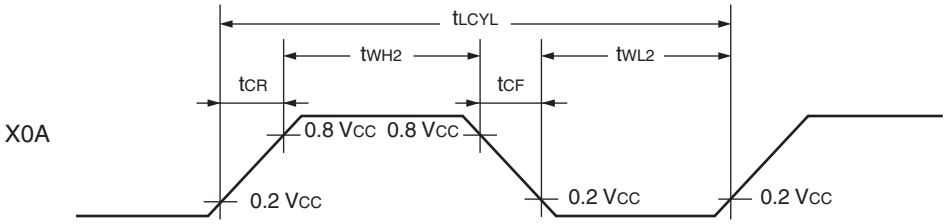
- Figure of main clock input port external connection

When using a crystal or Ceramic oscillator



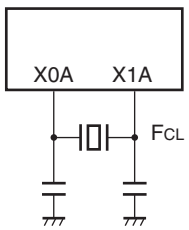
When using external clock



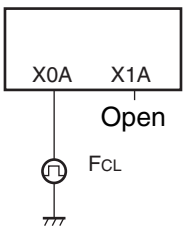


- Figure of sub clock input port external connection

When using a crystal or Ceramic oscillator



When using external clock



(2) Source Clock/Machine Clock

(Vcc = 3.3 V, Vss = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Source clock cycle time*1 (Clock before division)	t_{SCLK}	—	100	—	2000	ns	When using main external clock Min : F_{CH} = 20 MHz, divided by 2 Max : F_{CH} = 1 MHz, divided by 2
			125	—	1000	ns	When using main CR oscillation clock Min : F_{CRH} = 8 MHz Max : F_{CRH} = 1 MHz
			—	61	—	µs	When using sub oscillation clock F_{CL} = 32.768 kHz, divided by 2
			—	20	—	µs	When using sub oscillation clock F_{CRL} = 100 kHz, divided by 2
Source clock frequency	F_{SP}	—	0.5	—	10	MHz	When using main oscillation clock
			1	—	8	MHz	When using main CR oscillation clock
	F_{SPL}		—	16.384	—	kHz	When using sub oscillation clock
			—	50	—	kHz	When using sub CR clock
Machine clock cycle time*2 (Minimum instruction execution time)	t_{MCLK}	—	100	—	32000	ns	When using main oscillation clock Min : F_{SP} = 10 MHz, no division Max : F_{SP} = 0.5 MHz, divided by 16
			100	—	16000	ns	When using main CR clock Min : F_{SP} = 10 MHz, no division Max : F_{SP} = 1 MHz, divided by 16
			61	—	976.5	µs	When using sub oscillation clock Min : F_{SPL} = 16.384 kHz, no division Max : F_{SPL} = 16.384 kHz, divided by 16
			20	—	320	µs	When using sub CR clock Min : F_{SPL} = 50 kHz, no division Max : F_{SPL} = 50 kHz, divided by 16
Machine clock frequency	F_{MP}	—	0.031	—	10	MHz	When using main oscillation clock
			0.0625	—	8	MHz	When using main CR clock
	F_{MPL}		1.024	—	16.384	kHz	When using sub oscillation clock
			3.125	—	50	kHz	When using sub CR clock

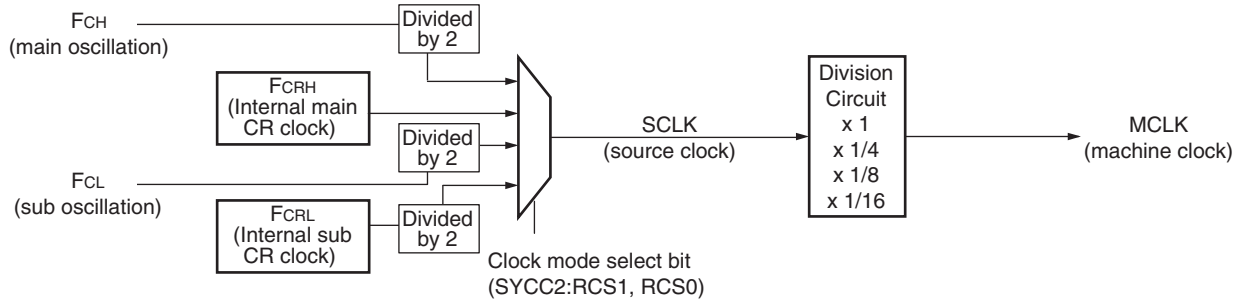
*1 : Clock before setting division due to machine clock division ratio selection bit (SYCC : DIV1 and DIV0) . This source clock is divided by the machine clock division ratio selection bit (SYCC : DIV1 and DIV0) , and it becomes the machine clock. Further, the source clock can be selected as follows.

- Main clock divided by 2
- Main CR clock
- Sub clock divided by 2
- Sub CR clock divided by 2

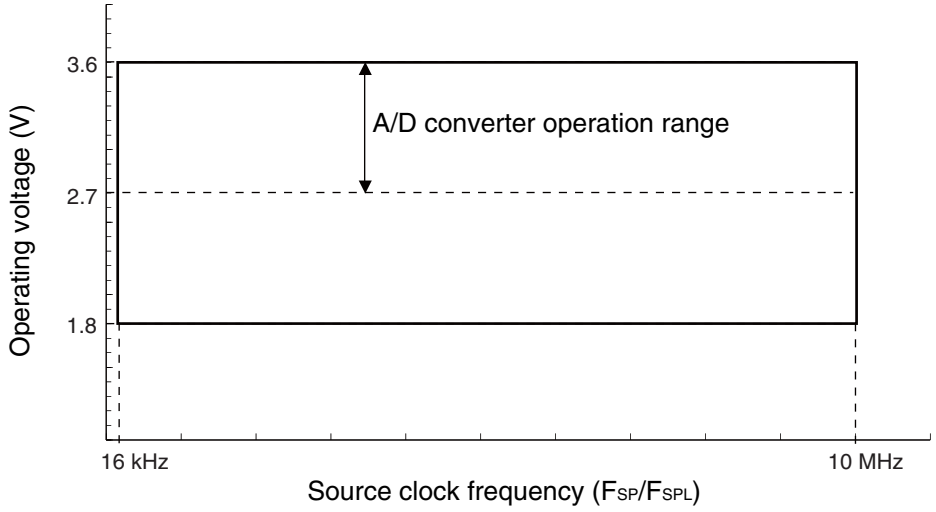
*2 : Operation clock of the microcontroller. Machine clock can be selected as follows.

- Source clock (no division)
- Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

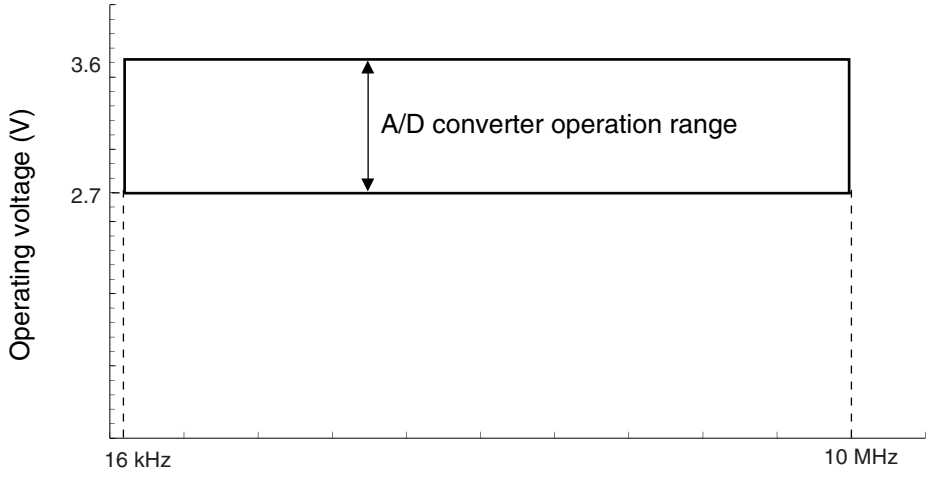
• Outline of clock generation block



• Operating voltage - Operating frequency (When $T_A = -40$ °C to $+85$ °C)
(Without on chip debug function)



• Operating voltage - Operating frequency ($T_A = +5$ °C to $+35$ °C)
(With on chip debug function)



(3) External Reset

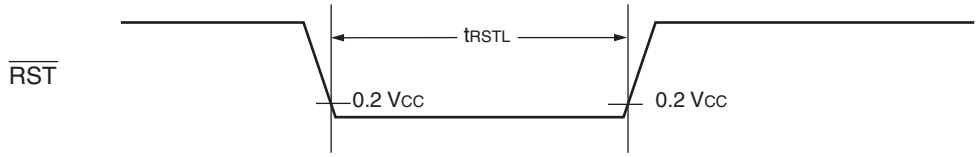
(Vcc = 3.3 V, Vss = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
$\overline{RST}$ "L" level pulse width	t_{RSTL}	2 t_{MCLK}*1	—	ns	At normal operating
		Oscillation time of oscillator*2 + 100	—	µs	At stop mode, sub clock mode, sub sleep mode, and watch mode
		100	—	µs	At time-base timer mode

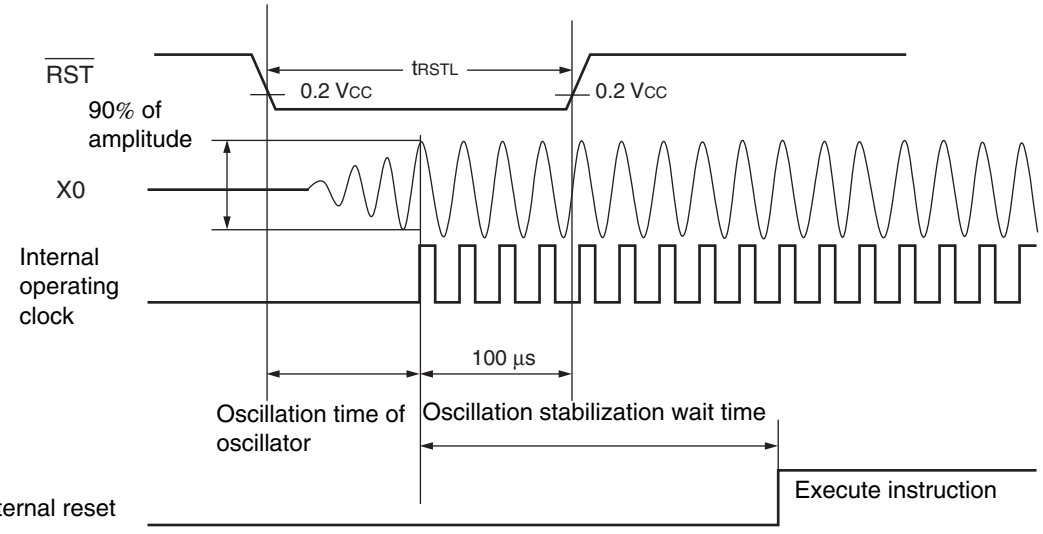
*1 : Refer to " (2) Source Clock/Machine Clock" for t_{MCLK}.

*2 : Oscillation time of oscillator is the time that the amplitude reaches 90%. In the crystal oscillator, the oscillation time is between several ms and tens of ms. In ceramic oscillators, the oscillation time is between hundreds of µs and several ms. In the external clock, the oscillation time is 0 ms.

• At normal operating



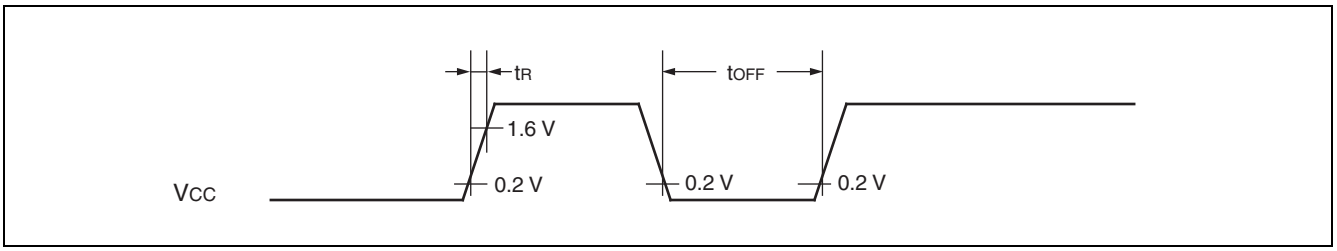
• At stop mode, sub clock mode, sub sleep mode, watch mode, and power-on



(4) Power-on Reset

(Vss = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Power supply rising time	t_R	—	0.1	50	ms	
Power supply cutoff time	t_{OFF}	—	1	—	ms	Waiting time until power-on



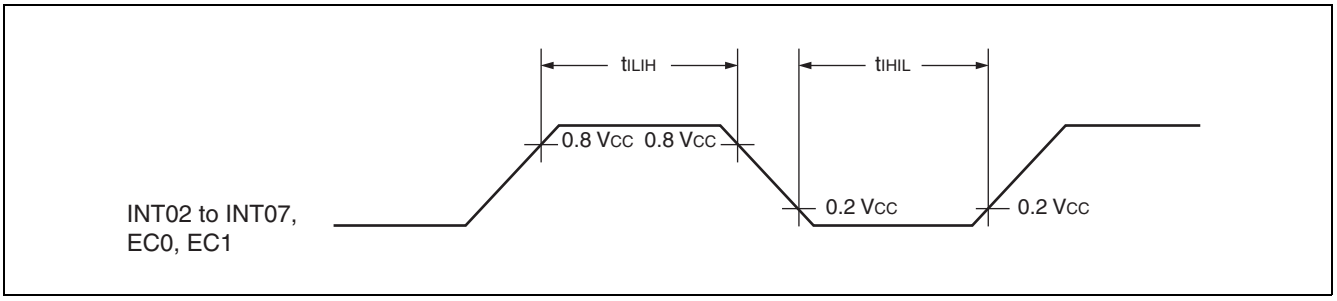
Note: A sudden change the power supply voltage may activate the power-on reset function. When changing power supply voltages during operation, set the slope of rising within 30 mV/ms.

(5) Peripheral Input Timing

(Vcc = 3.3 V, Vss = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
Peripheral input “H” pulse	t_{ILIH}	INT02 to INT07, EC0, EC1	2 t_{MCLK}*	—	ns
Peripheral input “L” pulse	t_{IHIL}		2 t_{MCLK}*	—	ns

* : Refer to “ (2) Source Clock/Machine Clock” for t_{MCLK}.



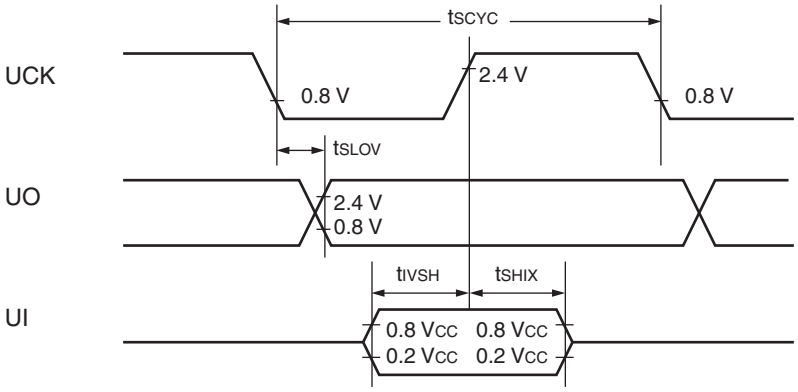
(6) UART/SIO, Serial I/O Timing

(Vcc = 3.3 V, Vss = 0.0 V, T_A = –40 °C to +85 °C)

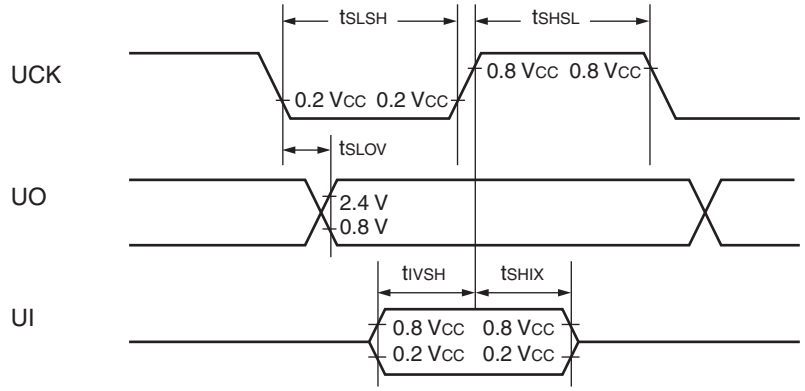
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	UCK	Internal clock operation output pin : C_L = 80 pF + 1 TTL.	4 t_{MCLK}*	—	ns
UCK ↓ → UO time	t_{SLOV}	UCK, UO		–190	+190	ns
Valid UI → UCK ↑	t_{IVSH}	UCK,UI		2 t_{MCLK}*	—	ns
UCK ↑→ valid UI hold time	t_{SHIX}	UCK, UI		2 t_{MCLK}*	—	ns
Serial clock “H” pulse width	t_{SHSL}	UCK	External clock operation output pin : C_L = 80 pF + 1 TTL.	4 t_{MCLK}*	—	ns
Serial clock “L” pulse width	t_{SLSH}	UCK		4 t_{MCLK}*	—	ns
UCK ↓ → UO time	t_{SLOV}	UCK, UO		0	190	ns
Valid UI → UCK ↑	t_{IVSH}	UCK, UI		2 t_{MCLK}*	—	ns
UCK ↑→ valid UI hold time	t_{SHIX}	UCK, UI		2 t_{MCLK}*	—	ns

* : Refer to “ (2) Source Clock/Machine Clock” for details on t_{MCLK}.

• Internal shift clock mode



• External shift clock mode



(7) I²C Timing

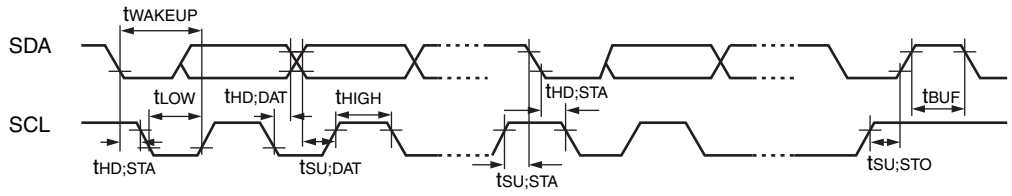
(Vcc = 3.3 V, Vss = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value				Unit
				Standard-mode		Fast-mode		
				Min	Max	Min	Max	
SCL clock frequency	t_{SCYC}	SCL	R = 1.7 kΩ, C = 50 pF*1	0	100	0	400	kHz
(Repeat) Start condition hold time SDA ↓ → SCL ↓	$t_{HD;STA}$	SCL SDA		4.0	—	0.6	—	µs
SCL clock “L” width	t_{LOW}	SCL		4.7	—	1.3	—	µs
SCL clock “H” width	t_{HIGH}	SCL		4.0	—	0.6	—	µs
(Repeat) Start condition setup time SCL ↑ → SDA ↓	$t_{SU;STA}$	SCL SDA		4.7	—	0.6	—	µs
Data hold time SCL ↓ → SDA ↓ ↑	$t_{HD;DAT}$	SCL SDA		0	3.45*2	0	0.9*2	µs
Data setup time SDA ↓ ↑ → SCL ↑	$t_{SU;DAT}$	SCL SDA		0.25	—	0.1	—	µs
Stop condition setup time SCL ↑ → SDA ↓	$t_{SU;STO}$	SCL SDA		4.0	—	0.6	—	µs
Bus free time between stop condition and start condition	t_{BUF}	SCL SDA		4.7	—	1.3	—	µs

*1 : R, C : Pull-up resistance and load capacitance of the SCL and SDA lines.

*2 : The maximum value of $t_{HD;DAT}$ is applicable only if the device does not extend the “L” width (t_{LOW}) of the SCL signal.

*3 : A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met.



(Vcc = 3.3 V, Vss = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value*2		Unit	Remarks
				Min	Max		
SCL clock “L” width	t_{LOW}	SCL	R = 1.7 kΩ, C = 50 pF*1	(2 + nm / 2) t_{MCLK} – 20	—	ns	Master mode
SCL clock “H” width	t_{HIGH}	SCL		(nm / 2) t_{MCLK} – 20	(nm / 2) t_{MCLK} + 20	ns	Master mode
Start condition hold time	$t_{HD;STA}$	SCL SDA		(–1 + nm / 2) t_{MCLK} – 20	(–1 + nm / 2) t_{MCLK} + 20	ns	Master mode maximum value is applied when m, n = 1, 8. Otherwise, the minimum value is applid.
Stop condition setup time	$t_{SU;STO}$	SCL SDA		(1 + nm / 2) t_{MCLK} – 20	(1 + nm / 2) t_{MCLK} + 20	ns	Master mode
Start condition setup time	$t_{SU;STA}$	SCL SDA		(1 + nm / 2) t_{MCLK} – 20	(1 + nm / 2) t_{MCLK} + 20	ns	Master mode
Bus free time between stop condition and start condition	t_{BUF}	SCL SDA		(2 nm + 4) t_{MCLK} – 20	—	ns	
Data hold time	$t_{HD;DAT}$	SCL SDA		3 t_{MCLK} – 20	—	ns	Master mode
Data setup time	$t_{SU;DAT}$	SCL SDA		(–2 + nm / 2) t_{MCLK} – 20	(–1 + nm / 2) t_{MCLK} + 20	ns	Master mode When assuming that “L” of SCL is not extended, the minimum value is applied to first bit of continuous data. Otherwise, the maximum value is applied.
Setup time between cleaning interrupt and SCL rising	$t_{SU;INT}$	SCL		(nm / 2) t_{MCLK} – 20	(1 + nm / 2) t_{MCLK} + 20	ns	Minimum value is applied to interrupt at 9th SCL↓. Maximum value is applied to interrupt at 8th SCL↓.
SCL clock “L” width	t_{LOW}	SCL		4 t_{MCLK} – 20	—	ns	At reception
SCL clock “H” width	t_{HIGH}	SCL		4 t_{MCLK} – 20	—	ns	At reception
Start condition detection	$t_{HD;STA}$	SCL SDA		4 t_{MCLK} – 20	—	ns	Undetected when 1 t_{MCLK} is used at reception

(Continued)

(Continued)

(Vcc = 3.3 V, Vss = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value*2		Unit	Remarks
				Min	Max		
Stop condition detection	$t_{SU;STO}$	SCL SDA	R = 1.7 kΩ, C = 50 pF*1	4 t_{MCLK} – 20	—	ns	Undetected when 1 t_{MCLK} is used at reception
Restart condition detection condition	$t_{SU;STA}$	SCL SDA		2 t_{MCLK} – 20	—	ns	Undetected when 1 t_{MCLK} is used at reception
Bus free time	t_{BUF}	SCL SDA		2 t_{MCLK} – 20	—	ns	During reception
Data hold time	$t_{HD;DAT}$	SCL SDA		2 t_{MCLK} – 20	—	ns	In slave transmission mode
Data setup time	$t_{SU;DAT}$	SCL SDA		t_{LOW} – 3 t_{MCLK} – 20	—	ns	In slave transmission mode
Data hold time	$t_{HD;DAT}$	SCL SDA		0	—	ns	During reception
Data setup time	$t_{SU;DAT}$	SCL SDA		t_{MCLK} – 20	—	ns	During reception
SDA ↓ → SCL ↑ (when using wakeup function)	t_{WAKEUP}	SCL SDA		Oscillation stabilization wait time + 2 t_{MCLK} – 20	—	ns	

*1 : R, C : Pull-up resistance and load capacitance of the SCL and SDA lines.

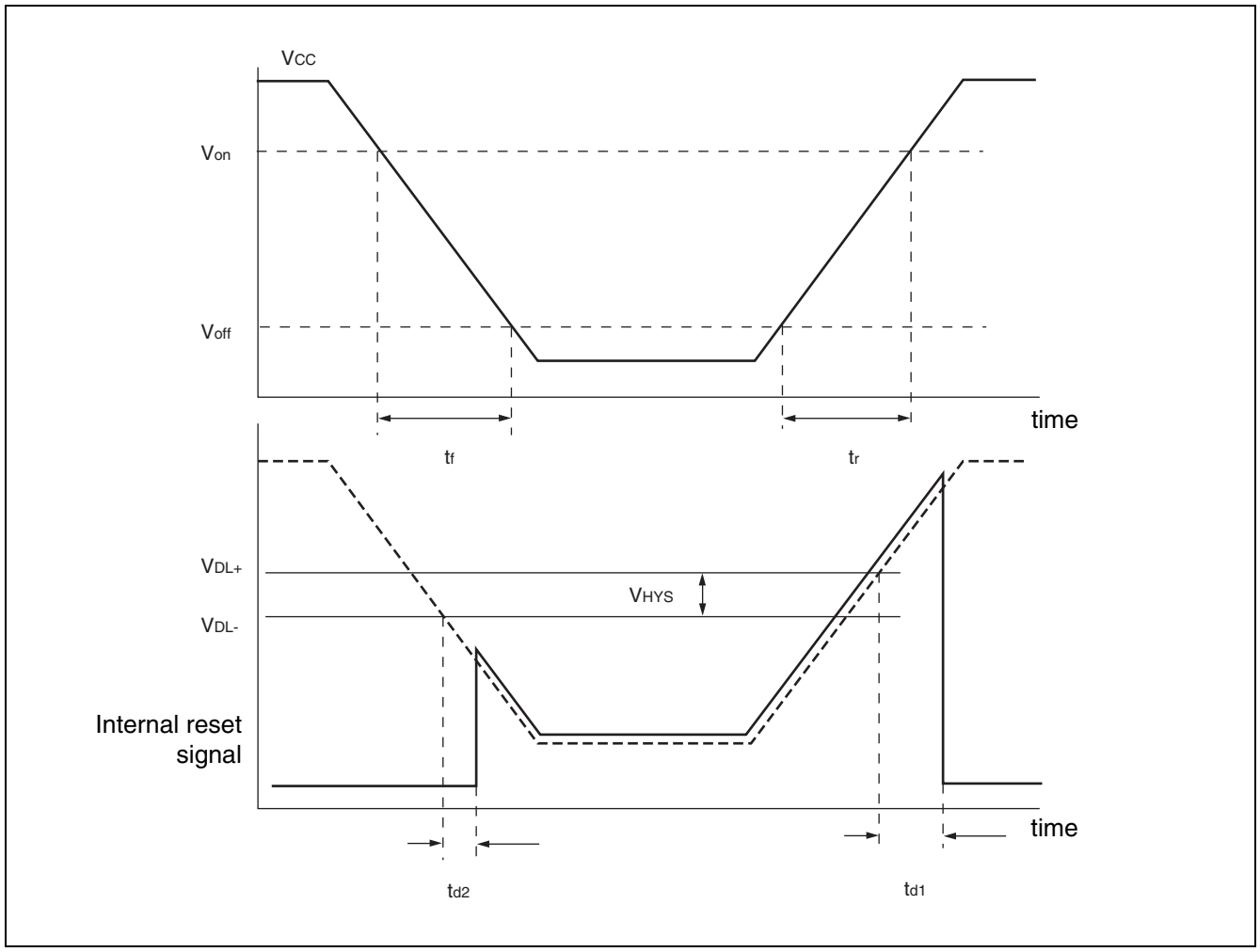
*2 :
- Refer to " (2) Source Clock/Machine Clock" for details on t_{MCLK}.
- m is the CS4 and CS3 bits (bit4 and bit3) of the I²C clock control register (ICCR0) .
- n is the CS2 to CS0 bits (bit2 to bit0) of the I²C clock control register (ICCR0) .
- The actual I²C timing is determined by the machine (t_{MCLK}) and the values of m and n configured in bits CS4 to CS0 of the I²C clock control register (ICCR0) .
- Standard-mode :
  m and n can be set in the range : 0.9 MHz < t_{MCLK} (machine clock) < 10 MHz.
  The machine clock to be used is determined by the settings of m and n as follows.
  (m, n) = (1, 8) : 0.9 MHz < t_{MCLK} ≤ 1 MHz
  (m, n) = (1, 22) , (5, 4) , (6, 4) , (7, 4) , (8, 4) , : 0.9 MHz < t_{MCLK} ≤ 2 MHz
  (m, n) = (1, 38) , (5, 8) , (6, 8) , (7, 8) , (8, 8) , : 0.9 MHz < t_{MCLK} ≤ 4 MHz
  (m, n) = (1, 98) : 0.9 MHz < t_{MCLK} ≤ 1 MHz
- Fast-mode :
  m and n can be set in the range : 3.3 MHz < t_{MCLK} (machine clock) < 10 MHz.
  The machine clock to be used is determined by the settings of m and n as follows.
  (m, n) = (1, 8) : 3.3 MHz < t_{MCLK} ≤ 4 MHz
  (m, n) = (1, 22) , (5, 4) : 3.3 MHz < t_{MCLK} ≤ 8 MHz
  (m, n) = (6, 4) : 3.3 MHz < t_{MCLK} ≤ 10 MHz

(8) Low Voltage Detection

(V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter		Symbol	Value			Unit	Remarks
			Min	Typ	Max		
Low voltage detection reset	Release voltage	V_{DL+}	1.75	1.85	1.95	V	At power-supply rise
	Detection voltage	V_{DL-}	1.65	1.75	1.85	V	At power-supply fall
	Hysteresis width	V_{HYS}	70	100	—	mV	
FRAM power supply monitor	Release voltage	V_{DL+}	1.8	1.9	2.0	V	At power-supply rise
	Detection voltage	V_{DL-}	1.7	1.8	1.9	V	At power-supply fall
	Hysteresis width	V_{HYS}	70	100	—	mV	
Low voltage detection interrupt	Release voltage	V_{DL+}	2.2	2.3	2.4	V	At LS1 = 0, LS0 = 0, power-supply rise*
			2.4	2.5	2.6	V	At LS1 = 0, LS0 = 1, power-supply rise*
			2.6	2.7	2.8	V	At LS1 = 1, LS0 = 0, power-supply rise*
			2.8	2.9	3.0	V	At LS1 = 1, LS0 = 1, power-supply rise*
	Detection voltage	V_{DL-}	2.1	2.2	2.3	V	At LS1 = 0, LS0 = 0, power-supply fall*
			2.3	2.4	2.5	V	At LS1 = 0, LS0 = 1, power-supply fall*
			2.5	2.6	2.7	V	At LS1 = 1, LS0 = 0, power-supply fall*
			2.7	2.8	2.9	V	At LS1 = 1, LS0 = 1, power-supply fall*
	Hysteresis width	V_{HYS}	70	100	—	mV	
Power-supply start voltage		V_{off}	—	—	1.2	V	
Power-supply end voltage		V_{on}	2.0	—	—	V	
Power-supply voltage change time (at power supply rise)		t_r	0.3	—	—	µs	Slope of power supply that reset release signal generates
			—	200	—	µs	Slope of power supply that reset release signal generates within rating ($V1_{DL+}$, $V2_{DL+}$)
Power-supply voltage change time (at power supply fall)		t_f	0.3	—	—	µs	Slope of power supply that reset detection signal generates
			—	200	—	µs	Slope of power supply that reset detection signal generates within rating ($V1_{DL-}$, $V2_{DL-}$)
Reset release delay time		t_{d1}	—	—	300	µs	
Reset detection delay time		t_{d2}	—	—	20	µs	

* : LS1 and LS0 mean the LS1 bit and the LS0 bit (bit1 and bit0) for the low voltage detection interrupt control register (LVDCR) respectively.


VCC
Von
Voff
time
tf
tr
VDL+
VDL-
VHYS
Internal reset signal
time
td2
td1

5. A/D Converter

(1) A/D Converter Electrical Characteristics

(Vcc = 2.7 V to 3.6 V, Vss = 0.0 V, T_A = –40 °C to +85 °C)

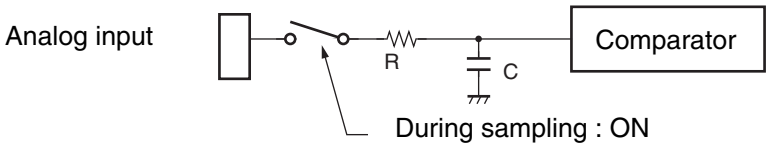
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	10	bit	
Total error		– 3.0	—	+ 3.0	LSB	
Linearity error		– 2.5	—	+ 2.5	LSB	
Differential linear error		– 1.9	—	+ 1.9	LSB	
Zero transition voltage	V_{OT}	V_{SS} – 1.5 LSB	V_{SS} + 0.5 LSB	V_{SS} + 2.5 LSB	V	
Full-scale transition voltage	V_{FST}	V_{CC} – 3.5 LSB	V_{CC} – 1.5 LSB	V_{CC} + 0.5 LSB	V	
Compare time	—	0.6	—	140	µs	
Sampling time	—	0.4	—	∞	µs	2.7 V ≤ Vcc ≤ 3.6 V At external impedance < 1.8 kΩ
Analog input current	I_{AIN}	– 4	—	+ 4	µA	
Analog input voltage	V_{AIN}	V_{SS}	—	V_{CC}	V	

(2) Notes on Using A/D Converter

- **About the external impedance of analog input and its sampling time**

A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. Also, if the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

- Analog input equivalent circuit

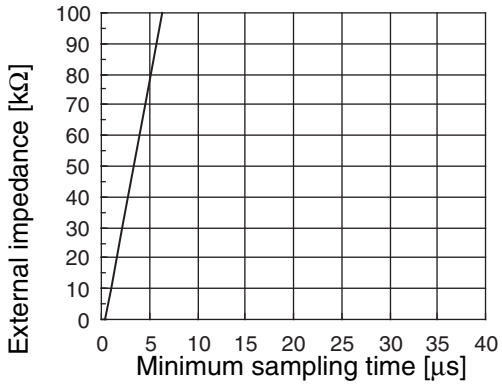


2.7 V ≤ Vcc ≤ 3.6 V : R ≒ 5.3 kΩ (Max) , C ≒ 8.5 pF (Max)

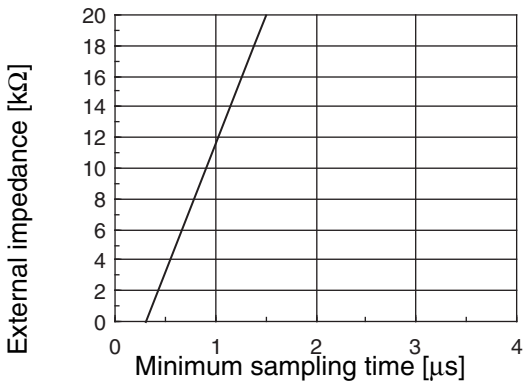
Note : The values are reference values.

- The relationship between external impedance and minimum sampling time.

[External impedance = 0 kΩ to 100 kΩ]



[External impedance = 0 kΩ to 20 kΩ]

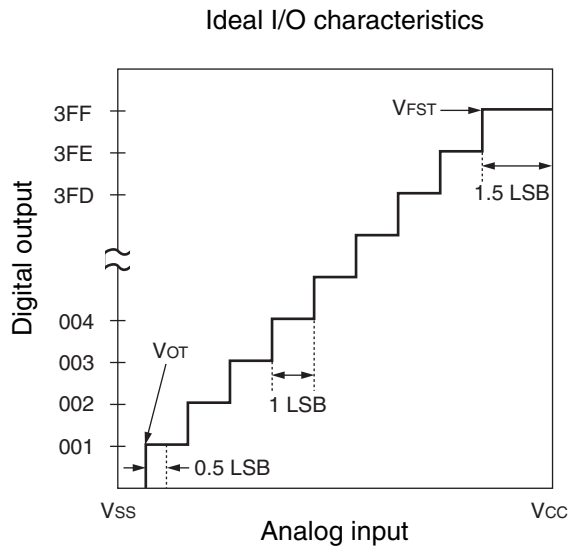


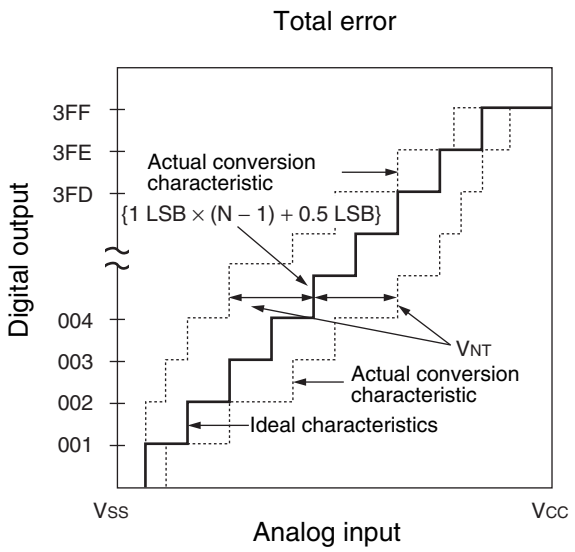
- **About errors**

$|V_{CC} - V_{SS}|$ becomes smaller, values of relative errors grow larger.

(3) Definition of A/D Converter Terms

- Resolution
  The level of analog variation that can be distinguished by the A/D converter.
  When the number of bits is 10, analog voltage can be divided into $2^{10} = 1024$.
- Linearity error (unit : LSB)
  The deviation between the value along a straight line connecting the zero transition point
  (“00 0000 0000” ←→ “00 0000 0001”) of a device and the full-scale transition point
  (“11 1111 1111” ←→ “11 1111 1110”) compared with the actual conversion values obtained.
- Differential linear error (Unit : LSB)
  Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
- Total error (unit : LSB)
  Difference between actual and theoretical values, caused by a zero transition error, full-scale transition error, linearity error, quantum error, and noise.





$$1\ \text{LSB} = \frac{V_{CC} - V_{SS}}{1024}\ (\text{V})$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

N : A/D converter digital output value
V_{NT} : A voltage at which digital output transits from (N - 1) to N

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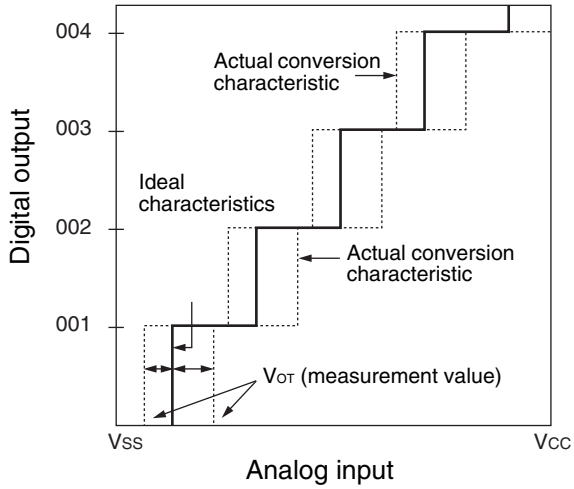
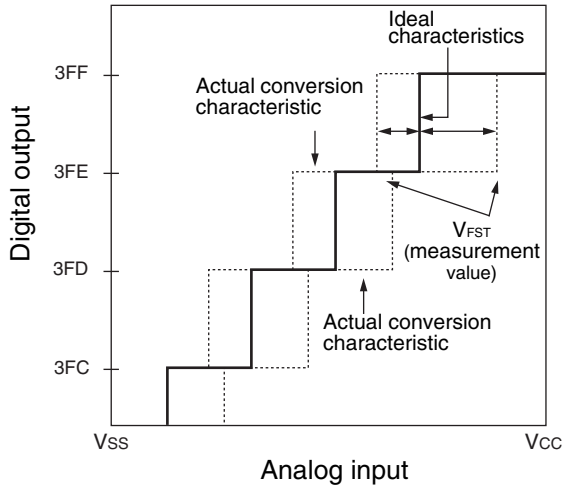
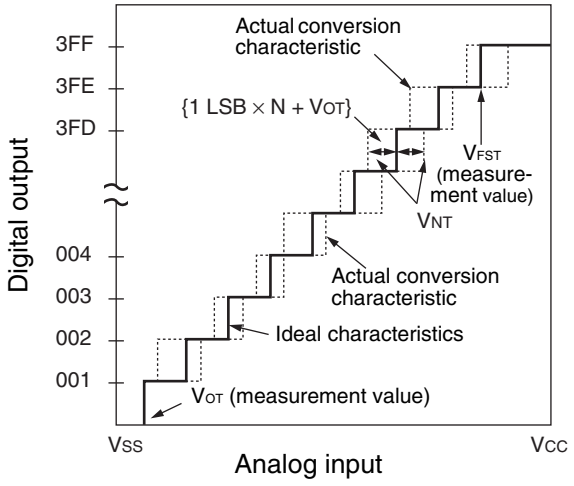
Zero transition error



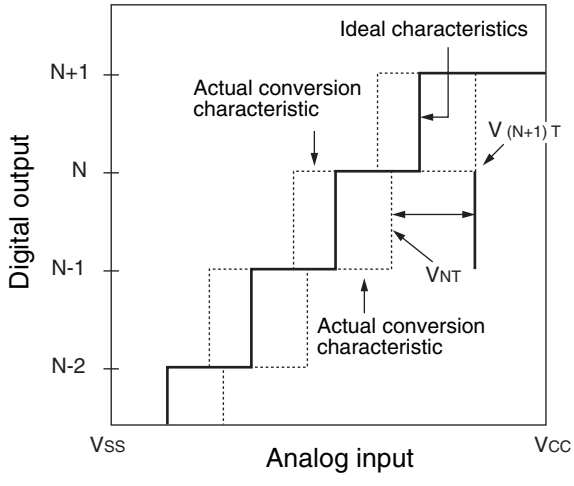
Full-scale transition error



Linearity error



Differential linear error



$$\text{Linearity error in digital output N} = \frac{V_{NT} - \{1\ LSB \times N + V_{OT}\}}{1\ LSB}$$

$$\text{Differential linear error In digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ LSB} - 1$$

N : A/D converter digital output value
V_{NT} : A voltage at which digital output transits from (N - 1) to N.
V_{OT} (Ideal value) = V_{SS} + 0.5 LSB [V]
V_{FST} (Ideal value) = V_{CC} – 2.0 LSB [V]

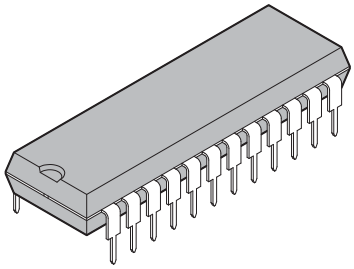
6. FRAM Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Number of read/write cycle	10^{15}	—	—	cycle	

■ ORDERING INFORMATION

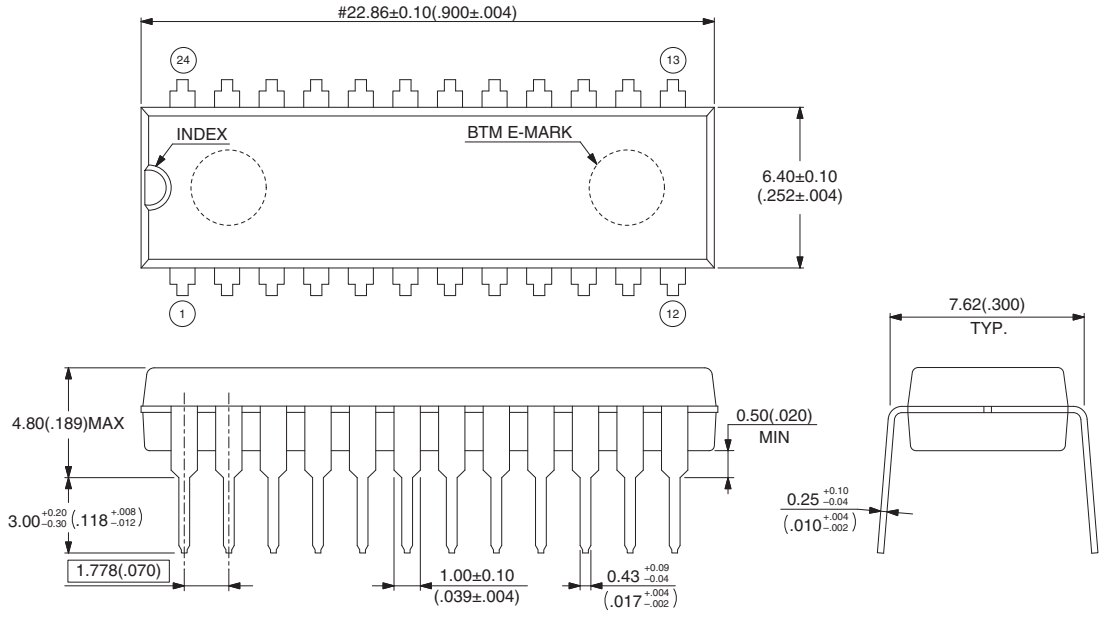
Part number	Package	Remarks
MB95R203AP-G-SH-JNE2	24-pin plastic DIP (DIP-24P-M07)	
MB95R203APF-G-JNE2	20-pin plastic SOP (FPT-20P-M09)	

■ PACKAGE DIMENSIONS

24-pin plastic SDIP		
 (DIP-24P-M07)	Lead pitch	1.778 mm
	Package width × package length	6.40 mm × 22.86 mm
	Sealing method	Plastic mold
	Mounting height	4.80 mm Max

24-pin plastic SDIP
(DIP-24P-M07)

Note 1) Pins width and pins thickness include plating thickness.
Note 2) Pins width do not include tie bar cutting remainder.
Note 3) # : These dimensions do not include resin protrusion.



Dimensions in mm (inches).
Note: The values in parentheses are reference values

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

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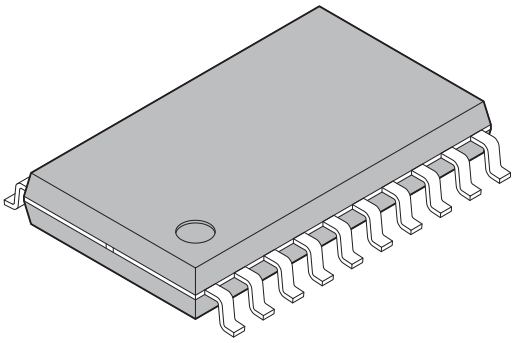
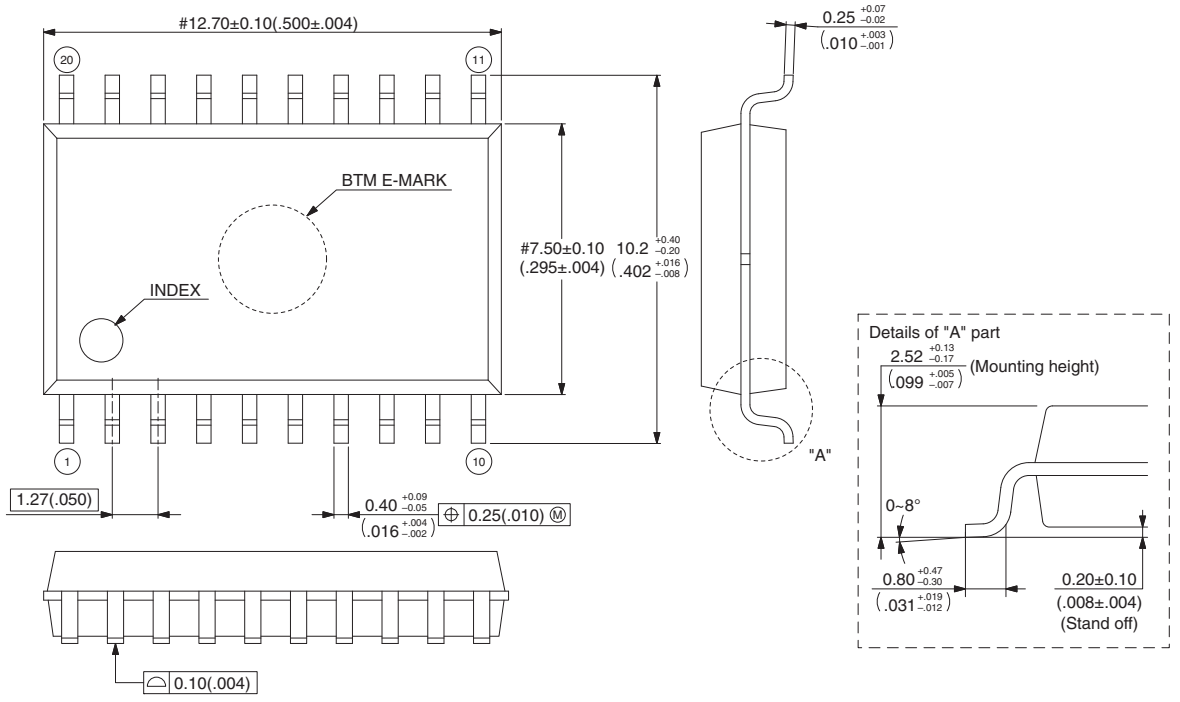
20-pin plastic SOP		
 (FPT-20P-M09)	Lead pitch	1.27 mm
	Package width × package length	7.50 mm × 12.70 mm
	Lead shape	Gullwing
	Lead bend direction	Normal bend
	Sealing method	Plastic mold
	Mounting height	2.65 mm Max

20-pin plastic SOP
(FPT-20P-M09)

Note 1) Pins width and pins thickness include plating thickness.
Note 2) Pins width do not include tie bar cutting remainder.
Note 3) # : These dimensions do not include resin protrusion.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

MEMO

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