FUJITSU MICROELECTRONICS
DATA SHEET

DS07-12626-2E

8-bit Microcontroller

CMOS

F²MC-8FX MB95220H Series

MB95F222H/F223H
MB95F222K/F223K

■ DESCRIPTION

MB95220H are a series of general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers of these series contain a variety of peripheral resources.

Note: F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

■ FEATURES

- F²MC-8FX CPU core
  Instruction set optimized for controllers
  - Multiplication and division instructions
  - 16-bit arithmetic operations
  - Bit test branch instructions
  - Bit manipulation instructions, etc.
- Clock
  - Selectable main clock source
    External clock (up to 32.5 MHz, maximum machine clock frequency: 16.25 MHz)
    Main internal CR clock (1/8/10 MHz ±3%, maximum machine clock frequency: 10 MHz)
  - Selectable subclock source
    External clock (32.768 kHz)
    Sub-internal CR clock (typ: 100 kHz, min: 50 kHz, max: 200 kHz)
- Timer
  - 8/16-bit composite timer
  - Timebase timer
  - Watch prescaler
- LIN-UART (MB95F222H/F222K/F223H/F223K)
  - Full duplex double buffer
  - Capable of clock-synchronized serial data transfer and clock-asynchronized serial data transfer

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- External interrupt
  - Interrupt by edge detection (rising edge, falling edge, and both edges can be selected)
  - Can be used to wake up the device from different low power consumption (standby) modes
- 8/10-bit A/D converter
  - 8-bit or 10-bit resolution can be selected.
- Low power consumption (standby) modes
  - Stop mode
  - Sleep mode
  - Watch mode
  - Timebase timer mode
- I/O port (max: 13) (MB95F222K/F223K)
  - General-purpose I/O ports (max):
    CMOS I/O: 11, N-ch open drain: 2
- I/O port (max: 12) (MB95F222H/F223H)
  - General-purpose I/O ports (max):
    CMOS I/O: 11, N-ch open drain: 1
- On-chip debug
  - 1-wire serial control
  - Serial writing supported (asynchronous mode)
- Hardware/software watchdog timer
  - Built-in hardware watchdog timer
- Low-voltage detection reset circuit
  - Built-in low-voltage detector
- Clock supervisor counter
  - Built-in clock supervisor counter function
- Programmable port input voltage level
  - CMOS input level / hysteresis input level
- Flash memory security function
  - Protects the contents of flash memory

■ PRODUCT LINE-UP

Part number / Parameter	MB95F223H	MB95F222H	MB95F223K	MB95F222K
Type	Flash memory product			
Clock supervisor counter	It supervises the main clock oscillation.			
ROM capacity	8 KB	4 KB	8 KB	4 KB
RAM capacity	496 B	240 B	496 B	240 B
Low-voltage detection reset	No		Yes	
Reset input	Dedicated		Selected by software	
CPU functions	Number of basic instructions : 136 Instruction bit length : 8 bits Instruction length : 1 to 3 bytes Data bit length : 1, 8, and 16 bits Minimum instruction execution time : 61.5 ns (with machine clock = 16.25 MHz) Interrupt processing time : 0.6 µs (with machine clock = 16.25 MHz)			
General-purpose I/O	I/O ports (max): 12 CMOS: 11, N-ch: 1		I/O ports (max): 13 CMOS: 11, N-ch: 2	
Timebase timer	Interrupt cycle : 0.256 ms - 8.3 s (when external clock = 4 MHz)			
Hardware/ software watchdog timer	Reset generation cycle Main oscillation clock at 10 MHz : 105 ms (min) The sub-internal CR clock can be used as the source clock of the hardware watchdog timer.			
Wild register	It can be used to replace three bytes of data.			
LIN-UART	A wide range of communication speed can be selected by a dedicated reload timer. It has a full duplex double buffer. Clock-synchronized serial data transfer and clock-asynchronized serial data transfer is enabled. The LIN function can be used as a LIN master or a LIN slave.			
8/10-bit A/D converter	5 ch.			
	8-bit or 10-bit resolution can be selected.			
8/16-bit composite timer	1 ch.			
	The timer can be configured as an "8-bit timer x 2 channels" or a "16-bit timer x 1 channel". It has built-in timer function, PWC function, PWM function and input capture function. Count clock: it can be selected from internal clocks (seven types) and external clocks. It can output square wave.			
External interrupt	6 ch.			
	Interrupt by edge detection (The rising edge, falling edge, or both edges can be selected.) It can be used to wake up the device from standby modes.			
On-chip debug	1-wire serial control It supports serial writing. (asynchronous mode)			

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Part number / Parameter	MB95F223H	MB95F222H	MB95F223K	MB95F222K
Watch prescaler	Eight different time intervals can be selected.			
Flash memory	It supports automatic programming, Embedded Algorithm, write/erase/erase-suspend/erase-resume commands. It has a flag indicating the completion of the operation of Embedded Algorithm. Number of write/erase cycles (min): 100000 Data retention time: 20 years For write/erase, external Vpp(+10 V) input is required. Flash security feature for protecting the contents of the flash			
Standby mode	Sleep mode, stop mode, watch mode, timebase timer mode			
Package	DIP-16P-M06 FPT-16P-M06			

■ PACKAGES AND CORRESPONDING PRODUCTS

Part number / Package	MB95F223H	MB95F222H	MB95F223K	MB95F222K
DIP-16P-M06	O	O	O	O
FPT-16P-M06	O	O	O	O

O: Available

■ DIFFERENCES AMONG PRODUCTS AND NOTES ON PRODUCT SELECTION

• Current consumption

When using the on-chip debug function, take account of the current consumption of flash erase/program.

For details of current consumption, see "■ ELECTRICAL CHARACTERISTICS".

• Package

For details of information on each package, see "■ PACKAGES AND CORRESPONDING PRODUCTS" and "■ PACKAGE DIMENSIONS".

• Operating voltage

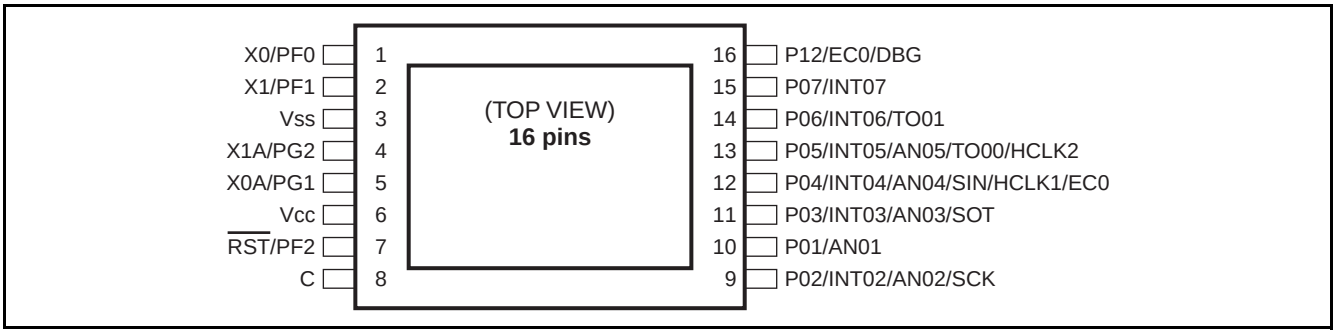
The operating voltage varies, depending on whether the on-chip debug function is used or not.

For details of the operating voltage, see "■ ELECTRICAL CHARACTERISTICS".

• On-chip debug function

The on-chip debug function requires that V_{CC}, V_{SS} and 1 serial-wire be connected to an evaluation tool. In addition, if the flash memory data has to be updated, the $\overline{RST}$/PF2 pin must also be connected to the same evaluation tool.

■ PIN ASSIGNMENT



■ PIN DESCRIPTION (MB95220H Series)

Pin no.	Pin name	I/O circuit type*	Function
1	PF0	B	General-purpose I/O port
	X0		Main clock input oscillation pin
2	PF1	B	General-purpose I/O port
	X1		Main clock I/O oscillation pin
3	V_{SS}	—	Power supply pin (GND)
4	PG2	C	General-purpose I/O port
	X1A		Subclock I/O oscillation pin
5	PG1	C	General-purpose I/O port
	X0A		Subclock input oscillation pin
6	V_{CC}	—	Power supply pin
7	PF2	A	General-purpose I/O port
	$\overline{RST}$		Reset pin This pin is a dedicated reset pin in MB95F222H/F223H.
8	C	—	Capacitor connection pin
9	P02	E	General-purpose I/O port
	INT02		External interrupt input pin
	AN02		A/D converter analog input pin
	SCK		LIN-UART clock I/O pin
10	P01	E	General-purpose I/O port
	AN01		A/D converter analog input pin
11	P03	E	General-purpose I/O port
	INT03		External interrupt input pin
	AN03		A/D converter analog input pin
	SOT		LIN-UART data output pin
12	P04	F	General-purpose I/O port
	INT04		External interrupt input pin
	AN04		A/D converter analog input pin
	SIN		LIN-UART data input pin
	HCLK1		External clock input pin
	EC0		8/16-bit composite timer ch. 0 clock input pin

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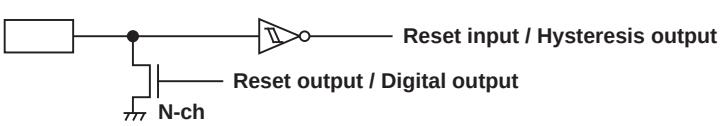
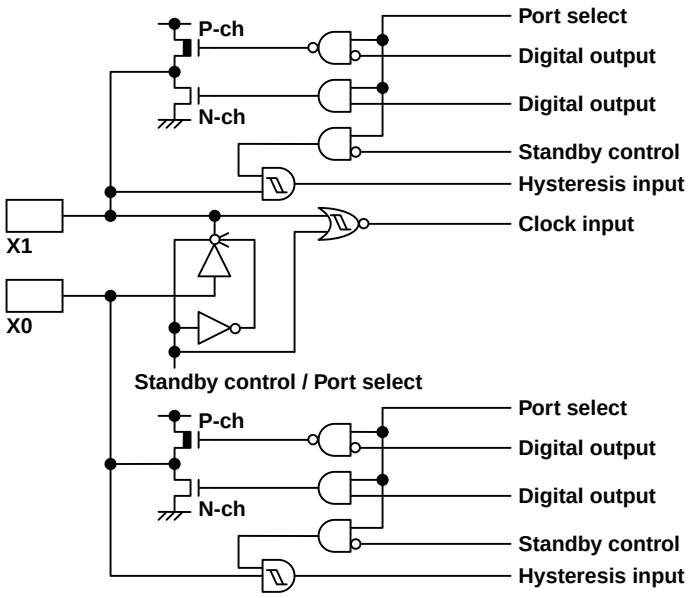
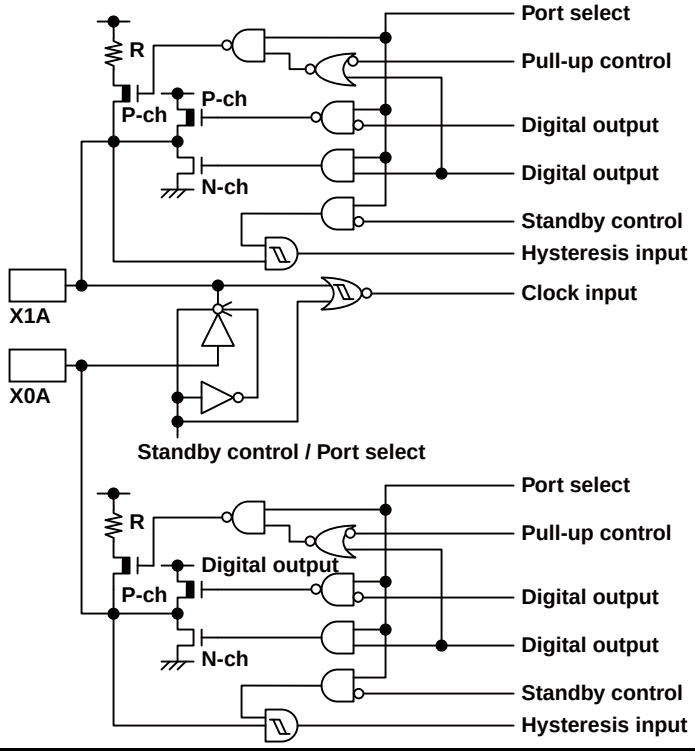
Pin no.	Pin name	I/O circuit type*	Function
13	P05	E	General-purpose I/O port High-current port
	INT05		External interrupt input pin
	AN05		A/D converter analog input pin
	TO00		8/16-bit composite timer ch. 0 clock input pin
	HCLK2		External clock input pin
14	P06	G	General-purpose I/O port High-current port
	INT06		External interrupt input pin
	TO01		8/16-bit composite timer ch. 0 clock input pin
15	P07	G	General-purpose I/O port
	INT07		External interrupt input pin
16	P12	H	General-purpose I/O port
	EC0		8/16-bit composite timer ch. 0 clock input pin
	DBG		DBG input pin

*: For the I/O circuit types, see "■ I/O CIRCUIT TYPE".

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• N-ch open drain output • Hysteresis input • Reset output
B		• Oscillation circuit • High-speed side Feedback resistance: approx. 1 MΩ • CMOS output • Hysteresis input
C		• Oscillation circuit • Low-speed side Feedback resistance: approx. 10 MΩ • CMOS output • Hysteresis input • Pull-up control available

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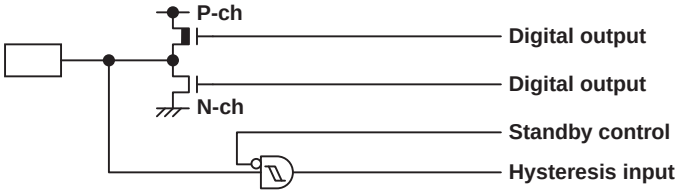
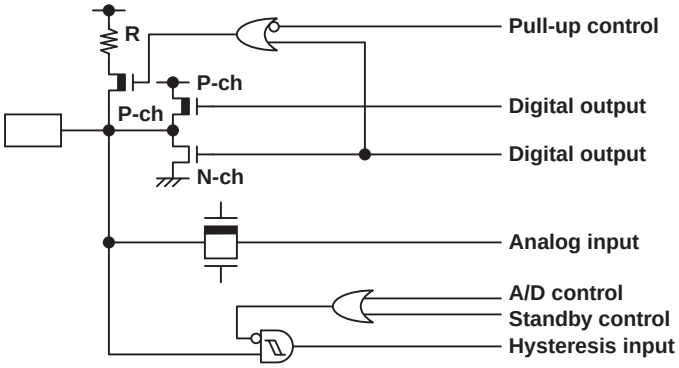
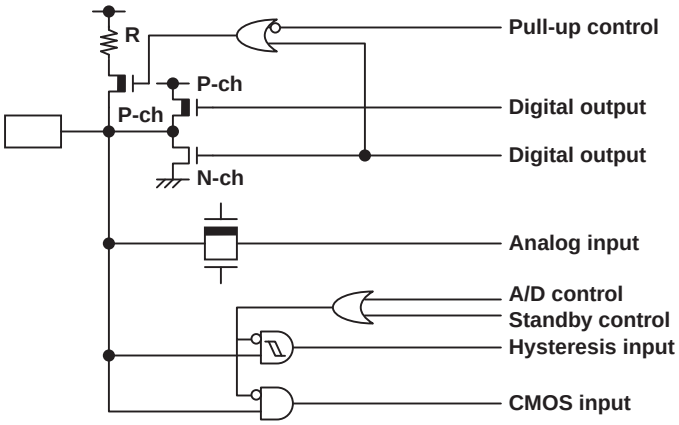
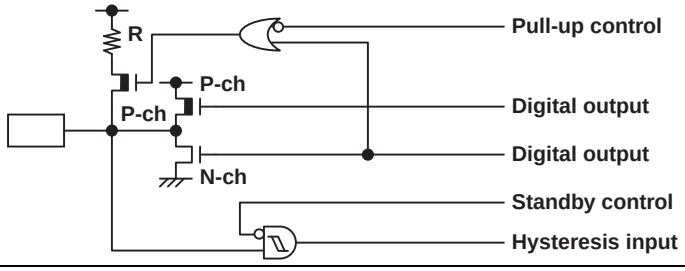
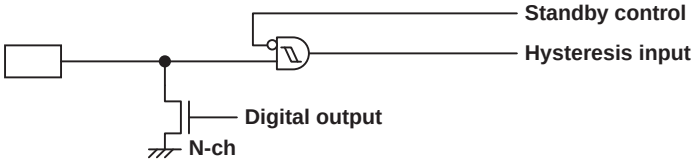
Type	Circuit	Remarks
D		• CMOS output • Hysteresis input
E		• CMOS output • Hysteresis input • Pull-up control available
F		• CMOS output • Hysteresis input • CMOS input • Pull-up control available
G		• Hysteresis input • CMOS output • Pull-up control available
H		• N-ch open drain output • Hysteresis input

■ NOTES ON DEVICE HANDLING

• Preventing latch-ups

When using the device, ensure that the voltage applied does not exceed the maximum voltage rating.
In a CMOS IC, if a voltage higher than V_{CC} or a voltage lower than V_{SS} is applied to an input/output pin that is neither a medium-withstand voltage pin nor a high-withstand voltage pin, or if a voltage out of the rating range of power supply voltage mentioned in 1. Absolute Maximum Ratings of ■ ELECTRICAL CHARACTERISTICS" is applied to the V_{CC} pin or the V_{SS} pin, a latch-up may occur.
When a latch-up occurs, power supply current increases significantly, which may cause a component to be thermally destroyed.

• Stabilizing supply voltage

Supply voltage must be stabilized.
A malfunction may occur when power supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the V_{CC} power supply voltage.
As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in V_{CC} ripple (p-p value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard V_{CC} value, and the transient fluctuation rate does not exceed 0.1 V/ms at a momentary fluctuation such as switching the power supply.

• Notes on using the external clock

When an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from subclock mode or stop mode.

■ PIN CONNECTION

• Treatment of unused pins

If an unused input pin is left unconnected, a component may be permanently damaged due to malfunctions or latch-ups. Always pull up or pull down an unused input pin through a resistor of at least 2 kΩ. Set an unused input/output pin to the output state and leave it unconnected, or set it to the input state and treat it the same as an unused input pin. If there is an unused output pin, leave it unconnected.

• Power supply pins

To reduce unnecessary electro-magnetic emission, prevent malfunctions of strobe signals due to an increase in the ground level, and conform to the total output current standard, always connect the V_{CC} pin and the V_{SS} pin to the power supply and ground outside the device. In addition, connect the current supply source to the V_{CC} pin and the V_{SS} pin with low impedance.
It is also advisable to connect a ceramic capacitor of approximately 0.1 µF as a bypass capacitor between the V_{CC} pin and the V_{SS} pin at a location close to this device.

• DBG pin

Connect the DBG pin directly to an external pull-up resistor.
To prevent the device from unintentionally entering the debug mode due to noise, minimize the distance between the DBG pin and the V_{CC} or V_{SS} pin when designing the layout of the printed circuit board.
The DBG pin should not stay at "L" level after power-on until the reset output is released.

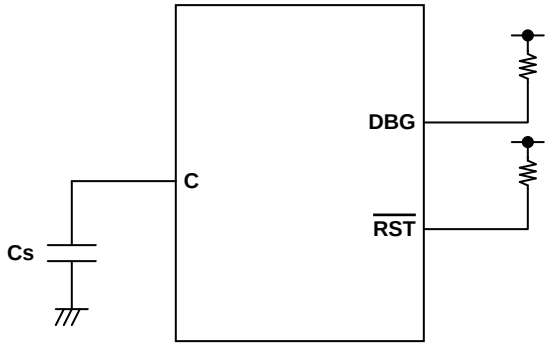
• $\overline{RST}$ pin

Connect the $\overline{RST}$ pin directly to an external pull-up resistor.
To prevent the device from unintentionally entering the reset mode due to noise, minimize the distance between the $\overline{RST}$ pin and the V_{CC} or V_{SS} pin when designing the layout of the printed circuit board.
The $\overline{RST}$/PF2 pin functions as the reset input/output pin after power-on. In addition, the reset output of the $\overline{RST}$/PF2 pin can be enabled by the RSTOE bit of the SYSC register, and the reset input function and the general purpose I/O function can be selected by the RSTEN bit of the SYSC register.

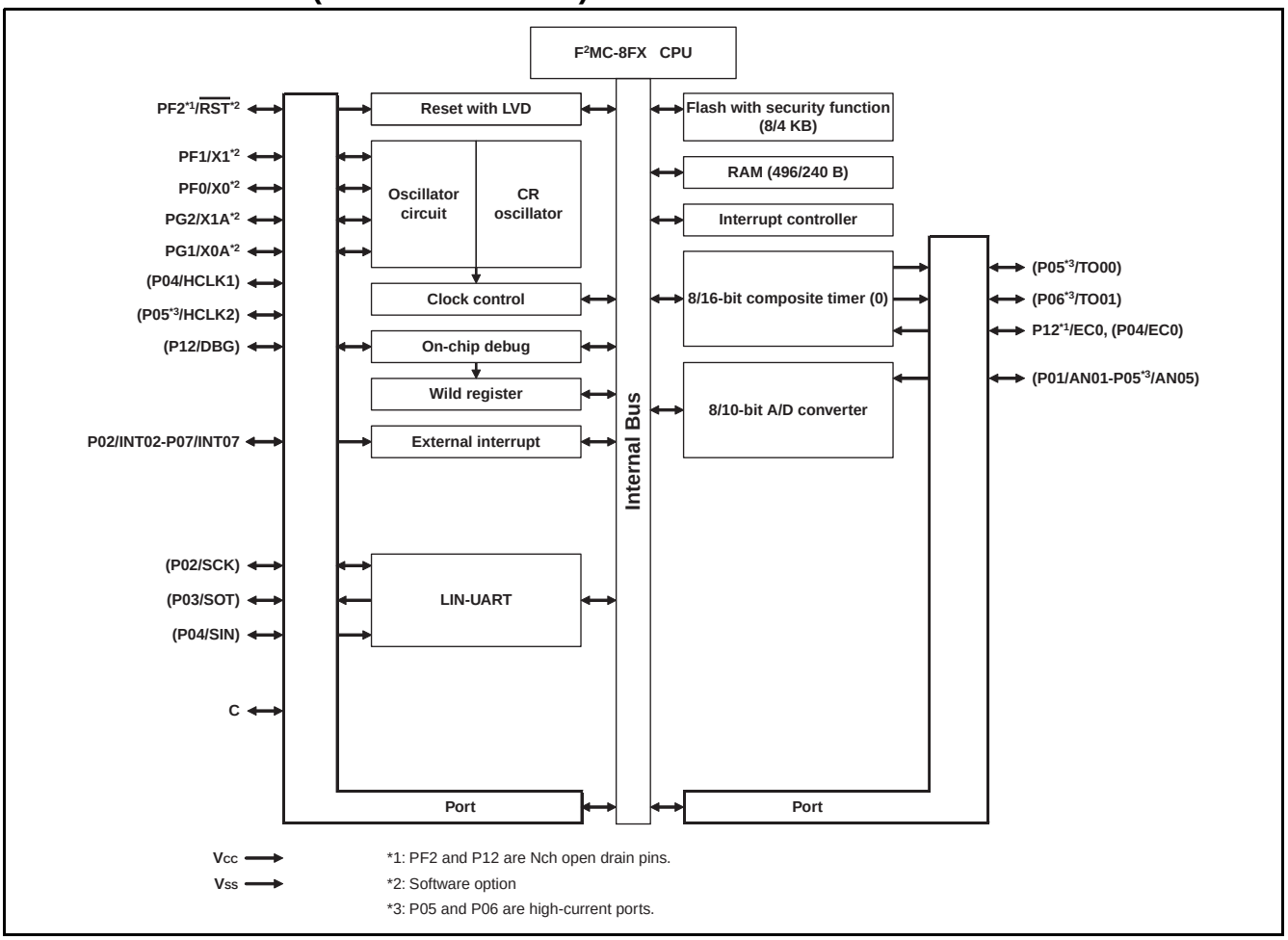
- C pin

  Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The bypass capacitor for the V_{CC} pin must have a capacitance larger than C_S. For the connection to a smoothing capacitor C_S, see the diagram below. To prevent the device from unintentionally entering a mode to which the device is not set to transit due to noise, minimize the distance between the C pin and C_S and the distance between C_S and the V_{SS} pin when designing the layout of a printed circuit board.

- DBG/$\overline{\text{RST}}$/C pin connection diagram



■ BLOCK DIAGRAM (MB95220H Series)

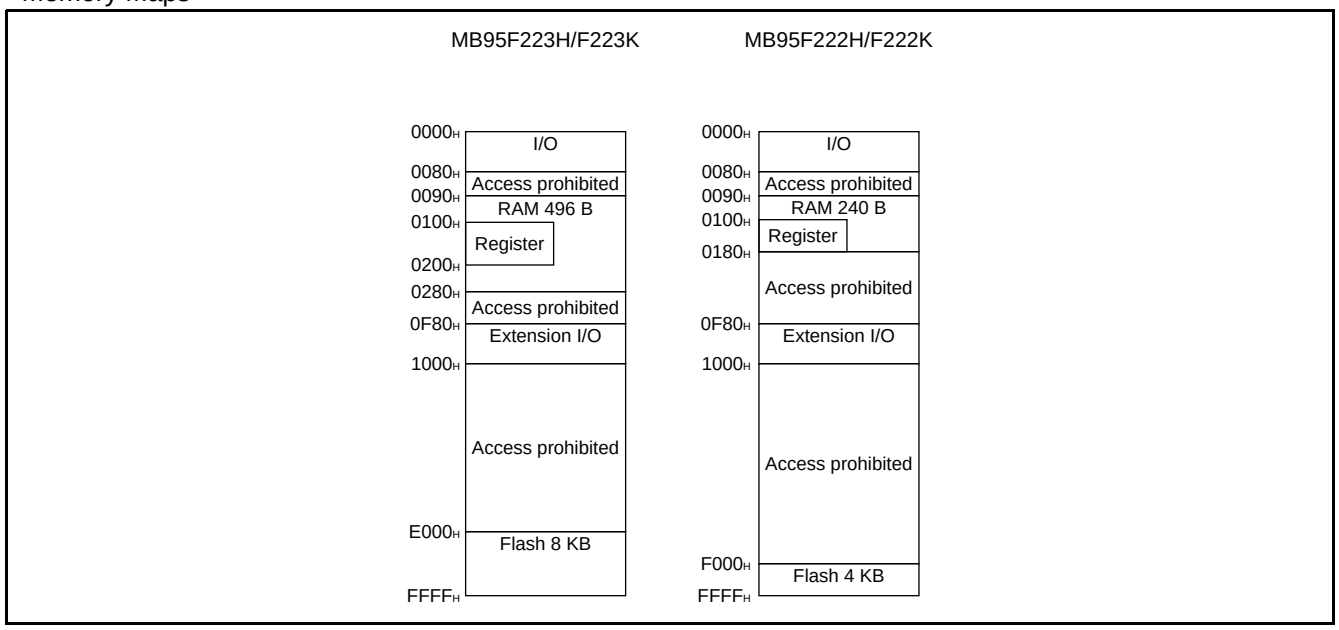


■ CPU CORE

• Memory Space

The memory space of the MB95220H Series is 64 KB in size, and consists of an I/O area, a data area, and a program area. The memory space includes areas intended for specific purposes such as general-purpose registers and a vector table. The memory maps of the MB95220H Series are shown below.

• Memory Maps



■ I/O MAP (MB95220H Series)

Address	Register abbreviation	Register name	R/W	Initial value
0000H	PDR0	Port 0 data register	R/W	00000000B
0001H	DDR0	Port 0 direction register	R/W	00000000B
0002H	PDR1	Port 1 data register	R/W	00000000B
0003H	DDR1	Port 1 direction register	R/W	00000000B
0004H	—	(Disabled)	—	—
0005H	WATR	Oscillation stabilization wait time setting register	R/W	11111111B
0006H	—	(Disabled)	—	—
0007H	SYCC	System clock control register	R/W	0000X011B
0008H	STBC	Standby control register	R/W	00000XXXB
0009H	RSRR	Reset source register	R	XXXXXXXXB
000AH	TBTC	Timebase timer control register	R/W	00000000B
000BH	WPCR	Watch prescaler control register	R/W	00000000B
000CH	WDTC	Watchdog timer control register	R/W	00000000B
000DH	SYCC2	System clock control register 2	R/W	XX100011B
000EH to 0015H	—	(Disabled)	—	—
0016H	—	(Disabled)	—	—
0017H	—	(Disabled)	—	—
0018H to 0027H	—	(Disabled)	—	—
0028H	PDRF	Port F data register	R/W	00000000B
0029H	DDRF	Port F direction register	R/W	00000000B
002AH	PDRG	Port G data register	R/W	00000000B
002BH	DDRG	Port G direction register	R/W	00000000B
002CH	PUL0	Port 0 pull-up register	R/W	00000000B
002DH to 0034H	—	(Disabled)	—	—
0035H	PULG	Port G pull-up register	R/W	00000000B
0036H	T01CR1	8/16-bit composite timer 01 status control register 1 ch. 0	R/W	00000000B
0037H	T00CR1	8/16-bit composite timer 00 status control register 1 ch. 0	R/W	00000000B
0038H	—	(Disabled)	—	—
0039H	—	(Disabled)	—	—
003AH to 0048H	—	(Disabled)	—	—
0049H	EIC10	External interrupt circuit control register ch. 2/ch. 3	R/W	00000000B

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Address	Register abbreviation	Register name	R/W	Initial value
004A$_H$	EIC20	External interrupt circuit control register ch. 4/ch. 5	R/W	00000000$_B$
004B$_H$	EIC30	External interrupt circuit control register ch. 6/ch. 7	R/W	00000000$_B$
004C$_H$ to 004F$_H$	—	(Disabled)	—	—
0050$_H$	SCR	LIN-UART serial control register	R/W	00000000$_B$
0051$_H$	SMR	LIN-UART serial mode register	R/W	00000000$_B$
0052$_H$	SSR	LIN-UART serial status register	R/W	00001000$_B$
0053$_H$	RDR/TDR	LIN-UART receive/transmit data register	R/W	00000000$_B$
0054$_H$	ESCR	LIN-UART extended status control register	R/W	00000100$_B$
0055$_H$	ECCR	LIN-UART extended communication control register	R/W	000000XX$_B$
0056$_H$ to 006B$_H$	—	(Disabled)	—	—
006C$_H$	ADC1	8/10-bit A/D converter control register 1	R/W	00000000$_B$
006D$_H$	ADC2	8/10-bit A/D converter control register 2	R/W	00000000$_B$
006E$_H$	ADDH	8/10-bit A/D converter data register (Upper)	R/W	00000000$_B$
006F$_H$	ADDL	8/10-bit A/D converter data register (Lower)	R/W	00000000$_B$
0070$_H$, 0071$_H$	—	(Disabled)	—	—
0072$_H$	FSR	Flash memory status register	R/W	000X0000$_B$
0073$_H$ to 0075$_H$	—	(Disabled)	—	—
0076$_H$	WREN	Wild register address compare enable register	R/W	00000000$_B$
0077$_H$	WROR	Wild register data test setting register	R/W	00000000$_B$
0078$_H$	—	Mirror of register bank pointer (RP) and direct bank pointer (DP)	—	—
0079$_H$	ILR0	Interrupt level setting register 0	R/W	11111111$_B$
007A$_H$	ILR1	Interrupt level setting register 1	R/W	11111111$_B$
007B$_H$	ILR2	Interrupt level setting register 2	R/W	11111111$_B$
007C$_H$	—	(Disabled)	—	—
007D$_H$	ILR4	Interrupt level setting register 4	R/W	11111111$_B$
007E$_H$	ILR5	Interrupt level setting register 5	R/W	11111111$_B$
007F$_H$	—	(Disabled)	—	—
0F80$_H$	WRARH0	Wild register address setting register (Upper) ch. 0	R/W	00000000$_B$

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Address	Register abbreviation	Register name	R/W	Initial value
0F81H	WRARL0	Wild register address setting register (Lower) ch. 0	R/W	00000000B
0F82H	WRDR0	Wild register data setting register ch. 0	R/W	00000000B
0F83H	WRARH1	Wild register address setting register (Upper) ch. 1	R/W	00000000B
0F84H	WRARL1	Wild register address setting register (Lower) ch. 1	R/W	00000000B
0F85H	WRDR1	Wild register data setting register ch. 1	R/W	00000000B
0F86H	WRARH2	Wild register address setting register (Upper) ch. 2	R/W	00000000B
0F87H	WRARL2	Wild register address setting register (Lower) ch. 2	R/W	00000000B
0F88H	WRDR2	Wild register data setting register ch. 2	R/W	00000000B
0F89H to 0F91H	—	(Disabled)	—	—
0F92H	T01CR0	8/16-bit composite timer 01 status control register 0 ch. 0	R/W	00000000B
0F93H	T00CR0	8/16-bit composite timer 00 status control register 0 ch. 0	R/W	00000000B
0F94H	T01DR	8/16-bit composite timer 01 data register ch. 0	R/W	00000000B
0F95H	T00DR	8/16-bit composite timer 00 data register ch. 0	R/W	00000000B
0F96H	TMCR0	8/16-bit composite timer 00/01 timer mode control register ch. 0	R/W	00000000B
0F97H	—	(Disabled)	—	—
0F98H	—	(Disabled)	—	—
0F99H	—	(Disabled)	—	—
0F9AH	—	(Disabled)	—	—
0F9BH	—	(Disabled)	—	—
0F9CH to 0FBBH	—	(Disabled)	—	—
0FBCH	BGR1	LIN-UART baud rate generator register 1	R/W	00000000B
0FBDH	BGR0	LIN-UART baud rate generator register 0	R/W	00000000B
0FBEH to 0FC2H	—	(Disabled)	—	—
0FC3H	AIDRL	A/D input disable register (Lower)	R/W	00000000B
0FC4H to 0FE3H	—	(Disabled)	—	—
0FE4H	CRTH	Main CR clock trimming register (Upper)	R/W	1XXXXXXXB
0FE5H	CRTL	Main CR clock trimming register (Lower)	R/W	000XXXXXB

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Address	Register abbreviation	Register name	R/W	Initial value
0FE6H, 0FE7H	—	(Disabled)	—	—
0FE8H	SYSC	System configuration register	R/W	11000011B
0FE9H	CMCR	Clock monitoring control register	R/W	00000000B
0FEAH	CMDR	Clock monitoring data register	R/W	00000000B
0FEBH	WDTH	Watchdog timer selection ID register (Upper)	R/W	XXXXXXXXB
0FECH	WDTL	Watchdog timer selection ID register (Lower)	R/W	XXXXXXXXB
0FEDH	—	(Disabled)	—	—
0FEEH	ILSR	Input level select register	R/W	00000000B
0FEFH to 0FFFH	—	(Disabled)	—	—

- R/W access symbols
  - R/W : Readable / Writable
  - R : Read only
  - W : Write only

- Initial value symbols
  - 0 : The initial value of this bit is “0”.
  - 1 : The initial value of this bit is “1”.
  - X : The initial value of this bit is undefined.

Note: Do not write to an address that is “(Disabled)”. If a “(Disabled)” address is read, an undefined value is returned.

■ INTERRUPT SOURCE TABLE (MB95220H Series)

Interrupt source	Interrupt request number	Vector table address		Bit name of interrupt level setting register	Priority order of interrupt sources of the same level (occurring simultaneously)
		Upper	Lower		
External interrupt ch. 4	IRQ0	FFFA$_H$	FFFB$_H$	L00 [1:0]	High
External interrupt ch. 5	IRQ1	FFF8$_H$	FFF9$_H$	L01 [1:0]	
External interrupt ch. 2	IRQ2	FFF6$_H$	FFF7$_H$	L02 [1:0]	
External interrupt ch. 6					
External interrupt ch. 3	IRQ3	FFF4$_H$	FFF5$_H$	L03 [1:0]	
External interrupt ch. 7					
—	IRQ4	FFF2$_H$	FFF3$_H$	L04 [1:0]	
8/16-bit composite timer ch. 0 (Lower)	IRQ5	FFF0$_H$	FFF1$_H$	L05 [1:0]	
8/16-bit composite timer ch. 0 (Upper)	IRQ6	FFEE$_H$	FFEF$_H$	L06 [1:0]	
LIN-UART (reception)	IRQ7	FFEC$_H$	FFED$_H$	L07 [1:0]	
LIN-UART (transmission)	IRQ8	FFEA$_H$	FFEB$_H$	L08 [1:0]	
—	IRQ9	FFE8$_H$	FFE9$_H$	L09 [1:0]	
—	IRQ10	FFE6$_H$	FFE7$_H$	L10 [1:0]	
—	IRQ11	FFE4$_H$	FFE5$_H$	L11 [1:0]	
—	IRQ12	FFE2$_H$	FFE3$_H$	L12 [1:0]	
—	IRQ13	FFE0$_H$	FFE1$_H$	L13 [1:0]	
—	IRQ14	FFDE$_H$	FFDF$_H$	L14 [1:0]	
—	IRQ15	FFDC$_H$	FFDD$_H$	L15 [1:0]	
—	IRQ16	FFDA$_H$	FFDB$_H$	L16 [1:0]	
—	IRQ17	FFD8$_H$	FFD9$_H$	L17 [1:0]	
8/10-bit A/D converter	IRQ18	FFD6$_H$	FFD7$_H$	L18 [1:0]	
Timebase timer	IRQ19	FFD4$_H$	FFD5$_H$	L19 [1:0]	
Watch prescaler	IRQ20	FFD2$_H$	FFD3$_H$	L20 [1:0]	
—	IRQ21	FFD0$_H$	FFD1$_H$	L21 [1:0]	
—	IRQ22	FFCE$_H$	FFCF$_H$	L22 [1:0]	
Flash memory	IRQ23	FFCC$_H$	FFCD$_H$	L23 [1:0]	Low

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS}–0.3	V_{SS}+6	V	
Input voltage*1	V_I	V_{SS}–0.3	V_{SS}+6	V	*2
Output voltage*1	V_O	V_{SS}–0.3	V_{SS}+6	V	*2
Maximum clamp current	I_{CLAMP}	-2	+2	mA	Applicable to specific pins*3
Total maximum clamp current	$\Sigma\lvert I_{CLAMP}\rvert$	—	20	mA	Applicable to specific pins*3
"L" level maximum output current	I_{OL1}	—	15	mA	Other than P05, P06
	I_{OL2}		15		P05, P06
"L" level average current	I_{OLAV1}	—	4	mA	Other than P05, P06 Average output current = operating current × operating ratio (1 pin)
	I_{OLAV2}		12		P05, P06 Average output current = operating current × operating ratio (1 pin)
"L" level total maximum output current	ΣI_{OL}	—	100	mA	
"L" level total average output current	ΣI_{OLAV}	—	50	mA	Total average output current = operating current × operating ratio (Total number of pins)
"H" level maximum output current	I_{OH1}	—	-15	mA	Other than P05, P06
	I_{OH2}		-15		P05, P06
"H" level average current	I_{OHAV1}	—	-4	mA	Other than P05, P06 Average output current = operating current × operating ratio (1 pin)
	I_{OHAV2}		-8		P05, P06 Average output current = operating current × operating ratio (1 pin)
"H" level total maximum output current	ΣI_{OH}	—	-100	mA	
"H" level total average output current	ΣI_{OHAV}	—	-50	mA	Total average output current = operating current × operating ratio (Total number of pins)
Power consumption	Pd	—	320	mW	
Operating temperature	T_A	-40	+85	°C	
Storage temperature	Tstg	-55	+150	°C	

(Continued)

(Continued)

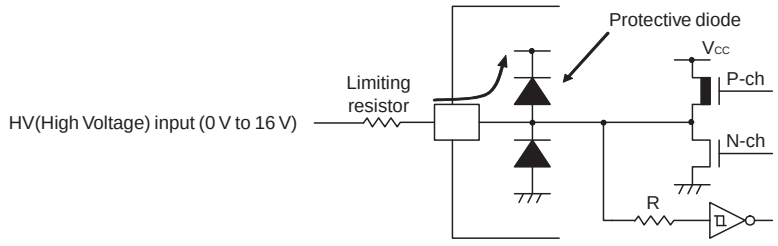
*1: The parameter is based on V_{SS} = 0.0 V.

*2: V_I and V_O must not exceed V_{CC}+0.3 V. V_I must not exceed the rated voltage. However, if the maximum current to/from an input is limited by means of an external component, the I_{CLAMP} rating is used instead of the V_I rating.

*3: Applicable to the following pins: P01 to P07, PG1, PG2, PF0, PF1

- Use under recommended operating conditions.
- Use with DC voltage (current).
- The HV (High Voltage) signal is an input signal exceeding the V_{CC} voltage. Always connect a limiting resistor between the HV (High Voltage) signal and the microcontroller before applying the HV (High Voltage) signal.
- The value of the limiting resistor should be set to a value at which the current to be input to the microcontroller pin when the HV (High Voltage) signal is input is below the standard value, irrespective of whether the current is transient current or stationary current.
- When the microcontroller drive current is low, such as in low power consumption modes, the HV (High Voltage) input potential may pass through the protective diode to increase the potential of the V_{CC} pin, affecting other devices.
- If the HV (High Voltage) signal is input when the microcontroller power supply is off (not fixed at 0 V), since power is supplied from the pins, incomplete operations may be executed.
- If the HV (High Voltage) input is input after power-on, since power is supplied from the pins, the voltage of power supply may not be sufficient to enable a power-on reset.
- Do not leave the HV (High Voltage) input pin unconnected.
- Example of a recommended circuit:

- Input/Output equivalent circuit



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS} = 0.0 V)

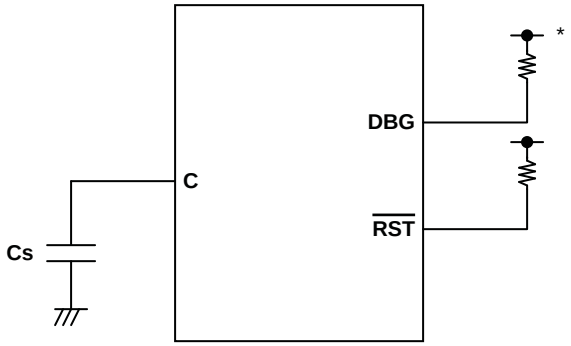
Parameter	Symbol	Value		Unit	Remarks	
		Min	Max			
Power supply voltage	V_{CC}	2.4*1*2	5.5*1	V	In normal operation	Other than on-chip debug mode
		2.3	5.5		Hold condition in stop mode	
		2.9	5.5		In normal operation	On-chip debug mode
		2.3	5.5		Hold condition in stop mode	
Smoothing capacitor	C_S	0.022	1	µF	*3	
Operating temperature	T_A	-40	+85	°C	Other than on-chip debug mode	
		+5	+35		On-chip debug mode	

*1: The value varies depending on the operating frequency, the machine clock and the analog guaranteed range.

*2: The value is 2.88 V when the low-voltage detection reset is used.

*3: Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The bypass capacitor for the V_{CC} pin must have a capacitance larger than C_S. For the connection to a smoothing capacitor C_S, see the diagram below. To prevent the device from unintentionally entering an unknown mode due to noise, minimize the distance between the C pin and C_S and the distance between C_S and the V_{SS} pin when designing the layout of a printed circuit board.

- DBG / $\overline{\text{RST}}$ / C pin connection diagram



*: Since the DBG pin becomes a communication pin in on-chip debug mode, set a pull-up resistor value suiting the input/output specifications of P12/DBG.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

3. DC Characteristics

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IHI}	P04	*1	0.7 V_{CC}	—	V_{CC}+0.3	V	When CMOS input level (hysteresis input) is selected
	V_{IHS}	P01 to P07, P12, PF0, PF1, PG1, PG2	*1	0.8 V_{CC}	—	V_{CC}+0.3	V	Hysteresis input
	V_{IHM}	PF2	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
"L" level input voltage	V_{IL}	P04	*1	V_{SS}–0.3	—	0.3 V_{CC}	V	When CMOS input level (hysteresis input) is selected
	V_{ILS}	P01 to P07, P12, PF0, PF1, PG1, PG2	*1	V_{SS}–0.3	—	0.2 V_{CC}	V	Hysteresis input
	V_{ILM}	PF2	—	V_{SS}–0.3	—	0.3 V_{CC}	V	Hysteresis input
Open-drain output application voltage	V_D	PF2, P12	—	V_{SS}–0.3	—	0.2 V_{CC}	V	
"H" level output voltage	V_{OH1}	Output pins other than P05, P06, P12, PF2	I_{OH} = -4 mA	V_{CC}–0.5	—	—	V	
	V_{OH2}	P05, P06	I_{OH} = -8 mA	V_{CC}–0.5	—	—	V	
"L" level output voltage	V_{OL1}	Output pins other than P05, P06	I_{OL} = 4 mA	—	—	0.4	V	
	V_{OL2}	P05, P06	I_{OL} = 12 mA	—	—	0.4	V	
Input leak current (Hi-Z output leak current)	I_{LI}	All input pins	0.0 V < V_I < V_{CC}	-5	—	+5	µA	When pull-up resistance is disabled
Pull-up resistance	R_{PULL}	P01 to P07, PG1, PG2	V_I = 0 V	25	50	100	kΩ	When pull-up resistance is enabled
Input capacitance	C_{IN}	Other than V_{CC} and V_{SS}	f = 1 MHz	—	5	15	pF	

(Continued)

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*2	I_{CC}	V_{CC} (External clock operation)	V_{CC} = 5.5 V F_{CH} = 32 MHz F_{MP} = 16 MHz Main clock mode (divided by 2)	—	13	17	mA	Flash memory product (except writing and erasing)
				—	33.5	39.5	mA	Flash memory product (at writing and erasing)
				—	15	21	mA	At A/D conversion
	I_{CCS}		V_{CC} = 5.5 V F_{CH} = 32 MHz F_{MP} = 16 MHz Main sleep mode (divided by 2)	—	5.5	9	mA	
	I_{CCL}		V_{CC} = 5.5 V F_{CL} = 32 kHz F_{MPL} = 16 kHz Subclock mode (divided by 2) T_A = +25°C	—	65	153	µA	
	I_{CCLS}		V_{CC} = 5.5 V F_{CL} = 32 kHz F_{MPL} = 16 kHz Subsleep mode (divided by 2) T_A = +25°C	—	10	84	µA	
	I_{CCT}		V_{CC} = 5.5 V F_{CL} = 32 kHz Watch mode Main stop mode T_A = +25°C	—	5	30	µA	
	I_{CCMCR}	V_{CC}	V_{CC} = 5.5 V F_{CRH} = 10 MHz F_{MP} = 10 MHz Main CR clock mode	—	8.6	—	mA	
	I_{CCSCR}		V_{CC} = 5.5 V Sub-CR clock mode (divided by 2) T_A = +25°C	—	110	410	µA	

(Continued)

(Continued)

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*2	I_{CCTS}	V_{CC} (External clock operation)	V_{CC} = 5.5 V F_{CH} = 32 MHz Timebase timer mode T_A = +25°C	—	1.1	3	mA	
	I_{CCH}		V_{CC} = 5.5 V Substop mode T_A = +25°C	—	3.5	22.5	µA	Main stop mode for single clock selection
	I_{LVD}	V_{CC}	Current consumption for low-voltage detection circuit only	—	37	54	µA	
	I_{CRH}		Current consumption for the internal main CR oscillator	—	0.5	0.6	mA	
	I_{CRL}		Current consumption for the internal sub-CR oscillator oscillating at 100 kHz	—	20	72	µA	

*1: The input level of P04 can be switched between “CMOS input level” and “hysteresis input level”. The input level selection register (ILSR) is used to switch between the two input levels.

*2:
- The power supply current is determined by the external clock. When the low-voltage detection option is selected, the power-supply current will be the sum of adding the current consumption of the low-voltage detection circuit (I_{LVD}) to one of the value from I_{CC} to I_{CCH}. In addition, when both the low-voltage detection option and the internal CR oscillator are selected, the power supply current will be the sum of adding up the current consumption of the low-voltage detection circuit, the current consumption of the internal CR oscillators (I_{CRH}, I_{CRL}) and a specified value. In on-chip debug mode, the internal CR oscillator (I_{CRH}) and the low-voltage detection circuit are always enabled, and current consumption therefore increases accordingly.
- See "4. AC Characteristics: (1) Clock Timing" for F_{CH} and F_{CL}.
- See "4. AC Characteristics: (2) Source Clock/Machine Clock" for F_{MP} and F_{MPL}.

4. AC Characteristics

(1) Clock Timing

(V_{CC} = 2.4 V to 5.5 V, V_{SS} = 0.0 V, T_A = -40°C to +85°C)

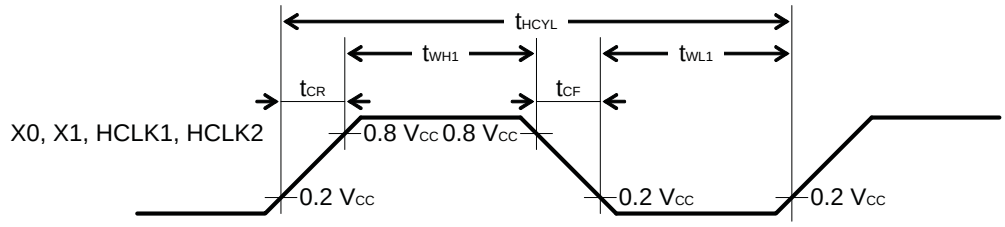
Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_{CH}	X0, X1	—	1	—	16.25	MHz	When the main oscillation circuit is used
		X0, HCLK1, HCLK2	X1 open	1	—	12	MHz	When the main external clock is used
		X0, X1, HCLK1, HCLK2	—	1	—	32.5	MHz	
	F_{CRH}	—	—	9.7	10	10.3	MHz	When the main internal clock is used 2.4 V ≤ Vcc < 5.5 V(0 °C ≤ T_A ≤ 40 °C)
				7.76	8	8.24	MHz	
				0.97	1	1.03	MHz	
				9.5	10	10.5	MHz	When the main internal clock is used 2.4 V ≤ Vcc < 5.5 V (-40 °C ≤ T_A < 0 °C, 40 °C < T_A ≤ 85 °C)
				7.6	8	8.4	MHz	
				0.95	1	1.05	MHz	
	F_{CL}	X0A, X1A	—	—	32.768	—	kHz	When the sub oscillation circuit is used
				—	32.768	—	kHz	When the sub-external clock is used
	F_{CRL}	—	—	50	100	200	kHz	When the sub-internal CR clock is used
Clock cycle time	t_{HCYL}	X0, X1	—	61.5	—	1000	ns	When the main oscillation circuit is used
		X0, HCLK1, HCLK2	X1 open	83.4	—	1000	ns	When the external clock is used
		X0, X1, HCLK1, HCLK2	—	30.8	—	1000	ns	
	t_{LCYL}	X0A, X1A	—	—	30.5	—	µs	When the subclock is used

(Continued)

(Continued)

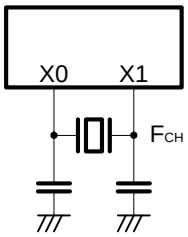
(V_{CC} = 2.4 V to 5.5 V, V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input clock pulse width	t_{WH1} t_{WL1}	X0, HCLK1, HCLK2	X1 open	33.4	—	—	ns	When the external clock is used, the duty ratio should range between 40% and 60%.
		X0, X1, HCLK1, HCLK2	—	12.4	—	—	ns	
	t_{WH2} t_{WL2}	X0A	—	—	15.2	—	µs	
Input clock rise time and fall time	t_{CR} t_{CF}	X0, HCLK1, HCLK2	X1 open	—	—	5	ns	When the external clock is used
		X0, X1, HCLK1, HCLK2	—	—	—	5	ns	
Internal CR oscillation start time	t_{CRHWK}	—	—	—	—	80	µs	When the main internal CR clock is used
	t_{CRLWK}	—	—	—	—	10	µs	When the sub-internal CR clock is used

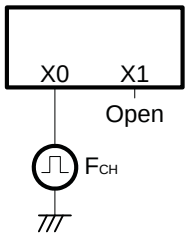


- Figure of main clock input port external connection

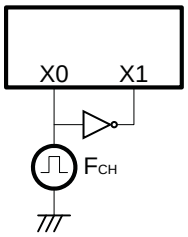
When a crystal oscillator or a ceramic oscillator is used

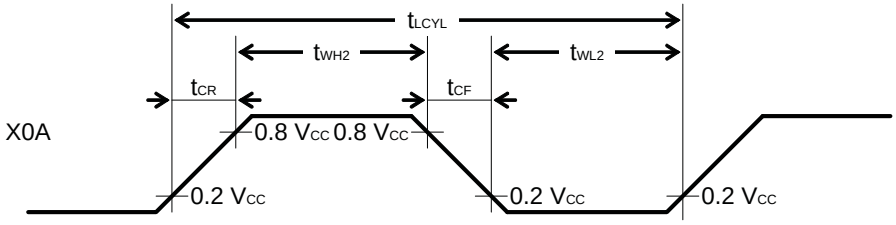


When the external clock is used (X1 is open)



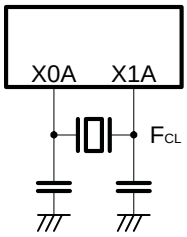
When the external clock is used



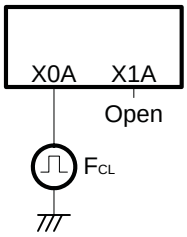


- Figure of subclock input port external connection

When a crystal oscillator or a ceramic oscillator is used



When the external clock is used



(2) Source Clock/Machine Clock

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Source clock cycle time*1 (clock before division)	t_{SCLK}	—	61.5	—	2000	ns	When the main external clock is used Min: F_{CH} = 32.5 MHz, divided by 2 Max: F_{CH} = 1 MHz, divided by 2
			100	—	1000	ns	When the main CR clock is used Min: F_{CRH} = 10 MHz Max: F_{CRH} = 1 MHz
			—	61	—	µs	When the sub-oscillation clock is used F_{CL} = 32.768 kHz, divided by 2
			—	20	—	µs	When the sub-oscillation clock is used F_{CRL} = 100 kHz, divided by 2
Source clock frequency	F_{SP}	—	0.5	—	16.25	MHz	When the main oscillation clock is used
			1	—	10	MHz	When the main CR clock is used
	F_{SPL}		—	16.384	—	kHz	When the sub-oscillation clock is used
			—	50	—	kHz	When the sub-CR clock is used F_{CRL} = 100 kHz, divided by 2
Machine clock cycle time*2 (minimum instruction execution time)	t_{MCLK}	—	61.5	—	32000	ns	When the main oscillation clock is used Min: F_{SP} = 16.25 MHz, no division Max: F_{SP} = 0.5 MHz, divided by 16
			100	—	16000	ns	When the main CR clock is used Min: F_{SP} = 10 MHz Max: F_{SP} = 1 MHz, divided by 16
			61	—	976.5	µs	When the sub-oscillation clock is used Min: F_{SPL} = 16.384 kHz, no division Max: F_{SPL} = 16.384 kHz, divided by 16
			20	—	320	µs	When the sub-CR clock is used Min: F_{SPL} = 50 kHz, no division Max: F_{SPL} = 50 kHz, divided by 16
Machine clock frequency	F_{MP}	—	0.031	—	16.25	MHz	When the main oscillation clock is used
			0.0625	—	10	MHz	When the main CR clock is used
	F_{MPL}		1.024	—	16.384	kHz	When the sub-oscillation clock is used
			3.125	—	50	kHz	When the sub-CR clock is used F_{CRL} = 100 kHz

*1: This is the clock before it is divided according to the division ratio set by the machine clock division ratio selection bits (SYCC : DIV1 and DIV0) . This source clock is divided to become a machine clock according to the division ratio set by the machine clock division ratio selection bits (SYCC : DIV1 and DIV0) . In addition, a source clock can be selected from the following.

- Main clock divided by 2
- Main CR clock
- Subclock divided by 2
- Sub-CR clock divided by 2

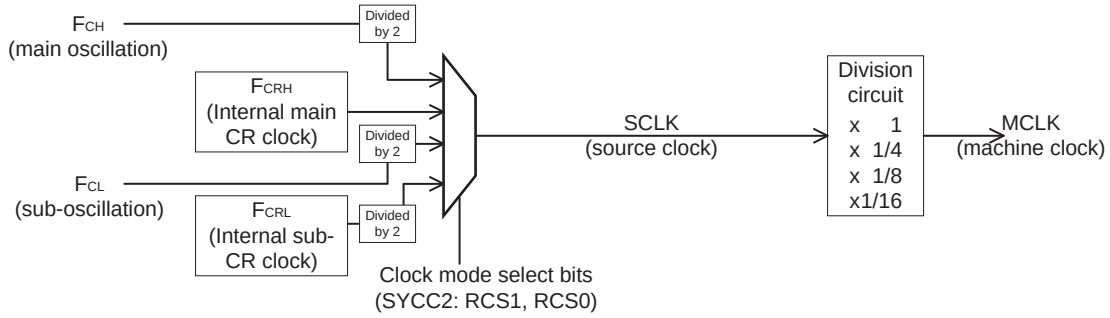
(Continued)

(Continued)

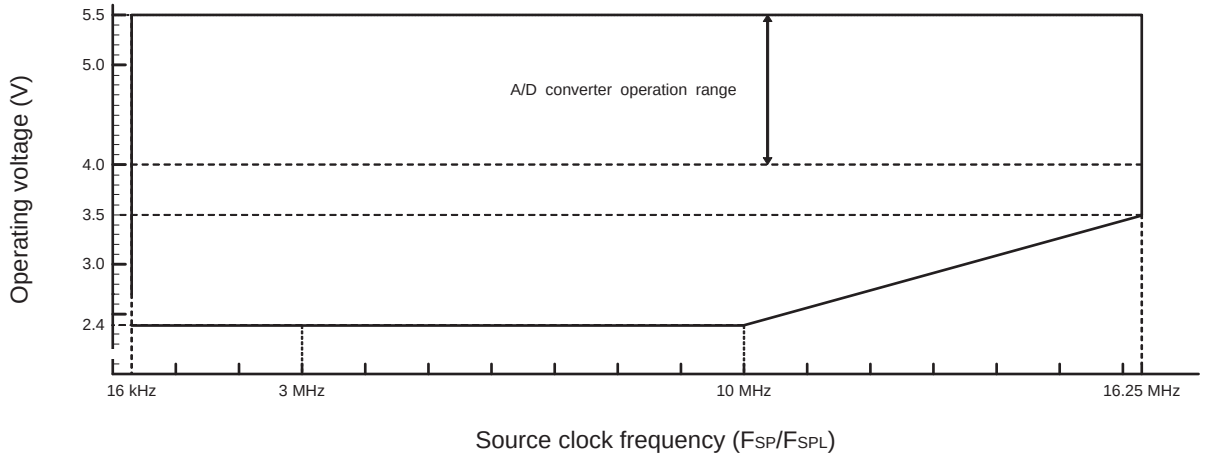
*2: This is the operating clock of the microcontroller. A machine clock can be selected from the following.

- Source clock (no division)
- Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

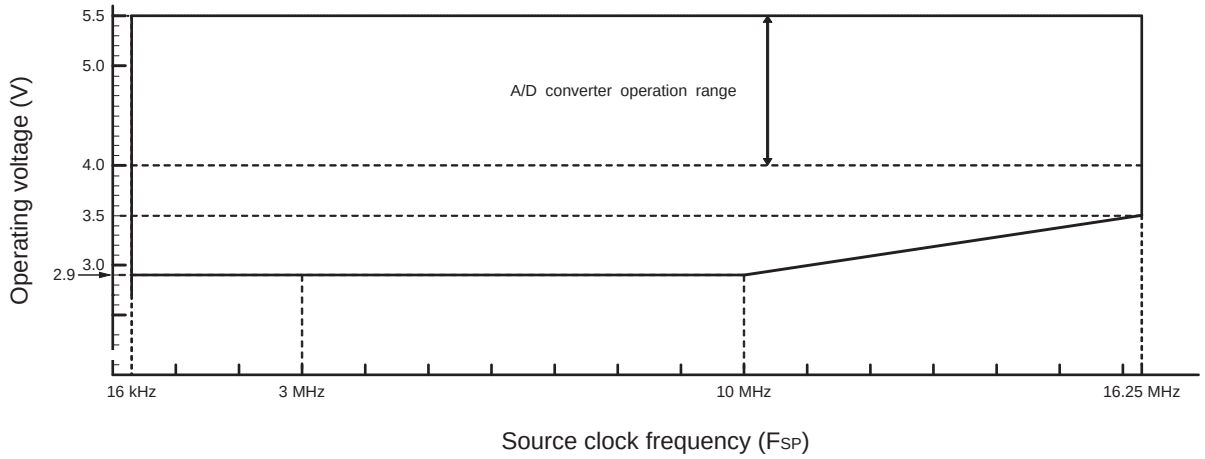
- Schematic diagram of the clock generation block



- Operating voltage - Operating frequency (When T_A = -40°C to +85°C)
  MB95220H (without the on-chip debug function)



- Operating voltage - Operating frequency (When T_A = -40°C to +85°C)
  MB95220H (with the on-chip debug function)



(3) External Reset

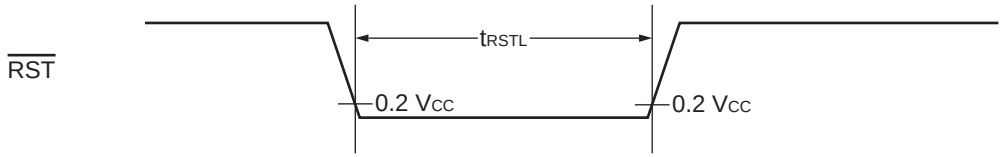
(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
$\overline{RST}$ "L" level pulse width	t_{RSTL}	2 t_{MCLK}*1	—	ns	In normal operation
		Oscillation time of the oscillator*2+100	—	µs	In stop mode, subclock mode, sub-sleep mode, and watch mode
		100	—	µs	In timebase timer mode

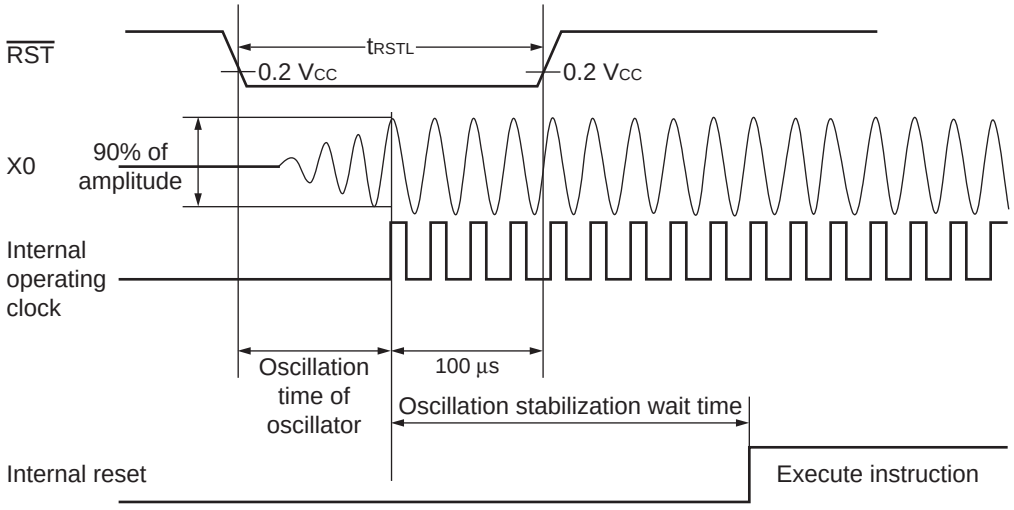
*1: See " (2) Source Clock/Machine Clock" for t_{MCLK}.

*2: The oscillation time of an oscillator is the time for it to reach 90% of its amplitude. The crystal oscillator has an oscillation time of between several ms and tens of ms. The ceramic oscillator has an oscillation time of between hundreds of µs and several ms. The external clock has an oscillation time of 0 ms. The CR oscillator clock has an oscillation time of between several µs and several ms.

- In normal operation



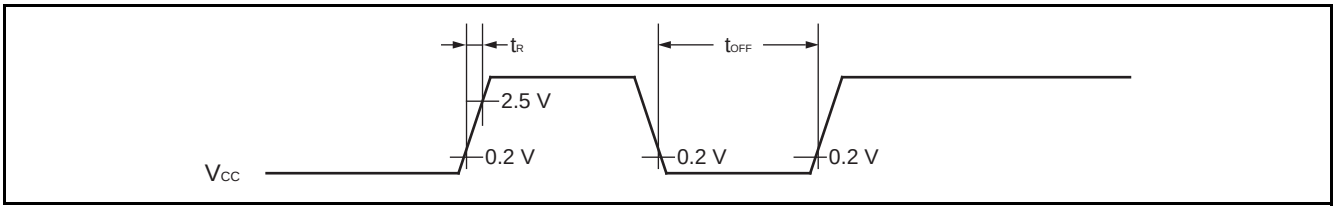
- In stop mode, subclock mode, subsleep mode, watch mode and power-on



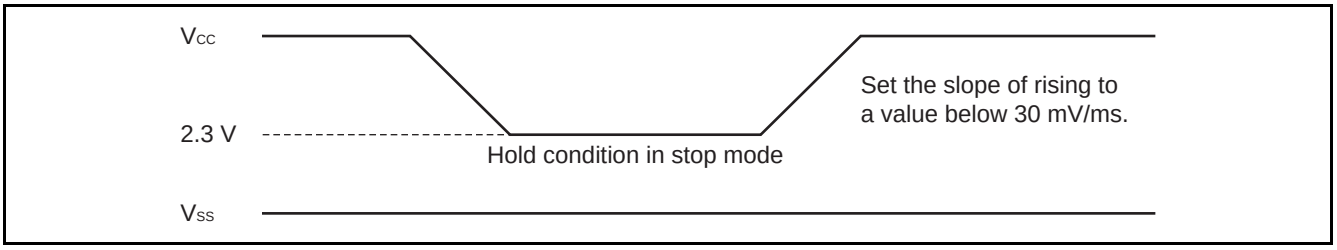
(4) Power-on Reset

(V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Power supply rising time	t_R	—	—	50	ms	
Power supply cutoff time	t_{OFF}	—	1	—	ms	Wait time until power-on



Note: A sudden change of power supply voltage may activate the power-on reset function. When changing the power supply voltage during the operation, set the slope of rising to a value below within 30 mV/ms as shown below.

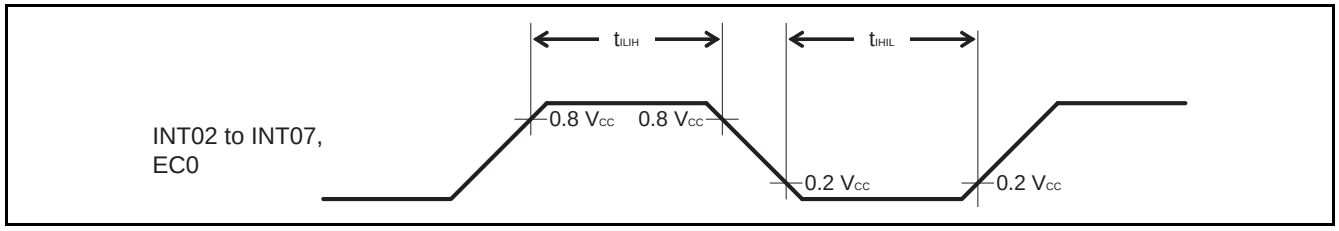


(5) Peripheral Input Timing

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
Peripheral input “H” pulse width	t_{ILIH}	INT02 to INT07, EC0	2 t_{MCLK}*	—	ns
Peripheral input “L” pulse width	t_{IHIL}		2 t_{MCLK}*	—	ns

* See “(2) Source Clock/Machine Clock” for t_{MCLK}.



(6) LIN-UART Timing (Available only in MB95F222H/F222K/F223H/F223K)

Sampling is executed at the rising edge of the sampling clock*1, and serial clock delay is disabled*2. (ESCR register:SCES bit = 0, ECCR register:SCDE bit = 0)

(V_{CC} = 5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = -40°C to +85°C)

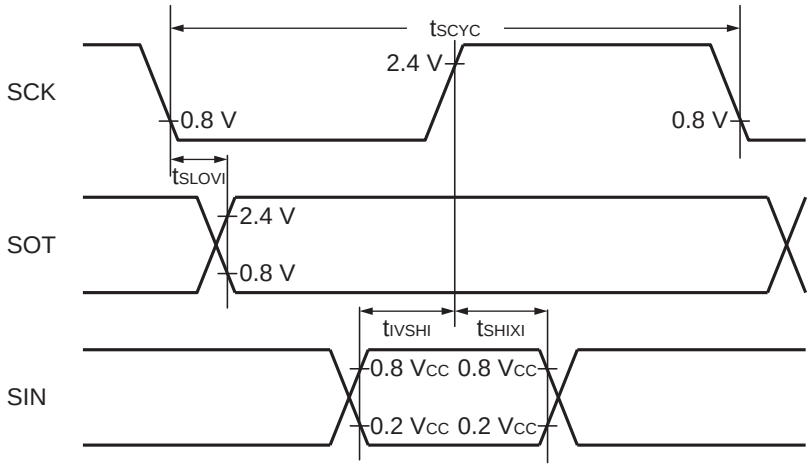
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF+1 TTL	5 t_{MCLK}*3	—	ns
SCK ↓→ SOT delay time	t_{SLOVI}	SCK, SOT		-95	+95	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK, SIN		t_{MCLK}*3+190	—	ns
SCK ↑→ valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK	External clock operation output pin: C_L = 80 pF+1 TTL	3 t_{MCLK}*3–t_R	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK		t_{MCLK}*3+95	—	ns
SCK ↓→ SOT delay time	t_{SLOVE}	SCK, SOT		—	2 t_{MCLK}*3+95	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCK, SIN		190	—	ns
SCK ↑→ valid SIN hold time	t_{SHIXE}	SCK, SIN		t_{MCLK}*3+95	—	ns
SCK fall time	t_F	SCK		—	10	ns
SCK rise time	t_R	SCK		—	10	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

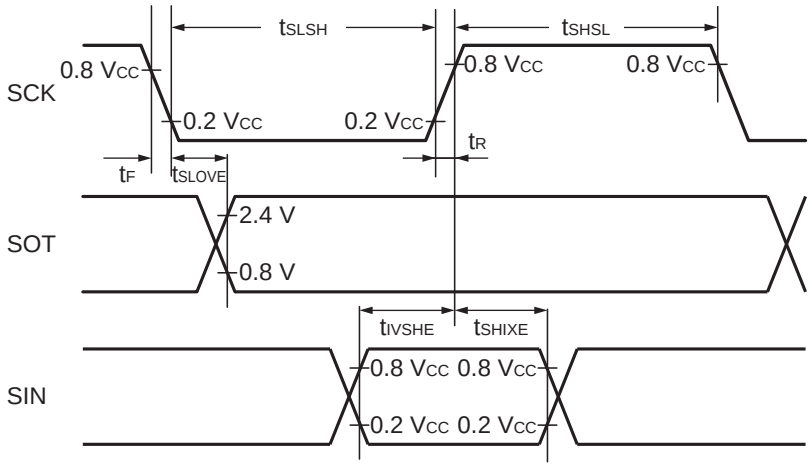
*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

*3: See “(2) Source Clock/Machine Clock” for t_{MCLK}.

- Internal shift clock mode



- External shift clock mode



Sampling is executed at the falling edge of the sampling clock*1, and serial clock delay is disabled*2. (ESCR register:SCES bit = 1, ECCR register:SCDE bit = 0)

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = -40°C to +85°C)

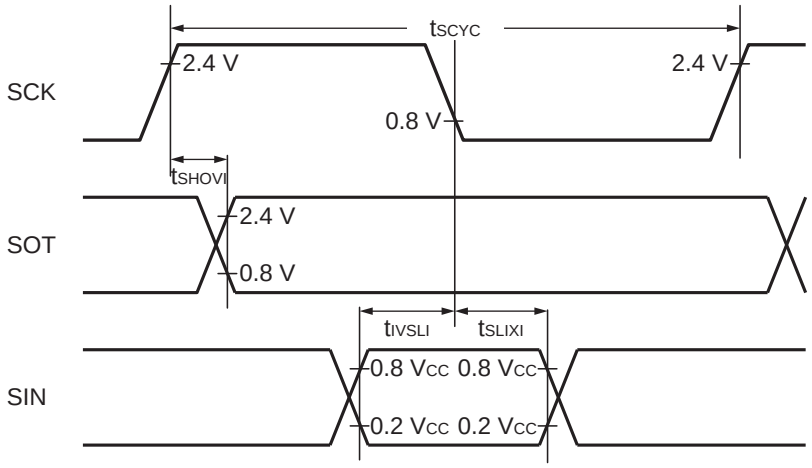
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF+1 TTL	5 t_{MCLK}*3	—	ns
SCK ↑→ SOT delay time	t_{SHOVI}	SCK, SOT		-95	+95	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK, SIN		t_{MCLK}*3+190	—	ns
SCK ↓→ valid SIN hold time	t_{SLIXI}	SCK, SIN		0	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK	External clock operation output pin: C_L = 80 pF+1 TTL	3 t_{MCLK}*3–t_R	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK		t_{MCLK}*3+95	—	ns
SCK ↑→ SOT delay time	t_{SHOVE}	SCK, SOT		—	2 t_{MCLK}*3+95	ns
Valid SIN → SCK ↓	t_{IVSLE}	SCK, SIN		190	—	ns
SCK ↓→ valid SIN hold time	t_{SLIXE}	SCK, SIN		t_{MCLK}*3+95	—	ns
SCK fall time	t_F	SCK		—	10	ns
SCK rise time	t_R	SCK		—	10	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

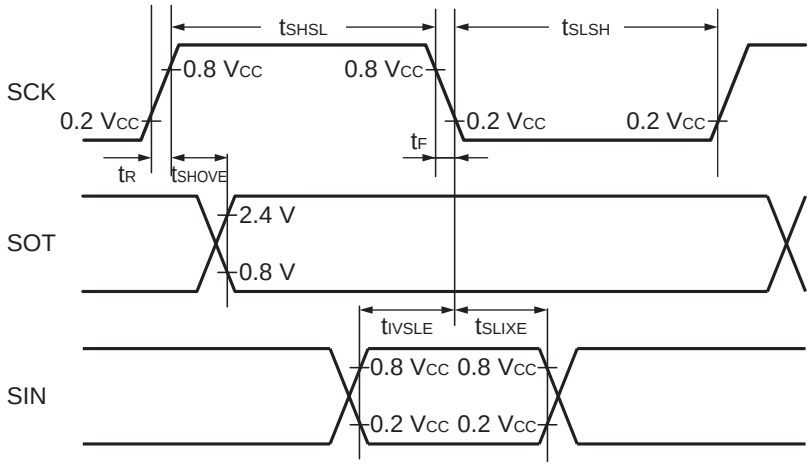
*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

*3: See “(2) Source Clock/Machine Clock” for t_{MCLK}.

- Internal shift clock mode



- External shift clock mode



Sampling is executed at the rising edge of the sampling clock*1, and serial clock delay is enabled*2. (ESCR register:SCES bit = 0, ECCR register:SCDE bit = 1)

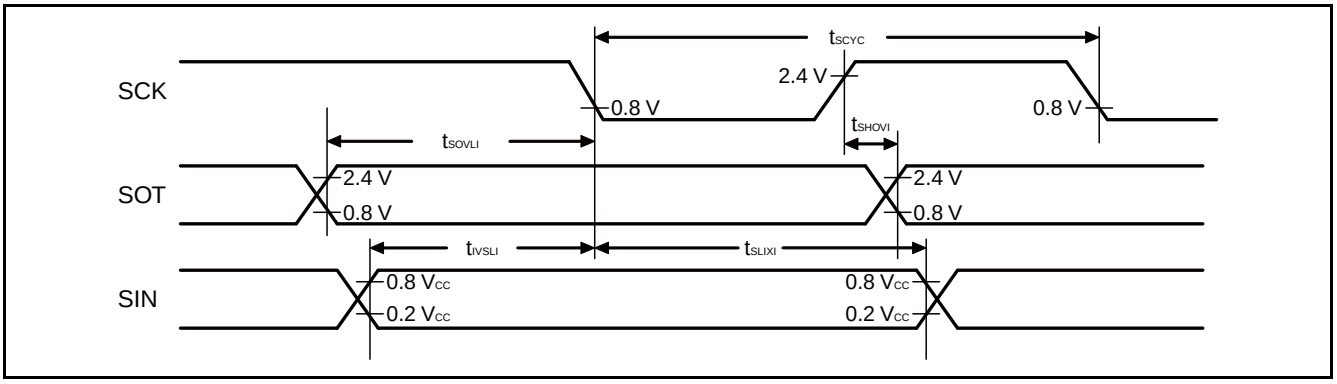
(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF+1 TTL	5 t_{MCLK}*3	—	ns
SCK ↑→ SOT delay time	t_{SHOVI}	SCK, SOT		-95	+95	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK, SIN		t_{MCLK}*3+190	—	ns
SCK ↓→ valid SIN hold time	t_{SLIXI}	SCK, SIN		0	—	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCK, SOT		—	4 t_{MCLK}*3	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function that delays the output signal of the serial clock for half clock.

*3: See “(2) Source Clock/Machine Clock” for t_{MCLK}.



Sampling is executed at the falling edge of the sampling clock*1, and serial clock delay is enabled*2. (ESCR register:SCES bit = 1, ECCR register:SCDE bit = 1)

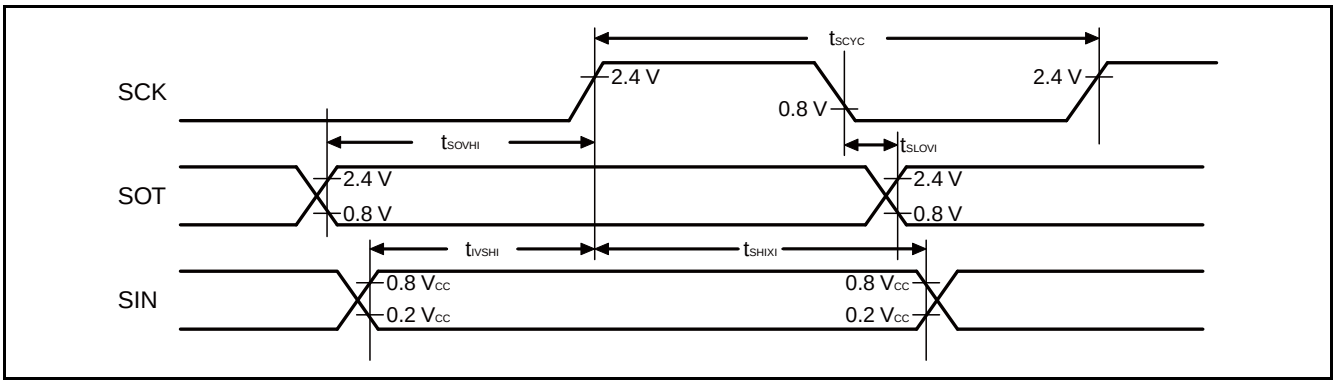
(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF+1 TTL	5 t_{MCLK}*3	—	ns
SCK ↓→ SOT delay time	t_{SLOVI}	SCK, SOT		-95	+95	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK, SIN		t_{MCLK}*3+190	—	ns
SCK ↑→ valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCK, SOT		—	4 t_{MCLK}*3	ns

*1:There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function that delays the output signal of the serial clock for half clock.

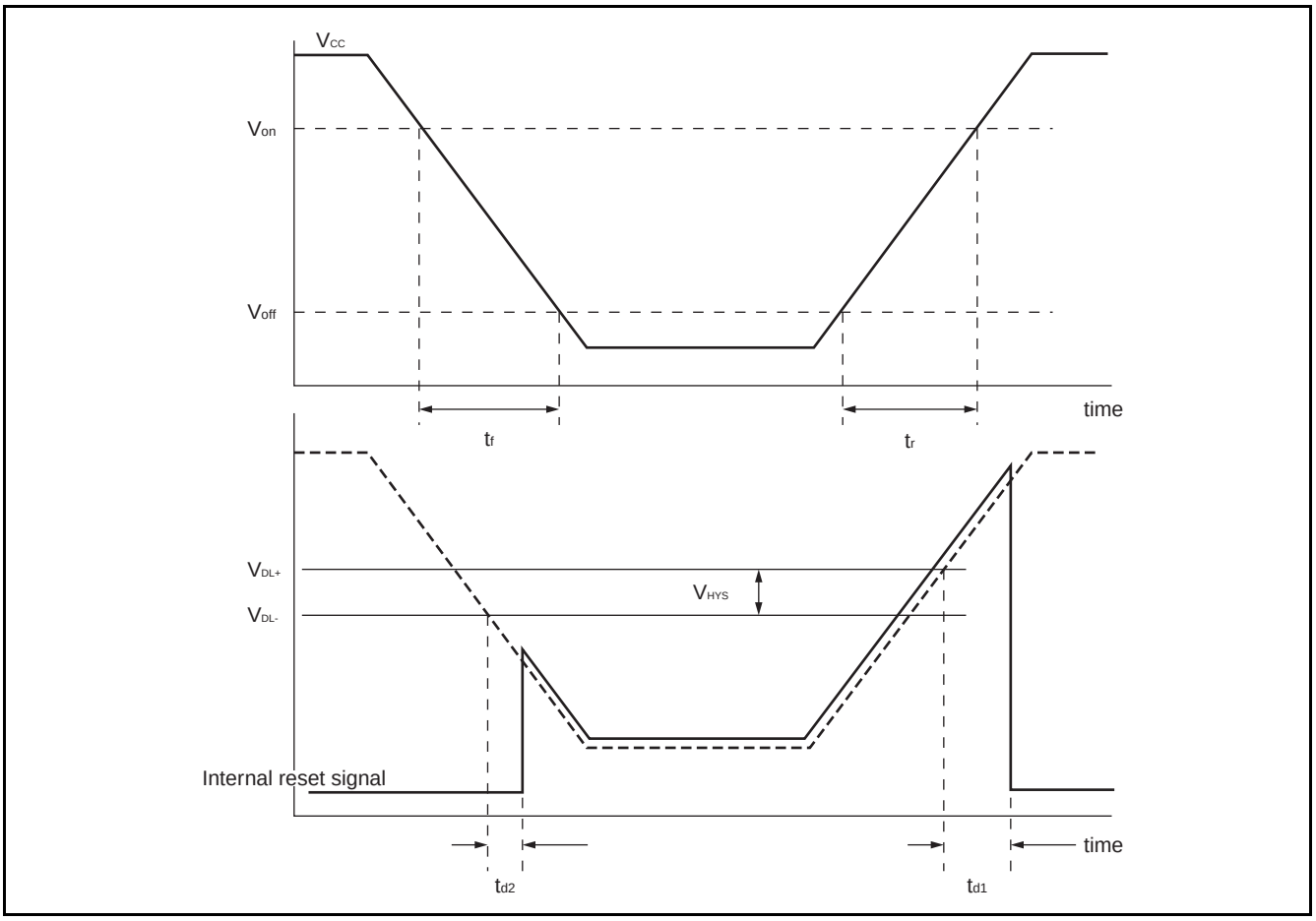
*3: See “(2) Source Clock/Machine Clock” for t_{MCLK}.



(7) Low-voltage Detection

(V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Release voltage	V_{DL+}	2.52	2.7	2.88	V	At power supply rise
Detection voltage	V_{DL-}	2.42	2.6	2.78	V	At power supply fall
Hysteresis width	V_{HYS}	70	100	—	mV	
Power supply start voltage	V_{off}	—	—	2.3	V	
Power supply end voltage	V_{on}	4.9	—	—	V	
Power supply voltage change time (at power supply rise)	t_r	1	—	—	µs	Slope of power supply that the reset release signal generates
		—	3000	—	µs	Slope of power supply that the reset release signal generates within the rating (V_{DL+})
Power supply voltage change time (at power supply fall)	t_f	300	—	—	µs	Slope of power supply that the reset detection signal generates
		—	300	—	µs	Slope of power supply that the reset detection signal generates within the rating (V_{DL-})
Reset release delay time	t_{d1}	—	—	300	µs	
Reset detection delay time	t_{d2}	—	—	20	µs	


VCC
Von
Voff
time
tf
tr
VDL+
VDL-
VHYS
Internal reset signal
time
td2
td1

5. A/D Converter

(1) A/D Converter Electrical Characteristics

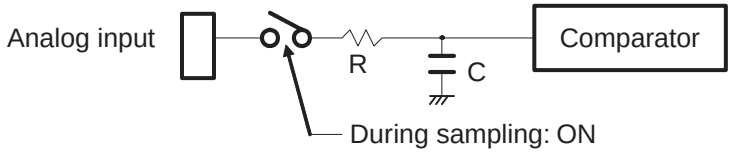
(V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	10	bit	
Total error		-3	—	+3	LSB	
Linearity error		-2.5	—	+2.5	LSB	
Differential linear error		-1.9	—	+1.9	LSB	
Zero transition voltage	V_{OT}	V_{SS}–1.5 LSB	V_{SS}+0.5 LSB	V_{SS}+2.5 LSB	V	
Full-scale transition voltage	V_{FST}	V_{CC}–4.5 LSB	V_{CC}–2 LSB	V_{CC}+0.5 LSB	V	
Compare time	—	0.9	—	16500	µs	4.5 V ≤ V_{CC} ≤ 5.5 V
		1.8	—	16500	µs	4.0 V ≤ V_{CC} < 4.5 V
Sampling time	—	0.6	—	∞	µs	4.5 V ≤ V_{CC} ≤ 5.5 V, with external impedance < 5.4 kΩ
		1.2	—	∞	µs	4.0 V ≤ V_{CC} ≤ 4.5 V, with external impedance < 2.4 kΩ
Analog input current	I_{AIN}	-0.3	—	+0.3	µA	
Analog input voltage	V_{AIN}	V_{SS}	—	V_{CC}	V	

(2) Notes on Using the A/D Converter

- **External impedance of analog input and its sampling time**
  - The A/D converter has a sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the capacitor of the internal sample and hold circuit is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, considering the relationship between the external impedance and minimum sampling time, either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. In addition, if sufficient sampling time cannot be secured, connect a capacitor of about 0.1 µF to the analog input pin.

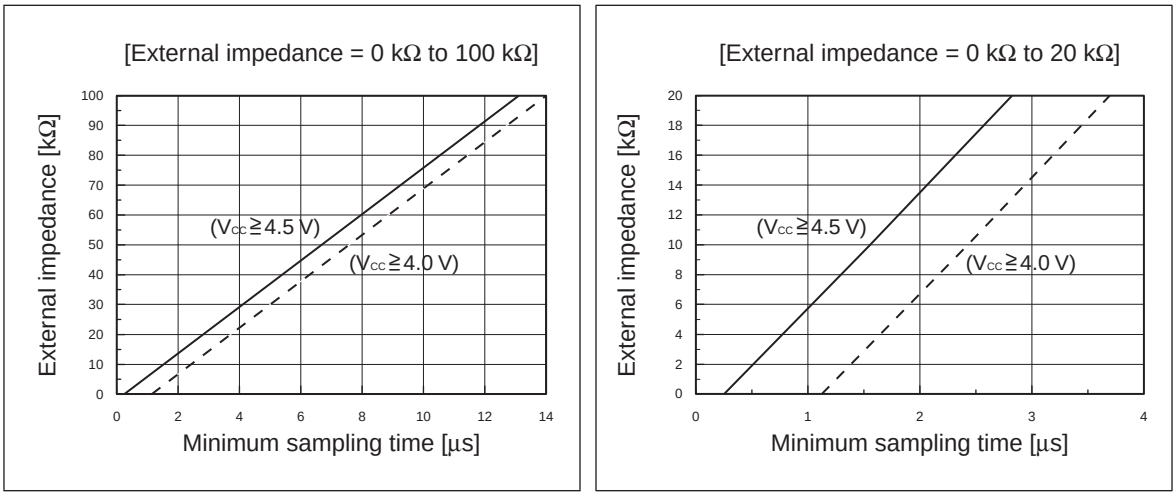
- Analog input equivalent circuit



$4.5\ V \leqq V_{CC} \leqq 5.5\ V$: $R \approx 1.95\ k\Omega$ (max), $C \approx 17\ pF$ (max)
$4.0\ V \leqq V_{CC} < 4.5\ V$: $R \approx 8.98\ k\Omega$ (max), $C \approx 17\ pF$ (max)

Note: The values are reference values.

- Relationship between external impedance and minimum sampling time

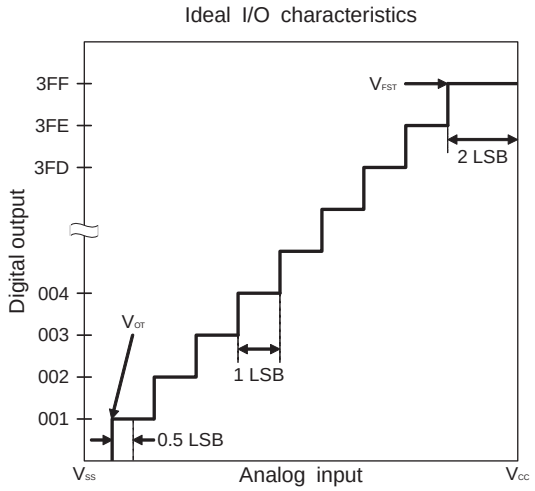


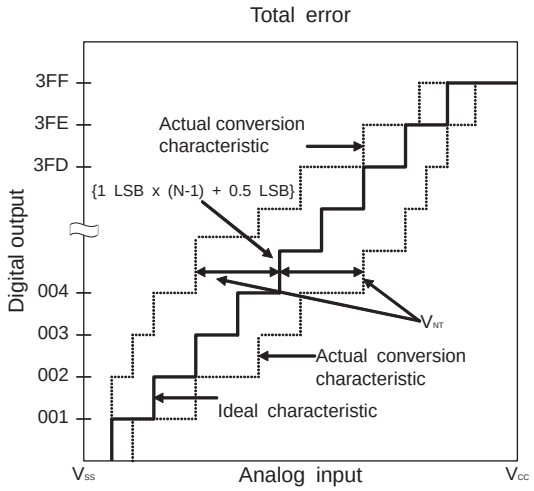
- **A/D conversion error**

As $|V_{CC}–V_{SS}|$ decreases, the A/D conversion error increases proportionately.

(3) Definitions of A/D Converter Terms

- Resolution
  It indicates the level of analog variation that can be distinguished by the A/D converter.
  When the number of bits is 10, analog voltage can be divided into 2^{10} = 1024.
- Linearity error (unit: LSB)
  It indicates how much an actual conversion value deviates from the straight line connecting the zero transition point (“00 0000 0000” ← → “00 0000 0001”) of a device to the full-scale transition point (“11 1111 1111“ ← → “11 1111 1110”) of the same device.
- Differential linear error (unit : LSB)
  It indicates how much the input voltage required to change the output code by 1 LSB deviates from an ideal value.
- Total error (unit: LSB)
  It indicates the difference between an actual value and a theoretical value. The error can be caused by a zero transition error, a full-scale transition errors, a linearity error, a quantum error, or noise.





$$1\ \text{LSB} = \frac{V_{CC} - V_{SS}}{1024}\ (\text{V})$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

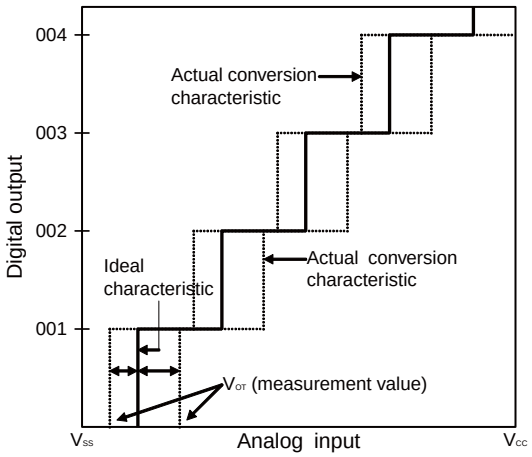
N : A/D converter digital output value

V_{NT}: Voltage at which the digital output transits from (N - 1) to N

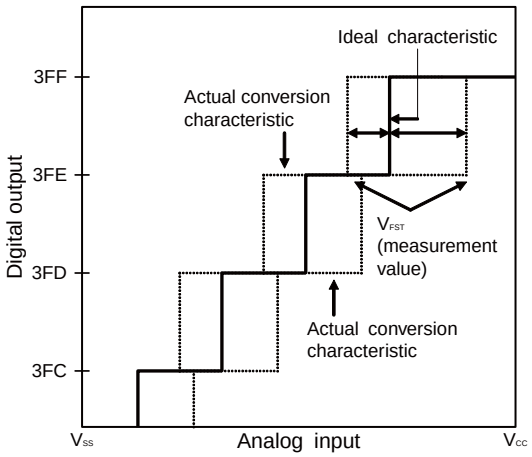
(Continued)

(Continued)

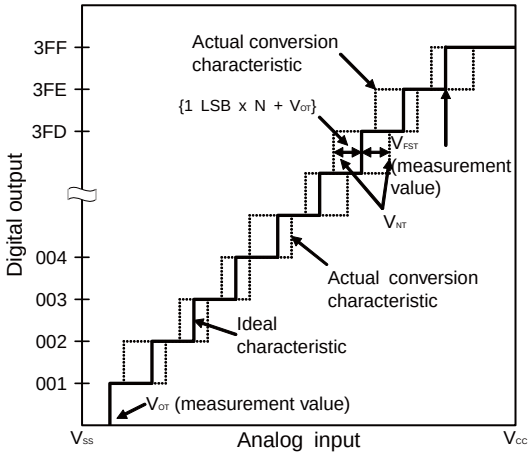
Zero transition error



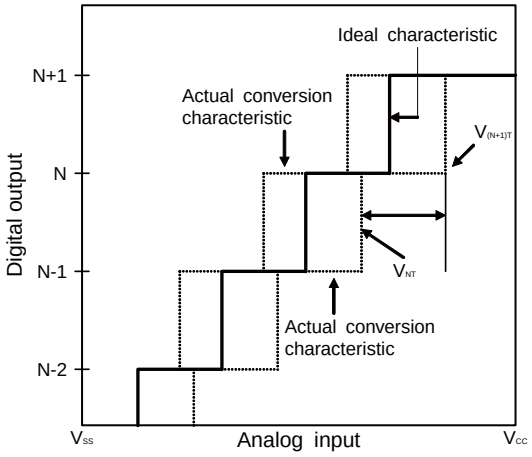
Full-scale transition error



Linearity error



Differential linearity error



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times N + V_{OT}\}}{1\ \text{LSB}}$$

$$\text{Differential linear error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1$$

N : A/D converter digital output value

V_{NT}: Voltage at which the digital output transits from (N - 1) to N

V_{OT} (ideal value) = V_{SS} + 0.5 LSB [V]

V_{FST} (ideal value) = V_{CC} - 2 LSB [V]

6. Flash Memory Program/Erase Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Chip erase time	—	1*1	15*2	s	00_H programming time prior to erasure is excluded.
Byte programming time	—	32	3600	µs	System-level overhead is excluded.
Erase/program voltage	9.5	10	10.5	V	The erase/program voltage must be applied to the $\overline{RST}$ pin in erase/program.
Erase/program cycle	—	100000	—	cycle	
Power supply voltage at erase/ program	4.5	—	5.5	V	
Flash memory data retention time	20*3	—	—	year	Average T_A = +85°C

*1: T_A = +25°C, V_{CC} = 5.0 V, 100000 cycles

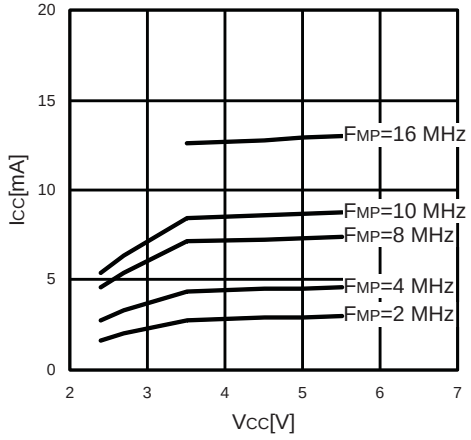
*2: T_A = +85°C, V_{CC} = 4.5 V, 100000 cycles

*3: This value is converted from the result of a technology reliability assessment. (The value is converted from the result of a high temperature accelerated test by using the Arrhenius equation with the average temperature being +85°C) .

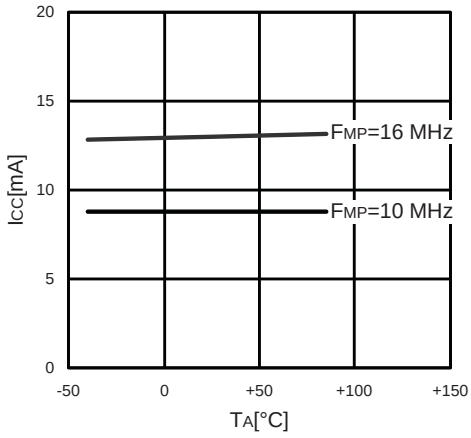
■ SAMPLE ELECTRICAL CHARACTERISTICS

• Power supply current•temperature

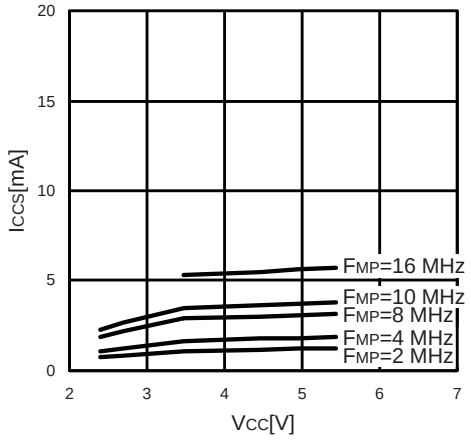
I_{CC} - V_{CC}
T_A=+25°C, F_{MP}=2, 4, 8, 10, 16 MHz (divided by 2)
Main clock mode with the external clock operating



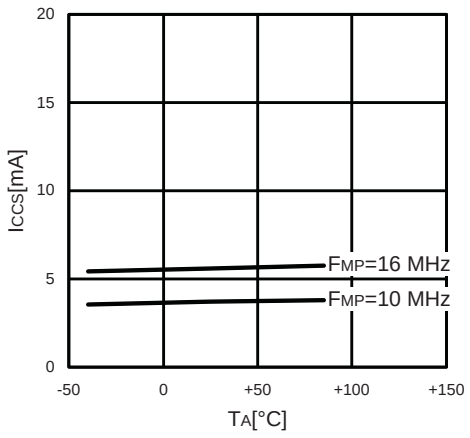
I_{CC} - T_A
V_{CC}=5.5 V, F_{MP}=10, 16 MHz (divided by 2)
Main clock mode with the external clock operating



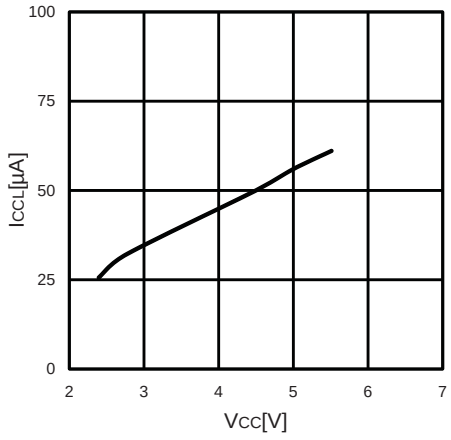
I_{CCS} - V_{CC}
T_A=+25°C, F_{MP}=2, 4, 8, 10, 16 MHz (divided by 2)
Main sleep mode with the external clock operating



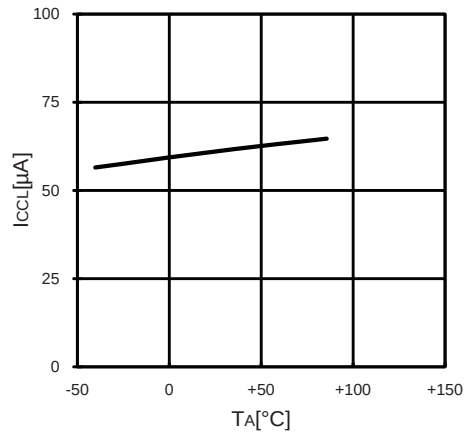
I_{CCS} - T_A
V_{CC}=5.5 V, F_{MP}=10, 16 MHz (divided by 2)
Main sleep mode with the external clock operating



I_{CCL} - V_{CC}
T_A=+25°C, F_{MPL}=16 kHz (divided by 2)
Subclock mode with the external clock operating



I_{CCL} - T_A
V_{CC}=5.5 V, F_{MPL}=16 kHz (divided by 2)
Subclock mode with the external clock operating



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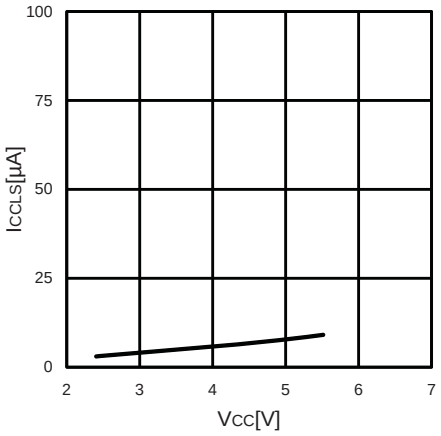
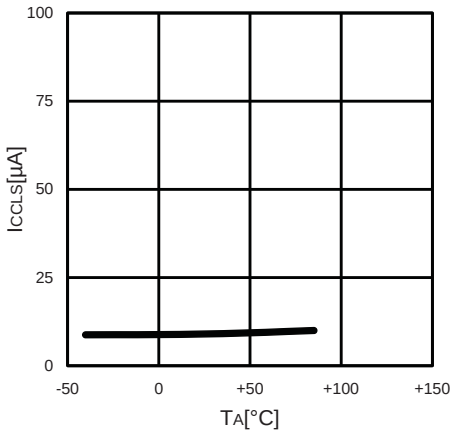
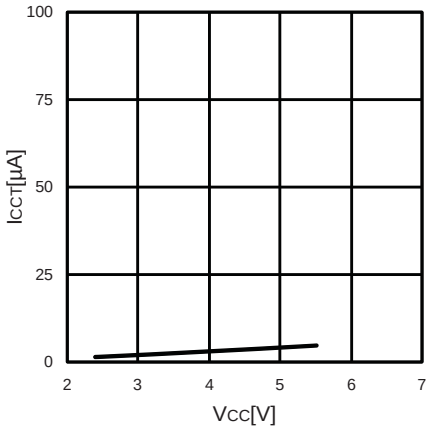
ICCLS - VCC
TA=+25°C, FMPL=16 kHz (divided by 2)
Subsleep mode with the external clock operating



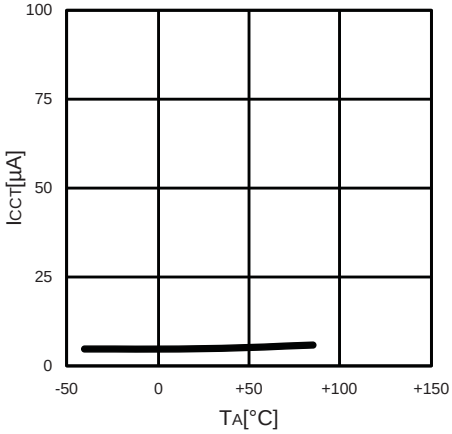
ICCLS - TA
VCC=5.5 V, FMPL=16 kHz (divided by 2)
Subsleep mode with the external clock operating



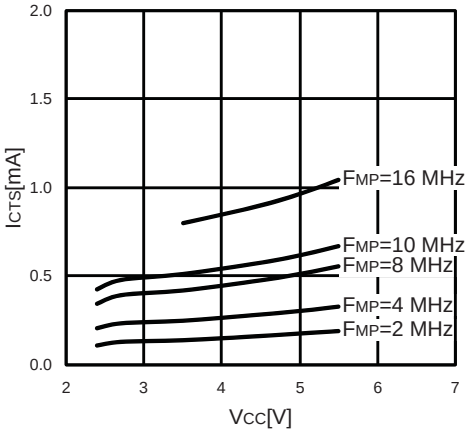
ICCT - VCC
TA=+25°C, FMPL=16 kHz (divided by 2)
Clock mode with the external clock operating



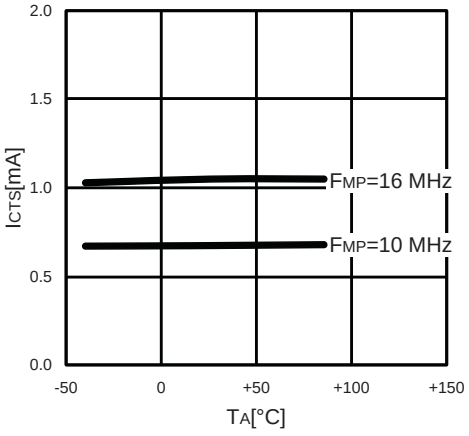
ICCT - TA
V=5.5 V, FMPL=16 kHz (divided by 2)
Clock mode with the external clock operating



ICTS - VCC
TA=+25°C, FMP=2, 4, 8, 10, 16 MHz (divided by 2)
Timebase timer mode with the external clock operating



ICTS - TA
V=5.5 V, FMP=10, 16 MHz (divided by 2)
Timebase timer mode with the external clock operating



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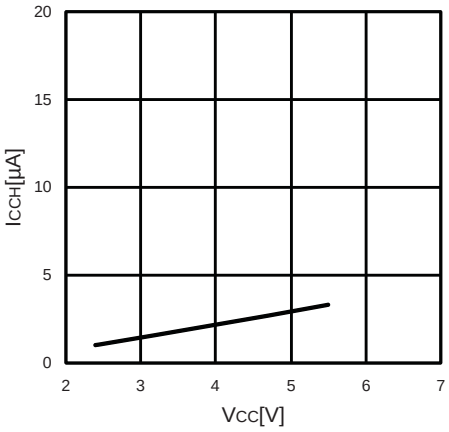
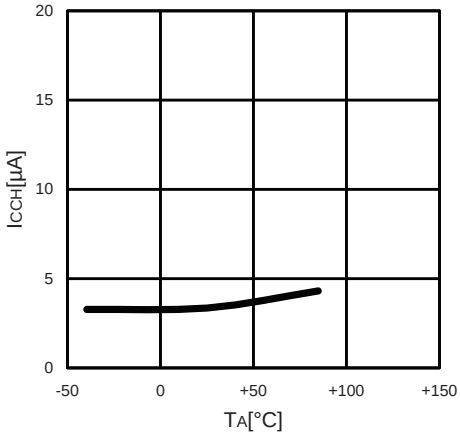
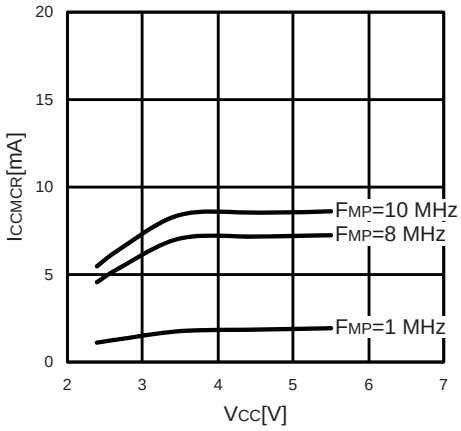
I_{CCH} - V_{CC}
T_A=+25°C, F_{MPL}=(stop)
Substop mode wtih the external clock stopping



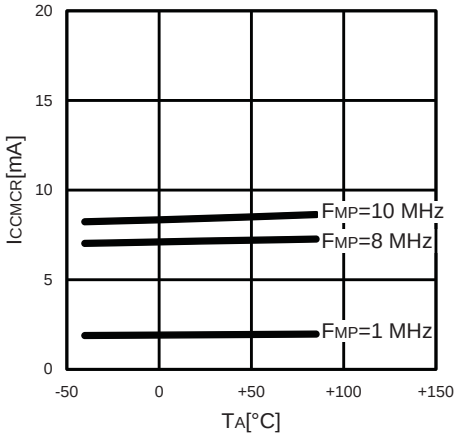
I_{CCH} - T_A
V=5.5 V, F_{MPL}=(stop)
Substop mode with the external clock stopping



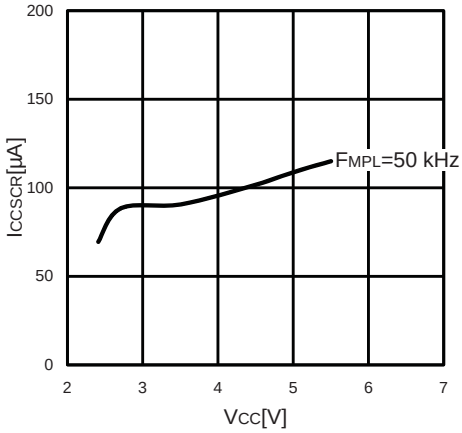
I_{CCMCR} - V_{CC}
T_A=+25°C, F_{MP}=1, 8, 10 MHz (no division)
Main clock mode with the internal main CR clock operating



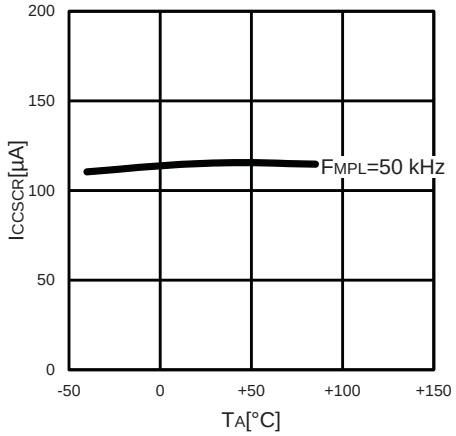
I_{CCMCR} - T_A
V=5.5 V, F_{MPL}=1, 8, 10 MHz (no division)
Main clock mode with the internal main CR clock operating



I_{CCSCR} - V_{CC}
T_A=+25°C, F_{MPL}=50 kHz (divided by 2)
Subclock mode with the internal sub-CR clock operating

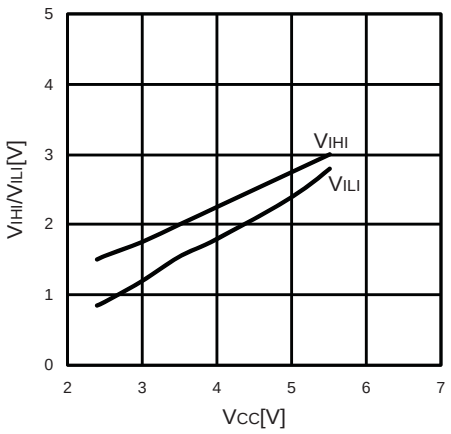


I_{CCSCR} - T_A
V_{CC}=5.5 V, F_{MPL}=50 kHz (divided by 2)
Subclock mode with the internal sub-CR clock operating

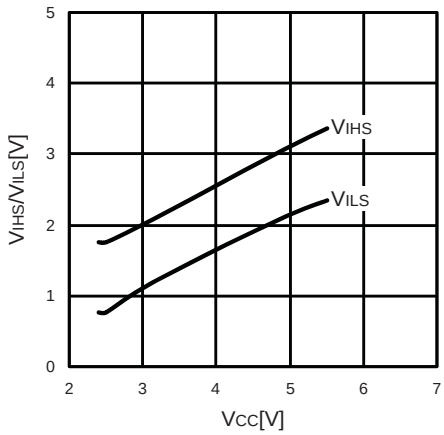


• Input voltage

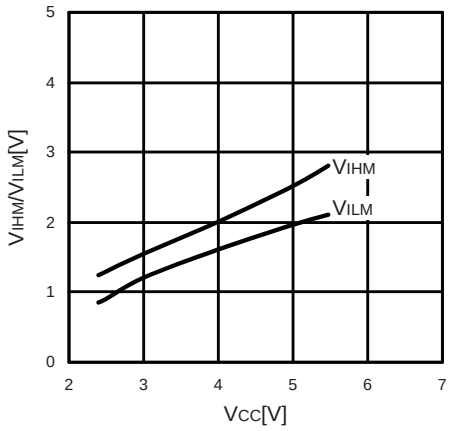
VIHI - VCC and VILI - VCC
TA=+25°C



VIHS - VCC and VILS - VCC
TA=+25°C

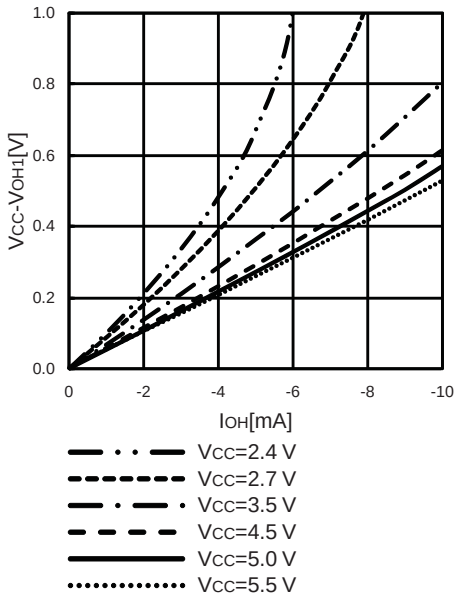


VIHM - VCC and VILM - VCC
TA=+25°C

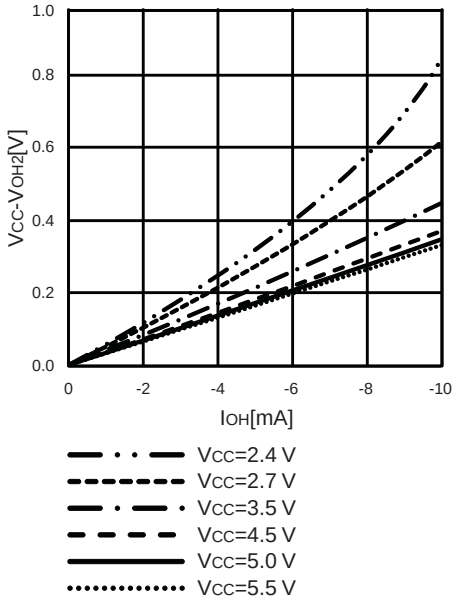


• Output voltage

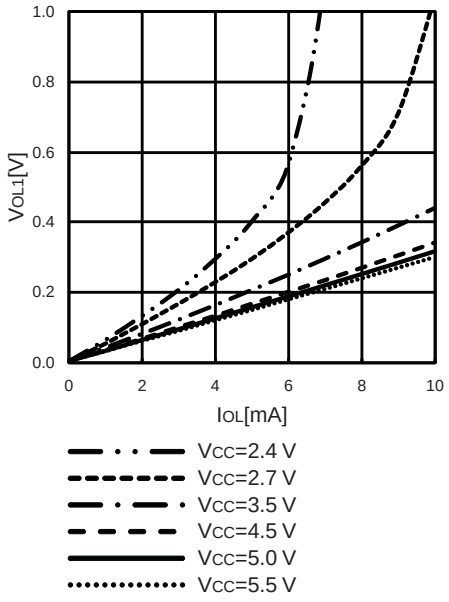
(VCC-VOH1) - IOH
TA=+25°C



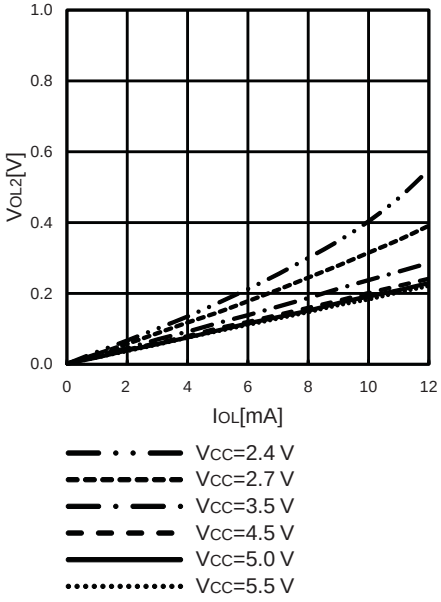
(VCC-VOH2) - IOH
TA=+25°C



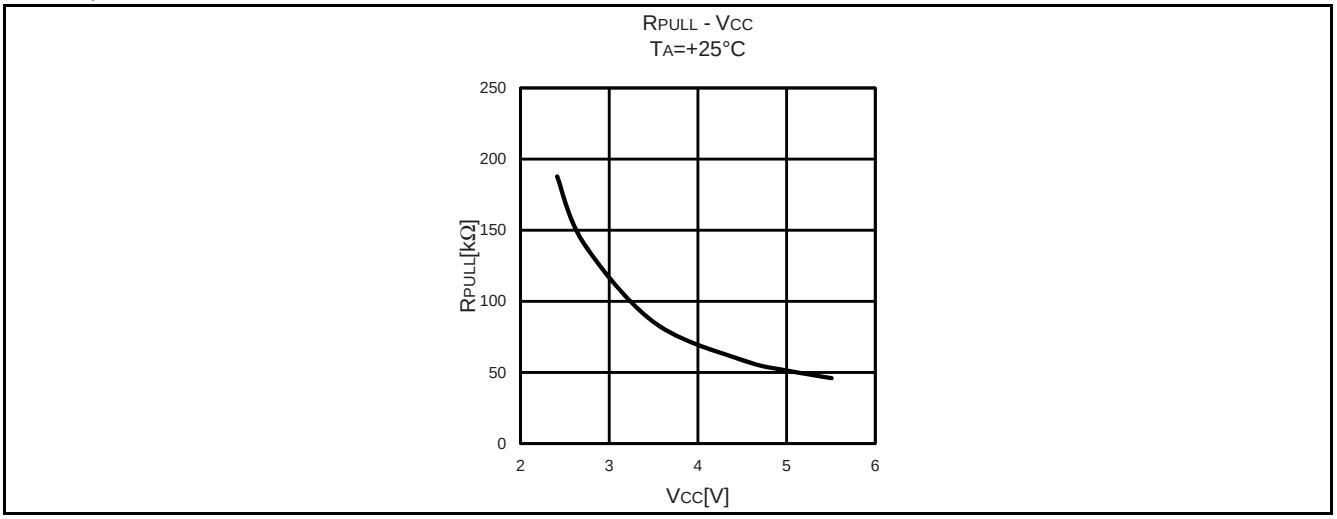
VOL1 - IOL
TA=+25°C



VOL2 - IOL
TA=+25°C



• Pull-up



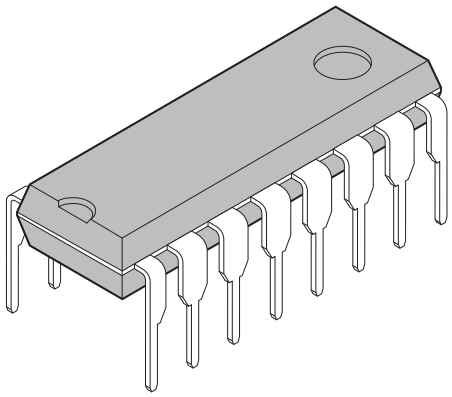
■ MASK OPTIONS

No.	Part Number	MB95F222H MB95F223H	MB95F222K MB95F223K
	Selectable/Fixed	Fixed	Fixed
1	Low-voltage detection reset • With low-voltage detection reset • Without low-voltage detection reset	Without low-voltage detection reset	With low-voltage detection reset
2	Reset • With dedicated reset input • Without dedicated reset input	With dedicated reset input	Without dedicated reset input

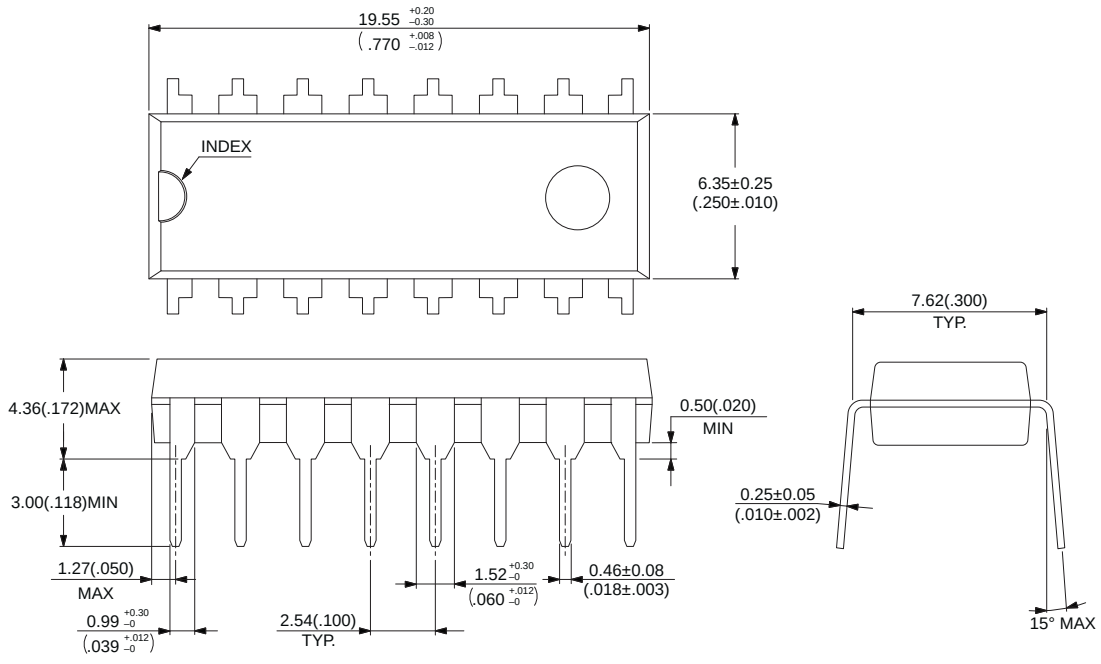
■ ORDERING INFORMATION

Part Number	Package
MB95F222HPH-G-SNE2 MB95F222KPH-G-SNE2 MB95F223HPH-G-SNE2 MB95F223KPH-G-SNE2	16-pin plastic DIP (DIP-16P-M06)
MB95F222HPF-G-SNE1 MB95F222KPF-G-SNE1 MB95F223HPF-G-SNE1 MB95F223KPF-G-SNE1	16-pin plastic SOP (FPT-16P-M06)

■ PACKAGE DIMENSIONS

16-pin plastic DIP		
 (DIP-16P-M06)	Lead pitch	2.54 mm
	Sealing method	Plastic mold

16-pin plastic DIP
(DIP-16P-M06)



Dimensions in mm (inches).
Note: The values in parentheses are reference values

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

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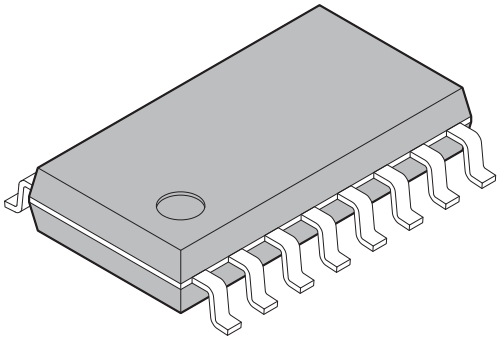
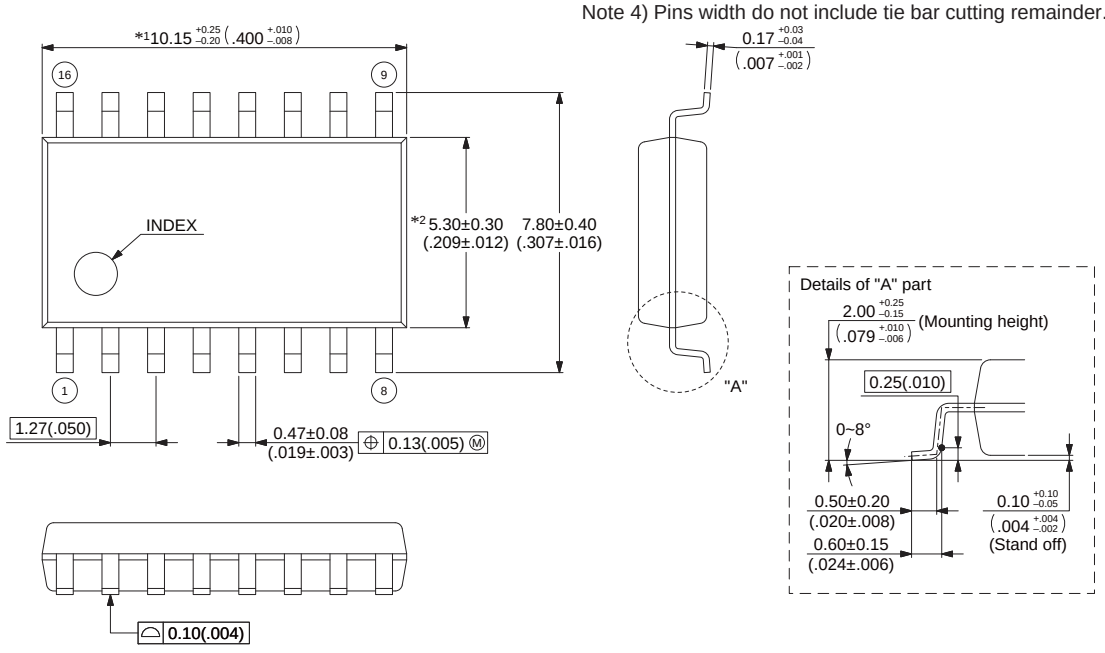
(Continued)

16-pin plastic SOP		
	Lead pitch	1.27 mm
	Package width × package length	5.3 × 10.15 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	2.25 mm MAX
	Weight	0.20 g
(FPT-16P-M06)	Code (Reference)	P-SOP16-5.3×10.15-1.27

16-pin plastic SOP
(FPT-16P-M06)

Note 1) *1 : These dimensions include resin protrusion.
Note 2) *2 : These dimensions do not include resin protrusion.
Note 3) Pins width and pins thickness include plating thickness.
Note 4) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
27	■ ELECTRICAL CHARACTERISTICS 4. AC Characteristics (1) Clock Timing	Changed the Remarks.
49 to 54	■ SAMPLE ELECTRICAL CHARACTERISTICS	Added the “SAMPLE ELECTRICAL CHARACTERISTICS”.

The vertical lines marked in the left side of the page show the changes.

MEMO

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