

# 8-bit Proprietary Microcontrollers

CMOS

## F<sup>2</sup>MC-8FX MB95120H Series

### MB95F128H/F128T/FV100B-103

#### ■ DESCRIPTION

The MB95120H series is general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers contain a variety of peripheral functions.

Note : F<sup>2</sup>MC is the abbreviation of FUJITSU Flexible Microcontroller.

#### ■ FEATURE

- F<sup>2</sup>MC-8FX CPU core
  - Instruction set optimized for controllers
    - Multiplication and division instructions
    - 16-bit arithmetic operations
    - Bit test branch instruction
    - Bit manipulation instructions etc.
- Clock
  - Main clock
  - Main PLL clock
  - Sub clock
  - Sub PLL clock

(Continued)

Be sure to refer to the "Check Sheet" for the latest cautions on development.

"Check Sheet" is seen at the following support page

URL : <http://www.fujitsu.com/global/services/microelectronics/product/micom/support/index.html>

"Check Sheet" lists the minimal requirement items to be checked to prevent problems beforehand in system development.

# MB95120H Series

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- Timer
  - 8/16-bit compound timer × 2 channels
  - 16-bit reload timer
  - 8/16-bit PPG × 2 channels
  - 16-bit PPG × 2 channels
  - Timebase timer
  - Watch prescaler
- LIN-UART
  - Full duplex double buffer
  - Clock asynchronous or clock synchronous serial data transfer capable
- UART/SIO
  - Full duplex double buffer
  - Clock asynchronous or clock synchronous serial data transfer capable
- I<sup>2</sup>C\*
  - Built-in wake-up function
- External interrupt
  - Interrupt by edge detection (rising, falling, or both edges can be selected)
  - Can be used to recover from low-power consumption (standby) modes.
- 8/10-bit A/D converter
  - 8-bit or 10-bit resolution can be selected
- LCD controller (LCDC)
  - 40 SEG × 4 COM (Max 160 pixels)
  - With blinking function
- Low-power consumption (standby) mode
  - Stop mode
  - Sleep mode
  - Watch mode
  - Timebase timer mode
- I/O port
  - The number of maximum ports : Max 87
  - Port configuration
    - General-purpose I/O ports (N-ch open drain) : 2 ports
    - General-purpose I/O ports (CMOS) : 85 ports

\* : Purchase of Fujitsu I<sup>2</sup>C components conveys a license under the Philips I<sup>2</sup>C Patent Rights to use, these components in an I<sup>2</sup>C system provided that the system conforms to the I<sup>2</sup>C Standard Specification as defined by Philips.

# MB95120H Series

## ■ PRODUCT LINEUP

Part number*1		MB95F128H	MB95F128T
Parameter			
Type		Flash memory product	
ROM capacity		60K bytes	
RAM capacity		2K bytes	
Reset output		Yes	
Option*2	Clock system	Dual clock	
	Low voltage detection reset	No	Yes
CPU functions		Number of basic instructions : 136 Instruction bit length : 8 bits Instruction length : 1 to 3 bytes Data bit length : 1, 8, and 16 bits Minimum instruction execution time : 0.1 $\mu$ s (at machine clock frequency 10 MHz) Interrupt processing time : 0.9 $\mu$ s (at machine clock frequency 10 MHz)	
Peripheral functions	Ports (Max 87 ports)	General-purpose I/O port (N-ch open drain) : 2 ports General-purpose I/O port (CMOS) : 85 ports	
	Timebase timer	Interrupt cycle : 0.5 ms, 2.1 ms, 8.2 ms, 32.8 ms (at main oscillation clock 4 MHz)	
	Watchdog timer	Reset generated cycle At main oscillation clock 10 MHz : Min 105 ms At sub oscillation clock 32.768 kHz : Min 250 ms	
	Wild register	Capable of replacing 3 bytes of ROM data	
	I <sup>2</sup> C	Master/slave sending and receiving Bus error function and arbitration function Detecting transmitting direction function Start condition repeated generation and detection functions Built-in wake-up function	
	UART/SIO	Data transfer capable in UART/SIO Full duplex double buffer Variable data length (5/6/7/8-bit), built-in baud rate generator Transfer rate : 2400 bps to 1250000 bps (at machine clock 10 MHz) NRZ type transfer format, error detected function LSB-first or MSB-first can be selected. Clock synchronous (SIO) or clock asynchronous (UART) serial data transfer capable	
	LIN-UART	Dedicated reload timer allowing a wide range of communication speeds to be set. Full duplex double buffer. Capable of serial data transfer synchronous or asynchronous to clock signal. LIN functions available as the LIN master or LIN slave.	
	8/10-bit A/D converter (12 channels)	8-bit or 10-bit resolution can be selected.	

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# MB95120H Series

(Continued)

Part number*1		MB95F128H	MB95F128T
Parameter			
Peripheral functions	LCD controller (LCDC)	COM output : 4 (Max) SEG output : 40 (Max) LCD drive power supply (bias) pin : 4 (Max) 40 SEG × 4 COM : 160 pixels can be displayed. Duty LCD mode With blinking function Built-in division resistance for LCD drive	
	16-bit reload timer	Two clock modes and two counter operating modes can be selected. Square waveform output Count clock : 7 internal clocks and external clock can be selected. Counter operating mode : reload mode or one-shot mode can be selected.	
	8/16-bit compound timer (2 channels)	Each channel of the timer can be used as "8-bit timer × 2 channels" or "16-bit timer × 1 channel". Built-in timer function, PWC function, PWM function, capture function and square waveform output Count clock : 7 internal clocks and external clock can be selected.	
	16-bit PPG (2 channels)	PWM mode or one-shot mode can be selected. Counter operating clock : Eight selectable clock sources Support for external trigger start	
	8/16-bit PPG (2 channels)	Each channel of the PPG can be used as "8-bit PPG × 2 channels" or "16-bit PPG × 1 channel". Counter operating clock : Eight selectable clock sources	
	Watch counter	Count clock : Four selectable clock sources (125 ms, 250 ms, 500 ms, or 1 s) Counter value can be set from 0 to 63. (Capable of counting for 1 minute when selecting clock source 1 second and setting counter value to 60)	
	Watch prescaler	4 selectable interval times (125 ms, 250 ms, 500 ms, or 1 s)	
	External interrupt (12 channels)	Interrupt by edge detection (rising, falling, or both edges can be selected.) Can be used to recover from standby modes.	
Standby mode	Sleep, stop, watch, and timebase timer		

\*1 : MASK ROM products are currently under consideration.

\*2 : For details of option, refer to "■ MASK OPTION".

Note : Part number of evaluation device in MB95120 series is MB95FV100B-103. When using it, the MCU board (MB2146-303) is required.

## ■ OSCILLATION STABILIZATION WAIT TIME

The initial value of the main clock oscillation stabilization wait time is fixed to the maximum value. The maximum value is shown as follows.

Oscillation stabilization wait time	Remarks
$(2^{14}-2) / F_{CH}$	Approx. 4.10 ms (at main oscillation clock 4 MHz)

## ■ PACKAGES AND CORRESPONDING PRODUCTS

Package \ Part number	MB95F128H MB95F128T	MB95FV100B-103
FPT-100P-M05	○	×
FPT-100P-M06	○	×
BGA-224P-M08	×	○

- : Available  
 × : Unavailable

# MB95120H Series

## ■ DIFFERENCES AMONG PRODUCTS AND NOTES ON SELECTING PRODUCTS

### • Notes on Using Evaluation Products

The Evaluation product has not only the functions of the MB95120H series but also those of other products to support software development for multiple series and models of the F<sup>2</sup>MC-8FX family. The I/O addresses for peripheral resources not used by the MB95120H series are therefore access-barred. Read/write access to these access-barred addresses may cause peripheral resources supposed to be unused to operate, resulting in unexpected malfunctions of hardware or software.

Particularly, do not use word access to odd numbered byte address in the prohibited areas (If these access are used, the address may be read or written unexpectedly).

Note that the values read from barred addresses are different between the Evaluation product and the Flash memory product. Therefore, the data must not be used for software processing.

The Evaluation product do not support the functions of some bits in single-byte registers. Read/write access to these bits does not cause hardware malfunctions. The Evaluation, and Flash memory product are designed to behave completely the same way in terms of hardware and software.

### • Difference of Memory Spaces

If the amount of memory on the Evaluation product is different from that of the Flash memory product, carefully check the difference in the amount of memory from the model to be actually used when developing software.

For details of memory space, refer to “■ CPU CORE”.

### • Current Consumption

- For details of current consumption, refer to “■ ELECTRICAL CHARACTERISTICS”.

### • Package

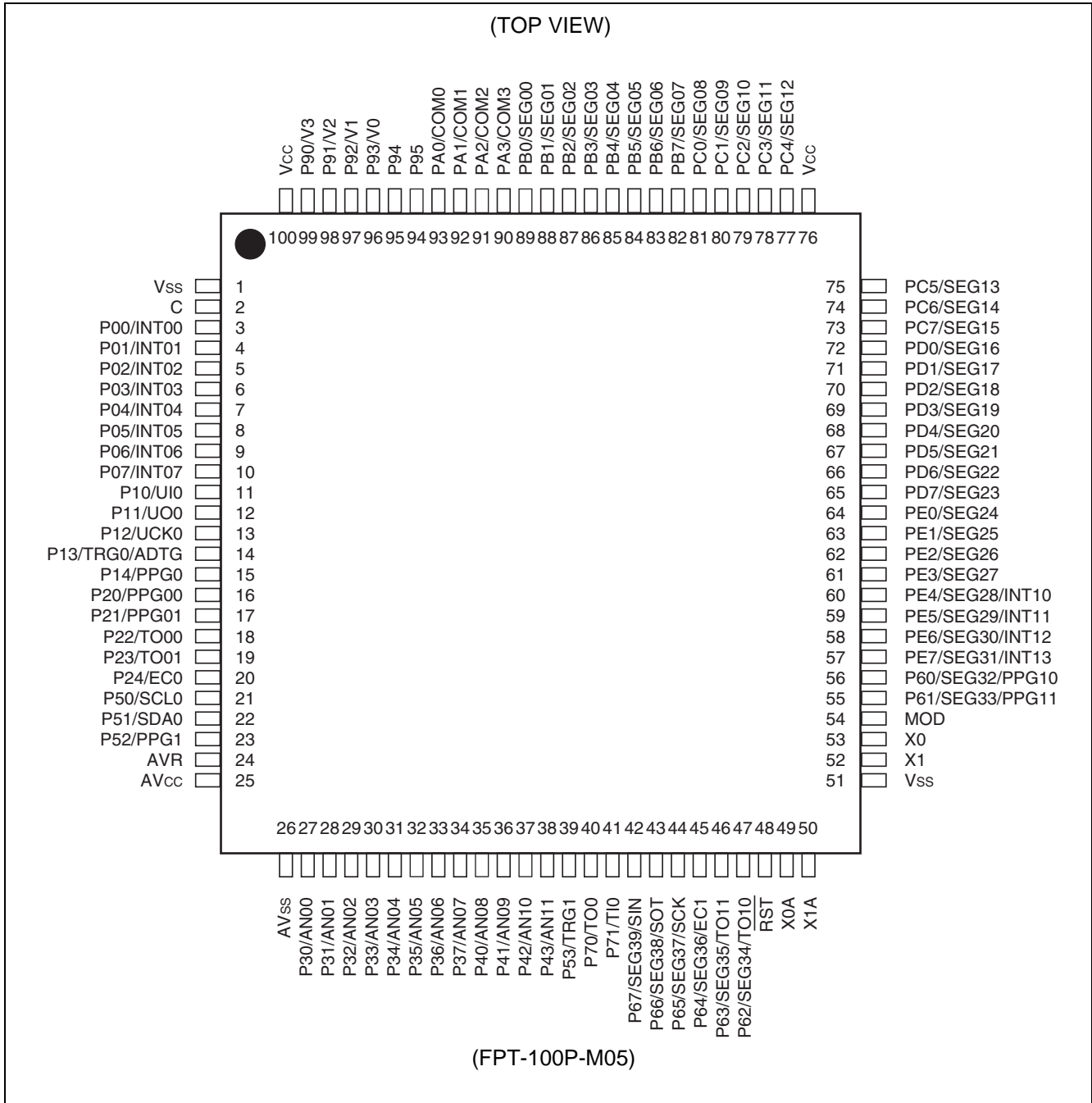
For details of information on each package, refer to “■ PACKAGES AND CORRESPONDING PRODUCTS” and “■ PACKAGE DIMENSIONS”.

### • Operating voltage

The operating voltage are different between the Evaluation and Flash memory products.

For details of operating voltage, refer to “■ ELECTRICAL CHARACTERISTICS”.

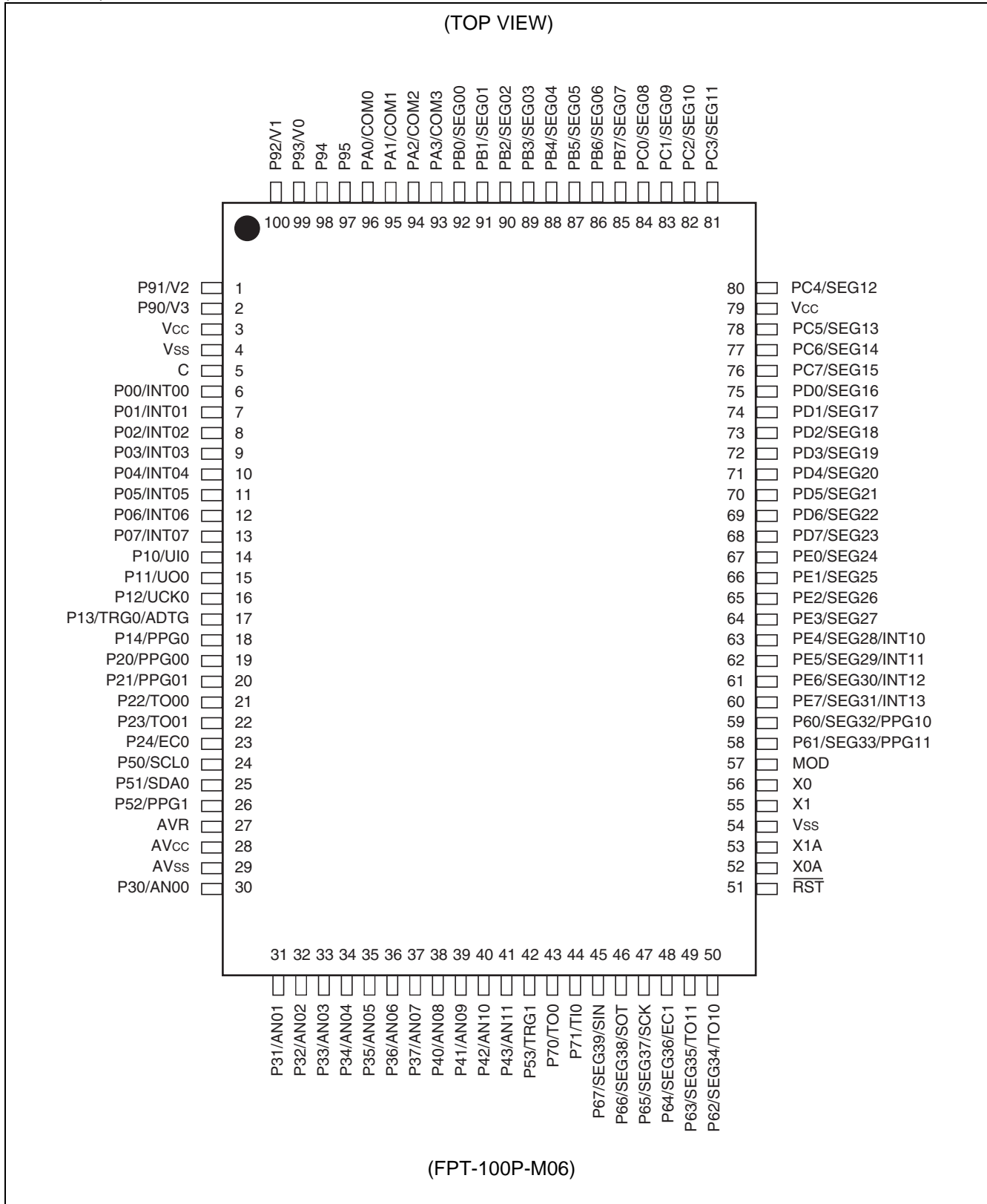
## PIN ASSIGNMENT



(Continued)

# MB95120H Series

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## ■ PIN DESCRIPTION

Pin no.		Pin name	I/O circuit type*3	Function		
LQFP *1	QFP *2					
1	4	V <sub>SS</sub>	—	Power supply pin (GND)		
2	5	C	—	Capacitor connection pin		
3	6	P00/INT00	C	General-purpose I/O port The pins are shared with external interrupt input. Large current port.		
4	7	P01/INT01				
5	8	P02/INT02				
6	9	P03/INT03				
7	10	P04/INT04				
8	11	P05/INT05				
9	12	P06/INT06				
10	13	P07/INT07				
11	14	P10/UI0			G	General-purpose I/O port The pin is shared with UART/SIO ch.0 data input.
12	15	P11/UO0			H	General-purpose I/O port The pin is shared with UART/SIO ch.0 data output.
13	16	P12/UCK0	General-purpose I/O port The pin is shared with UART/SIO ch.0 clock I/O.			
14	17	P13/TRG0/ ADTG	General-purpose I/O port The pin is shared with 16-bit PPG ch.0 trigger input (TRG0) and A/D trigger input (ADTG).			
15	18	P14/PPG0	General-purpose I/O port The pin is shared with 16-bit PPG ch.0 output.			
16	19	P20/PPG00	H	General-purpose I/O port The pins are shared with 8/16-bit compound timer ch.0 output.		
17	20	P21/PPG01				
18	21	P22/TO00				
19	22	P23/TO01				
20	23	P24/EC0	I	General-purpose I/O port The pin is shared with 8/16-bit compound timer ch.0 clock input.		
21	24	P50/SCL0		General-purpose I/O port The pin is shared with I <sup>2</sup> C ch.0 clock I/O.		
22	25	P51/SDA0	H	General-purpose I/O port The pin is shared with I <sup>2</sup> C ch.0 data I/O.		
23	26	P52/PPG1		General-purpose I/O port The pin is shared with 16-bit PPG ch.1 output.		
24	27	AVR	—	A/D converter reference input pin		
25	28	AV <sub>CC</sub>	—	A/D converter power supply pin		

(Continued)

# MB95120H Series

Pin no.		Pin name	I/O circuit type*3	Function
LQFP *1	QFP *2			
26	29	AV <sub>ss</sub>	—	A/D converter power supply pin (GND)
27	30	P30/AN00	J	General-purpose I/O port The pins are shared with A/D converter analog input.
28	31	P31/AN01		
29	32	P32/AN02		
30	33	P33/AN03		
31	34	P34/AN04		
32	35	P35/AN05		
33	36	P36/AN06		
34	37	P37/AN07		
35	38	P40/AN08	J	General-purpose I/O port The pins are shared with A/D converter analog input.
36	39	P41/AN09		
37	40	P42/AN10		
38	41	P43/AN11		
39	42	P53/TRG1	H	General-purpose I/O port The pin is shared with 16 - bit PPG ch.1 trigger input.
40	43	P70/TO0	H	General-purpose I/O port The pin is shared with 16 - bit reload timer ch.0 output.
41	44	P71/TI0		General-purpose I/O port The pin is shared with 16 - bit reload timer ch.0 input.
42	45	P67/SEG39/ SIN	N	General-purpose I/O port The pin is shared with LIN-UART data input (SIN) and LCDC SEG output (SEG39) .
43	46	P66/SEG38/ SOT	M	General-purpose I/O port The pin is shared with LIN-UART data output (SOT) and LCDC SEG output (SEG38) .
44	47	P65/SEG37/ SCK		General-purpose I/O port The pins are shared with LIN-UART clock I/O (SCK) and LCDC SEG output (SEG37) .
45	48	P64/SEG36/ EC1		General-purpose I/O port The pins are shared with 8/16-bit compound timer ch.1 clock input (EC1) and LCDC SEG output (SEG36) .
46	49	P63/SEG35/ TO11		General-purpose I/O port The pins are shared with 8/16-bit compound timer ch.1 output (TO10, TO11) and LCDC SEG output (SEG34, SEG35) .
47	50	P62/SEG34/ TO10		
48	51	$\overline{RST}$		B'
49	52	X0A	A	Sub clock oscillation pin (32 kHz)
50	53	X1A		
51	54	V <sub>ss</sub>	—	Power supply pin (GND)

(Continued)

# MB95120H Series

Pin no.		Pin name	I/O circuit type*3	Function
LQFP *1	QFP *2			
52	55	X1	A	Main clock oscillation pin
53	56	X0		
54	57	MOD	B	An operating mode designation pin
55	58	P61/SEG33/ PPG11	M	General-purpose I/O port The pins are shared with 8/16-bit PPG ch.1 output (PPG10, PPG11) and LCDC SEG output (SEG32, SEG33) .
56	59	P60/SEG32/ PPG10		
57	60	PE7/SEG31/ INIT13	Q	General-purpose I/O port The pins are shared with external interrupt input (INIT10 to INIT13) and LCDC SEG output (SEG28 to SEG31) .
58	61	PE6/SEG30/ INIT12		
59	62	PE5/SEG29/ INIT11		
60	63	PE4/SEG28/ INIT10		
61	64	PE3/SEG27	M	General-purpose I/O port The pins are shared with LCDC SEG output.
62	65	PE2/SEG26		
63	66	PE1/SEG25		
64	67	PE0/SEG24		
65	68	PD7/SEG23	M	General-purpose I/O port The pins are shared with LCDC SEG output.
66	69	PD6/SEG22		
67	70	PD5/SEG21		
68	71	PD4/SEG20		
69	72	PD3/SEG19		
70	73	PD2/SEG18		
71	74	PD1/SEG17		
72	75	PD0/SEG16		
73	76	PC7/SEG15	M	General-purpose I/O port The pins are shared with LCDC SEG output.
74	77	PC6/SEG14		
75	78	PC5/SEG13		
76	79	V <sub>cc</sub>	—	Power supply pin

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# MB95120H Series

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Pin no.		Pin name	I/O circuit type*3	Function
LQFP *1	QFP *2			
77	80	PC4/SEG12	M	General-purpose I/O port The pins are shared with LCDC SEG output.
78	81	PC3/SEG11		
79	82	PC2/SEG10		
80	83	PC1/SEG09		
81	84	PC0/SEG08		
82	85	PB7/SEG07	M	General-purpose I/O port The pins are shared with LCDC SEG output.
83	86	PB6/SEG06		
84	87	PB5/SEG05		
85	88	PB4/SEG04		
86	89	PB3/SEG03		
87	90	PB2/SEG02		
88	91	PB1/SEG01		
89	92	PB0/SEG00	M	General-purpose I/O port The pins are shared with LCDC COM output.
90	93	PA3/COM3		
91	94	PA2/COM2		
92	95	PA1/COM1		
93	96	PA0/COM0	M	General-purpose I/O port
94	97	P95		
95	98	P94	R	General-purpose I/O port The pins are shared with power supply pins for LCDC drive.
96	99	P93/V0		
97	100	P92/V1		
98	1	P91/V2		
99	2	P90/V3		
100	3	V <sub>CC</sub>	—	Power supply pin

\*1 : FPT-100P-M05

\*2 : FPT-100P-M06

\*3 : For the I/O circuit type, refer to "■ I/O CIRCUIT TYPE".

## ■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		<ul style="list-style-type: none"> <li>• Oscillation circuit</li> <li>• High-speed side Feedback resistance : approx. 1 MΩ</li> <li>• Low-speed side Feedback resistance : approx. 10 MΩ</li> </ul>
B		<ul style="list-style-type: none"> <li>• Only for input</li> <li>• Hysteresis input</li> </ul>
B'		<ul style="list-style-type: none"> <li>• Reset output</li> <li>• Hysteresis input</li> </ul>
C		<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• Hysteresis input</li> </ul>
G		<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• CMOS input</li> <li>• Hysteresis input</li> <li>• With pull-up control</li> </ul>
H		<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• Hysteresis input</li> <li>• With pull-up control</li> </ul>

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# MB95120H Series

Type	Circuit	Remarks
I	<p>Standby control</p> <p>Digital output</p> <p>CMOS input</p> <p>Hysteresis input</p>	<ul style="list-style-type: none"> <li>• N-ch open drain output</li> <li>• CMOS input</li> <li>• Hysteresis input</li> </ul>
J	<p>Pull-up control</p> <p>Digital output</p> <p>Digital output</p> <p>Analog input</p> <p>A/D control</p> <p>Standby control</p> <p>Hysteresis input</p>	<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• Hysteresis input</li> <li>• Analog input</li> <li>• With pull-up control</li> </ul>
M	<p>Digital output</p> <p>Digital output</p> <p>LCD output</p> <p>LCD control</p> <p>Standby control</p> <p>Hysteresis input</p>	<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• LCD output</li> <li>• Hysteresis input</li> </ul>
N	<p>Digital output</p> <p>Digital output</p> <p>LCD output</p> <p>LCD control</p> <p>Standby control</p> <p>CMOS input</p> <p>Hysteresis input</p>	<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• LCD output</li> <li>• CMOS input</li> <li>• Hysteresis input</li> </ul>

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Type	Circuit	Remarks
Q	<p>             P-ch — Digital output              N-ch — Digital output              LCD output              LCD control              Standby control              External interrupt control — Hysteresis input         </p>	<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• LCD output</li> <li>• Hysteresis input</li> </ul>
R	<p>             P-ch — Digital output              N-ch — Digital output              LCD built-in division resistance I/O              LCD control              Standby control — Hysteresis input         </p>	<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• LCD power supply</li> <li>• Hysteresis input</li> </ul>

# MB95120H Series

## ■ CAUTION OF USING DEVICES

### • Preventing Latch-up

Care must be taken to ensure that maximum voltage ratings are not exceeded when they are used.

Latch-up may occur on CMOS ICs if voltage higher than  $V_{CC}$  or lower than  $V_{SS}$  is applied to input and output pins other than medium- and high-withstand voltage pins or if higher than the rating voltage is applied between  $V_{CC}$  pin and  $V_{SS}$  pin.

When latch-up occurs, power supply current increases rapidly and might thermally damage elements.

Also, take care to prevent the analog power supply voltage ( $AV_{CC}$ ,  $AVR$ ) and analog input voltage from exceeding the digital power supply voltage ( $V_{CC}$ ) when the analog system power supply is turned on or off.

### • Stable Supply Voltage

Supply voltage should be stabilized.

A sudden change in power-supply voltage may cause a malfunction even within the guaranteed operating range of the  $V_{CC}$  power-supply voltage.

For stabilization, in principle, keep the variation in  $V_{CC}$  ripple (p-p value) in a commercial frequency range (50/60 Hz) not to exceed 10% of the standard  $V_{CC}$  value and suppress the voltage variation so that the transient variation rate does not exceed 0.1 V/ms during a momentary change such as when the power supply is switched.

### • Precautions for Use of External Clock

Even when an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from sub clock mode or stop mode.

## ■ PIN CONNECTION

### • Treatment of Unused Pin

Leaving unused input pins unconnected can cause abnormal operation or latch-up, leaving to permanent damage.

Unused input pins should always be pulled up or down through resistance of at least 2 k $\Omega$ . Any unused input/output pins may be set to output mode and left open, or set to input mode and treated the same as unused input pins. If there is unused output pin, make it open.

### • Treatment of Power Supply Pins on A/D Converter

Connect to be  $AV_{CC} = V_{CC}$  and  $AV_{SS} = AVR = V_{SS}$  even if the A/D converter is not in use.

Noise riding on the  $AV_{CC}$  pin may cause accuracy degradation. So, connect approx. 0.1  $\mu$ F ceramic capacitor as a bypass capacitor between  $AV_{CC}$  and  $AV_{SS}$  pins in the vicinity of this device.

### • Power Supply Pins

In products with multiple  $V_{CC}$  or  $V_{SS}$  pins, the pins of the same potential are internally connected in the device to avoid abnormal operations including latch-up. However, you must connect the pins to external power supply and a ground line to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with the  $V_{CC}$  and  $V_{SS}$  pins of this device at the low impedance.

It is also advisable to connect a ceramic bypass capacitor of approximately 0.1  $\mu$ F between  $V_{CC}$  and  $V_{SS}$  near this device.



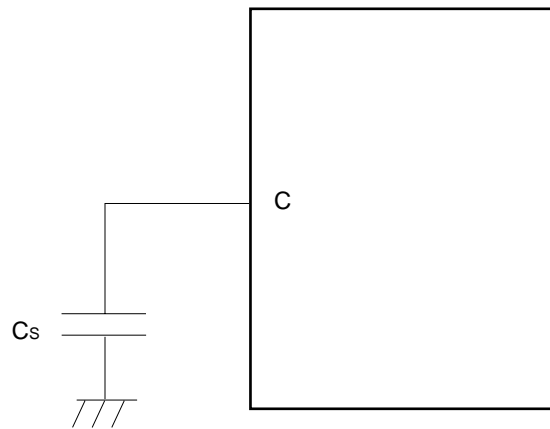
- Mode Pin (MOD)

Connect the mode pin directly to  $V_{CC}$  or  $V_{SS}$  pins.

To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the mode pins to  $V_{CC}$  or  $V_{SS}$  pins and to provide a low-impedance connection.

Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. A bypass capacitor of  $V_{CC}$  pin must have a capacitance value higher than  $C_s$ . For connection of smoothing capacitor  $C_s$ , see the diagram below.

- C pin connection diagram



- Analog Power Supply

Always set the same potential to  $AV_{CC}$  and  $V_{CC}$  pins. When  $V_{CC} > AV_{CC}$ , the current may flow through the AN00 to AN11 pins.

# MB95120H Series

## PROGRAMMING FLASH MEMORY MICROCONTROLLERS USING PARALLEL PROGRAMMER

### Supported Parallel Programmers and Adapters

Package	Applicable adapter model	Parallel programmers
FPT-100P-M05	TEF110-95F128HSPFV	AF9708 (Ver 02.35G or more) AF9709/B (Ver 02.35G or more) AF9723+AF9834 (Ver 02.08E or more)
FPT-100P-M06	TEF110-95F128HSPF	

Note : For information on applicable adapter models and parallel programmers, contact the following:  
Flash Support Group, Inc. TEL: +81-53-428-8380

### Sector Configuration

The individual sectors of Flash memory correspond to addresses used for CPU access and programming by the parallel programmer as follows:

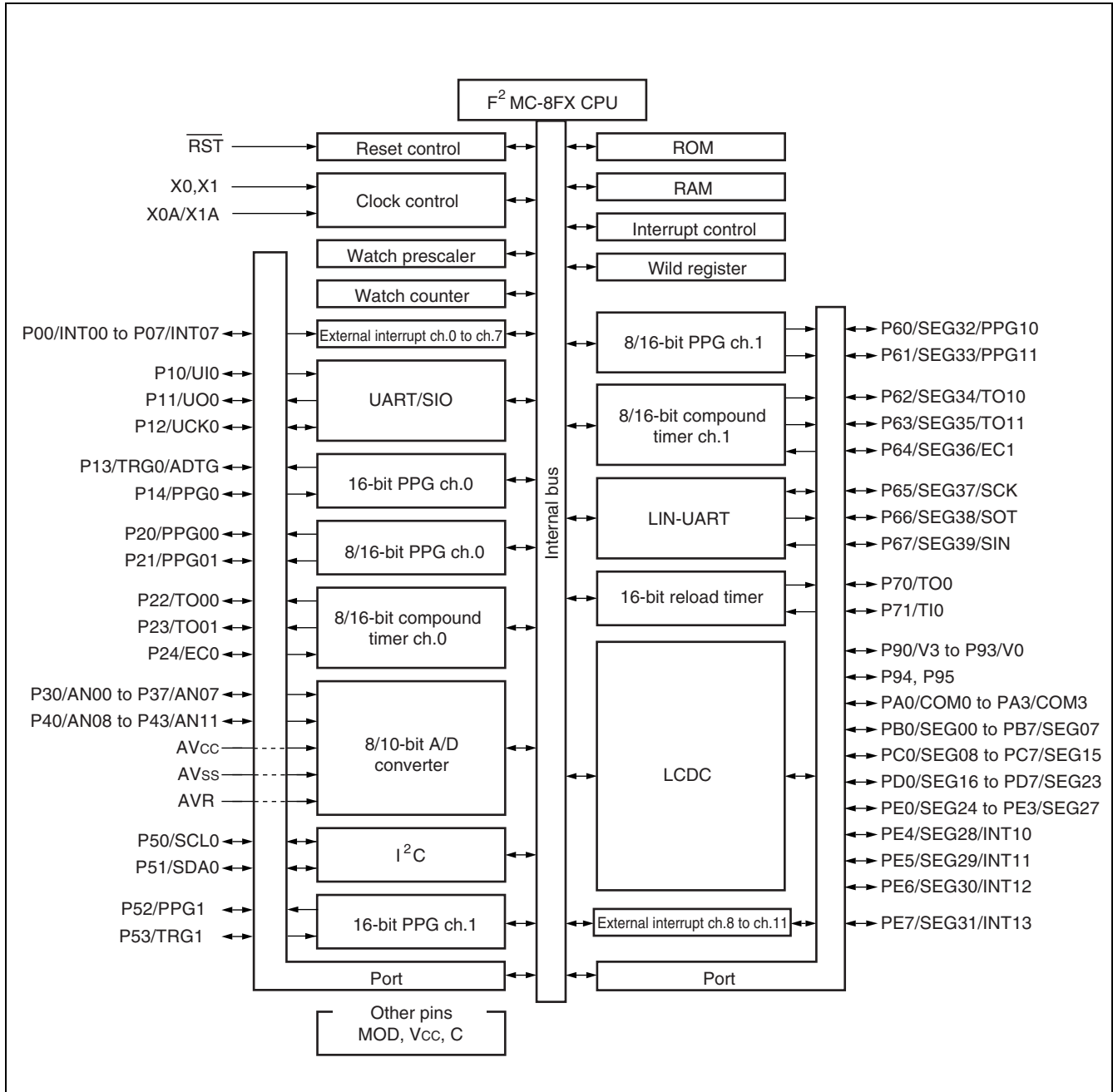
Flash memory	CPU address	Programmer address*
SA1 (4K bytes)	1000 <sub>H</sub>	71000 <sub>H</sub>
SA2 (4K bytes)	1FFF <sub>H</sub>	71FFF <sub>H</sub>
	2000 <sub>H</sub>	72000 <sub>H</sub>
SA3 (4K bytes)	2FFF <sub>H</sub>	72FFF <sub>H</sub>
	3000 <sub>H</sub>	73000 <sub>H</sub>
SA4 (16K bytes)	3FFF <sub>H</sub>	73FFF <sub>H</sub>
	4000 <sub>H</sub>	74000 <sub>H</sub>
SA5 (16K bytes)	7FFF <sub>H</sub>	77FFF <sub>H</sub>
	8000 <sub>H</sub>	78000 <sub>H</sub>
SA6 (4K bytes)	BFFF <sub>H</sub>	7BFFF <sub>H</sub>
	C000 <sub>H</sub>	7C000 <sub>H</sub>
SA7 (4K bytes)	CFFF <sub>H</sub>	7CFFF <sub>H</sub>
	D000 <sub>H</sub>	7D000 <sub>H</sub>
SA8 (4K bytes)	DFFF <sub>H</sub>	7DFFF <sub>H</sub>
	E000 <sub>H</sub>	7E000 <sub>H</sub>
SA9 (4K bytes)	EFFF <sub>H</sub>	7EFFF <sub>H</sub>
	F000 <sub>H</sub>	7F000 <sub>H</sub>
	FFF <sub>H</sub>	7FFF <sub>H</sub>

\*: Programmer addresses are corresponding to CPU addresses, used when the parallel programmer programs data into Flash memory.  
These programmer addresses are used for the parallel programmer to program or erase data in Flash memory.

### Programming Method

- 1) Set the type code of the parallel programmer to 17222.
- 2) Load program data to programmer addresses 71000<sub>H</sub> to 7FFFF<sub>H</sub>.
- 3) Programmed by parallel programmer

## ■ BLOCK DIAGRAM



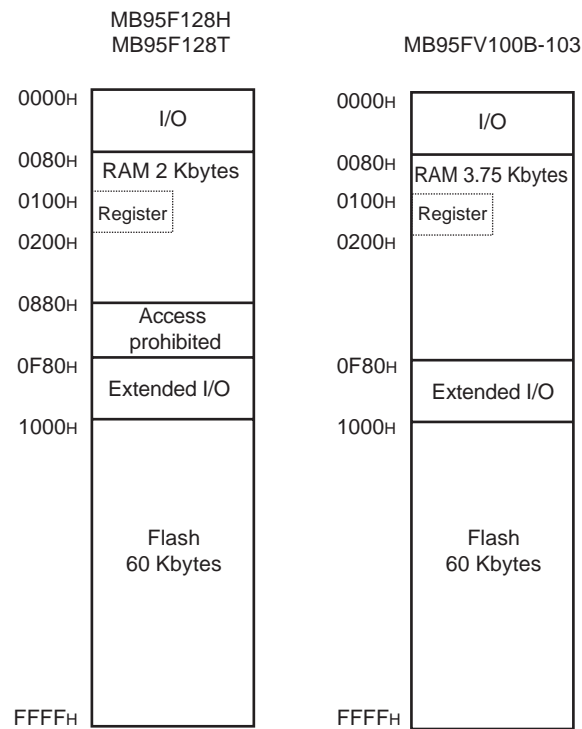
# MB95120H Series

## ■ CPU CORE

### 1. Memory space

Memory space of the MB95120H series is 64K bytes and consists of I/O area, data area, and program area. The memory space includes special - purpose areas such as the general - purpose registers and vector table. Memory map of the MB95120H series is shown below.

- Memory Map



## 2. Register

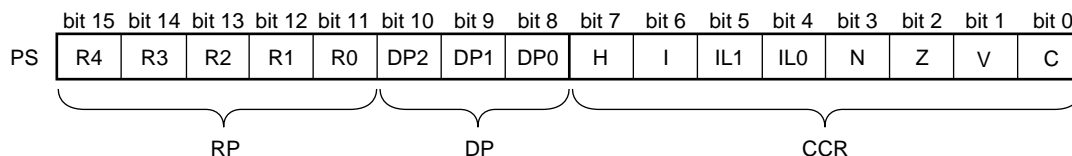
The MB95120H series has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The dedicated registers are as follows:

- Program counter (PC) : A 16-bit register to indicate locations where instructions are stored.
- Accumulator (A) : A 16-bit register for temporary storage of arithmetic operations. In the case of an 8-bit data processing instruction, the lower 1 byte is used.
- Temporary accumulator (T) : A 16-bit register which performs arithmetic operations with the accumulator. In the case of an 8-bit data processing instruction, the lower 1 byte is used.
- Index register (IX) : A 16-bit register for index modification
- Extra pointer (EP) : A 16-bit pointer to point to a memory address.
- Stack pointer (SP) : A 16-bit register to indicate a stack area.
- Program status (PS) : A 16-bit register for storing a register bank pointer, a direct bank pointer, and a condition code register

16-bit		Initial Value
PC	: Program counter	FFFD <sub>H</sub>
A	: Accumulator	0000 <sub>H</sub>
T	: Temporary accumulator	0000 <sub>H</sub>
IX	: Index register	0000 <sub>H</sub>
EP	: Extra pointer	0000 <sub>H</sub>
SP	: Stack pointer	0000 <sub>H</sub>
PS	: Program status	0030 <sub>H</sub>

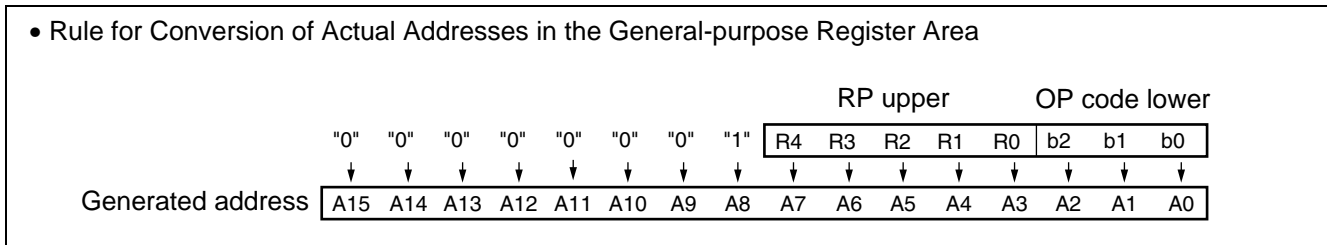
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and a direct bank pointer (DP) and the lower 8 bits for use as a condition code register (CCR) . (See the diagram below.)

### • Structure of the program status



# MB95120H Series

The RP indicates the address of the register bank currently being used. The relationship between the content of RP and the real address conforms to the conversion rule illustrated below:



The DP specifies the area for mapping instructions (16 different instructions such as MOV A, dir) using direct addresses to 0080H to 00FFH.

Direct bank pointer (DP2 to DP0)	Specified address area	Mapping area
XXX <sub>B</sub> (no effect to mapping)	0000 <sub>H</sub> to 007F <sub>H</sub>	0000 <sub>H</sub> to 007F <sub>H</sub> (without mapping)
000 <sub>B</sub> (initial value)	0080 <sub>H</sub> to 00FF <sub>H</sub>	0080 <sub>H</sub> to 00FF <sub>H</sub> (without mapping)
001 <sub>B</sub>		0100 <sub>H</sub> to 017F <sub>H</sub>
010 <sub>B</sub>		0180 <sub>H</sub> to 01FF <sub>H</sub>
011 <sub>B</sub>		0200 <sub>H</sub> to 027F <sub>H</sub>
100 <sub>B</sub>		0280 <sub>H</sub> to 02FF <sub>H</sub>
101 <sub>B</sub>		0300 <sub>H</sub> to 037F <sub>H</sub>
110 <sub>B</sub>		0380 <sub>H</sub> to 03FF <sub>H</sub>
111 <sub>B</sub>		0400 <sub>H</sub> to 047F <sub>H</sub>

The CCR consists of the bits indicating arithmetic operation results or transfer data contents and the bits that control CPU operations at interrupt.

- H flag : Set to "1" when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared to "0" otherwise. This flag is for decimal adjustment instructions.
- I flag : Interrupt is enabled when this flag is set to "1". Interrupt is disabled when this flag is set to "0". The flag is cleared to "0" when reset.
- IL1, IL0 : Indicates the level of the interrupt currently enabled. Processes an interrupt only if its request level is higher than the value indicated by these bits.

IL1	IL0	Interrupt level	Priority
0	0	0	High ↑ ↓ Low = no interruption
0	1	1	
1	0	2	
1	1	3	

- N flag : Set to "1" if the MSB is set to "1" as the result of an arithmetic operation. Cleared to "0" when the bit is set to "0".
- Z flag : Set to "1" when an arithmetic operation results in "0". Cleared to "0" otherwise.
- V flag : Set to "1" if the complement on 2 overflows as a result of an arithmetic operation. Cleared to "0" otherwise.
- C flag : Set to "1" when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared to "0" otherwise. Set to the shift-out value in the case of a shift instruction.

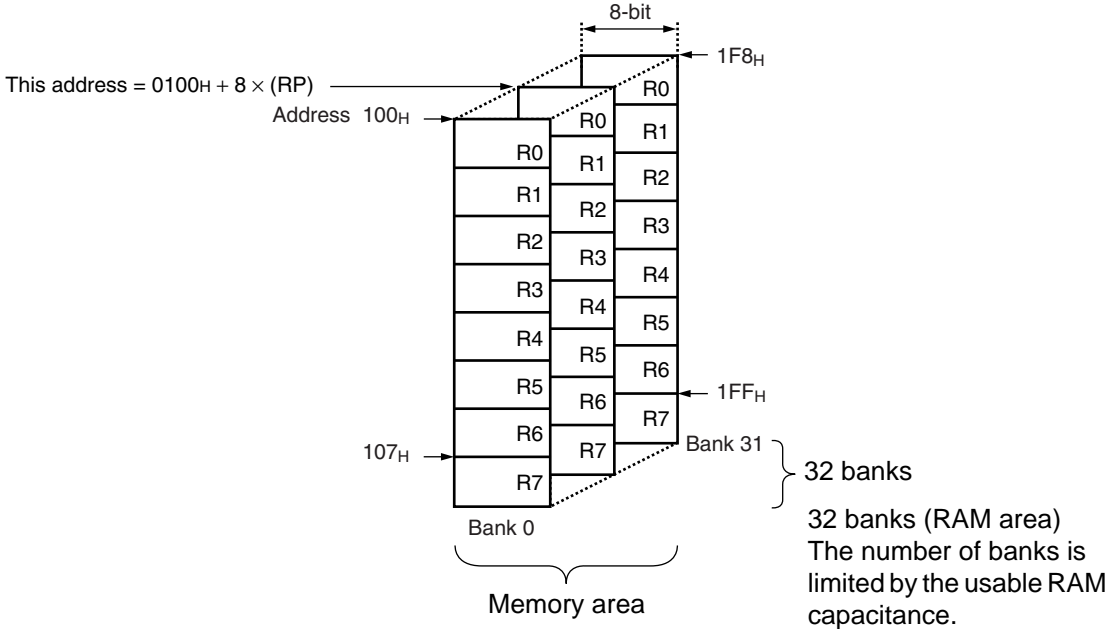
# MB95120H Series

The following general-purpose registers are provided:

General-purpose registers: 8-bit data storage registers

The general-purpose registers are 8 bits and located in the register banks on the memory. 1-bank contains 8-registers. Up to a total of 32 banks can be used on the MB95120H series. The bank currently in use is indicated by the register bank pointer (RP).8-register. Up to a total of 32 banks can be used on the MB95120H series. The bank currently in use is specified by the register bank pointer (RP), and the lower 3 bits of OP code indicates the general-purpose register 0 (R0) to general-purpose register 7 (R7).

- Register Bank Configuration



# MB95120H Series

## ■ I/O MAP

Address	Register abbreviation	Register name	R/W	Initial value
0000 <sub>H</sub>	PDR0	Port 0 data register	R/W	00000000 <sub>B</sub>
0001 <sub>H</sub>	DDR0	Port 0 direction register	R/W	00000000 <sub>B</sub>
0002 <sub>H</sub>	PDR1	Port 1 data register	R/W	00000000 <sub>B</sub>
0003 <sub>H</sub>	DDR1	Port 1 direction register	R/W	00000000 <sub>B</sub>
0004 <sub>H</sub>	—	(Disabled)	—	—
0005 <sub>H</sub>	WATR	Oscillation stabilization wait time setting register	R/W	11111111 <sub>B</sub>
0006 <sub>H</sub>	PLLC	PLL control register	R/W	00000000 <sub>B</sub>
0007 <sub>H</sub>	SYCC	System clock control register	R/W	1010X011 <sub>B</sub>
0008 <sub>H</sub>	STBC	Standby control register	R/W	00000000 <sub>B</sub>
0009 <sub>H</sub>	RSRR	Reset source register	R	XXXXXXXX <sub>B</sub>
000A <sub>H</sub>	TBTC	Timebase timer control register	R/W	00000000 <sub>B</sub>
000B <sub>H</sub>	WPCR	Watch prescaler control register	R/W	00000000 <sub>B</sub>
000C <sub>H</sub>	WDTC	Watchdog timer control register	R/W	00000000 <sub>B</sub>
000D <sub>H</sub>	—	(Disabled)	—	—
000E <sub>H</sub>	PDR2	Port 2 data register	R/W	00000000 <sub>B</sub>
000F <sub>H</sub>	DDR2	Port 2 direction register	R/W	00000000 <sub>B</sub>
0010 <sub>H</sub>	PDR3	Port 3 data register	R/W	00000000 <sub>B</sub>
0011 <sub>H</sub>	DDR3	Port 3 direction register	R/W	00000000 <sub>B</sub>
0012 <sub>H</sub>	PDR4	Port 4 data register	R/W	00000000 <sub>B</sub>
0013 <sub>H</sub>	DDR4	Port 4 direction register	R/W	00000000 <sub>B</sub>
0014 <sub>H</sub>	PDR5	Port 5 data register	R/W	00000000 <sub>B</sub>
0015 <sub>H</sub>	DDR5	Port 5 direction register	R/W	00000000 <sub>B</sub>
0016 <sub>H</sub>	PDR6	Port 6 data register	R/W	00000000 <sub>B</sub>
0017 <sub>H</sub>	DDR6	Port 6 direction register	R/W	00000000 <sub>B</sub>
0018 <sub>H</sub>	PDR7	Port 7 data register	R/W	00000000 <sub>B</sub>
0019 <sub>H</sub>	DDR7	Port 7 direction register	R/W	00000000 <sub>B</sub>
001A <sub>H</sub> , 001B <sub>H</sub>	—	(Disabled)	—	—
001C <sub>H</sub>	PDR9	Port 9 data register	R/W	00000000 <sub>B</sub>
001D <sub>H</sub>	DDR9	Port 9 direction register	R/W	00000000 <sub>B</sub>
001E <sub>H</sub>	PDRA	Port A data register	R/W	00000000 <sub>B</sub>
001F <sub>H</sub>	DDRA	Port A direction register	R/W	00000000 <sub>B</sub>
0020 <sub>H</sub>	PDRB	Port B data register	R/W	00000000 <sub>B</sub>
0021 <sub>H</sub>	DDRB	Port B direction register	R/W	00000000 <sub>B</sub>
0022 <sub>H</sub>	PDRC	Port C data register	R/W	00000000 <sub>B</sub>

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# MB95120H Series

Address	Register abbreviation	Register name	R/W	Initial value
0023 <sub>H</sub>	DDRC	Port C direction register	R/W	00000000 <sub>B</sub>
0024 <sub>H</sub>	PDRD	Port D data register	R/W	00000000 <sub>B</sub>
0025 <sub>H</sub>	DDRD	Port D direction register	R/W	00000000 <sub>B</sub>
0026 <sub>H</sub>	PDRE	Port E data register	R/W	00000000 <sub>B</sub>
0027 <sub>H</sub>	DDRE	Port E direction register	R/W	00000000 <sub>B</sub>
0028 <sub>H</sub> to 002C <sub>H</sub>	—	(Disabled)	—	—
002D <sub>H</sub>	PUL1	Port 1 pull-up register	R/W	00000000 <sub>B</sub>
002E <sub>H</sub>	PUL2	Port 2 pull-up register	R/W	00000000 <sub>B</sub>
002F <sub>H</sub>	PUL3	Port 3 pull-up register	R/W	00000000 <sub>B</sub>
0030 <sub>H</sub>	PUL4	Port 4 pull-up register	R/W	00000000 <sub>B</sub>
0031 <sub>H</sub>	PUL5	Port 5 pull-up register	R/W	00000000 <sub>B</sub>
0032 <sub>H</sub>	PUL7	Port 7 pull-up register	R/W	00000000 <sub>B</sub>
0033 <sub>H</sub> to 0035 <sub>H</sub>	—	(Disabled)	—	—
0036 <sub>H</sub>	T01CR1	8/16-bit compound timer 01 control status register 1 ch.0	R/W	00000000 <sub>B</sub>
0037 <sub>H</sub>	T00CR1	8/16-bit compound timer 00 control status register 1 ch.0	R/W	00000000 <sub>B</sub>
0038 <sub>H</sub>	T11CR1	8/16-bit compound timer 11 control status register 1 ch.1	R/W	00000000 <sub>B</sub>
0039 <sub>H</sub>	T10CR1	8/16-bit compound timer 10 control status register 1 ch.1	R/W	00000000 <sub>B</sub>
003A <sub>H</sub>	PC01	8/16-bit PPG1 control register ch.0	R/W	00000000 <sub>B</sub>
003B <sub>H</sub>	PC00	8/16-bit PPG0 control register ch.0	R/W	00000000 <sub>B</sub>
003C <sub>H</sub>	PC11	8/16-bit PPG1 control register ch.1	R/W	00000000 <sub>B</sub>
003D <sub>H</sub>	PC10	8/16-bit PPG0 control register ch.1	R/W	00000000 <sub>B</sub>
003E <sub>H</sub>	TMCSRH0	16-bit reload timer control status register (upper byte) ch.0	R/W	00000000 <sub>B</sub>
003F <sub>H</sub>	TMCSRL0	16-bit reload timer control status register (lower byte) ch.0	R/W	00000000 <sub>B</sub>
0040 <sub>H</sub> , 0041 <sub>H</sub>	—	(Disabled)	—	—
0042 <sub>H</sub>	PCNTH0	16-bit PPG status control register (upper byte) ch.0	R/W	00000000 <sub>B</sub>
0043 <sub>H</sub>	PCNTL0	16-bit PPG status control register (lower byte) ch.0	R/W	00000000 <sub>B</sub>
0044 <sub>H</sub>	PCNTH1	16-bit PPG status control register (upper byte) ch.1	R/W	00000000 <sub>B</sub>
0045 <sub>H</sub>	PCNTL1	16-bit PPG status control register (lower byte) ch.1	R/W	00000000 <sub>B</sub>
0046 <sub>H</sub> , 0047 <sub>H</sub>	—	(Disabled)	—	—
0048 <sub>H</sub>	EIC00	External interrupt circuit control register ch.0/1	R/W	00000000 <sub>B</sub>
0049 <sub>H</sub>	EIC10	External interrupt circuit control register ch.2/3	R/W	00000000 <sub>B</sub>

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# MB95120H Series

Address	Register abbreviation	Register name	R/W	Initial value
004A <sub>H</sub>	EIC20	External interrupt circuit control register ch.4/5	R/W	00000000 <sub>B</sub>
004B <sub>H</sub>	EIC30	External interrupt circuit control register ch.6/7	R/W	00000000 <sub>B</sub>
004C <sub>H</sub>	EIC01	External interrupt circuit control register ch.8/9	R/W	00000000 <sub>B</sub>
004D <sub>H</sub>	EIC11	External interrupt circuit control register ch.10/11	R/W	00000000 <sub>B</sub>
004E <sub>H</sub> , 004F <sub>H</sub>	—	(Disabled)	—	—
0050 <sub>H</sub>	SCR	LIN-UART serial control register	R/W	00000000 <sub>B</sub>
0051 <sub>H</sub>	SMR	LIN-UART serial mode register	R/W	00000000 <sub>B</sub>
0052 <sub>H</sub>	SSR	LIN-UART serial status register	R/W	00001000 <sub>B</sub>
0053 <sub>H</sub>	RDR/TDR	LIN-UART reception/transmission data register	R/W	00000000 <sub>B</sub>
0054 <sub>H</sub>	ESCR	LIN-UART extended status control register	R/W	00000100 <sub>B</sub>
0055 <sub>H</sub>	ECCR	LIN-UART extended communication control register	R/W	000000XX <sub>B</sub>
0056 <sub>H</sub>	SMC10	UART/SIO serial mode control register 1 ch.0	R/W	00000000 <sub>B</sub>
0057 <sub>H</sub>	SMC20	UART/SIO serial mode control register 2 ch.0	R/W	00100000 <sub>B</sub>
0058 <sub>H</sub>	SSR0	UART/SIO serial status register ch.0	R/W	00000001 <sub>B</sub>
0059 <sub>H</sub>	TDR0	UART/SIO serial output data register ch.0	R/W	00000000 <sub>B</sub>
005A <sub>H</sub>	RDR0	UART/SIO serial input data register ch.0	R	00000000 <sub>B</sub>
005B <sub>H</sub> to 005F <sub>H</sub>	—	(Disabled)	—	—
0060 <sub>H</sub>	IBCR00	I <sup>2</sup> C bus control register 0 ch.0	R/W	00000000 <sub>B</sub>
0061 <sub>H</sub>	IBCR10	I <sup>2</sup> C bus control register 1 ch.0	R/W	00000000 <sub>B</sub>
0062 <sub>H</sub>	IBSR0	I <sup>2</sup> C bus status register ch.0	R	00000000 <sub>B</sub>
0063 <sub>H</sub>	IDDR0	I <sup>2</sup> C data register ch.0	R/W	00000000 <sub>B</sub>
0064 <sub>H</sub>	IAAR0	I <sup>2</sup> C address register ch.0	R/W	00000000 <sub>B</sub>
0065 <sub>H</sub>	ICCR0	I <sup>2</sup> C clock control register ch.0	R/W	00000000 <sub>B</sub>
0066 <sub>H</sub> to 006B <sub>H</sub>	—	(Disabled)	—	—
006C <sub>H</sub>	ADC1	8/10-bit A/D converter control register 1	R/W	00000000 <sub>B</sub>
006D <sub>H</sub>	ADC2	8/10-bit A/D converter control register 2	R/W	00000000 <sub>B</sub>
006E <sub>H</sub>	ADDH	8/10-bit A/D converter data register (upper byte)	R/W	00000000 <sub>B</sub>
006F <sub>H</sub>	ADDL	8/10-bit A/D converter data register (lower byte)	R/W	00000000 <sub>B</sub>
0070 <sub>H</sub>	WCSR	Watch counter status register	R/W	00000000 <sub>B</sub>
0071 <sub>H</sub>	—	(Disabled)	—	—
0072 <sub>H</sub>	FSR	Flash memory status register	R/W	000X0000 <sub>B</sub>

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# MB95120H Series

Address	Register abbreviation	Register name	R/W	Initial value
0073 <sub>H</sub>	SWRE0	FLASH memory sector writing control register 0	R/W	00000000 <sub>B</sub>
0074 <sub>H</sub>	SWRE1	FLASH memory sector writing control register 1	R/W	00000000 <sub>B</sub>
0075 <sub>H</sub>	—	(Disabled)	—	—
0076 <sub>H</sub>	WREN	Wild register address compare enable register	R/W	00000000 <sub>B</sub>
0077 <sub>H</sub>	WROR	Wild register data test setting register	R/W	00000000 <sub>B</sub>
0078 <sub>H</sub>	—	Register bank pointer (RP) , Mirror of direct bank pointer (DP)	—	—
0079 <sub>H</sub>	ILR0	Interrupt level setting register 0	R/W	11111111 <sub>B</sub>
007A <sub>H</sub>	ILR1	Interrupt level setting register 1	R/W	11111111 <sub>B</sub>
007B <sub>H</sub>	ILR2	Interrupt level setting register 2	R/W	11111111 <sub>B</sub>
007C <sub>H</sub>	ILR3	Interrupt level setting register 3	R/W	11111111 <sub>B</sub>
007D <sub>H</sub>	ILR4	Interrupt level setting register 4	R/W	11111111 <sub>B</sub>
007E <sub>H</sub>	ILR5	Interrupt level setting register 5	R/W	11111111 <sub>B</sub>
007F <sub>H</sub>	—	(Disabled)	—	—
0F80 <sub>H</sub>	WRARH0	Wild register address setting register (upper byte) ch.0	R/W	00000000 <sub>B</sub>
0F81 <sub>H</sub>	WRARL0	Wild register address setting register (lower byte) ch.0	R/W	00000000 <sub>B</sub>
0F82 <sub>H</sub>	WRDR0	Wild register data setting register ch.0	R/W	00000000 <sub>B</sub>
0F83 <sub>H</sub>	WRARH1	Wild register address setting register (upper byte) ch.1	R/W	00000000 <sub>B</sub>
0F84 <sub>H</sub>	WRARL1	Wild register address setting register (lower byte) ch.1	R/W	00000000 <sub>B</sub>
0F85 <sub>H</sub>	WRDR1	Wild register data setting register ch.1	R/W	00000000 <sub>B</sub>
0F86 <sub>H</sub>	WRARH2	Wild register address setting register (upper byte) ch.2	R/W	00000000 <sub>B</sub>
0F87 <sub>H</sub>	WRARL2	Wild register address setting register (lower byte) ch.2	R/W	00000000 <sub>B</sub>
0F88 <sub>H</sub>	WRDR2	Wild register data setting register ch.2	R/W	00000000 <sub>B</sub>
0F89 <sub>H</sub> to 0F91 <sub>H</sub>	—	(Disabled)	—	—
0F92 <sub>H</sub>	T01CR0	8/16-bit compound timer 01 control status register 0 ch.0	R/W	00000000 <sub>B</sub>
0F93 <sub>H</sub>	T00CR0	8/16-bit compound timer 00 control status register 0 ch.0	R/W	00000000 <sub>B</sub>
0F94 <sub>H</sub>	T01DR	8/16-bit compound timer 01 data register ch.0	R/W	00000000 <sub>B</sub>
0F95 <sub>H</sub>	T00DR	8/16-bit compound timer 00 data register ch.0	R/W	00000000 <sub>B</sub>
0F96 <sub>H</sub>	TMCR0	8/16-bit compound timer 00/01 timer mode control register ch.0	R/W	00000000 <sub>B</sub>
0F97 <sub>H</sub>	T11CR0	8/16-bit compound timer 11 control status register 0 ch.1	R/W	00000000 <sub>B</sub>
0F98 <sub>H</sub>	T10CR0	8/16-bit compound timer 10 control status register 0 ch.1	R/W	00000000 <sub>B</sub>
0F99 <sub>H</sub>	T11DR	8/16-bit compound timer 11 data register ch.1	R/W	00000000 <sub>B</sub>
0F9A <sub>H</sub>	T10DR	8/16-bit compound timer 10 data register ch.1	R/W	00000000 <sub>B</sub>

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# MB95120H Series

Address	Register abbreviation	Register name	R/W	Initial value
0F9B <sub>H</sub>	TMCR1	8/16-bit compound timer 10/11 timer mode control register ch.1	R/W	00000000 <sub>B</sub>
0F9C <sub>H</sub>	PPS01	8/16-bit PPG1 cycle setting buffer register ch.0	R/W	11111111 <sub>B</sub>
0F9D <sub>H</sub>	PPS00	8/16-bit PPG0 cycle setting buffer register ch.0	R/W	11111111 <sub>B</sub>
0F9E <sub>H</sub>	PDS01	8/16-bit PPG1 duty setting buffer register ch.0	R/W	11111111 <sub>B</sub>
0F9F <sub>H</sub>	PDS00	8/16-bit PPG0 duty setting buffer register ch.0	R/W	11111111 <sub>B</sub>
0FA0 <sub>H</sub>	PPS11	8/16-bit PPG1 cycle setting buffer register ch.1	R/W	11111111 <sub>B</sub>
0FA1 <sub>H</sub>	PPS10	8/16-bit PPG0 cycle setting buffer register ch.1	R/W	11111111 <sub>B</sub>
0FA2 <sub>H</sub>	PDS11	8/16-bit PPG1 duty setting buffer register ch.1	R/W	11111111 <sub>B</sub>
0FA3 <sub>H</sub>	PDS10	8/16-bit PPG0 duty setting buffer register ch.1	R/W	11111111 <sub>B</sub>
0FA4 <sub>H</sub>	PPGS	8/16-bit PPG start register	R/W	00000000 <sub>B</sub>
0FA5 <sub>H</sub>	REVC	8/16-bit PPG output inversion register	R/W	00000000 <sub>B</sub>
0FA6 <sub>H</sub>	TMRH0/ TMRLRH0	16-bit reload timer timer/reload register (upper byte) ch.0	R/W	00000000 <sub>B</sub>
0FA7 <sub>H</sub>	TMRL0/ TMRLRLO	16-bit reload timer timer/reload register (lower byte) ch.0	R/W	00000000 <sub>B</sub>
0FA8 <sub>H</sub> , 0FA9 <sub>H</sub>	—	(Disabled)	—	—
0FAA <sub>H</sub>	PDCRH0	16-bit PPG down counter register (upper byte) ch.0	R	00000000 <sub>B</sub>
0FAB <sub>H</sub>	PDCRL0	16-bit PPG down counter register (lower byte) ch.0	R	00000000 <sub>B</sub>
0FAC <sub>H</sub>	PCSRH0	16-bit PPG cycle setting buffer register (upper byte) ch.0	R/W	11111111 <sub>B</sub>
0FAD <sub>H</sub>	PCSRL0	16-bit PPG cycle setting buffer register (lower byte) ch.0	R/W	11111111 <sub>B</sub>
0FAE <sub>H</sub>	PDUTH0	16-bit PPG duty setting buffer register (upper byte) ch.0	R/W	11111111 <sub>B</sub>
0FAF <sub>H</sub>	PDUTL0	16-bit PPG duty setting buffer register (lower byte) ch.0	R/W	11111111 <sub>B</sub>
0FB0 <sub>H</sub>	PDCRH1	16-bit PPG down counter register (upper byte) ch.1	R	00000000 <sub>B</sub>
0FB1 <sub>H</sub>	PDCRL1	16-bit PPG down counter register (lower byte) ch.1	R	00000000 <sub>B</sub>
0FB2 <sub>H</sub>	PCSRH1	16-bit PPG cycle setting buffer register (upper byte) ch.1	R/W	11111111 <sub>B</sub>
0FB3 <sub>H</sub>	PCSRL1	16-bit PPG cycle setting buffer register (lower byte) ch.1	R/W	11111111 <sub>B</sub>
0FB4 <sub>H</sub>	PDUTH1	16-bit PPG duty setting buffer register (upper byte) ch.1	R/W	11111111 <sub>B</sub>
0FB5 <sub>H</sub>	PDUTL1	16-bit PPG duty setting buffer register (lower byte) ch.1	R/W	11111111 <sub>B</sub>
0FB6 <sub>H</sub> to 0FBB <sub>H</sub>	—	(Disabled)	—	—
0FBC <sub>H</sub>	BGR1	LIN-UART baud rate generator register 1	R/W	00000000 <sub>B</sub>
0FBD <sub>H</sub>	BGR0	LIN-UART baud rate generator register 0	R/W	00000000 <sub>B</sub>
0FBE <sub>H</sub>	PSSR0	UART/SIO dedicated baud rate generator prescaler select register ch.0	R/W	00000000 <sub>B</sub>

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Address	Register abbreviation	Register name	R/W	Initial value
0FBFH	BRSR0	UART/SIO dedicated baud rate generator baud rate setting register ch.0	R/W	00000000 <sub>B</sub>
0FC0H, 0FC1H	—	(Disabled)	—	—
0FC2H	AIDRH	A/D input disable register (upper byte)	R/W	00000000 <sub>B</sub>
0FC3H	AIDRL	A/D input disable register (lower byte)	R/W	00000000 <sub>B</sub>
0FC4H	LCDCC	LCDC control register	R/W	00010000 <sub>B</sub>
0FC5H	LCDCE1	LCDC enable register 1	R/W	00110000 <sub>B</sub>
0FC6H	LCDCE2	LCDC enable register 2	R/W	00000000 <sub>B</sub>
0FC7H	LCDCE3	LCDC enable register 3	R/W	00000000 <sub>B</sub>
0FC8H	LCDCE4	LCDC enable register 4	R/W	00000000 <sub>B</sub>
0FC9H	LCDCE5	LCDC enable register 5	R/W	00000000 <sub>B</sub>
0FCAH	LCDCE6	LCDC enable register 6	R/W	00000000 <sub>B</sub>
0FCBH	LCDCB1	LCDC blinking setting register 1	R/W	00000000 <sub>B</sub>
0FCC <sub>H</sub>	LCDCB2	LCDC blinking setting register 2	R/W	00000000 <sub>B</sub>
0FCD <sub>H</sub> to 0FE0 <sub>H</sub>	LCDRAM	LCDC display RAM	R/W	00000000 <sub>B</sub>
0FE1 <sub>H</sub> , 0FE2 <sub>H</sub>	—	(Disabled)	—	—
0FE3 <sub>H</sub>	WCDR	Watch counter data register	R/W	00111111 <sub>B</sub>
0FE4 <sub>H</sub> to 0FED <sub>H</sub>	—	(Disabled)	—	—
0FEE <sub>H</sub>	ILSR	Input level select register	R/W	00000000 <sub>B</sub>
0FEF <sub>H</sub>	WICR	Interrupt pin select circuit control register	R/W	01000000 <sub>B</sub>
0FF0 <sub>H</sub> to 0FFF <sub>H</sub>	—	(Disabled)	—	—

- R/W access symbols

R/W : Readable/Writable

R : Read only

W : Write only

- Initial value symbols

0 : The initial value of this bit is "0".


1 : The initial value of this bit is "1".

X : The initial value of this bit is undefined.

Note : Do not write to the "(Disabled)". Reading the "(Disabled)" returns an undefined value.

# MB95120H Series

## ■ INTERRUPT SOURCE TABLE

Interrupt source	Interrupt request number	Vector table address		Bit name of interrupt level setting register	Same level priority order (at simultaneous occurrence)
		Upper	Lower		
External interrupt ch.0	IRQ0	FFFA <sub>H</sub>	FFFB <sub>H</sub>	L00 [1 : 0]	High 
External interrupt ch.4					
External interrupt ch.1	IRQ1	FFF8 <sub>H</sub>	FFF9 <sub>H</sub>	L01 [1 : 0]	
External interrupt ch.5					
External interrupt ch.2	IRQ2	FFF6 <sub>H</sub>	FFF7 <sub>H</sub>	L02 [1 : 0]	
External interrupt ch.6					
External interrupt ch.3	IRQ3	FFF4 <sub>H</sub>	FFF5 <sub>H</sub>	L03 [1 : 0]	
External interrupt ch.7					
UART/SIO ch.0	IRQ4	FFF2 <sub>H</sub>	FFF3 <sub>H</sub>	L04 [1 : 0]	
8/16-bit compound timer ch.0 (Lower)	IRQ5	FFF0 <sub>H</sub>	FFF1 <sub>H</sub>	L05 [1 : 0]	
8/16-bit compound timer ch.0 (Upper)	IRQ6	FFEE <sub>H</sub>	FFEF <sub>H</sub>	L06 [1 : 0]	
LIN-UART (reception)	IRQ7	FFEC <sub>H</sub>	FFED <sub>H</sub>	L07 [1 : 0]	
LIN-UART (transmission)	IRQ8	FFEA <sub>H</sub>	FFEB <sub>H</sub>	L08 [1 : 0]	
8/16-bit PPG ch.1 (Lower)	IRQ9	FFE8 <sub>H</sub>	FFE9 <sub>H</sub>	L09 [1 : 0]	
8/16-bit PPG ch.1 (Upper)	IRQ10	FFE6 <sub>H</sub>	FFE7 <sub>H</sub>	L10 [1 : 0]	
16-bit reload timer ch.0	IRQ11	FFE4 <sub>H</sub>	FFE5 <sub>H</sub>	L11 [1 : 0]	
8/16-bit PPG ch.0 (Upper)	IRQ12	FFE2 <sub>H</sub>	FFE3 <sub>H</sub>	L12 [1 : 0]	
8/16-bit PPG ch.0 (Lower)	IRQ13	FFE0 <sub>H</sub>	FFE1 <sub>H</sub>	L13 [1 : 0]	
8/16-bit compound timer ch.1 (Upper)	IRQ14	FFDE <sub>H</sub>	FFDF <sub>H</sub>	L14 [1 : 0]	
16-bit PPG ch.0	IRQ15	FFDC <sub>H</sub>	FFDD <sub>H</sub>	L15 [1 : 0]	
I <sup>2</sup> C ch.0	IRQ16	FFDA <sub>H</sub>	FFDB <sub>H</sub>	L16 [1 : 0]	
16-bit PPG ch.1	IRQ17	FFD8 <sub>H</sub>	FFD9 <sub>H</sub>	L17 [1 : 0]	
8/10-bit A/D converter	IRQ18	FFD6 <sub>H</sub>	FFD7 <sub>H</sub>	L18 [1 : 0]	
Timebase timer	IRQ19	FFD4 <sub>H</sub>	FFD5 <sub>H</sub>	L19 [1 : 0]	
Watch timer/counter	IRQ20	FFD2 <sub>H</sub>	FFD3 <sub>H</sub>	L20 [1 : 0]	
External interrupt ch.8	IRQ21	FFD0 <sub>H</sub>	FFD1 <sub>H</sub>	L21 [1 : 0]	
External interrupt ch.9					
External interrupt ch.10					
External interrupt ch.11					
8/16-bit compound timer ch.1 (Lower)	IRQ22	FFCE <sub>H</sub>	FFCF <sub>H</sub>	L22 [1 : 0]	
Flash memory	IRQ23	FFCC <sub>H</sub>	FFCD <sub>H</sub>	L23 [1 : 0]	

## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V <sub>CC</sub> AV <sub>CC</sub>	V <sub>SS</sub> - 0.3	V <sub>SS</sub> + 6.0	V	*2
	AVR	V <sub>SS</sub> - 0.3	V <sub>SS</sub> + 6.0		*2
Power supply voltage for LCD	V <sub>0</sub> to V <sub>3</sub>	V <sub>SS</sub> - 0.3	V <sub>SS</sub> + 6.0	V	*3
Input voltage*1	V <sub>I</sub>	V <sub>SS</sub> - 0.3	V <sub>SS</sub> + 6.0	V	*4
Output voltage*1	V <sub>O</sub>	V <sub>SS</sub> - 0.3	V <sub>SS</sub> + 6.0	V	*4
Maximum clamp current	I <sub>CLAMP</sub>	- 2.0	+ 2.0	mA	Applicable to pins*5
Total maximum clamp current	Σ I <sub>CLAMP</sub>	—	20	mA	Applicable to pins*5
“L” level maximum output current	I <sub>OL1</sub>	—	15	mA	Other than P00 to P07
	I <sub>OL2</sub>		15		P00 to P07
“L” level average current	I <sub>OLAV1</sub>	—	4	mA	Other than P00 to P07 Average output current = operating current × operating ratio (1 pin)
	I <sub>OLAV2</sub>		12		P00 to P07 Average output current = operating current × operating ratio (1 pin)
“L” level total maximum output current	ΣI <sub>OL</sub>	—	100	mA	
“L” level total average output current	ΣI <sub>OLAV</sub>	—	50	mA	Total average output current = operating current × operating ratio (Total of pins)
“H” level maximum output current	I <sub>OH1</sub>	—	- 15	mA	Other than P00 to P07
	I <sub>OH2</sub>		- 15		P00 to P07
“H” level average current	I <sub>OHAV1</sub>	—	- 4	mA	Other than P00 to P07 Average output current = operating current × operating ratio (1 pin)
	I <sub>OHAV2</sub>		- 8		P00 to P07 Average output current = operating current × operating ratio (1 pin)
“H” level total maximum output current	ΣI <sub>OH</sub>	—	- 100	mA	
“H” level total average output current	ΣI <sub>OHAV</sub>	—	- 50	mA	Total average output current = operating current × operating ratio (Total of pins)

(Continued)

# MB95120H Series

(Continued)

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power consumption	Pd	—	320	mW	
Operating temperature	T <sub>A</sub>	- 40	+ 85	°C	
Storage temperature	T <sub>stg</sub>	- 55	+ 150	°C	

\*1 : The parameter is based on AV<sub>ss</sub> = V<sub>ss</sub> = 0.0 V.

\*2 : Apply equal potential to AV<sub>cc</sub> and V<sub>cc</sub>. AVR should not exceed AV<sub>cc</sub> + 0.3 V.

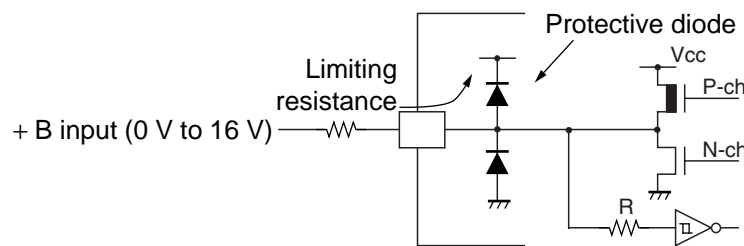
\*3 : V<sub>0</sub> to V<sub>3</sub> should not exceed V<sub>cc</sub> + 0.3 V.

\*4 : V<sub>i</sub> and V<sub>o</sub> should not exceed V<sub>cc</sub> + 0.3 V. V<sub>i</sub> must not exceed the rating voltage. However, if the maximum current to/from an input is limited by some means with external components, the I<sub>CLAMP</sub> rating supersedes the V<sub>i</sub> rating.

\*5 : Applicable to pins : P00 to P07, P10 to P14, P20 to P24, P30 to P37, P40 to P43, P52, P53

- Use within recommended operating conditions.
- Use at DC voltage (current).
- +B signal is an input signal that exceeds V<sub>cc</sub> voltage. The + B signal should always be applied a limiting resistance placed between the + B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the + B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V<sub>cc</sub> pin, and this affects other devices.
- Note that if the + B signal is inputted when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the + B input is applied during power-on, the power supply is provided from the pins and the resulting power supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the + B input pin open.
- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, etc.) cannot accept +B signal input.
- Sample recommended circuits :

• Input/Output Equivalent circuits



**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.



## 2. Recommended Operating Conditions

( $V_{SS} = V_{SS} = 0.0\text{ V}$ )

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks	
				Min	Max			
Power supply voltage	$V_{CC}, AV_{CC}$	—	—	2.5*1,*2	5.5*1	V	In normal operating	MB95F128H MB95F128T
		—	—	2.3	5.5		Hold condition in STOP mode	
		—	—	2.7	5.5		In normal operating	MB95FV100B-103
		—	—	2.3	5.5		Hold condition in STOP mode	
Power supply voltage for LCD	$V_0$ to $V_3$	—	—	$V_{SS}$	$V_{CC}$	V	The range of liquid crystal power supply: without up-conversion (The optimal value depends on liquid crystal display elements used.)	
"H" level input voltage	$V_{IH1}$	P10 (selectable at UI), P67 (selectable at SIN)	—	$0.7 V_{CC}$	$V_{CC} + 0.3$	V	Hysteresis input (When selecting CMOS input level)	
	$V_{IH2}$	P50, P51 (selectable at I <sup>2</sup> C)	—	$0.7 V_{CC}$	$V_{SS} + 5.5$	V		
	$V_{IHS1}$	P00 to P07, P10 to P14, P20 to P24, P30 to P37, P40 to P43, P52, P53, P60 to P67, P70, P71, P90 to P95, PA0 to PA3, PB0 to PB7, PC0 to PC7, PD0 to PD7, PE0 to PE7	—	$0.8 V_{CC}$	$V_{CC} + 0.3$	V	Hysteresis input	
	$V_{IHS2}$	P50, P51	—	$0.8 V_{CC}$	$V_{SS} + 5.5$	V		
	$V_{IHM}$	RST, MOD	—	$0.8 V_{CC}$	$V_{CC} + 0.3$	V	Hysteresis input	
"L" level input voltage	$V_{IL}$	P10 (selectable at UI), P50, P51 (selectable at I <sup>2</sup> C) P67 (selectable at SIN)	—	$V_{SS} - 0.3$	$0.3 V_{CC}$	V	Hysteresis input (When selecting CMOS input level)	

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# MB95120H Series

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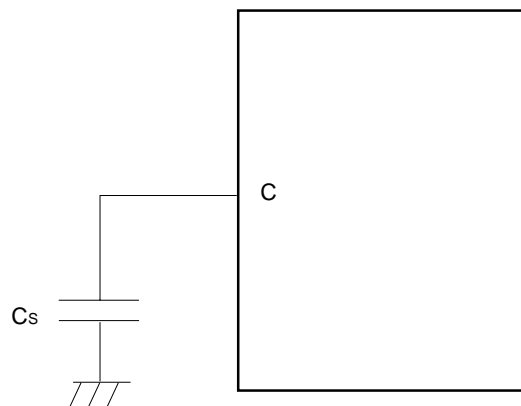
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
“L” level input voltage	$V_{ILS}$	P00 to P07, P10 to P14, P20 to P24, P30 to P37, P40 to P43, P50 to P53, P60 to P67, P70, P71, P90 to P95, PA0 to PA3, PB0 to PB7, PC0 to PC7, PD0 to PD7, PE0 to PE7	—	$V_{SS} - 0.3$	$0.2 V_{CC}$	V	Hysteresis input
	$V_{ILM}$	$\overline{RST}$ , MOD	—	$V_{SS} - 0.3$	$0.2 V_{CC}$	V	Hysteresis input
A/D converter reference input voltage	AVR	—	—	4.0	$AV_{CC}$	V	
Smoothing capacitor	$C_s$	—	—	0.1	1.0	$\mu F$	*3
Operating temperature	$T_A$	—	—	- 40	+ 85	$^{\circ}C$	MB95F128H, MB95F128T
				+ 5	+ 35	$^{\circ}C$	MB95FV100B-103

\*1 : The values vary with the operating frequency, machine clock or analog guarantee range.

\*2 : The value is 2.9 V when the low voltage detection reset is used.

\*3 : Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. A bypass capacitor of  $V_{CC}$  pin must have a capacitor value higher than  $C_s$ . For connection of smoothing capacitor  $C_s$ , see the diagram below.

- C pin connection diagram



**WARNING:** The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

# MB95120H Series

## 3. DC Characteristics

( $V_{CC} = AV_{CC} = 5.0\text{ V} \pm 10\%$ ,  $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
“H” level output voltage	$V_{OH1}$	Output pin other than P00 to P07	$I_{OH} = -4.0\text{ mA}$	4.0	—	—	V	
	$V_{OH2}$	P00 to P07	$I_{OH} = -8.0\text{ mA}$	4.0	—	—	V	
“L” level output voltage	$V_{OL1}$	Output pin other than P00 to P07, $\overline{RST}$	$I_{OL} = 4.0\text{ mA}$	—	—	0.4	V	
	$V_{OL2}$	P00 to P07	$I_{OL} = 12\text{ mA}$	—	—	0.4	V	
Open-drain output application voltage	$V_{D1}$	P50, P51	—	$V_{SS} - 0.3$	—	$V_{SS} + 5.5$	V	
Input leakage current (Hi-Z output leakage current)	$I_{LI}$	Port other than P50, P51	$0.0\text{ V} < V_I < V_{CC}$	-5	—	+5	$\mu\text{A}$	When the pull-up prohibition setting
Open-drain output leakage current	$I_{LIOD}$	P50, P51, P72, P73, P80 to P83	$0.0\text{ V} < V_I < V_{SS} + 5.5\text{ V}$	—	—	5	$\mu\text{A}$	
Pull-up resistor	$R_{PULL}$	P10 to P14, P20 to P24, P30 to P37, P40 to P43, P52, P53, P70, P71	$V_I = 0.0\text{ V}$	25	50	100	$\text{k}\Omega$	When the pull-up permission setting
Input capacitance	$C_{IN}$	Other than $AV_{CC}$ , $AV_{SS}$ , AVR, $V_{CC}$ , $V_{SS}$	$f = 1\text{ MHz}$	—	5	15	pF	
Power supply current*	$I_{CC}$	$V_{CC}$ (External clock operation)	$F_{CH} = 20\text{ MHz}$ $F_{MP} = 10\text{ MHz}$ Main clock mode (divided by 2)	—	9.5	12.5	mA	At other than Flash memory writing and erasing
			$F_{CH} = 20\text{ MHz}$ $F_{MP} = 10\text{ MHz}$ Main Sleep mode (divided by 2)	—	30.0	35.0	mA	At Flash memory writing and erasing
	$I_{CCS}$		$F_{CH} = 20\text{ MHz}$ $F_{MP} = 10\text{ MHz}$ Main Sleep mode (divided by 2)	—	4.5	7.5	mA	

(Continued)

# MB95120H Series

( $V_{CC} = AV_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $AV_{SS} = V_{SS} = 0.0 \text{ V}$ ,  $T_A = -40 \text{ }^\circ\text{C}$  to  $+85 \text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*	I <sub>CCL</sub>	V <sub>CC</sub> (External clock operation)	F <sub>CL</sub> = 32 kHz F <sub>MPL</sub> = 16 kHz sub clock mode (divided by 2)	—	45	100	μA	
	I <sub>CCLS</sub>		F <sub>CL</sub> = 32 kHz F <sub>MPL</sub> = 16 kHz Sub sleep mode (divided by 2)	—	10	81	μA	
	I <sub>CCT</sub>		F <sub>CL</sub> = 32 kHz Watch mode Main stop mode T <sub>A</sub> = +25 °C	—	4.6	27.0	μA	
	I <sub>CCMPLL</sub>		F <sub>CH</sub> = 4 MHz F <sub>MP</sub> = 10 MHz Main PLL mode (multiplied by 2.5)	—	9.3	12.5	mA	
	I <sub>CCSPLL</sub>		F <sub>CL</sub> = 32 kHz F <sub>MPL</sub> = 128 kHz Sub PLL mode (multiplied by 4), T <sub>A</sub> = +25 °C	—	160	400	μA	
	I <sub>CTS</sub>		F <sub>CH</sub> = 10 MHz Timebase timer mode T <sub>A</sub> = +25 °C	—	0.40	1.10	mA	
	I <sub>CCH</sub>		Sub stop mode T <sub>A</sub> = +25 °C	—	3.5	20	μA	
	I <sub>A</sub>	AV <sub>CC</sub>	F <sub>CH</sub> = 10 MHz At operating of A/D conversion	—	2.4	4.7	mA	
	I <sub>AH</sub>		F <sub>CH</sub> = 10 MHz At stopping of A/D conversion T <sub>A</sub> = +25 °C	—	1	5	μA	
LCD internal division resistance	R <sub>LCD</sub>	—	Between V <sub>3</sub> and V <sub>SS</sub>	—	300	—	kΩ	
COM0 to COM3 output impedance	R <sub>VCOM</sub>	COM0 to COM3	V1 to V3 = 3.6 V	—	—	5	kΩ	

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# MB95120H Series

(Continued)

( $V_{CC} = AV_{CC} = 5.0\text{ V}$ ,  $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ °C to }+85\text{ °C}$ )

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
SEG00 to SEG39 output impedance	$R_{VSEG}$	SEG00 to SEG39	—	—	—	7	k $\Omega$	
LCD leak current	$I_{LCDL}$	V0 to V3, COM0 to COM3 SEG00 to SEG39	—	-1	—	+1	$\mu\text{A}$	

- \* :
- The power-supply current is determined by the external clock. When both low voltage detection option is selected, the power-supply current will be a value of adding current consumption of the low voltage detection circuit ( $I_{LVD}$ ) to the specified value.
  - Refer to "4. AC characteristics (1) Clock Timing" for  $F_{CH}$  and  $F_{CL}$ .
  - Refer to "4. AC characteristics (2) Source Clock/Machine Clock" for  $F_{MP}$  and  $F_{MPL}$ .

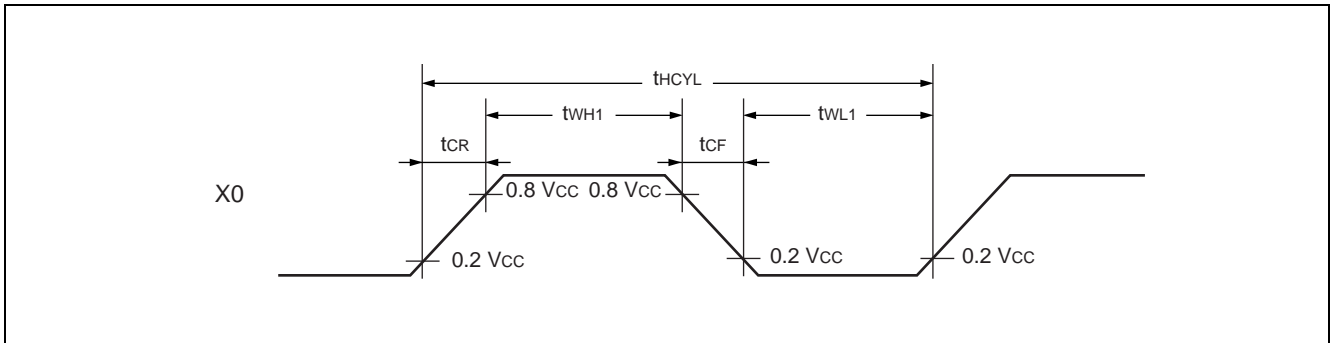
# MB95120H Series

## 4. AC Characteristics

### (1) Clock Timing

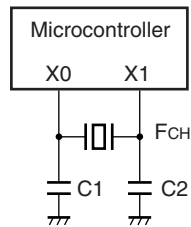
( $V_{CC} = 2.5\text{ V to } 5.5\text{ V}$ ,  $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C to } +85\text{ }^\circ\text{C}$ )

Parameter	Sym- bol	Pin name	Condi- tions	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F <sub>CH</sub>	X0, X1	—	1	—	10	MHz	When using main oscillation circuit
				1	—	20	MHz	When using external clock
				3	—	10	MHz	Main PLL multiplied by 1
				3	—	5	MHz	Main PLL multiplied by 2
				3	—	4	MHz	Main PLL multiplied by 2.5
	F <sub>CL</sub>	X0A, X1A		—	32.768	—	kHz	When using sub oscillation circuit
			—	32.768	—	kHz	When using sub PLL $V_{CC} = 2.3\text{ V to } 3.6\text{ V}$	
Clock cycle time	t <sub>H CYL</sub>	X0, X1	100	—	1000	ns	When using main oscillation circuit	
			50	—	1000	ns	When using external clock	
	t <sub>L CYL</sub>	X0A, X1A	—	30.5	—	μs	When using sub oscillation circuit	
Input clock pulse width	t <sub>WH1</sub> t <sub>WL1</sub>	X0	10	—	—	ns	When using external clock Duty ratio is about 30% to 70%.	
	t <sub>WH2</sub> t <sub>WL2</sub>	X0A	—	15.2	—	μs		
Input clock rise time and fall time	t <sub>CR</sub> t <sub>CF</sub>	X0, X0A	—	—	5	ns	When using external clock	

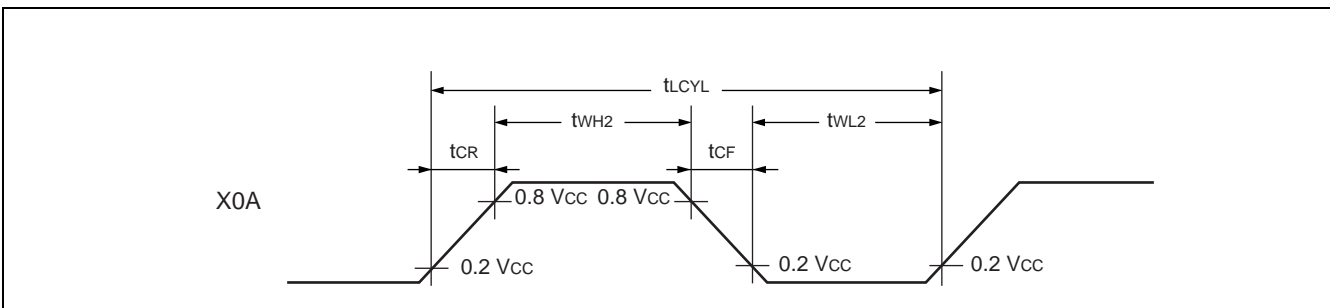
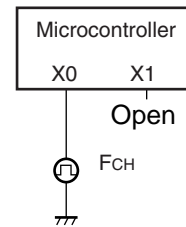


• Figure of Main Clock Input Port External Connection

When using a crystal or ceramic oscillator

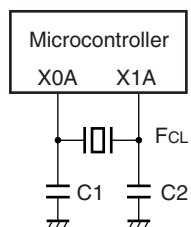


When using external clock

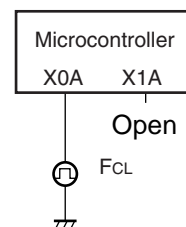


• Figure of Sub clock Input Port External Connection

When using a crystal or ceramic oscillator



When using external clock



# MB95120H Series

## (2) Source Clock/Machine Clock

( $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

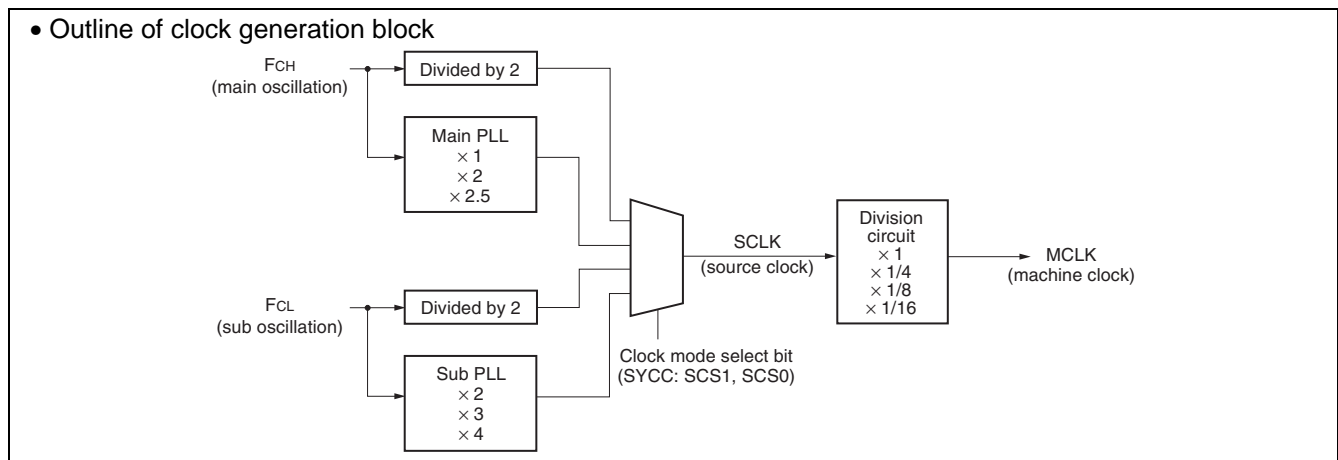
Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Source clock cycle time*1 (Clock before setting division)	$t_{SCLK}$	—	100	—	2000	ns	When using main clock Min : $F_{CH} = 10\text{ MHz}$ , PLL multiplied by 1 Max : $F_{CH} = 1\text{ MHz}$ , divided by 2
			7.6	—	61.0	$\mu\text{s}$	When using sub clock Min : $F_{CL} = 32\text{ kHz}$ , PLL multiplied by 4 Max : $F_{CL} = 32\text{ kHz}$ , divided by 2
Source clock frequency	$F_{SP}$	—	0.5	—	10.0	MHz	When using main clock
	$F_{SPL}$	—	16.384	—	131.072	kHz	When using sub clock
Machine clock cycle time*2 (Minimum instruction execution time)	$t_{MCLK}$	—	100	—	32000	ns	When using main clock Min : $F_{SP} = 10\text{ MHz}$ , no division Max : $F_{SP} = 0.5\text{ MHz}$ , divided by 16
			7.6	—	976.5	$\mu\text{s}$	When using sub clock Min : $F_{SPL} = 131\text{ kHz}$ , no division Max : $F_{SPL} = 16\text{ kHz}$ , divided by 16
Machine clock frequency	$F_{MP}$	—	0.031	—	10.000	MHz	When using main clock
	$F_{MPL}$	—	1.024	—	131.072	kHz	When using sub clock

\*1 : Clock before setting division due to machine clock division ratio selection bit (SYCC : DIV1 and DIV0) . This source clock is divided by the machine clock division ratio selection bit (SYCC : DIV1 and DIV0) , and it becomes the machine clock. Further, the source clock can be selected as follows.

- Main clock divided by 2
- PLL multiplication of main clock (select from 1, 2, 2.5 multiplication)
- Sub clock divided by 2
- PLL multiplication of sub clock (select from 2, 3, 4 multiplication)

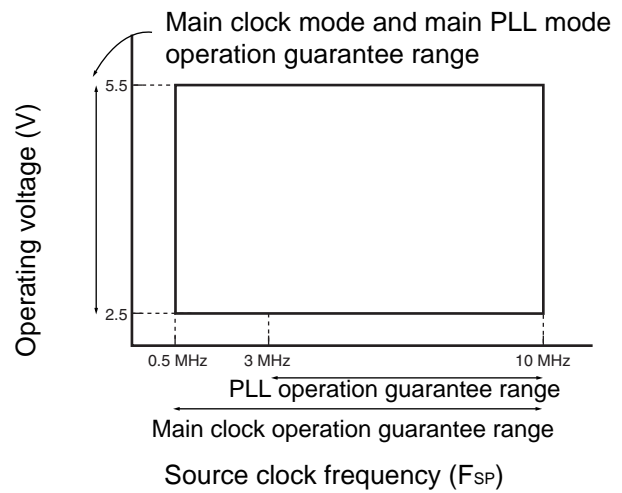
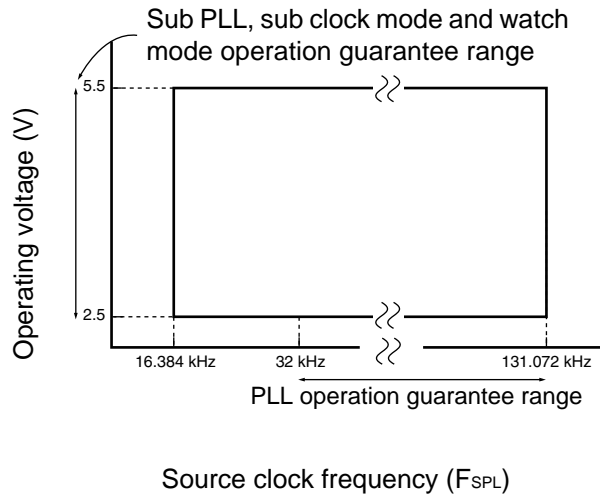
\*2 : Operation clock of the microcontroller. Machine clock can be selected as follows.

- Source clock (no division)
- Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

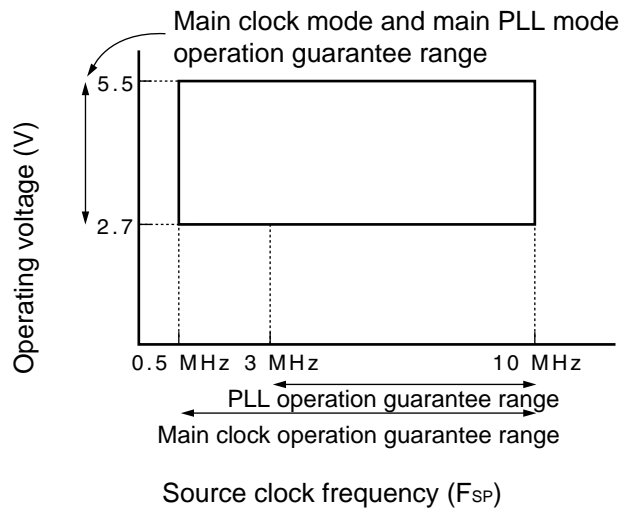
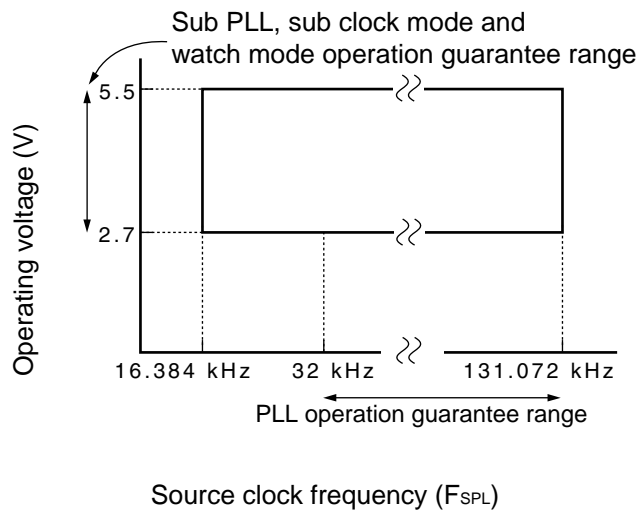




- **Operating voltage - Operating frequency ( $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )**
  - MB95F128H, MB95F128T

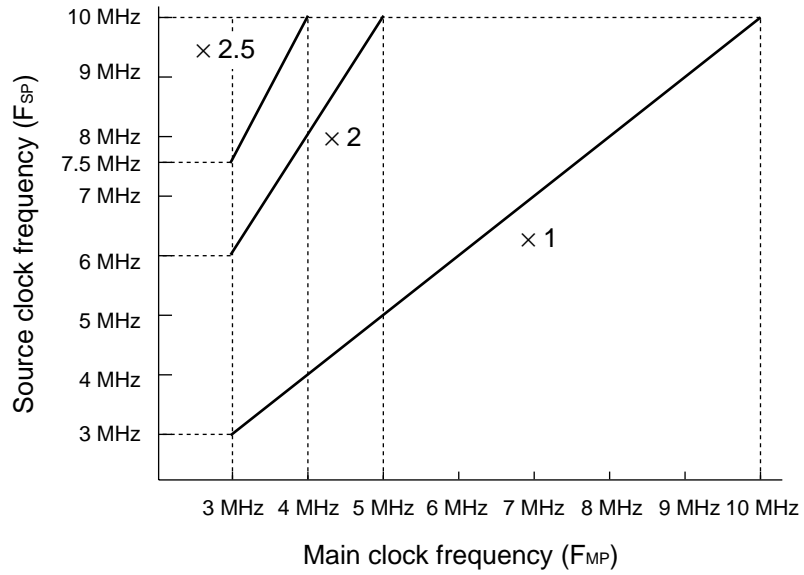


- **Operating voltage - Operating frequency ( $T_A = +5\text{ }^\circ\text{C}$  to  $+35\text{ }^\circ\text{C}$ )**
  - MB95FV100B-103



# MB95120H Series

- Main PLL operation frequency



## (3) External Reset

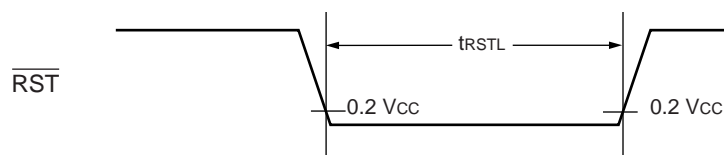
( $V_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $A_{V_{SS}} = V_{SS} = 0.0 \text{ V}$ ,  $T_A = -40 \text{ }^\circ\text{C}$  to  $+85 \text{ }^\circ\text{C}$ )

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
$\overline{\text{RST}}$ "L" level pulse width	$t_{\text{RSTL}}$	$2 t_{\text{MCLK}}^{*1}$	—	ns	At normal operating
		Oscillation time of oscillator <sup>*2</sup> + 100	—	$\mu\text{s}$	At stop mode, sub clock mode, sub sleep mode, and watch mode
		100	—		At timebase timer mode

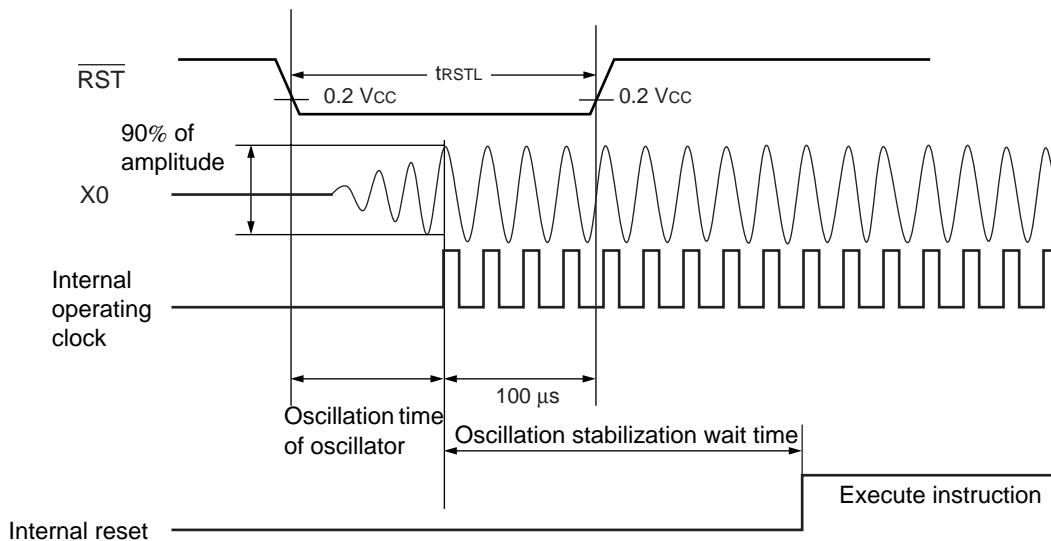
\*1 : Refer to "(2) Source Clock/Machine Clock" for  $t_{\text{MCLK}}$ .

\*2 : Oscillation start time of oscillator is the time that the amplitude reaches 90 %. In the crystal oscillator, the oscillation time is between several ms and tens of ms. In ceramic oscillators, the oscillation time is between hundreds of  $\mu\text{s}$  and several ms. In the external clock, the oscillation time is 0 ms.

- At normal operating



- At stop mode, sub clock mode, sub sleep mode, watch mode, and power-on

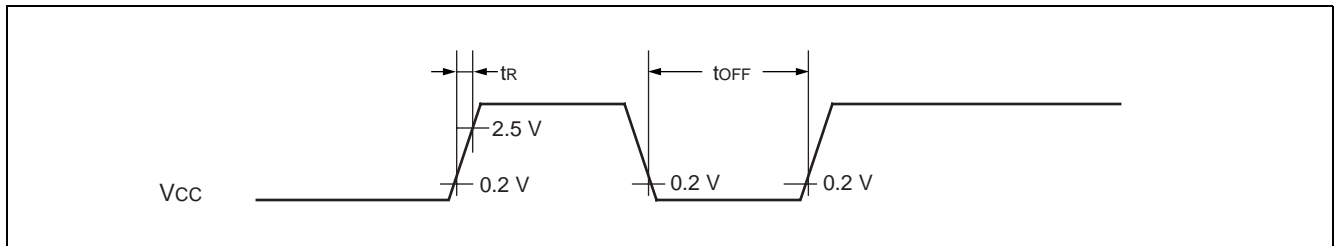


# MB95120H Series

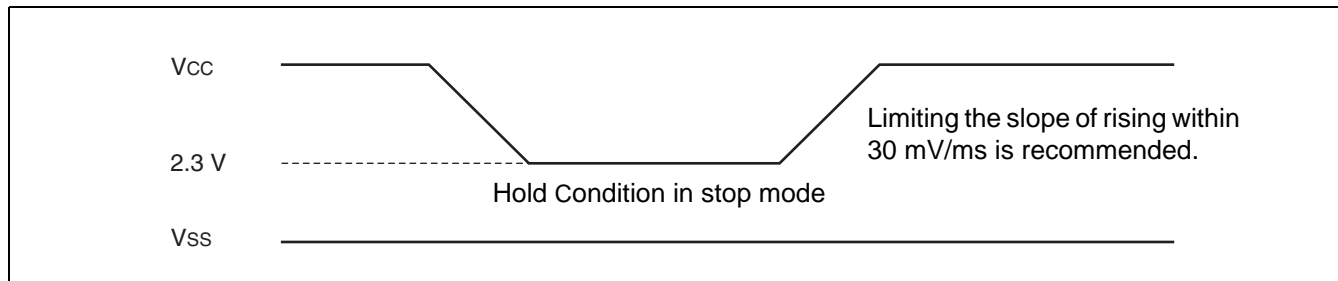
## (4) Power-on Reset

( $A_{V_{SS}} = V_{SS} = 0.0 \text{ V}$ ,  $T_A = -40 \text{ }^\circ\text{C}$  to  $+85 \text{ }^\circ\text{C}$ )

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Power supply rising time	$t_R$	—	—	50	ms	
Power supply cutoff time	$t_{OFF}$	—	1	—	ms	Waiting time until power-on



Note : Sudden change of power supply voltage may activate the power-on reset function. When changing power supply voltages during operation, set the slope of rising within 30 mV/ms as shown below.

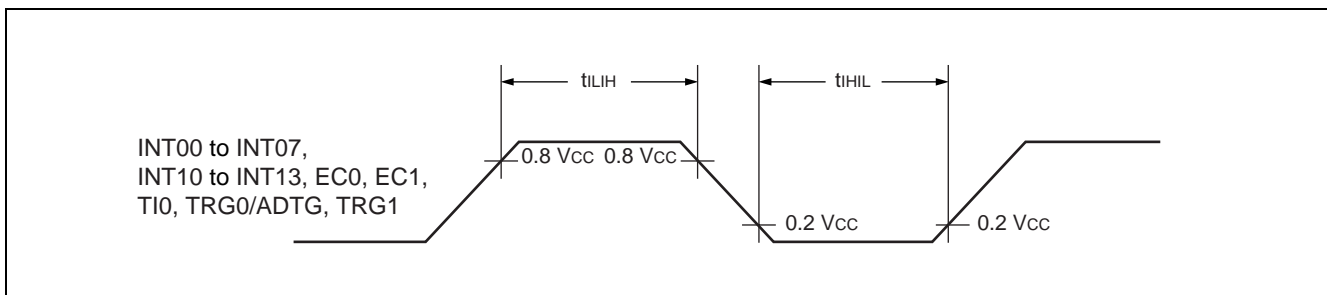


## (5) Peripheral Input Timing

( $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $A_{V_{SS}} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Peripheral input "H" pulse width	$t_{LIH}$	INT00 to INT07, INT10 to INT13,	$2 t_{MCLK}^*$	—	ns	
Peripheral input "L" pulse width	$t_{LIL}$	EC0, EC1, T10, TRG0/ADTG, TRG1	$2 t_{MCLK}^*$	—	ns	

\* : Refer to "(2) Source Clock/Machine Clock" for  $t_{MCLK}$ .



# MB95120H Series

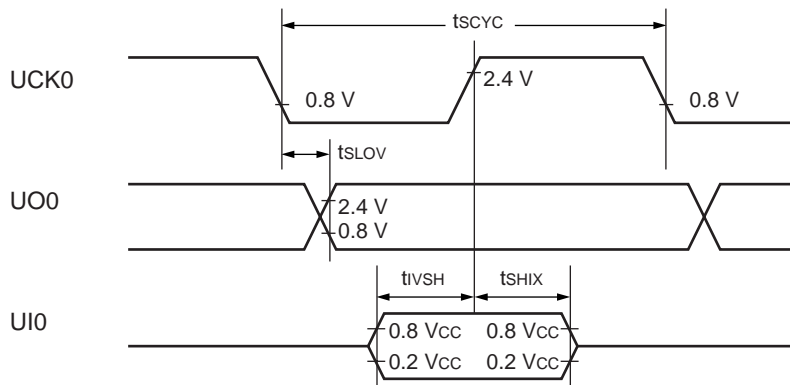
## (6) UART/SIO, Serial I/O Timing

( $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

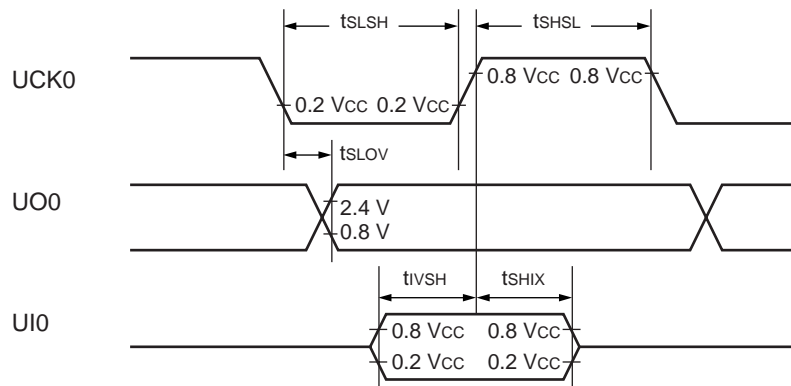
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	$t_{SCYC}$	UCK0	Internal clock operation output pin : $C_L = 80\text{ pF} + 1\text{ TTL}$ .	$4\ t_{MCLK}^*$	—	ns	
UCK ↓ → UO time	$t_{SLOV}$	UCK0, UO0		-190	+190	ns	
Valid UI → UCK ↑	$t_{VSH}$	UCK0, UI0		$2\ t_{MCLK}^*$	—	ns	
UCK ↑ → valid UI hold time	$t_{SHIX}$	UCK0, UI0		$2\ t_{MCLK}^*$	—	ns	
Serial clock "H" pulse width	$t_{SHSL}$	UCK0	External clock operation output pin : $C_L = 80\text{ pF} + 1\text{ TTL}$ .	$4\ t_{MCLK}^*$	—	ns	
Serial clock "L" pulse width	$t_{SLSH}$	UCK0		$4\ t_{MCLK}^*$	—	ns	
UCK ↓ → UO time	$t_{SLOV}$	UCK0, UO0		0	190	ns	
Valid UI → UCK ↑	$t_{VSH}$	UCK0, UI0		$2\ t_{MCLK}^*$	—	ns	
UCK ↑ → valid UI hold time	$t_{SHIX}$	UCK0, UI0	$2\ t_{MCLK}^*$	—	ns		

\* : Refer to "(2) Source Clock/Machine Clock" for  $t_{MCLK}$ .

### • Internal shift clock mode



### • External shift clock mode



## (7) LIN-UART Timing

Sampling at the rising edge of sampling clock\*1 and prohibited serial clock delay\*2

(ESCR register : SCES bit = 0, ECCR register : SCDE bit = 0)

( $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	$t_{SCYC}$	SCK	Internal clock operation output pin : $C_L = 80\text{ pF} + 1\text{ TTL}$ .	$5\ t_{MCLK}^{*3}$	—	ns
SCK ↓ → SOT delay time	$t_{SLOVI}$	SCK, SOT		-95	+95	ns
Valid SIN → SCK ↑	$t_{IVSHI}$	SCK, SIN		$t_{MCLK}^{*3} + 190$	—	ns
SCK ↑ → valid SIN hold time	$t_{SHIXI}$	SCK, SIN		0	—	ns
Serial clock "L" pulse width	$t_{SLSH}$	SCK	External clock operation output pin : $C_L = 80\text{ pF} + 1\text{ TTL}$ .	$3\ t_{MCLK}^{*3} - t_R$	—	ns
Serial clock "H" pulse width	$t_{SHSL}$	SCK		$t_{MCLK}^{*3} + 95$	—	ns
SCK ↓ → SOT delay time	$t_{SLOVE}$	SCK, SOT		—	$2\ t_{MCLK}^{*3} + 95$	ns
Valid SIN → SCK ↑	$t_{IVSHE}$	SCK, SIN		190	—	ns
SCK ↑ → valid SIN hold time	$t_{SHIXE}$	SCK, SIN		$t_{MCLK}^{*3} + 95$	—	ns
SCK fall time	$t_F$	SCK		—	10	ns
SCK rise time	$t_R$	SCK		—	10	ns

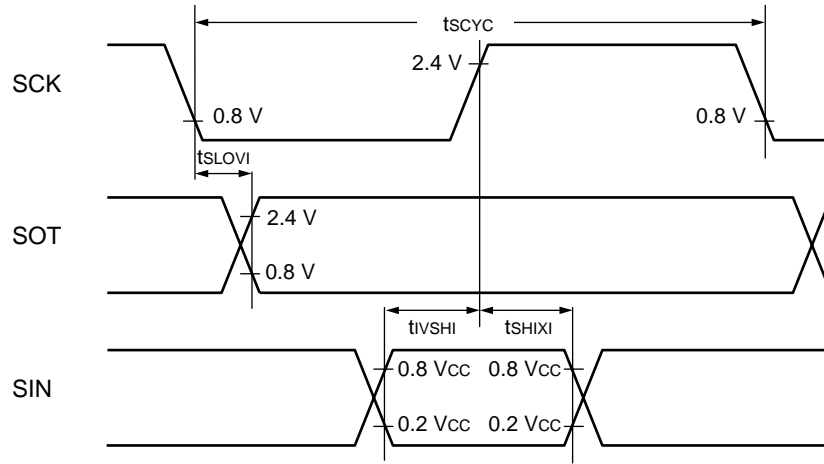
\*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

\*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

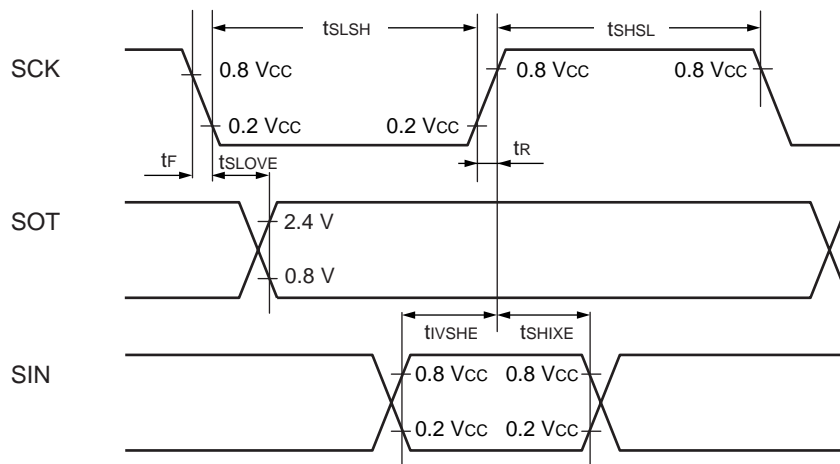
\*3 : Refer to "(2) Source Clock/Machine Clock" for  $t_{MCLK}$ .

# MB95120H Series

- Internal shift clock mode



- External shift clock mode





**Sampling at the falling edge of sampling clock\*1 and prohibited serial clock delay\*2  
(ESCR register : SCES bit = 1, ECCR register : SCDE bit = 0)**

( $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	$t_{SCYC}$	SCK	Internal clock operation output pin : $C_L = 80\text{ pF} + 1\text{ TTL}$ .	$5 t_{MCLK}^{*3}$	—	ns
SCK $\uparrow$ $\rightarrow$ SOT delay time	$t_{SHOVI}$	SCK, SOT		-95	+95	ns
Valid SIN $\rightarrow$ SCK $\downarrow$	$t_{IVSLI}$	SCK, SIN		$t_{MCLK}^{*3} + 190$	—	ns
SCK $\downarrow$ $\rightarrow$ valid SIN hold time	$t_{SLIXI}$	SCK, SIN		0	—	ns
Serial clock "H" pulse width	$t_{SHSL}$	SCK	External clock operation output pin : $C_L = 80\text{ pF} + 1\text{ TTL}$ .	$3 t_{MCLK}^{*3} - t_R$	—	ns
Serial clock "L" pulse width	$t_{SLSH}$	SCK		$t_{MCLK}^{*3} + 95$	—	ns
SCK $\uparrow$ $\rightarrow$ SOT delay time	$t_{SHOVE}$	SCK, SOT		—	$2 t_{MCLK}^{*3} + 95$	ns
Valid SIN $\rightarrow$ SCK $\downarrow$	$t_{IVSLE}$	SCK, SIN		190	—	ns
SCK $\downarrow$ $\rightarrow$ valid SIN hold time	$t_{SLIXE}$	SCK, SIN		$t_{MCLK}^{*3} + 95$	—	ns
SCK fall time	$t_F$	SCK		—	10	ns
SCK rise time	$t_R$	SCK		—	10	ns

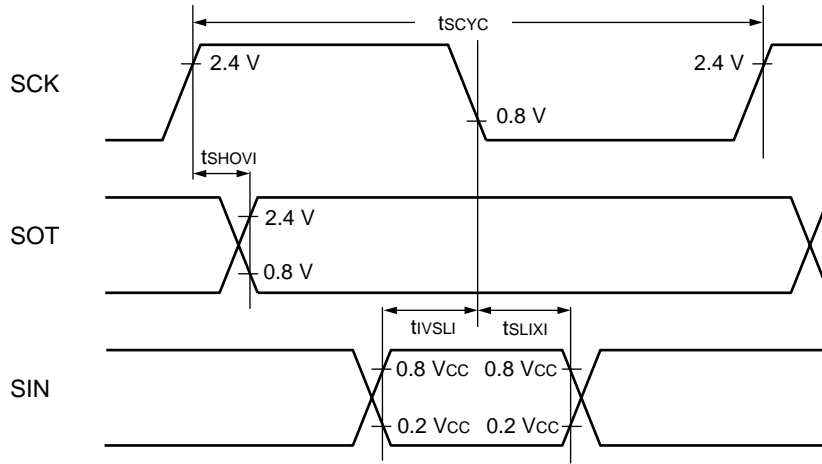
\*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

\*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

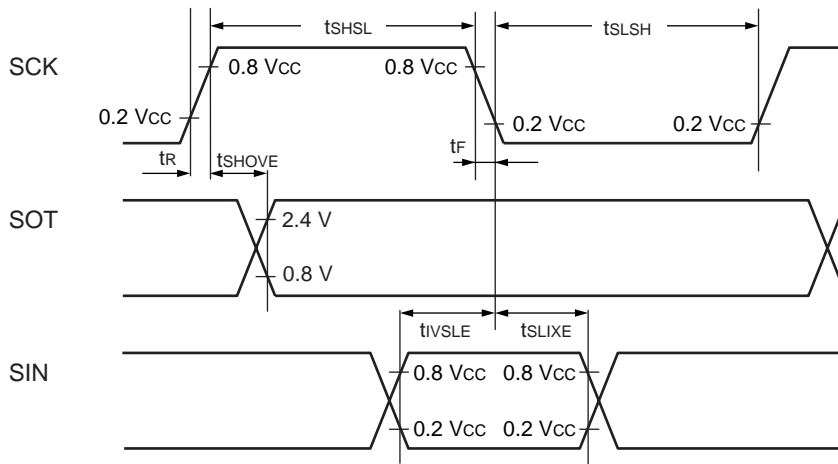
\*3 : Refer to " (2) Source Clock/Machine Clock" for  $t_{MCLK}$ .

# MB95120H Series

- Internal shift clock mode



- External shift clock mode



**Sampling at the rising edge of sampling clock\*<sup>1</sup> and enabled serial clock delay\*<sup>2</sup>**  
**(ESCR register : SCES bit = 0, ECCR register : SCDE bit = 1)**

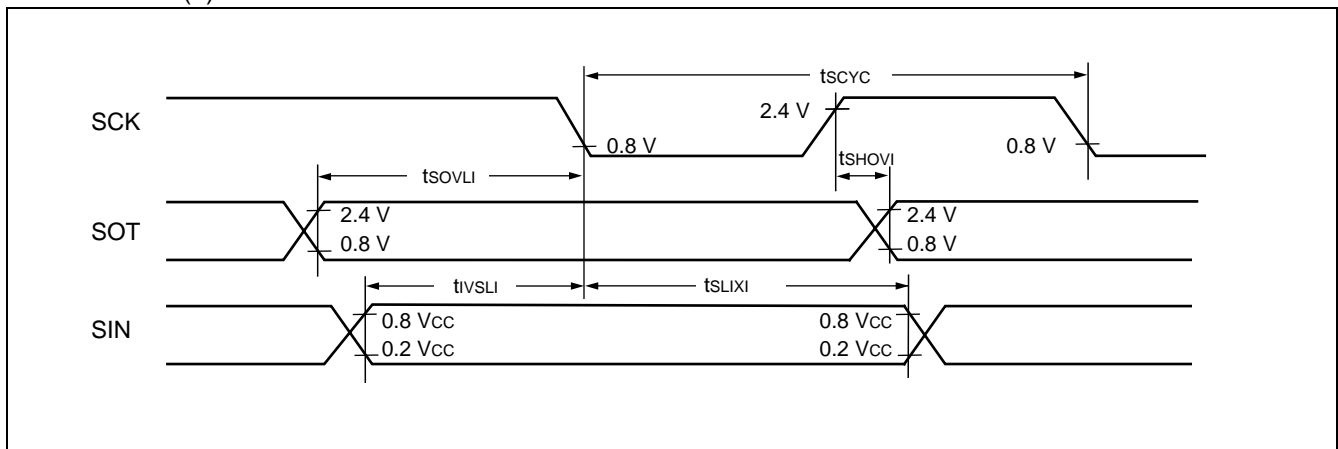
( $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	$t_{SCYC}$	SCK	Internal clock operation output pin : $C_L = 80\text{ pF} + 1\text{ TTL.}$	$5 t_{MCLK}^{*3}$	—	ns
SCK $\uparrow$ $\rightarrow$ SOT delay time	$t_{SHOVI}$	SCK, SOT		-95	+95	ns
Valid SIN $\rightarrow$ SCK $\downarrow$	$t_{IVSLI}$	SCK, SIN		$t_{MCLK}^{*3} + 190$	—	ns
SCK $\downarrow$ $\rightarrow$ valid SIN hold time	$t_{SLIXI}$	SCK, SIN		0	—	ns
SOT $\rightarrow$ SCK $\downarrow$ delay time	$t_{SOVLI}$	SCK, SOT		—	$4 t_{MCLK}^{*3}$	ns

\*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

\*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

\*3 : Refer to “ (2) Source Clock/Machine Clock” for  $t_{MCLK}$ .



# MB95120H Series

Sampling at the falling edge of sampling clock\*1 and enabled serial clock delay\*2  
 (ESCR register : SCES bit = 1, ECCR register : SCDE bit = 1)

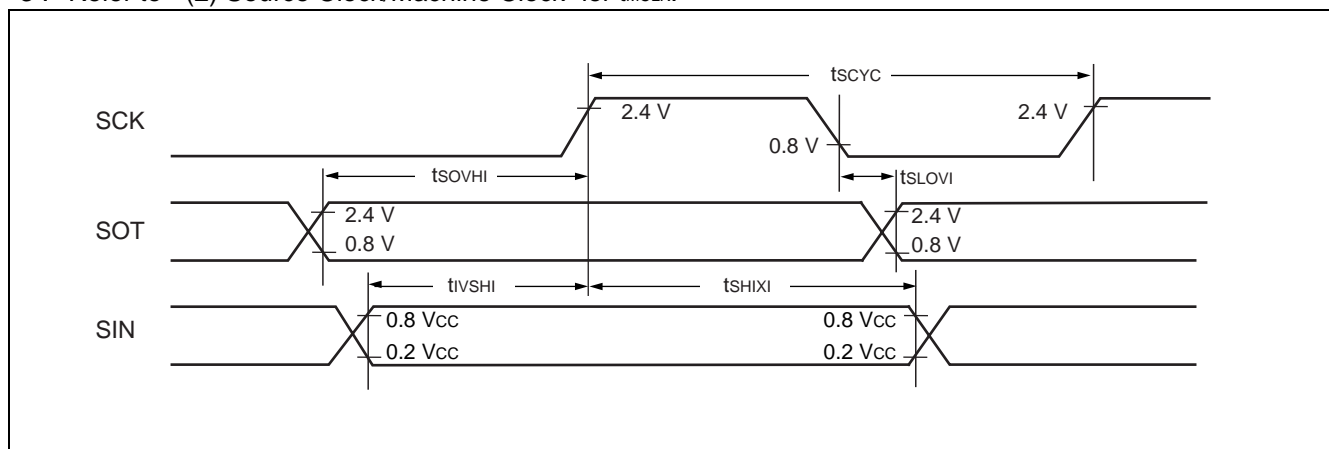
( $V_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $AV_{SS} = V_{SS} = 0.0 \text{ V}$ ,  $T_A = -40 \text{ }^\circ\text{C}$  to  $+85 \text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	$t_{SCYC}$	SCK	Internal clock operating output pin : $C_L = 80 \text{ pF} + 1 \text{ TTL.}$	$5 t_{MCLK}^{*3}$	—	ns
SCK $\downarrow \rightarrow$ SOT delay time	$t_{SLOVI}$	SCK, SOT		-95	+95	ns
Valid SIN $\rightarrow$ SCK $\uparrow$	$t_{IVSHI}$	SCK, SIN		$t_{MCLK}^{*3} + 190$	—	ns
SCK $\uparrow \rightarrow$ valid SIN hold time	$t_{SHIXI}$	SCK, SIN		0	—	ns
SOT $\rightarrow$ SCK $\uparrow$ delay time	$t_{SOVHI}$	SCK, SOT		—	$4 t_{MCLK}^{*3}$	ns

\*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

\*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

\*3 : Refer to “ (2) Source Clock/Machine Clock” for  $t_{MCLK}$ .



## (8) I<sup>2</sup>C Timing

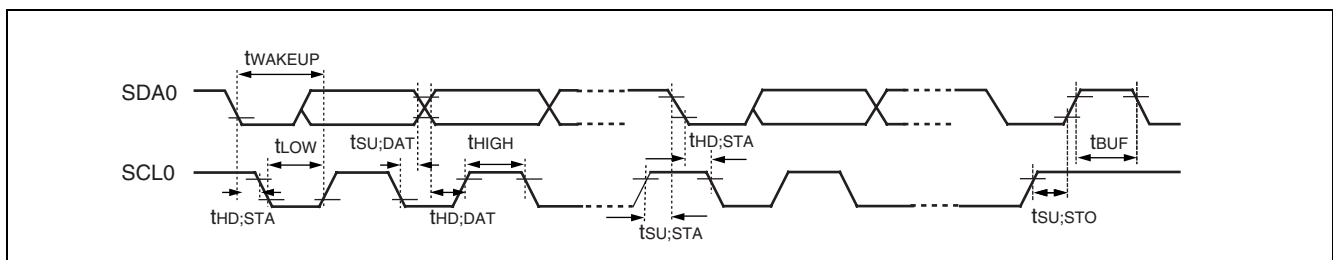
(V<sub>CC</sub> = 5.0 V ± 10%, AV<sub>SS</sub> = V<sub>SS</sub> = 0.0 V, T<sub>A</sub> = -40 °C to +85 °C)

Parameter	Sym- bol	Pin name	Conditions	Value				Unit	Re- marks
				Standard- mode		Fast-mode			
				Min	Max	Min	Max		
SCL clock frequency	f <sub>SCL</sub>	SCL0		0	100	0	400	kHz	
(Repeat) Start condition hold time SDA ↓ → SCL ↓	t <sub>HD;STA</sub>	SCL0 SDA0	R = 1.7 kΩ, C = 50 pF*1	4.0	—	0.6	—	μs	
SCL clock "L" width	t <sub>LOW</sub>	SCL0		4.7	—	1.3	—	μs	
SCL clock "H" width	t <sub>HIGH</sub>	SCL0		4.0	—	0.6	—	μs	
(Repeat) Start condition setup time SCL ↑ → SDA ↓	t <sub>SU;STA</sub>	SCL0 SDA0		4.7	—	0.6	—	μs	
Data hold time SCL ↓ → SDA ↓ ↑	t <sub>HD;DAT</sub>	SCL0 SDA0		0	3.45*2	0	0.9*3	μs	
Data setup time SDA ↓ ↑ → SCL ↑	t <sub>SU;DAT</sub>	SCL0 SDA0		0.25	—	0.1	—	μs	
Stop condition setup time SCL ↑ → SDA ↑	t <sub>SU;STO</sub>	SCL0 SDA0		4	—	0.6	—	μs	
Bus free time between stop condition and start condition	t <sub>BUF</sub>	SCL0 SDA0		4.7	—	1.3	—	μs	

\*1 : R, C : Pull-up resistor and load capacitor of the SCL and SDA lines.

\*2 : The maximum t<sub>HD;DAT</sub> have only to be met if the device dose not stretch the "L" width (t<sub>LOW</sub>) of the SCL signal.

\*3 : A fast-mode I<sup>2</sup>C-bus device can be used in a standard-mode I<sup>2</sup>C-bus system, but the requirement t<sub>SU;DAT</sub> ≥ 250 ns must then be met.



# MB95120H Series

( $V_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $AV_{SS} = V_{SS} = 0.0 \text{ V}$ ,  $T_A = -40 \text{ }^\circ\text{C}$  to  $+85 \text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Conditions	Value*2		Unit	Remarks
				Min	Max		
SCL clock "L" width	$t_{LOW}$	SCL0	R = 1.7 k $\Omega$ , C = 50 pF*1	$(2 + nm / 2) t_{MCLK} - 20$	—	ns	Master mode
SCL clock "H" width	$t_{HIGH}$	SCL0		$(nm / 2) t_{MCLK} - 20$	$(nm / 2) t_{MCLK} + 20$	ns	Master mode
Start condition hold time	$t_{HD,STA}$	SCL0 SDA0		$(-1 + nm / 2) t_{MCLK} - 20$	$(-1 + nm) t_{MCLK} + 20$	ns	Master mode Maximum value is applied when m, n = 1, 8. Otherwise, the minimum value is applied.
Stop condition setup time	$t_{SU,STO}$	SCL0 SDA0		$(1 + nm / 2) t_{MCLK} - 20$	$(1 + nm / 2) t_{MCLK} + 20$	ns	Master mode
Start condition setup time	$t_{SU,STA}$	SCL0 SDA0		$(1 + nm / 2) t_{MCLK} - 20$	$(1 + nm / 2) t_{MCLK} + 20$	ns	Master mode
Bus free time between stop condition and start condition	$t_{BUF}$	SCL0 SDA0		$(2 nm + 4) t_{MCLK} - 20$	—	ns	
Data hold time	$t_{HD,DAT}$	SCL0 SDA0		$3 t_{MCLK} - 20$	—	ns	Master mode
Data setup time	$t_{SU,DAT}$	SCL0 SDA0		$(-2 + nm / 2) t_{MCLK} - 20$	$(-1 + nm / 2) t_{MCLK} + 20$	ns	Master mode When assuming that "L" of SCL is not extended, the minimum value is applied to first bit of continuous data. Otherwise, the maximum value is applied.
Setup time between clearing interrupt and SCL rising	$t_{SU,INT}$	SCL0		$(nm / 2) t_{MCLK} - 20$	$(1 + nm / 2) t_{MCLK} + 20$	ns	Minimum value is applied to interrupt at 9th SCL $\downarrow$ . Maximum value is applied to interrupt at 8th SCL $\downarrow$ .
SCL clock "L" width	$t_{LOW}$	SCL0		$4 t_{MCLK} - 20$	—	ns	At reception
SCL clock "H" width	$t_{HIGH}$	SCL0		$4 t_{MCLK} - 20$	—	ns	At reception
Start condition detection	$t_{HD,STA}$	SCL0 SDA0		$2 t_{MCLK} - 20$	—	ns	Undetected when 1 $t_{MCLK}$ is used at reception

(Continued)

(Continued)

( $V_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $AV_{SS} = V_{SS} = 0.0 \text{ V}$ ,  $T_A = -40 \text{ }^\circ\text{C}$  to  $+85 \text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Conditions	Value*2		Unit	Remarks
				Min	Max		
Stop condition detection	$t_{SU;STO}$	SCL0 SDA0	R = 1.7 k $\Omega$ , C = 50 pF*1	$2 t_{MCLK} - 20$	—	ns	Undetected when 1 $t_{MCLK}$ is used at reception
Restart condition detection condition	$t_{SU;STA}$	SCL0 SDA0		$2 t_{MCLK} - 20$	—	ns	Undetected when 1 $t_{MCLK}$ is used at reception
Bus free time	$t_{BUF}$	SCL0 SDA0		$2 t_{MCLK} - 20$	—	ns	At reception
Data hold time	$t_{HD;DAT}$	SCL0 SDA0		$2 t_{MCLK} - 20$	—	ns	At slave transmission mode
Data setup time	$t_{SU;DAT}$	SCL0 SDA0		$t_{LOW} - 3 t_{MCLK} - 20$	—	ns	At slave transmission mode
Data hold time	$t_{HD;DAT}$	SCL0 SDA0		0	—	ns	At reception
Data setup time	$t_{SU;DAT}$	SCL0 SDA0		$t_{MCLK} - 20$	—	ns	At reception
SDA $\downarrow$ →SCL $\uparrow$ (at wakeup function)	$t_{WAKE-UP}$	SCL0 SDA0		Oscillation stabilization wait time + $2 t_{MCLK} - 20$	—	ns	

\*1 : R, C : Pull-up resistor and load capacitor of the SCL and SDA lines.

\*2 : • Refer to “(2) Source Clock/Machine Clock” for  $t_{MCLK}$ .

- m is CS4 bit and CS3 bit (bit 4 and bit 3) of I<sup>2</sup>C clock control register (ICCR) .
- n is CS2 bit to CS0 bit (bit 2 to bit 0) of I<sup>2</sup>C clock control register (ICCR) .
- Actual timing of I<sup>2</sup>C is determined by m and n values set by the machine clock ( $t_{MCLK}$ ) and CS4 to CS0 of ICCR0 register.
- Standard-mode :  
m and n can be set at the range :  $0.9 \text{ MHz} < t_{MCLK} \text{ (machine clock)} < 10 \text{ MHz}$ .  
Setting of m and n determines the machine clock that can be used below.
 

(m, n) = (1, 8)	: $0.9 \text{ MHz} < t_{MCLK} \leq 1 \text{ MHz}$
(m, n) = (1, 22), (5, 4), (6, 4), (7, 4), (8, 4)	: $0.9 \text{ MHz} < t_{MCLK} \leq 2 \text{ MHz}$
(m, n) = (1, 38), (5, 8), (6, 8), (7, 8), (8, 8)	: $0.9 \text{ MHz} < t_{MCLK} \leq 4 \text{ MHz}$
(m, n) = (1, 98)	: $0.9 \text{ MHz} < t_{MCLK} \leq 10 \text{ MHz}$
- Fast-mode :  
m and n can be set at the range :  $3.3 \text{ MHz} < t_{MCLK} \text{ (machine clock)} < 10 \text{ MHz}$ .  
Setting of m and n determines the machine clock that can be used below.
 

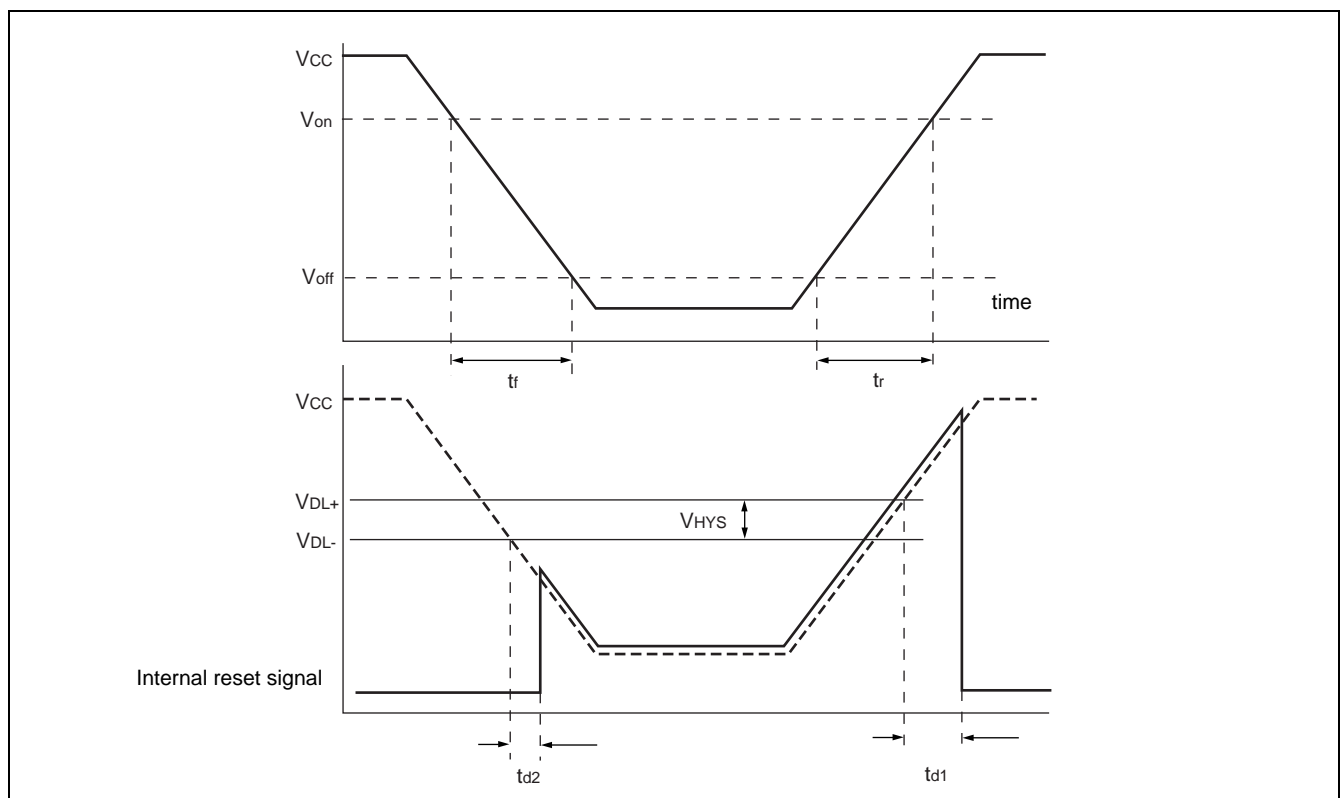
(m, n) = (1, 8)	: $3.3 \text{ MHz} < t_{MCLK} \leq 4 \text{ MHz}$
(m, n) = (1, 22), (5, 4)	: $3.3 \text{ MHz} < t_{MCLK} \leq 8 \text{ MHz}$
(m, n) = (6, 4)	: $3.3 \text{ MHz} < t_{MCLK} \leq 10 \text{ MHz}$

# MB95120H Series

## (9) Low Voltage Detection

(AVSS = VSS = 0.0 V, TA = -40 °C to +85 °C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Release voltage	V <sub>DL+</sub>	2.55	2.70	2.85	V	At power-supply rise
Detection voltage	V <sub>DL-</sub>	2.45	2.60	2.75	V	At power-supply fall
Hysteresis width	V <sub>HYS</sub>	70	100	—	mV	
Power-supply start voltage	V <sub>off</sub>	—	—	2.3	V	
Power-supply end voltage	V <sub>on</sub>	4.9	—	—	V	
Power-supply voltage change time (at power supply rise)	t <sub>r</sub>	0.3	—	—	μs	Slope of power supply that reset release signal generates
		—	3000	—	μs	Slope of power supply that reset release signal generates within rating (V <sub>DL+</sub> )
Power-supply voltage change time (at power supply fall)	t <sub>f</sub>	300	—	—	μs	Slope of power supply that reset detection signal generates
		—	300	—	μs	Slope of power supply that reset detection signal generates within rating (V <sub>DL-</sub> )
Reset release delay time	t <sub>d1</sub>	—	—	400	μs	
Reset detection delay time	t <sub>d2</sub>	—	—	30	μs	
Current consumption	I <sub>LVD</sub>	—	38	50	μA	Current consumption of low voltage detection circuit only





## 5. A/D Converter

### (1) A/D Converter Electrical Characteristics

(AVcc = Vcc = 4.0 V to 5.5 V, AVss = Vss = 0.0 V, TA = -40 °C to +85 °C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	10	bit	
Total error		-3.0	—	+3.0	LSB	
Linearity error		-2.5	—	+2.5	LSB	
Differential linear error		-1.9	—	+1.9	LSB	
Zero transition voltage	V <sub>0T</sub>	AVss - 1.5 LSB	AVss + 0.5 LSB	AVss + 2.5 LSB	V	
Full-scale transition voltage	V <sub>FST</sub>	AVR - 3.5 LSB	AVR - 1.5 LSB	AVR + 0.5 LSB	V	
Compare time	—	0.9	—	16500	μs	4.5 V ≤ AVcc ≤ 5.5 V
		1.8	—	16500	μs	4.0 V ≤ AVcc < 4.5 V
Sampling time	—	0.6	—	∞	μs	4.5 V ≤ AVcc ≤ 5.5 V, At external impedance < 5.4 kΩ
		1.2	—	∞	μs	4.0 V ≤ AVcc < 4.5 V, At external impedance < 2.4 kΩ
Analog input current	I <sub>AIN</sub>	-0.3	—	+0.3	μA	
Analog input voltage	V <sub>AIN</sub>	AVss	—	AVR	V	
Reference voltage	—	AVss + 4.0	—	AVcc	V	AVR pin
Reference voltage supply current	I <sub>R</sub>	—	600	900	μA	AVR pin, During A/D operation
	I <sub>RH</sub>	—	—	5	μA	AVR pin, At stop mode

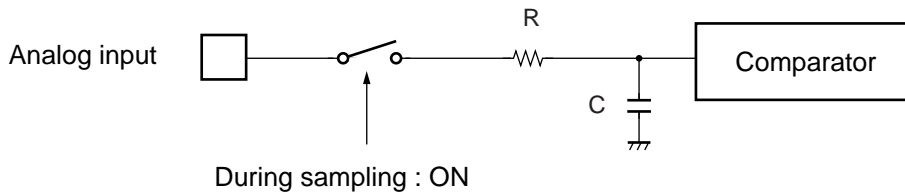
# MB95120H Series

## (2) Notes on Using A/D Converter

### • About the external impedance of analog input and its sampling time

A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision. Therefore to satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. Also, if the sampling time cannot be sufficient, connect a capacitor of about 0.1  $\mu\text{F}$  to the analog input pin.

#### • Analog input equivalent circuit

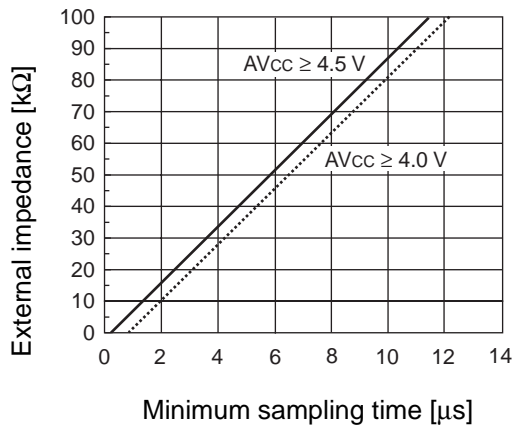


	R	C
$4.5 \text{ V} \leq AV_{CC} \leq 5.5 \text{ V}$	2.0 k $\Omega$ (Max)	16 pF (Max)
$4.0 \text{ V} \leq AV_{CC} < 4.5 \text{ V}$	8.2 k $\Omega$ (Max)	16 pF (Max)

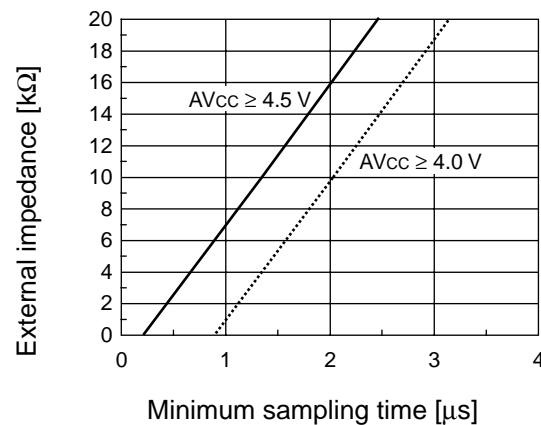
Note : The values are reference values.

#### • The relationship between external impedance and minimum sampling time

(External impedance = 0 k $\Omega$  to 100 k $\Omega$ )



(External impedance = 0 k $\Omega$  to 20 k $\Omega$ )



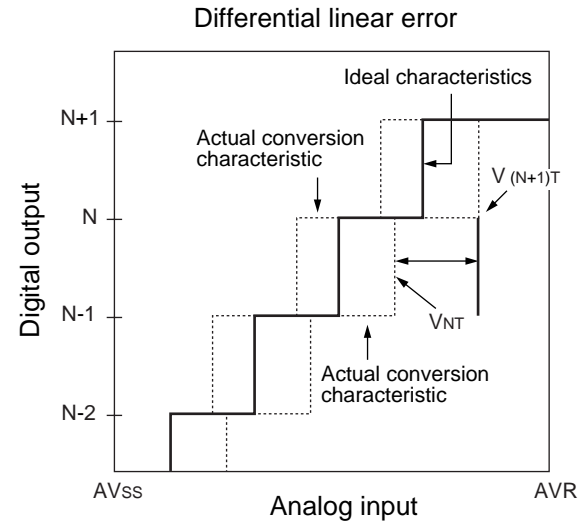
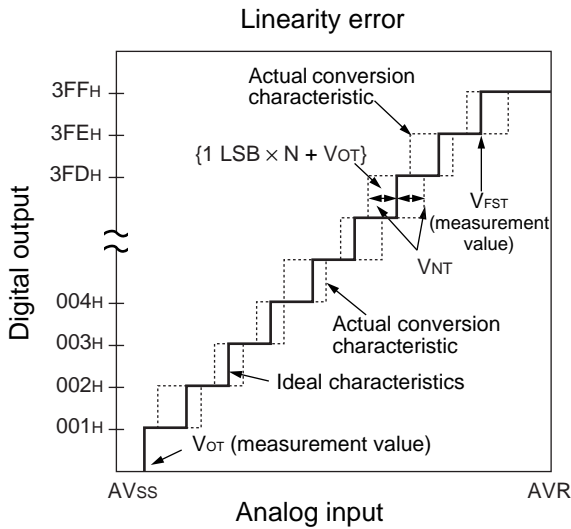
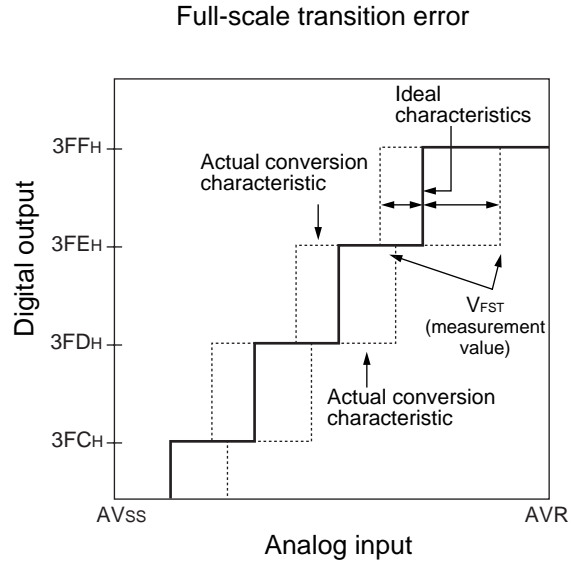
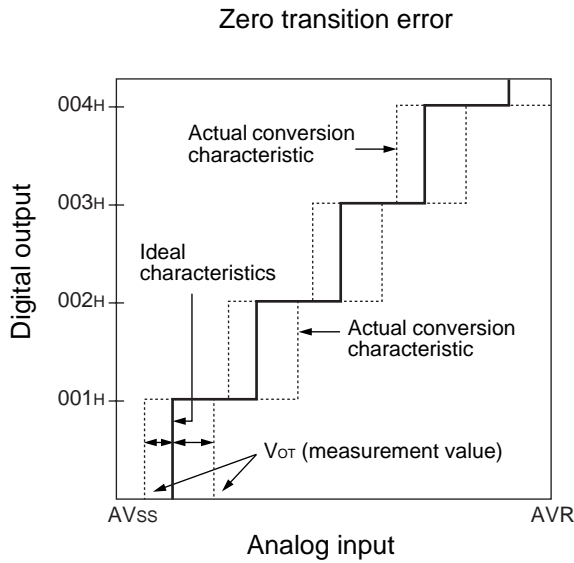
### • About errors

As  $|AV_{CC} - AV_{SS}|$  becomes smaller, values of relative errors grow larger.



# MB95120H Series

(Continued)



$$\text{Linear error in digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times N + V_{OT}\}}{1 \text{ LSB}}$$

$$\text{Differential linear error in digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} - 1$$

N : A/D Converter digital output value

$V_{NT}$  : A voltage at which digital output transits from (N - 1) to N.

$V_{OT}$  (Ideal value) =  $AV_{SS} + 0.5 \text{ LSB [V]}$

$V_{FST}$  (Ideal value) =  $AVR - 1.5 \text{ LSB [V]}$

## 6. Flash Memory Program/Erase Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time (4K bytes sector)	—	0.2*1	0.5*2	s	Excludes 00H programming prior erasure.
Sector erase time (16K bytes sector)	—	0.5*1	7.5*2	s	Excludes 00H programming prior erasure.
Byte programming time	—	32	3600	μs	Excludes system-level overhead.
Program/erase cycle	10000	—	—	cycle	
Power supply voltage at program/erase	4.5	—	5.5	V	
Flash memory data retention time	20*3	—	—	year	Average T <sub>A</sub> = +85 °C

\*1 : T<sub>A</sub> = + 25 °C, V<sub>CC</sub> = 5.0 V, 10000 cycles

\*2 : T<sub>A</sub> = + 85 °C, V<sub>CC</sub> = 4.5 V, 10000 cycles

\*3 : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at +85 °C) .

# MB95120H Series

## ■ MASK OPTION

No.	Part number	MB95F128H MB95F128T	MB95FV100B-103
	Specifying procedure	Setting disabled	Setting disabled
1	Clock mode select • Single-system clock mode • Dual-system clock mode	Dual-system clock mode	Changing by the switch on MCU board
2	Low voltage detection reset* • With low voltage detection reset • Without low voltage detection reset	Specified by part number	Changing by the switch on MCU board
3	Oscillation stabilization wait time	Fixed to oscillation stabilization wait time of $(2^{14}-2) / F_{CH}$	Fixed to oscillation stabilization wait time of $(2^{14}-2) / F_{CH}$

\* : Refer to table below about clock mode select, low voltage detection reset, and reset output.

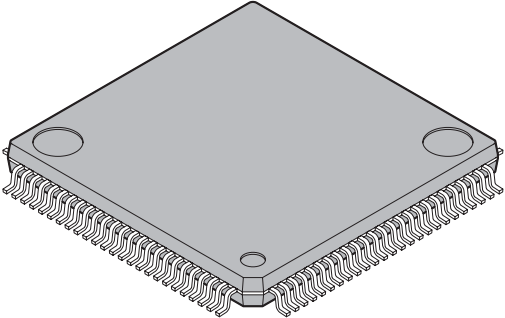
Part number	Clock mode select	Low voltage detection reset	Reset output
MB95F128H	Dual-system	No	Yes
MB95F128T		Yes	Yes
MB95FV100B-103	Single-system	No	Yes
		Yes	Yes
	Dual-system	No	Yes
		Yes	Yes

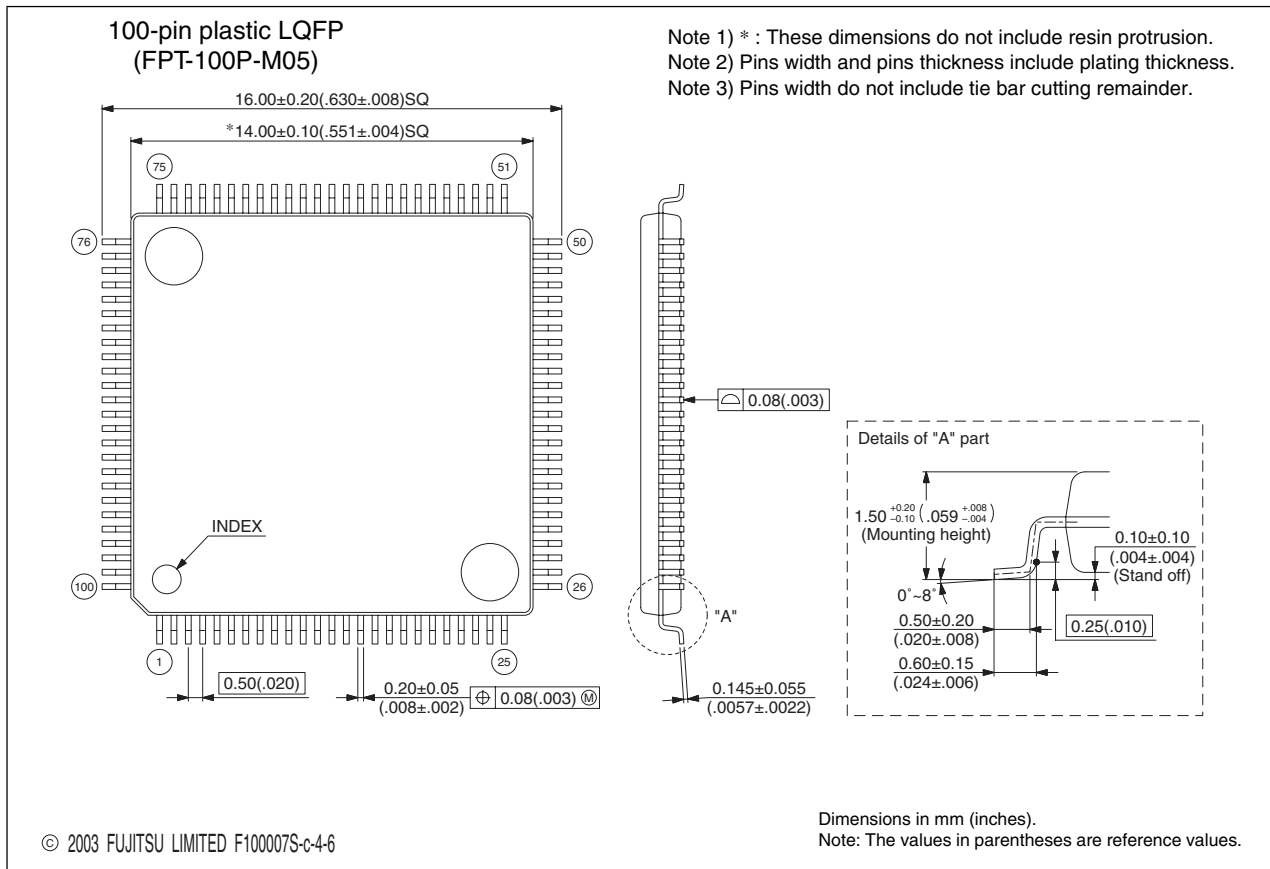
## ■ ORDERING INFORMATION

Part number	Package	Remarks
MB95F128HPFV MB95F128TPFV	100-pin plastic LQFP (FPT-100P-M05)	
MB95F128HPF MB95F128TPF	100-pin plastic QFP (FPT-100P-M06)	
MB2146-303 (MB95FV100B-103PBT)	MCU board ( 224-pin plastic PFBGA ) (BGA-224P-M08)	

# MB95120H Series

## PACKAGE DIMENSIONS

<p>100-pin plastic LQFP</p>  <p>(FPT-100P-M05)</p>	Lead pitch	0.50 mm
	Package width × package length	14.0 × 14.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.65g
	Code (Reference)	P-LFQFP100-14×14-0.50

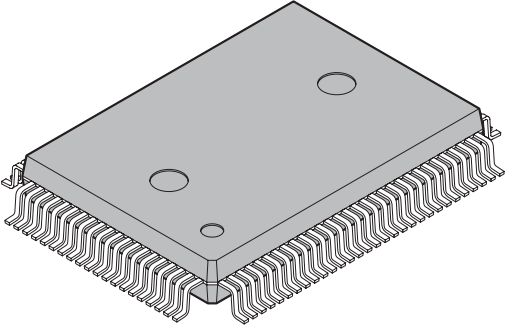


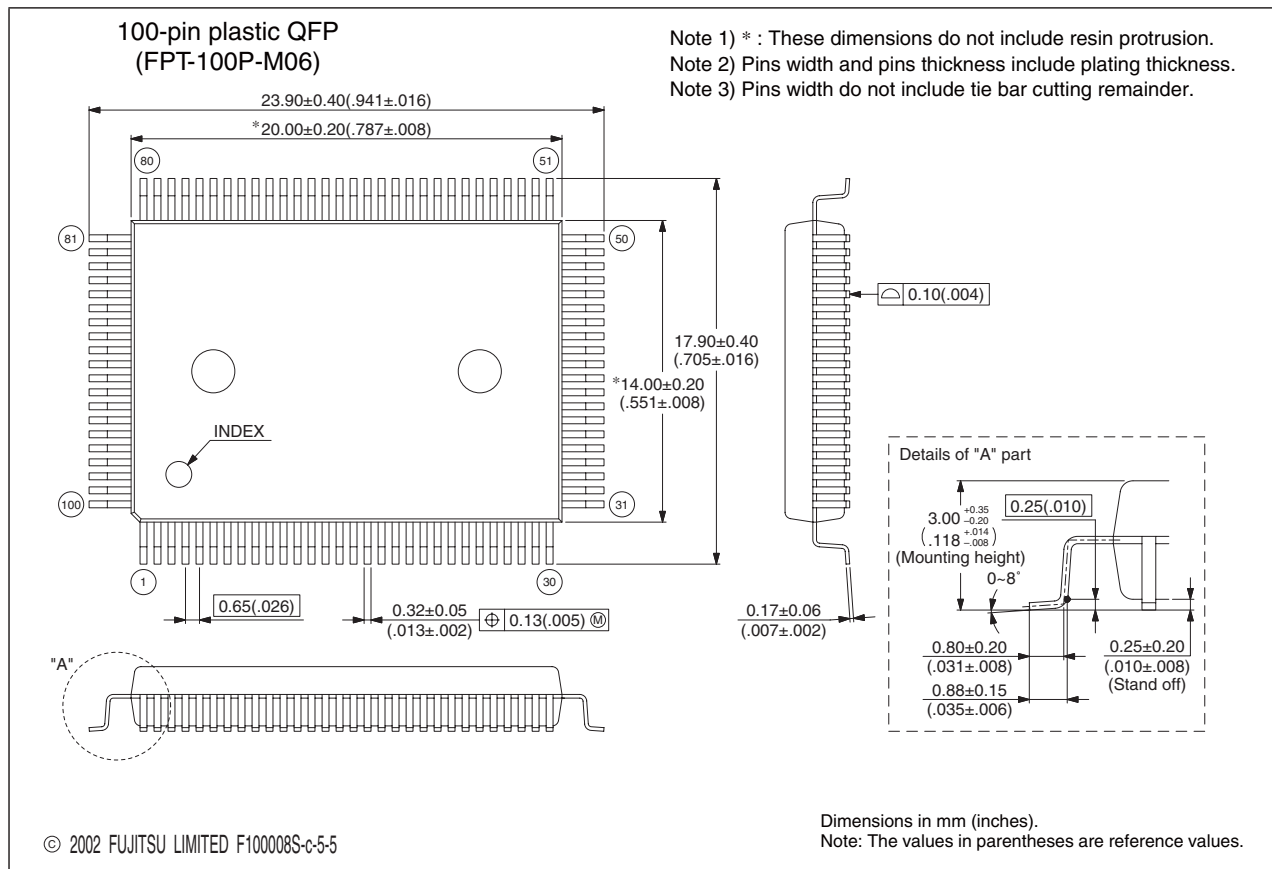
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# MB95120H Series

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<p style="text-align: center;">100-pin plastic QFP</p>  <p style="text-align: center;">(FPT-100P-M06)</p>	Lead pitch	0.65 mm
	Package width × package length	14.00 × 20.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	3.35 mm MAX
	Code (Reference)	P-QFP100-14×20-0.65



# MB95120H Series

The information for microcontroller supports is shown in the following homepage.  
<http://www.fujitsu.com/global/services/microelectronics/product/micom/support/index.html>

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