FUJITSU MICROELECTRONICS
DATA SHEET

DS07-12614-2Ea

8-bit Proprietary Microcontrollers

CMOS

F²MC-8FX MB95100AM Series

MB95108AM/F104AMS/F104ANS/F104AJS/F106AMS/F106ANS/F106AJS/ MB95F108AMS/F108ANS/F108AJS/F104AMW/F104ANW/F104AJW/F106AMW/ MB95F106ANW/F106AJW/F108AMW/F108ANW/F108AJW/FV100D-103

■ DESCRIPTION

The MB95100AM series is general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers contain a variety of peripheral functions.

Note : F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

■ FEATURE

- F²MC-8FX CPU core
  Instruction set optimized for controllers
  - Multiplication and division instructions
  - 16-bit arithmetic operations
  - Bit test branch instruction
  - Bit manipulation instructions etc.
- Clock
  - Main clock
  - Main PLL clock
  - Sub clock (for dual clock product)
  - Sub PLL clock (for dual clock product)

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Be sure to refer to the “Check Sheet” for the latest cautions on development.

“Check Sheet” is seen at the following support page
URL : http://edevice.fujitsu.com/micom/en-support/

“Check Sheet” lists the minimal requirement items to be checked to prevent problems beforehand in system development.

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- Timer
  - 8/16-bit compound timer × 2 channels
  - 16-bit reload timer
  - 8/16-bit PPG × 2 channels
  - 16-bit PPG × 2 channels
  - Timebase timer
  - Watch prescaler (for dual clock product)
- LIN-UART
  - Full duplex double buffer
  - Clock asynchronous (UART) or clock synchronous (SIO) serial data transfer capable
- UART/SIO
  - Full duplex double buffer
  - Clock asynchronous (UART) or clock synchronous (SIO) serial data transfer capable
- I^2C*
  Built-in wake-up function
- External interrupt
  - Interrupt by edge detection (rising, falling, or both edges can be selected)
  - Can be used to recover from low-power consumption (standby) modes.
- 8/10-bit A/D converter
  - 8-bit or 10-bit resolution can be selected
- Low-power consumption (standby) mode
  - Stop mode
  - Sleep mode
  - Watch mode (for dual clock product)
  - Timebase timer mode
- I/O ports :
  - The number of maximum ports
    - Single clock product : 54 ports
    - Dual clock product : 52 ports
  - Port configuration
    - General-purpose I/O ports (N-ch open drain) : 6 ports
    - General-purpose I/O ports (CMOS) : Single clock product : 48 ports
      Dual clock product : 46 ports
- Programmable input voltage levels of port
  Automotive input level / CMOS input level / hysteresis input level
- Flash memory security function
  Protects the content of Flash memory (Flash memory device only)

* : Purchase of Fujitsu I^2C components conveys a license under the Philips I^2C Patent Rights to use, these components in an I^2C system provided that the system conforms to the I^2C Standard Specification as defined by Philips.

■ MEMORY LINEUP

	Flash	RAM
MB95F104AMS/F104ANS/F104AJS	16K bytes	512 bytes
MB95F104AMW/F104ANW/F104AJW		
MB95F106AMS/F106ANS/F106AJS	32K bytes	1K byte
MB95F106AMW/F106ANW/F106AJW		
MB95F108AMS/F108ANS/F108AJS	60K bytes	2K bytes
MB95F108AMW/F108ANW/F108AJW		

■ PRODUCT LINEUP

Parameter \ Part number		MB95 108AM	MB95F 104AMS/ MB95F 106AMS/ MB95F 108AMS	MB95F 104ANS/ MB95F 106ANS/ MB95F 108ANS	MB95F 104AMW/ MB95F 106AMW/ MB95F 108AMW	MB95F 104ANW/ MB95F 106ANW/ MB95F 108ANW	MB95F 104AJS/ MB95F 106AJS/ MB95F 108AJS	MB95F 104AJW/ MB95F 106AJW/ MB95F 108AJW
Type		MASK ROM product	Flash memory product					
ROM capacity*1		60 Kbytes (Max)						
RAM capacity*1		2 Kbytes (Max)						
Reset output		Yes					No	
Option*2	Clock system	Selectable single/dual clock*3	Single clock		Dual clock		Single clock	Dual clock
	Low voltage detection reset	Yes/No	No	Yes	No	Yes		
	Clock supervisor	No					Yes	
CPU functions		Number of basic instructions : 136 Instruction bit length : 8 bits Instruction length : 1 to 3 bytes Data bit length : 1, 8, and 16 bits Minimum instruction execution time : 61.5 ns (at machine clock frequency 16.25 MHz) Interrupt processing time : 0.6 µs (at machine clock frequency 16.25 MHz)						
Peripheral functions	General-purpose I/O ports	• Single clock product : 54 ports (N-ch open drain : 6 ports, CMOS : 48 ports) • Dual clock product : 52 ports (N-ch open drain : 6 ports, CMOS : 46 ports) Programmable input voltage levels of port : Automotive input level / CMOS input level / hysteresis input level						
	Timebase timer	Interrupt cycle : 0.5 ms, 2.1 ms, 8.2 ms, 32.8 ms (at main oscillation clock 4 MHz)						
	Watchdog timer	Reset generated cycle At main oscillation clock 10 MHz : Min 105 ms At sub oscillation clock 32.768 kHz (for dual clock product) : Min 250 ms						
	Wild register	Capable of replacing 3 bytes of ROM data						
	I²C	Master/slave sending and receiving Bus error function and arbitration function Detecting transmitting direction function Start condition repeated generation and detection functions Built-in wake-up function						
	UART/SIO	Data transfer capable in UART/SIO Full duplex double buffer, variable data length (5/6/7/8-bit), built-in baud rate generator NRZ type transfer format, error detected function LSB-first or MSB-first can be selected. Clock asynchronous (UART) or clock synchronous (SIO) serial data transfer capable						

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Parameter \ Part number		MB95 108AM	MB95F 104AMS/ MB95F 106AMS/ MB95F 108AMS	MB95F 104ANS/ MB95F 106ANS/ MB95F 108ANS	MB95F 104AMW/ MB95F 106AMW/ MB95F 108AMW	MB95F 104ANW/ MB95F 106ANW/ MB95F 108ANW	MB95F 104AJS/ MB95F 106AJS/ MB95F 108AJS	MB95F 104AJW/ MB95F 106AJW/ MB95F 108AJW
Peripheral functions	LIN-UART	Dedicated reload timer allowing a wide range of communication speeds to be set. Full duplex double buffer Clock asynchronous (UART) or clock synchronous (SIO) serial data transfer capable LIN functions available as the LIN master or LIN slave.						
	8/10-bit A/D converter (12 channels)	8-bit or 10-bit resolution can be selected.						
	16-bit reload timer	Two clock modes and two counter operating modes can be selected. Square waveform output Count clock : 7 internal clocks and external clock can be selected. Counter operating mode : reload mode or one-shot mode can be selected.						
	8/16-bit compound timer (2 channels)	Each channel of the timer can be used as “8-bit timer × 2 channels” or “16-bit timer × 1 channel”. Built-in timer function, PWC function, PWM function, capture function, and square waveform output Count clock : 7 internal clocks and external clock can be selected						
	16-bit PPG (2 channels)	PWM mode or one-shot mode can be selected. Counter operating clock : 8 selectable clock sources Support for external trigger start						
	8/16-bit PPG (2 channels)	Each channel of the PPG can be used as “8-bit PPG × 2 channels” or “16-bit PPG × 1 channel”. Counter operating clock : Eight selectable clock sources						
	Watch counter (for dual clock product)	Count clock : 4 selectable clock sources (125 ms, 250 ms, 500 ms, or 1 s) Counter value can be set from 0 to 63. (Capable of counting for 1 minute when selecting clock source 1 second and setting counter value to 60)						
	Watch prescaler (for dual clock product)	4 selectable interval times (125 ms, 250 ms, 500 ms, or 1 s)						
	External interrupt (12 channels)	Interrupt by edge detection (rising, falling, or both edges can be selected.) Can be used to recover from standby modes.						
	Flash memory	Supports automatic programming, Embedded Algorithm™ *4 Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Number of write/erase cycles (Minimum) : 10000 times Data retention time : 20 years Erase can be performed on each block Block protection with external programming voltage Flash Security Feature for protecting the content of the Flash (MB95F108AMS/F108ANS/F108AJS/F108AMW/F108ANW/F108AJW only)						
Standby mode		Sleep, stop, watch (for dual clock product) , and timebase timer						

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*1 : For ROM capacity and RAM capacity, refer to “■ MEMORY LINEUP”.

*2 : For details of option, refer to “■ MASK OPTION”.

*3 : Specify clock mode when ordering MASK ROM.

*4 : Embedded Algorithm is a trade mark of Advanced Micro Devices Inc.

Note : Part number of the evaluation product in MB95100AM series is MB95FV100D-103. When using it, the MCU board (MB2146-303A) is required.

■ OSCILLATION STABILIZATION WAIT TIME

The initial value of the main clock oscillation stabilization wait time is fixed to the maximum value. The maximum value is shown as follows.

Oscillation stabilization wait time	Remarks
$(2^{14}-2) / F_{CH}$	Approx. 4.10 ms (at main oscillation clock 4 MHz)

■ PACKAGES AND CORRESPONDING PRODUCTS

Part number / Parameter	MB95108AM	MB95F104AMS/F104ANS/ F104AJS MB95F106AMS/F106ANS/ F106AJS MB95F108AMS/F108ANS/ F108AJS	MB95F104AMW/F104ANW/ F104AJW MB95F106AMW/F106ANW/ F106AJW MB95F108AMW/F108ANW/ F108AJW	MB95FV100D-103
FPT-64P-M03	○	○	○	×
FPT-64P-M09	○	○	○	×
BGA-224P-M08	×	×	×	○

○ : Available
× : Unavailable

■ DIFFERENCES AMONG PRODUCTS AND NOTES ON SELECTING PRODUCTS

• Notes on Using Evaluation Products

The Evaluation product has not only the functions of the MB95100AM series but also those of other products to support software development for multiple series and models of the F²MC-8FX family. The I/O addresses for peripheral resources not used by the MB95100AM series are therefore access-barred. Read/write access to these access-barred addresses may cause peripheral resources supposed to be unused to operate, resulting in unexpected malfunctions of hardware or software.

Particularly, do not use word access to odd numbered byte address in the prohibited areas (If these access are used, the address may be read or write unexpectedly) .

Also, as the read values of prohibited addresses on the evaluation product are different to the values on the flash memory and MASK ROM products, do not use these values in the program.

The Evaluation product do not support the functions of some bits in single-byte registers. Read/write access to these bits does not cause hardware malfunctions. Since the Evaluation, Flash memory, and MASK ROM products are designed to behave completely the same way in terms of hardware and software.

• Difference of Memory Spaces

If the amount of memory on the Evaluation product is different from that of the Flash memory or MASK ROM product, carefully check the difference in the amount of memory from the model to be actually used when developing software.

For details of memory space, refer to “■ CPU CORE”.

• Current Consumption

The current consumption of Flash memory product is typically greater than for MASK ROM product.

For details of current consumption, refer to “■ ELECTRICAL CHARACTERISTICS”.

• Package

For details of information on each package, refer to “■ PACKAGES AND CORRESPONDING PRODUCTS” and “■ PACKAGE DIMENSIONS”.

• Operating Voltage

The operating voltage are different among the Evaluation, Flash memory, and MASK ROM products.

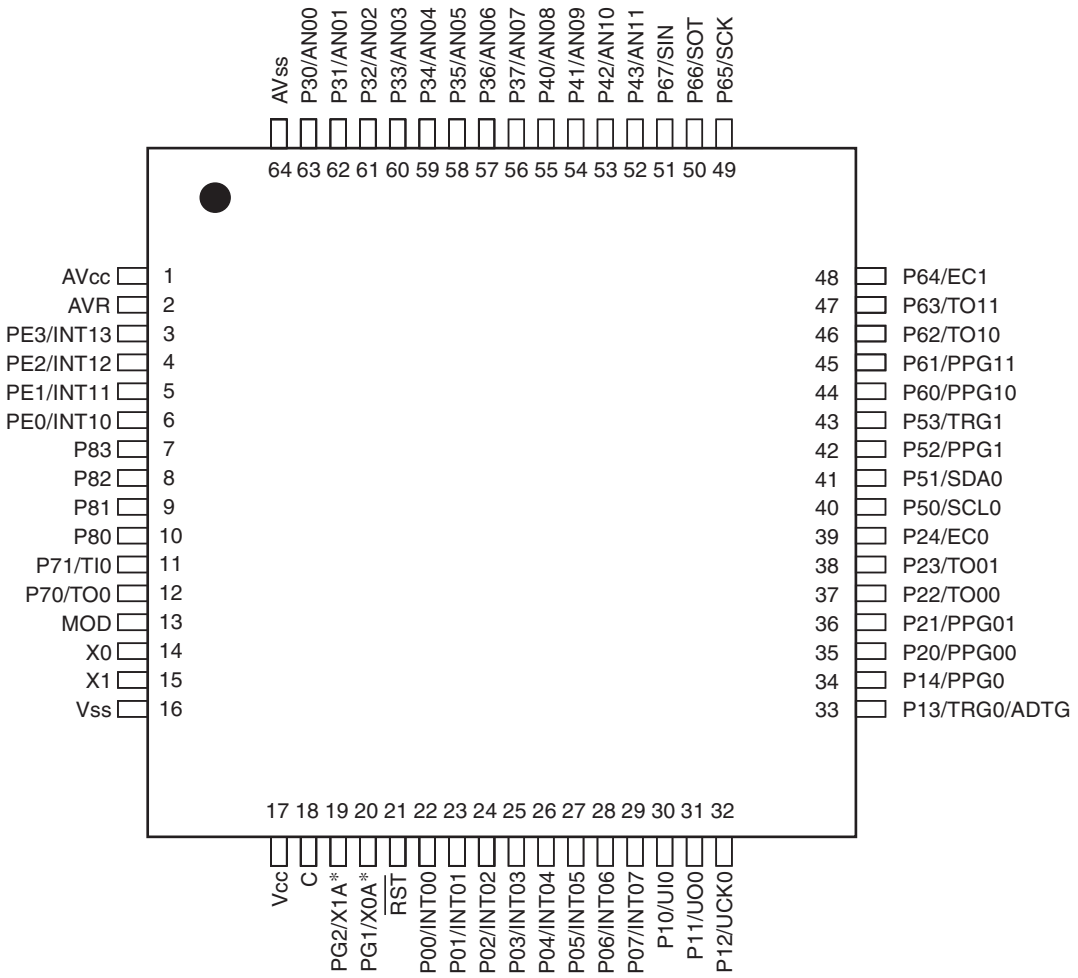
For details of operating voltage, refer to “■ ELECTRICAL CHARACTERISTICS”.

• Difference between $\overline{\text{RST}}$ and MOD Pins

The $\overline{\text{RST}}$ and MOD pins are hysteresis inputs on the MASK ROM product. A pull-down resistor is provided for the MOD pin of the MASK ROM product.

■ PIN ASSIGNMENT

(TOP VIEW)



(FPT-64P-M03, FPT-64P-M09)

* : Single clock product is general-purpose port, and dual clock product is sub clock oscillation pin.

■ PIN DESCRIPTION

Pin no.	Pin name	I/O Circuit type*	Function
1	AVcc	—	A/D converter power supply pin
2	AVR	—	A/D converter reference input pin
3	PE3/INT13	P	General-purpose I/O port. The pins are shared with the external interrupt input.
4	PE2/INT12		
5	PE1/INT11		
6	PE0/INT10		
7	P83	O	General-purpose I/O port
8	P82		
9	P81		
10	P80		
11	P71/TI0	H	General-purpose I/O port. The pin is shared with 16-bit reload timer ch.0 output.
12	P70/TO0		General-purpose I/O port. The pin is shared with 16-bit reload timer ch.0 input.
13	MOD	B	An operating mode designation pin
14	X0	A	Main clock input oscillation pin
15	X1		Main clock input/output oscillation pin
16	Vss	—	Power supply pin (GND)
17	Vcc	—	Power supply pin
18	C	—	Capacitor connection pin
19	PG2/X1A	H/A	Single clock product is general-purpose port (PG2) . Dual clock product is sub clock input/output oscillation pin (32 kHz).
20	PG1/X0A		Single clock product is general-purpose port (PG1) . Dual clock product is sub clock input oscillation pin (32 kHz).
21	$\overline{\text{RST}}$	B’	Reset pin
22	P00/INT00	C	General-purpose I/O port. The pins are shared with external interrupt input. Large current port.
23	P01/INT01		
24	P02/INT02		
25	P03/INT03		
26	P04/INT04		
27	P05/INT05		
28	P06/INT06		
29	P07/INT07		
30	P10/UI0	G	General-purpose I/O port. The pin is shared with UART/SIO ch.0 data input.

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Pin no.	Pin name	I/O Circuit type*	Function
31	P11/UO0	H	General-purpose I/O port. The pin is shared with UART/SIO ch.0 data output.
32	P12/UCK0		General-purpose I/O port. The pin is shared with UART/SIO ch.0 clock I/O.
33	P13/TRG0/ ADTG		General-purpose I/O port. The pin is shared with 16-bit PPG ch.0 trigger input (TRG0) and A/D trigger input (ADTG).
34	P14/PPG0		General-purpose I/O port. The pin is shared with 16-bit PPG ch.0 output.
35	P20/PPG00	H	General-purpose I/O port. The pins are shared with 8/16-bit PPG ch.0 output.
36	P21/PPG01		
37	P22/TO00		General-purpose I/O port. The pins are shared with 8/16-bit compound timer ch.0 output.
38	P23/TO01		
39	P24/EC0		General-purpose I/O port. The pin is shared with 8/16-bit compound timer ch.0 clock input.
40	P50/SCL0	I	General-purpose I/O port. The pin is shared with I^2C ch.0 clock I/O.
41	P51/SDA0		General-purpose I/O port. The pin is shared with I^2C ch.0 data I/O.
42	P52/PPG1	H	General-purpose I/O port. The pin is shared with 16-bit PPG ch.1 output.
43	P53/TRG1		General-purpose I/O port. The pin is shared with 16-bit PPG ch.1 trigger input.
44	P60/PPG10	K	General-purpose I/O port. The pins are shared with 8/16-bit PPG ch.1 output.
45	P61/PPG11		
46	P62/TO10		General-purpose I/O port. The pins are shared with 8/16-bit compound timer ch.1 output.
47	P63/TO11		
48	P64/EC1		General-purpose I/O port. The pin is shared with 8/16-bit compound timer ch.1 clock input.
49	P65/SCK		General-purpose I/O port. The pin is shared with LIN-UART clock I/O.
50	P66/SOT		General-purpose I/O port. The pin is shared with LIN-UART data output.
51	P67/SIN	L	General-purpose I/O port. The pin is shared with LIN-UART data input.
52	P43/AN11	J	General-purpose I/O port. The pins are shared with A/D converter analog input.
53	P42/AN10		
54	P41/AN09		
55	P40/AN08		

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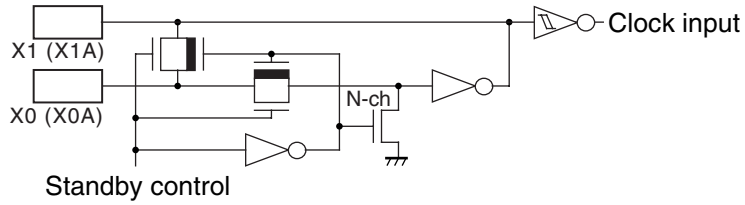
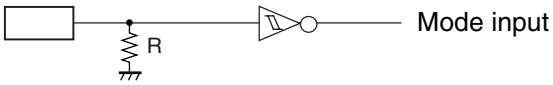
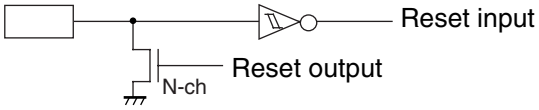
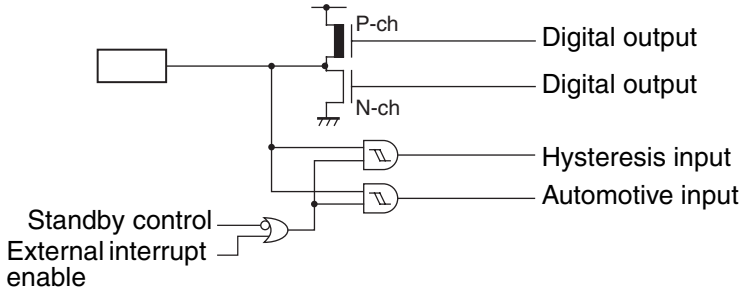
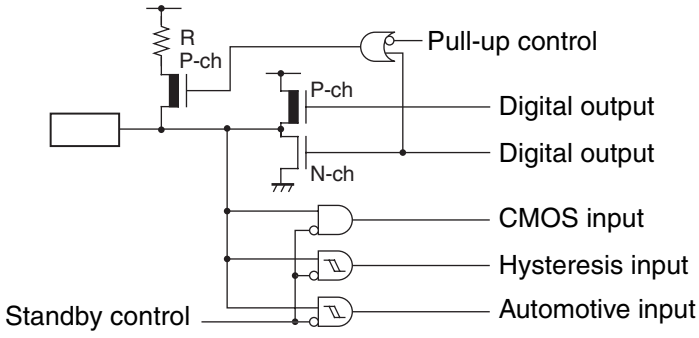
Pin no.	Pin name	I/O Circuit type*	Function
56	P37/AN07	J	General-purpose I/O port. The pins are shared with A/D converter analog input.
57	P36/AN06		
58	P35/AN05		
59	P34/AN04		
60	P33/AN03		
61	P32/AN02		
62	P31/AN01		
63	P30/AN00		
64	AVss	—	A/D converter power supply pin (GND)

*: For the I/O circuit type, refer to “■ I/O CIRCUIT TYPE”

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• Oscillation circuit • High-speed side Feedback resistance : approx. 1 MΩ • Low-speed side Feedback resistance : approx. 10 MΩ
B		• Only for input Hysteresis input only for MASK ROM product With pull-down resistor only for MASK ROM product
B’		• Hysteresis input only for MASK ROM product • Reset output
C		• CMOS output • Hysteresis input • Automotive input
G		• CMOS output • CMOS input • Hysteresis input • With pull-up control • Automotive input

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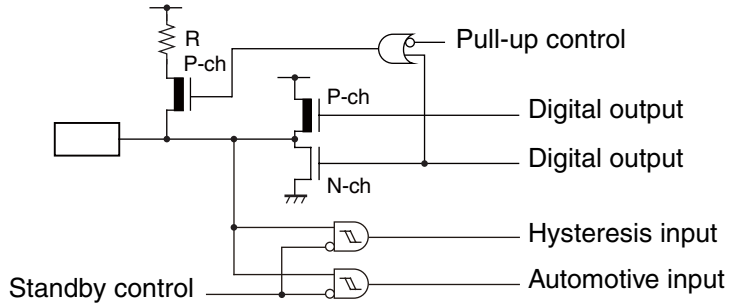
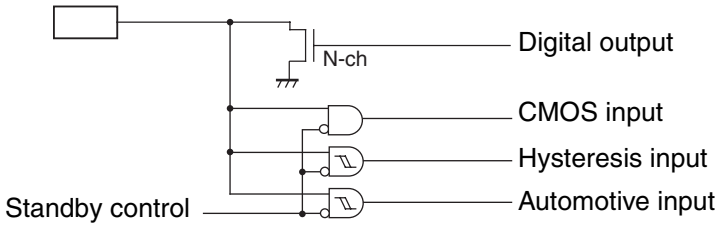
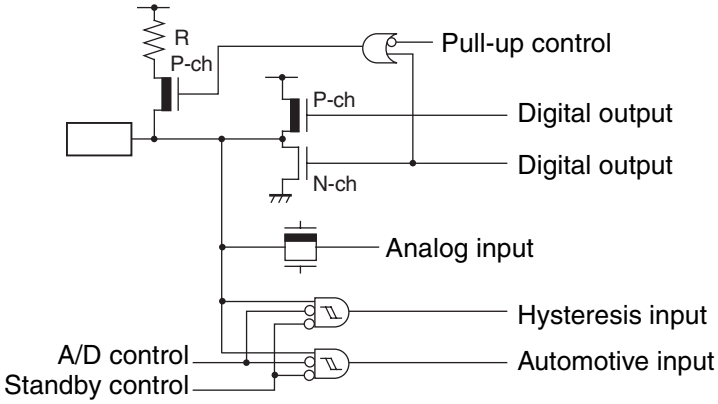
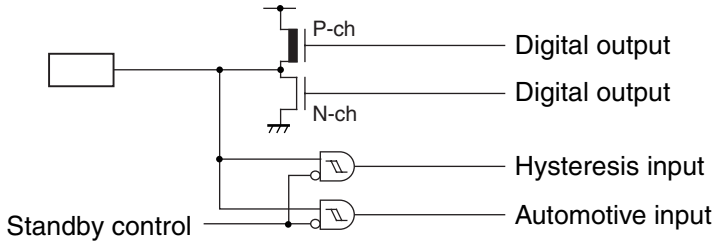
Type	Circuit	Remarks
H		• CMOS output • Hysteresis input • With pull-up control • Automotive input
I		• N-ch open drain output • CMOS input • Hysteresis input • Automotive input
J		• CMOS output • Hysteresis input • Analog input • With pull-up control • Automotive input
K		• CMOS output • Hysteresis input • Automotive input

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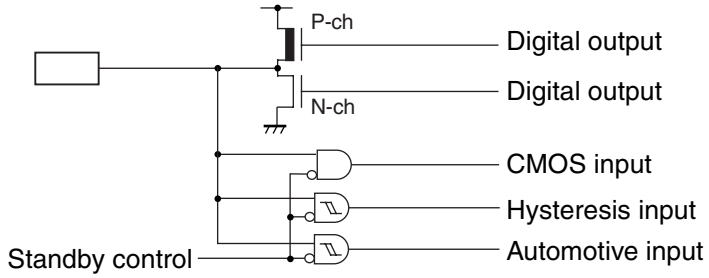
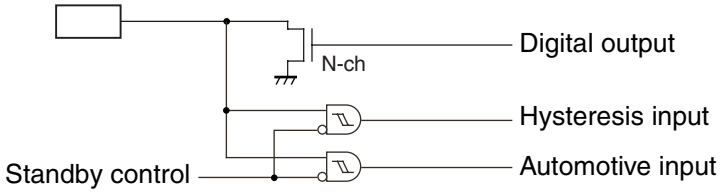
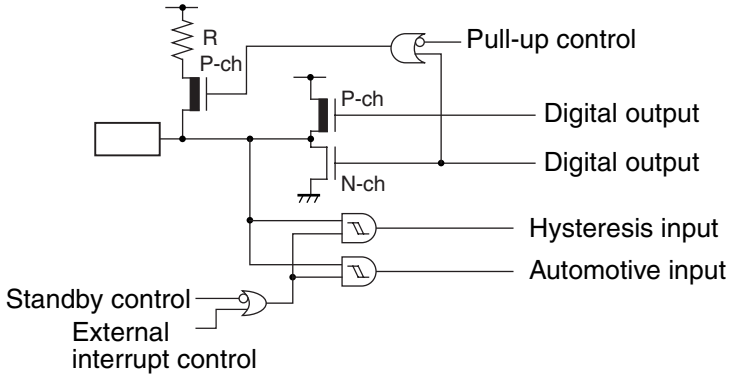
Type	Circuit	Remarks
L		• CMOS output • CMOS input • Hysteresis input • Automotive input
O		• N-ch open drain output • Hysteresis input • Automotive input
P		• CMOS output • Hysteresis input • With pull-up control • Automotive input

■ HANDLING DEVICES

• Preventing Latch-up

Care must be taken to ensure that maximum voltage ratings are not exceeded when they are used.

Latch-up may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- and high-withstand voltage pins or if higher than the rating voltage is applied between V_{CC} pin and V_{SS} pin.

When latch-up occurs, power supply current increases rapidly and might thermally damage elements.

Also, take care to prevent the analog power supply voltage (AV_{CC}, AVR) and analog input voltage from exceeding the digital power supply voltage (V_{CC}) when the analog system power supply is turned on or off.

• Stable Supply Voltage

Supply voltage should be stabilized.

A sudden change in power-supply voltage may cause a malfunction even within the guaranteed operating range of the Vcc power-supply voltage.

For stabilization, in principle, keep the variation in Vcc ripple (p-p value) in a commercial frequency range (50 Hz/60 Hz) not to exceed 10% of the standard Vcc value and suppress the voltage variation so that the transient variation rate does not exceed 0.1 V/ms during a momentary change such as when the power supply is switched.

• Precautions for Use of External Clock

Even when an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from sub clock mode or stop mode.

■ PIN CONNECTION

• Treatment of Unused Input Pin

Leaving unused input pins unconnected can cause abnormal operation or latch-up, leaving to permanent damage. Unused input pins should always be pulled up or down through resistance of at least 2 kΩ. Any unused input/output pins may be set to output mode and left open, or set to input mode and treated the same as unused input pins. If there is unused output pin, make it to open.

• Treatment of Power Supply Pins on A/D Converter

Connect to be $AV_{CC} = V_{CC}$ and $AV_{SS} = AVR = V_{SS}$ even if the A/D converter is not in use.

Noise riding on the AV_{CC} pin may cause accuracy degradation. So, connect approx. 0.1 µF ceramic capacitor as a bypass capacitor between AV_{CC} and AV_{SS} pins in the vicinity of this device.

• Power Supply Pins

In products with multiple V_{CC} or V_{SS} pins, the pins of the same potential are internally connected in the device to avoid abnormal operations including latch-up. However, you must connect the pins to external power supply and a ground line to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with the V_{CC} and V_{SS} pins of this device at the low impedance.

It is also advisable to connect a ceramic bypass capacitor of approximately 0.1 µF between V_{CC} and V_{SS} near this device.

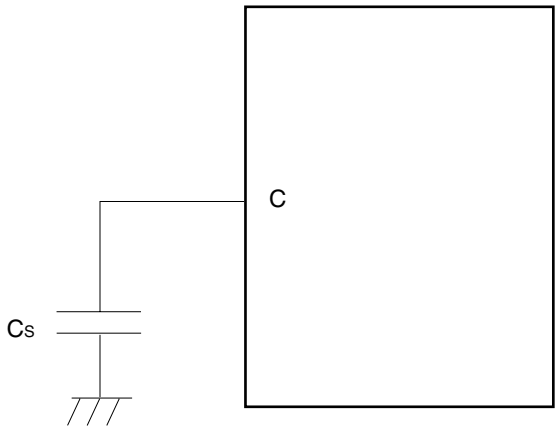
- Mode Pin (MOD)

  Connect the MOD pin directly to V_{CC} or V_{SS} pins.

  To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the MOD pins to V_{CC} or V_{SS} pins and to provide a low-impedance connection.

  Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. A bypass capacitor of V_{CC} pin must have a capacitance value higher than C_S. For connection of smoothing capacitor C_S, refer to the diagram below.

- C pin connection diagram



- Analog Power Supply

  Always set the same potential to AV_{CC} and V_{CC} pins. When V_{CC} > AV_{CC}, the current may flow through the AN00 to AN11 pins.

■ PROGRAMMING FLASH MEMORY MICROCONTROLLERS USING PARALLEL PROGRAMMER

• **Supported Parallel Programmers and Adapters**

The following table lists supported parallel programmers and adapters.

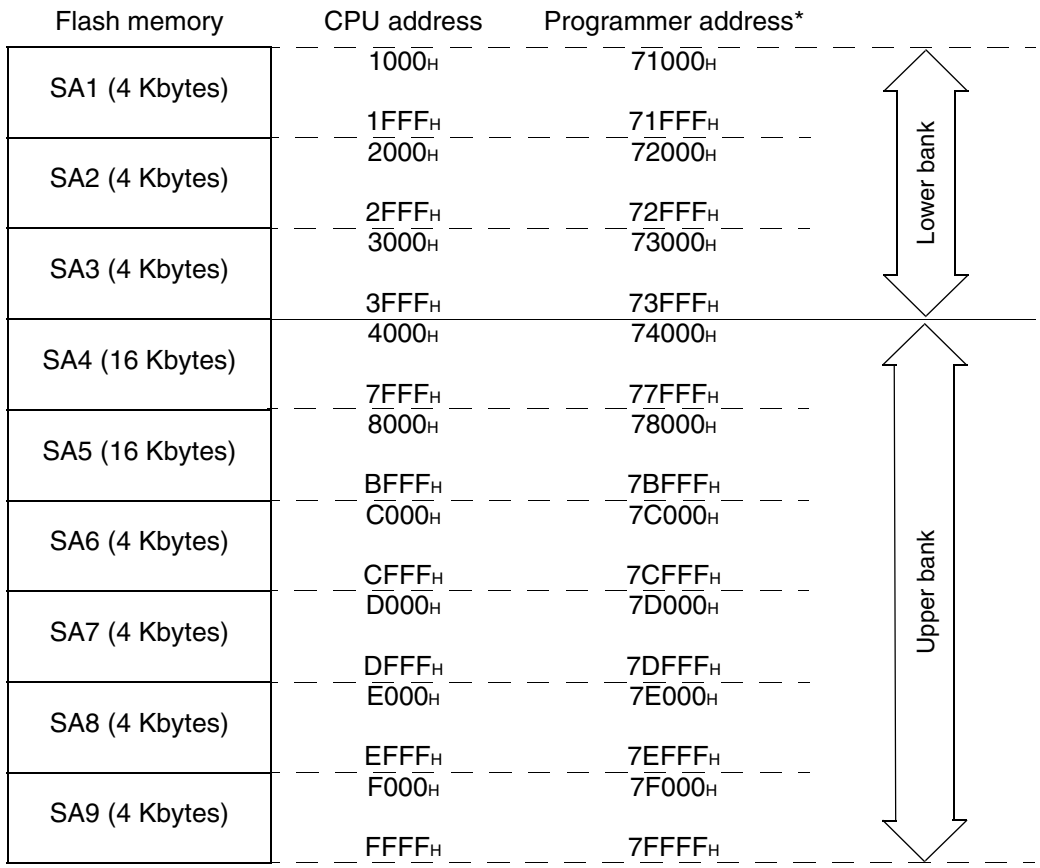
Package	Applicable adapter model	Parallel programmers
FPT-64P-M03	TEF110-108F35AP	AF9708 (Ver 02.35G or more) AF9709/B (Ver 02.35G or more) AF9723+AF9834 (Ver 02.08E or more)
FPT-64P-M09	TEF110-108F36AP	

Note : For information on applicable adapter models and parallel programmers, contact the following:
Flash Support Group, Inc. TEL: +81-53-428-8380

• **Sector Configuration**

The individual sectors of Flash memory correspond to addresses used for CPU access and programming by the parallel programmer as follows:

• MB95F108AMS/F108ANS/F108AJS/F108AMW/F108ANW/F108AJW (60 Kbytes)



*: Programmer addresses are equivalent to CPU addresses, used when the parallel programmer programs data into Flash memory.
These programmer addresses are used for the parallel programmer to program or erase data in Flash memory.

• **Programming Method**

1) Set the type code of the parallel programmer to “17222”.

2) Load program data to programmer addresses 71000H to 7FFFFH.

3) Programmed by parallel programmer

• MB95F106AMS/F106ANS/F106AJS/F106AMW/F106ANW/F106AJW (32 Kbytes)

Flash memory	CPU address	Programmer address*
SA5 (16 Kbytes)	8000H	78000H
	BFFFH	7BFFFH
SA6 (4 Kbytes)	C000H	7C000H
	CFFFH	7CFFFH
SA7 (4 Kbytes)	D000H	7D000H
	DFFFH	7DFFFH
SA8 (4 Kbytes)	E000H	7E000H
	EFFFH	7EFFFH
SA9 (4 Kbytes)	F000H	7F000H
	FFFFH	7FFFFH

*: Programmer addresses are equivalent to CPU addresses, used when the parallel programmer programs data into Flash memory.
These programmer addresses are used for the parallel programmer to program or erase data in Flash memory.

• **Programming Method**

1) Set the type code of the parallel programmer to "17222"
2) Load program data to programmer addresses 78000H to 7FFFFH.
3) Programmed by parallel programmer

• MB95F104AMS/F104ANS/F104AJS/F104AMW/F104ANW/F104AJW (16 Kbytes)

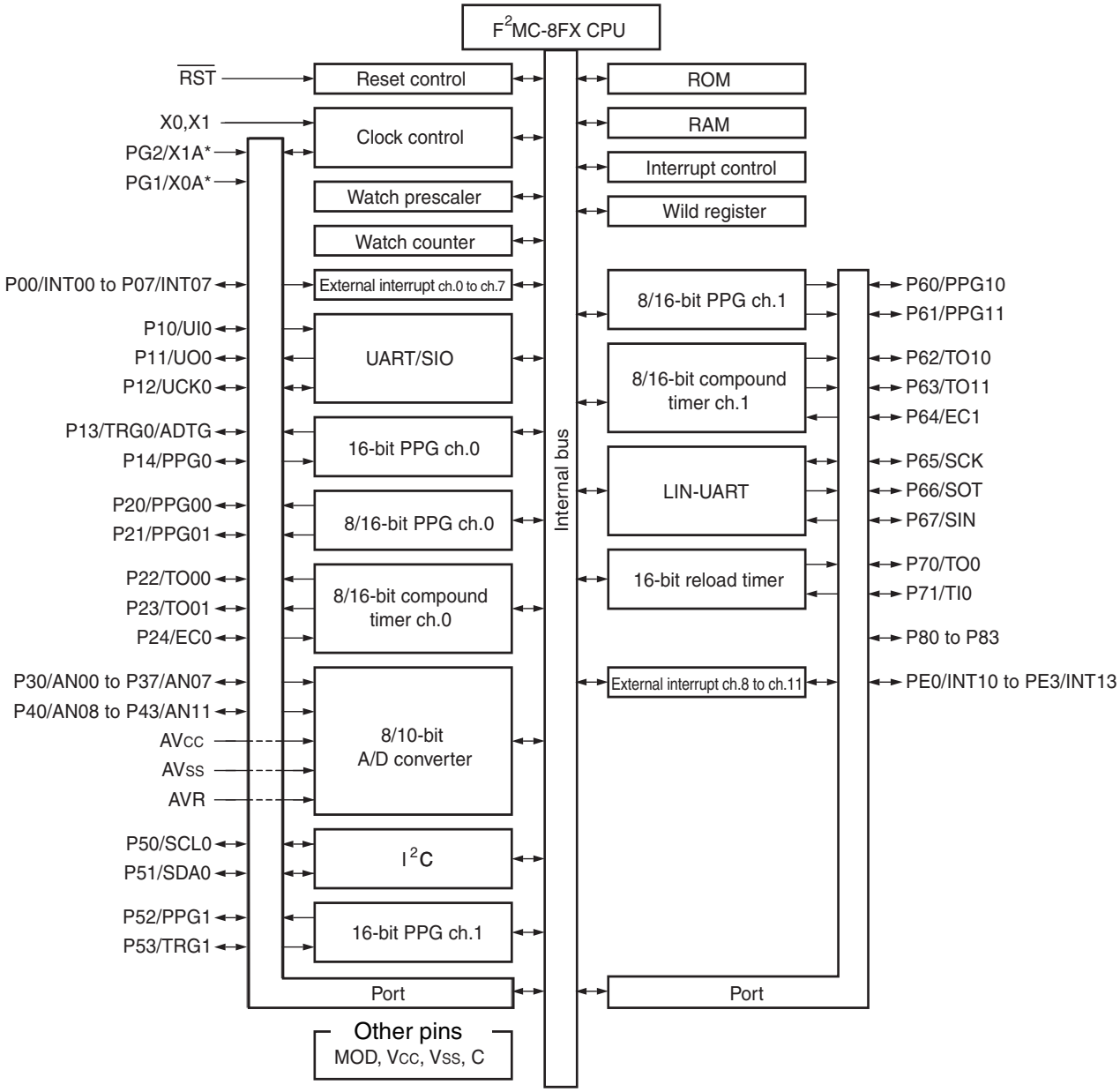
Flash memory	CPU address	Programmer address*
SA6 (4 Kbytes)	C000H	7C000H
	CFFFH	7CFFFH
SA7 (4 Kbytes)	D000H	7D000H
	DFFFH	7DFFFH
SA8 (4 Kbytes)	E000H	7E000H
	EFFFH	7EFFFH
SA9 (4 Kbytes)	F000H	7F000H
	FFFFH	7FFFFH

*: Programmer addresses are equivalent to CPU addresses, used when the parallel programmer programs data into Flash memory.
These programmer addresses are used for the parallel programmer to program or erase data in Flash memory.

• **Programming Method**

1) Set the type code of the parallel programmer to "17222"
2) Load program data to programmer addresses 7C000H to 7FFFFH.
3) Programmed by parallel programmer

■ BLOCK DIAGRAM



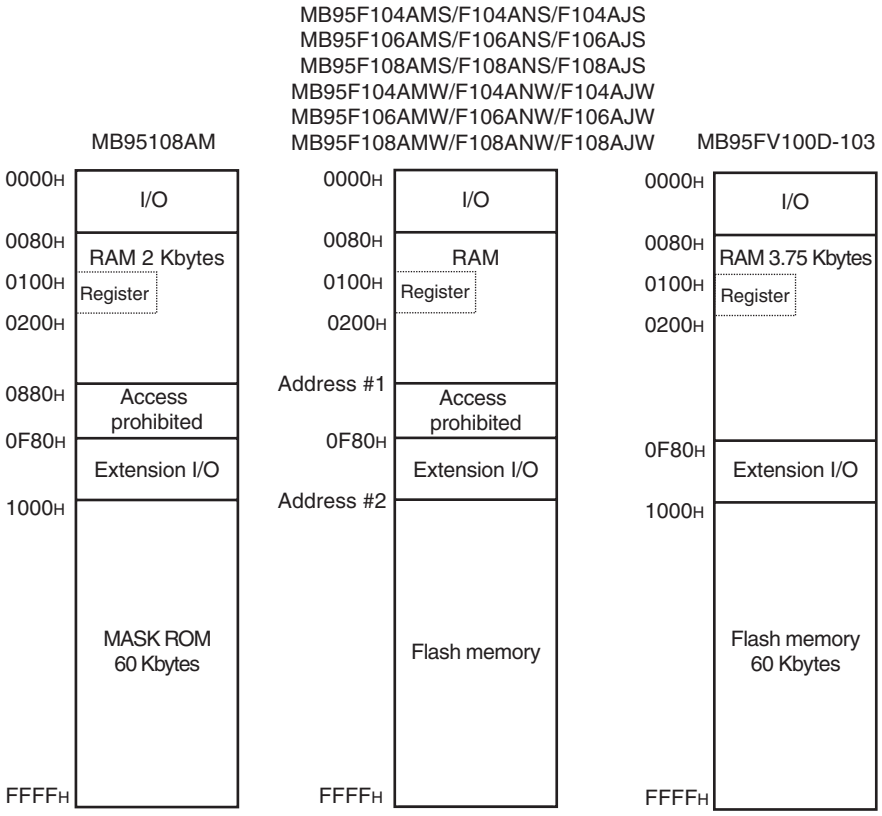
* : Single clock product is general-purpose port, and dual clock product is sub clock oscillation pin.

■ CPU CORE

1. Memory space

Memory space of the MB95100AM series is 64 Kbytes and consists of I/O area, data area, and program area. The memory space includes special-purpose areas such as the general-purpose registers and vector table. Memory map of the MB95100AM series is shown below.

• Memory Map

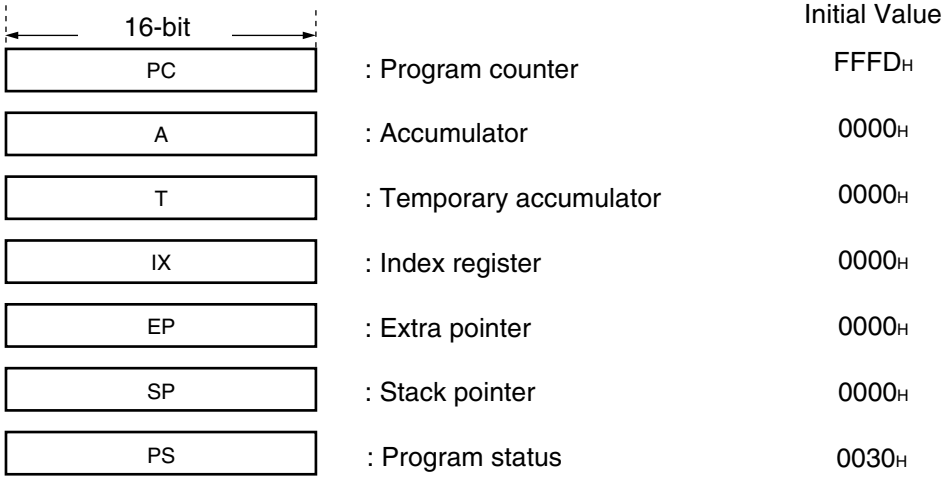


	Flash	RAM	Address #1	Address #2
MB95F104AMS/F104ANS/F104AJS	16 Kbytes	512 bytes	0280H	C000H
MB95F104AMW/F104ANW/F104AJW				
MB95F106AMS/F106ANS/F106AJS	32 Kbytes	1 Kbyte	0480H	8000H
MB95F106AMW/F106ANW/F106AJW				
MB95F108AMS/F108ANS/F108AJS	60 Kbytes	2 Kbytes	0880H	1000H
MB95F108AMW/F108ANW/F108AJW				

2. Register

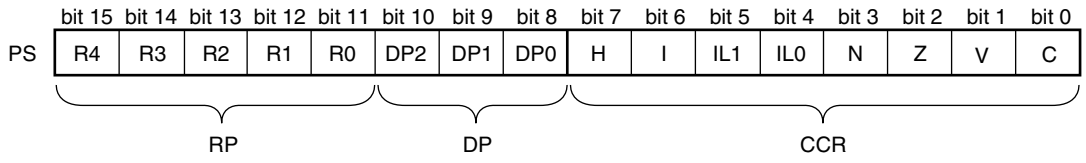
The MB95100AM series has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The dedicated registers are as follows:

Program counter (PC)	:	A 16-bit register to indicate locations where instructions are stored.
Accumulator (A)	:	A 16-bit register for temporary storage of arithmetic operations. In the case of an 8-bit data processing instruction, the lower one byte is used.
Temporary accumulator (T)	:	A 16-bit register which performs arithmetic operations with the accumulator. In the case of an 8-bit data processing instruction, the lower one byte is used.
Index register (IX)	:	A 16-bit register for index modification.
Extra pointer (EP)	:	A 16-bit pointer to point to a memory address.
Stack pointer (SP)	:	A 16-bit register to indicate a stack area.
Program status (PS)	:	A 16-bit register for storing a register bank pointer, a direct bank pointer, and a condition code register.



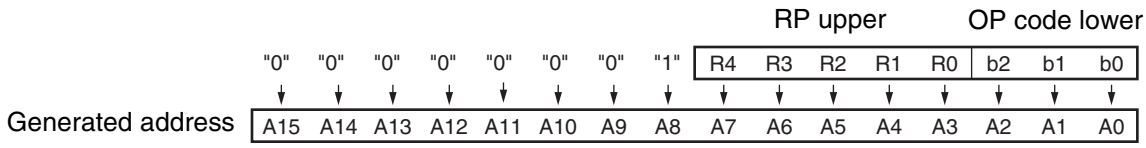
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and a direct bank pointer (DP) and the lower 8 bits for use as a condition code register (CCR) . (Refer to the diagram below.)

• Structure of the Program Status



The RP indicates the address of the register bank currently being used. The relationship between the content of RP and the real address conforms to the conversion rule illustrated below:

• Rule for Conversion of Actual Addresses in the General-purpose Register Area



The DP specifies the area for mapping instructions (16 different instructions such as MOV A, dir) using direct addresses to 0080_H to $00FF_H$.

Direct bank pointer (DP2 to DP0)	Specified address area	Mapping area
XXX_B (no effect to mapping)	0000_H to $007F_H$	0000_H to $007F_H$ (without mapping)
000_B (initial value)	0080_H to $00FF_H$	0080_H to $00FF_H$ (without mapping)
001_B		0100_H to $017F_H$
010_B		0180_H to $01FF_H$
011_B		0200_H to $027F_H$
100_B		0280_H to $02FF_H$
101_B		0300_H to $037F_H$
110_B		0380_H to $03FF_H$
111_B		0400_H to $047F_H$

The CCR consists of the bits indicating arithmetic operation results or transfer data contents and the bits that control CPU operations at interrupt.

H flag : Set to “1” when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared to “0” otherwise. This flag is for decimal adjustment instructions.

I flag : Interrupt is enabled when this flag is set to “1”. Interrupt is disabled when this flag is set to “0”. The flag is set to “0” when reset.

IL1, IL0 : Indicates the level of the interrupt currently enabled. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	Priority
0	0	0	High
0	1	1	↕
1	0	2	
1	1	3	Low = no interruption

N flag : Set to “1” if the MSB is set to “1” as the result of an arithmetic operation. Cleared to “0” when the bit is set to “0”.

Z flag : Set to “1” when an arithmetic operation results in “0”. Cleared to “0” otherwise.

V flag : Set to “1” if the complement on 2 overflows as a result of an arithmetic operation. Cleared to “0” otherwise.

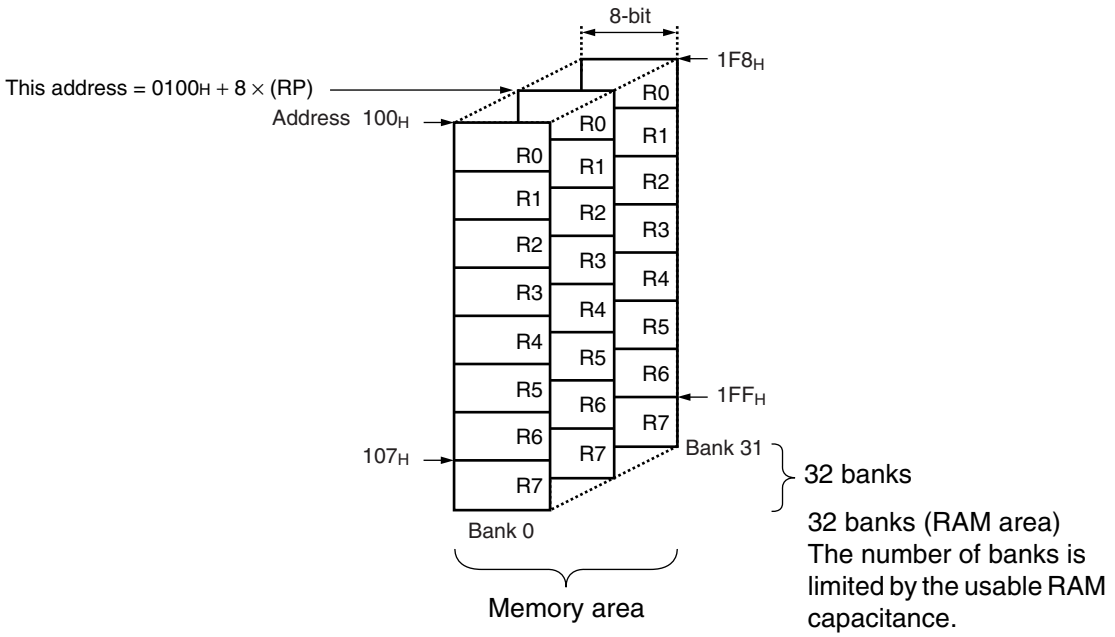
C flag : Set to “1” when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared to “0” otherwise. Set to the shift-out value in the case of a shift instruction.

The following general-purpose registers are provided:

General-purpose registers: 8-bit data storage registers

The general-purpose registers are 8 bits and located in the register banks on the memory. 1-bank contains 8-registers. Up to a total of 32 banks can be used on the MB95100AM series. The bank currently in use is specified by the register bank pointer (RP), and the lower 3 bits of OP code indicates the general-purpose register 0 (R0) to general-purpose register 7 (R7).

- Register Bank Configuration



■ I/O MAP

Address	Register abbreviation	Register name	R/W	Initial value
0000H	PDR0	Port 0 data register	R/W	00000000B
0001H	DDR0	Port 0 direction register	R/W	00000000B
0002H	PDR1	Port 1 data register	R/W	00000000B
0003H	DDR1	Port 1 direction register	R/W	00000000B
0004H	—	(Disabled)	—	—
0005H	WATR	Oscillation stabilization wait time setting register	R/W	11111111B
0006H	PLLC	PLL control register	R/W	00000000B
0007H	SYCC	System clock control register	R/W	1010X011B
0008H	STBC	Standby control register	R/W	00000000B
0009H	RSRR	Reset source register	R	XXXXXXXXB
000AH	TBTC	Timebase timer control register	R/W	00000000B
000BH	WPCR	Watch prescaler control register	R/W	00000000B
000CH	WDTC	Watchdog timer control register	R/W	00000000B
000DH	—	(Disabled)	—	—
000EH	PDR2	Port 2 data register	R/W	00000000B
000FH	DDR2	Port 2 direction register	R/W	00000000B
0010H	PDR3	Port 3 data register	R/W	00000000B
0011H	DDR3	Port 3 direction register	R/W	00000000B
0012H	PDR4	Port 4 data register	R/W	00000000B
0013H	DDR4	Port 4 direction register	R/W	00000000B
0014H	PDR5	Port 5 data register	R/W	00000000B
0015H	DDR5	Port 5 direction register	R/W	00000000B
0016H	PDR6	Port 6 data register	R/W	00000000B
0017H	DDR6	Port 6 direction register	R/W	00000000B
0018H	PDR7	Port 7 data register	R/W	00000000B
0019H	DDR7	Port 7 direction register	R/W	00000000B
001AH	PDR8	Port 8 data register	R/W	00000000B
001BH	DDR8	Port 8 direction register	R/W	00000000B
001CH to 0025H	—	(Disabled)	—	—
0026H	PDRE	Port E data register	R/W	00000000B
0027H	DDRE	Port E direction register	R/W	00000000B
0028H, 0029H	—	(Disabled)	—	—
002AH	PDRG	Port G data register	R/W	00000000B

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
002B$_H$	DDRG	Port G direction register	R/W	00000000$_B$
002C$_H$	—	(Disabled)	—	—
002D$_H$	PUL1	Port 1 pull-up register	R/W	00000000$_B$
002E$_H$	PUL2	Port 2 pull-up register	R/W	00000000$_B$
002F$_H$	PUL3	Port 3 pull-up register	R/W	00000000$_B$
0030$_H$	PUL4	Port 4 pull-up register	R/W	00000000$_B$
0031$_H$	PUL5	Port 5 pull-up register	R/W	00000000$_B$
0032$_H$	PUL7	Port 7 pull-up register	R/W	00000000$_B$
0033$_H$	—	(Disabled)	—	—
0034$_H$	PULE	Port E pull-up register	R/W	00000000$_B$
0035$_H$	PULG	Port G pull-up register	R/W	00000000$_B$
0036$_H$	T01CR1	8/16-bit compound timer 01 control status register 1 ch.0	R/W	00000000$_B$
0037$_H$	T00CR1	8/16-bit compound timer 00 control status register 1 ch.0	R/W	00000000$_B$
0038$_H$	T11CR1	8/16-bit compound timer 11 control status register 1 ch.1	R/W	00000000$_B$
0039$_H$	T10CR1	8/16-bit compound timer 10 control status register 1 ch.1	R/W	00000000$_B$
003A$_H$	PC01	8/16-bit PPG1 control register ch.0	R/W	00000000$_B$
003B$_H$	PC00	8/16-bit PPG0 control register ch.0	R/W	00000000$_B$
003C$_H$	PC11	8/16-bit PPG1 control register ch.1	R/W	00000000$_B$
003D$_H$	PC10	8/16-bit PPG0 control register ch.1	R/W	00000000$_B$
003E$_H$	TMCSRH0	16-bit reload timer control status register (Upper byte) ch.0	R/W	00000000$_B$
003F$_H$	TMCSRL0	16-bit reload timer control status register (Lower byte) ch.0	R/W	00000000$_B$
0040$_H$, 0041$_H$	—	(Disabled)	—	—
0042$_H$	PCNTH0	16-bit PPG status control register (Upper byte) ch.0	R/W	00000000$_B$
0043$_H$	PCNTL0	16-bit PPG status control register (Lower byte) ch.0	R/W	00000000$_B$
0044$_H$	PCNTH1	16-bit PPG status control register (Upper byte) ch.1	R/W	00000000$_B$
0045$_H$	PCNTL1	16-bit PPG status control register (Lower byte) ch.1	R/W	00000000$_B$
0046$_H$, 0047$_H$	—	(Disabled)	—	—
0048$_H$	EIC00	External interrupt circuit control register ch.0/ch.1	R/W	00000000$_B$
0049$_H$	EIC10	External interrupt circuit control register ch.2/ch.3	R/W	00000000$_B$
004A$_H$	EIC20	External interrupt circuit control register ch.4/ch.5	R/W	00000000$_B$
004B$_H$	EIC30	External interrupt circuit control register ch.6/ch.7	R/W	00000000$_B$
004C$_H$	EIC01	External interrupt circuit control register ch.8/ch.9	R/W	00000000$_B$
004D$_H$	EIC11	External interrupt circuit control register ch.10/ch.11	R/W	00000000$_B$

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
004E$_H$, 004F$_H$	—	(Disabled)	—	—
0050$_H$	SCR	LIN-UART serial control register	R/W	00000000$_B$
0051$_H$	SMR	LIN-UART serial mode register	R/W	00000000$_B$
0052$_H$	SSR	LIN-UART serial status register	R/W	00001000$_B$
0053$_H$	RDR/TDR	LIN-UART reception/transmission data register	R/W	00000000$_B$
0054$_H$	ESCR	LIN-UART extended status control register	R/W	00000100$_B$
0055$_H$	ECCR	LIN-UART extended communication control register	R/W	000000XX$_B$
0056$_H$	SMC10	UART/SIO serial mode control register 1 ch.0	R/W	00000000$_B$
0057$_H$	SMC20	UART/SIO serial mode control register 2 ch.0	R/W	00100000$_B$
0058$_H$	SSR0	UART/SIO serial status register ch.0	R/W	00000001$_B$
0059$_H$	TDR0	UART/SIO serial output data register ch.0	R/W	00000000$_B$
005A$_H$	RDR0	UART/SIO serial input data register ch.0	R	00000000$_B$
005B$_H$ to 005F$_H$	—	(Disabled)	—	—
0060$_H$	IBCR00	I^{2}C bus control register 0 ch.0	R/W	00000000$_B$
0061$_H$	IBCR10	I^{2}C bus control register 1 ch.0	R/W	00000000$_B$
0062$_H$	IBSR0	I^{2}C bus status register ch.0	R	00000000$_B$
0063$_H$	IDDR0	I^{2}C data register ch.0	R/W	00000000$_B$
0064$_H$	IAAR0	I^{2}C address register ch.0	R/W	00000000$_B$
0065$_H$	ICCR0	I^{2}C clock control register ch.0	R/W	00000000$_B$
0066$_H$ to 006B$_H$	—	(Disabled)	—	—
006C$_H$	ADC1	8/10-bit A/D converter control register 1	R/W	00000000$_B$
006D$_H$	ADC2	8/10-bit A/D converter control register 2	R/W	00000000$_B$
006E$_H$	ADDH	8/10-bit A/D converter data register (Upper byte)	R/W	00000000$_B$
006F$_H$	ADDL	8/10-bit A/D converter data register (Lower byte)	R/W	00000000$_B$
0070$_H$	WCSR	Watch counter status register	R/W	00000000$_B$
0071$_H$	—	(Disabled)	—	—
0072$_H$	FSR	Flash memory status register	R/W	000X0000$_B$
0073$_H$	SWRE0	Flash memory sector writing control register 0	R/W	00000000$_B$
0074$_H$	SWRE1	Flash memory sector writing control register 1	R/W	00000000$_B$
0075$_H$	—	(Disabled)	—	—
0076$_H$	WREN	Wild register address compare enable register	R/W	00000000$_B$
0077$_H$	WROR	Wild register data test setting register	R/W	00000000$_B$

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0078H	—	Mirror of register bank pointer (RP) and direct bank pointer (DP)	—	—
0079H	ILR0	Interrupt level setting register 0	R/W	11111111B
007AH	ILR1	Interrupt level setting register 1	R/W	11111111B
007BH	ILR2	Interrupt level setting register 2	R/W	11111111B
007CH	ILR3	Interrupt level setting register 3	R/W	11111111B
007DH	ILR4	Interrupt level setting register 4	R/W	11111111B
007EH	ILR5	Interrupt level setting register 5	R/W	11111111B
007FH	—	(Disabled)	—	—
0F80H	WRARH0	Wild register address setting register (Upper byte) ch.0	R/W	00000000B
0F81H	WRARL0	Wild register address setting register (Lower byte) ch.0	R/W	00000000B
0F82H	WRDR0	Wild register data setting register ch.0	R/W	00000000B
0F83H	WRARH1	Wild register address setting register (Upper byte) ch.1	R/W	00000000B
0F84H	WRARL1	Wild register address setting register (Lower byte) ch.1	R/W	00000000B
0F85H	WRDR1	Wild register data setting register ch.1	R/W	00000000B
0F86H	WRARH2	Wild register address setting register (Upper byte) ch.2	R/W	00000000B
0F87H	WRARL2	Wild register address setting register (Lower byte) ch.2	R/W	00000000B
0F88H	WRDR2	Wild register data setting register ch.2	R/W	00000000B
0F89H to 0F91H	—	(Disabled)	—	—
0F92H	T01CR0	8/16-bit compound timer 01 control status register 0 ch.0	R/W	00000000B
0F93H	T00CR0	8/16-bit compound timer 00 control status register 0 ch.0	R/W	00000000B
0F94H	T01DR	8/16-bit compound timer 01 data register ch.0	R/W	00000000B
0F95H	T00DR	8/16-bit compound timer 00 data register ch.0	R/W	00000000B
0F96H	TMCR0	8/16-bit compound timer 00/01 timer mode control register ch.0	R/W	00000000B
0F97H	T11CR0	8/16-bit compound timer 11 control status register 0 ch.1	R/W	00000000B
0F98H	T10CR0	8/16-bit compound timer 10 control status register 0 ch.1	R/W	00000000B
0F99H	T11DR	8/16-bit compound timer 11 data register ch.1	R/W	00000000B
0F9AH	T10DR	8/16-bit compound timer 10 data register ch.1	R/W	00000000B
0F9BH	TMCR1	8/16-bit compound timer 10/11 timer mode control register ch.1	R/W	00000000B
0F9CH	PPS01	8/16-bit PPG1 cycle setting buffer register ch.0	R/W	11111111B
0F9DH	PPS00	8/16-bit PPG0 cycle setting buffer register ch.0	R/W	11111111B
0F9EH	PDS01	8/16-bit PPG1 duty setting buffer register ch.0	R/W	11111111B
0F9FH	PDS00	8/16-bit PPG0 duty setting buffer register ch.0	R/W	11111111B

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0FA0H	PPS11	8/16-bit PPG1 cycle setting buffer register ch.1	R/W	11111111B
0FA1H	PPS10	8/16-bit PPG0 cycle setting buffer register ch.1	R/W	11111111B
0FA2H	PDS11	8/16-bit PPG1 duty setting buffer register ch.1	R/W	11111111B
0FA3H	PDS10	8/16-bit PPG0 duty setting buffer register ch.1	R/W	11111111B
0FA4H	PPGS	8/16-bit PPG start register	R/W	00000000B
0FA5H	REVC	8/16-bit PPG output inversion register	R/W	00000000B
0FA6H	TMRH0/ TMRLRH0	16-bit timer register (Upper byte) ch.0/ 16-bit reload register (Upper byte) ch.0	R/W	00000000B
0FA7H	TMRL0/ TMRLRL0	16-bit timer register (Lower byte) ch.0/ 16-bit reload register (Lower byte) ch.0	R/W	00000000B
0FA8H, 0FA9H	—	(Disabled)	—	—
0FAAH	PDCRH0	16-bit PPG down counter register (Upper byte) ch.0	R	00000000B
0FABH	PDCRL0	16-bit PPG down counter register (Lower byte) ch.0	R	00000000B
0FACH	PCSRH0	16-bit PPG cycle setting buffer register (Upper byte) ch.0	R/W	11111111B
0FADH	PCSRL0	16-bit PPG cycle setting buffer register (Lower byte) ch.0	R/W	11111111B
0FAEH	PDUTH0	16-bit PPG duty setting buffer register (Upper byte) ch.0	R/W	11111111B
0FAFH	PDUTL0	16-bit PPG duty setting buffer register (Lower byte) ch.0	R/W	11111111B
0FB0H	PDCRH1	16-bit PPG down counter register (Upper byte) ch.1	R	00000000B
0FB1H	PDCRL1	16-bit PPG down counter register (Lower byte) ch.1	R	00000000B
0FB2H	PCSRH1	16-bit PPG cycle setting buffer register (Upper byte) ch.1	R/W	11111111B
0FB3H	PCSRL1	16-bit PPG cycle setting buffer register (Lower byte) ch.1	R/W	11111111B
0FB4H	PDUTH1	16-bit PPG duty setting buffer register (Upper byte) ch.1	R/W	11111111B
0FB5H	PDUTL1	16-bit PPG duty setting buffer register (Lower byte) ch.1	R/W	11111111B
0FB6H to 0FBBH	—	(Disabled)	—	—
0FBCH	BGR1	LIN-UART baud rate generator register 1	R/W	00000000B
0FBDH	BGR0	LIN-UART baud rate generator register 0	R/W	00000000B
0FBEH	PSSR0	UART/SIO dedicated baud rate generator prescaler selection register ch.0	R/W	00000000B
0FBFH	BRSR0	UART/SIO dedicated baud rate generator baud rate setting register ch.0	R/W	00000000B
0FC0H, 0FC1H	—	(Disabled)	—	—
0FC2H	AIDRH	A/D input disable register (Upper byte)	R/W	00000000B
0FC3H	AIDRL	A/D input disable register (Lower byte)	R/W	00000000B

(Continued)

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0FC4H to 0FE2H	—	(Disabled)	—	—
0FE3H	WCDR	Watch counter data register	R/W	00111111B
0FE4H to 0FE6H	—	(Disabled)	—	—
0FE7H	ILSR2	Input level select register 2	R/W	00000000B
0FE8H, 0FE9H	—	(Disabled)	—	—
0FEAH	CSVCR	Clock supervisor control register	R/W	00011100B
0FEBH to 0FEDH	—	(Disabled)	—	—
0FEEH	ILSR	Input level select register	R/W	00000000B
0FEFH	WICR	Interrupt pin control register	R/W	01000000B
0FF0H to 0FFFH	—	(Disabled)	—	—

• R/W access symbols
  R/W : Readable/Writable
  R : Read only
  W : Write only

• Initial value symbols
  0 : The initial value of this bit is “0”.
  1 : The initial value of this bit is “1”.
  X : The initial value of this bit is undefined.

Note : Do not write to the “ (Disabled) ”. Reading the “ (Disabled) ” returns an undefined value.

■ INTERRUPT SOURCE TABLE

Interrupt source	Interrupt request number	Vector table address		Bit name of interrupt level setting register	Same level priority order (at simultaneous occurrence)
		Upper	Lower		
External interrupt ch.0	IRQ0	FFFA$_H$	FFFB$_H$	L00 [1 : 0]	High
External interrupt ch.4					
External interrupt ch.1	IRQ1	FFF8$_H$	FFF9$_H$	L01 [1 : 0]	
External interrupt ch.5					
External interrupt ch.2	IRQ2	FFF6$_H$	FFF7$_H$	L02 [1 : 0]	
External interrupt ch.6					
External interrupt ch.3	IRQ3	FFF4$_H$	FFF5$_H$	L03 [1 : 0]	
External interrupt ch.7					
UART/SIO ch.0	IRQ4	FFF2$_H$	FFF3$_H$	L04 [1 : 0]	
8/16-bit compound timer ch.0 (Lower)	IRQ5	FFF0$_H$	FFF1$_H$	L05 [1 : 0]	
8/16-bit compound timer ch.0 (Upper)	IRQ6	FFEE$_H$	FFEF$_H$	L06 [1 : 0]	
LIN-UART (reception)	IRQ7	FFEC$_H$	FFED$_H$	L07 [1 : 0]	
LIN-UART (transmission)	IRQ8	FFEA$_H$	FFEB$_H$	L08 [1 : 0]	
8/16-bit PPG ch.1 (Lower)	IRQ9	FFE8$_H$	FFE9$_H$	L09 [1 : 0]	
8/16-bit PPG ch.1 (Upper)	IRQ10	FFE6$_H$	FFE7$_H$	L10 [1 : 0]	
16-bit reload timer ch.0	IRQ11	FFE4$_H$	FFE5$_H$	L11 [1 : 0]	
8/16-bit PPG ch.0 (Upper)	IRQ12	FFE2$_H$	FFE3$_H$	L12 [1 : 0]	
8/16-bit PPG ch.0 (Lower)	IRQ13	FFE0$_H$	FFE1$_H$	L13 [1 : 0]	
8/16-bit compound timer ch.1 (Upper)	IRQ14	FFDE$_H$	FFDF$_H$	L14 [1 : 0]	
16-bit PPG ch.0	IRQ15	FFDC$_H$	FFDD$_H$	L15 [1 : 0]	
I^{2}C ch.0	IRQ16	FFDA$_H$	FFDB$_H$	L16 [1 : 0]	
16-bit PPG ch.1	IRQ17	FFD8$_H$	FFD9$_H$	L17 [1 : 0]	
8/10-bit A/D converter	IRQ18	FFD6$_H$	FFD7$_H$	L18 [1 : 0]	
Timebase timer	IRQ19	FFD4$_H$	FFD5$_H$	L19 [1 : 0]	
Watch prescaler/Watch counter	IRQ20	FFD2$_H$	FFD3$_H$	L20 [1 : 0]	
External interrupt ch.8	IRQ21	FFD0$_H$	FFD1$_H$	L21 [1 : 0]	
External interrupt ch.9					
External interrupt ch.10					
External interrupt ch.11					
8/16-bit compound timer ch.1 (Lower)	IRQ22	FFCE$_H$	FFCF$_H$	L22 [1 : 0]	
Flash memory	IRQ23	FFCC$_H$	FFCD$_H$	L23 [1 : 0]	Low

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	Vcc AVcc	Vss − 0.3	Vss + 6.0	V	*2
	AVR	Vss − 0.3	Vss + 6.0		*2
Input voltage*1	V_I	Vss − 0.3	Vss + 6.0		*3
Output voltage*1	V_O	Vss − 0.3	Vss + 6.0	V	*3
Maximum clamp current	I_{CLAMP}	− 2.0	+ 2.0	mA	Applicable to pins*4
Total maximum clamp current	$\Sigma\lvert I_{CLAMP}\rvert$	—	20	mA	Applicable to pins*4
"L" level maximum output current	I_{OL1}	—	15	mA	Other than P00 to P07
	I_{OL2}		15		P00 to P07
"L" level average current	I_{OLAV1}	—	4	mA	Other than P00 to P07 Average output current = operating current × operating ratio (1 pin)
	I_{OLAV2}		12		P00 to P07 Average output current = operating current × operating ratio (1 pin)
"L" level total maximum output current	ΣI_{OL}	—	100	mA	
"L" level total average output current	ΣI_{OLAV}	—	50	mA	Total average output current = operating current × operating ratio (Total of pins)
"H" level maximum output current	I_{OH1}	—	− 15	mA	Other than P00 to P07
	I_{OH2}		− 15		P00 to P07
"H" level average current	I_{OHAV1}	—	− 4	mA	Other than P00 to P07 Average output current = operating current × operating ratio (1 pin)
	I_{OHAV2}		− 8		P00 to P07 Average output current = operating current × operating ratio (1 pin)
"H" level total maximum output current	ΣI_{OH}	—	− 100	mA	
"H" level total average output current	ΣI_{OHAV}	—	− 50	mA	Total average output current = operating current × operating ratio (Total of pins)

(Continued)

(Continued)

Parameter	Symbol	Rating		Unit
		Min	Max	
Power consumption	Pd	—	320	mW
Operating temperature	T_A	− 40	+ 85	°C
Storage temperature	Tstg	− 55	+ 150	°C

*1 : The parameter is based on AV_{SS} = V_{SS} = 0.0 V.

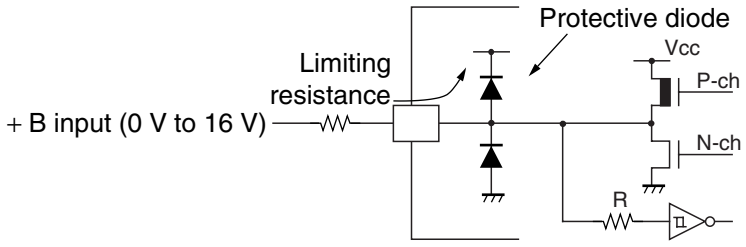
*2 : Apply equal potential to AVcc and Vcc. AVR should not exceed AVcc + 0.3 V.

*3 : V_I and Vo should not exceed V_{CC} + 0.3 V. V_I must not exceed the rating voltage. However, if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

*4 : Applicable to pins : P00 to P07, P10 to P14, P20 to P24, P30 to P37, P40 to P43, P52, P53, P70, P71, PE0 to PE3

- Use within recommended operating conditions.
- Use at DC voltage (current).
- +B signal is an input signal that exceeds V_{CC} voltage. The + B signal should always be applied a limiting resistance placed between the + B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the + B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this affect other devices.
- Note that if the + B signal is inputted when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the + B input is applied during power-on, the power supply is provided from the pins and the resulting power supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the + B input pin open.
- Sample recommended circuits :

• Input/Output Equivalent circuits



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

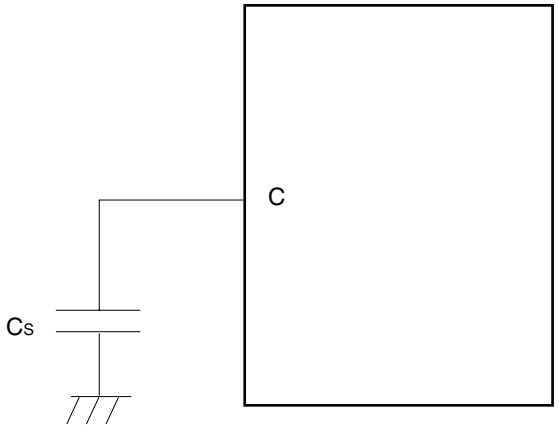
(AVss = Vss = 0.0 V)

Parameter	Symbol	Pin name	Conditions	Value Min	Value Max	Unit	Remarks	
Power supply voltage	V_{CC}, AV_{CC}	—	—	2.42*1	5.5	V	At normal operating	Other than MB95FV100D-103
				2.3	5.5		Retain status of stop operation	
				2.7	5.5		At normal operating	MB95FV100D-103
				2.3	5.5		Retain status of stop operation	
A/D converter reference input voltage	AVR	—	—	4.0	AV_{CC}	V		
Smoothing capacitor	C_S	—	—	0.1	1.0	µF	*2	
Operating temperature	T_A	—	—	− 40	+ 85	°C	Other than MB95FV100D-103	
				+ 5	+ 35		MB95FV100D-103	

*1 : The value is 2.88 V when the low voltage detection reset is used.

*2 : Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. A bypass capacitor of V_{CC} pin must have a capacitance value higher than C_S. For connection of smoothing capacitor C_S, refer to the diagram below.

• C pin connection diagram



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

3. DC Characteristics

(Vcc = AVcc = 5.0 V ± 10%, AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH}	P10, P50, P51, P67	*1	0.7 Vcc	—	Vcc + 0.3	V	Hysteresis input of CMOS input level
	V_{IHA}	P00 to P07, P10 to P14, P20 to P24, P30 to P37, P40 to P43, P50 to P53, P60 to P67, P70, P71, P80 to P83, PE0 to PE3, PG1*2, PG2*2	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Pin input at selecting of Automotive input level
	V_{IHS}	P00 to P07, P10 to P14, P20 to P24, P30 to P37, P40 to P43, P50 to P53, P60 to P67, P70, P71, P80 to P83, PE0 to PE3, PG1*2, PG2*2	*1	0.8 Vcc	—	Vcc + 0.3	V	Hysteresis input
	V_{IHM}	$\overline{RST}$, MOD	—	0.7 Vcc	—	Vcc + 0.3	V	CMOS input (MASK ROM product is hysteresis input)
"L" level input voltage	V_{IL}	P10, P50, P51, P67	*1	Vss − 0.3	—	0.3 Vcc	V	Hysteresis input of CMOS input level
	V_{ILA}	P00 to P07, P10 to P14, P20 to P24, P30 to P37, P40 to P43, P50 to P53, P60 to P67, P70, P71, P80 to P83, PE0 to PE3, PG1*2, PG2*2	—	V_{SS} − 0.3	—	0.5 V_{CC}	V	Pin input at selecting of Automotive input level
	V_{ILS}	P00 to P07, P10 to P14, P20 to P24, P30 to P37, P40 to P43, P50 to P53, P60 to P67, P70, P71, P80 to P83, PE0 to PE3, PG1*2, PG2*2	*1	Vss − 0.3	—	0.2 Vcc	V	Hysteresis input
	V_{ILM}	$\overline{RST}$, MOD	—	Vss − 0.3	—	0.3 Vcc	V	CMOS input (MASK ROM product is hysteresis input)

(Continued)

(Vcc = AVcc = 5.0 V ± 10%, AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Open-drain output application voltage	V_D	P50, P51, P80 to P83	—	Vss − 0.3	—	Vss + 5.5	V	
"H" level output voltage	V_{OH1}	Output pin other than P00 to P07	I_{OH} = − 4.0 mA	Vcc − 0.5	—	—	V	
	V_{OH2}	P00 to P07	I_{OH} = − 8.0 mA	Vcc − 0.5	—	—	V	
"L" level output voltage	V_{OL1}	Output pin other than P00 to P07, $\overline{RST}$*3	I_{OL} = 4.0 mA	—	—	0.4	V	
	V_{OL2}	P00 to P07	I_{OL} = 12 mA	—	—	0.4	V	
Input leakage current (Hi-Z output leakage current)	I_{LI}	Port other than P50, P51, P80 to P83	0.0 V < V_I < Vcc	− 5	—	+ 5	µA	When the pull-up prohibition setting
Open-drain output leakage current	I_{LIOD}	P50, P51, P80 to P83	0.0 V < V_I < Vss + 5.5 V	—	—	5	µA	
Pull-up resistor	R_{PULL}	P10 to P14,P20 to P24, P30 to P37, P40 to P43, P52, P53, P70, P71, PE0 to PE3, PG1*2, PG2*2	V_I = 0.0 V	25	50	100	kΩ	When the pull-up permission setting
Pull-down resistor	R_{MOD}	MOD	V_I = Vcc	25	50	100	kΩ	MASK ROM product
Input capacitance	C_{IN}	Other than AVcc, AVss, AVR, Vcc, Vss	f = 1 MHz	—	5	15	pF	
Power supply current*4	I_{CC}	Vcc (External clock operation)	Vcc = 5.5 V, F_{CH} = 20 MHz, F_{MP} = 10 MHz, Main clock mode (divided by 2)	—	9.5	12.5	mA	Flash memory product (At other than writing and erasing)
				—	30	35	mA	Flash memory product (At writing and erasing)
				—	7.2	9.5	mA	MASK ROM product
			F_{CH} = 32 MHz, F_{MP} = 16 MHz, Main clock mode (divided by 2)	—	15.2	20.0	mA	Flash memory product (At other than writing and erasing)
				—	35.7	42.5	mA	Flash memory product (At writing and erasing)
				—	11.6	15.2	mA	MASK ROM product

(Continued)

(Vcc = AVcc = 5.0 V ± 10%, AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Sym-bol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*4	I_{CCS}	Vcc (External clock operation)	V_{CC} = 5.5 V F_{CH} = 20 MHz F_{MP} = 10 MHz Main sleep mode (divided by 2)	—	4.5	7.5	mA	
			F_{CH} = 32 MHz F_{MP} = 16 MHz Main sleep mode (divided by 2)	—	7.2	12.0	mA	
	I_{CCL}		V_{CC} = 5.5 V F_{CL} = 32 kHz F_{MPL} = 16 kHz Sub clock mode (divided by 2) , T_A = + 25 °C	—	45	100	µA	Dual clock product only
	I_{CCLS}		V_{CC} = 5.5 V F_{CL} = 32 kHz F_{MPL} = 16 kHz Sub sleep mode (divided by 2) , T_A = + 25 °C	—	10	81	µA	Dual clock product only
	I_{CCT}		V_{CC} = 5.5 V F_{CL} = 32 kHz Watch mode Main stop mode T_A = + 25 °C	—	4.6	27.0	µA	Dual clock product only
	I_{CCMPLL}		V_{CC} = 5.5 V F_{CH} = 4 MHz F_{MP} = 10 MHz Main PLL mode (multiplied by 2.5)	—	9.3	12.5	mA	Flash memory product
				—	7.0	9.5	mA	MASK ROM product
			F_{CH} = 6.4 MHz F_{MP} = 16 MHz Main PLL mode (multiplied by 2.5)	—	14.9	20.0	mA	Flash memory product
				—	11.2	15.2	mA	MASK ROM product
	I_{CCSPLL}		V_{CC} = 5.5 V F_{CL} = 32 kHz F_{MPL} = 128 kHz Sub PLL mode (multiplied by 4) , T_A = + 25 °C	—	160	400	µA	Dual clock product only

(Continued)

(Continued)

(Vcc = AVcc = 5.0 V ± 10%, AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Sym-bol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*4	I_{CTS}	V_{CC} (External clock operation)	V_{CC} = 5.5 V F_{CH} = 10 MHz Timebase timer mode T_A = + 25 °C	—	0.15	1.10	mA	
	I_{CCH}		V_{CC} = 5.5 V Sub stop mode T_A = + 25 °C	—	3.5	20	µA	Main stop mode for single clock product
	I_{LVD}	V_{CC}	Current consumption for low voltage detection circuit only	—	38	50	µA	
	I_{CSV}		At oscillating 100 kHz current consumption of internal CR oscillator	—	20	36	µA	
	I_A	AVcc	V_{CC} = 5.5 V F_{CH} = 16 MHz At operating of A/D conversion	—	2.4	4.7	mA	
	I_{AH}		V_{CC} = 5.5 V F_{CH} = 16 MHz At stopping A/D conversion T_A = + 25 °C	—	1	5	µA	

*1 : P10, P50, P51, and P67 can switch the input level to either the “CMOS input level” or “hysteresis input level”. The switching of the input level can be set by the input level selection register (ILSR).

*2 : Single clock products only

*3 : Product without clock supervisor only

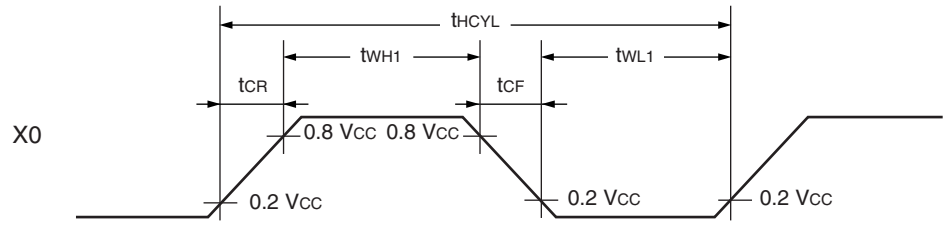
*4 :
- The power-supply current is determined by the external clock. When the low voltage detection option is selected, the power-supply current will be a value of adding current consumption of the low voltage detection circuit (I_{LVD}) to the specified value. Also, when both low voltage detection option and clock supervisor are selected, the power-supply current will be a value of adding current consumption of the low voltage detection circuit (I_{LVD}) and current consumption of internal CR oscillator (I_{CSV}) to the specified value.
- Refer to “4. AC Characteristics (1) Clock Timing” for F_{CH} and F_{CL}.
- Refer to “4. AC Characteristics (2) Source Clock/Machine Clock” for F_{MP} and F_{MPL}.

4. AC Characteristics

(1) Clock Timing

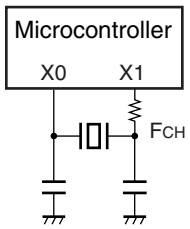
(Vcc = 2.42 V to 5.0 V, AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_{CH}	X0, X1	—	1.00	—	16.25	MHz	When using main oscillation circuit
				1.00	—	32.50	MHz	When using external clock
				3.00	—	10.00	MHz	Main PLL multiplied by 1
				3.00	—	8.13	MHz	Main PLL multiplied by 2
				3.00	—	6.50	MHz	Main PLL multiplied by 2.5
	F_{CL}	X0A, X1A		—	32.768	—	kHz	When using sub oscillation circuit
				—	32.768	—	kHz	When using sub PLL
Clock cycle time	t_{HCYL}	X0, X1		61.5	—	1000	ns	When using oscillation circuit
				30.8	—	1000	ns	When using external clock
	t_{LCYL}	X0A, X1A		—	30.5	—	µs	When using sub clock
Input clock pulse width	t_{WH1} t_{WL1}	X0		61.5	—	—	ns	When using external clock Duty ratio is about 30% to 70%.
	t_{WH2} t_{WL2}	X0A		—	15.2	—	µs	
Input clock rise time and fall time	t_{CR} t_{CF}	X0, X0A		—	—	5	ns	When using external clock

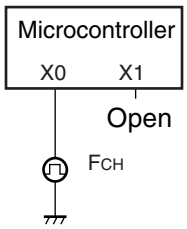


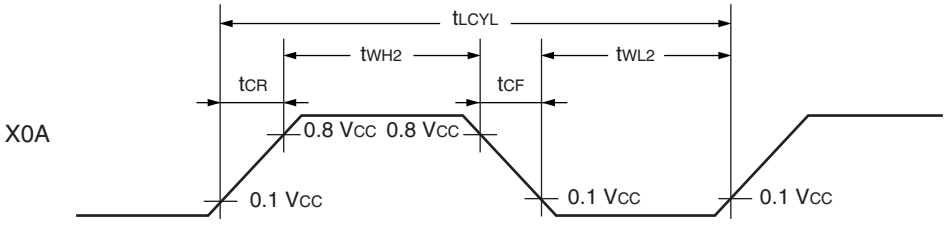
- Figure of main clock input port external connection

When using a crystal or ceramic oscillator



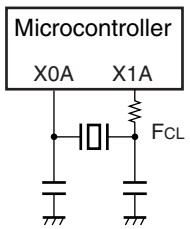
When using external clock



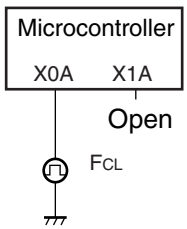


- Figure of sub clock input port external connection

When using a crystal or ceramic oscillator



When using external clock



(2) Source Clock/Machine Clock

(Vcc = 5.0 V ± 10%, AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Source clock*1 (Clock before setting division)	t_{SCLK}	—	61.5	—	2000	ns	When using main clock Min : F_{CH} = 16.25 MHz, PLL multiplied by 1 Max : F_{CH} = 1 MHz, divided by 2
			7.6	—	61.0	µs	When using sub clock Min : F_{CL} = 32 kHz, PLL multiplied by 4 Max : F_{CL} = 32 kHz, divided by 2
Source clock frequency	F_{SP}	—	0.50	—	16.25	MHz	When using main clock
	F_{SPL}	—	16.384	—	131.072	kHz	When using sub clock
Machine clock*2 (Minimum instruction execution time)	t_{MCLK}	—	61.5	—	32000	ns	When using main clock Min : F_{SP} = 16.25 MHz, no division Max : F_{SP} = 0.5 MHz, divided by 16
			7.6	—	976.5	µs	When using sub clock Min : F_{SPL} = 131 kHz, no division Max : F_{SPL} = 16 kHz, divided by 16
Machine clock frequency	F_{MP}	—	0.031	—	16.250	MHz	When using main clock
	F_{MPL}		1.024	—	131.072	kHz	When using sub clock

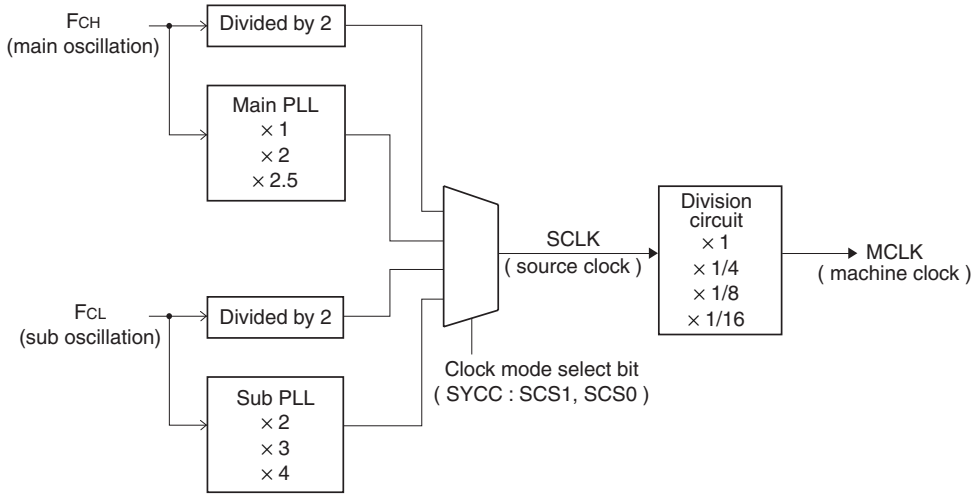
*1 : Clock before setting division due to machine clock division ratio selection bit (SYCC : DIV1 and DIV0) . This source clock is divided by the machine clock division ratio selection bit (SYCC : DIV1 and DIV0) , and it becomes the machine clock. Further, the source clock can be selected as follows.

- Main clock divided by 2
- PLL multiplication of main clock (select from 1, 2, 2.5 multiplication)
- Sub clock divided by 2
- PLL multiplication of sub clock (select from 2, 3, 4 multiplication)

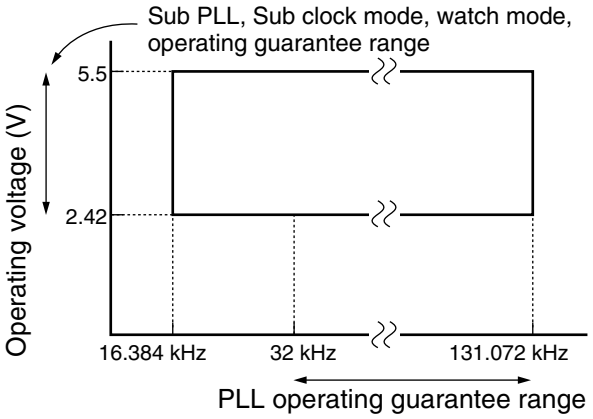
*2 : Operation clock of the microcontroller. Machine clock can be selected as follows.

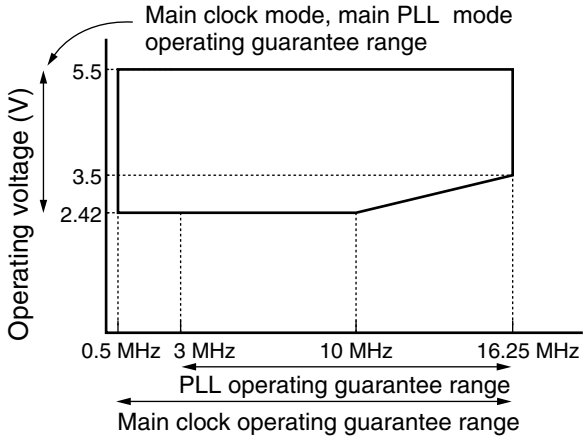
- Source clock (no division)
- Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

• Outline of clock generation block

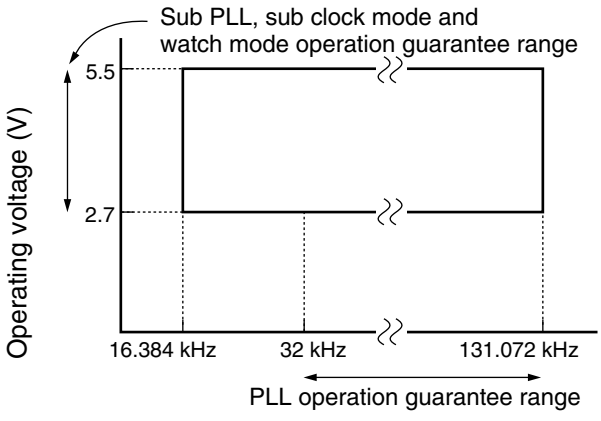


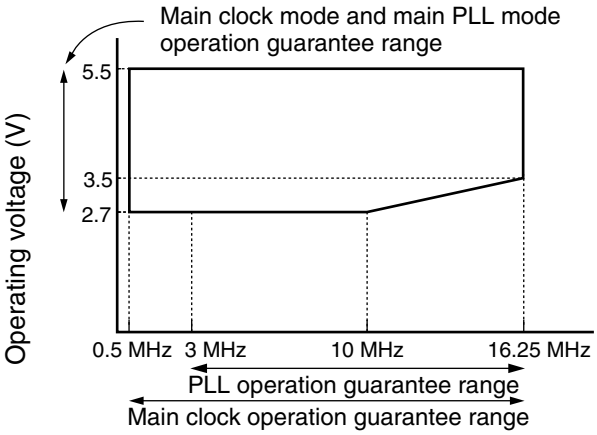
- **Operating voltage – Operating frequency (T_A = – 40 °C to + 85 °C)**
  - MB95F104AMS/F104ANS/F104AJS/F106AMS/F106ANS/F106AJS/F108AMS/F108ANS/F108AJS/F104AMW/ MB95F104ANW/F104AJW/F106AMW/F106ANW/F106AJW/F108AMW/F108ANW/F108AJW



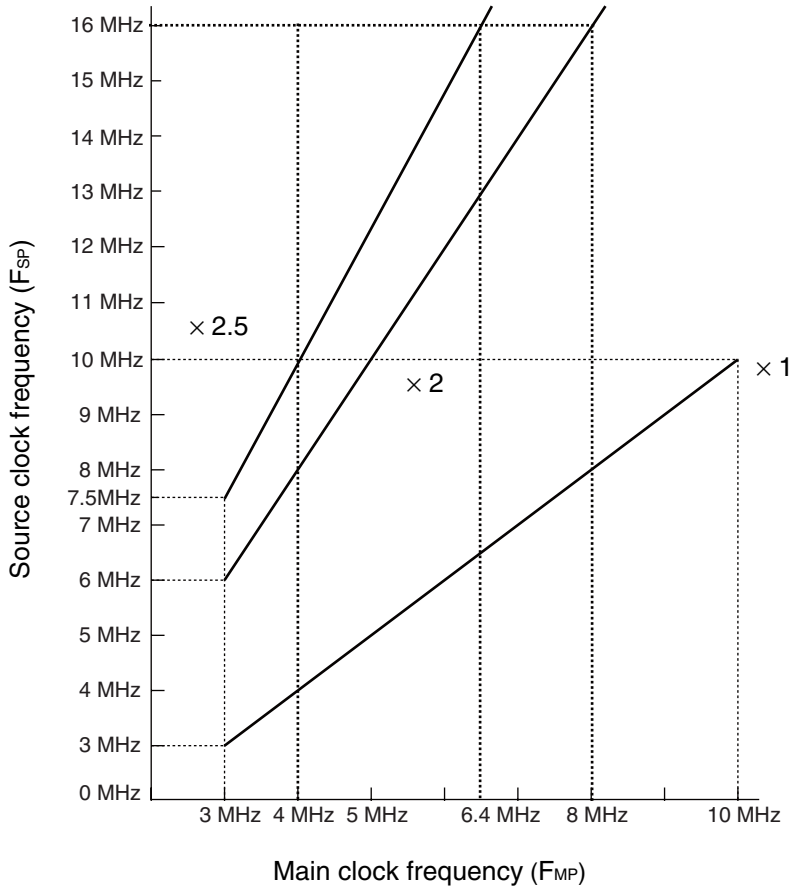


- **Operating voltage – Operating frequency (T_A = + 5 °C to + 35 °C)**
  - MB95FV100D-103





• **Main PLL operation frequency**



(3) External Reset

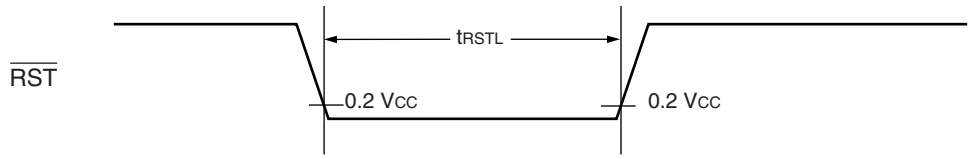
(Vcc = 5.0 V ± 10%, AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
$\overline{RST}$ "L" level pulse width	t_{RSTL}	2 t_{MCLK}*1	—	ns	At normal operating
		Oscillation time of oscillator*2 + 100	—	µs	At stop mode, sub clock mode, sub sleep mode, and watch mode
		100	—	µs	At timebase timer mode

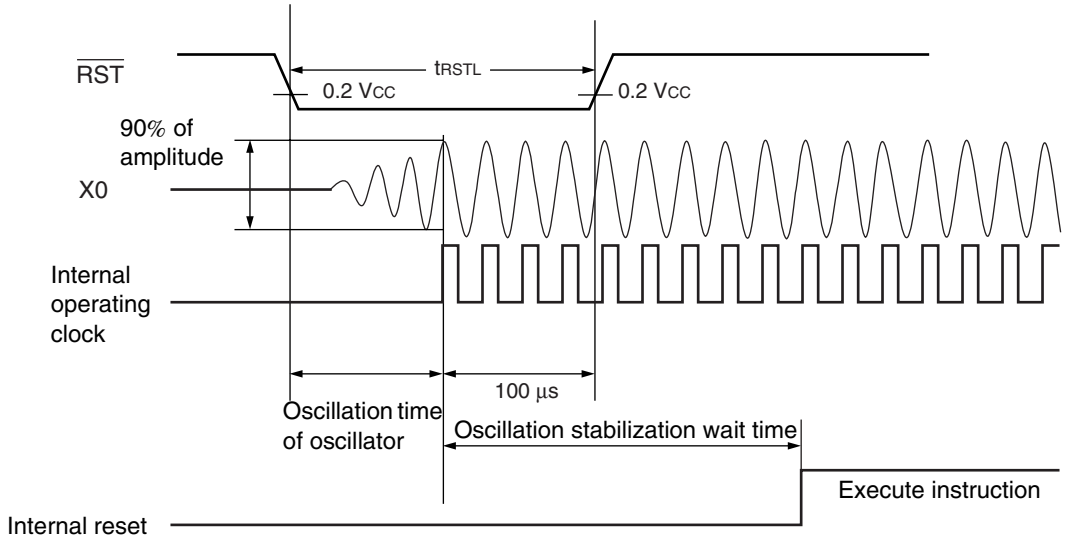
*1 : Refer to " (2) Source Clock/Machine Clock" for t_{MCLK}.

*2 : Oscillation time of oscillator is the time that the amplitude reaches 90 %. In the crystal oscillator, the oscillation time is between several ms and tens of ms. In ceramic oscillators, the oscillation time is between hundreds of µs and several ms. In the external clock, the oscillation time is 0 ms.

• At normal operating



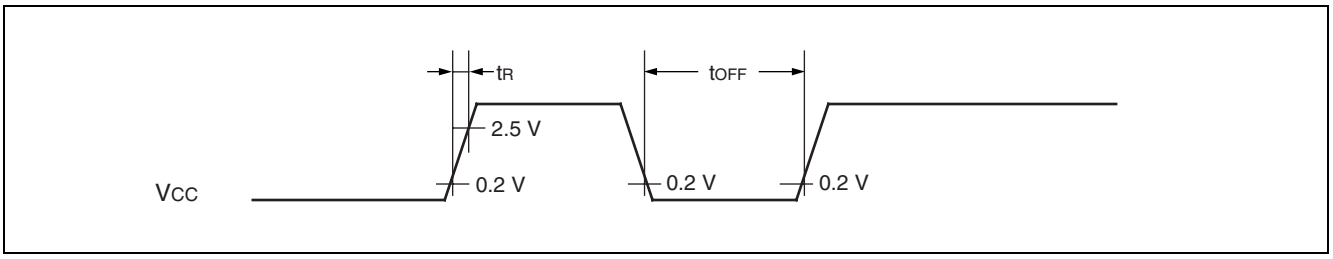
• At stop mode, sub clock mode, sub sleep mode, watch mode, and power-on



(4) Power-on Reset

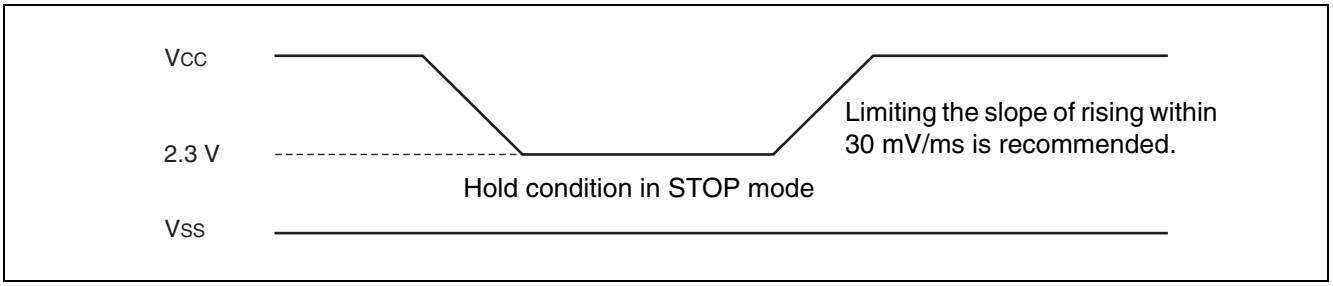
(AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Power supply rising time	t_R	—	—	50	ms	
Power supply cutoff time	t_{OFF}	—	1	—	ms	Waiting time until power-on



Note : Sudden change of power supply voltage may activate the power-on reset function. When changing power supply voltages during operation, set the slope of rising within 30 mV/ms as shown below

.

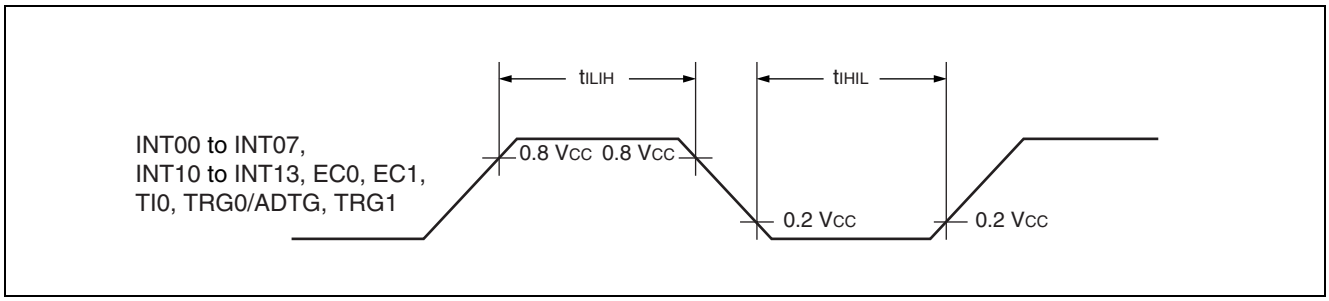


(5) Peripheral Input Timing

(Vcc = 5.0 V ± 10%, AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
Peripheral input “H” pulse width	t_{ILIH}	INT00 to INT07, INT10 to INT13, EC0, EC1, TI0, TRG0/ADTG, TRG1	2 t_{MCLK}*	—	ns
Peripheral input “L” pulse width	t_{IHIL}		2 t_{MCLK}*	—	ns

* : Refer to “ (2) Source Clock/Machine Clock” for t_{MCLK}.



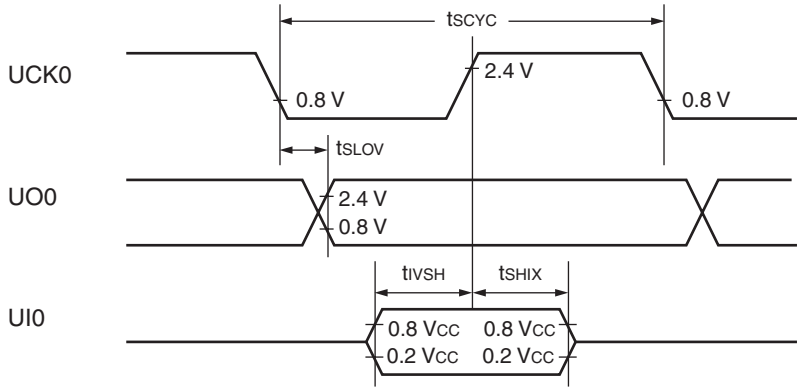
(6) UART/SIO, Serial I/O Timing

(Vcc = 5.0 V ± 10%, AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

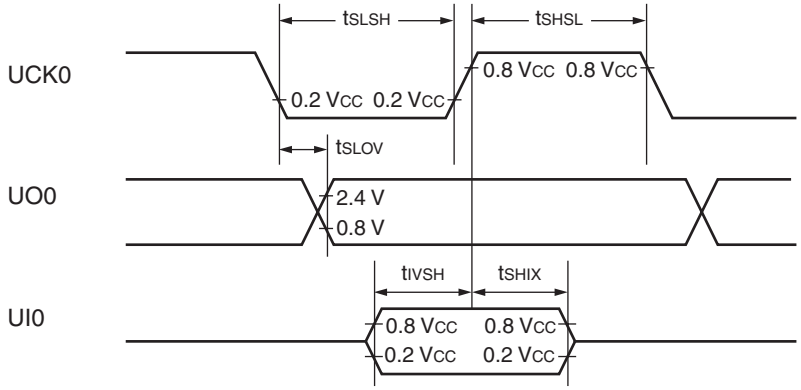
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	UCK0	Internal clock operation	4 t_{MCLK}*	—	ns
UCK ↓ → UO time	t_{SLOV}	UCK0, UO0		− 190	+ 190	ns
Valid UI → UCK ↑	t_{IVSH}	UCK0, UI0		2 t_{MCLK}*	—	ns
UCK ↑ → valid UI hold time	t_{SHIX}	UCK0, UI0		2 t_{MCLK}*	—	ns
Serial clock “H” pulse width	t_{SHSL}	UCK0	External clock operation	4 t_{MCLK}*	—	ns
Serial clock “L” pulse width	t_{SLSH}	UCK0		4 t_{MCLK}*	—	ns
UCK ↓ → UO time	t_{SLOV}	UCK0, UO0		—	190	ns
Valid UI → UCK ↑	t_{IVSH}	UCK0, UI0		2 t_{MCLK}*	—	ns
UCK ↑ → valid UI hold time	t_{SHIX}	UCK0, UI0		2 t_{MCLK}*	—	ns

* : Refer to “ (2) Source Clock/Machine Clock” for t_{MCLK}.

- Internal shift clock mode



- External shift clock mode



(7) LIN-UART Timing

Sampling at the rising edge of sampling clock*1 and prohibited serial clock delay*2

(ESCR register : SCES bit = 0, ECCR register : SCDE bit = 0)

(Vcc = 5.0 V ± 10%, AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

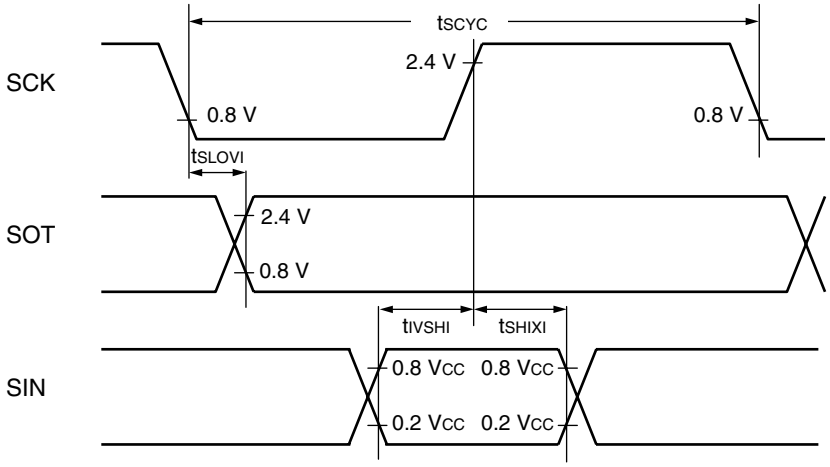
Parameter	Sym-bol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin : C_L = 80 pF + 1 TTL.	5 t_{MCLK}*3	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK, SOT		− 95	+ 95	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK, SIN		t_{MCLK}*3 + 190	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK	External clock operation output pin : C_L = 80 pF + 1 TTL.	3 t_{MCLK}*3 − t_R	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK		t_{MCLK}*3 + 95	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCK, SOT		—	2 t_{MCLK}*3 + 95	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCK, SIN		190	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXE}	SCK, SIN		t_{MCLK}*3 + 95	—	ns
SCK fall time	t_F	SCK		—	10	ns
SCK rise time	t_R	SCK		—	10	ns

*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

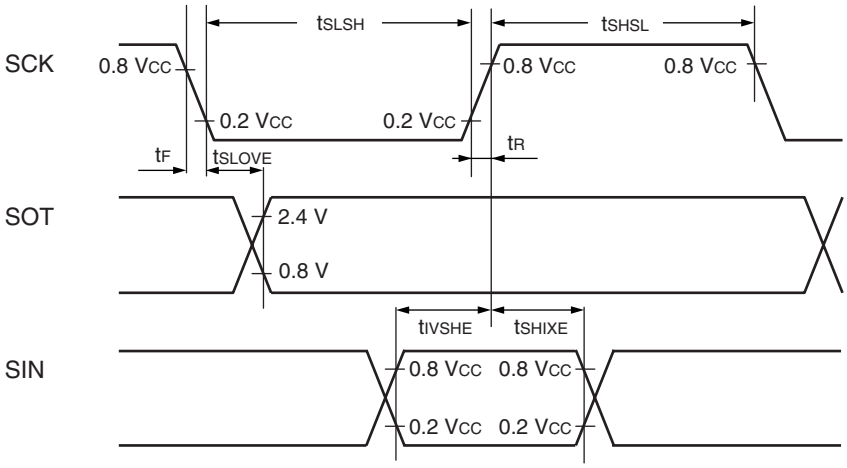
*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

*3 : Refer to “ (2) Source Clock/Machine Clock” for t_{MCLK}.

- Internal shift clock mode



- External shift clock mode



Sampling at the falling edge of sampling clock*1 and prohibited serial clock delay*2

(ESCR register : SCES bit = 1, ECCR register : SCDE bit = 0)

(Vcc = 5.0 V ± 10%, AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

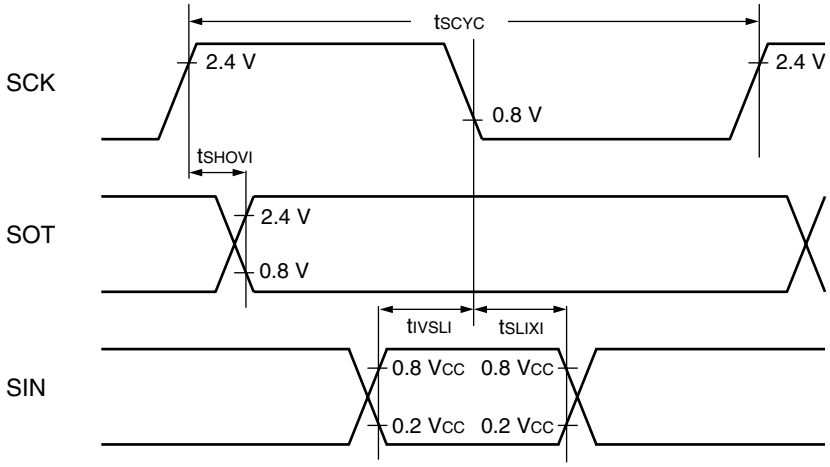
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin : C_L = 80 pF + 1 TTL.	5 t_{MCLK}*3	—	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCK, SOT		− 95	+ 95	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK, SIN		t_{MCLK}*3 + 190	—	ns
SCK ↓ → valid SIN hold time	t_{SLIXI}	SCK, SIN		0	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK	External clock operation output pin : C_L = 80 pF + 1 TTL.	3 t_{MCLK}*3 − t_R	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK		t_{MCLK}*3 + 95	—	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCK, SOT		—	2 t_{MCLK}*3 + 95	ns
Valid SIN → SCK ↓	t_{IVSLE}	SCK, SIN		190	—	ns
SCK ↓ → valid SIN hold time	t_{SLIXE}	SCK, SIN		t_{MCLK}*3 + 95	—	ns
SCK fall time	t_F	SCK		—	10	ns
SCK rise time	t_R	SCK		—	10	ns

*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

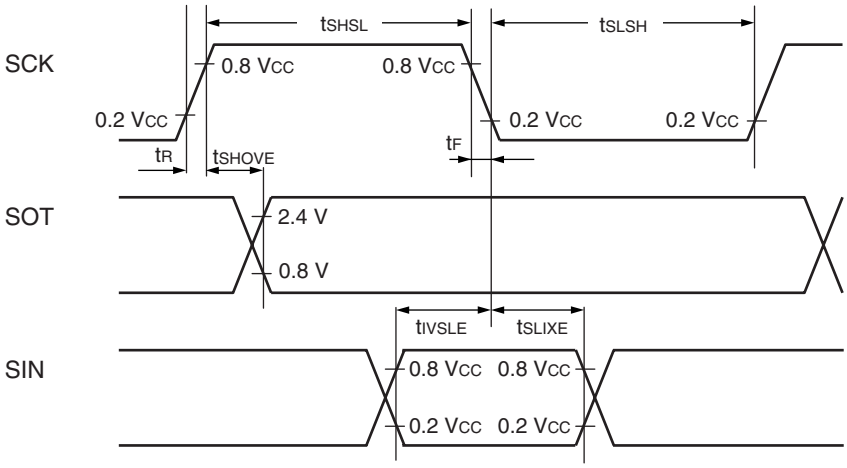
*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

*3 : Refer to “ (2) Source Clock/Machine Clock” for t_{MCLK}.

- Internal shift clock mode



- External shift clock mode



Sampling at the rising edge of sampling clock*1 and enabled serial clock delay*2

(ESCR register : SCES bit = 0, ECCR register : SCDE bit = 1)

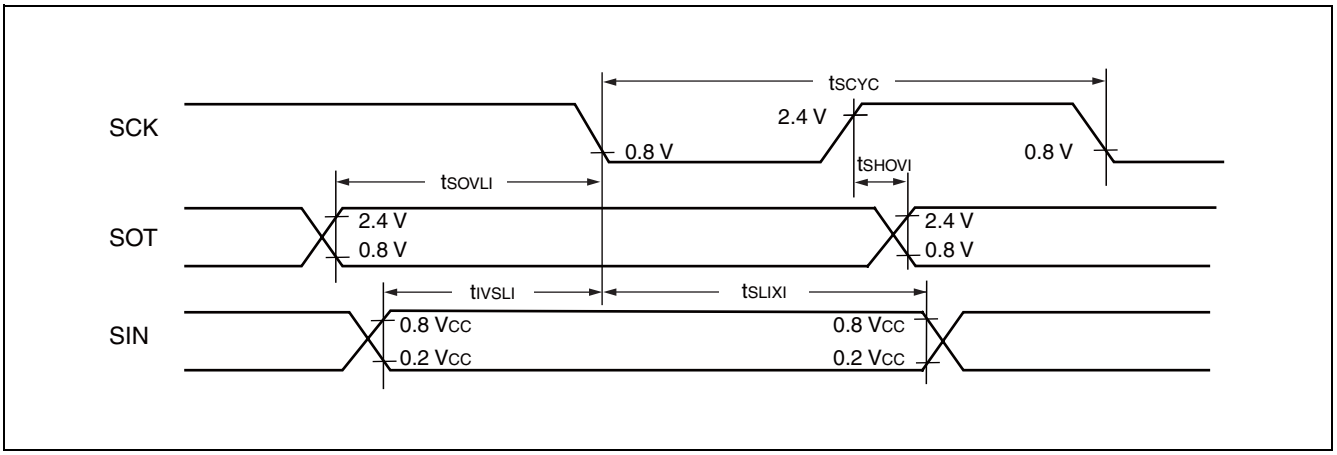
(Vcc = 5.0 V ± 10%, AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin : C_L = 80 pF + 1 TTL.	5 t_{MCLK}*3	—	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCK, SOT		− 95	+ 95	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK, SIN		t_{MCLK}*3 + 190	—	ns
SCK ↓ → valid SIN hold time	t_{SLIXI}	SCK, SIN		0	—	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCK, SOT		—	4 t_{MCLK}*3	ns

*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

*3 : Refer to “ (2) Source Clock/Machine Clock” for t_{MCLK}.



Sampling at the falling edge of sampling clock*1 and enabled serial clock delay*2

(ESCR register : SCES bit = 1, ECCR register : SCDE bit = 1)

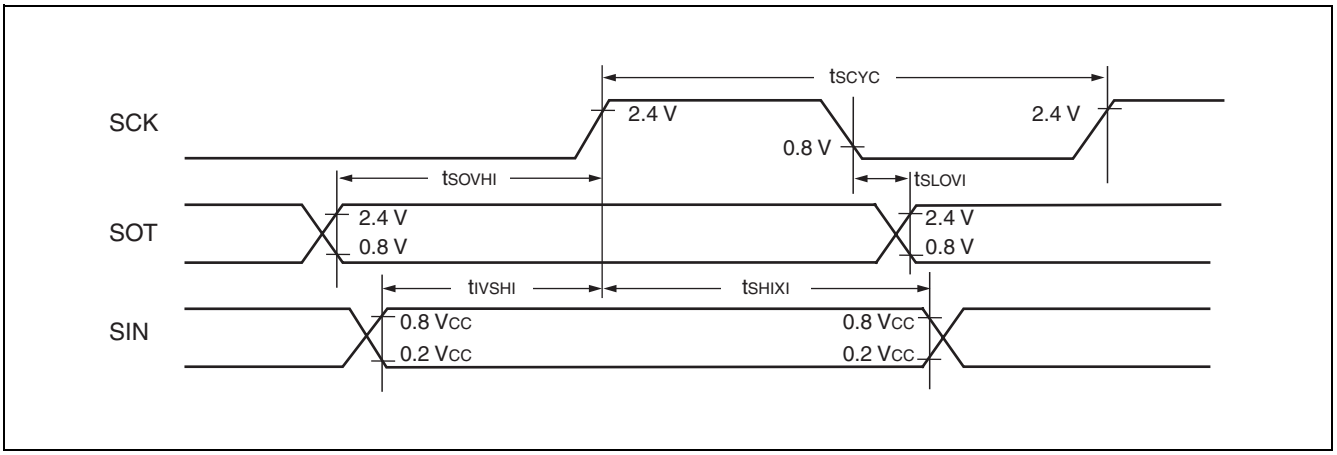
(Vcc = 5.0 V ± 10%, AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Sym-bol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operating output pin : C_L = 80 pF + 1 TTL.	5 t_{MCLK}*3	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK, SOT		− 95	+ 95	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK, SIN		t_{MCLK}*3 + 190	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCK, SOT		—	4 t_{MCLK}*3	ns

*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

*3 : Refer to “ (2) Source Clock/Machine Clock” for t_{MCLK}.



(8) I²C Timing

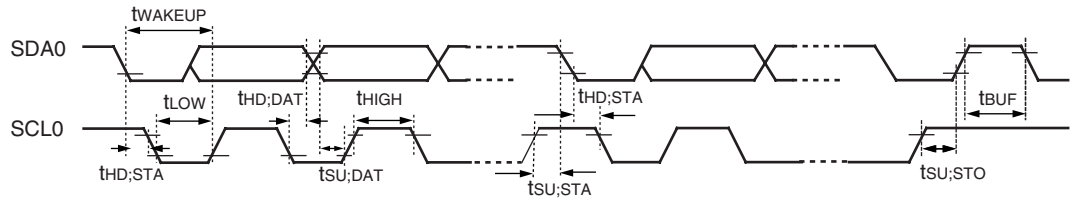
(Vcc = 5.0 V ± 10%, AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value				Unit
				Standard-mode		Fast-mode		
				Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	SCL0	R = 1.7 kΩ, C = 50 pF*1	0	100	0	400	kHz
(Repeat) Start condition hold time SDA ↓ → SCL ↓	$t_{HD;STA}$	SCL0 SDA0		4.0	—	0.6	—	µs
SCL clock "L" width	t_{LOW}	SCL0		4.7	—	1.3	—	µs
SCL clock "H" width	t_{HIGH}	SCL0		4.0	—	0.6	—	µs
(Repeat) Start condition setup time SCL ↑ → SDA ↓	$t_{SU;STA}$	SCL0 SDA0		4.7	—	0.6	—	µs
Data hold time SCL ↓ → SDA ↓ ↑	$t_{HD;DAT}$	SCL0 SDA0		0	3.45*2	0	0.9*3	µs
Data setup time SDA ↓ ↑ → SCL ↑	$t_{SU;DAT}$	SCL0 SDA0		0.25	—	0.1	—	µs
Stop condition setup time SCL ↑ → SDA ↑	$t_{SU;STO}$	SCL0 SDA0		4	—	0.6	—	µs
Bus free time between stop condition and start condition	t_{BUF}	SCL0 SDA0		4.7	—	1.3	—	µs

*1 : R, C : Pull-up resistor and load capacitor of the SCL and SDA lines.

*2 : The maximum $t_{HD;DAT}$ have only to be met if the device dose not stretch the "L" width (t_{LOW}) of the SCL signal.

*3 : A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement $t_{SU;DAT} \geq$ 250 ns must then be met.



(Vcc = 5.0 V ± 10%, AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condition	Value*2		Unit	Remarks
				Min	Max		
SCL clock “L” width	t_{LOW}	SCL0	R = 1.7 kΩ, C = 50 pF*1	(2 + nm / 2) t_{MCLK} – 20	—	ns	Master mode
SCL clock “H” width	t_{HIGH}	SCL0		(nm / 2) t_{MCLK} – 20	(nm / 2) t_{MCLK} + 20	ns	Master mode
Start condition hold time	$t_{HD;STA}$	SCL0 SDA0		(–1 + nm / 2) t_{MCLK} – 20	(–1 + nm) t_{MCLK} + 20	ns	Master mode Maximum value is applied when m, n = 1, 8. Otherwise, the minimum value is applied.
Stop condition setup time	$t_{SU;STO}$	SCL0 SDA0		(1 + nm / 2) t_{MCLK} – 20	(1 + nm / 2) t_{MCLK} + 20	ns	Master mode
Start condition setup time	$t_{SU;STA}$	SCL0 SDA0		(1 + nm / 2) t_{MCLK} – 20	(1 + nm / 2) t_{MCLK} + 20	ns	Master mode
Bus free time between stop condition and start condition	t_{BUF}	SCL0 SDA0		(2 nm + 4) t_{MCLK} – 20	—	ns	
Data hold time	$t_{HD;DAT}$	SCL0 SDA0		3 t_{MCLK} – 20	—	ns	Master mode
Data setup time	$t_{SU;DAT}$	SCL0 SDA0		(–2 + nm / 2) t_{MCLK} – 20	(–1 + nm / 2) t_{MCLK} + 20	ns	Master mode When assuming that “L” of SCL is not extended, the minimum value is applied to first bit of continuous data. Otherwise, the maximum value is applied.
Setup time between clearing interrupt and SCL rising	$t_{SU;INT}$	SCL0		(nm / 2) t_{MCLK} – 20	(1 + nm / 2) t_{MCLK} + 20	ns	Minimum value is applied to interrupt at 9th SCL↓. Maximum value is applied to interrupt at 8th SCL↓.
SCL clock “L” width	t_{LOW}	SCL0		4 t_{MCLK} – 20	—	ns	At reception
SCL clock “H” width	t_{HIGH}	SCL0		4 t_{MCLK} – 20	—	ns	At reception
Start condition detection	$t_{HD;STA}$	SCL0 SDA0		2 t_{MCLK} – 20	—	ns	Undetected when 1 t_{MCLK} is used at reception
Stop condition detection	$t_{SU;STO}$	SCL0 SDA0		2 t_{MCLK} – 20	—	ns	Undetected when 1 t_{MCLK} is used at reception
Restart detection condition	$t_{SU;STA}$	SCL0 SDA0		2 t_{MCLK} – 20	—	ns	Undetected when 1 t_{MCLK} is used at reception
Bus free time	t_{BUF}	SCL0 SDA0		2 t_{MCLK} – 20	—	ns	At reception
Data hold time	$t_{HD;DAT}$	SCL0 SDA0		2 t_{MCLK} – 20	—	ns	At slave transmission mode
Data setup time	$t_{SU;DAT}$	SCL0 SDA0		t_{LOW} – 3 t_{MCLK} – 20	—	ns	At slave transmission mode

(Continued)

(Continued)

(Vcc = 5.0 V ± 10%, AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Sym-bol	Pin name	Condition	Value*2		Unit	Remarks
				Min	Max		
Data hold time	$t_{HD;DAT}$	SCL0 SDA0	R = 1.7 kΩ, C = 50 pF*1	0	—	ns	At reception
Data setup time	$t_{SU;DAT}$	SCL0 SDA0		t_{MCLK} − 20	—	ns	At reception
SDA↓→SCL↑ (at wake-up function)	t_{WAKEUP}	SCL0 SDA0		Oscillation stabilization wait time + 2 t_{MCLK} − 20	—	ns	

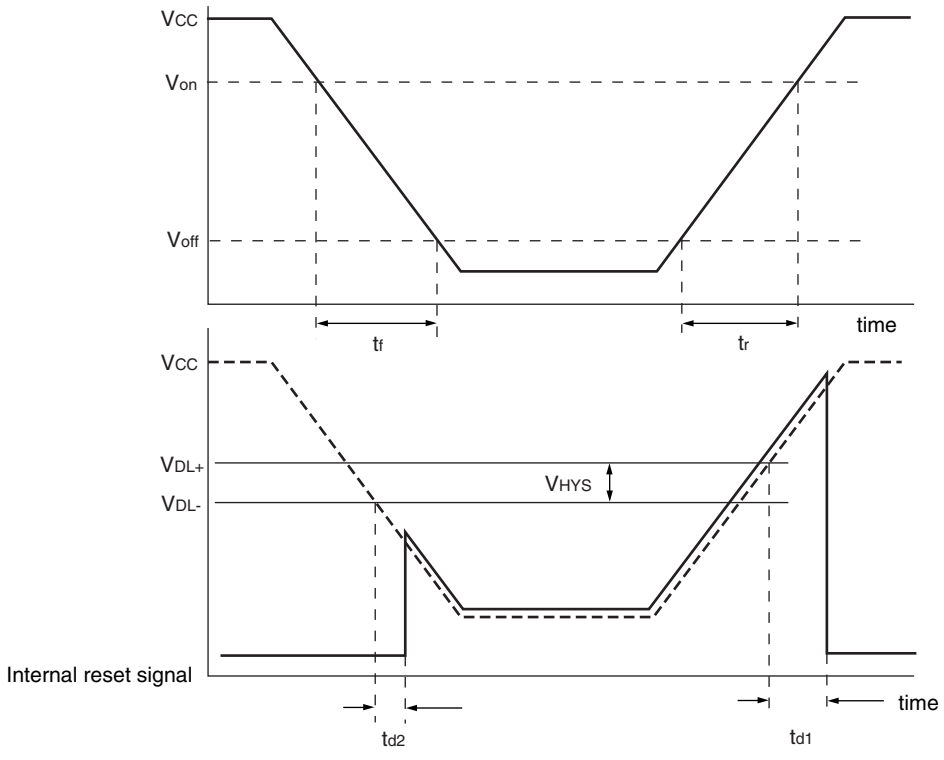
*1 : R, C : Pull-up resistor and load capacitor of the SCL and SDA lines.

*2 :
- Refer to " (2) Source Clock/Machine Clock" for t_{MCLK}.
- m is CS4 bit and CS3 bit (bit 4 and bit 3) of clock control register (ICCR0) .
- n is CS2 bit to CS0 bit (bit 2 to bit 0) of clock control register (ICCR0) .
- Actual timing of I²C is determined by m and n values set by the machine clock (t_{MCLK}) and CS4 to CS0 of ICCR0 register.
- Standard-mode :
  m and n can be set at the range : 0.9 MHz < t_{MCLK} (machine clock) < 10 MHz.
  Setting of m and n limits the machine clock that can be used below.
  (m, n) = (1, 8) : 0.9 MHz < t_{MCLK} ≤ 1 MHz
  (m, n) = (1, 22) , (5, 4) , (6, 4) , (7, 4) , (8, 4) : 0.9 MHz < t_{MCLK} ≤ 2 MHz
  (m, n) = (1, 38) , (5, 8) , (6, 8) , (7, 8) , (8, 8) : 0.9 MHz < t_{MCLK} ≤ 4 MHz
  (m, n) = (1, 98) : 0.9 MHz < t_{MCLK} ≤ 10 MHz
- Fast-mode :
  m and n can be set at the range : 3.3 MHz < t_{MCLK} (machine clock) < 10 MHz.
  Setting of m and n limits the machine clock that can be used below.
  (m, n) = (1, 8) : 3.3 MHz < t_{MCLK} ≤ 4 MHz
  (m, n) = (1, 22) , (5, 4) : 3.3 MHz < t_{MCLK} ≤ 8 MHz
  (m, n) = (6, 4) : 3.3 MHz < t_{MCLK} ≤ 10 MHz

(9) Low Voltage Detection

(AVss = Vss = 0.0 V, T_A = –40 °C to + 85 °C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Release voltage	V_{DL+}	2.52	2.70	2.88	V	At power-supply rise
Detection voltage	V_{DL-}	2.42	2.60	2.78	V	At power-supply fall
Hysteresis width	V_{HYS}	70	100	—	mV	
Power-supply start voltage	V_{off}	—	—	2.3	V	
Power-supply end voltage	V_{on}	4.9	—	—	V	
Power-supply voltage change time (at power supply rise)	t_r	0.3	—	—	µs	Slope of power supply that reset release signal generates
		—	3000	—	µs	Slope of power supply that reset release signal generates within rating (V_{DL+})
Power-supply voltage change time (at power supply fall)	t_f	300	—	—	µs	Slope of power supply that reset detection signal generates
		—	300	—	µs	Slope of power supply that reset detection signal generates within rating (V_{DL-})
Reset release delay time	t_{d1}	—	—	400	µs	
Reset detection delay time	t_{d2}	—	—	30	µs	
Current consumption	I_{LVD}	—	38	50	µA	Current consumption for low voltage detection circuit only



(10) Clock Supervisor Clock

(Vcc = AVcc = 5.0 V ± 10%, AVss = Vss = 0.0 V, T_A = –40 °C to + 85 °C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Oscillation frequency	f_{OUT}	50	100	200	kHz	
Oscillation start time	t_{wk}	—	—	10	µs	
Current consumption	I_{CSV}	—	20	36	µA	Current consumption of built-in CR oscillator, at oscillation of 100 kHz

5. A/D Converter

(1) A/D Converter Electrical Characteristics

(AVcc = Vcc = 4.0 V to 5.5 V, AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

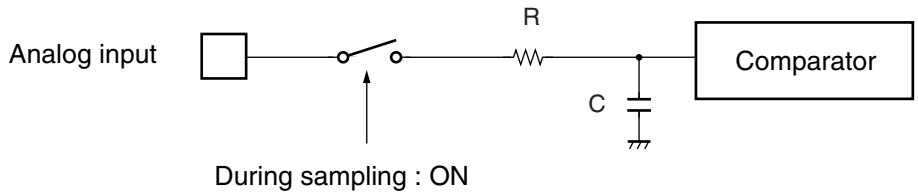
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	10	bit	
Total error		− 3.0	—	+ 3.0	LSB	
Linearity error		− 2.5	—	+ 2.5	LSB	
Differential linear error		− 1.9	—	+ 1.9	LSB	
Zero transition voltage	V_{OT}	AVss − 1.5 LSB	AVss + 0.5 LSB	AVss + 2.5 LSB	V	
Full-scale transition voltage	V_{FST}	AVR − 3.5 LSB	AVR − 1.5 LSB	AVR + 0.5 LSB	V	
Compare time	—	0.9	—	16500	µs	4.5 V ≤ AVcc ≤ 5.5 V
		1.8	—	16500	µs	4.0 V ≤ AVcc < 4.5 V
Sampling time	—	0.6	—	∞	µs	4.5 V ≤ AVcc ≤ 5.5 V, At external impedance < 5.4 kΩ
		1.2	—	∞	µs	4.0 V ≤ AVcc < 4.5 V, At external impedance < 2.4 kΩ
Analog input current	I_{AIN}	− 0.3	—	+ 0.3	µA	
Analog input voltage	V_{AIN}	AVss	—	AVR	V	
Reference voltage	—	AVss + 4.0	—	AVcc	V	AVR pin
Reference voltage supply current	I_R	—	600	900	µA	AVR pin, During A/D operation
	I_{RH}	—	—	5	µA	AVR pin, At stop mode

(2) Notes on Using A/D Converter

- **About the external impedance of analog input and its sampling time**

A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. Also, if the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

- Analog input equivalent circuit

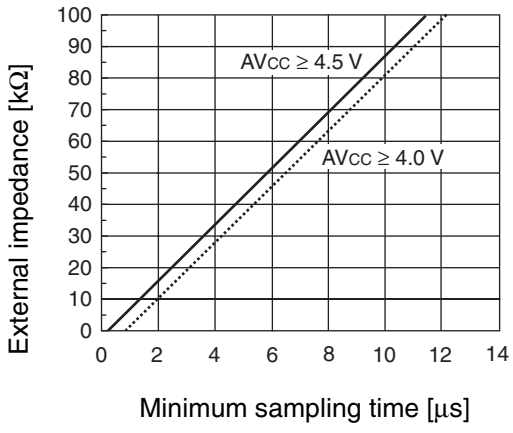


	R	C
4.5 V ≤ AVcc ≤ 5.5 V	2.0 kΩ (Max)	16 pF (Max)
4.0 V ≤ AVcc < 4.5 V	8.2 kΩ (Max)	16 pF (Max)

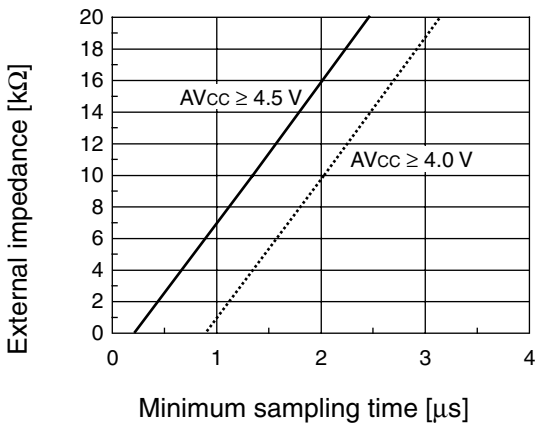
Note : The values are reference values.

- The relationship between external impedance and minimum sampling time

(External impedance = 0 kΩ to 100 kΩ)



(External impedance = 0 kΩ to 20 kΩ)

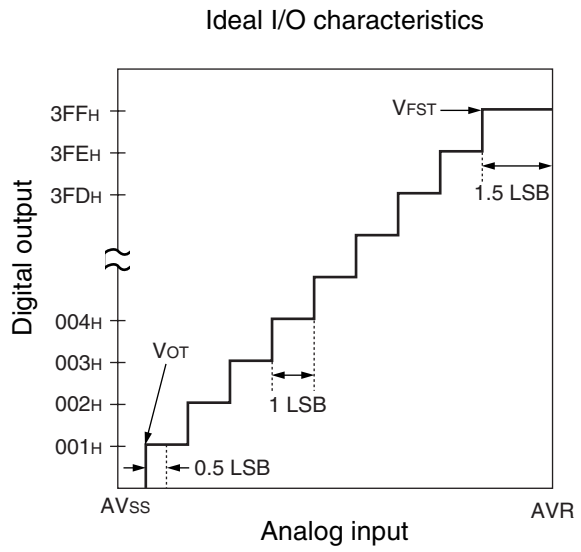


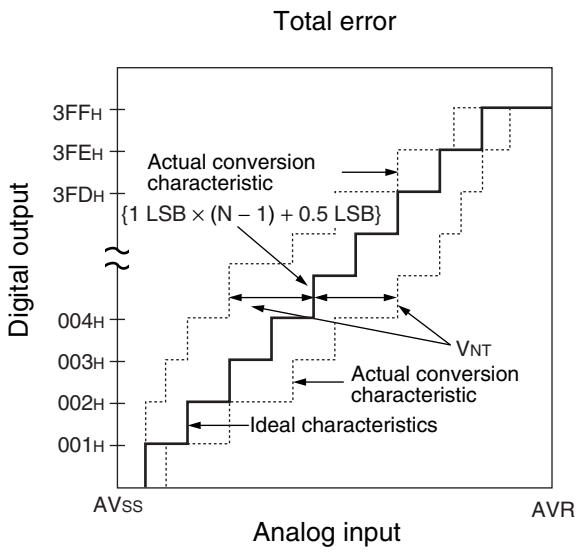
- **About errors**

As |AVR - AVSS| becomes smaller, values of relative errors grow larger.

(3) Definition of A/D Converter Terms

- Resolution
  The level of analog variation that can be distinguished by the A/D converter.
  When the number of bits is 10, analog voltage can be divided into $2^{10} = 1024$.
- Linearity error (unit : LSB)
  The deviation between the value along a straight line connecting the zero transition point (“00 0000 0000” ← → “00 0000 0001”) of a device and the full-scale transition point (“11 1111 1111” ← → “11 1111 1110”) compared with the actual conversion values obtained.
- Differential linear error (Unit : LSB)
  Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
- Total error (unit: LSB)
  Difference between actual and theoretical values, caused by a zero transition error, full-scale transition error, linearity error, quantum error, and noise.





$$1\ \text{LSB} = \frac{\text{AVR} - \text{AVss}}{1024}\ \text{(V)}$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (\text{N} - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ \text{[LSB]}$$

N : A/D converter digital output value
V_{NT} : A voltage at which digital output transits from (N – 1) to N.

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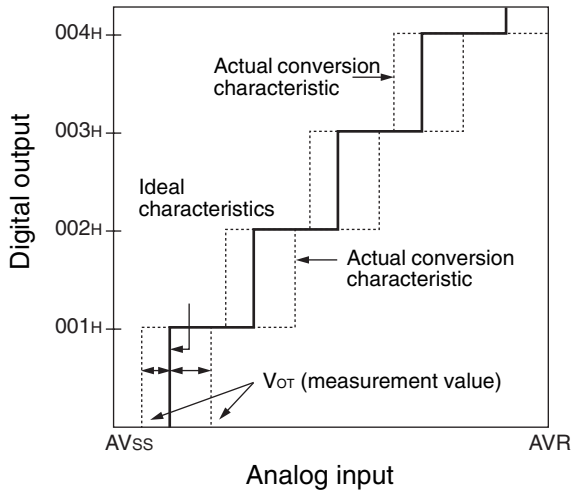
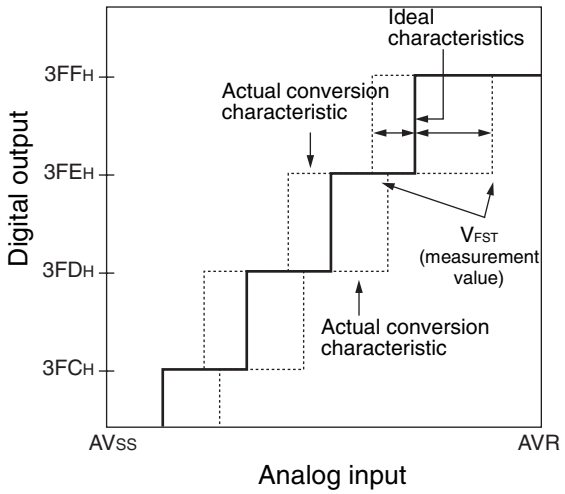
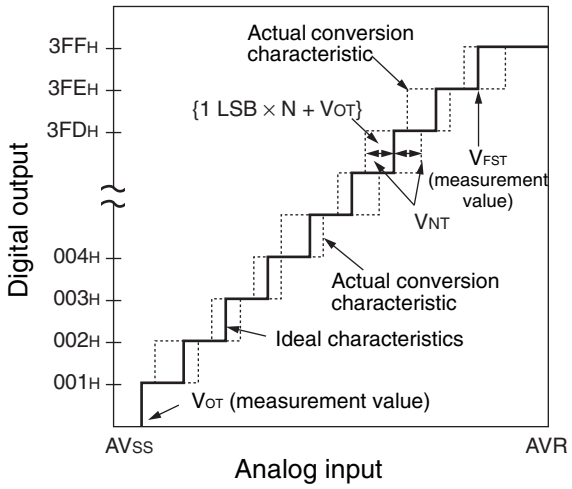
Zero transition error



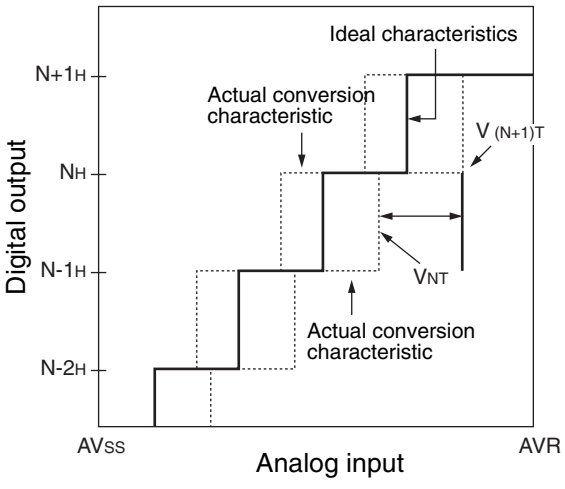
Full-scale transition error



Linearity error



Differential linear error



$$\text{Linearity error in digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times N + V_{OT}\}}{1\ \text{LSB}}$$

$$\text{Differential linear error in digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1$$

N : A/D converter digital output value
V_{NT} : A voltage at which digital output transits from (N – 1) to N.
V_{OT} (Ideal value) = AV_{SS} + 0.5 LSB [V]
V_{FST} (Ideal value) = AVR – 1.5 LSB [V]

6. Flash Memory Program/Erase Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time (4 Kbytes sector)	—	0.2*1	0.5*2	s	Excludes 00_H programming prior erasure.
Sector erase time (16 Kbytes sector)	—	0.5*1	7.5*2	s	Excludes 00_H programming prior erasure.
Byte programming time	—	32	3,600	µs	Excludes system-level overhead.
Erase/program cycle	10000	—	—	cycle	
Power supply voltage at erase/ program	4.5	—	5.5	V	
Flash memory data retention time	20*3	—	—	year	Average T_A = +85 °C

*1 : T_A = + 25 °C, V_{CC} = 5.0 V, 10000 cycles

*2 : T_A = + 85 °C, V_{CC} = 4.5 V, 10000 cycles

*3 : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at +85 °C) .

■ MASK OPTION

No.	Part number	MB95108AM	MB95F104AMS MB95F104ANS MB95F104AJS MB95F106AMS MB95F106ANS MB95F106AJS MB95F108AMS MB95F108ANS MB95F108AJS	MB95F104AMW MB95F104ANW MB95F104AJW MB95F106AMW MB95F106ANW MB95F106AJW MB95F108AMW MB95F108ANW MB95F108AJW	MB95FV100D-103
	Specifying procedure	**Specify when ordering MASK**	**Setting disabled**	**Setting disabled**	**Setting disabled**
1	Clock mode select • Single-system clock mode • Dual-system clock mode	Selectable	Single-system clock mode	Dual-system clock mode	Changing by the switch on MCU board
2	Low voltage detection reset* • With low voltage detection reset • Without low voltage detection reset	Specify when ordering MASK	Specified by part number	Specified by part number	Changing by the switch on MCU board
3	Clock supervisor* • With clock supervisor • Without clock supervisor	Specify when ordering MASK	Specified by part number	Specified by part number	Changing by the switch on MCU board
4	Reset output* • With reset output • Without reset output	Specify when ordering MASK	Specified by part number	Specified by part number	MCU board switch set as following ; • With supervisor : Without reset output • Without supervisor : With reset output
5	Oscillation stabilization wait time	Fixed to oscillation stabilization wait time of $(2^{14}-2)/F_{CH}$	Fixed to oscillation stabilization wait time of $(2^{14}-2)/F_{CH}$	Fixed to oscillation stabilization wait time of $(2^{14}-2)/F_{CH}$	Fixed to oscillation stabilization wait time of $(2^{14}-2)/F_{CH}$

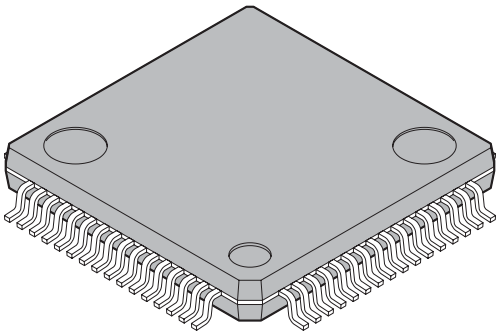
* : Refer to table below about clock mode select, low voltage detection reset, clock supervisor select and reset output.

Part number	Clock mode select	Low voltage detection reset	Clock supervisor	Reset output
MB95108AM	Single-system	No	No	Yes
		Yes	No	Yes
		Yes	Yes	No
	Dual-system	No	No	Yes
		Yes	No	Yes
		Yes	Yes	No
MB95F104AMS	Single-system	No	No	Yes
MB95F104ANS		Yes	No	Yes
MB95F104AJS		Yes	Yes	No
MB95F106AMS		No	No	Yes
MB95F106ANS		Yes	No	Yes
MB95F106AJS		Yes	Yes	No
MB95F108AMS		No	No	Yes
MB95F108ANS		Yes	No	Yes
MB95F108AJS		Yes	Yes	No
MB95F104AMW	Dual-system	No	No	Yes
MB95F104ANW		Yes	No	Yes
MB95F104AJW		Yes	Yes	No
MB95F106AMW		No	No	Yes
MB95F106ANW		Yes	No	Yes
MB95F106AJW		Yes	Yes	No
MB95F108AMW		No	No	Yes
MB95F108ANW		Yes	No	Yes
MB95F108AJW		Yes	Yes	No
MB95FV100D-103	Single-system	No	No	Yes
		Yes	No	Yes
		Yes	Yes	No
	Dual-system	No	No	Yes
		Yes	No	Yes
		Yes	Yes	No

■ ORDERING INFORMATION

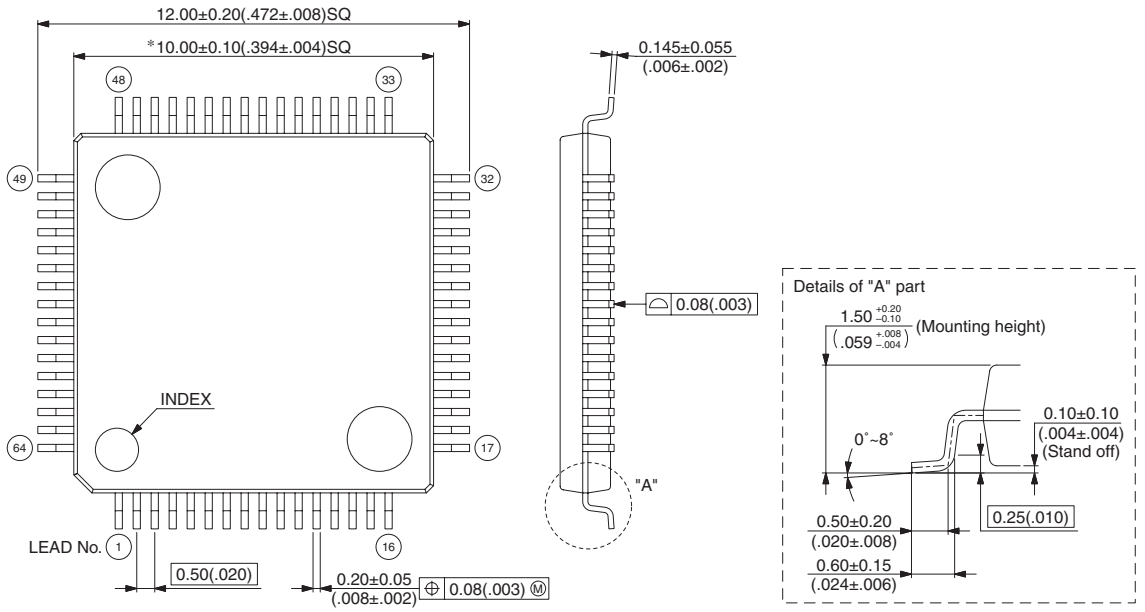
Part number	Package
MB95108AMPFV MB95F104AMSPFV/F104ANSPFV/F104AJSPFV MB95F104AMWPFV/F104ANWPFV/F104AJWPFV MB95F106AMSPFV/F106ANSPFV/F106AJSPFV MB95F106AMWPFV/F106ANWPFV/F106AJWPFV MB95F108AMSPFV/F108ANSPFV/F108AJSPFV MB95F108AMWPFV/F108ANWPFV/F108AJWPFV	64-pin plastic LQFP (FPT-64P-M03)
MB95108AMPFM MB95F104AMSPFM/F104ANSPFM/F104AJSPFM MB95F104AMWPFM/F104ANWPFM/F104AJWPFM MB95F106AMSPFM/F106ANSPFM/F106AJSPFM MB95F106AMWPFM/F106ANWPFM/F106AJWPFM MB95F108AMSPFM/F108ANSPFM/F108AJSPFM MB95F108AMWPFM/F108ANWPFM/F108AJWPFM	64-pin plastic LQFP (FPT-64P-M09)
MB2146-303 (MB95FV100D-103PBT)	MCU board (224-pin plastic PFBGA (BGA-224P-M08))

■ PACKAGE DIMENSIONS

64-pin plastic LQFP		
 (FPT-64P-M03)	Lead pitch	0.50 mm
	Package width × package length	10.0 × 10.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.32g
	Code (Reference)	P-LFQFP64-10×10-0.50

64-pin plastic LQFP
(FPT-64P-M03)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

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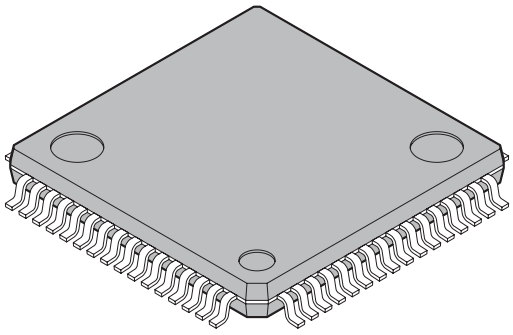
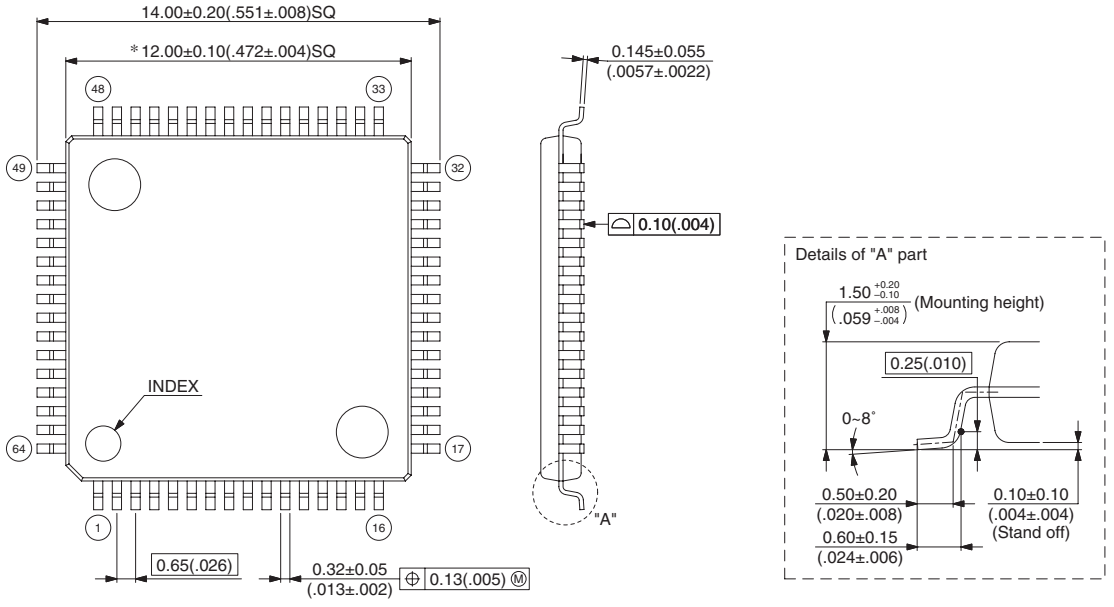
64-pin plastic LQFP		
 (FPT-64P-M09)	Lead pitch	0.65 mm
	Package width × package length	12 × 12 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Code (Reference)	P-LQFP64-12×12-0.65

64-pin plastic LQFP
(FPT-64P-M09)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.
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■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
—	—	Added the part numbers. (MB95F104AJS/MB95F104AJW MB95F106AJS/MB95F106AJW MB95F108AJS/MB95F108AJW)
4	■ PRODUCT LINEUP	Added the description "Clock supervisor" in the section "Option".
18	■ PROGRAMMING FLASH MEMORY MICROCONTROLLERS USING PARALLEL PROGRAMMER	Inserted "• Programming Method".
31	■ I/O MAP	Added the address 0FEA$_H$.
35	2. Recommended Operating Conditions	"Verified the Min value in the section of "Other than MB95FV100D-103", "In normal operating" of "Power supply voltage"; 2.45 → 2.42.
		Verified the value in *1; 2.9 V → 2.88 V.
		Moved “H” level input voltage and “L” level input voltage to the section "3. DC Characteristics".
36	3. DC Characteristics	Added the pin name at the "Pin name" in the section of V_{IHA}, “H” level input voltage.
		Added the pin name at the "Pin name" in the section of V_{ILA}, “L” level input voltage.
39		Deleted the line of "F_{CH} = 16 MHz" in the section "I_{CTS}" of Power supply current.
40	4. AC Characteristics (1) Clock Timing	Changed in the table; V_{CC} = 2.5 V to 5.5 V → V_{CC} = 2.42 V to 5.5 V.
		Changed the Max value on the third column of the clock frequency; 16.25 → 10.00
45	4. AC Characteristics (2) Source Clock/Machine Clock	Verified the diagram of Main PLL operation frequency range.
59	(9) Low Voltage Detection	Changed the release voltage: 2.55 → 2.52 (Min value) 2.85 → 2.88 (Max value)
		Changed the detection voltage: 2.45 → 2.42 (Min value) 2.75 → 2.78 (Max value)

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Edited Strategic Business Development Dept.