Large Current External FET Controller Type Switching Regulator

Dual-output, high voltage, high-efficiency step-down switching controller

BD9012KV

●Overview

The BD9012KV is a 2-ch synchronous controller with rectification switching for enhanced power management efficiency. It supports a wide input range, enabling low power consumption ecodesign for an array of electronics.

●Features

1) Wide input voltage range: 4.5V to 30V
2) Precision voltage references: 0.8V±1%
3) FET direct drive
4) Rectification switching for increased efficiency
5) Variable frequency: 250k to 1200kHz (external synchronization to 1200kHz)
6) Built-in selected auto remove over current protection
7) Built-in independent power up/power down sequencing control
8) Make various application , step-down , step-up and step-up-down
9) Small footprint packages: VQFP48C

●Applications

Car audio and navigation systems, CRTTV, LCDTV, PDPTV, STB, DVD, and PC systems, portable CD and DVD players, etc.

●Absolute Maximum Ratings (Ta=25℃)

Parameter	Symbol	Limits	Unit	Parameter	Symbol	Limits	Unit
VCC Voltage	VCC	34 *1	V	VREG33 Voltage	VREG33	VREG5	V
EXTVCC Voltage	EXTVCC	34 *1	V	SS1,2、FB1,2 Voltage	SS1,2、FB1,2		
VCCCL1,2 Voltage	VCCCL1,2	34	V	COMP1,2 Voltage	COMP1,2		
CL1,2 Voltage	CL1,2	34	V	DET1,2 Voltage	DET1,2		
SW1,2 Voltage	SW1,2	34 *1	V	RT、SYNC Voltage	RT、SYNC		
BOOT1,2 Voltage	BOOT1,2	40 *1	V	Power Dissipation	Pd	1.1 *2	W
BOOT1,2-SW1,2 Voltage	BOOT1,2 -SW1,2	7 *1	V	Operating Temperature Range	Topr	-40 to +105	℃
STB, EN1,2 Voltage	STB, EN1,2	VCC	V	Storage Temperature Range	Tstg	-55 to +150	℃
VREG5,5A Voltage	VREG5,5A	7 *1	V	Maximum Junction Temperature	Tj	+150	℃

*1 Regardless of the listed rating, do not exceed Pd in any circumstances.

*2 Pd de-rated at 7mW/℃ for temperature above Ta=25℃, Mounted on PCB 70mm×70mm×1.6mm.

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●Operating conditions (Ta=25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input voltage 1	EXTVCC	4.5 *1 *2	12	30	V
Input voltage 2	VCC	4.5 *1 *2	12	30	V
BOOT－SW voltage	BOOT－SW	4.5	5	VREG5	V
Carrier frequency	OSC	250	300	1200	kHz
Synchronous frequency	SYNC	OSC	-	1200*3*4	kHz
Synchronous pulse duty	Duty	40	50	60	%
Min OFF pulse	TMIN	-	150	-	nsec

★This product is not designed to provide resistance against radiation.

*1 After more than 4.5V, voltage range.

*2 In case of using less than 6V, Short to VCC, EXTVCC and VREG5.

*3 Please do not exceed OSC×1.5.

*4 Do not do such things as switching over to internal oscillating frequency while external synchronization frequency is used.

●Electrical characteristics (Unless otherwise specified, Ta=25℃ VCC=12V STB=5V EN1,2=5V)

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
VIN bias current	IIN	-	6	10	mA	
Shutdown mode current	IST	-	0	10	μA	VSTB=0V
［Error Amp Block］						
Feedback reference voltage	VOB	0.792	0.800	0.808	V	
Feedback reference voltage (Ta=-40 to 105℃)	VOB+	0.784	0.800	0.816	V	Ta=-40 to 105℃ ※
Open circuit voltage gain	Averr	-	46	-	dB	
VO input bias current	IVo+	-	-	1	μA	
［Oscillator］						
Carrier frequency	FOSC	900	1000	1100	kHz	RT=27 kΩ
Synchronous frequency	Fsync	-	1200	-	kHz	RT=27 kΩ,SYNC=1200kHz
［Over Current Protection Block］						
CL threshold voltage	Vswth	70	90	110	mV	
CL threshold voltage （Ta=-40 to 105℃）	Vswth+	67	90	113	mV	Ta=-40 to 105℃ ※
［VREG Block］						
VREG5 output voltage	VREG5	4.8	5	5.2	V	IREF=6mA
VREG33 reference voltage	VREG33	3.0	3.3	3.6	V	IREG=6mA
VREG5 threshold voltage	VREG_UVLO	2.6	2.8	3.0	V	VREG:Sweep down
VREG5 hysteresis voltage	DVREG_UVLO	50	100	200	mV	VREG:Sweep up
［Soft start block］						
Charge current	ISS	6.5	10	13.5	μA	VSS=1V
Charge current (Ta=-40 to 105℃)	ISS+	6	10	14	μA	VSS=1V,Ta=-40 to 105℃ ※

Note: Not all shipped products are subject to outgoing inspection.

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●Reference data (Unless otherwise specified, Ta=25℃)

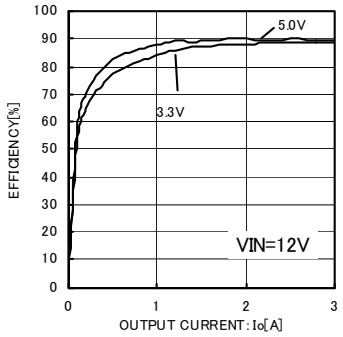

Fig.1 Efficiency 1

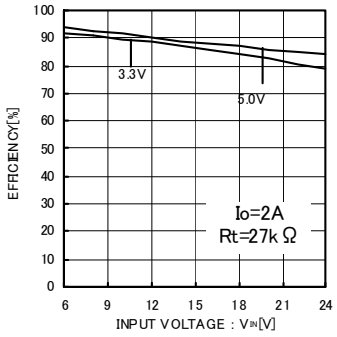

Fig.2 Efficiency 2

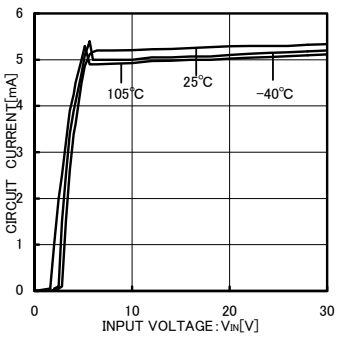

Fig.3 Circuit current

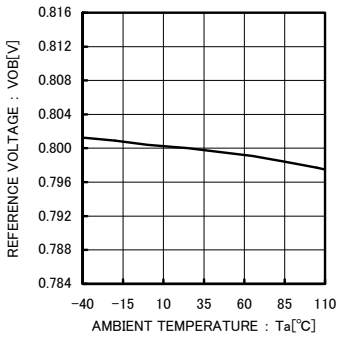

Fig.4 Reference voltage vs. temperature characteristics

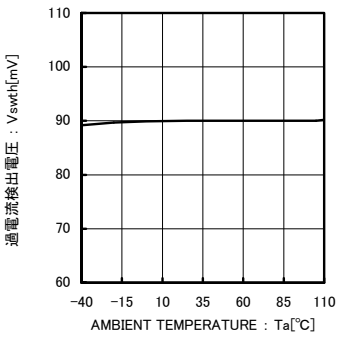

Fig.5 Over current detection vs. temperature characteristics

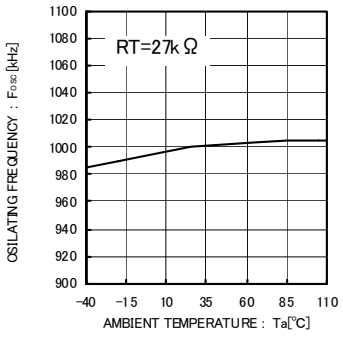

Fig.6 Frequency vs. temperature characteristics

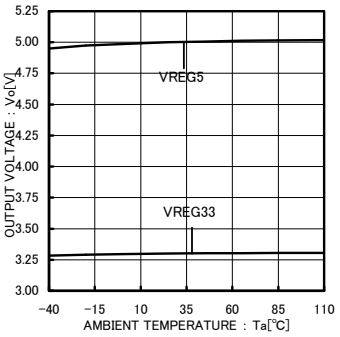

Fig.7 Internal Reg vs. temperature characteristics

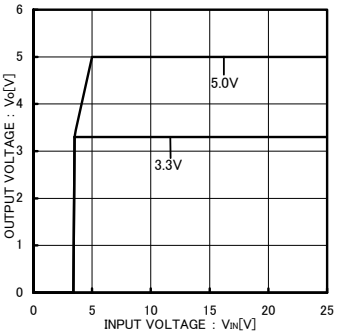

Fig.8 Line regulation

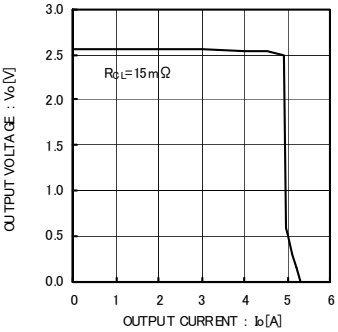

Fig.9 Load regulation

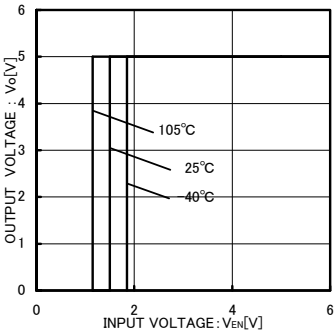

Fig.10 EN threshold voltage

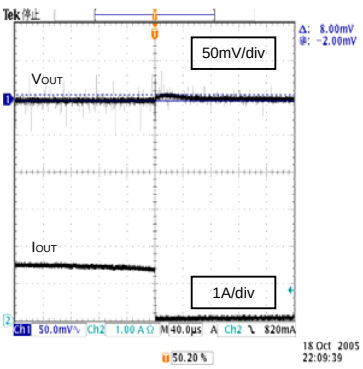

Fig.11 Load transient response 1

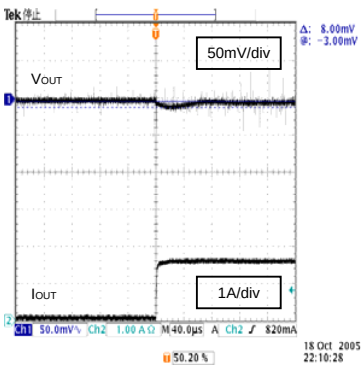

Fig.12 Load transient response 2

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●Block diagram

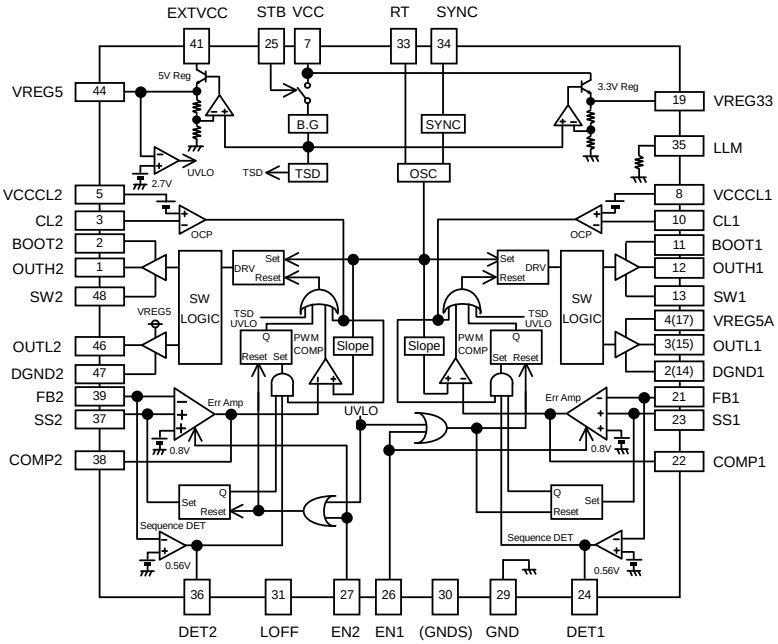

Fig-13

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●Pin configuration

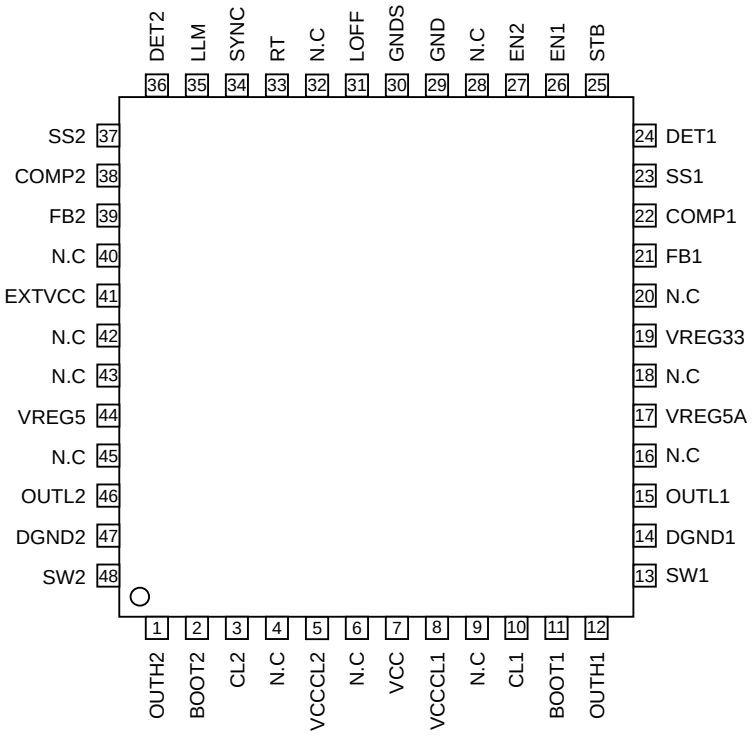

Fig-15

●Pin function table

Pin No.	Pin name	Function
1	OUTH2	High side FET gate drive pin 2
2	BOOT2	OUTH2 driver power pin
3	CL2	Over current detection pin 2
4	N.C	Non-connect (unused) pin
5	VCCCL2	Over current detection VCC2
6	N.C	Non-connect (unused) pin
7	VCC	Input power pin
8	VCCCL1	Over current detection CC1
9	N.C	Non-connect (unused) pin
10	CL1	Over current detection setting pin 1
11	BOOT1	OUTH1 driver power pin
12	OUTH1	High side FET gate drive pin 1
13	SW1	High side FET source pin 1
14	DGND1	Low side FET source pin 1
15	OUTL1	Low side FET gate drive pin 1
16	N.C	Non-connect (unused) pin
17	VREG5A	FET drive REG input
18	N.C	Non-connect (unused) pin
19	VREG33	Reference input REG output
20	N.C	Non-connect (unused) pin
21	FB1	Error amp input 1
22	COMP1	Error amp output 1
23	SS1	Soft start setting pin 1
24	DET1	FB detector output 1
25	STB	Standby ON/OFF pin
26	EN1	Output 1 ON/OFF pin
27	EN2	Output 2 ON/OFF pin
28	N.C	Non-connect (unused) pin
29	GND	Ground
30	GNDS	Sense ground
31	LOFF	Test Mode Terminal
32	N.C	Non-connect (unused) pin
33	RT	Switching frequency setting pin
34	SYNC	External synchronous pulse input pin
35	LLM	Built-in pull-down resistor pin
36	DET2	FB detector output 2
37	SS2	Soft start setting pin 2
38	COMP2	Error amp output 2
39	FB2	Error amp input 2
40	N.C	Non-connect (unused) pin
41	EXTVCC	External power input pin
42	N.C	Non-connect (unused) pin
43	N.C	Non-connect (unused) pin
44	VREG5	FET drive REG output
45	N.C	Non-connect (unused) pin
46	OUTL2	Low side FET gate drive pin 2
47	DGND2	Low side FET source pin 2
48	SW2	High side FET source pin 2

●Block functional descriptions

・Error amp
The error amp compares output feedback voltage to the 0.8V reference voltage and provides the comparison result as COMP voltage, which is used to determine the switching Duty. COMP voltage is limited to the SS voltage, since soft start at power up is based on SS pin voltage.

・Oscillator (OSC)
Oscillation frequency is determined by the switching frequency pin (RT) in this block. The frequency can be set between 250kHz and 550kHz.

・SLOPE
The SLOPE block uses the clock produced by the oscillator to generate a triangular wave, and sends the wave to the PWM comparator.

・PWM COMP
The PWM comparator determines switching Duty by comparing the COMP voltage, output from the error amp, with the triangular wave from the SLOPE block. Switching duty is limited to a percentage of the internal maximum duty, and thus cannot be 100% of the maximum.

・Reference voltage (5Vreg, 33Vreg)
This block generates the internal reference voltages: 5V and 3.3V.

・External synchronization (SYNC)
Determines the switching frequency, based on the external pulse applied.

・Over current protection (OCP)
Over current protection is activated when the VCCCL-CL voltage reaches or exceeds 90mV. When over current protection is active, Duty is low, and output voltage also decreases. When LOFF=L, the output voltage has fallen to 70% or below and output is latched OFF. The OFF latch mode ends when the latch is set to STB, EN.

・Sequence control (Sequence DET)
Compares FB voltage with reference voltage (0.56V) and outputs the result as DET.

・Protection circuits (UVLO/TSD)
The UVLO lock out function is activated when VREG falls to about 2.8V, while TSD turns outputs OFF when the chip temperature reaches or exceeds 150℃. Output is restored when temperature falls back below the threshold value.

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●Application circuit example (Parentheses indicate VQFP48C pin numbers)

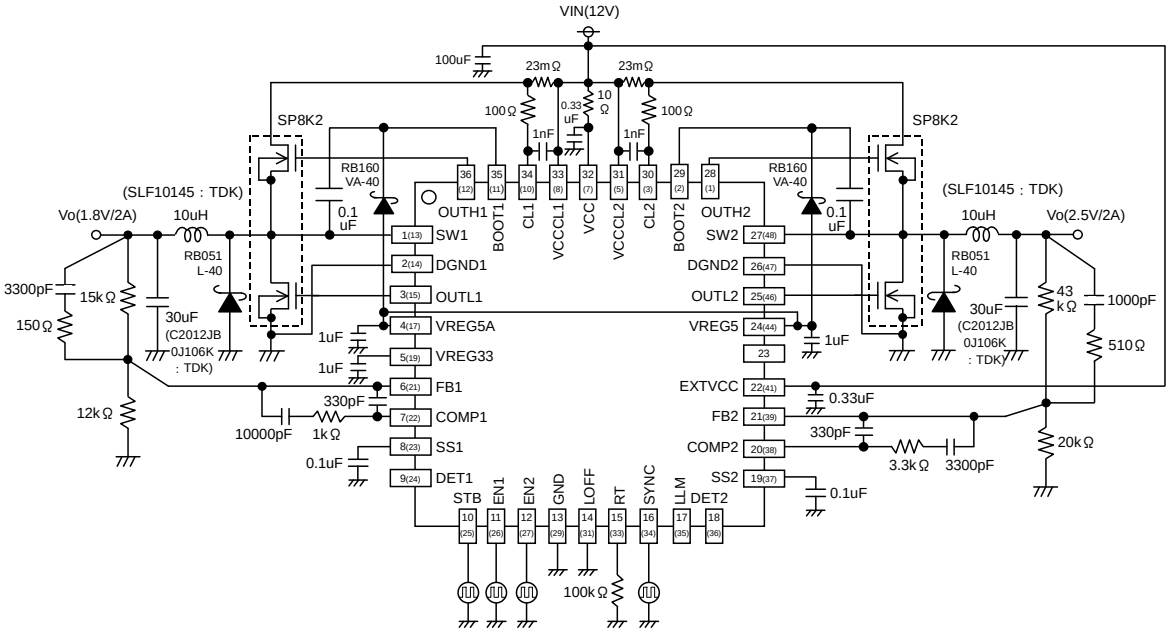

Fig-16B（Step-Down：Cout=Ceramic Capacitor）

There are many factors(The PCB board layout, Output Current, etc.)that can affect the DCDC characteristics. Please verify and confirm using practical applications.

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●Application component selection

(1) Setting the output L value

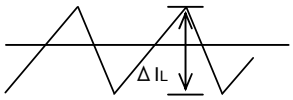

Fig-17

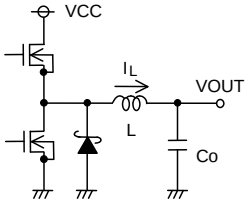

Fig-18

Output ripple current

The coil value significantly influences the output ripple current. Thus, as seen in equation (5), the larger the coil, and the higher the switching frequency, the lower the drop in ripple current.

$$\Delta IL = \frac{(VCC-VOUT) \times VOUT}{L \times VCC \times f} \quad [A] \cdots (5)$$

The optimal output ripple current setting is 30% of maximum current.

$\Delta IL = 0.3 \times IOUTmax.[A] \cdots (6)$

$$L = \frac{(VCC-VOUT) \times VOUT}{\Delta IL \times VCC \times f} \quad [H] \cdots (7)$$

（ΔIL：output ripple current　f：switching frequency）

※Outputting a current in excess of the coil current rating will cause magnetic saturation of the coil and decrease efficiency.

Please establish sufficient margin to ensure that peak current does not exceed the coil current rating.

※Use low resistance (DCR, ACR) coils to minimize coil loss and increase efficiency.

(2) Setting the output capacitor Co value

Select the output capacitor with the highest value for ripple voltage (V_{PP}) tolerance and maximum drop voltage (at rapid load change). The following equation is used to determine the output ripple voltage.

Step down $\Delta V_{PP} = \Delta I_L \times R_{ESR} + \frac{\Delta I_L}{Co} \times \frac{Vo}{Vcc} \times \frac{1}{f}$ [V]　　Note: f：switching frequency

Be sure to keep the output Co setting within the allowable ripple voltage range.

※Please allow sufficient output voltage margin in establishing the capacitor rating. Note that low-ESR capacitors enable lower output ripple voltage.

Also, to meet the requirement for setting the output startup time parameter within the soft start time range, please factor in the conditions described in the capacitance equation (9) for output capacitors, below.

$$Co \leqq \frac{TSS \times (Limit - IOUT)}{VOUT} \quad \cdots (9)$$

Tss：　soft start time

ILimit：over current detection value（2/16）reference

Note: less than optimal capacitance values may cause problems at startup.

(3) Input capacitor selection

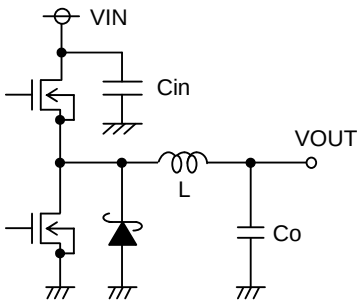

Fig-19

Input capacitor

The input capacitor serves to lower the output impedance of the power source connected to the input pin (VCC). Increased power supply output impedance can cause input voltage (VCC) instability, and may negatively impact oscillation and ripple rejection characteristics. Therefore, be certain to establish an input capacitor in close proximity to the VCC and GND pins. Select a low-ESR capacitor with the required ripple current capacity and the capability to withstand temperature changes without wide tolerance fluctuations. The ripple current IRMSS is determined using equation (10).

$$IRMS = IOUT \times \frac{\sqrt{VOUT\ (VCC - VOUT)}}{VCC} \quad [A] \cdots (10)$$

Also, be certain to ascertain the operating temperature, load range and MOSFET conditions for the application in which the capacitor will be used, since capacitor performance is heavily dependent on the application's input power characteristics, substrate wiring and MOSFET gate drain capacity.

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(4) Feedback resistor design

Please refer to the following equation in determining the proper feedback resistance. The recommended setting is in a range between 10kΩ and 330kΩ. Resistance less than 10kΩ risks decreased power efficiency, while setting the resistance value higher than 330kΩ will result in an internal error amp input bias current of 0.2uA increasing the offset voltage. Please use it with 150nsec or more so that there is a possibility that the output becomes unstable when the output pulse width is small. (12)

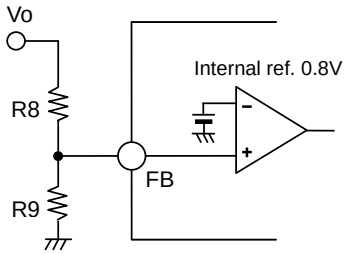

Fig-20

$$Vo = \frac{R8 + R9}{R9} \times 0.8\,[V] \quad \cdots (11)$$

$$\frac{Vo}{Vin} \times \frac{1}{f} \geqq 150ns \quad \cdots (12)$$

(5) Setting switching frequency

The triangular wave switching frequency can be set by connecting a resistor to the RT 15(33) pin. The RT sets the frequency by adjusting the charge/discharge current in relation to the internal capacitor. Refer to the figure below in determining proper RT resistance, noting that the recommended resistance setting is between 50kΩ and 130kΩ. Settings outside this range may render the switching function inoperable, and proper operation of the controller overall cannot be guaranteed when unsupported resistance values are used.

Fig-21 RT vs. switching frequency

(6) Setting the soft start delay

The soft start function is necessary to prevent an inrush of coil current and output voltage overshoot at startup. The figure below shows the relation between soft start delay time and capacitance, which can be calculated using equation (12) at right.

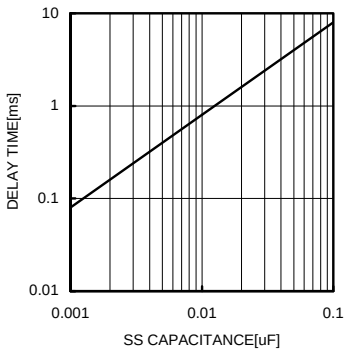

Fig-22 SS capacitance vs. delay time

$$TSS = \frac{0.8V(typ.) \times CSS}{ISS(10\,\mu A\ Typ.)}\ [sec] \quad \cdots (12)$$

Recommended capacitance values are between 0.01uF and 0.1uF. Capacitance lower than 0.01uF may generate output overshoots. Please use high accuracy components (such as X5R) when implementing sequential startups involving other power sources. Be sure to test the actual devices and applications to be used, since the soft start time varies, depending on input voltage, output voltage and capacitance, coils and other characteristics.

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(7) Setting over current detection values

The current limit value（ILimit）is determined by the resistance of the RCL established between CL and VCCCL.

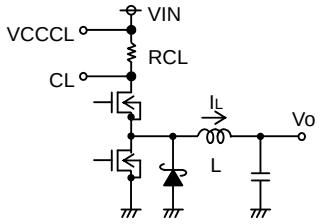

Fig-23

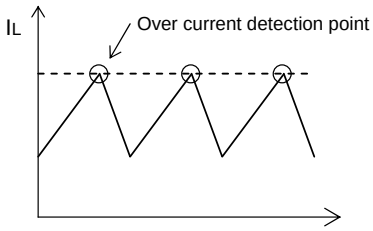

Fig-24

$$ILimit = \frac{90m}{RCL}\ [A] \cdot \cdot \cdot (13)$$

When the current goes beyond the threshold value, the current can be limited by reducing the ON Duty Cycle. When the load goes back to the normal operation, the output voltage also becomes back on to the specific level.

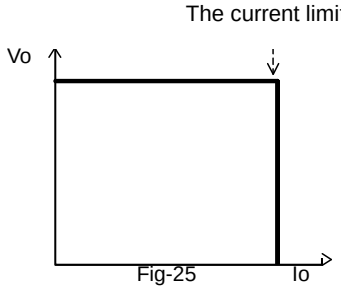

Fig-25

(8) Method for determining phase compensation

Conditions for application stability

Feedback stability conditions are as follows:

・When gain is 1 (0dB) and phase shift is 150° or less (i.e., phase margin is at least 30°):
a dual-output high-frequency step-down switching regulator is required

Additionally, in DC/DC applications, sampling is based on the switching frequency; therefore, overall GBW may be set at no more than 1/10 the switching frequency. In summary, target characteristics for application stability are:

・Phase shift of 150° or less (i.e., phase margin of 30° or more) with gain of 1 (0dB)

・GBW (i.e., gain 0dB frequency) no more than 1/10 the switching frequency.

Stability conditions mandate a relatively higher switching frequency, in order to limit GBW enough to increase response.

The key to achieving successful stabilization using phase compensation is to cancel the secondary phase margin/delay (-180°) generated by LC resonance, by employing a dual phase lead. In short, adding two phase leads stabilizes the application.

GBW (the frequency at gain 1) is determined by the phase compensation capacitor connected to the error amp. Thus, a larger capacitor will serve to lower GBW if desired.

① General use integrator (low-pass filter) ② Integrator open loop characteristics

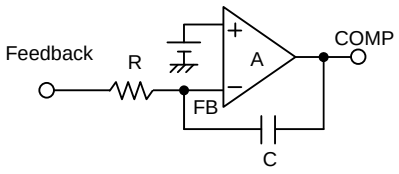

Fig-26

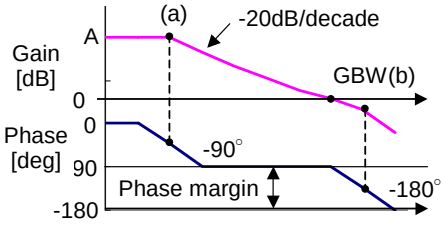

Fig-27

$$\text{point (a)}\quad fa = \frac{1}{2\pi RCA}\ 1.25[Hz]$$

$$\text{point (b)点}\quad fa = GBW\ \frac{1}{2\pi RC}\ [Hz]$$

The error amp is provided with phase compensation similar to that depicted in figures ① and ② above and thus serves as the system's low-pass filter.

In DC/DC converter applications, R is established parallel to the feedback resistance.

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When electrolytic or other high-ESR output capacitors are used:

Phase compensation is relatively simple for applications employing high-ESR output capacitors (on the order of several Ω). In DC/DC converter applications, where LC resonance circuits are always incorporated, the phase margin at these locations is -180°. However, wherever ESR is present, a 90° phase lead is generated, limiting the net phase margin to -90° in the presence of ESR. Since the desired phase margin is in a range less than 150°, this is a highly advantageous approach in terms of the phase margin. However, it also has the drawback of increasing output voltage ripple components.

③ LC resonance circuit

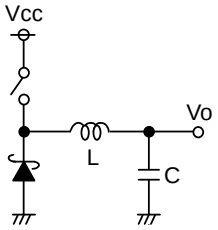

Fig-28

$$fr = \frac{1}{2\pi\sqrt{LC}} \quad [Hz]$$

Resonance point phase margin -180°

④ ESR connected

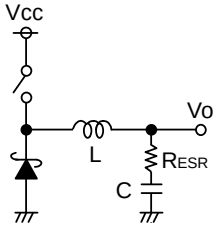

Fig-29

$$fr = \frac{\text{resonance point1}}{2\pi\sqrt{LC}} \quad [Hz] : \text{Resonance Point}$$

$$f_{ESR} = \frac{1}{2\pi R_{ESR}C} \quad [Hz] : \text{Zero}$$

-90° :Pole

Since ESR changes the phase characteristics, only one phase lead need be provided for high-ESR applications. Please choose one of the following methods to add the phase lead.

⑤ Add C to feedback resistor

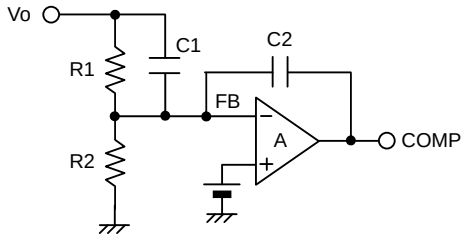

Fig-30

Phase lead $fz = \frac{1}{2\pi C1R1}$ [Hz]

⑥ Add R3 to aggregator

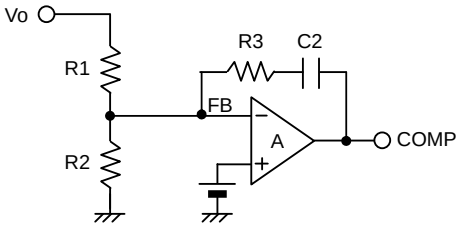

Fig-31

Phase lead $fz = \frac{1}{2\pi C2R3}$ [Hz]

Set the phase lead frequency close to the LC resonance frequency in order to cancel the LC resonance.

When using ceramic, OS-CON, or other low-ESR capacitors for the output capacitor:

Where low-ESR (on the order of tens of mΩ) output capacitors are employed, a two phase-lead insertion scheme is required, but this is different from the approach described in figure ③~⑥, since in this case the LC resonance gives rise to a 180° phase margin/delay. Here, a phase compensation method such as that shown in figure ⑦ below can be implemented.

⑦ Phase compensation provided by secondary (dual) phase lead

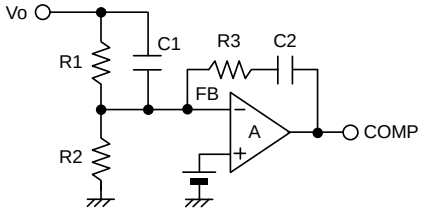

Fig-32

Phase lead $fz1 = \frac{1}{2\pi R1C1}$ [Hz]

Phase lead $fz2 = \frac{1}{2\pi R3C2}$ [Hz]

LC resonance frequency $fr = \frac{1}{2\pi\sqrt{LC}}$ [Hz]

Once the phase-lead frequency is determined, it should be set close to the LC resonance frequency.
This technique simplifies the phase topology of the DCDC Converter. Therefore, it might need a certain amount of trial-and-error process. There are many factors(The PCB board layout, Output Current, etc.)that can affect the DCDC characteristics. Please verify and confirm using practical applications.

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（9）MOSFET selection

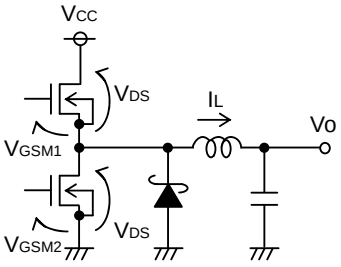

Fig-33

FET uses Nch MOS

- V_{DS} > Vcc
- V_{GSM1} > BOOT-SW interval voltage
- V_{GSM2} > VREG5
- Allowable current > voltage current + ripple current

※Should be at least the over current protection value

※Select a low ON-resistance MOSFET for highest efficiency

- The shoot-through may happen when the input parasitic capacitance of FET is extremely big or the Duty ratio is less than or equal to 10%. Less than or equal to 1000pF input parasitic capacitance is recommended. Please confirm operation on the actual application since this character is affected by PCB layout and components.

（10）Schottky barrier diode selection

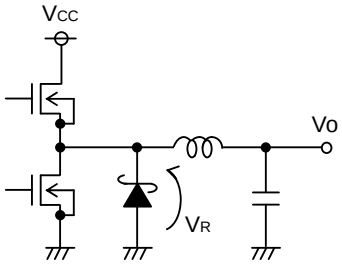

Fig-34

- Reverse voltage V_R > Vcc
- Allowable current > voltage current + ripple current

※Should be at least the over current protection value

※Select a low forward voltage, fast recovery diode for highest efficiency

（11）Sequence function

●Circuit diagram

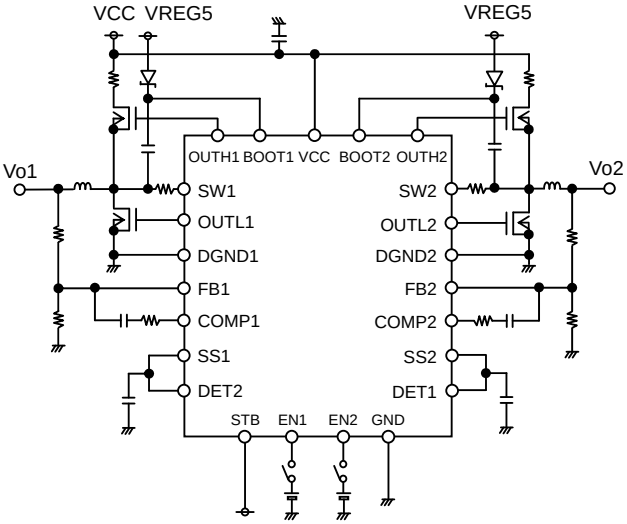

Fig-35

●Timing chart

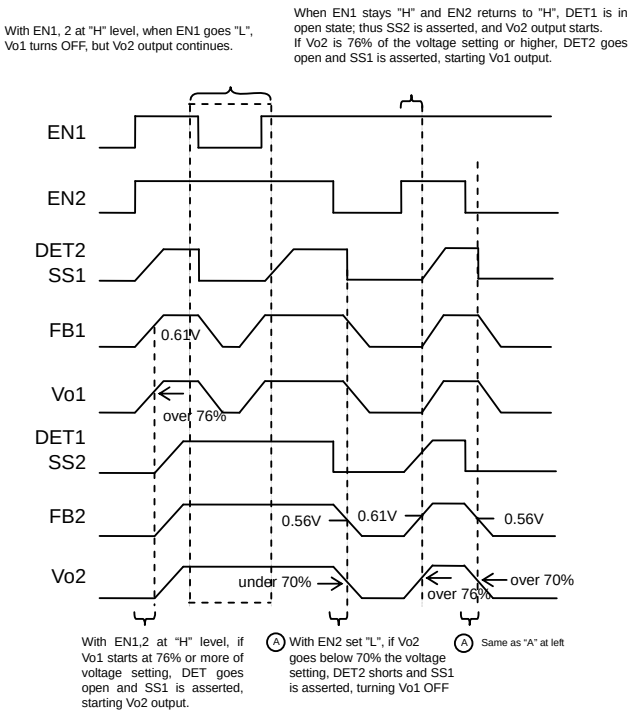

Fig-36

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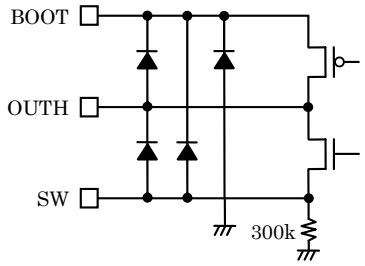
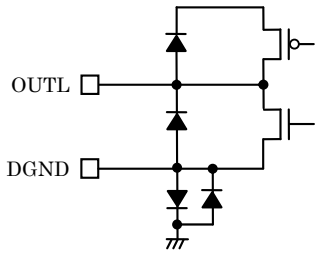
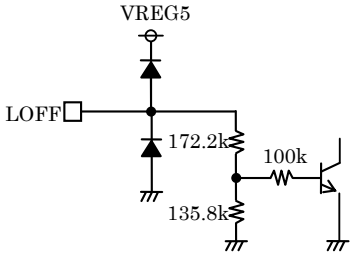
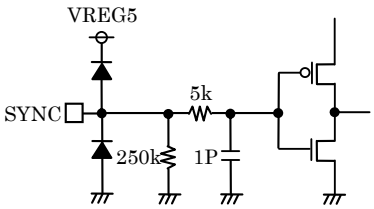
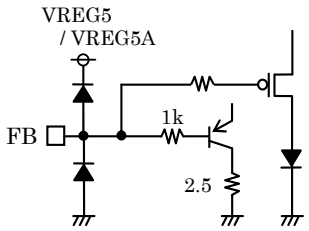
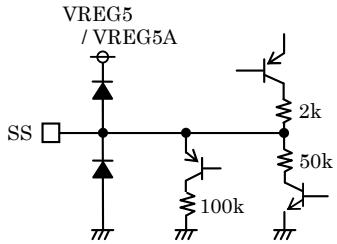
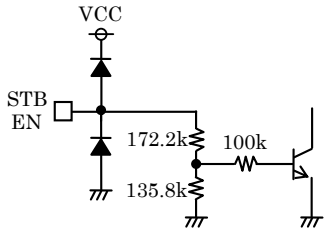
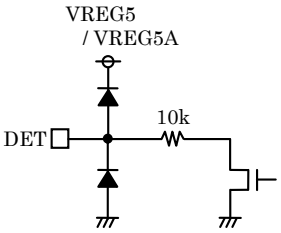
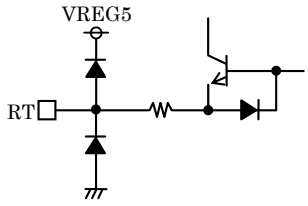
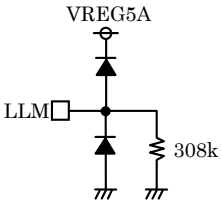
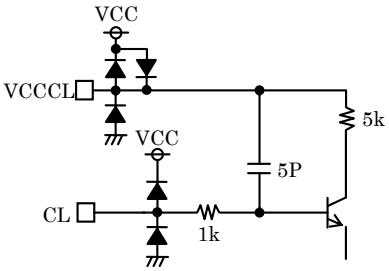
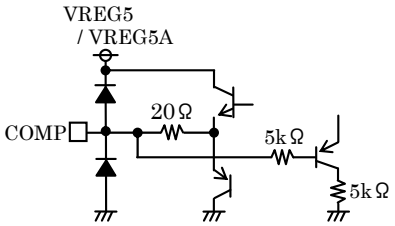
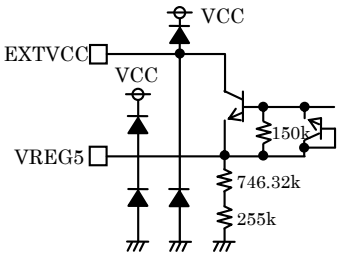
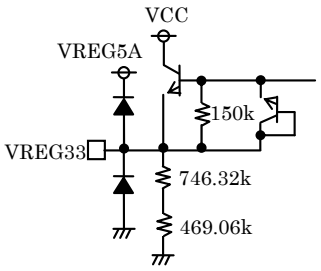
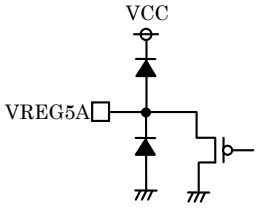
●Input/Output equivalent circuits

13, 48PIN (SW1, SW2) 2, 11PIN (BOOT2, BOOT1) 1, 15PIN (OUTH1, OUTH2)	14, 47PIN (DGND1, DGND2) 15, 46PIN (OUTL1, OUTL2) 44, 17PIN (VREG5, VREG5A)	31PIN (LOFF)
		
34PIN (SYNC)	21, 39PIN (FB1, FB2)	23, 37PIN (SS1, SS2)
		
25, 26, 27PIN (STB, EN1, EN2)	24, 36PIN (DET1, DET2)	33PIN (RT)
		
35PIN (LLM)	3, 10PIN (CL2, CL1) 5, 8PIN (VCCCL2, VCCCL1)	22, 38PIN (COMP1, COMP2)
		
41PIN (EXTVCC) 44PIN (VREG5)	19PIN (VREG33)	17PIN (VREG5A)
		

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●Operation notes

1）Absolute maximum ratings

Exceeding the absolute maximum ratings for supply voltage, operating temperature or other parameters can damage or destroy the IC. When this occurs, it is impossible to identify the source of the damage as a short circuit, open circuit, etc. Therefore, if any special mode is being considered with values expected to exceed absolute maximum ratings, consider taking physical safety measures to protect the circuits, such as adding fuses.

2）GND electric potential

Keep the GND terminal potential at the lowest (minimum) potential under any operating condition.

3）Thermal design

Be sure that the thermal design allows sufficient margin for power dissipation (Pd) under actual operating conditions.

4）Inter-pin shorts and mounting errors

Use caution when positioning the IC for mounting on printed surface boards. Connection errors may result in damage or destruction of the IC. The IC can also be damaged when foreign substances short output pins together, or cause shorts between the power supply and GND.

5）Operation in strong electromagnetic fields

Use caution when operating in the presence of strong electromagnetic fields, as this may cause the IC to malfunction.

6）Testing on application boards

Connecting a capacitor to a low impedance pin for testing on an application board may subject the IC to stress. Be sure to discharge the capacitors after every test process or step. Always turn the IC power supply off before connecting it to or removing it from any of the apparatus used during the testing process. In addition, ground the IC during all steps in the assembly process, and take similar antistatic precautions when transporting or storing the IC.

7) The output FET

The shoot-through may happen when the input parasitic capacitance of FET is extremely big or the Duty ratio is less than or equal to 10%. Less than or equal to 1000pF input parasitic capacitance is recommended. Please confirm operation on the actual application since this character is affected by PCB layout and components.

8）This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. Relations between each potential may form as shown in the example below, where a resistor and transistor are connected to a pin:

- ○ With the resistor, when GND＞ Pin A, and with the transistor (NPN), when GND＞Pin B:
  The P-N junction operates as a parasitic diode
- ○ With the transistor (NPN), when GND＞ Pin B:
  The P-N junction operates as a parasitic transistor by interacting with the N layers of elements in proximity to the parasitic diode described above.

Parasitic diodes inevitably occur in the structure of the IC. Their operation can result in mutual interference between circuits, and can cause malfunctions, and, in turn, physical damage or destruction. Therefore, do not employ any of the methods under which parasitic diodes can operate, such as applying a voltage to an input pin lower than the (P substrate) GND.

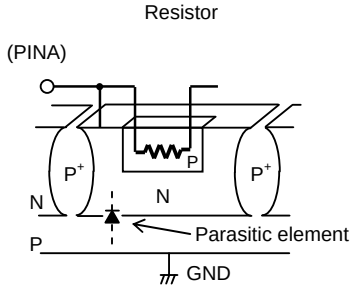

Fig-37

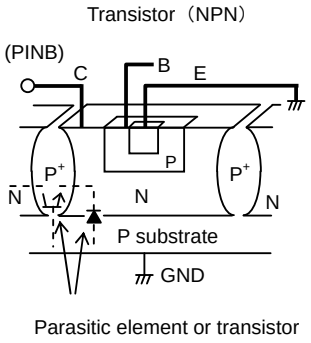

Fig-38

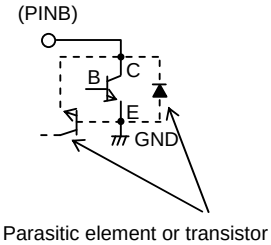

Fig-39

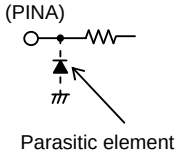

Fig-40

9）GND wiring pattern

When both a small-signal GND and high current GND are present, single-point grounding (at the set standard point) is recommended, in order to separate the small-signal and high current patterns, and to be sure voltage changes stemming from the wiring resistance and high current do not cause any voltage change in the small-signal GND. In the same way, care must be taken to avoid wiring pattern fluctuations in any connected external component GND.

10）In some application and process testing, Vcc and pin potential may be reversed, possibly causing internal circuit or element damage. For example, when the external capacitor is charged, the electric charge can cause a Vcc short circuit to the GND.

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In order to avoid these problems, limiting output pin capacitance to 100μF or less and inserting a Vcc series countercurrent prevention diode or bypass diode between the various pins and the Vcc is recommended.

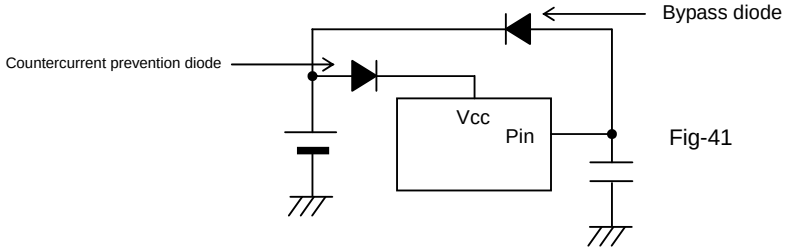

Fig-41

11）Thermal shutdown (TSD)

This IC is provided with a built-in thermal shutdown (TSD) circuit, which is designed to prevent thermal damage to or destruction of the IC. Normal operation should be within the power dissipation parameter, but if the IC should run beyond allowable Pd for a continued period, junction temperature (Tj) will rise, thus activating the TSD circuit, and turning all output pins OFF. When Tj again falls below the TSD threshold, circuits are automatically restored to normal operation. Note that the TSD circuit is only asserted beyond the absolute maximum rating. Therefore, under no circumstances should the TSD be used in set design or for any purpose other than protecting the IC against overheating

12）The SW pin

When the SW pin is connected in an application, its coil counter-electromotive force may give rise to a single electric potential. When setting up the application, make sure that the SW pin never exceeds the absolute maximum value. Connecting a resistor of several Ω will reduce the electric potential. (See Fig. 43)

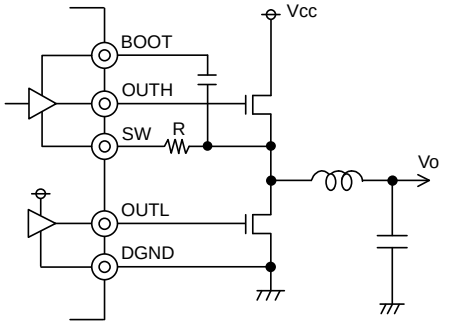

Fig-42

13）Dropout operation

When input voltage falls below approximately output voltage / 0.9 (varying depending on operating frequency) the ON interval on the OUTL side MOS is lost, making boost applications and wrap operation impossible. If a small differential between input and output voltage is envisioned for a prospective application, connect the load such that the SW voltage drops to the GND level. Managing this load requires discharging the SW line capacitance (SW pin capacitance: approx. 500pF; OUTL side MOS D-S capacitance; Schottky capacitance). Supported loads can be calculated using the equation below.

$$ILOAD = \frac{\text{Output voltage} \times \text{SW line capacitance}}{25n}$$

Note that SW line capacitance is lower with smaller loads, and more stable operation is attained when low voltage bias circuits are configured as in the example below (Fig. 44). However, the degree to which line capacitance is reduced or operational stability is attained will vary depending on the board layout and components. Therefore, be certain to confirm the effectiveness of these design factors in actual operation before entering mass production.

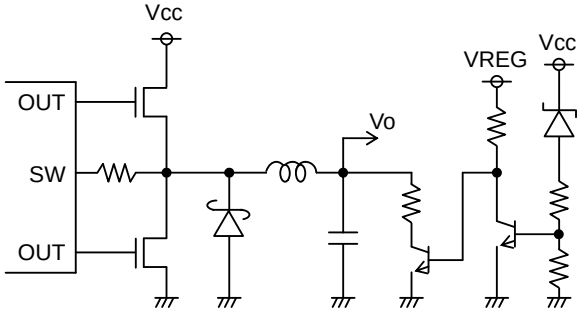

Fig-43

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14) Logic of Output

When each function operates, each output is as follows.

Function	Upper side FET	OUTH	Lower side FET	OUTL
EN= L	OFF	L	OFF	L
OCP	OFF	L	ON	H
UVLO	OFF	L	OFF	L
TSD	OFF	L	OFF	L

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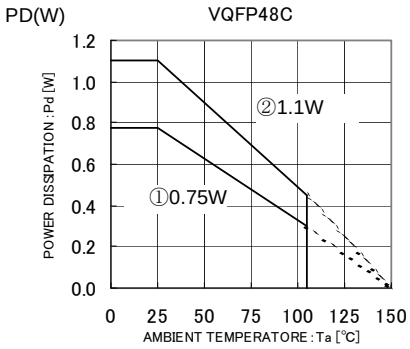
●Power dissipation vs. temperature characteristics



①：Stand-alone IC

②：Mounted on Rohm standard board

（70mm x 70mm x 1.6mm glass-epoxy board ）

●Part order number

B	D	9	0	1	2	K	V	−	E	2

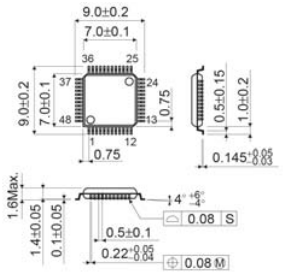
ROHM part code

Type/No.

Package type
KV ： VQFP48C

VQFP48C

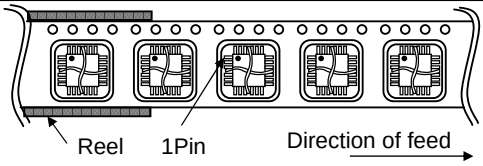
<Dimension>



（Unit:mm)

< Packing information >

Tape	Embossed carrier tape
Quantity	1500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



※When you order , please order in times the amount of package quantity.

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