Large Current External FET Controller Type Switching Regulators

Step-down,High-efficiency Switching Regulator (Controller type)

BD9017KV

No.09028ECT01

●Overview

The BD9017KV is a 2-ch synchronous controller with rectification switching for enhanced power management efficiency. It supports a wide input range and leads to eco-design (low power consumption) for various electronics.

●Features

1) Wide input voltage range: 3.9V～30V
2) Precision voltage references: 0.8V±1%
3) FET direct drive
4) Rectification switching for increased efficiency
5) Variable frequency: 250k～550kHz (external synchronization to 600kHz)
6) Built-in auto-recovery over-current protection
7) Separate enable-pins per CH for individual power up/down control
8) Supports various applications: step-down, step-up, and step-up-down
9) Small footprint packages: VQFP48C
10) When operating at Max Duty, the switching frequency slows down to 1/5 to reduce input/output difference.

●Applications

Car audio and navigation systems, CRTTV,LCDTV,PDPTV,STB,DVD,and PC systems,portable CD and DVD players, etc.

●Absolute Maximum Ratings (Ta=25℃)

Parameter	Symbol	Rating	Unit
VCC Voltage	VCC	35 *1	V
EXTVCC Voltage	EXTVCC	35 *1	V
VCCCL1,2 Voltage	VCCCL1,2	35 *1	V
CL1,2 Voltage	CL1,2	35	V
SW1,2 Voltage	SW1,2	35 *1	V
BOOT1,2 Voltage	BOOT1,2	40 *1	V
BOOT1,2-SW1,2Voltage	BOOT1,2-SW1,2	7 *1	V
EN1,2 Voltage	EN1,2	EXTVCC	V
VREG5,5A	VREG5,5A	7	V
PGOOD Voltage	PGOOD	7	V
SS1,2 Voltage	SS1,2	VREG5	V
FB1,2 Voltage	FB1,2		
P1,2 Voltage	COMP1,2		
RT Voltage	RT		
SYNC Voltage	SYNC		
Power Dissipation	Pd	1.1 *2	W
Operating temperature	Topr	-40～+85	℃
Storage temperature	Tstg	-55～+150	℃
Junction temperature	Tj	+150	℃

*1 Regardless of the listed rating, do not exceed Pd in any circumstances.
*2 Mounted on a 70mm x 70mm x 1.6mm glass-epoxy board. Reduce by 8.8mW/℃ (VQFP48C) above 25℃.

●**Recommend operating range** (Ta=25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input voltage 1	VCC,EXTVCC	3.9 *1 *2	12	30	V
Input voltage 2	VCCCL	3 *1 *2	12	VCC	V
BOOT－SW voltage	BOOT－SW	3.9	5	VREG5	V
Oscillator frequency	OSC	250	300	550	kHz
Synchronous frequency	SYNC	OSC	-	600 *2	kHz
Synchronous frequency pulse width (ON Time)	Ton	0.2	1/(2×SYNC)	-	μsec
Synchronous frequency pulse width (OFF Time)	Toff	0.2	1/(2×SYNC)	-	μsec

*1 In case of using less than 6V, Short VCC, EXTVCC and VREG5.
Moreover, it is the voltage range when 4.5V or greater is once supplied to the input.
*2 Should not exceed OSC×2
★ This product is not designed to provide resistance against radiation.

●**Electrical characteristics** (Unless otherwise specified, Ta=25℃ VCC=12V STB=5V EN1,2=5V)

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
VIN bias current	IIN	-	5	10	mA	
Shutdown mode current	IST	-	0	10	μA	EN1,EN2=0V , VREG5 OFF
EN1,2 low voltage	VENth1	GND	-	1.0	V	When each EN is OFF,each ch is OFF
EN1,2 high voltage	VENth2	2.6	-	Vcc	V	When EN is ON,each ch is ON
EN1,2 input current	IEN	12	23	48	μA	VEN=5V
[VREG5 Block]						
VREG5 output voltage	VREG5	4.7	4.95	5.2	V	I_{REF}=6mA
[Under Voltage Lock Out Block]						
VREG5 threshold voltage	VREG_UVLO	3.5	3.7	3.9	V	V_{REG}:Sweep down
VREG5 hysteresis voltage	DVREG_UVLO	100	200	400	mV	V_{REG}:Sweep up
[Oscillator]						
Oscillator frequency	FOSC	270	300	330	kHz	RT=100 kΩ
Synchronous frequency	Fsync	-	500	-	kHz	RT=100 kΩ,SYNC=500kHz
SYNC pulse low voltage	Vsynclow	GNC	-	0.5	V	
SYNC pulse high voltage	Vsynchigh	2.5	-	7	V	
SYNC input current	Isync	10	20	40	μA	Vsync=5V
[Error Amp Block]						
VO input bias current	IVo+	-	-	1	μA	
Feedback reference voltage	VOB	0.792	0.800	0.808	V	
[Soft start block]						
Charge current	ISS	6.5	10	13.5	μA	VSS=1V
Discharge current	IDIS	0.6	1.7	3	mA	VSS=1V,VCC=3V
Maximum voltage	Vss_MAX	2.05	2.25	2.45	V	
Standby voltage	Vss_STB	-	-	0.3	V	VCC=0.3V
[Over Current Protection Block]						
CL threshold voltage	Vswth	70	90	110	mV	
CL input current 1,2	Iswin	-	-	10	μA	
Output short detection voltage	Vosh	0.46	0.56	0.66	V	VFB
Output short release voltage	Vodet	0.51	0.61	0.71	V	VFB
[PGOOD]						
PGOOD output L current	IPGOODL	0.56	0.7	-	mA	PGOOD=1V,FB=0V
PGOOD output H current	IPGOODH	-	0	3	μA	PGOOD=5V
Over voltage detection voltage	V_{FBO}	0.874	0.92	0.966	V	VFB

●Reference data (Unless otherwise specified, Ta=25℃)

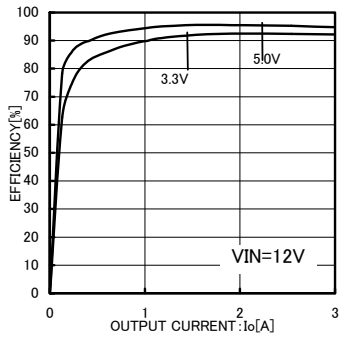


Fig.1 Efficiency 1

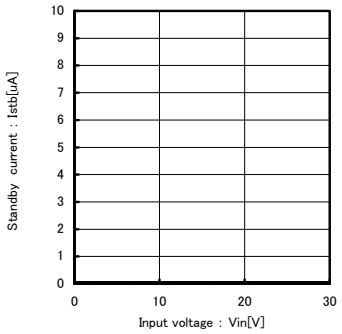


Fig.2 Standby current

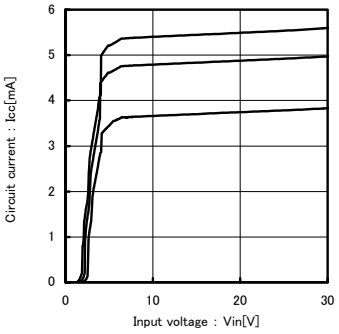


Fig.3 Circuit current

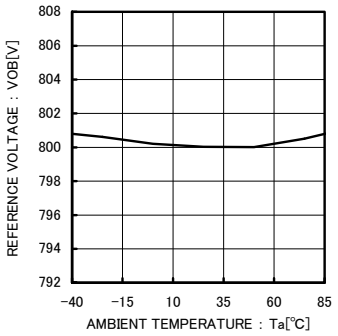


Fig.4 Reference voltage vs. temperature characteristics

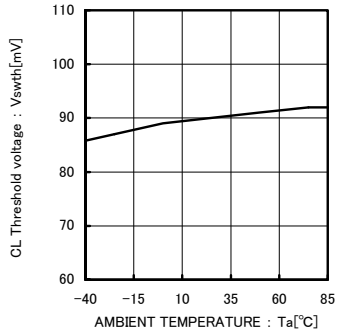


Fig.5 Over current detection vs. temperature characteristics

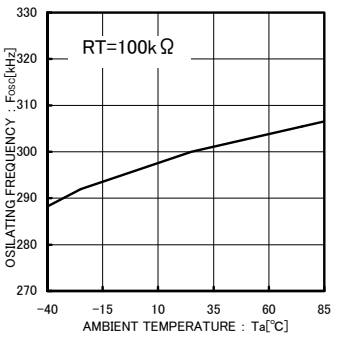


Fig.6 Frequency vs. temperature characteristics

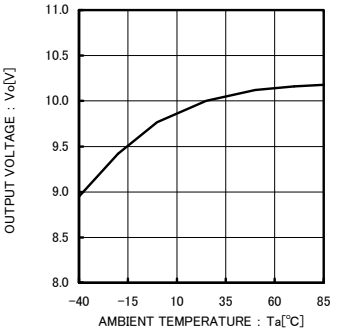


Fig.7 SS Charge current vs temperature characteristics

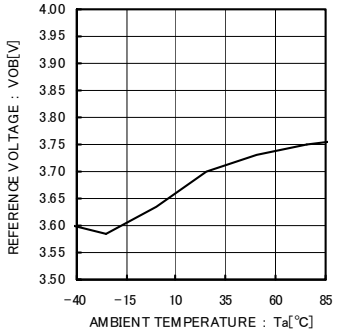


Fig.8 UVLO threshold voltage vs temperature characteristics

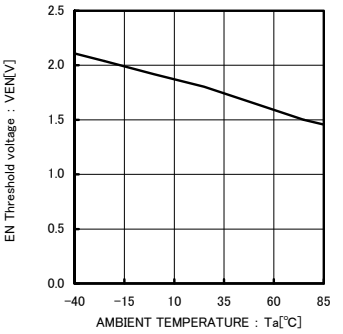


Fig.9 EN threshold voltage vs temperature characteristics

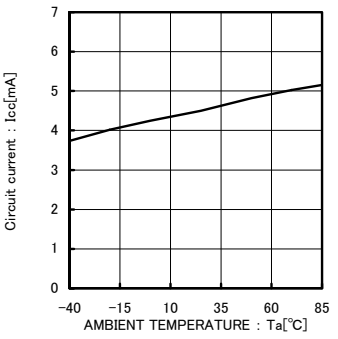


Fig.10 Circuit current vs temperature characteristics

●Block diagram

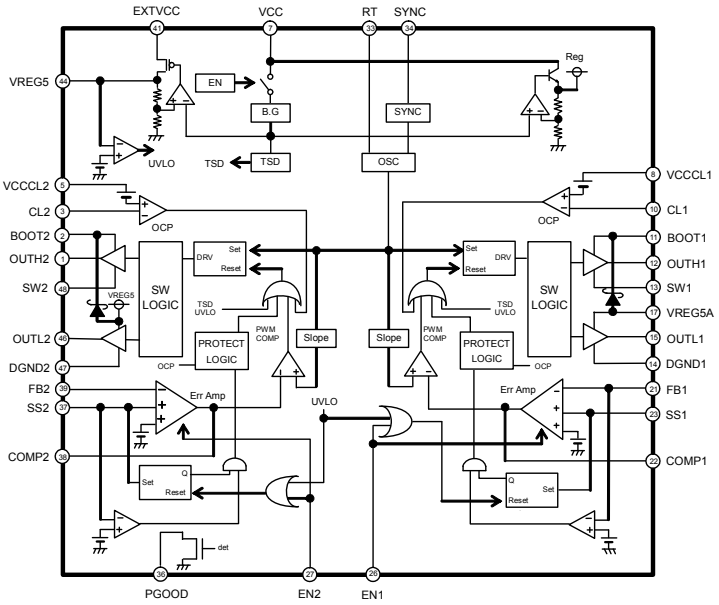


Fig. 11

●Pin configuration

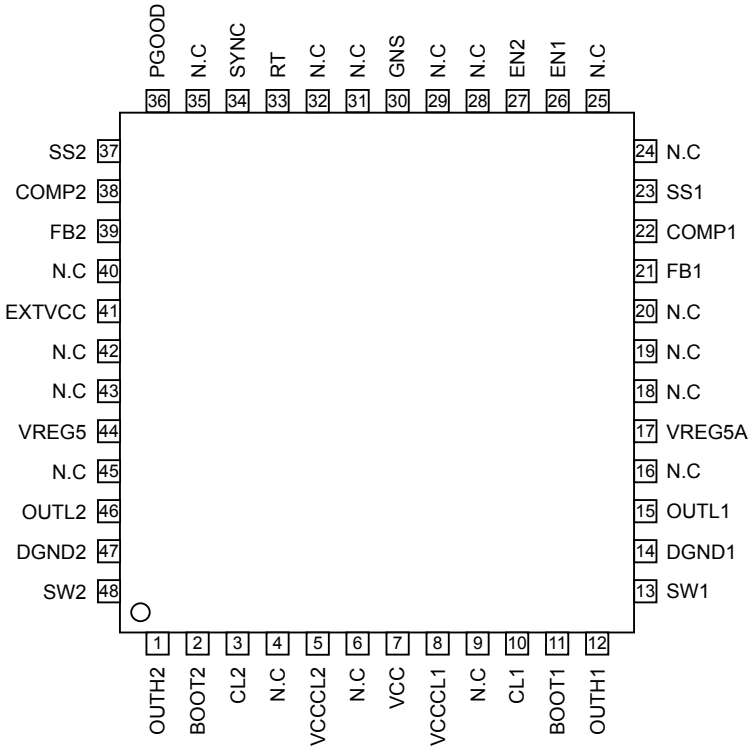


Fig. 12

●PIN function table

Pin No.	Pin name	Function
1	OUTH2	High side FET gate drive pin 2
2	BOOT2	OUTH2 driver power pin
3	CL2	Over current detection pin 2
4	N.C	Non-connect (unused) pin
5	VCCCL2	Over current detection VCC2
6	N.C	Non-connect (unused) pin
7	VCC	Input power pin
8	VCCCL1	Over current detection CC1
9	N.C	Non-connect (unused) pin
10	CL1	Over current detection setting pin 1
11	BOOT1	OUTH1 driver power pin
12	OUTH1	High side FET gate drive pin 1
13	SW1	High side FET source pin 1
14	DGND1	Low side FET source pin 1
15	OUTL1	Low side FET gate drive pin 1
16	N.C	Non-connect (unused) pin
17	VREG5A	FET drive REG input
18	N.C	Non-connect (unused) pin
19	N.C	Non-connect (unused) pin
20	N.C	Non-connect (unused) pin
21	FB1	Error amp input 1
22	COMP1	Error amp output 1
23	SS1	Soft start setting pin 1
24	N.C	Non-connect (unused) pin
25	N.C	Non-connect (unused) pin
26	EN1	Output 1 ON/OFF pin
27	EN2	Output 2 ON/OFF pin
28	N.C	Non-connect (unused) pin
29	N.C	Non-connect (unused) pin
30	GNDS	Ground
31	N.C	Non-connect (unused) pin
32	N.C	Non-connect (unused) pin
33	RT	Switching frequency setting pin
34	SYNC	External synchronous pulse input pin
35	N.C	Non-connect (unused) pin
36	PGOOD	Power good terminal
37	SS2	Soft start setting pin 2
38	COMP2	Error amp output 2
39	FB2	Error amp input 2
40	N.C	Non-connect (unused) pin
41	EXTVCC	External power input pin
42	N.C	Non-connect (unused) pin
43	N.C	Non-connect (unused) pin
44	VREG5	FET drive REG output
45	N.C	Non-connect (unused) pin
46	OUTL2	Low side FET gate drive pin 2
47	DGND2	Low side FET source pin 2
48	SW2	High side FET source pin 2

●Block functional descriptions

・Error amp
The error amp compares output feedback voltage to the 0.8V reference voltage and provides the comparison result as COMP voltage, which is used to determine the switching Duty. COMP voltage is limited to the SS voltage, since soft start at power up is based on SS pin voltage.

・Oscillator (OSC)
Oscillation frequency is determined by the switching frequency pin (RT) in this block. The frequency can be set between 250 kHz and 550 kHz.The phase difference between each output is 180deg.

・SLOPE
The SLOPE block uses the clock produced by the oscillator to generate a triangular wave, and sends the wave to the PWM comparator.

・PWM COMP
The PWM comparator determines switching Duty by comparing the COMP voltage, output from the error amp, with the triangular wave from the SLOPE block. Switching duty is limited to a percentage of the internal maximum duty, and thus cannot be 100% of the maximum.

・Reference voltage (VREG5)
This block generates the internal reference voltage: 5V. The external capacitor is necessary for VREG5. Moreover, the external capacitor should be set to VREG5A which is FET drive REG input. It is recommended to use the ceramic capacitor that is low ESR and 6.6μF～12μF according to VREG5 and VREG5A.

・External synchronization (SYNC)
When pulses are supplied to the SYNC terminal, the internal frequency synchronizes with the frequency of the supplied pulses. Whensynchronized with SYNC, 1ch is turned on with the rising edge of SYNC and 2ch is turned on with the falling edge of SYNC so that the phase difference between each output depends on the Duty of SYNC.
The pulse width needs to be more than 200nsec for both on time and off time. Supply a pulse wave faster than the frequency determined with the setting resistor (RT), but slower than 600 kHz (Fosc×1.5 or less). Moreover, it is recommended to insert the low pass filter to the SYNC terminal. (Refer to fig.13)

・Over current protection (OCP)
The over current protection is activated when the VCCCL-CL voltage reaches or exceeds 90mV. When the over current protection is active, Duty is low, and the output voltage also decreases.

・Short circuit protection (SCP)
After activating the over current protection and if the output voltage falls below 70%, then the short circuit protection will be activated. When the short circuit protection is active, the output is turned off for 32 pulses of the oscillation frequency, and the SS and COMP are discharged.

・Protection circuits (UVLO/TSD)
The UVLO lock out function is activated when VREG5 falls to about 3.7V. The TSD turns outputs OFF when the chip temperature reaches or exceeds 150℃. Output is restored when the temperature drops below the threshold value.

・Power GOOD (PGOOD)terminal
The UVLO lock out function is activated when VREG5 falls to about 3.7V. The TSD turns outputs OFF when the chip temperature reaches or exceeds 150℃. Output is restored when the temperature drops below the threshold value.

●**Application circuit example**

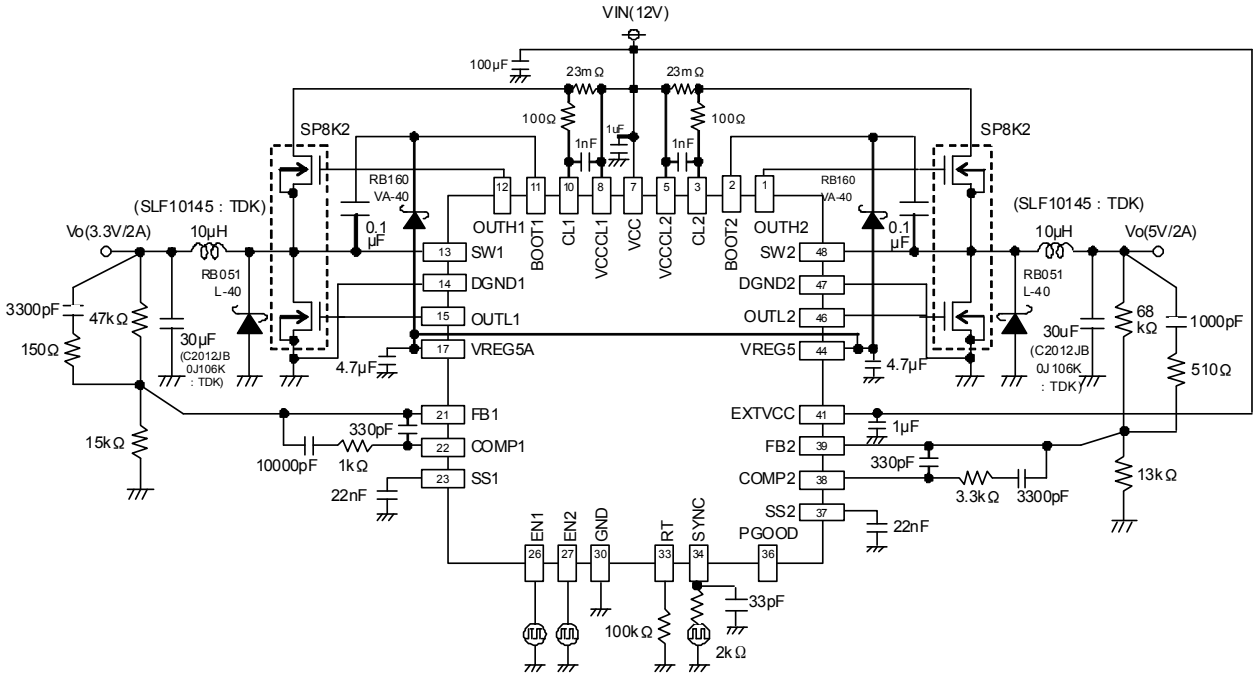


Fig. 13(Step-Down)

There are many factors (PCB board layout, Output Current, etc.) that can affect the DCDC characteristics.
Please verify and confirm using practical applications.

●Application component selection

(1) Setting the output L value

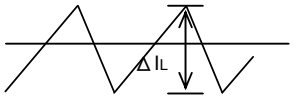


Fig. 14

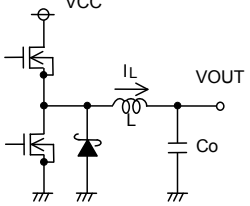


Fig. 15

Output ripple current

The coil value significantly influences the output ripple current. Thus, as seen in equation (5), the larger the coil, and the higher the switching frequency, the lower the drop in ripple current.

$$\Delta IL = \frac{(VCC-VOUT) \times VOUT}{L \times VCC \times f} \quad [A] \cdot \cdot \cdot (5)$$

The optimal output ripple current setting is 30% of maximum current.

$$\Delta IL = 0.3 \times IOUTmax.[A] \cdot \cdot \cdot (6)$$

$$L = \frac{(VCC-VOUT) \times VOUT}{\Delta IL \times VCC \times f} \quad [H] \cdot \cdot \cdot (7)$$

(ΔIL : output ripple current f : switching frequency)

※Outputting a current in excess of the coil current rating will cause magnetic saturation of the coil and decrease efficiency.
It is recommend establishing sufficient margin to ensure that peak current does not exceed the coil current rating.

※Use low resistance (DCR, ACR) coils to minimize coil loss and increase efficiency.

(2) Setting the output capacitor Co value

Select output capacitor with consideration to the ripple voltage (Vpp) tolerance.
The following equation is used to determine the output ripple voltage.

Step down $\Delta V_{PP} = \Delta I_L \times R_{ESR} + \frac{\Delta I_L}{Co} \times \frac{Vo}{Vcc} \times \frac{1}{f}$ [V] Note: f : switching frequency

Be sure to keep the output Co setting within the allowable ripple voltage range.

※Please allow sufficient output voltage margin in establishing the capacitor rating. Note that low-ESR capacitors enable lower output ripple voltage. Also, to meet the requirement for setting the output startup time parameter within the soft start time range, please factor in the conditions described in the capacitance equation (9) for output capacitors, below.

$$Co \leqq \frac{TSS \times (Limit - IOUT)}{VOUT} \cdot \cdot \cdot (8)$$

Tss : soft start time

ILimit : over current detection value Refer to (9)

Note: less than optimal capacitance values may cause problems at startup.

(3) Setting the Input capacitor Cin value

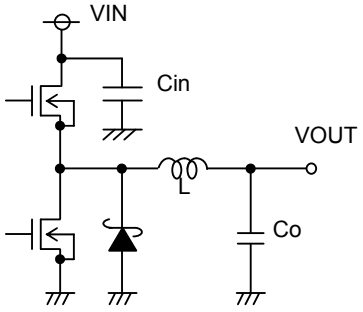


Fig. 16

Input capacitor

The input capacitor serves to lower the output impedance of the power source connected to the input pin (VCC). Increased power supply output impedance can cause input voltage (VCC) instability, and may negatively impact oscillation and ripple rejection characteristics. Therefore, be certain to establish an input capacitor in close proximity to the VCC and GND pins. Select a low-ESR capacitor with the required ripple current capacity and the capability to withstand temperature changes without wide tolerance fluctuations. The ripple current IRMSS is determined using equation (10).

$$IRMS = IOUT \times \sqrt{\frac{VOUT\ (VCC - VOUT)}{VCC}} \quad [A] \cdot \cdot \cdot (10)$$

Also, be certain to ascertain the operating temperature, load range and MOSFET conditions for the application in which the capacitor will be used, since capacitor performance is heavily dependent on the application's input power characteristics, substrate wiring and MOSFET gate drain capacity.

(4) Feedback resistor design

Please refer to the following equation in determining the proper feedback resistance. The recommended setting is in a range between 10kΩ and 330kΩ(total of R1 and R2). Resistance less than 10kΩ risks decreased power efficiency, while setting the resistance value higher than 330kΩ will result in an internal error amp input bias current of 0.2uA increasing the offset voltage. Also when the output pulse width is too short, there is a possibility the output becomes unstable. It is recommend putting the load more than half of the ripple current on the output or using the output pulse width longer than 250nsec.

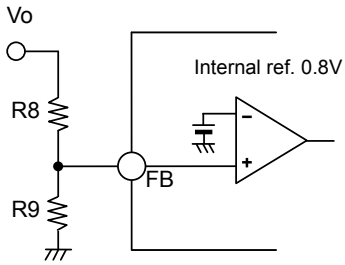


Fig. 17

$$Vo = \frac{R8 + R9}{R9} \times 0.8\ [V] \quad \cdot\cdot\cdot (11)$$

$$\frac{Vo}{Vin} \times \frac{1}{f} \geqq 250nsec \quad \cdot\cdot\cdot (12)$$

For applications where Vin and EN are directly connected, the output may overshoot. To avoid this issue it is recommended to select the lower side of the feedback resistor to more than 47kΩ.
This restriction does not apply if the EN is individually turned on when the VCC is greater than 4.5V.

(5) Setting switching frequency

The triangular wave switching frequency can be set by connecting a resistor to the RT 15(33) pin. The RT sets the frequency by adjusting the charge/discharge current in relation to the internal capacitor. Refer to the figure below in determining proper RT resistance, noting that the recommended resistance setting is between 50kΩ and 130kΩ. Settings outside this range may render the switching function inoperable, and proper operation of the controller overall cannot be guaranteed when unsupported resistance values are used.

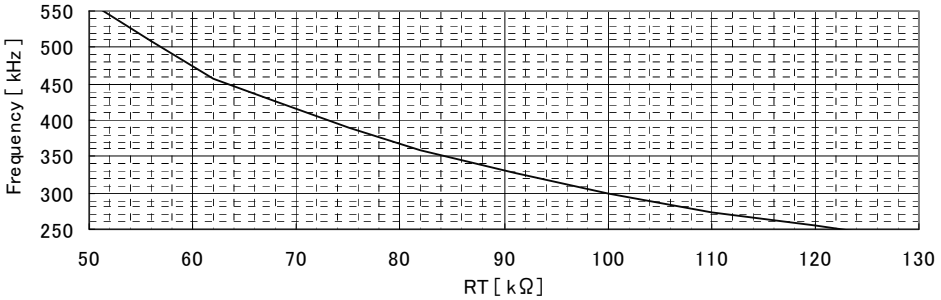


Fig. 18 RT vs. switching frequency

(6) Setting the soft start time

The soft start function is necessary to prevent an inrush of coil current and output voltage overshoot at startup. The figure below shows the relation between soft start delay time and capacitance, which can be calculated using equation (13) at right.

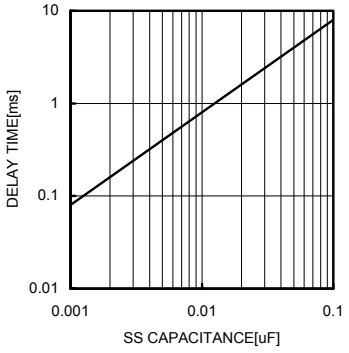


Fig. 19 SS capacitance vs. delay time

$$TSS = \frac{0.8V(typ.) \times CSS}{ISS(10\mu A\ Typ.)}\ [sec] \quad \cdot\cdot\cdot (13)$$

Recommended capacitance values are between 0.01uF and 0.1uF. There is a possibility that the overshoot is generated in the output according to the phase compensation and the output capacity, etc. , and let me confirm it with a real machine, please. For the case with larger capacitance, the SS-pin may not become fully discharged when the EN becomes from H to L, which might cause the output overshoot when the EN becomes back H. Hence the discharge time (Tdis) needs to be carefully considered.

$$Tdis = \frac{Css \times Vss\_MAX}{Idis} \quad [sec]$$

The insertion of the CR filter is recommended as a noise measures because similar is thought when the noise enters the terminal EN.

Please use high accuracy components (such as X5R) when implementing sequential startups involving other power sources. Be sure to test the actual devices and applications to be used, since the soft start time varies, depending on input voltage, output voltage and capacitance, coils and other characteristics.

(7) Setting over current detection values

The current limit value(ILimit)is determined by the resistance of the RCL established between CL and VCCCL.

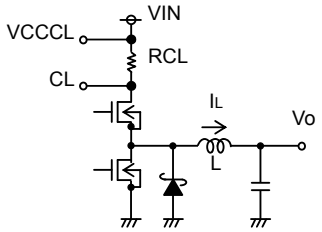


Fig. 20

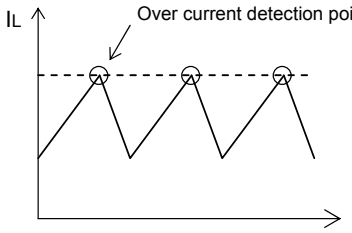


Fig. 21

$$ILimit = \frac{90m}{RCL} \quad [A] \cdot \cdot \cdot (14)$$

The current limit is an auto-recovery type. When the over current is detected, the output Duty is reduced to limit the output current. The output voltage returns to normal when the load returns to the normal state.

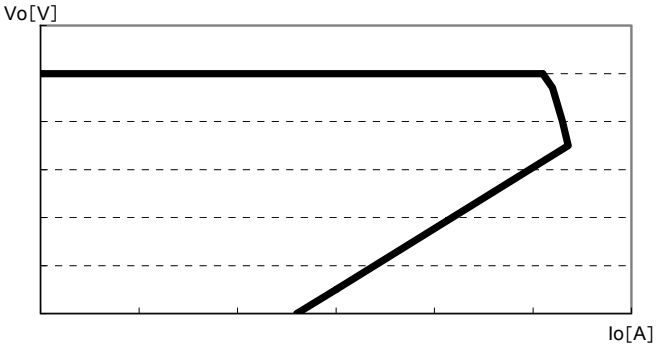


Fig. 22

(8) Method for determining phase compensation

In switching regulator applications, the phase needs to be compensated in accordance with the operating conditions as well as the used external parts. In case the margin is not enough, then the output may possibly overshoot or undershoot when the load current, input voltage or switching frequency rapidly changes.The compensation technique is described below.Conditions for application stability

Feedback stability conditions are as follows:

・At the unity (0-dB) gain, the phase delay is 150° or less (i.e., phase margin is at least 30°):

Since the DC/DC converter application is sampled according to the switching frequency, GBW (frequency at 0-dB gain) of the overall system should be set to 1/10 or less of the switching frequency. The following section summarizes the targeted characteristics of this application.

・At the unity (0-dB) gain, the phase delay is 150˚ or less (i.e. the phase margin is 30˚ or more).

・The GBW for this occasion is 1/10 or less of the switching frequency.

Responsiveness is determined with restrictions on the GBW. To improve responsiveness, higher switching frequency should be provided.The key to achieving successful stabilization using phase compensation is to cancel the secondary phase margin/delay (-180°) generated by LC resonance, by employing a dual phase lead. In short, adding two phase leads stabilizes the application.GBW (the frequency at unity gain) is determined by the phase compensation capacitor connected to the error amp. Thus, a larger capacitor will serve to lower GBW if desired.

① General use integrator (low-pass filter) ② Integrator open loop characteristics

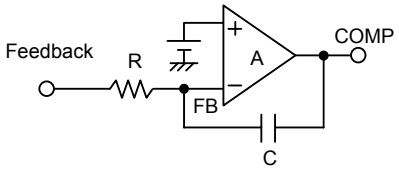


Fig. 23

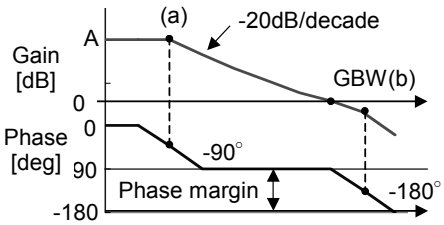


Fig. 24

point (a) $fa = \frac{1}{2\pi RCA}$ 1.25[Hz]

point (b) $fa = GBW \frac{1}{2\pi RC}$ [Hz]

The error amp is provided with phase compensation similar to that depicted in figures ① and ② above and thus serves as the system's low-pass filter.
In DC/DC converter applications, R is established parallel to the feedback resistance.

When electrolytic or other high-ESR output capacitors are used:

Phase compensation is relatively simple for applications employing high-ESR output capacitors (on the order of several Ω). In DC/DC converter applications, where LC resonance circuits are always incorporated, the phase margin at these locations is -180°. However, wherever ESR is present, a 90° phase lead is generated, limiting the net phase margin to -90° in the presence of ESR. Since the desired phase margin is in a range less than 150°, this is a highly advantageous approach in terms of the phase margin. However, it also has the drawback of increasing output voltage ripple components.

③ LC resonance circuit

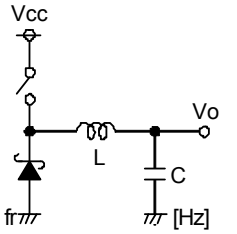


Fig. 25

$\frac{1}{2\pi\sqrt{LC}}$

Resonance point phase delay -180°

④ ESR connected

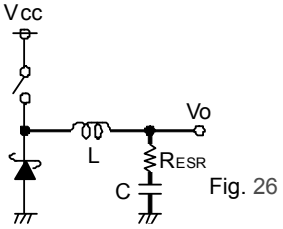


Fig. 26

$fr = \frac{1}{2\pi\sqrt{LC}}$ [Hz] : Resonance Point

$f_{ESR} = \frac{1}{2\pi R_{ESR}C}$ [Hz] :Phase lead

Phase delay -90°

Since ESR changes the phase characteristics, only one phase lead need be provided for high-ESR applications. Please choose one of the following methods to add the phase lead.

⑤ Add C to feedback resistor

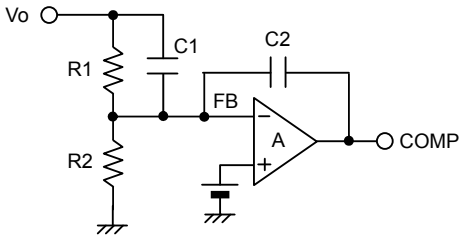


Fig. 27

Phase lead $fz = \frac{1}{2\pi C1R1}$ [Hz]

⑥ Add R3 to aggregator

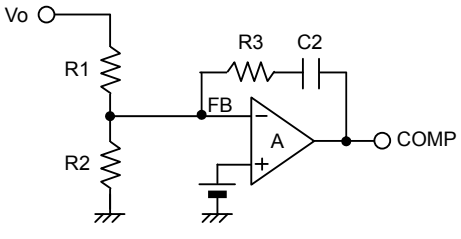


Fig. 28

Phase lead $fz = \frac{1}{2\pi C2R3}$ [Hz]

Set the phase lead frequency close to the LC resonance frequency in order to cancel the LC resonance.
When using ceramic, OS-CON, or other low-ESR capacitors for the output capacitor:
Where low-ESR (on the order of tens of mΩ) output capacitors are employed, a two phase-lead insertion scheme is required, but this is different from the approach described in figure ③~⑥, since in this case the LC resonance gives rise to a 180° phase margin/delay. Here, a phase compensation method such as that shown in figure ⑦ below can be implemented.

⑦ Phase compensation provided by secondary (dual) phase lead

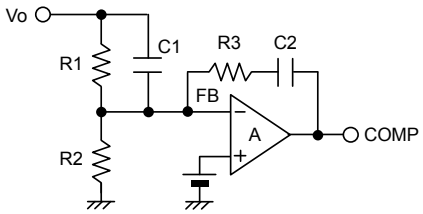


Fig. 29

$$\text{Phase lead} \quad fz1 = \frac{1}{2\pi R1C1} \quad [\text{Hz}]$$

$$\text{Phase lead} \quad fz2 = \frac{1}{2\pi R3C2} \quad [\text{Hz}]$$

$$\text{LC resonance frequency } fr = \frac{1}{2\pi\sqrt{LC}} \quad [\text{Hz}]$$

Once the phase-lead frequency is determined, it should be set close to the LC resonance frequency.
This technique simplifies the phase topology of the DCDC Converter. Therefore, it might need a certain amount of trial-and-error process. There are many factors (The PCB board layout, Output Current, etc.)that can affect the DCDC characteristics. Please verify and confirm using practical applications.

(9)MOSFET selection

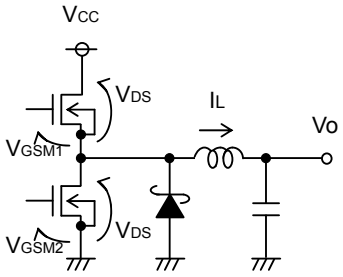


Fig. 30

FET uses Nch MOS
- V_{DS} > Vcc
- V_{GSM1} > Voltage between BOOT and SW pins
- V_{GSM2} > VREG5
- Allowable current > voltage current + ripple current

※Should be at least the over current protection value
※Select a low ON-resistance MOSFET for highest efficiency
- The shoot-through may happen when the input parasitic capacitance of FET is extremely big. Less than or equal to 1200pF input parasitic capacitance is recommended. Please confirm operation on the actual application since this character is affected by PCB layout and components.

(10)Schottky barrier diode selection

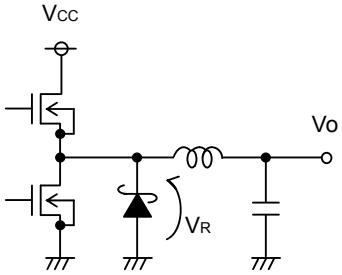


Fig. 31

- Reverse voltage V_R > Vcc
- Allowable current > voltage current + ripple current

※Should be at least the over current protection value
※Select a low forward voltage, fast recovery diode for highest efficiency

<Reference> Measurement of open loop of the DC/DC converter

To measure the open loop of the DC/DC converter, use the gain phase analyzer or FRA to measure the frequency characteristics.

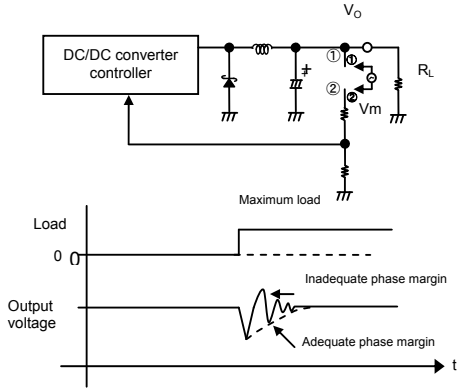


Fig. 32

<Procedure>
1.Check to ensure output causes no oscillation at the maximum load in closed loop.
2.Isolate ① and ② and insert Vm (with amplitude of approximately.100mVpp).
3.Measure (probe) the oscillation of ① to that of ②.

Furthermore, the phase margin can also be measured with the load responsiveness. Measure variations in the output voltage when instantaneously changing the load from no load to the maximum load. Even though ringing phenomenon is caused, due to low phase margin, no ringing takes place. Phase margin is provided. However, no specific phase margin can be probed.

※Please contact us if you have any questions regarding phase compensation

●**Thermal design**

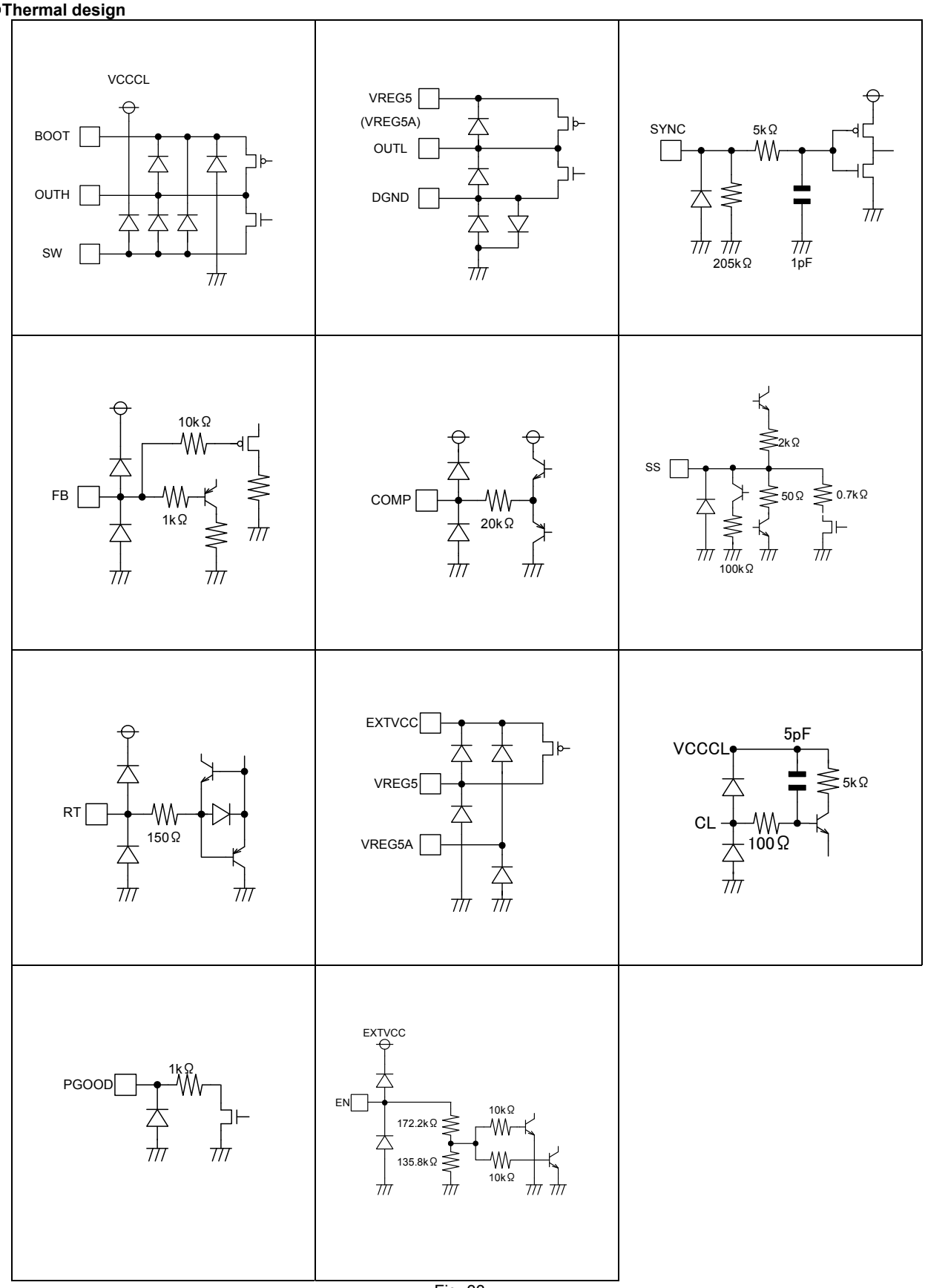


Fig. 33

●Notes for use

1)Absolute maximum ratings

Exceeding the absolute maximum ratings for supply voltage, operating temperature or other parameters can damage or destroy the IC. When this occurs, it is impossible to identify the source of the damage as a short circuit, open circuit, etc. Therefore, if any special mode is being considered with values expected to exceed absolute maximum ratings, consider taking physical safety measures to protect the circuits, such as adding fuses.

2)GND electric potential

Keep the GND terminal potential at the lowest (minimum) potential under any operating condition. Moreover, all terminal voltages except SW must not become less than GND. In any case where any terminal voltages become less than GND, apply measures such as adding by-pass route.

3)Power Dissipation Pd

The power dissipation exceeding its rating would deteriorate the IC characteristics, such as the decrease in the current capability due to the temperature rise of the chip, and hence lead to less reliable. Thus please allow enough margins from the power dissipation rating.

4)Input supply voltage

Input supply pattern layout should be as short as possible and free from electrical interferences.

5)Electrical characteristics

The electrical characteristics of the specifications may vary with the temperature, supply voltage and external circuit, etc. It is recommend to thoroughly verify including transient characteristics.

6)Thermal shutdown (TSD)

This IC is provided with a built-in thermal shutdown (TSD) circuit, which is designed to prevent thermal damage to or destruction of the IC. Normal operation should be within the power dissipation parameter, but if the IC should run beyond allowable Pd for a continued period, junction temperature (Tj) will rise, thus activating the TSD circuit, and turning all output pins OFF. When Tj again falls below the TSD threshold, circuits are automatically restored to normal operation. Note that the TSD circuit is only asserted beyond the absolute maximum rating. Therefore, under no circumstances should the TSD be used in set design or for any purpose other than protecting the IC against overheating

7)Inter-pin shorts and mounting errors

Use caution when positioning the IC for mounting on printed surface boards. Connection errors may result in damage or destruction of the IC. The IC can also be damaged when foreign substances short output pins together, or cause shorts between the power supply and GND.

8)In some application and process testing, Vcc and pin potential may be reversed, possibly causing internal circuit or element damage. For example, when the external capacitor is charged, the electric charge can cause a Vcc short circuit to the GND. In order to avoid these problems, limiting VREG5 pin capacitance to 12μF or less and inserting a Vcc series countercurrent prevention diode or bypass diode between the various pins and the Vcc is recommended.

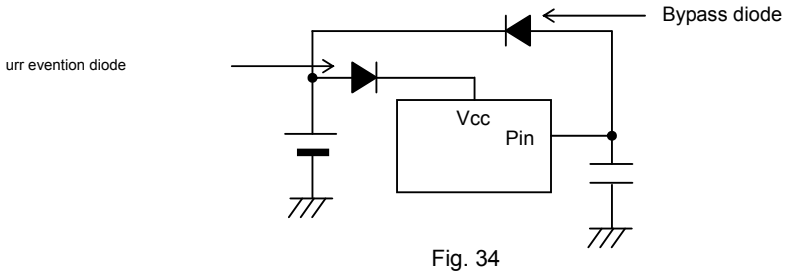


Fig. 34

9)Operation in strong electromagnetic fields

Use caution when operating in the presence of strong electromagnetic fields, as this may cause the IC to malfunction.

10)For applications where the output-pin is connected with large inductive load, which counter-EMF (electromotive force) might possibly occur at the start up or shut down, add a diode for protection.

11)Testing on application boards

Connecting a capacitor to a low impedance pin for testing on an application board may subject the IC to stress. Be sure to discharge the capacitors after every test process or step. Always turn the IC power supply off before connecting it to or removing it from any of the apparatus used during the testing process. In addition, ground the IC during all steps in the assembly process, and take similar antistatic precautions when transporting or storing the IC.

12)GND wiring pattern

When both a small-signal GND and high current GND are present, single-point grounding (at the set standard point) is recommended, in order to separate the small-signal and high current patterns, and to be sure voltage changes stemming from the wiring resistance and high current do not cause any voltage change in the small-signal GND. In the same way, care must be taken to avoid wiring pattern fluctuations in any connected external component GND.

13)The SW pin

When the SW pin is connected in an application, its coil counter-electromotive force may give rise to a single electric potential. When setting up the application, make sure that the SW pin never exceeds the absolute maximum value. Connecting a resistor of several Ω will reduce the electric potential. (See Fig. 35)

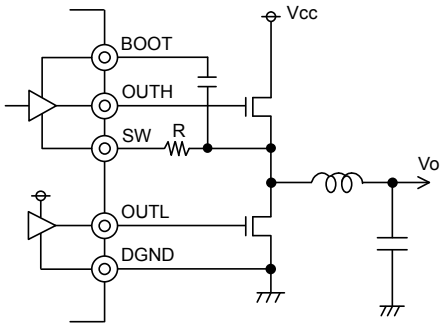


Fig. 35

14)The output FET

The shoot-through may happen when the input parasitic capacitance of FET is extremely big. Less than or equal to 1200pF input parasitic capacitance is recommended. Please confirm operation on the actual application since this character is affected by PCB layout and components.

15)This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated.P-N junctions are formed at the intersection of these Players with the N layers of other elements, creating a parasitic diode or transistor. Relations between each potential may form as shown in the example below, where a resistor and transistor are connected to a pin:

○With the resistor, when GND＞ Pin A, and with the transistor (NPN), when GND＞Pin B:
The P-N junction operates as a parasitic diode

○With the transistor (NPN), when GND＞ Pin B:
The P-N junction operates as a parasitic transistor by interacting with the N layers of elements in proximity to the parasitic diode described above.

Parasitic diodes inevitably occur in the structure of the IC. Their operation can result in mutual interference between circuits, and can cause malfunctions, and, in turn, physical damage or destruction. Therefore, do not employ any of the methods under which parasitic diodes can operate, such as applying a voltage to an input pin lower than the (Psub strate) GND.

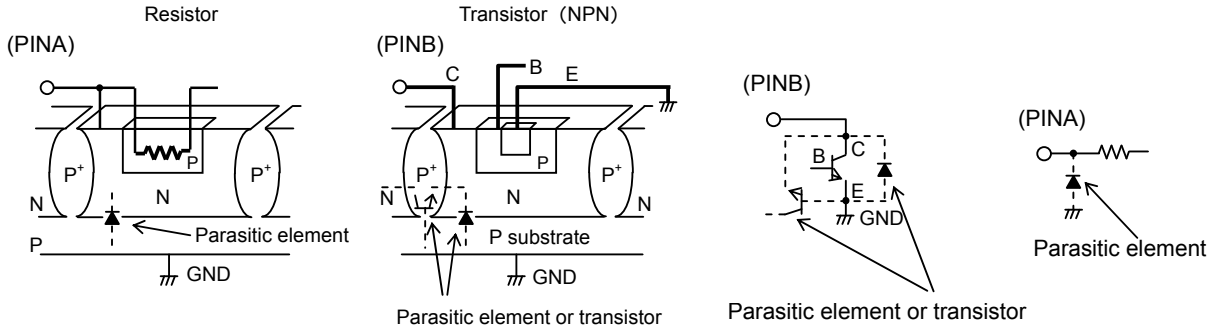


Fig. 36

16) For applications where Vin and EN are directly connected, the output may overshoot. To avoid this issue it is recommended to select the lower side of the feedback resistor to more than 47kΩ.
This restriction does not apply if the EN is individually turned on when the VCC is greater than 4.5V.

17) Changing the switching frequency between the internal oscillator and external synchronization (SYNC)
When the switching frequency changes from the internal oscillator to SYNC, one switching pulse might be skipped. In contrast, when the switching frequency changes from SYNC to the internal oscillator, one extra switching pulse might be added.This would cause the output voltage to be dropped or raised when the switching pulse is skipped or added extra, as shown in Fig. 38.The magnitude of the output voltage drop or rise depends on phase compensation design.

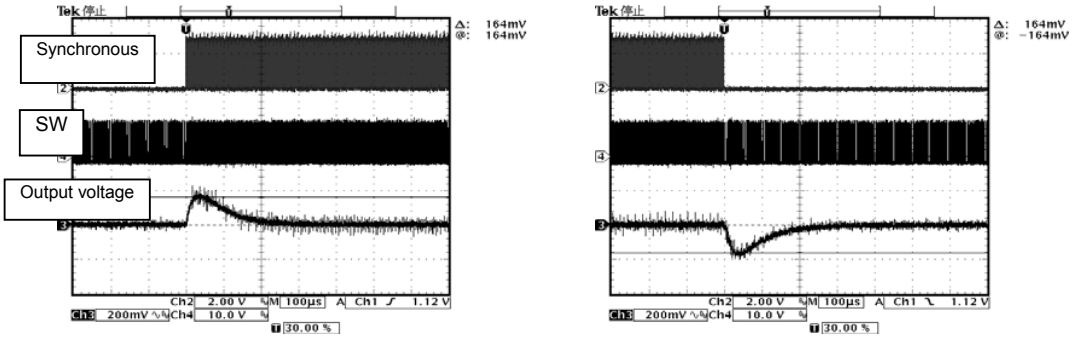


Fig. 38 Output voltage fluctuation when the frequency switch
(Internal oscillator：300kHz、SYNC：450kHz)

Start supplying pluses to SYNC terminal before EN is turned on, or after EN is turned on and Soft start time is passed, as shown in Fig. 39.

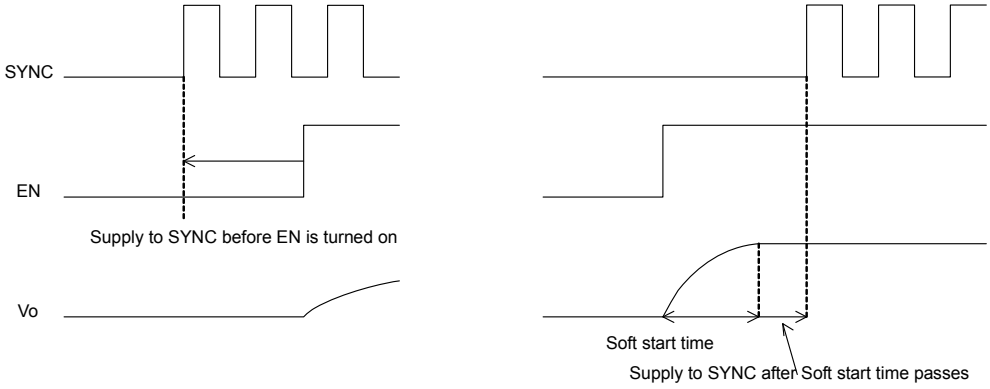


Fig. 39 Timing chart for changing from internal oscillator to SYNC

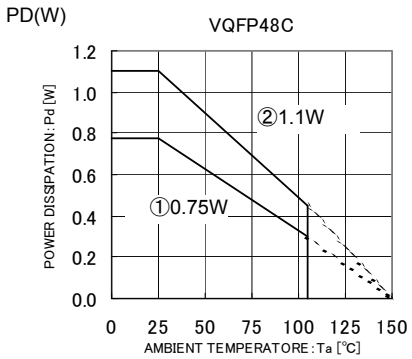
17) EN terminal

There is a possibility that the output doesn't stand up when the charge remains in the output when EN is ON→OFF, and OFF→ON again. Therefore, please turn on EN after Dischargeing it up to 1V the voltage of the output when you turn on EN again. Necessary time for Discharge: t calculates in the type in the under.

$$t = -Co \times Ro \times \ln \frac{1}{Vo} \quad [sec]$$

Vo: Output voltage, Co: Output capacitor, Ro: Output load

●Power dissipation vs. Temperature characteristics



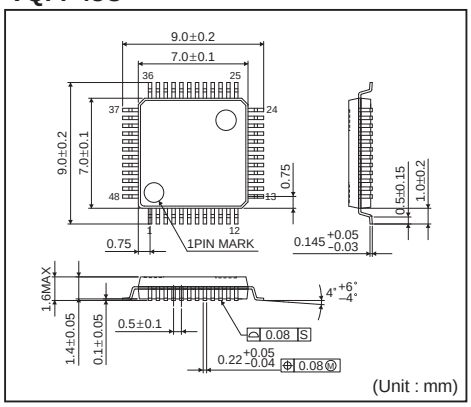
① : Stand-alone IC
② : Mounted on Rohm standard board
(70mm × 70mm × 1.6mm glass-epoxy board)

●Ordering part number

B	D	9	0	1	7	K	V	-	E	2

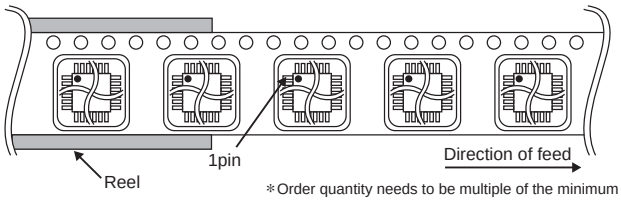
Part No. (BD) — Part No. (9017) — Package KV:VQFP48C — Packaging and forming specification E2: Embossed tape and reel

VQFP48C



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	1500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

Notes

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