Single-chip built-in FET type Switching Regulator Series

1ch High Efficiency Step-down Switching Regulator

BD9180GUL

●Description

The BD9180GUL is a step-down Switching regulator designed to produce a low voltage from 1-cell Li-Ion batteries. The BD9180GUL is suitable for low power application,and an internally set 2MHz switching frequency allows the use of small inductors and capacitors to achieve a small application.Offers high efficiency with our original pulse skip control technology and synchronous rectifier. Employs a current mode control system to provide faster transient response to sudden change in load.

●Features

1) Offers fast transient response with current mode PWM control system.
2) Offers highly efficiency for all load range with synchronous rectifier (Nch/Pch FET) and SLLM (Simple Light Load Mode)
3) Input voltage range : 2.3V to 5.5V
4) Output current max. : 300mA
5) 2MHz Fixed frequency Operation
6) Incorporates soft-start function
7) Incorporates thermal protection, ULVO and short-current protection circuit with time delay function.
8) Incorporates shutdown function.
9) Employs WL-CSP : small 1.1mm×1.6mm

●Use

- Mobile Phone, Smart-phone, PDAS
- Digital Still Cameras
- Portable Media Players
- Wireless-LAN

○ABSOLUTE MAXIMUM RATING(Ta=25℃)

Parameter	Symbol	Limit	Unit
Supply Voltage	VCC	-0.3～+7 *1	V
EN Voltage	VEN	-0.3～+7	V
SW Voltage	VSW	-0.3～+7	V
SW Output Current	ISW	450 *1	mA
Power Dissipation	Pd	510 *2	mW
Operating Temperature Range	Topr	-30～+85	℃
Storage Temperature Range	Tstg	-55～+150	℃
Maximum Junction Temperature	Tjmax	+150	℃

*1 Pd, ASO, and Tjmax=150℃ should not be exceeded.
*2 Derating is 4.08 mW /℃ for temperatures above Ta=25℃
(when mounted on 50mm×58mm×1.75mm glass epoxy PCB which has 8 layers).

○OPERATING CONDITIONS(Ta=-30～+85℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	VCC	2.3	3.3	5.5	V
EN Voltage	VEN	0	-	5.5	V
SW Average Output Current	ISW	-	-	300*3,4	mA

*3 In case set output current 300mA, VccMin.=2.7V.
*4 Pd and ASO should not be exceeded.

This product is not designed for protection against radioactive rays.

Status of this document
The Japanese version of this document is the formal specification. This translated version is exclusively intended as a reference, and may only be used as an auxiliary aid in reading the formal version. If there are any differences between the Japanese and translated versions of this document, the formal version takes priority.

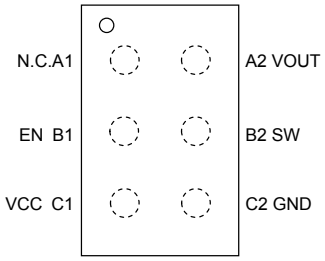
Apr.2008

○ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, Ta=25℃, VCC =3.3V, EN=VCC)

Parameter	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
Standby Current	ISTB	-	0	2	μA	EN=0V
Bias Current	ICC	-	200	350	μA	
EN Low Voltage	VENL	-	GND	0.3	V	Standby Mode
EN High Voltage	VENH	0.95	Vcc	-	V	Active Mode
EN Input Current	IEN	-	1	2	μA	VEN=2V
Oscillation Frequency	FOSC	1.6	2	2.4	MHz	
Pch FET ON Resistance	RONP	-	0.6	1.2	Ω	Vcc=3.3V
Nch FET ON Resistance	RONN	-	0.5	1.0	Ω	Vcc=3.3V
Output Voltage	VOUT	1.846	1.875	1.903	V	±1.5%
UVLO Threshold Voltage	VUVLO1	2.0	2.1	2.2	V	Vcc=3.3→0V
UVLO Release Voltage	VUVLO2	2.02	2.15	2.3	V	Vcc=0→3.3V
Soft Start Time	TSS	0.1	0.2	0.4	ms	
Timer Latch Time	TLATCH	0.25	0.5	1	ms	SCP/TSD Operational Mode
Output Short circuit Threshold Voltage	VSCP	-	0.93	1.31	V	VOUT=1.875→0V

●Block Diagram



TOP View
VCSP50L1

Fig.1 Pin Distribution

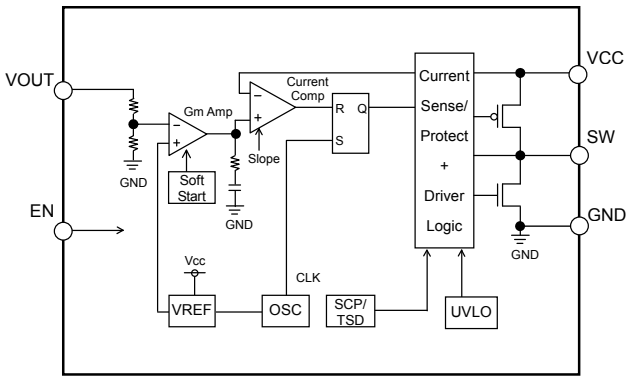
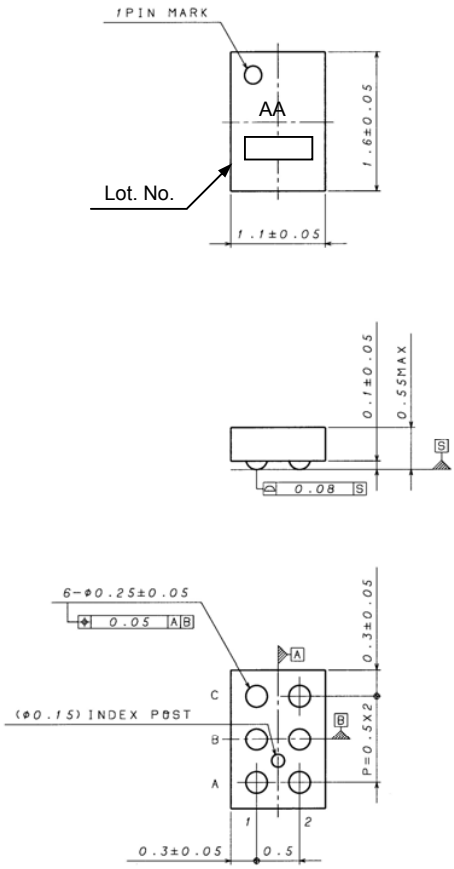


Fig.2 Block Diagram



VCSP50L1

Fig.3 Physical Dimension

●Pin No. & Pin name

Pin No.	Pin name	PIN function
A1	N.C.	N.C. pin
B1	EN	Enable pin(Active High)
C1	VCC	Vcc power supply input pin / Pch FET source pin
A2	VOUT	Output voltage pin
B2	SW	Pch/Nch FET drain output pin
C2	GND	Ground pin/ Nch FET source pin

●Characteristics data【BD9180GUL】

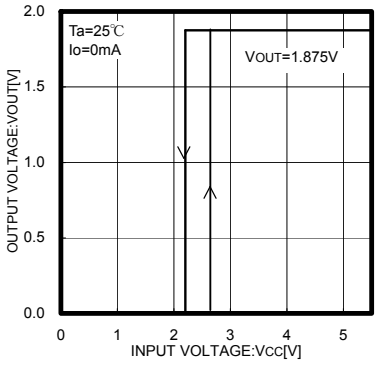


Fig.4 Vcc-VOUT

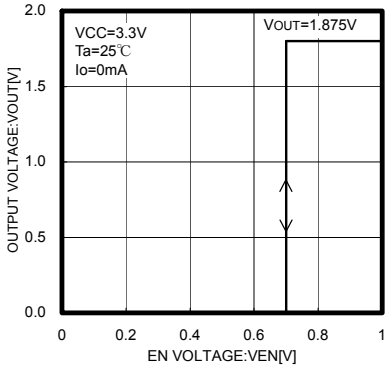


Fig.5 EN-VOUT

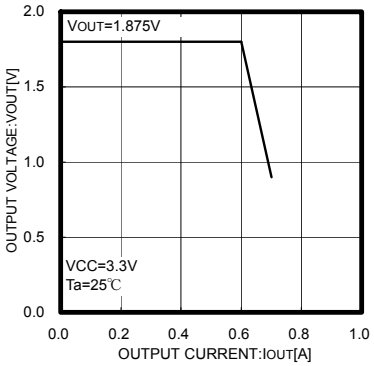


Fig.6 IOUT-VOUT

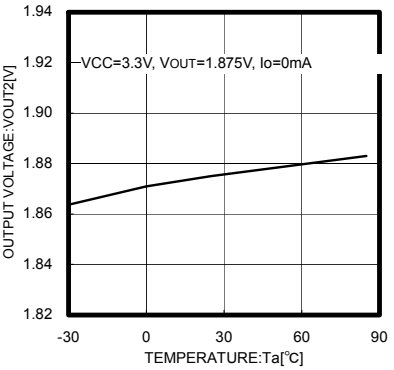


Fig.7 Ta-VOUT

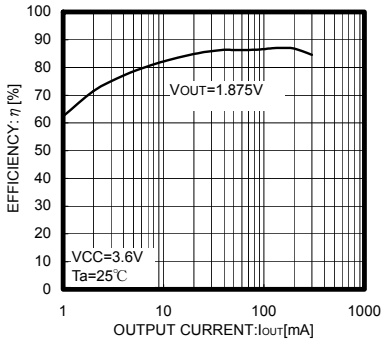


Fig.8 Efficiency

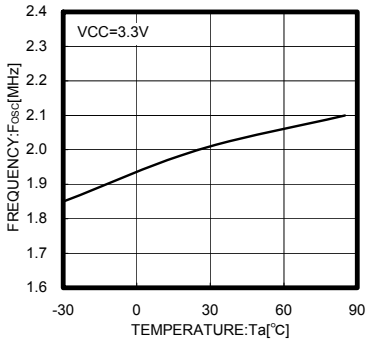


Fig.9 Ta--Fosc

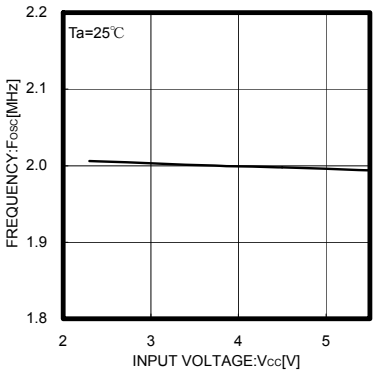


Fig.10 Vcc-Fosc

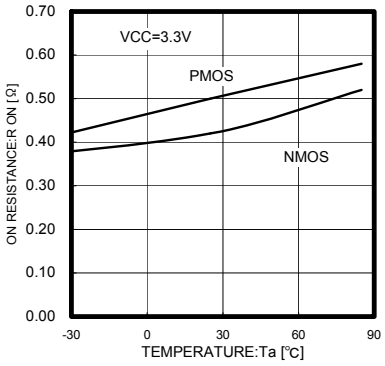


Fig.11 Ta-NMOS-PMOS FET Ron

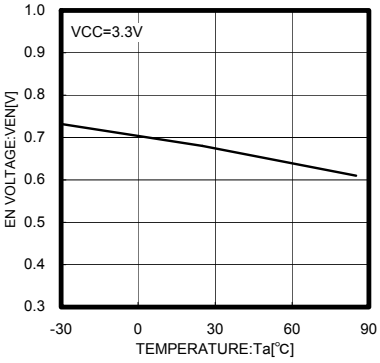


Fig.12 Ta-V_{EN}

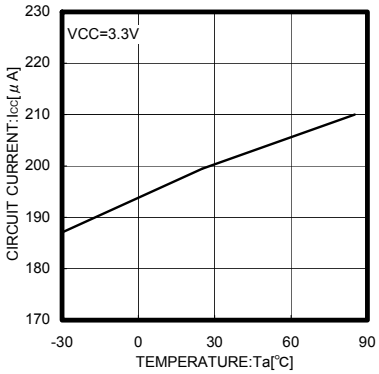


Fig.13 Ta-Icc

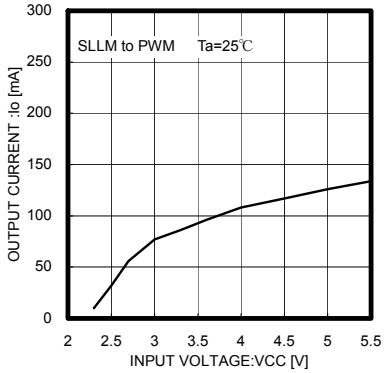


Fig.14 Input Voltage – Output Current at mode change point

●特性データ【BD9180GUL】

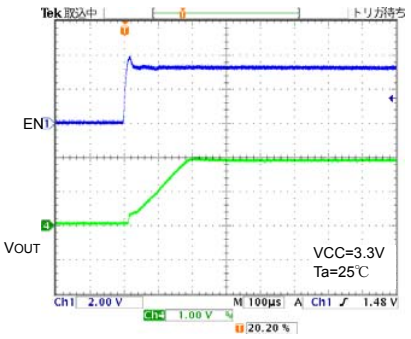


Fig.15 Soft start waveform
(Io=0mA)

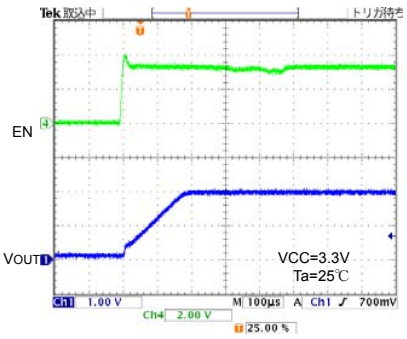


Fig.16 Soft start waveform
(Io=300mA)

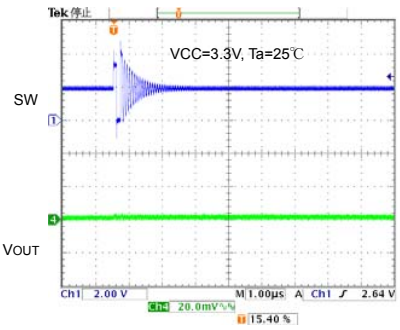


Fig.17 SW start waveform
(Io=0mA)

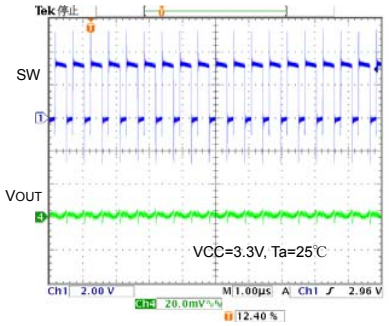


Fig.19 SW start waveform
(Io=300mA)

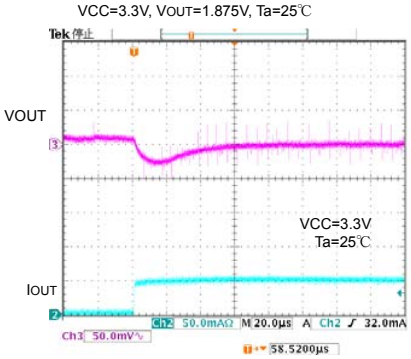


Fig.20 Transient Response
Io=1→50mA/μs

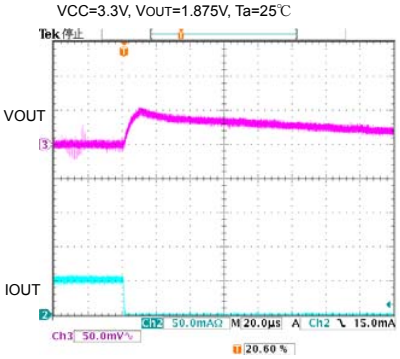


Fig.21 Transient Response
Io=50→1mA/μs

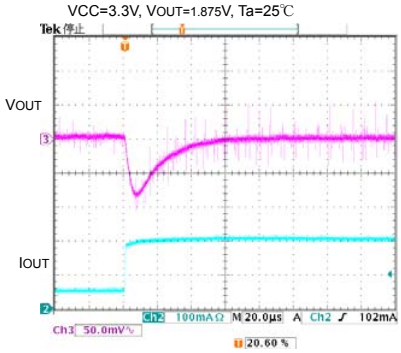


Fig.22 Transient Response
Io=50→200mA/μs

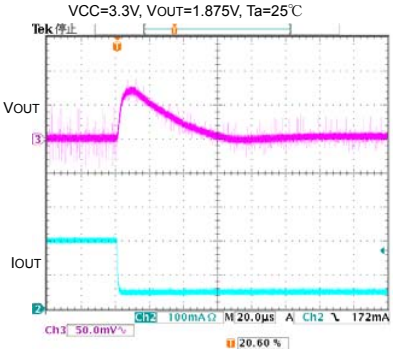
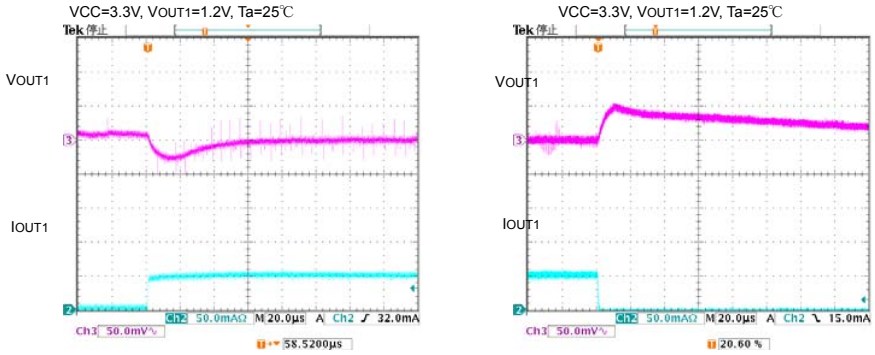


Fig.23 Transient Response
Io=200→50mA/μs

●Information on advantages

Advantage 1 : Offers fast transient response with current mode control system.

BD9180GUL(transient response Io=1mA⇔50mA/μs)



Io=1→50mA　　Io=50→1mA

Fig.24 Comparison of transient response

Advantage 2 : Offers high efficiency for all load range.

・For lighter load:

Utilizes the current mode control mode called SLLM for lighter load, which reduces various dissipation such as switching dissipation (P_{SW}), gate charge/discharge dissipation, ESR dissipation of output capacitor (P_{ESR}) and on-resistance dissipation (P_{RON}) that may otherwise cause degradation in efficiency for lighter load.

⬇

Achieves efficiency improvement for lighter load.

・For heavier load:

Utilizes the synchronous rectifying mode and the low on-resistance MOS FETs incorporated as power transistor.

{ ON resistance of P-channel MOS FET : 0.6Ω (Typ.)
{ ON resistance of N-channel MOS FET : 0.5Ω (Typ.)

⬇

Achieves efficiency improvement for heavier load.

Offers high efficiency for all load range with the improvements mentioned above.

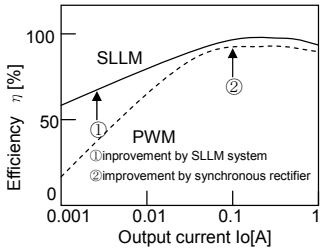


Fig.25 Efficiency

Advantage 3 : ・Supplied in smaller package due to small-sized power MOS FET incorporated.

⬇

・Output capacitor Co required for current mode control: 10μF ceramic capacitor.
・Inductance L required for the operating frequency of 2 MHz: 2.2μH inductor.

Reduces a mounting area required.

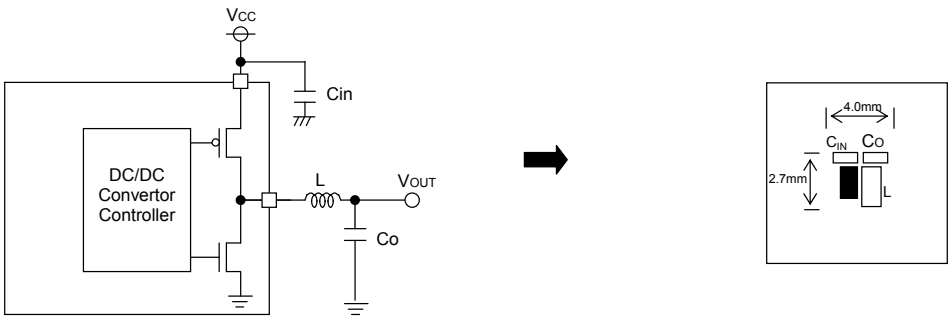


Fig.26 Example application

●Operation

BD919□GUL is a synchronous rectifying dual step-down switching regulator that achieves faster transient response by employing current mode PWM control system. It utilizes switching operation in PWM (Pulse Width Modulation) mode for heavier load, while it utilizes SLLM (Simple Light Load Mode) operation for lighter load to improve efficiency.

○Synchronous rectifier

It does not require the power to be dissipated by a rectifier externally connected to a conventional DC/DC converter IC, and its P.N junction shoot-through protection circuit limits the shoot-through current during operation, by which the power dissipation of the set is reduced.

○Current mode PWM control

Synthesizes a PWM control signal with a inductor current feedback loop added to the voltage feedback.

・PWM (Pulse Width Modulation) control

The oscillation frequency for PWM is 2 MHz. SET signal form OSC turns ON a P-channel MOS FET (while a N-channel MOS FET is turned OFF), and an inductor current I_L increases. The current comparator (Current Comp) receives two signals, a current feedback control signal (SENSE: Voltage converted from I_L) and a voltage feedback control signal (FB), and issues a RESET signal if both input signals are identical to each other, and turns OFF the P-channel MOS FET (while a N-channel MOS FET is turned ON) for the rest of the fixed period. The PWM control repeat this operation.

・SLLM (Simple Light Load Mode) control

When the control mode is shifted from PWM for heavier load to the one for lighter load or vise versa, the switching pulse is designed to turn OFF with the device held operated in normal PWM control loop, which allows linear operation without voltage drop or deterioration in transient response during the mode switching from light load to heavy load or vise versa.

Although the PWM control loop continues to operate with a SET signal from OSC and a RESET signal from Current Comp, it is so designed that the RESET signal is held issued if shifted to the light load mode, with which the switching is tuned OFF and the switching pulses are thinned out under control. Activating the switching intermittently reduces the switching dissipation and improves the efficiency.

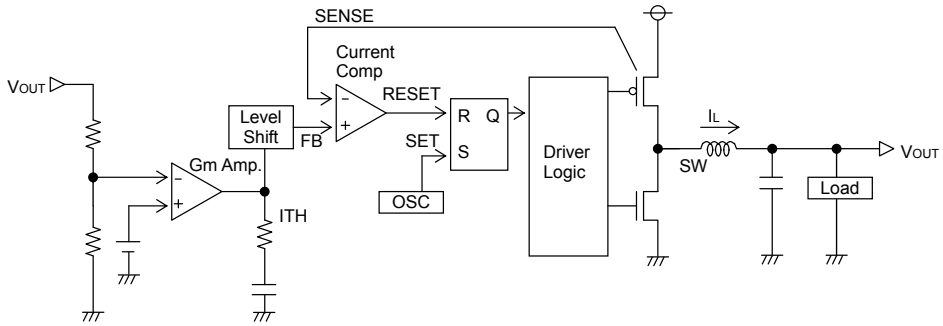


Fig.27 Diagram of current mode PWM control

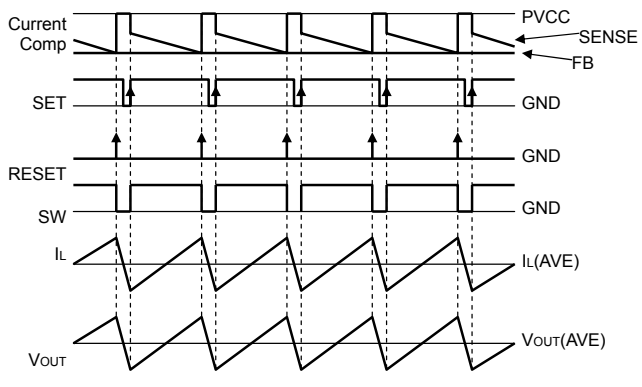


Fig.28 PWM switching timing chart

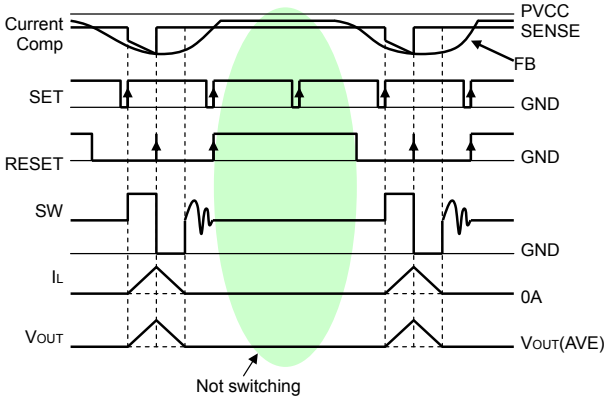


Fig.29 SLLM™ switching timing chart

●Description of operations

・Shutdown function

The device has a separate EN pin for esch converter to start up each converter independently.

If EN1 and EN2 are set to Low(<0.3V), all circuits are OFF and the device is Stand by mode.(I_{STB}=0uA typ). If EN1 and EN2 are set to High(>0.95V), thus is Active mode.

・Soft-start function

EN terminal shifted to “High” activates a soft-starter to gradually establish the output voltage with the current limited during startup, by which it is possible to prevent an overshoot of output voltage and an inrush current.

・UVLO function

Detects whether the input voltage sufficient to secure the output voltage of this IC is supplied. And the hysteresis width of 50 mV (Typ.) is provided to prevent output chattering.

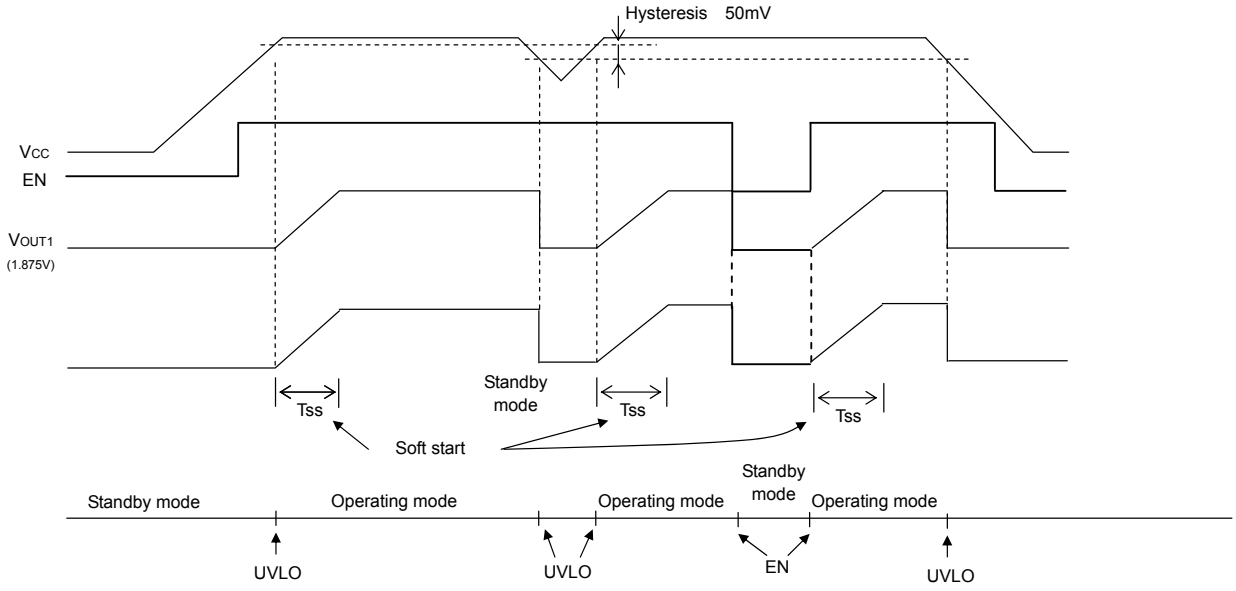


Fig.30 Soft start, Shutdown, UVLO timing chart

・Short-current protection circuit with time delay function

Turns OFF the output to protect the IC from breakdown when the incorporated current limiter of the other converter is activated continuously for the fixed time(T_{LATCH}) or more. The output thus held tuned OFF may be recovered by restarting EN or by re-unlocking UVLO.

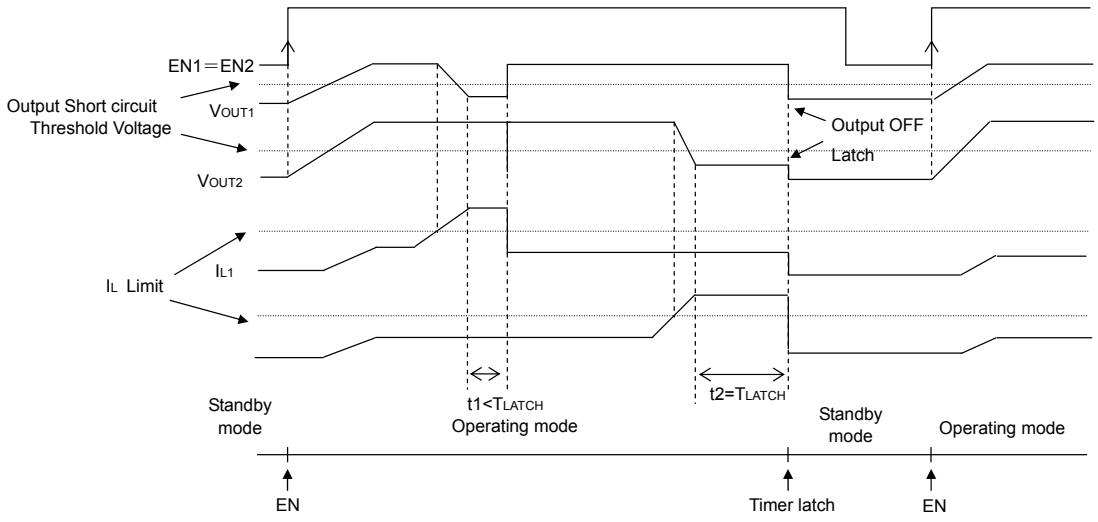


Fig.31 Short-current protection circuit with time delay timing chart

●Switching regulator efficiency

Efficiency η may be expressed by the equation shown below:

$$\eta = \frac{V_{OUT} \times I_{OUT}}{Vin \times Iin} \times 100[\%] = \frac{P_{OUT}}{Pin} \times 100[\%] = \frac{P_{OUT}}{P_{OUT}+P_D \alpha} \times 100[\%]$$

Efficiency may be improved by reducing the switching regulator power dissipation factors $P_D\alpha$ as follows:

Dissipation factors:

1) ON resistance dissipation of inductor and FET : PD(I^2R)
2) Gate charge/discharge dissipation : PD(Gate)
3) Switching dissipation : PD(SW)
4) ESR dissipation of capacitor : PD(ESR)
5) Operating current dissipation of IC : PD(IC)

1)$PD(I^2R)=I_{OUT}^2 \times (R_{COIL}+R_{ON})$ (R_{COIL}[Ω] : DC resistance of inductor, R_{ON}[Ω] : ON resistance of FET, I_{OUT}[A] : Output current.)

2)$PD(Gate)=Cgs \times f \times V$ (Cgs[F] : Gate capacitance of FET,f[H] : Switching frequency,V[V] : Gate driving voltage of FET)

3)$PD(SW)=\frac{Vin^2 \times C_{RSS} \times I_{OUT} \times f}{I_{DRIVE}}$ (C_{RSS}[F] : Reverse transfer capacitance of FET,I_{DRIVE}[A] : Peak current of gate.)

4)$PD(ESR)=I_{RMS}^2 \times ESR$ (I_{RMS}[A] : Ripple current of capacitor,ESR[Ω] : Equivalent series resistance.)

5)$PD(IC)=Vin \times I_{CC}$ (I_{CC}[A] : Circuit current.)

●Consideration on permissible dissipation and heat generation

As this IC functions with high efficiency without significant heat generation in most applications, no special consideration is needed on permissible dissipation or heat generation. In case of extreme conditions, however, including lower input voltage, higher output voltage, heavier load, and/or higher temperature, the permissible dissipation and/or heat generation must be carefully considered.

For dissipation, only conduction losses due to DC resistance of inductor and ON resistance of FET are considered. Because the conduction losses are considered to play the leading role among other dissipation mentioned above including gate charge/discharge dissipation and switching dissipation.

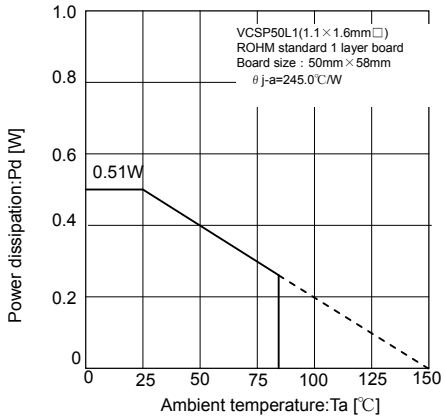


Fig.32 Thermal derating curve
(VCSP50L1)

$P=I_{OUT}^2 \times R_{ON}$

$R_{ON}=D \times R_{ONP}+(1-D)R_{ONN}$

D : ON duty (=V_{OUT}/V_{CC})
R_{COIL} : DC resistance of coil
R_{ONP} : ON resistance of P-channel MOS FET
R_{ONN} : ON resistance of N-channel MOS FET
I_{OUT} : Output current

If V_{CC}=3.3V, V_{OUT}=1.875V, R_{ONP}=0.6Ω, R_{ONN}=0.5Ω
I_{OUT}=0.3A, for example,

$D=V_{OUT}/V_{CC}=1.875/3.3=0.57$

$R_{ON}=0.57 \times 0.6+(1-0.57) \times 0.5$
$=0.342+0.215$
$=0.557[\Omega]$

$P=0.3^2 \times 0.557 \fallingdotseq 50.13[mW]$

As R_{ONP} is greater than R_{ONN} in this IC, the dissipation increases as the ON duty becomes greater. With the consideration on the dissipation as above, thermal design must be carried out with sufficient margin allowed.

●Selection of components externally connected

1. Selection of inductor (L)

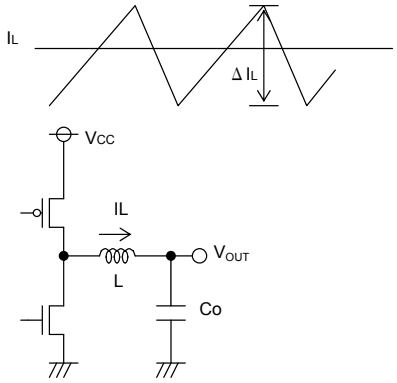


Fig.33 Output ripple current

The inductance significantly depends on output ripple current. As seen in the equation (1), the ripple current decreases as the inductor and/or switching frequency increases.

$$\Delta I_L = \frac{(V_{CC}-V_{OUT})\times V_{OUT}}{L\times V_{CC}\times f}\ [A]\ \cdot\ \cdot\ \cdot (1)$$

Appropriate ripple current at output should be 30% more or less of the maximum output current.

$$\Delta I_L = 0.3\times I_{OUT}\text{max.}\ [A]\ \cdot\ \cdot\ \cdot (2)$$

$$L = \frac{(V_{CC}-V_{OUT})\times V_{OUT}}{\Delta I_L\times V_{CC}\times f}\ [H]\ \cdot\ \cdot\ \cdot (3)$$

(ΔI_L: Output ripple current, and f: Switching frequency)

If VCC=3.3V, VOUT=1.875V, f=2MHz, IOUTmax=0.3A

$\Delta IL = 0.3\times 0.3 = 0.09$ [A]

$$L = \frac{(3.3-1.875)\times 1.875}{0.09\times 3.3\times 2}$$

$$= 4.5[uH]$$

*A 1to4.7uH inductor is recommended to be steady operation and achieve a small application.
Current exceeding the current rating of the inductor results in magnetic saturation of the inductor, which decreases efficiency. The inductor must be selected allowing sufficient margin with which the peak current may not exceed its current rating.

*Select the inductor of low resistance component (such as DCR and ACR) to minimize dissipation in the inductor for better efficiency.

2. Selection of output capacitor (Co)

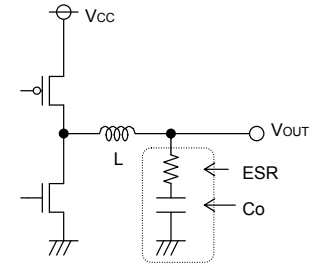


Fig.34 Output capacitor

Output capacitor should be selected with the consideration on the stability region and the equivalent series resistance required to smooth ripple voltage.

Output ripple voltage is determined by the equation (4) :

$\Delta V_{OUT} = \Delta I_L \times ESR$ [V] ・・・(4)

(ΔI_L: Output ripple current, ESR: Equivalent series resistance of output capacitor)

*Rating of the capacitor should be determined allowing sufficient margin against output voltage. Less ESR allows reduction in output ripple voltage.

As the output rise time must be designed to fall within the soft-start time, the capacitance of output capacitor should be determined with consideration on the requirements of equation (5):

$$Co \leqq \frac{T_{SS}\times(I_{limit}-I_{OUT})}{V_{OUT}} \quad \cdot\ \cdot\ \cdot (5)$$

Tss: Soft-start time
Ilimit: Over current detection level, 0.6A(Typ)

if VOUT=1.8V, IOUT=0.3A, and TSS=0.2ms,

$$Co \leqq \frac{0.2m\times(0.6-0.3)}{1.875} \fallingdotseq 33.3\ [\mu F]$$

Inappropriate capacitance may cause problem in startup. 10 μ F to 22 μ F ceramic capacitor is recommended.

3. Selection of input capacitor (Cin)

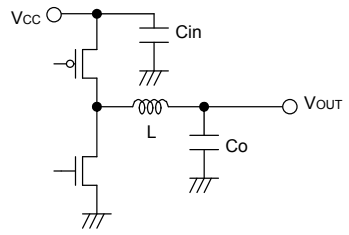


Fig.35 Input capacitor

Input capacitor to select must be a low ESR capacitor of the capacitance sufficient to cope with high ripple current to prevent high transient voltage. The ripple current IRMS is given by the equation (5):

$$I_{RMS}=I_{OUT}\times\frac{\sqrt{V_{OUT}(V_{CC}-V_{OUT})}}{V_{CC}}\ [A]\cdot\cdot\cdot(5)$$

< Worst case > $I_{RMS(max.)}$

When Vcc is twice the V_{OUT}, $I_{RMS}=\frac{I_{OUT}}{2}$

If V_{CC}=3.3V, V_{OUT}=1.V, and $I_{OUTmax.}$=0.3A

$$I_{RMS}=0.3\times\frac{\sqrt{1.875(3.3-1.875)}}{3.3}=0.15[A_{RMS}]$$

A low ESR 4.7 μ F/10V ceramic capacitor is recommended to reduce ESR dissipation of input capacitor for better efficiency.

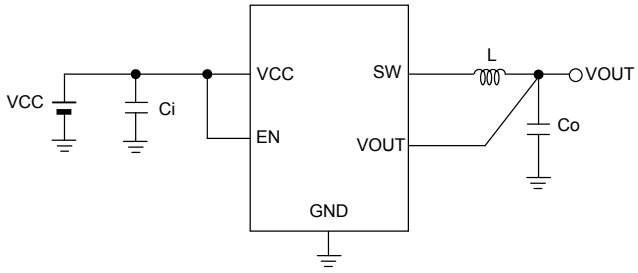


Fig.36 Typical application

●Cautions on PC Board layout

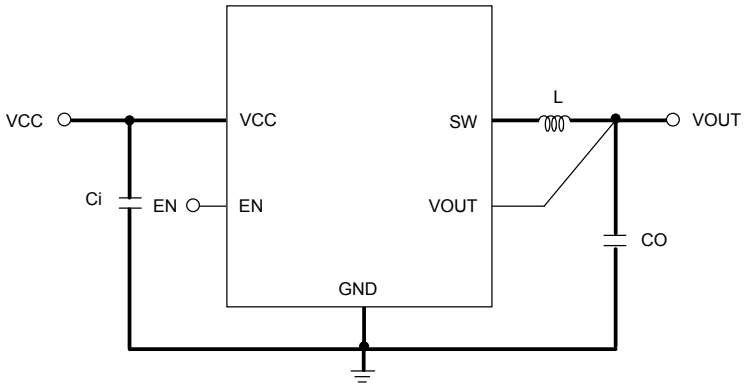


Fig.37 Layout diagram

① For the sections drawn with heavy line, use thick conductor pattern as short as possible.
② Lay out the input ceramic capacitor Ci closer to the pins VCC and GND, and the output capacitor Co1,Co2 closer to the pin GND.

●Recommended components Lists on above application

Symbol	Part	Value	Manufacturer	Series
L	Coil	2.2uH	muRata	LQM21PN2R2MC0
Ci	Ceramic capacitor	10uF	muRata	GRM21BB30J106K
			Kyocera	CM21B106M06A
Co	Ceramic capacitor	10uF	muRata	GRM21BB30J106K
			Kyocera	CM21B106M06A

*The parts list presented above is an example of recommended parts. Although the parts are sound, actual circuit characteristics should be checked on your application carefully before use. Be sure to allow sufficient margins to accommodate variations between external devices and this IC when employing the depicted circuit with other circuit constants modified. Both static and transient characteristics should be considered in establishing these margins. When switching noise is substantial and may impact the system, a schottky barrier diode established between the SW and GND pins.

●I/O equivalent circuit

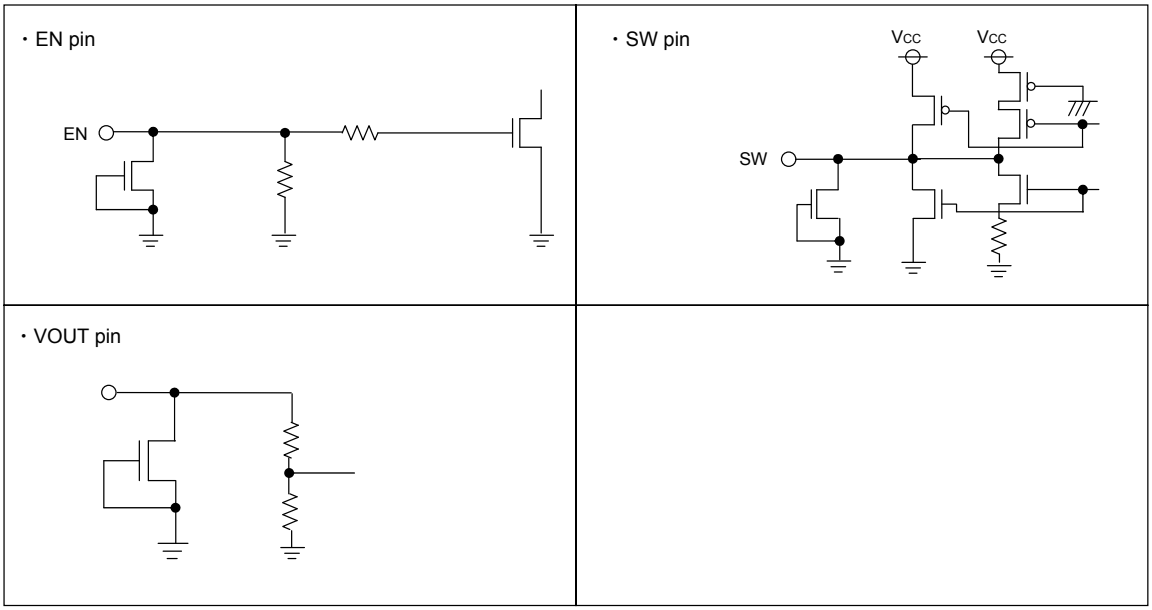


Fig.38 I/O equivalent circuit

●Cautions on use

1. Absolute Maximum Ratings

While utmost care is taken to quality control of this product, any application that may exceed some of the absolute maximum ratings including the voltage applied and the operating temperature range may result in breakage. If broken, short-mode or open-mode may not be identified. So if it is expected to encounter with special mode that may exceed the absolute maximum ratings, it is requested to take necessary safety measures physically including insertion of fuses.

2. Electrical potential at GND

GND must be designed to have the lowest electrical potential In any operating conditions.

3. Short-circuiting between terminals, and mismounting

When mounting to pc board, care must be taken to avoid mistake in its orientation and alignment. Failure to do so may result in IC breakdown. Short-circuiting due to foreign matters entered between output terminals, or between output and power supply or GND may also cause breakdown.

4.Operation in Strong electromagnetic field

Be noted that using the IC in the strong electromagnetic radiation can cause operation failures.

5. Thermal shutdown protection circuit

Thermal shutdown protection circuit is the circuit designed to isolate the IC from thermal runaway, and not intended to protect and guarantee the IC. So, the IC the thermal shutdown protection circuit of which is once activated should not be used thereafter for any operation originally intended.

6. Inspection with the IC set to a pc board

If a capacitor must be connected to the pin of lower impedance during inspection with the IC set to a pc board, the capacitor must be discharged after each process to avoid stress to the IC. For electrostatic protection, provide proper grounding to assembling processes with special care taken in handling and storage. When connecting to jigs in the inspection process, be sure to turn OFF the power supply before it is connected and removed.

7. Input to IC terminals

This is a monolithic IC with P^+ isolation between P-substrate and each element as illustrated below. This P-layer and the N-layer of each element form a P-N junction, and various parasitic element are formed.

If a resistor is joined to a transistor terminal as shown in Fig 39.

○P-N junction works as a parasitic diode if the following relationship is satisfied; GND>Terminal A (at resistor side), or GND>Terminal B (at transistor side); and

○if GND>Terminal B (at NPN transistor side),

a parasitic NPN transistor is activated by N-layer of other element adjacent to the above-mentioned parasitic diode.

The structure of the IC inevitably forms parasitic elements, the activation of which may cause interference among circuits, and/or malfunctions contributing to breakdown. It is therefore requested to take care not to use the device in such manner that the voltage lower than GND (at P-substrate) may be applied to the input terminal, which may result in activation of parasitic elements.

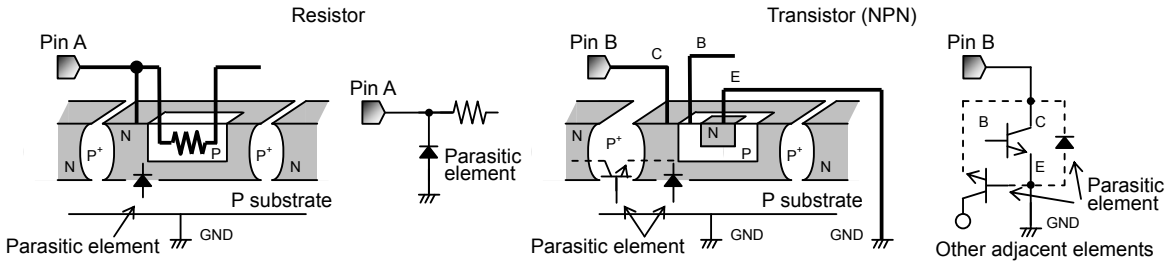


Fig.39 Simplified structure of monorisic IC

8. Ground wiring pattern

If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

● Type Designations (Selections) for Ordering

B	D	9	1	8	0	G	U	L	-	E	2

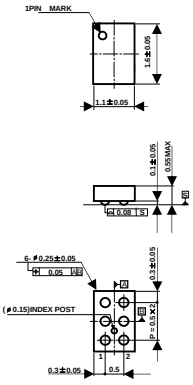
Product name
- **BD9180**

Package type
GUL : VCSP50L1

E2 Emboss tape reel Pin 1 opposite draw-out side

VCSP50L1

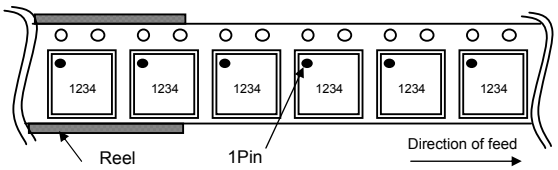
<Dimension>



(Unit:mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



※When you order , please order in times the amount of package quantity.

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