ROHM SEMICONDUCTOR

# TECHNICAL NOTE

**Single-chip Type with Built-in FET Switching Regulator Series**

Pb Free ROHM Electronic Components RoHS Directive Compliance

# High-efficiency Step-up Switching Regulator with Built-in Power MOSFET

## BD8311NUV

● General Description

ROHM's High-efficiency Step-up Switching Regulator Built-in Power MOSFET BD8311NUV generates step-up output including 8 V or 10 V from 4 batteries, batteries such as Li2cell etc. or a 5 V fixed power supply line.
This IC allows easy production of small and a wide range of output current, and is equipped with an external coil/capacitor downsized by high frequency operation of 1.2 MHz, built-in 2.5 A rated 80 mΩ Nch FET SW, and flexible phase compensation system on board.

● Features

1) Incorporates Nch FET capable of withstanding 2.5 A/14 V.
2) Incorporates phase compensation device between input and output of ERROR AMP.
3) Small coils and capacitors to be used by high frequency operation of 1.2 MHz
4) Input voltage 3.5 V – 11 V
5) Output current 600 mA (3.5 V – 10 V) at 10 V
800 mA (3.5 V – 8 V) at 8 V
6) Incorporates soft-start function.
7) Incorporates timer latch system short protecting function.
8) As small as 3 mm□, SON 10-pin package VSON010V3030

● Application

General portable equipment like DSC/DVC powered by 4 dry batteries or Li2cell

●Operating Conditions (Ta = 25°C)

| Parameter | Symbol | Voltage range | Unit |
|---|---|---|---|
| Power supply voltage | Vcc | 3.5 to 11 | V |
| Output voltage | VOUT | 4.0 to 11 | V |

●Absolute Maximum Ratings

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Maximum applied power voltage | VCC, LX | 14 | V |
| Maximum input voltage | SWOUT, INV | 14 | V |
| Maximum input current | Iinmax | 2.5 | A |
| Power dissipation | Pd | 700 | mW |
| Operating temperature range | Topr | -25 to +85 | °C |
| Storage temperature range | Tstg | -55 to +150 | °C |
| Junction temperature | Tjmax | +150 | °C |

*1 When used at Ta = 25°C or more installed on a 74.2 × 74.2 × 1.6t mm board, the rating is reduced by 5.6 mW/°C.

* These specifications are subject to change without advance notice for modifications and other reasons.

Mar. 2009

● Electrical Characteristics
(Unless otherwise specified, Ta = 25 °C, VCC = 7.4 V)

| Parameter | Symbol | Target Value | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Minimum | Typical | Maximum | | |
| [Low voltage input malfunction preventing circuit] | | | | | | |
| Detection threshold voltage | $V_{UV}$ | - | 2.9 | 3.2 | V | VREG monitor |
| Hysteresis range | $\Delta V_{UVhy}$ | 100 | 200 | 300 | mV | |
| [Oscillator] | | | | | | |
| Oscillation frequency | fosc | 1.1 | 1.2 | 1.3 | MHz | |
| [Regulator] | | | | | | |
| Output voltage | VREG | 4.65 | 5.0 | 5.35 | V | |
| [ERROR AMP] | | | | | | |
| INV threshold voltage | VINV | 0.99 | 1.00 | 1.01 | V | |
| Input bias current | IINV | -50 | 0 | 50 | nA | Vcc=11.0V , $V_{INV}$=5.5V |
| Soft-start time | Tss | 5.3 | 8.8 | 12.2 | msec | |
| [PWM comparator] | | | | | | |
| LX Max Duty | Dmax1 | 77 | 85 | 93 | % | |
| [SWOUT] | | | | | | |
| ON resistance | $R_{ONSWOUT}$ | - | 50 | 100 | Ω | |
| [Output] | | | | | | |
| LX NMOS ON resistance | $R_{ON}$ | - | 80 | 150 | mΩ | |
| LX leak current | Ileak | -1 | 0 | 1 | uA | |
| [STB] | | | | | | |
| STB pin control voltage — Operation | $V_{STBH}$ | 2.5 | - | 11 | V | |
| STB pin control voltage — No-operation | $V_{STBL}$ | -0.3 | - | 0.3 | V | |
| STB pin pull-down resistance | $R_{STB}$ | 250 | 400 | 700 | kΩ | |
| [Circuit current] | | | | | | |
| Standby current VCC | $I_{STB}$ | - | - | 1 | uA | |
| Circuit current at operation VCC | Icc | - | 600 | 900 | uA | $V_{INV}$=1.2V |

⊙ Not designed to be resistant to radiation

● Description of Pins

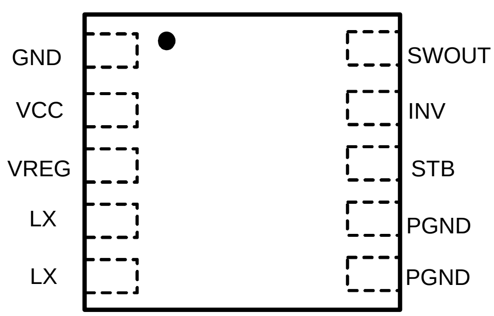



Fig.1 Pin layout

| Pin No. | Pin Name | Function |
|---|---|---|
| 1 | GND | Ground terminal |
| 2 | VCC | Control part power input terminal |
| 3 | VREG | 5 V output terminal of regulator for internal circuit |
| 4～5 | Lx | Coil connecting terminal |
| 6～7 | PGND | Power transistor ground terminal |
| 8 | STB | ON/OFF terminal |
| 9 | INV | ERROR AMP input terminal |
| 10 | SWOUT | STBSW for split resistance |

● Block Diagram

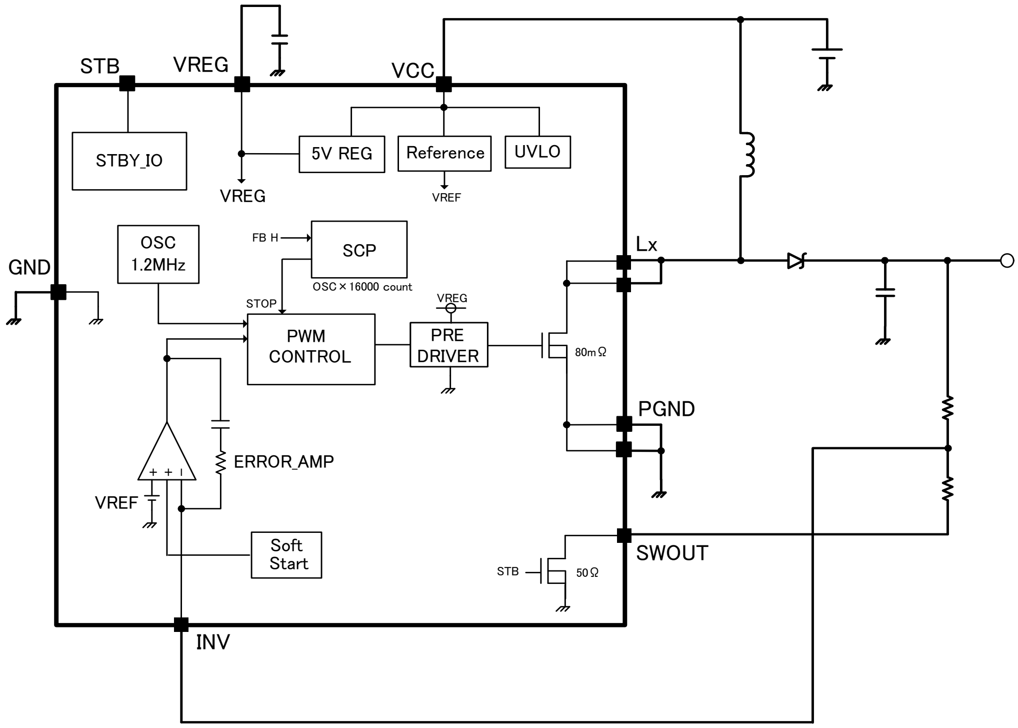



Fig.2 Block diagram

● Description of Blocks

1. VREF
   This block generates ERROR AMP reference voltage.
   The reference voltage is 1.0 V.

2. UVLO
   Circuit for preventing low voltage malfunction
   Prevents malfunction of the internal circuit at activation of the power supply voltage or at low power supply voltage. Monitors VCC pin voltage to turn off all output FET and DC/DC converter output when VCC voltage is lower than 2.9 V, and reset the timer latch of the internal SCP circuit and soft-start circuit. This threshold contains 200 mV hysteresis.

3. SCP
   Timer latch system short-circuit protection circuit
   When the INV pin is the set 1.0 V or lower voltage, the internal SCP circuit starts counting.
   The internal counter is in synch with OSC; the latch circuit activates after a lapse of 13.3 msec after the counter counts about 16000 oscillations and then, turn off DC/DC converter output.
   To reset the latch circuit, turn off the STB pin once. Then, turn it on again or turn on the power supply voltage again.

4. OSC
   Circuit for oscillating sawtooth waves with an operation frequency fixed at 1.2 MHz

5. ERROR AMP
   Error amplifier for detecting output signals and outputting PWM control signals
   The internal reference voltage is set at 1.0 V.
   A primary phase compensation device of 200 pF, 62 kΩ is built in between the inverting input terminal and the output terminal of this ERROR AMP.

6. PWM COMP
   Voltage-pulse width converter for controlling output voltage corresponding to input voltage
   Comparing the internal SLOPE waveform with the ERROR AMP output voltage, PWM COMP controls the pulse width to the output to the driver.
   Max Duty is set at 85%.

7. SOFT START
   Circuit for preventing in-rush current at startup by bringing the output voltage of the DC/DC converter into a soft-start
   Soft-start time is in synch with the internal OSC, and the output voltage of the DC/DC converter reaches the set voltage after about 10000 oscillations .

8. PRE DRIVER
   CMOS inverter circuit for driving the built-in Nch FET.

9. STBY_IO
   Voltage applied on STB pin (8 pin) to control ON/OFF of IC
   Turned ON when a voltage of 2.5 V or higher is applied and turned OFF when the terminal is open or 0 V is applied.
   Incorporates approximately 400 kΩ pull-down resistance.

10. Nch FET SW
   Built-in SW for switching the coil current of the DC/DC converter. Incorporates an 80 mΩ NchFET SW capable of withstanding 14 V.
   Since the current rating of this FET is 2.5 A, it should be used within 2.5 A including the DC current and ripple current of the coil.

● Reference Data

(Unless otherwise specified, Ta = 25°C, VCC = 7.4 V)

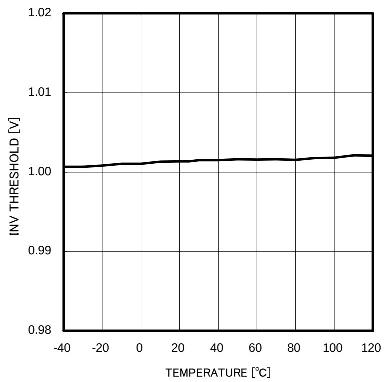



Fig.3. INV threshold temperature property

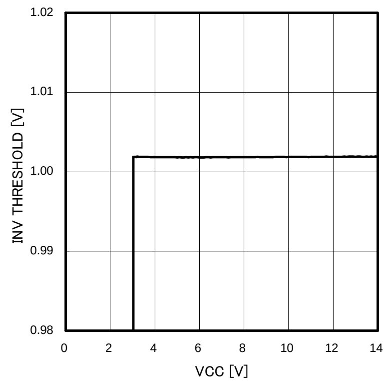



Fig.4. INV threshold power supply property

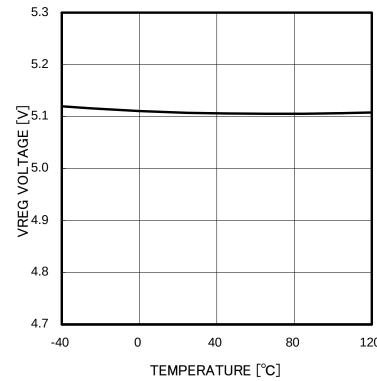



Fig.5. VREG output temperature property

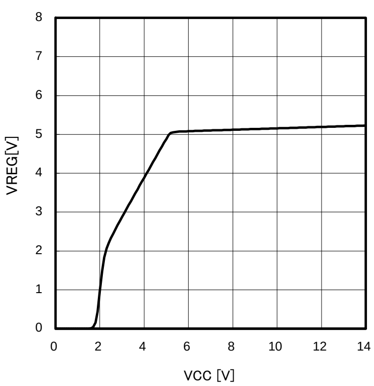



Fig.6. VREG output power supply property

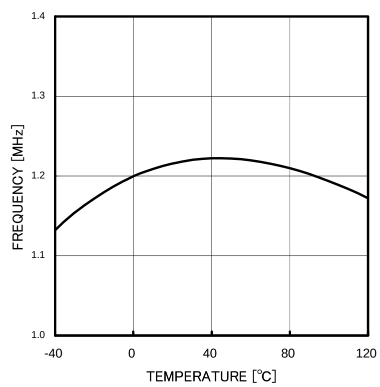



Fig.7. fosc temperature

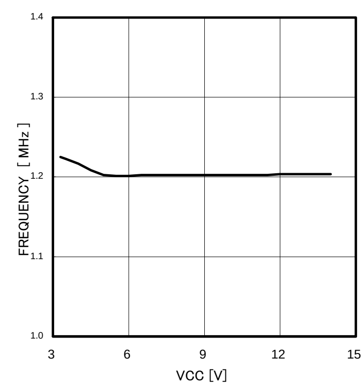



Fig.8. fosc voltage

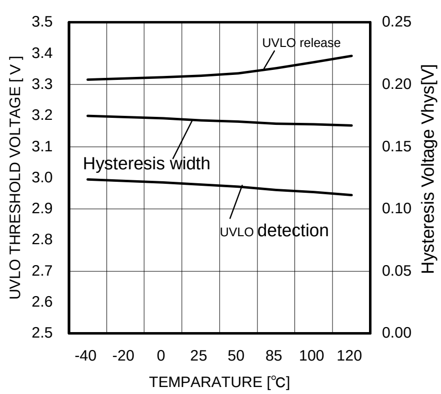



Fig.9. UVLO threshold temperature property

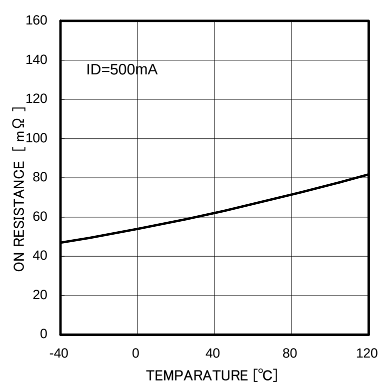



Fig.10. Nch FET ON resistance temperature

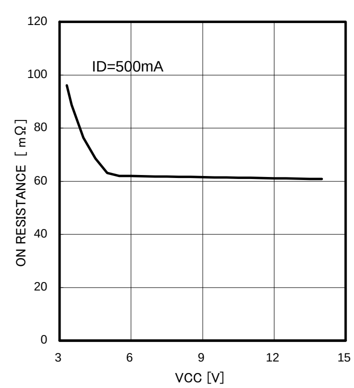



Fig.11. Nch FET ON resistance power supply

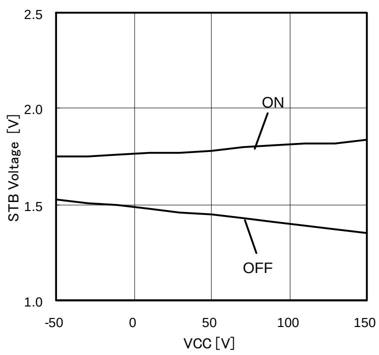



Fig.12. STB threshold temperature property

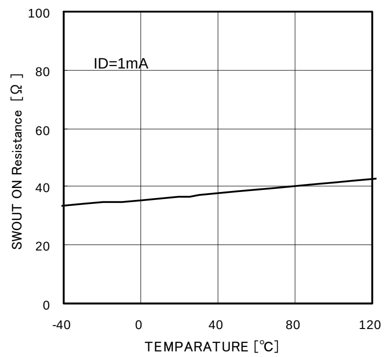



Fig.13. SWOUT ON resistance temperature property

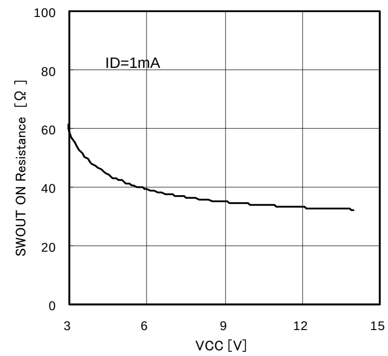



Fig.14. SWOUT ON resistance power supply property

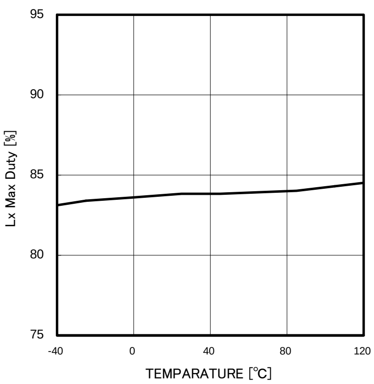



Fig.15. Lx Max duty temperature property

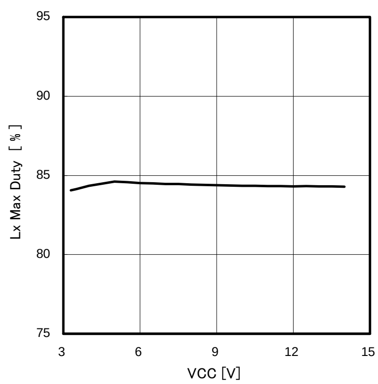



Fig.16. Lx Max duty power supply property

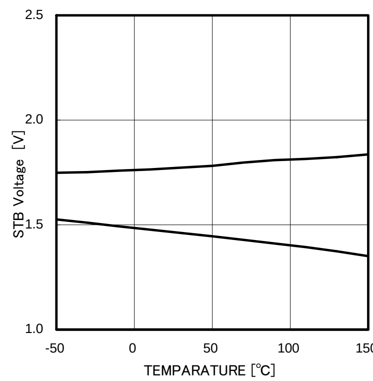



Fig.17. Circuit current temperature property

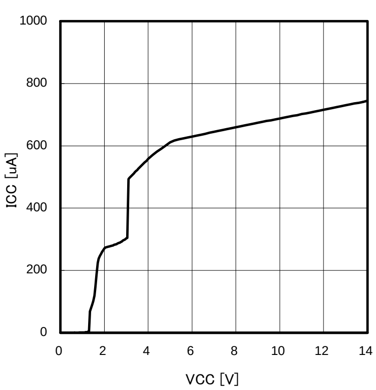



Fig.18. Circuit current power supply property

● Example of Application Input: 3.5 to 10 V, output: 10.1 V / 500 mA

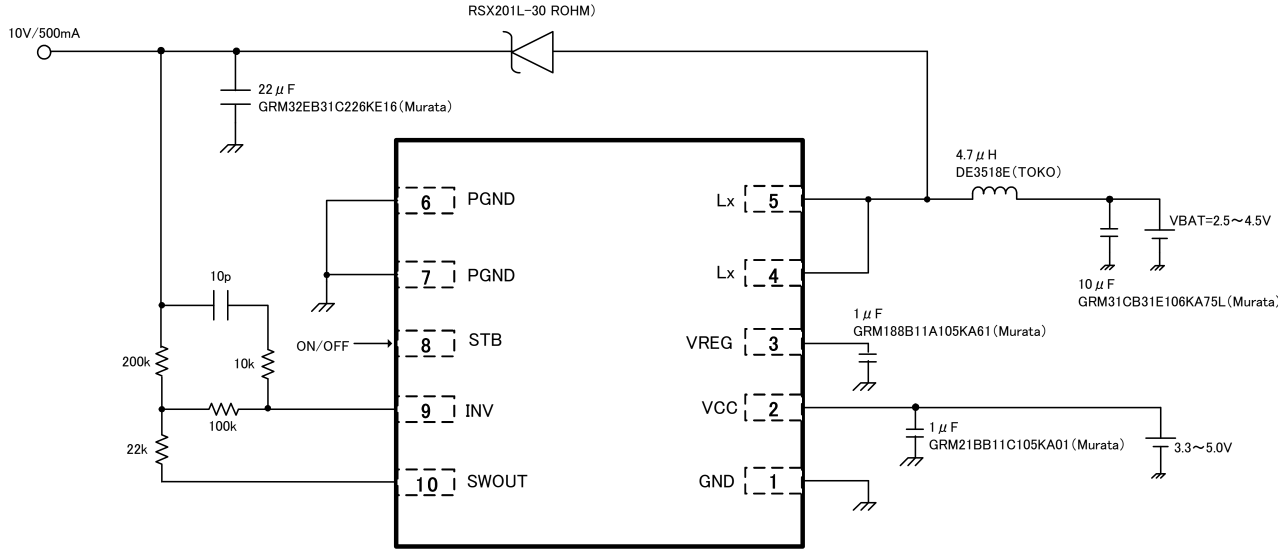



Fig.19 Reference application diagram

● Reference Application Data 1

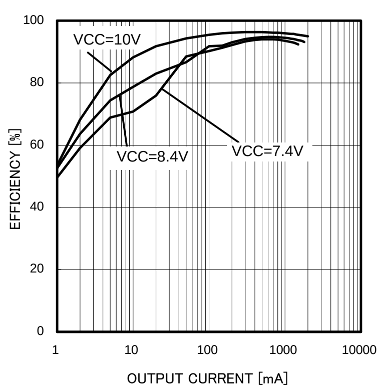



Fig.20 Power conversion

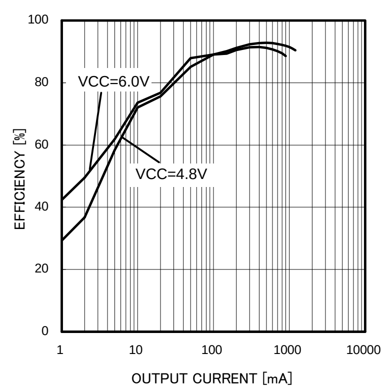



Fig.21 Power conversion

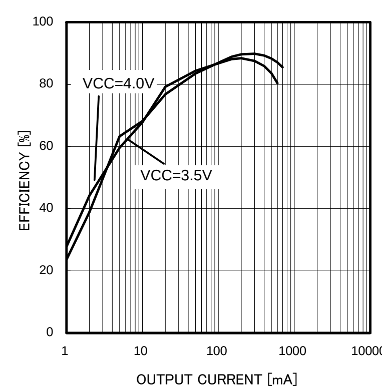



Fig.22 Power conversion

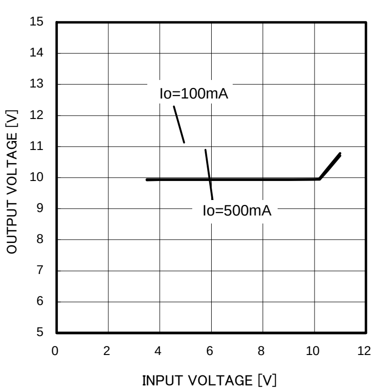



Fig.23 Line regulation

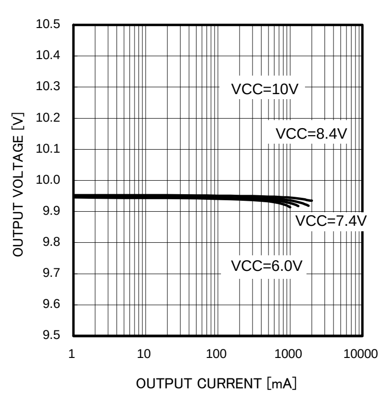



Fig.24 Load regulation 1

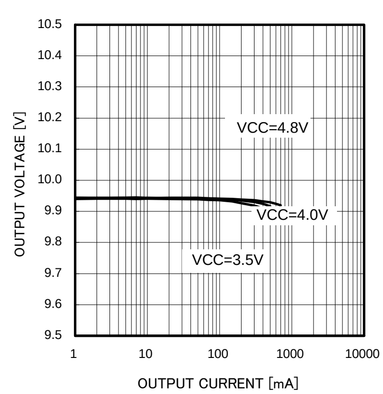



Fig.25 Load regulation 2

● Reference Application Data 2 (VCC = 3.5 V, 6.0 V, 8.4 V, VOUT = 10 V)

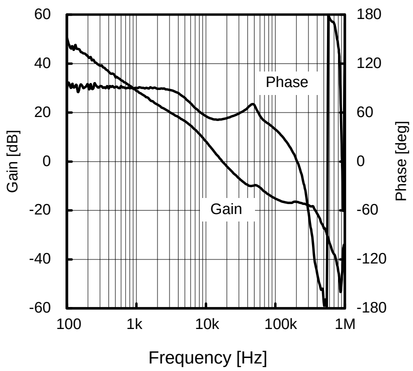


Fig.26 Frequency response property 1
(VCC = 3.5 V, Io = 200 mA)

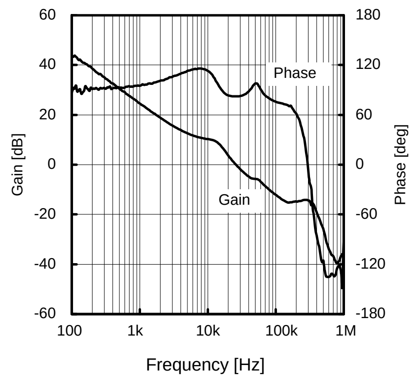


Fig.27 Frequency response property 2
(VCC = 6.0 V, Io = 200 mA)

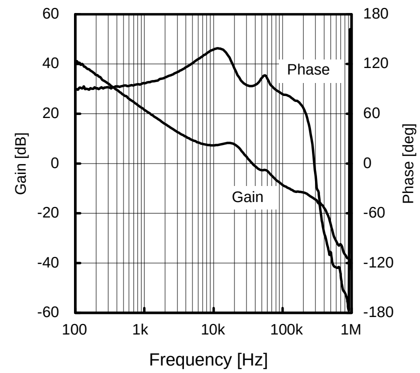


Fig.28 Frequency response property 3
(VCC = 8.4 V, Io = 200 mA)

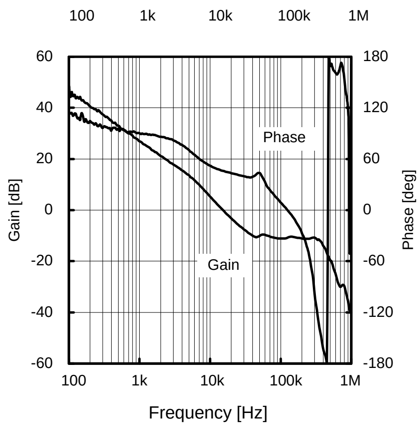


Fig.29 Frequency response property 4
(VCC = 3.5 V, Io = 500 mA)

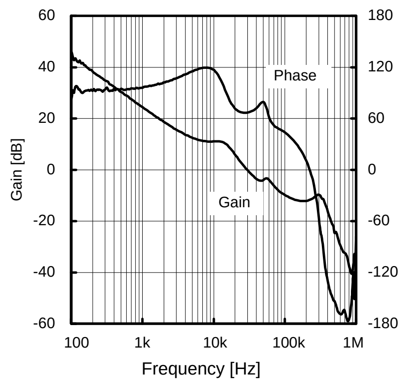


Fig.30 Frequency response property 5
(VCC = 6.0 V, Io = 500 mA)

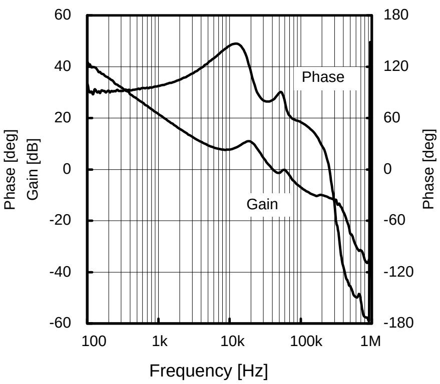
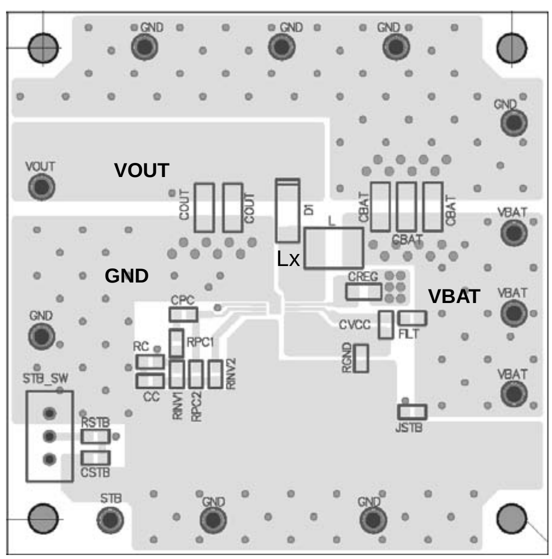


Fig.31 Frequency response property 6
(VCC = 8.4 V, Io = 500 mA)

● Reference Board Pattern




- The radiation plate on the rear should be a GND flat surface of low impedance in common with the PGND flat surface.
- It is recommended to install a GND pin in another system as shown in the drawing without connecting it directly to this PGND

● Selection of Part for Applications

(1) Inductor

A shielded inductor that satisfies the current rating (current value, Ipecac as shown in the drawing below) and has a low DCR (direct resistance component) is recommended.
Inductor values affect inductor ripple current, which will cause output ripple.
Ripple current can be reduced as the coil L value becomes larger and the switching frequency becomes higher.

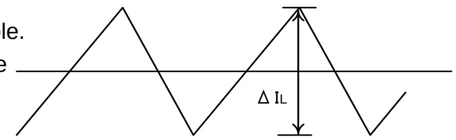


Fig.32 Inductor current

$$I_{peak} = I_{out} \times (V_{out}/V_{IN}) / \eta + \Delta I_L/2 \text{ [A]} \quad (1)$$

$$\Delta I_L = \frac{V_{in}}{L} \times \frac{V_{out} - V_{in}}{V_{out}} \times \frac{1}{f} \text{ [A]} \quad (2)$$

(η: Efficiency, ΔIL: Output ripple current, f: Switching frequency)

As a guide, inductor ripple current should be set at about 20 to 50% of the maximum input current.

* Current over the coil rating flowing in the coil brings the coil into magnetic saturation, which may lead to lower efficiency or output oscillation. Select an inductor with an adequate margin so that the peak current does not exceed the rated current of the coil.

(2) Output capacitor

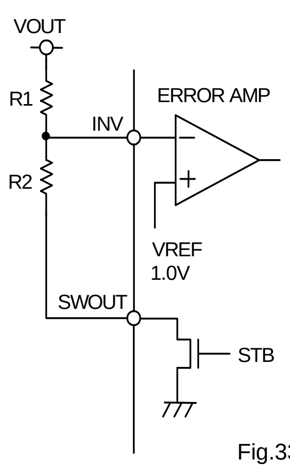
A ceramic capacitor with low ESR is recommended for output in order to reduce output ripple.
There must be an adequate margin between the maximum rating and output voltage of the capacitor, taking the DC bias property into consideration.
Output ripple voltage is obtained by the following equation.

$$V_{pp} = I_{out} \times \frac{V_{out} - V_{in}}{f \times C_o \times V_{out}} + I_{out} \times R_{ESR} \quad \text{[V]} \quad \dots (3)$$

Setting must be performed so that output ripple is within the allowable ripple voltage.

(3) Output voltage setting

The internal reference voltage of the ERROR AMP is 1.0 V. Output voltage is obtained by Equation (4) of Fig. 33, but it should be designed taking about 50 Ω, an error of NMOS ON resistance of SWOUT into consideration.




$$V_o = \frac{(R1+R2)}{R2} \times 1.0 \text{ [V]} \quad \cdots \quad (4)$$

Fig.33 Setting of voltage feedback resistance

(4) DC/DC converter frequency response adjustment system

Condition for stable application

The condition for feedback system stability under negative feedback is that the phase delay is 135 °or less when gain is 1 (0 dB).

Since DC/DC converter application is sampled according to the switching frequency, the bandwidth GBW of the whole system (frequency at which gain is 0 dB) must be controlled to be equal to or lower than 1/10 of the switching frequency.

In summary, the conditions necessary for the DC/DC converter are:

- Phase delay must be 135°or lower when gain is 1 (0 dB).
- Bandwidth GBW (frequency when gain is 0 dB) must be equal to or lower than 1/10 of the switching frequency.

To satisfy above two items, $R_1$, $R_2$, $R_3$, $D_S$ and $R_S$ in Fig. 34 should be set as follows.

[1] $R_1$, $R_2$, $R_3$

BD8311NUV incorporates phase compensation devices of R4=62 kΩ and C2=200pF. These C2 and $R_1$, $R_2$, and $R_3$ values decide the prim ary pole that determines the bandwidth of DC/DC converter.

Primary pole point frequency

$$fp=\frac{1}{2\pi\left\{A\times\left(\frac{R_1\cdot R_2}{R_1+R_2}+R_3\right)\times C_2\right\}} \quad \cdots\cdots\cdots\cdots\cdots (1)$$

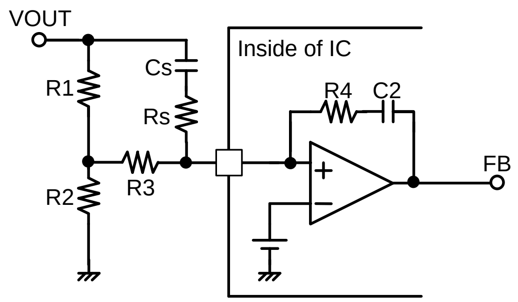



Fig.34 Example of phase compensation setting

DC/DC converter DC Gain

$$\text{DC Gain} = A\times\frac{1}{B}\times\frac{V_{OUT}}{V_{OUT}-V_{IN}} \quad \cdots\cdots\cdots\cdots\cdots (2)$$

A: ERROR AMP Gain
About 100dB = $10^5$
B: Oscillator amplification = 0.5
$V_{IN}$: Input voltage
$V_{OUT}$: Output voltage

By Equations (1) and (2), the frequency $f_{sw}$ of point 0 dB under limitation of the bandwidth of the DC gain at the primary pole point is as shown below.

$$f_{SW} = fp\times\text{DC Gain} = \frac{1}{2\pi C2\times\left(\frac{(R_1 . R_2)}{(R_1+R_2)}+R_3\right)}\times\frac{1}{B}\times\frac{V_{OUT}}{V_{OUT}-V_{IN}} \quad \cdots\cdots\cdots\cdots\cdots (3)$$

It is recommended that $f_{sw}$ should be approx.10 kHz. When load response is difficult, it may be set at approx. 20 kHz. By this setting, $R_1$ and $R_2$, which determine the voltage value, will be in the order of several hundred kΩ. Therefore, if an appropriate resistance value is not available and routing may cause noise, the use of $R_3$ enables easy setting.

[2] Cs and Rs setting

In the step-up DC/DC converter, the secondary pole point is caused by the coil and capacitor as expressed by the following equation.

$$f_{LC} = \frac{1-D}{2\pi\sqrt{(LC)}} \quad \cdots\cdots\cdots\cdots\cdots\cdots (4)$$

D:  ON Duty = ( $V_{OUT}$ - $V_{IN}$ ) / $V_{OUT}$

This secondary pole causes a phase rotation of 180°.  To secure the stability of the system, put zero points in 2 places to perform compensation.

Zero point by built-in CR  $$f_{Z1} = \frac{1}{2\pi R_4 C_2} = 13\text{kHz} \quad \cdots\cdots\cdots\cdots (5)$$

Zero point by Cs  $$f_{Z1} = \frac{1}{2\pi (R_1 + R_3) C_S} \quad \cdots\cdots\cdots\cdots\cdots\cdots (6)$$

Setting $C_{S2}$ to be half to 2 times a frequency as large as $f_{LC}$ provides an appropriate phase margin.
It is desirable to set Rs at about 1/20 of ($R_1$+$R_3$) to cancel any phase boosting at high frequencies.

Those pole points are summarized in the figure below.  The actual frequency property is different from the ideal calculation because of part constants.  If possible, check the phase margin with a frequency analyzer or network analyzer, etc..  Otherwise, check for the presence or absence of ringing by load response waveform and also check for the presence or absence of oscillation under a load of an adequate margin.

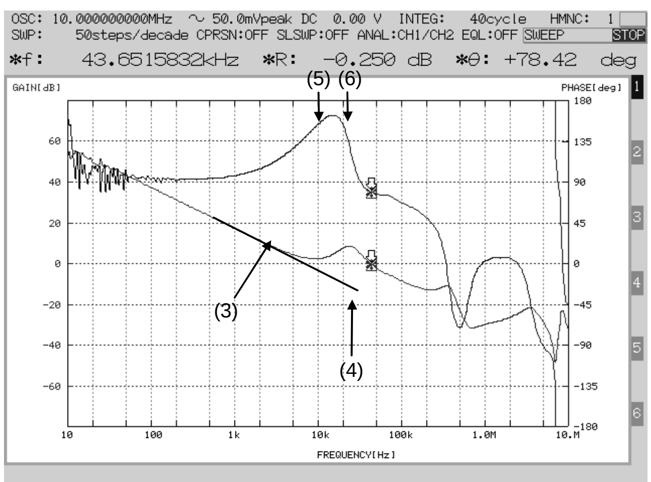
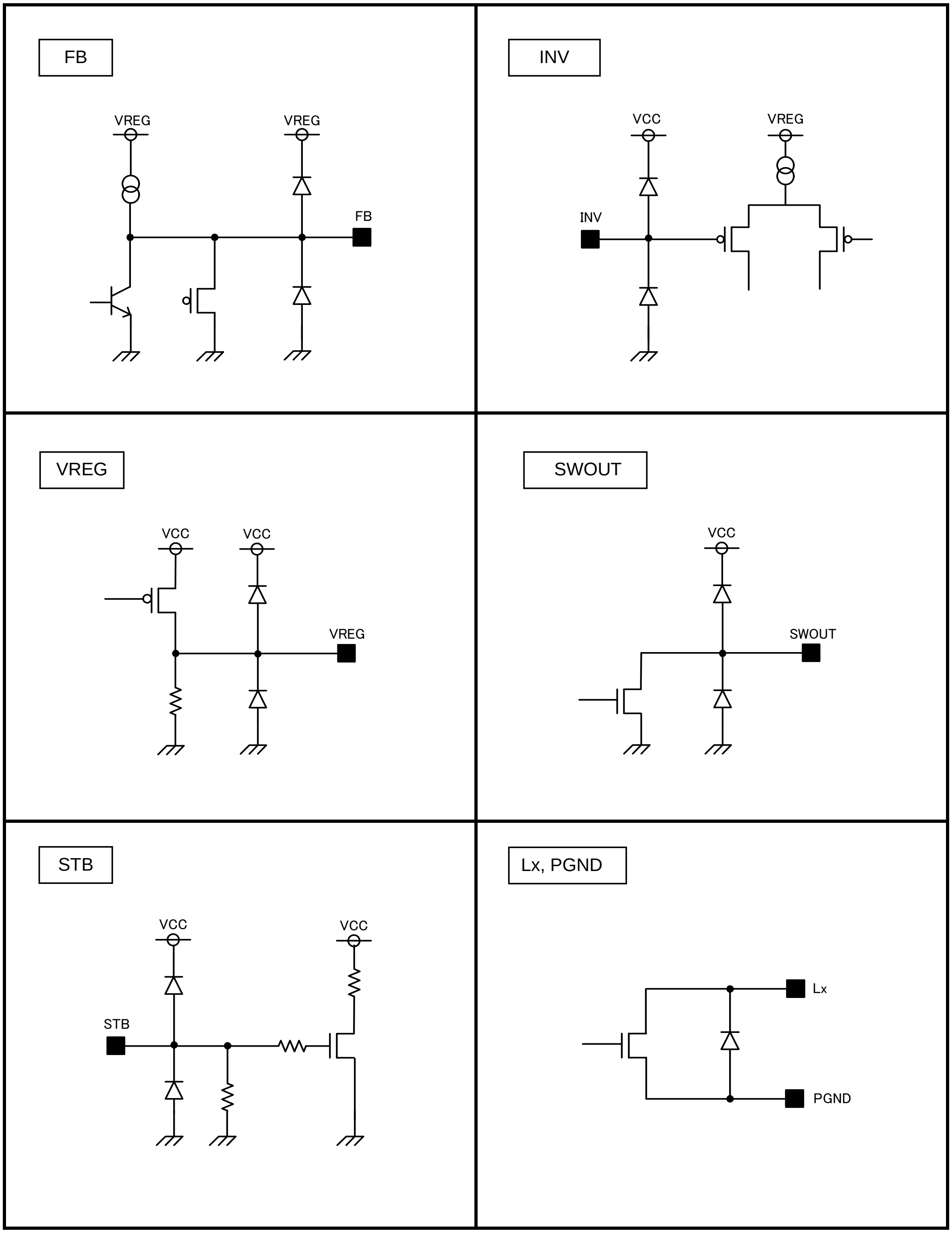



Fig. 35 Example of DC/DC converter frequency property
(Measured with FRA5097 by NF Corporation)

● I/O Equivalence Circuit



● Precautions for Use

1) Absolute Maximum Rating
We dedicate much attention to the quality control of these products, however the possibility of deterioration or destruction exists if the impressed voltage, operating temperature range, etc., exceed the absolute maximum ratings. In addition, it is impossible to predict all destructive situations such as short-circuit modes, open circuit modes, etc. If a special mode exceeding the absolute maximum rating is expected, please review matters and provide physical safety means such as fuses, etc.

2) GND Potential
Keep the potential of the GND pin below the minimum potential at all times.

3) Thermal Design
Work out the thermal design with sufficient margin taking power dissipation (Pd) in the actual operation condition into account.

4) Short Circuit between Pins and Incorrect Mounting
Attention to IC direction or displacement is required when installing the IC on a PCB. If the IC is installed in the wrong way, it may break. Also, the threat of destruction from short-circuits exists if foreign matter invades between outputs or the output and GND of the power supply.

5) Operation under Strong Electromagnetic Field
Be careful of possible malfunctions under strong electromagnetic fields.

6) Common Impedance
When providing a power supply and GND wirings, show sufficient consideration for lowering common impedance and reducing ripple (i.e., using thick short wiring, cutting ripple down by LC, etc.) as much as you can.

7) Thermal Protection Circuit (TSD Circuit)
This IC contains a thermal protection circuit (TSD circuit). The TSD circuit serves to shut off the IC from thermal runaway and does not aim to protect or assure operation of the IC itself. Therefore, do not use the TSD circuit for continuous use or operation after the circuit has tripped.

8) Rush Current at the Time of Power Activation
Be careful of the power supply coupling capacity and the width of the power supply and GND pattern wiring and routing since rush current flows instantaneously at the time of power activation in the case of CMOS IC or ICs with multiple power supplies.

9) IC Terminal Input
This is a monolithic IC and has P+ isolation and a P substrate for element isolation between each element. P-N junctions are formed and various parasitic elements are configured using these P layers and N layers of the individual elements.
For example, if a resistor and transistor are connected to a terminal as shown on Fig.36:

- ○ The P-N junction operates as a parasitic diode when GND > (Terminal A) in the case of a resistor or when GND > (Pin B) in the case of a transistor (NPN)
- ○ Also, a parasitic NPN transistor operates using the N layer of another element adjacent to the previous diode in the case of a transistor (NPN) when GND > (Pin B).

The parasitic element consequently rises under the potential relationship because of the IC's structure. The parasitic element pulls interference that could cause malfunctions or destruction out of the circuit. Therefore, use caution to avoid the operation of parasitic elements caused by applying voltage to an input terminal lower than the GND (P board), etc.

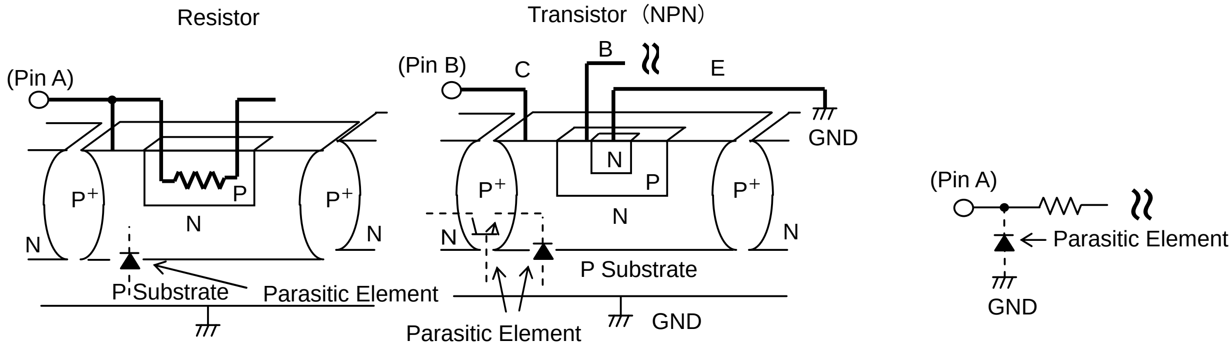



Fig.36 Example of simple structure of Bipolar IC

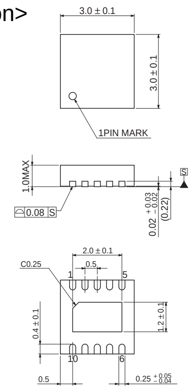
● **Ordering part number**

| B | D | | 8 | 3 | 1 | 1 | | N | U | V | - | E | 2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

- Part No.: BD
- Part No.: 8311
- Package
  NUV: VSON010V3030
- Packaging and forming specification
  E2: Embossed tape and reel

VSON010V3030

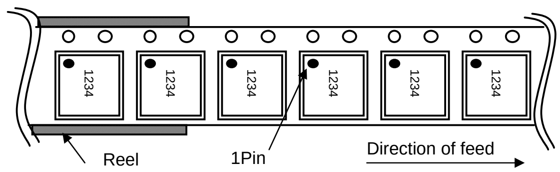
<Dimension>




(Unit:mm

<Tape and Reel information>

| | |
|---|---|
| Tape | Embossed carrier |
| Quantity | 3000pcs |
| Direction of feed | E2<br>(The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand) |




※When you order , please order in times the amount of package quantity.

The content specified in this document is correct as of 1st , 2009, March



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ROHM SEMICONDUCTOR


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