

STRUCTURESilicon Monolithic Integrated CircuitPRODUCT SERIES7-Channel Switching Regulator Controller for Digital Camera

Fig.1

Fig.1

Fig.2

TYPE

PIN ASSIGNMENT BLOCK DIAGRAM PACKAGE Functions BD9353MWV

● Power supply voltage 2.2~5.5V(at start-up), 2.05~5.5V(after start-up)

- CH1step-down converter, CH2cross converter, CH3 step-down converter, CH4 step-up converter CH5 inverting converter for CCD, CH6 boost converter for CCD, CH7 boost converter for LED
  All latural Dawn MOSEFT
- All Internal Power MOSFETs
- Built-In MOSFETs for synchronous rectifying action mode on CH1~4
- Built-In feedback resistors on CH2
- All channels contain internal compensation between inputs outputs of error amps
- Contains sequence control circuit for CH1~4
- Operating frequency 1.5MHz(CH1,3,4), 750KHz(CH2,5,6,7)
- Built-In Short-circuit Protection (SCP)
- CH6 have high side switches with soft start function
- Built-In Over voltage Protection (OVP)
- Thermally enhanced UQFN036V5050 package(5mm × 5mm, 0.4mm pitch)

#### OAbsolute maximum ratings( $Ta=25^{\circ}C$ )

Parameter	Symbol	Limit	Unit
	VCC,Hx13,Hx2, Hx4,Hx567,VO2,HS6L	-0.3~7	v
	STB1234,56	-0.3~7	V
Power Input Voltage	PWM7	-0.3~7	V
	Hx5 – Lx5	-0.3~15	V
	Lx6	-0.3~20	V
	Lx7,VO7	Lx7,VO7 -0.3~21	V
	IomaxLx1	±0.8	A
	IomaxHx2	±1.5	V A A A A
	IomaxHx3	±0.8	A
Output current	IomaxHx4,Lx4	±2.2	A
	IomaxHx5	±1.5	A
	IomaxHS6L	±1.2	A
	IomaxLx6~7	±1.2	Α
Power Dissipation	Pd	0.88 *1	W
Operating Temperature	Topr	-25~+85	°C
Storage Temperature	Tstg	-55~+150	°C
Junction Temperature	Tjmax	+150	°C

\*1 Should be derated by 7.04mW/°C at Ta=25°C or more. When mounted on a glass epoxy PCB of 74.2mm × 74.2 mm × 1.6 mm ORecommended operating conditions

	Cumula al		Limit		L la 34
Parameter	Symbol	MIN	TYP	MAX	Unit
Power Supply Voltage (at start-up)	VCC1	2.2	-	5.5	V
Power Supply Voltage (after start-up)	VCC2	2.05	_	5.5	V
VREF Pin Connecting Catacitor	CVREF	0.047	0.1	0.47	μF
VREGA Pin Connecting Capacitor	CVREGA	0.47	1.0	4.7	μF
PWM7 freqency	fpwm	20	-	100	kHz
[Oscillator]					
Oscillator (CH1,3,4)	fosc	0.8	1.5	1.8	MHz
OSC Timing Resistor	RT	47	62	120	kΩ



#### $OE lectrical characteristics (Ta=25^{\circ}C, VCC=3V, RT=62k\Omega, STB1~6=3V, PWM7=2.5V)$

		Sta	andard Va	lue						Sta	andard Val	lue		0
Parameter	Symbol	MIN	TYP	MAX	Unit	Condition	Param	eter	Symbol	MIN	TYP	MAX	Unit	Condition
[Internal Regulator ]	VREGA						[Soft Start]							
Output Voltage	VREG	2 125	22	2 275	V	Io=5mA	CH1,2,4 Soft S	Start time	Tss1,2,4	1.5	2.5	3.5	msec	RT=62kΩ
The dee Malterer Lander	A				•	10 01101	CH3 Soft Star	t time	Tss3	0.5	1.5	2.5	msec	RT=62kΩ
Under Voltage Locko	but						CH5 Soft Star	t time	Tss5	1.8	2.8	3.8	msec	RT=62kΩ
Threshold	Vuv1	-	1.95	2.05	V		CH6 Soft Star	t time	Tss6	2.5	3.5	4.5	msec	RT=62kΩ
VCC minimum			0.05	0.15										L=6.4 µ H,
after Turn-On	Vuv2	-	2.05	2.15	v		CH7 Soft Star	t time	Тртс	1.3	2.6	5.2	msec	Co=4.7 µ F
VREGA startup														(※3)
voltage	Vuv3	-	-	2.025	V	VCC=2.2V	CH1~4 Delay	time for	Td1	9	15	21	msec	RT=62kΩ
VREGA minimum							CH 56 Delay t	ime for						RT=62k O
operating voltage	Vuv4	-	-	2.15	v	VCC=2.2V	Soft Start		Td56	0.23	0.42	0.61	msec	STB1234=H
after Turn-On							【Output Dri	ver】						
Short Circuit Prot	tection】			i		INIV nin monitor	CH1 Highsi	de SW ON	RON1P	_	300	450	mΩ	Hx1=3.6V
Threshold	Vtcinv	0.42	0.48	0.54	V	CH4	resisitance		DONIN					
Delay time for SCP 1	Tscp	50	70	90	msec	CH1~3,5~7	CHI Lowside 3	SW ON resistance	RONIN	-	230	350	mΩ	Hx1=3.6V
Delay time for SCP 2	Tscp4	7	10	13	msec	CH4	resis	tance	RON21P	-	120	180	mΩ	Hx2=3.6V
[Oscillator]				i			CH2 Lx21	Lowside SW	RON21N	-	120	180	mΩ	Hx2=3.6V,
Frequency CH1,3,4	fosc1	1.3	1.5	1.7	MHz	RT=62kΩ	CH2 Lx22 Hig	sisitance shside SW ON	501005				0	
Rrequency CH2,5,6,7	fosc2	0.65	0.75	0.85	MHz	RT=62kΩ	resis	tance	RON22P	-	150	230	mΩ	VO2=3.4V
Max duty	Dmax1	-	-	100	%	Vscn=0V (※1)	CH2 Lx22 ON re	Lowside SW esistance	RON22N	-	120	180	mΩ	Hx2=3.6V
1,3	d			100	/0	VSCP-0V (X1)	CH3 Highside S	SW ON resistance	RON3P	-	300	450	mΩ	Hx3=3.6V
Max duty 4	Umax I u	86	92	96	%		CH3 Lowside	SW ON resistace	RON3N	-	230	350	mΩ	Hx3=3.6V
Max duty	Dmax2	86	92	96	%		CH4 Highside	SW ON resistace	RON4P	-	150	230	mΩ	Hx4=5V
5,6,7 Max duty	Billaxe		•2	••	,•		CH4 Lowside S	SW ON resistance	RON4N	-	110	170	mΩ	Hx4=5V
CH2 Lx21	Dmax3	-	-	100	%		CH5 PMOS S	SW ON resistace	RON5P	-	600	900	mΩ	Hx56=3.6V
Max duty	Dmax4	86	92	96	%		CH6.7 NMOS S	SW ON resistance	RON6N	-	500	800	mΩ	Hx56=3.6V
[Error AMP]							CH6 Load SW	ON resistance	RON67P	-	200	300	mO	Hx56=3.6V
Instat Bing Comment			0	50		INI) (1.2 6 = 2.0) (	[STR1=:6]	onrooiotado		l	200			
Input Blas Current		-	U	50	nA	11101,3~0-3.00	[31B1~0]	1						
INV Threshold	VINV	0.79	0.80	0.81	V	CH1,3~6	STB	Active	VSTBH1	1.5	-	5.5	V	
INV7 Threshold 1	VINV7	598	630	662	mV	PWM7 Duty=100%	Voltage	Non Active	VSTBL1	-0.3	-	0.3	V	
INIV/7 Thursday 14 0	VINV7	440	472	407		PWM7	Pull Down Re	sistance	RSTB1	250	400	700	kΩ	STB1234,
INV/ Threshold 2	2	449	4/3	497	mv	Duty=75%	[[]]							STB56
INV7 Threshold 3	VINV7	234	252	270	mV	PWM7 Duty=40%				0.05		4.00		
INIV7 Threadedd 4	VINV7	17	22	47	m\/	PWM7	Control		VPWMH	2.05	-	4.00	v	
INV / Threshold 4	4	17	52	47	IIIV	Duty=5%	Voltage	L Level	VPWML	0	-	0.40	V	
【CH2 Feedback】							Pull Down Re	sistance	RPWM	250	400	700	kΩ	
CH2 Output Voltage	VO2	3.332	3.4	3.46 8	V		CH7 Delay tin	ne for shutdown	Toff7	200	300	-	μ sec	RT=62kΩ
VO2S Input Current	IVO2S	4.7	6.7	8.7	uA	VO2S= 3.4V	[LEDSW]							
[Reference Voltage Vref for CH5]				LED PIN SW ON resistance RLED - 2 3 $\Omega$ VCC=3.6						VCC=3.6V				
CH5 Output Voltage	VOUT	-6.09	-6.00	-5.91	V	INV5 1M//200k $\Omega_{\rm c}$	(OVP)							
	5	0.00	0.00	0.01	•	1MΩ( <b>※</b> 2)	OVP Thresh	nold	VOVP7	18	19	20	V	V07 monitor
Line Regulation	DVLi	-	4.0	12.5	mV	VCC= 2.2~5V	[Circuit Cu	rrent]						
When shorted	Ios	0.2	1.0	-	mA	VREF5=0V	-	VCC terminal	ISTB1	-	-	5	μA	
							Stand-by	Hx terminal	ISTB2	-	-	5	μA	
							Current	Lx terminal	ISTB3	-	-	5	μA	
							Cinemit Com	L				-	<i></i>	INV1-7=1.2V
							VCC PIN Curren	rent)	Icc	-	5.0	11.0	mA	INV5=-0.2V
														VUU- 3.0V

 $(\divideontimes1)$   $\,$  When circuit is operated by 100% duty at CH1 and CH3, SCP timer start.

So it is possible to use only for transition time shorter than Tscp.

- $(\divideontimes3)$   $\hfill Related to LED quantity , LED forward voltage and Input voltage.$

◎ This product is not designed for normal operation with in a radioactive environment..



### OPIN Assignment Block Diagram



OPackage



# **OPIN** Description

端 子 名	機能
VCC	IC Power Supply Input
GND	Ground
PGND13,2,4,567	Ground for Internal FET
VREGA	VREGA Output
VREF5	CH5 Reference Output
Hx13,2,567	CH1~3,5,6 Pch FET Source Terminal , FET Driver Power Supply
Hx4	CH4 DC/DC Output
Lx1,3,4,5,6,7	Terminal for Connecting Inductor
Lx21	Terminal for Connecting Inductor For CH2 Input
Lx22	Terminal for Connecting Inductor For CH2 Output
VO2	CH2 DC/DC Output
HS6L	Output Terminal for Internal Load Switch
INV1,3,4,5,6,7	Error Amp Inverted Input
VO2S	CH2 Output Feedback Terminal
RT	Terminal for Connecting a Resister To Set the OSC Frequency
SCP	SCP Timer Flag Terminal
STB1234,56	CH1~CH6 ON/OFF Control Terminal
PWM7	CH7 ON/OFF Control, PWM Dimming Input
LED	Terminal for connecting LED Cathode
V07	CH7 DC/DC Output



# **OOperation Notes**

1.) Absolute maximum ratings

This product is produced with strict quality control. However, the IC may be destroyed if operated beyond its absolute maximum ratings. If the device is destroyed by exceeding the recommended maximum ratings, the failure mode will be difficult to determine. (E.g. short mode, open mode) Therefore, physical protection counter-measures (like fuse) should be implemented when operating conditions beyond the absolute maximum ratings anticipated.

2.) GND potential

Make sure GND is connected at lowest potential. All pins except NON5, must not have voltage below GND. Also, NON5 pin must not have voltage below - 0.3V on start up.

3.) Setting of heat

Make sure that power dissipation does not exceed maximum ratings.

4.) Pin short and mistake fitting

Avoid placing the IC near hot part of the PCB. This may cause damage to IC. Also make sure that the output-to-output and output to GND condition will not happen because this may damage the IC.

5.) Actions in strong magnetic field

Exposing the IC within a strong magnetic field area may cause malfunction.

6.) Mutual impedance

Use short and wide wiring tracks for the main supply and ground to keep the mutual impedance as small as possible. Use inductor and capacitor network to keep the ripple voltage minimum.

7.) Thermal shutdown circuit (TSD circuit)

The IC incorporates a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

- continue to use the rC after operating this circuit of use the rC in an environment where the operation
- 8.) Rush current at the time of power supply injection.

An IC which has plural power supplies, or CMOS IC could have momentary rush current at the time of power supply injection. Please take care about power supply coupling capacity and width of power Supply and GND pattern wiring.

9.) IC Terminal Input

This IC is a monolithic IC that has a P- board and P+ isolation for the purpose of keeping distance between elements. A P-N junction is formed between the P-layer and the N-layer of each element, and various types of parasitic elements are then formed. For example, an application where a resistor and a transistor are connected to a terminal (shown in Fig.15):

OWhen GND > (terminal A) at the resistor and GND > (terminal B) at the transistor (NPN), the P-N junction operates as a parasitic diode.

OWhen GND > (terminal B) at the transistor (NPN), a parasitic NPN transistor operates as a result of the NHayers of other elements in the proximity of the aforementioned parasitic diode.

Parasitic elements are structurally inevitable in the IC due to electric potential relationships. The operation of parasitic elements Induces the interference of circuit operations, causing malfunctions and possibly the destruction of the IC. Please be careful not to use the IC in a way that would cause parasitic elements to operate. For example, by applying a voltage that is lower than the GND (P-board) to the input terminal.



Fig - 3 Simplified structure of a Bipolar IC

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