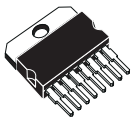
L9468

ALL SILICON VOLTAGE REGULATOR

1 Features

- FULLY MONOLITHIC DESIGN
- HIGH SIDE FIELD DRIVE
- THERMAL PROTECTION
- FIELD DRIVER SHORT CIRCUIT PROTECTION
- PROTECTED DIAGNOSTIC LAMP DRIVER
- REDUCED OUTPUT MODE
- COMPLEX DIAGNOSTICS
- LOAD RESPONSE CONTROL

Figure 1. Package



Multiwatt8

Table 1. Order Codes

Part Number	Package
L9468N	Multiwatt8

2 Description

The L9468 is a monolithic multifunction generator Voltage regulator intended for use in automotive applications.

This device regulates the output of an automotive generator by controlling the field winding current by means of a variable frequency PWM high side driver.

Figure 2. Block Diagram

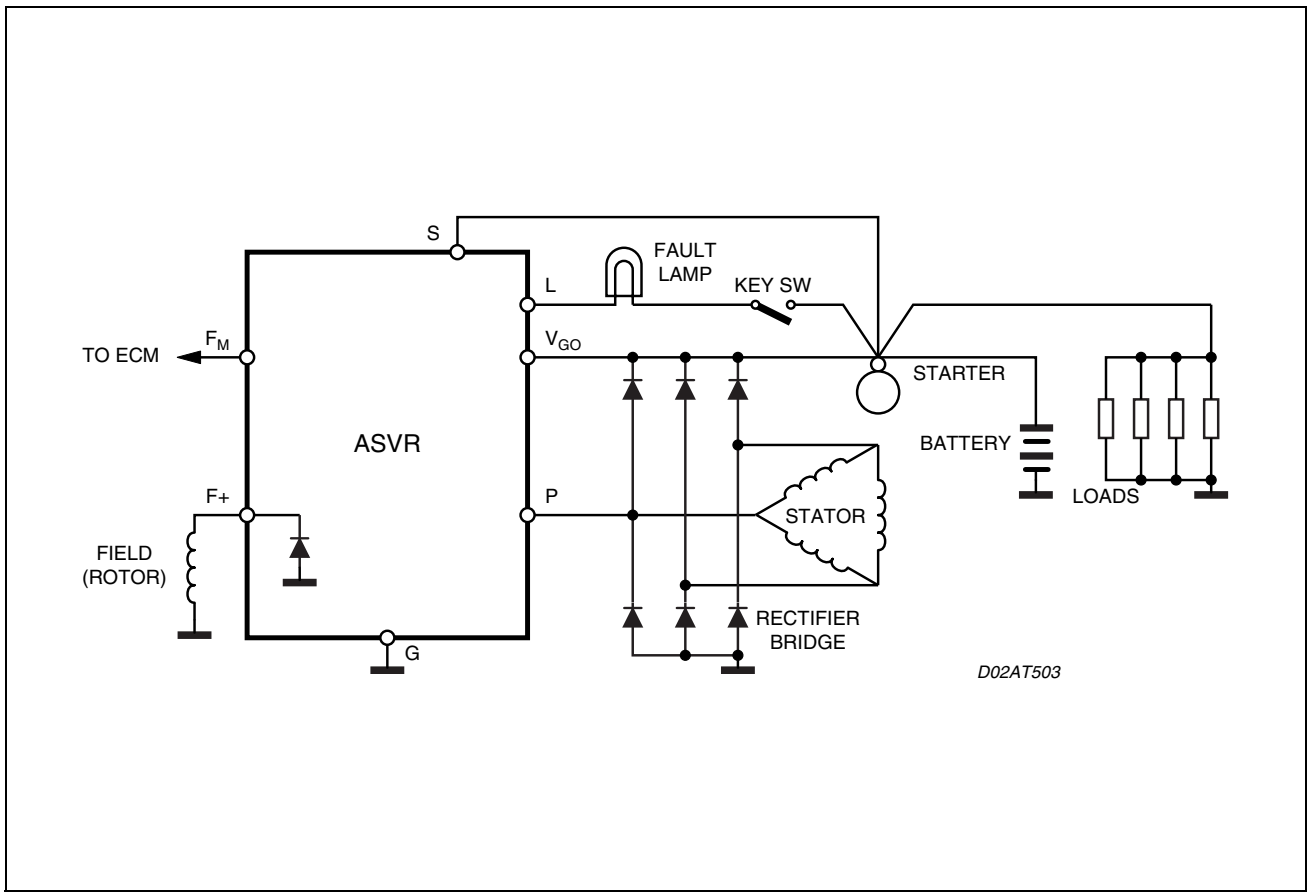


Table 2. Pin Description

N°	Pin	Function
1	V_{GO}	Generator output sense and voltage supply to L9468
2	F+	Field high side driver output
3	G	Ground for L9468
4	S	Battery sense input
5	GND	Connected to the Tab through the frame
6	F_M	Field monitor output
7	L	Lamp terminal low side driver
8	P	Phase sense input

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_S	Thermal Supply Voltage (load dump)	40	V
I_O	Output Current Capability	internally limited	A
P_{tot}	Total Power Dissipation (@T_{case} = 150°C, I_{FIELD} = 5A)	6	W
V_R	Reverse Voltage (see figure 1)	-2.5/-6	V

Figure 3. Pin Connection (Top view)

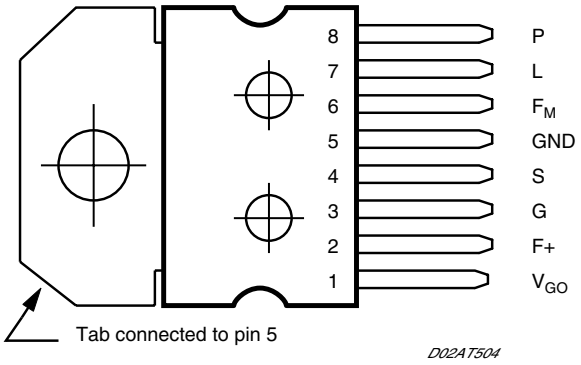


Table 4. Thermal Data

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance junction-case	-45 to 160	°C
T_{stg}	Storage Temperature	-50 to 175	°C
$R_{th\ sd}$	Thermal Shut-Down	175 ±15	°C
$R_{th\ j\text{-}case}$	Thermal Resistance junction -case	1.5	°C/W

Table 5. Electrical Characteristcs

(T_{case} = -35°C to 150°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{OS}	Operating Supply Voltage	T_{case} = +25 to +150 °C	8		20 [1]	V
V_{OS}	Operating Supply Voltage	T_{case} = - 40 to +25 °C	10		20	V
I_{SB}	Stand-by Current	V_{GO} = 12.6V, T_{case} -35 to +80 °C			400	µA
I_{SB}	Stand-by Current	V_{GO} = 12.6 V, 80°C <T_{case}< +150°C			1	mA
V_S	Regulator Set-Point	@ 71°C ± 3°C		14.1		V
V_{NB}	Generator output, no battery	No battery, I_{OUT} =2A to 50% Max Load	V_S-2		V_S+2	V
T_C	Thermal compensation	Voltage @ V_S or V_{GO} [2] in failsoft				V
V_{LR}	Load Regulation	6500 grpm, 10% to 95% load			300	mV
V_{SR}	Speed Regulation	15A load, 2,000 to 10,000 grpm			100	mV
V_{FON}	Output Saturation Voltage	I_F = 6A, V_{GO} = 14.7V, T_{case} = 25°C			750	mV
V_{FON}	Output Saturation Voltage	I_F = 5A, V_{GO} = 13.5V, T_{case} = 125°C			850	mV
I_{FLIM}	Field limit current	F terminal shorted to GND @ 25°C	8.3			A
		F terminal shorted to GND @ 150°C	5			A
V_F	Field Discharge Rectifier	I_F = 6A, T_{case} = 25°C			1.85	V
I_R	Diode Reverse Current	V_R = 20V			1	mA
f_{OSC}	Oscillation frequency	During LRC operation	340	400	460	Hz
MFDC	Minimum Field Duty-Cycle	V_{UV} < V(S or V_{GO}) < V_{OV} [3]		6.25		%
R_{FM}	Impedance @ F_M pin	Impedance between F_M and F+	5		15	KΩ

Notes:

1. 20 Volts is the maximum operating voltage because above this level the FAILSAFE feature shuts down the output stage.
2. Thermal slopes are shown in fig. 2
3. This value is present when the voltage sensed at the " S" or "VGO" terminal is between VUV and VOV. When the voltage sensed at the "S" or "VGO" terminal is above VOV the Minimum Field Duty-Cycle will be 0 %.

Figure 4. Reverse B+ Test Circuit

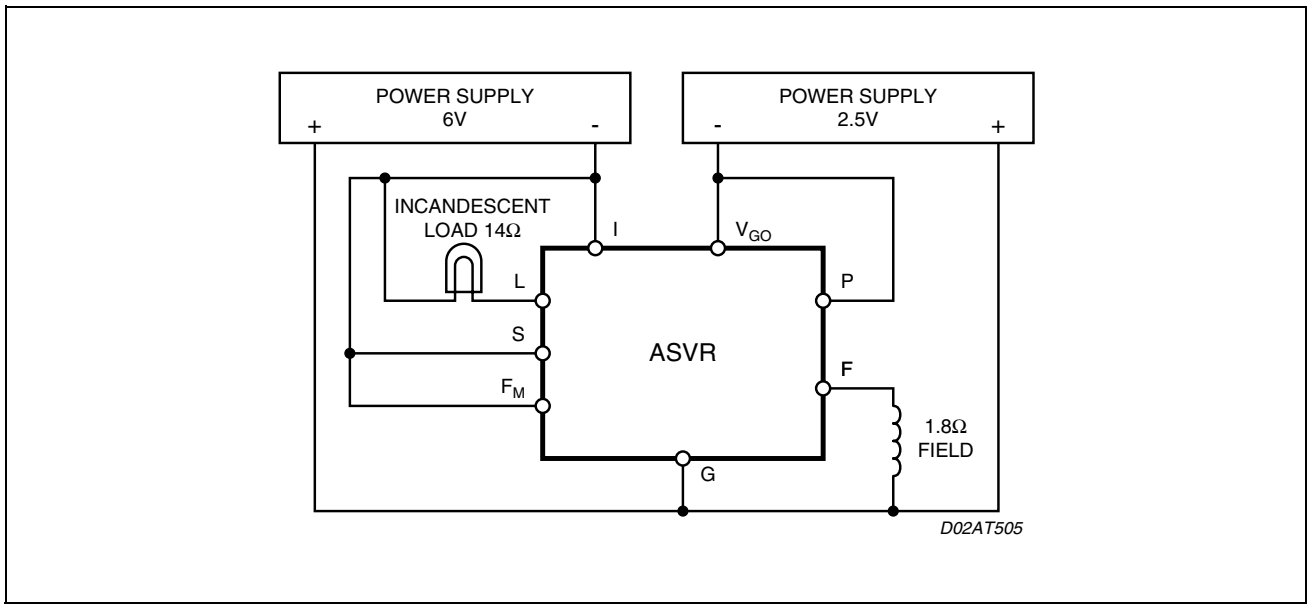


Figure 5. Setpoint Voltage vs. T_{case} Temperature

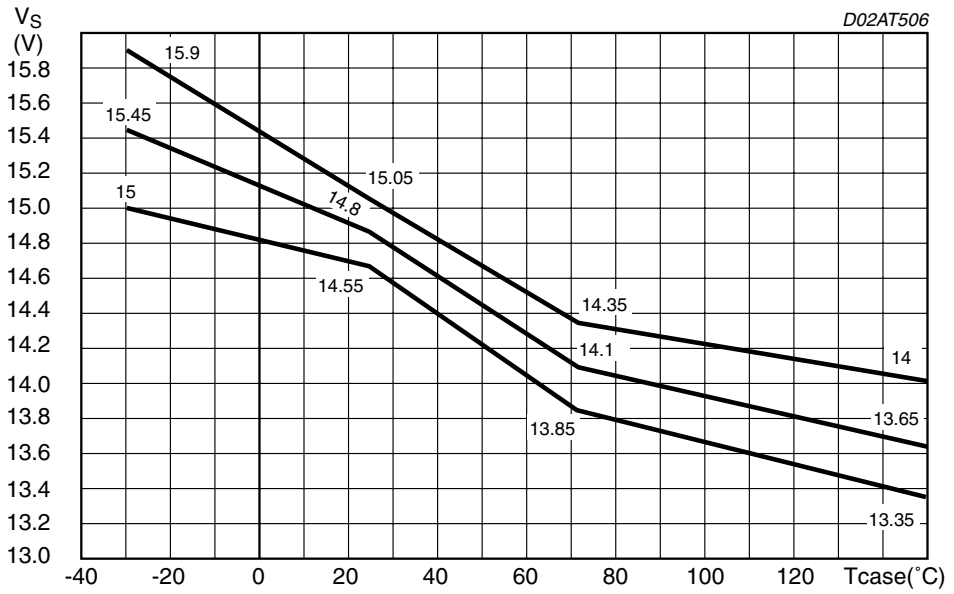


Table 6. Diagnostic (T_{case} -35°C to +150°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{FSO}	Failsafe Output Voltage	Voltage measured at V_{GO}	20	20.48	21	V
V_{FSL}	Switch sensing from S to V_{GO}	"S" Voltage falling into Fail Soft [4]	4	4.2		V
V_{FSH}	Switch sensing from V_{GO} to S	"S" Voltage rising out of Fail Soft		7.6	8	V
I_S	Sink current @ "S" pin	V_S = 14 V	1	1.75	2.5	mA
V_{UV}	Undervoltage	grpm > 3100 ± 15%	10.95	11.35	11.6	V
V_{OV}	Overvoltage		V_S+1	V_S+1.25	V_S+1.55	V
V_{LSAT}	Lamp saturation voltage	I_L = 0.5A		1.33	1.4	V
V_{LSAT}	Lamp on Voltage [5]	I_L < 0.5A,VGO=open, T_{case} = 25°C		3.8	5	V
T_{DELAY}	Fault Indication Delay Time		0.935	1.1	1.265	s

Notes:

4. When Fail Soft operation is detected, regulation sensing will switch from the "S" terminal to the VGO terminal.
5. This condition can happen when the connection between the battery and VGO or the output terminal of the generator is broken. In this case the delay of 1.1 seconds is not required.

3 FAULT

The following table lists the conditions that cause the fault lamp driver to function. To prevent lamp flicker, specific faults are required to be present for TDELAY seconds before the lamp driver is activated. This delay is indicated in the table.

Table 7.

Conditions	Delay
1. Key-on (wiring check), lamp stays on for 1 ± 0.15 sec regardless other conditions	No
2. V_{GO} / S> V_{OV}	Yes
3. V_{GO} / S < undervoltage threshold voltage **AND** Phase frequency > f_{LRC}	Yes
4. Phase Voltage < VP2 **AND** VGO / S < setpoint	Yes
5. Phase frequency < f_{IFR}	Yes
6. No connection between Battery and VGO	No
7. FAILSAFE	Yes

Table 8. Regulation Features

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{LON}	Lamp term turn on threshold [6]		0.8	1	1.15	V
I_{LON}	Lamp term current sensitivity	V_L = 1 V to Vsp	0.09		0.78	mA
V_{P1}	Initiation of regulation detection phase voltage threshold [7]	I_P = 1mA (sinking current)	2.5	3	3.5	V
V_{P2}	Fault detection phase voltage threshold [8]		7	8	9	V
I_P	Sinking current @ P terminal	V_P = 1.5V	0.5	1	1.8	mA
f_{IFR}	Initiation of field regulation frequency		53.04	61	70.15	Hz
FSDF	Field Strobe Duty Factor	@ "power up" with $f_{PHASE} < f_{IFR}$		31.25		%
LRC	Load Response Control rate [9]		2.125	2.5	2.875	s
f_{LRC}	LRC transition frequency	LRC is enabled below this value	263.5	310	356.5	Hz
V_{LCB}	"L" term. Cut-Back Setpoint	"L" = 0V, "I" = 0V [10]	V_S-20%	V_S-25%	V_S-30%	V

Notes:

6. Lamp and Ignition are cooperative. Either can turn on the device when the other is left open or held low. When both go below their minimum thresholds the L9468 goes into "L" Terminal Control (LTC). The L9468 will remain in LTC until the phase (P) voltage drops below VP2 and the frequency drops below fIRF at the VP1 threshold then the L9468 is disabled.
7. This threshold on the phase signal is used to detect the phase frequency, fIFR, for the Initiation of field regulation.
8. This threshold on the phase signal is used to sense the presence of the phase for fault detection purposes.
9. This is the time duration the L9468 takes to rump up from 0 % to 100% duty cycle in response to an increased load on the enerator. The LRC ratio is set 1:4 and the Vreg comparator status is latched at foundamental frequency rate.
10. Cut-back occurs when both the "L" and "I" terminals are LOW . If the "I" terminal is disconnected it will assume a logic LOW allowing the "L" terminal to perform the function alone. In cut-back, to prevent the loss of phase signal, a 31.25% duty cycle is applied to field output when phase drops below Vp2

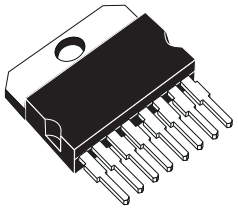
4 Package Information

Figure 6. Multiwatt 8 Mechanical Data & Package Dimensions

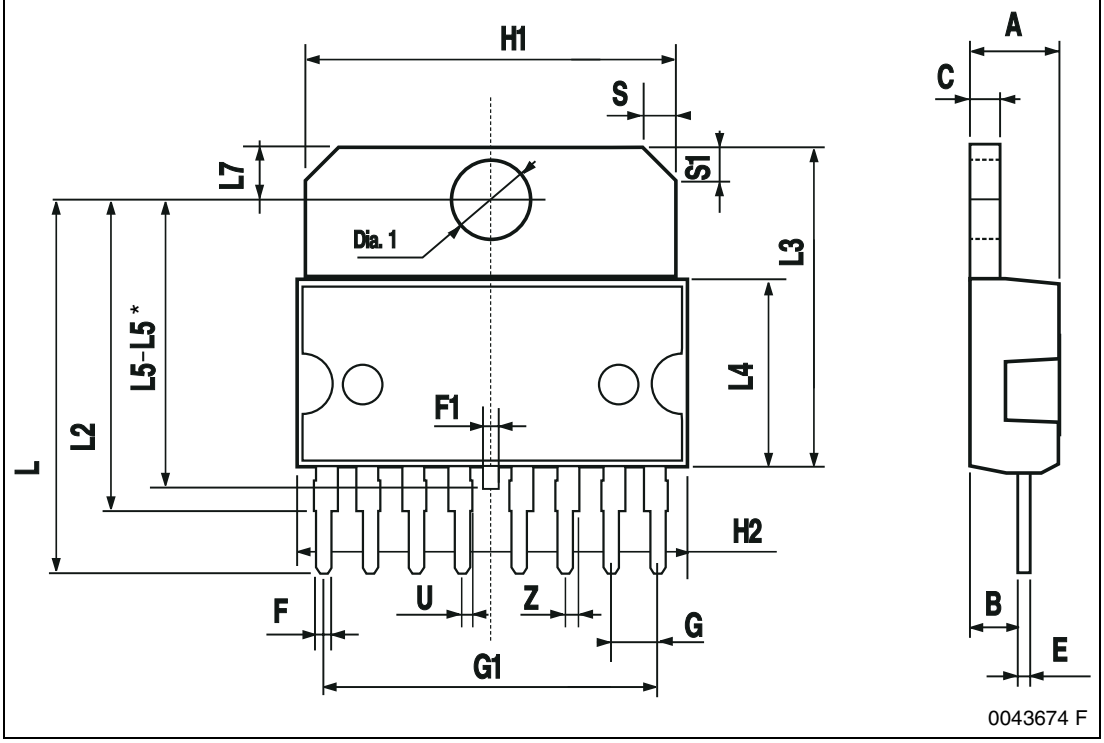
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5			0.197
B			2.65			0.104
C			1.6			0.063
E	0.49		0.55	0.019		0.022
F	0.78		0.85	0.030		0.033
F1	0.68		0.75	0.027		0.029
G	2.40	2.54	2.68	0.094	0.10	0.105
G1	17.64	17.78	17.92	0.69	0.70	0.71
H1	19.6			0.772		
H2			20.2			0.795
L	20.35		20.65	0.80		0.81
L2	17.05	17.20	17.35	0.67	0.68	0.68
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L5	15.45		15.75	0.61		0.62
L5*	15.05		15.35	0.59		0.60
L7	2.65		2.9	0.104		0.114
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
U	0.40		0.55	0.015		0.022
Z	0.70		0.85	0.028		0.034
Dia1	3.65		3.85	0.144		0.152

L5 = with wedged frame std.
L5* = with wedged frame anchor holes.

OUTLINE AND MECHANICAL DATA



Multiwatt8 (Floating)



5 Revision History

Table 9. Revision History

Date	Revision	Description of Changes
April 2005	1	First Issue