SGS-THOMSON MICROELECTRONICS

L4956

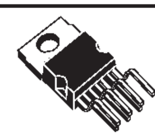
5A LOW DROP LINEAR REGULATOR

- SPLITTED SUPPLY VOLTAGE FOR IMPROVED EFFICIENCY:
  - V_{PW}: 3V MIN. POWER SUPPLY VOLTAGE
  - V_{SIG}: 4.5V MIN. SIGNAL SUPPLY VOLTAGE
- 5A OUTPUT CURRENT
- FAST LOAD TRANSIENT RESPONSE
- 0.75V TYP. DROP OUT VOLTAGE AT 5A
- INHIBIT WITH ZERO CURRENT COMSUMPTION
- POWER GOOD
- SHORT CIRCUIT PROTECTION
- THERMAL SHUTDOWN
- HEPTAWATT PACKAGE

APPLICATIONS

- PENTIUM™ AND POWER PC™ SUPPLIES
- LOW COST SOLUTION FOR 3.3V TO 1.5V CONVERSION
- SUITABLE FOR APPLICATIONS WITH STAND BY FEATURE

MULTIPOWER BCD TECHNOLOGY



HEPTAWATT

ORDERING NUMBER: L4956

DESCRIPTION

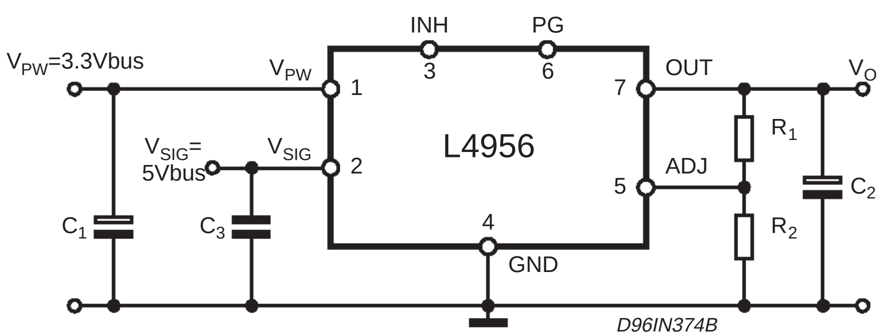
The L4956 is an adjustable monolithic linear regulator designed to satisfy very heavy load transient and efficient power conversion from 3.3V to 1.26V and lower, up to 5A.

Designed in BCDII technology, it uses a charge pump technique to have a proper internal N-channel gate drive. The signal supply voltage input V_{SIG} can operate from 4.5V up to an absolute of 7V and the power supply voltage input V_{PW} can opearte from 3V min to an absolute of 7V. An RDSON of 150mV gives a voltage drop of 750mV at 5A of load current.

Very fast load transients and ±1% of reference voltage precision makes this device suitable for supplying last micrprocessors generation and low voltage logics.

The Heptawatt package enriches the device with auxiliary functions like power good and inhibit.

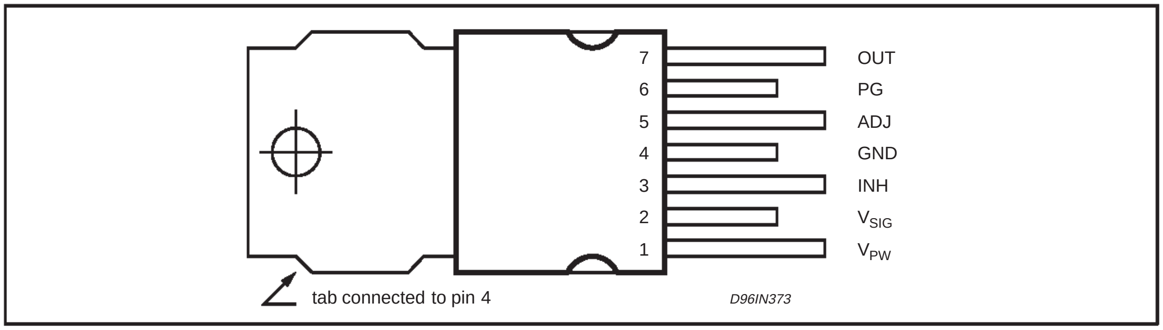
TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{PW}, V_{SIG}	Supply Input Voltage	7	V
	ADJ pin PG and INH pins	-0.3 to 4 0 to V_{SIG}	V V
P_{TOT}	Power Dissipation @ T_{amb} = 50°C Power Dissipation @ T_{case} = 90°C	2 15	W W
T_{st}, T_i	Storage Temperature	-40 to +150	°C

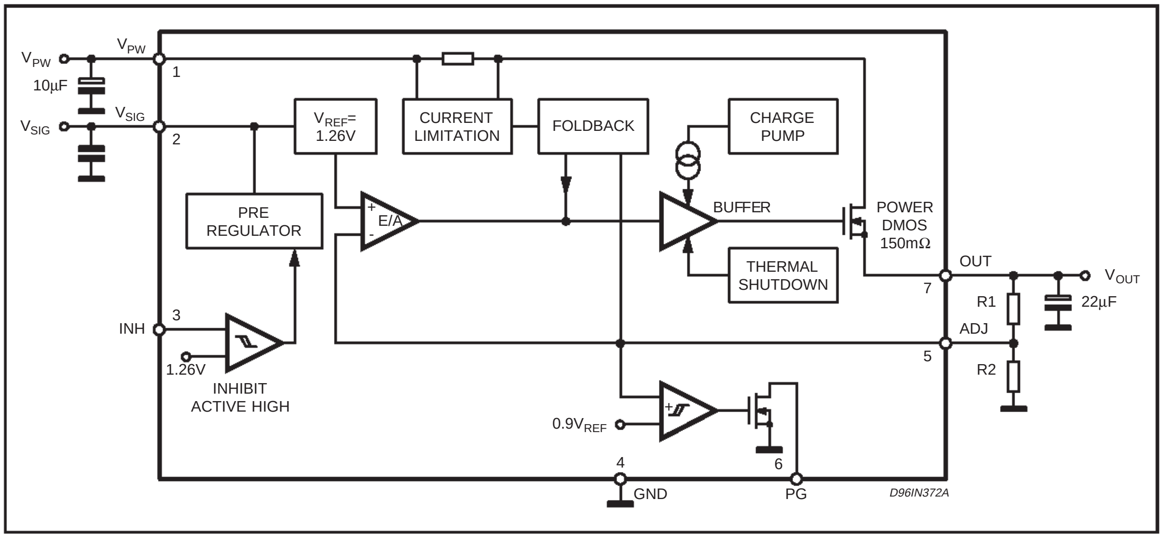
PIN CONNECTION (Top view)



PIN FUNCTIONS

No.	Name	Function
1	V_{PW}	Unregulated power input voltage; this pin must be bypassed with a capacitor larger than 10µF.
2	V_{SIG}	Unregulated signal input voltage this pin has to be by passed with a minimum capacitor of 0.1µF.
3	INH	TTL-CMOS input. A logic level on this input disable the device. An internal pull-down insures insures full functionally even if the pin is open.
4	GND	Ground.
5	ADJ	The output is connected directly to this terminal for 1.26V operation via divider for higher voltages.
6	PG	Open drain output, this pin is low when the output voltage is lower than 90%, otherwise is high.
7	OUT	Regulated output voltage. A minimum bypass capacitor of 22µF is required to insure stability.

BLOCK DIAGRAM



THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-case		2.5	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient		50	°C/W
	Thermal Shutdown	Typ.	150	°C
	Thermal Hysteresis	Typ.	20	°C

ELECTRICAL CHARACTERISTICS (T_j = 25°C, unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{PW}	Power Operating Supply Voltage		3		6.5	V
V_{SIG}	Signal Operating Supply Voltage		4.5		6.5	V
V_{OUT}	Output Voltage (1)	$0 < T_j < 125°C$; $V_{PW} = 3.3V$ $4.5V < V_{SIG} < 6.5V$; $0.1A < I_O < 5A$	1.240	1.260	1.280	V
		$3V < V_{PW} < 5.5V$; $4.5V < V_{SIG} < 6.5V$ $0.1A < I_O < 5A$; $0 < T_j < 125°C$	1.224	1.260	1.296	V
ΔV_{OUT}	Line regulation (1)	$3V < V_{PW} < 5.5V$; $I_O = 10mA$ $4.5V < V_{SIG} < 6.5V$		0.5	3	mV
ΔV_{OUT}	Load regulation (1)	VPW = 3.3V; $V_{SIG} = 5V$ $0.1A < I_O < 5A$		1	5	mV
	Drop-out Voltage	$I_O = 5A$ $I_O = 5A$, $T_j = 125°C$		0.75 1.1	1.1 1.5	V V
I_O	Current Limiting	$0 < T_j < 125°C$	5.1	6.3	7.5	A
	Short Circuit Current	$V_O = 0V$, $0 < T_j < 125°C$		1.8		A
I_Q	Quiescent Current at pin V_{SIG}	$0.1A < I_O < 5A$ $4.5V < V_{SIG} < 6.5V$		1.5	3	mA
	Stand By Current at pin V_{SIG}	INH = HIGH $V_{SIG} = 5V$		100	150	µA
	Inhibit Threshold	$0 < T_j < 125°C$	1.1	1.26	1.42	V
	Inhibit Histeresys			0.2		V
	Inhibit Bias Sink Current			5	10	µA
	Power Good Threshold			0.9 x V_{OUT}		V
	Power Good Saturation	$I_6 = 4mA$		0.1	0.4	V
	Power Good Histeresys			0.2		V

(1) Output voltage connected to ADJ.

Figure 1. DC Operating Area.

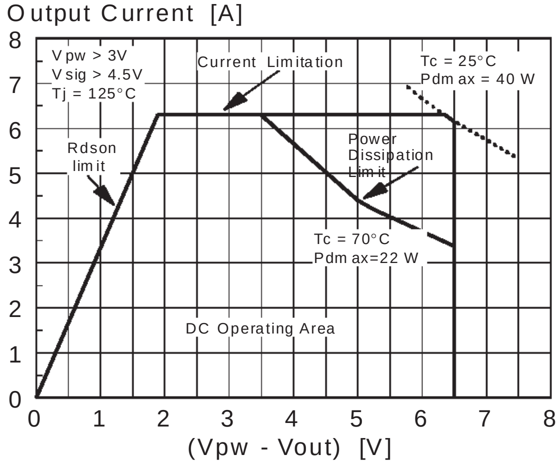


Figure 2. Output Voltage Stability vs. Junction Temperature

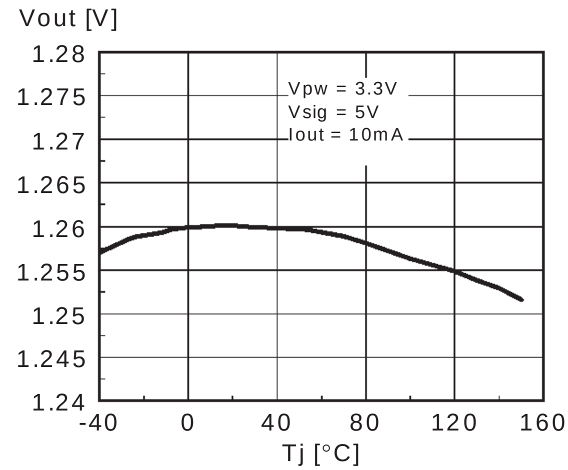


Figure 3. Load Regulation.

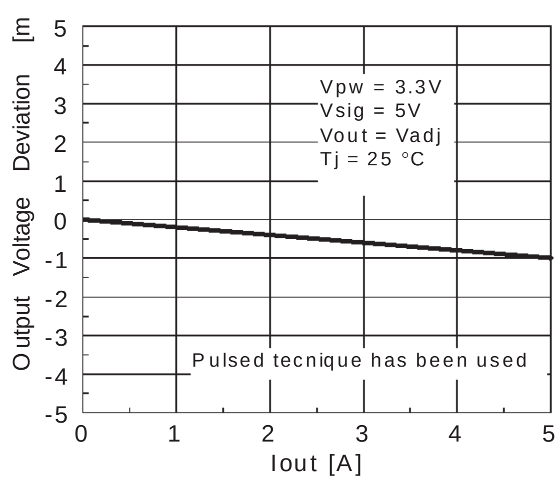


Figure 4. Dropout Voltage.

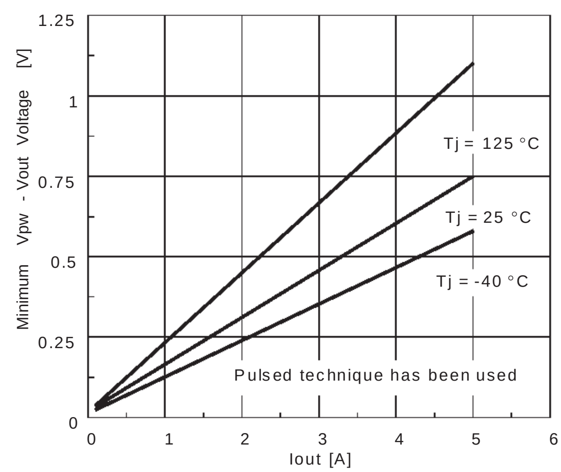


Figure 5. Maximum Output Current vs. Junction Temperature

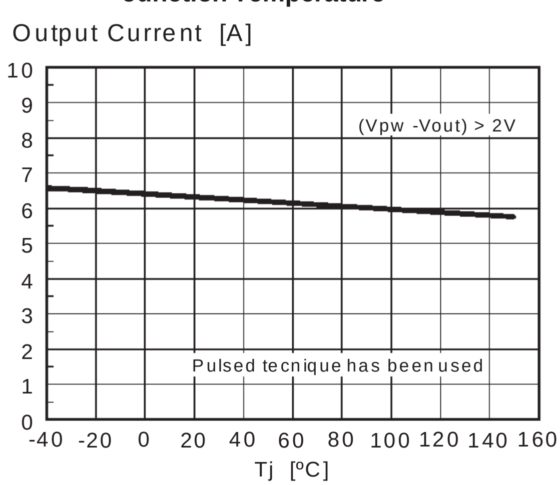


Figure 6. Quiescent Current at pin VSIG vs. Junction Temperature.

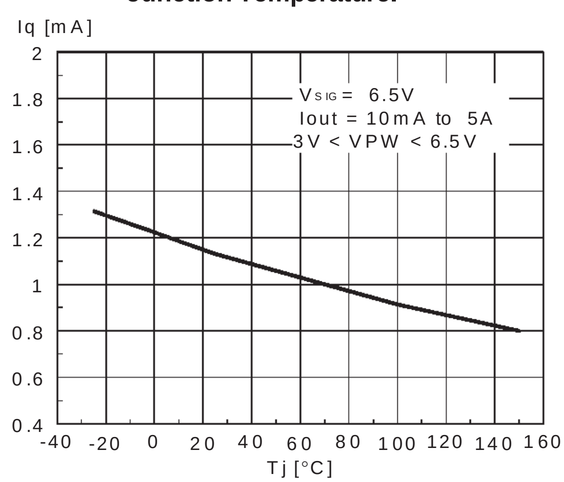


Figure 7. Quiescent Current at pin VSIG vs. Signal Input Voltage.

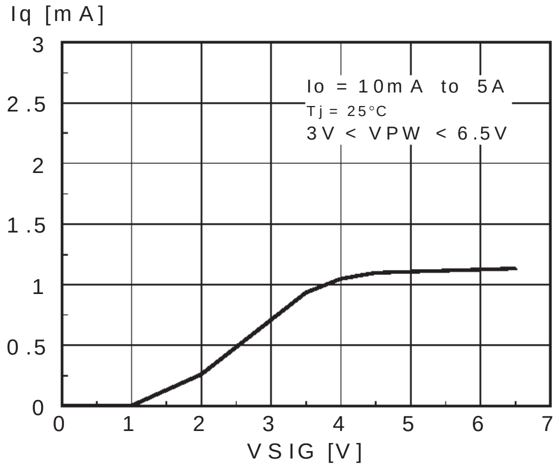


Figure 8. Stand-By Current at pin VSIG vs. Signal Input Voltage with INH = LOGIC HIGH

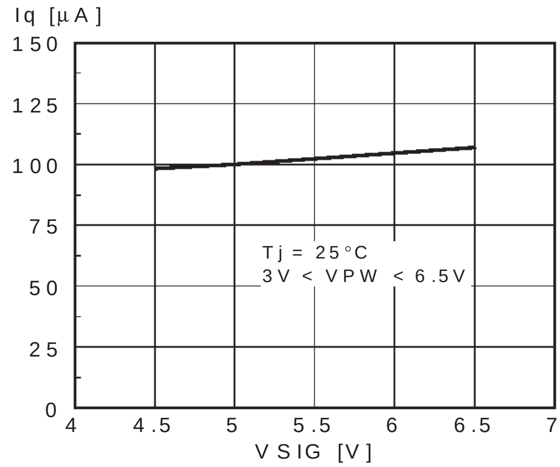


Figure 9. Power Good Function

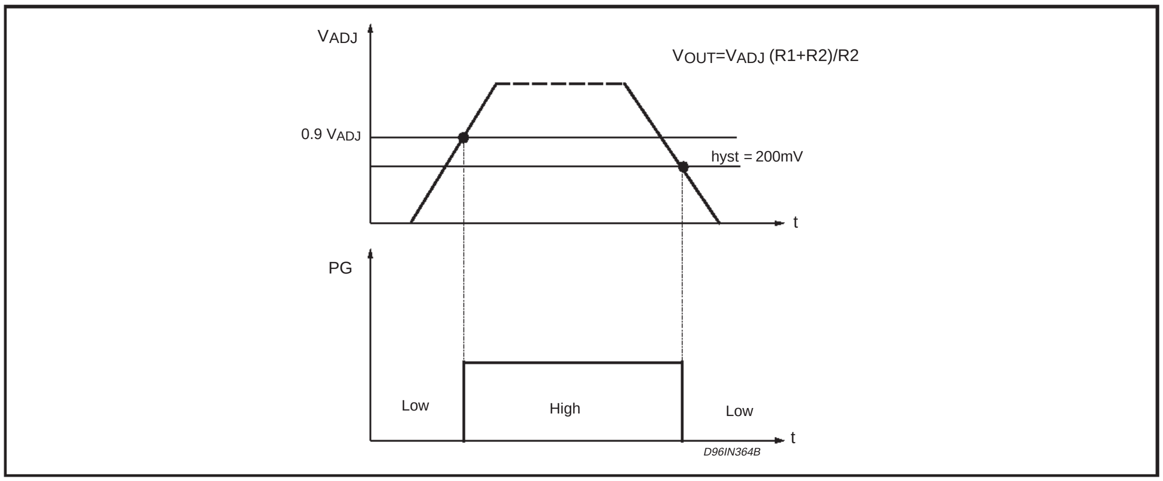
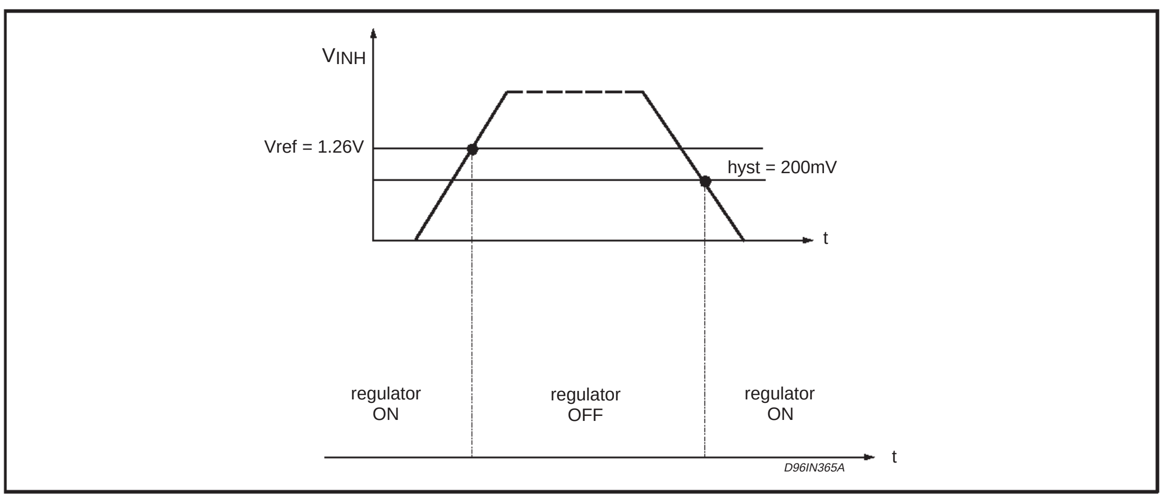


Figure 10. Inhibit Function



LOAD TRANSIENT RESPONSE

Figure 11.

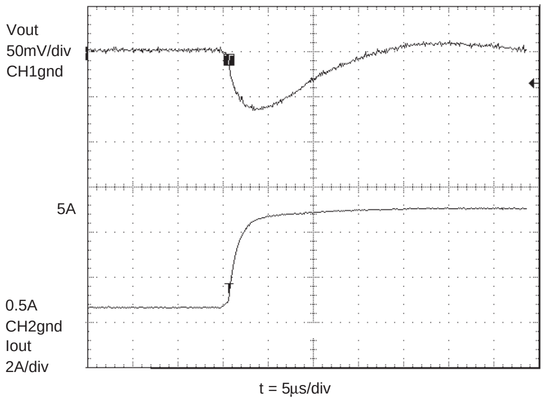


Figure 12.

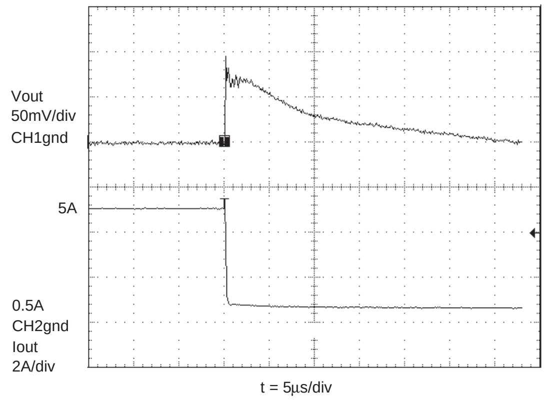
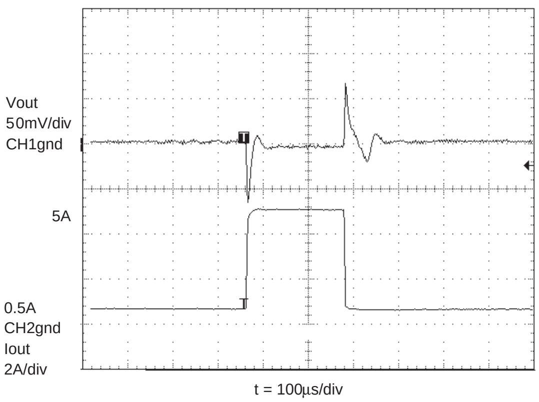


Figure 13.

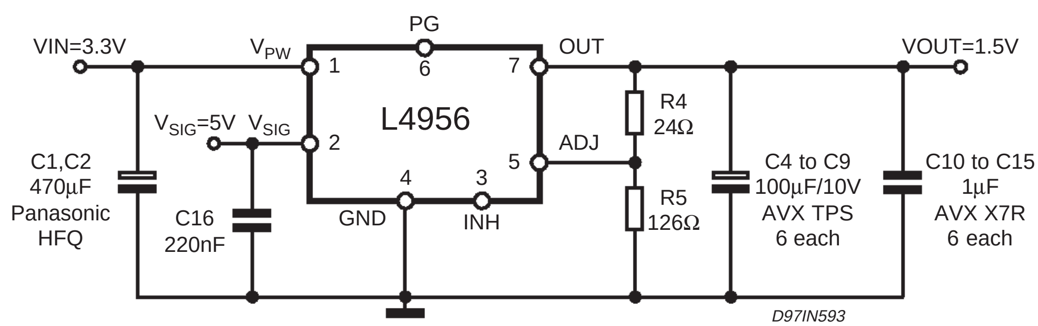


Test conditions:

V_{PW} = 3.3V; V_{SIG} = 5; V_{out} = 1.5V; Load Transient from 0.5A to 5A;

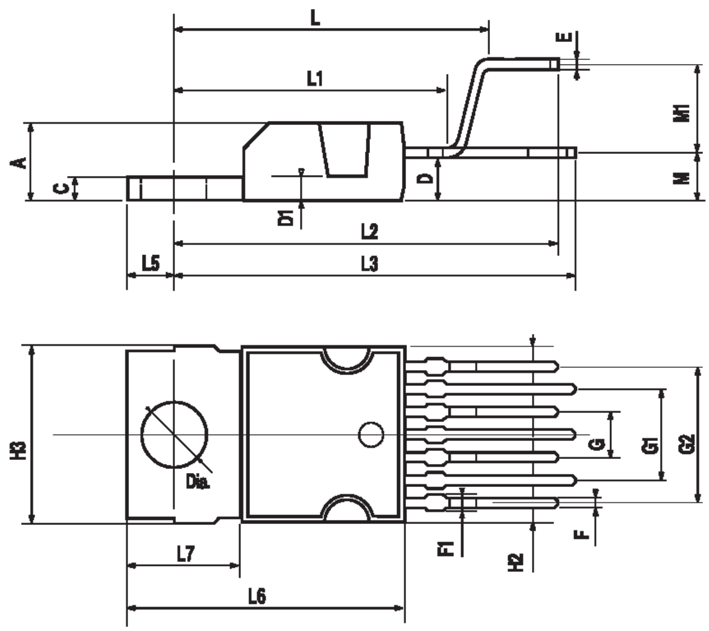
$\frac{dI_{out}}{dt}$ = 20A/µs; Tj = 25°C

Figure 14. Load transient test circuit.



HEPTAWATT PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.6		0.8	0.024		0.031
F1			0.9			0.035
G	2.41	2.54	2.67	0.095	0.100	0.105
G1	4.91	5.08	5.21	0.193	0.200	0.205
G2	7.49	7.62	7.8	0.295	0.300	0.307
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L		16.97			0.668	
L1		14.92			0.587	
L2		21.54			0.848	
L3		22.62			0.891	
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
M		2.8			0.110	
M1		5.08			0.200	
Dia	3.65		3.85	0.144		0.152



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