STRUCTURE Silicon Monolithic Integrated Circuit
TYPE Power switch for ExpressCard™
PRODUCT SERIES **BD4154FV**
FEATURES
- High Side Switch for ExpressCard™
- Soft Start Circuit
- Meets the ExpressCard™ Standard

○ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Limit	Unit
Input Voltage	V3AUX_IN, V3_IN, V15_IN	-0.3～5.0 *1	V
Logic Input Voltage 1	EN,CPPE#,CPUSB#,SYSR,PERST_IN#,RCLKEN	-0.3～V3AUX_IN+0.3 *1	V
Logic Output Voltage 1	RCLKEN	-0.3～V3AUX_IN+0.3 *1	V
Logic Output Voltage 2	PERST#	-0.3～V3AUX_IN+0.3	V
Output Voltage	V3AUX,V3, V15	-0.3～5.0 *1	V
Output Current 1	IOV3AUX	1.0	A
Output Current 2	IOV3	2.0	A
Output Current 3	IOV15	2.0	A
Power Dissipation 1	Pd1	500.0 *2	mW
Power Dissipation 2	Pd2	812.5 *3	mW
Operating Temperature Range	Topr	-40～+100	℃
Storage Temperature Range	Tstg	-55～+150	℃
Maximum Junction Temperature	Tjmax	+150	℃

*1 Not to exceed Pd.
*2 Reduced by 4.0mW for each increase in Ta of 1℃ over 25℃
*3 Reduced by 6.5mW for each increase in Ta of 1℃ over 25℃(When mounted on a board 70mm × 70mm × 1.6mm Glass-epoxy PCB)

○ OPERATING CONDITIONS (Ta=25℃)

Parameter	Symbol	MIN	MAX	Unit
Input Voltage 1	V3AUX_IN	3.0	3.6	V
Input Voltage 2	V3_IN	3.0	3.6	V
Input Voltage 3	V15_IN	1.35	1.65	V
Logic Input Voltage 1	EN	-0.3	3.6	V
Logic Input Voltage 2	CPPE#,CPUSB#,SYSR,PERST_IN#,RCLKEN	0	V3AUX_IN	V
Logic Output Voltage 1	RCLKEN	0	V3AUX_IN	V
Logic Output Voltage 2	PERST#	0	V3AUX_IN	V
Output Current 1	IOV3AUX	0	275	mA
Output Current 2	IOV3	0	1.3	A
Output Current 3	IOV15	0	650	mA

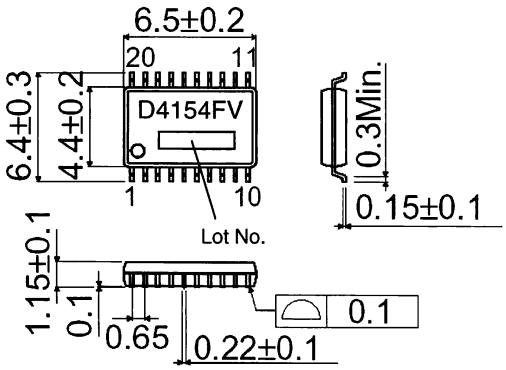
★ This product is not designed for protection against radioactive rays.

Status of this document
The Japanese version of this document is the official specification.
This translated version is intended only as a reference, to aid in understanding the official version.
If there are any differences between the original and translated versions of this document, the official Japanese language version takes priority.

○ ELECTRICAL CHARACTERISTICS (unless otherwise noted, Ta=25℃ VEN=3.3V V3AUX_IN =V3_IN=3.3V,V15_IN=1.5V)

Parameter	Symbol	Standard Value			Unit	Condition
		MIN	TYP	MAX		
Standby Current	IST	-	40	80	uA	VEN=0V (Include IEN, IRCLKEN)
Bias Current 1	Icc1	-	120	250	uA	VSYSR=0V
Bias Current 2	Icc2	-	250	500	uA	VSYSR=3.3V
[Enable]						
High Level Enable Input Voltage	VENHI	2.0	-	5.5	V	
Low Level Enable Input Voltage	VENLOW	-0.2	-	0.8	V	
Enable Pin Input Current	IEN	10	-	30	uA	VEN=0V
[Logic]						
High Level Logic Input Voltage	VLHI	2.0	-	-	V	
Low Level Logic Input Voltage	VLLOW	-	-	0.8	V	
Logic Pin Input Current	ICPPE#	-	0	1	uA	CPPE#=3.6V
		10	-	30	uA	CPPE#=0V
	ICPUSB#	-	0	1	uA	CPUSB#=3.6V
		10	-	30	uA	CPUSB#=0V
	ISYSR	-	0	1	uA	SYSR=3.6V
		10	-	30	uA	SYSR=0V
	IPRT_IN#	-	0	1	uA	PERST_IN#=3.6V
		10	-	30	uA	PERST_IN#=0V
	IRCLKEN	-	0	1	uA	RCLKEN=3.6V
		10	-	30	uA	RCLKEN=0V
RCLKEN Low Voltage	VRCLKEN	-	0.1	0.3	V	IRCLKEN=0.5mA
RCLKEN Leak Current	IRCLKEN	-	-	1	uA	VRCLKEN=3.65V
[Switch V3AUX]						
On Resistance	R_{V3AUX}	-	120	220	mΩ	Tj=-10～100℃
Discharge On Resistance	R_{V3AUX} Dis	-	60	150	Ω	
[Switch V3]						
On Resistance	R_{V3}	-	42	90	mΩ	Tj=-10～100℃
Discharge On Resistance	R_{V3}Dis	-	60	150	Ω	
[Switch V15]						
On Resistance	R_{V15}	-	45	90	mΩ	Tj=-10～100℃
Discharge On Resistance	R_{V15}Dis	-	60	150	Ω	
[Over Current Protection]						
V3 Over Current	OCP_{V3}	1.3	-	-	A	
V3AUX Over Current	OCP_{V3AUX}	0.275	-	-	A	
V15 Over Current	OCP_{V15}	0.65	-	-	A	
[Under Voltage Lockout]						
V3_IN UVLO OFF Voltage	$VUVLO_{V3\_IN}$	2.70	2.80	2.90	V	sweep up
V3_IN Hysteresis Voltage	$\Delta VUVLO_{V3\_IN}$	50	100	150	mV	sweep down
V3AUX_IN UVLO OFF Voltage	$VUVLO_{V3AUX\_IN}$	2.70	2.80	2.90	V	sweep up
V3AUX_IN Hysteresis Voltage	$\Delta VUVLO_{V3AUX\_IN}$	50	100	150	mV	sweep down
V15_IN UVLO OFF Voltage	$VUVLO_{V15\_IN}$	1.15	1.20	1.25	V	sweep up
V15_IN Hysteresis Voltage	$\Delta VUVLO_{V15\_IN}$	50	100	150	mV	sweep down
[POWER GOOD]						
V3 POWER GOOD Voltage	PG_{V3}	2.700	2.850	3.000	V	
V3AUX POWER GOOD Voltage	PG_{V3AUX}	2.700	2.850	3.000	V	
V15 POWER GOOD Voltage	PG_{V15}	1.200	1.275	1.350	V	
PERST# LOW Voltage	$VPERST\#_{Low}$	-	0.1	0.3	V	I_{PERST}=0.5mA
PERST# HIGH Voltage	$VPERST\#_{HIGH}$	3.0	-	-	V	
PERST# Delay Time	$T_{PERST\#}$	4	-	20	ms	
PERST# assertion time	Tast	-	-	500	ns	
[OUTPUT RISE TIME]						
V3_IN to V3	T_{V3}	0.1	-	3	ms	
V3AUX_IN to V3AUX	T_{V3AUX}	0.1	-	3	ms	
V15_IN to V15	T_{V15}	0.1	-	3	ms	

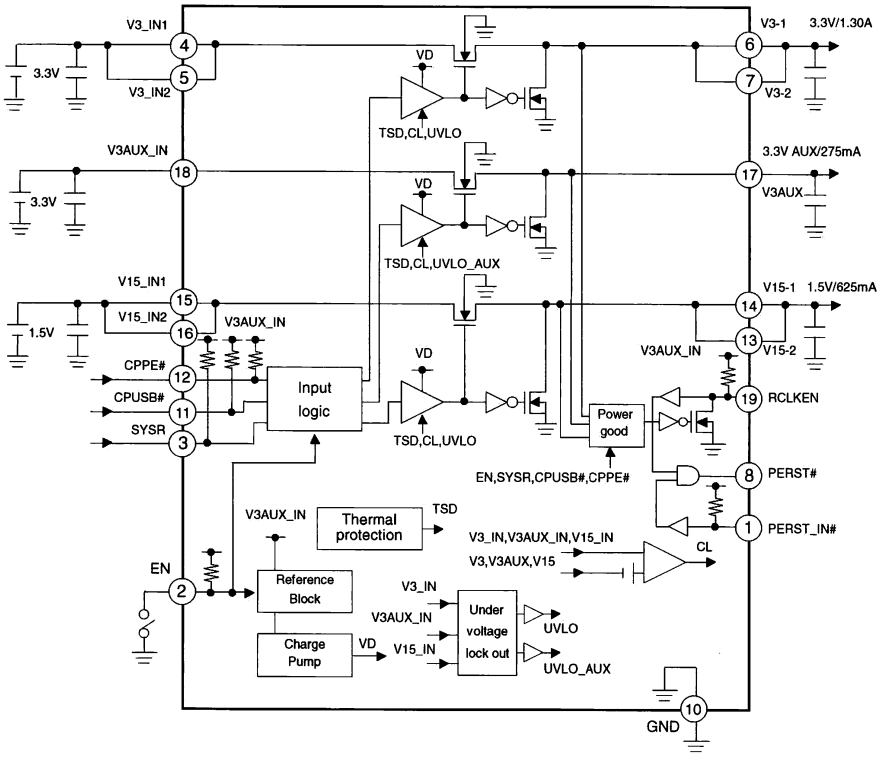
O PHYSICAL DIMENSIONS



(UNIT:mm)

SSOP-B20

O BLOCK DIAGRAM



O PIN DESCRIPTION

Pin number	Pin name
1	PERST_IN#
2	EN
3	SYSR
4	V3_IN1
5	V3_IN2
6	V3_1
7	V3_2
8	PERST#
9	TEST
10	GND
11	CPUSB#
12	CPPE#
13	V15_1
14	V15_2
15	V15_IN1
16	V15_IN2
17	V3AUX
18	V3AUX_IN
19	RCLKEN
20	NC

ONOTES FOR USE

(1) Absolute maximum ratings

Exceeding the absolute maximum ratings, including applied voltage and operating temperature range, may damage or destroy the IC. Since the cause of the damage cannot be conclusively identified (as, for example, a short or open mode), be sure to take appropriate physical safety measures, such as incorporating fuses, whenever a special mode anticipated to exceed absolute maximum ratings is employed.

(2) Thermal design

Provide sufficient margin in the thermal design to account for the allowable power dissipation (Pd) expected in actual use.

(3) Electromagnetic fields

Use in strong electromagnetic fields may cause malfunctions. Be careful operating in electromagnetic fields.

(4) Thermal shutdown circuit

The IC is provided with a built-in thermal shutdown (TSD) circuit. When chip temperature reaches the threshold temperature shown below, output goes to a cut-off (open) state. Note that the TSD circuit is designed exclusively to shut down the IC in abnormal thermal conditions. It is not intended to protect the IC per se or guarantee performance when extreme heat occurs. Therefore, the TSD circuit should not be employed with the expectation of continued use or subsequent operation once TSD is operated.

TSD ON temperature [℃] (typ.)	Hysteresis temperature [℃] (typ.)
175	15

(5) Ground wiring pattern

When both a small-signal GND and high current GND are present, single-point grounding (at the set standard point) is recommended, in order to separate the small-signal and high current patterns, and to be sure the voltage change stemming from the wiring resistance and high current does not cause any voltage change in the small-signal GND. In the same way, care must be taken to avoid wiring pattern fluctuations in any connected external component GND.

(6) Electrical Characteristics

Be sure to check the electrical characteristics, such as transient characteristics in the present specification, since these can be changed by temperature, supply voltage, and external circuits.

(7) Input Capacitor

The input capacitor reduces the output impedence of the voltage supply source. If the output impedence of this power supply increases, the input voltage (V3_IN,V3AUX_IN,V15_IN) may become unstable. A 0.1uF capacitor for the V3AUX_IN pin, and a 1uF capacitor for V3_IN and V15_IN pin are recommended. A low ESR capacitor with minimal susceptibility to temperature is preferable, but stability depends on power supply characteristics and the substrate wiring pattern. Please confirm operation across a variety of temperature and load conditions.

(8) Output Capacitor

Mount an output capacitor between output pin (V3,V3AUX,V15)and GND for stability purposes. A 10uF capacitor for the V3 and V15 pin, and a 1uF capacitor for the V3AUX pin are recommended. A low ESR capacitor with minimal susceptibility to temperature is preferable, but stability depends on power supply characteristics and the substrate wiring pattern. Please confirm operation across a variety of temperature and load conditions.

(9) Short-circuits between pins and and mounting errors

When mounting the IC onto a set substrate or circuit board, be careful to avoid incorrect orientation or mis-positioning of the IC, as such mounting errors may cause device malfunctions. Similar damage may occur when the power supply connection is reversed. Also, note that the introduction of foreign material between pins and the GND, or between the pins themselves may cause shorts and destroy the IC.

(10) Power dissipation

When exercising modes that exceed Pd, there is a risk that IC characteristics, such as current capability, may be negatively impacted by the rise in chip temperature. Provide sufficient margin in the thermal design to account for the allowable power dissipation (Pd) expected in actual use.

(11) Operating Conditions

The circuit functionality is guaranteed within the operating ambient temperature range. The standard electrical characteristics cannot be guaranteed, except at Ta=25℃. However, any variation will be small.

(12) Operating stability depends on the layout pattern. Make sure the wiring pattern for the input (V3_IN, V3AUX_IN, V15_IN) and the output (V3, V3AUX, V15) on the application board is designed wide and short , in order to minimize layout impedance.

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