IRU1260

DUAL 6A AND 1A LOW DROPOUT POSITIVE ADJUSTABLE REGULATOR

FEATURES

- Guaranteed <1.3V Dropout at 6A (Output #2)
- Guaranteed <0.6V Dropout at 1A (Output #1)
- Fast Transient Response
- 1% Voltage Reference Initial Accuracy
- Built-In Thermal Shutdown

APPLICATIONS

- Providing a Single Package Solution for GTL+ and High Speed Bus Termination
- Dual Supply P55C™ Applications

DESCRIPTION

The IRU1260 uses a proprietary process and combines a dual low dropout adjustable output regulator in a single package with one output having a minimum of 6A and the other one having a 1A output current capability. This product is specifically designed to provide well regulated supplies for low voltage ICs such as 3.3V to 1.5V and 2.5V supplies for the GTL+ termination and the new clock for Pentium II™ applications. Other applications include low cost dual supply for processors such as Intel P55C™ where 2.8V and 3.3V are needed for the Core and the I/O supplies from the 5V input.

TYPICAL APPLICATION

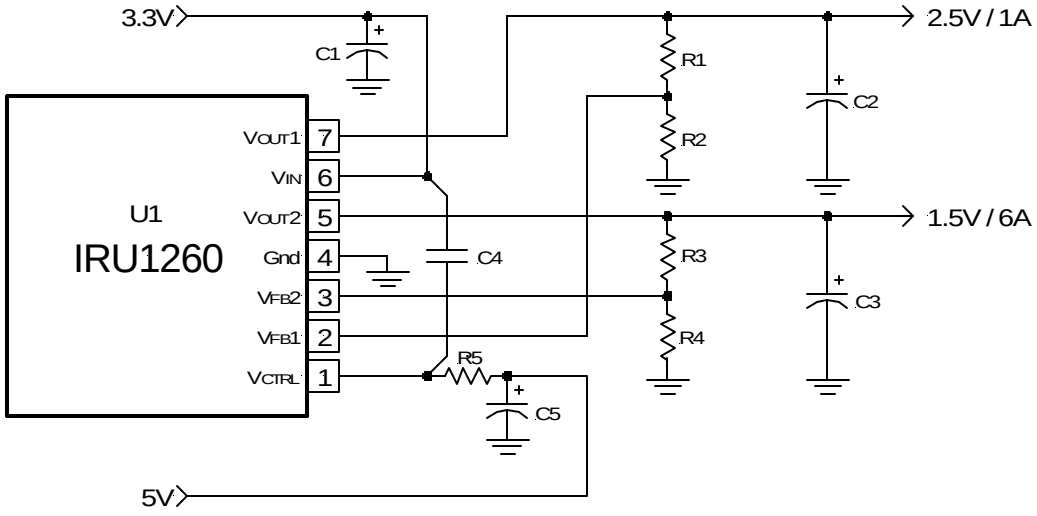


Figure 1 - Typical application of IRU1260 in the Pentium II™ design with the 1.5V output providing for GTL+ termination while 2.5V supplies the clock chip.

Notes: Pentium II™ is trademark of Intel Corp.
P55C™ is trademark of Intel Corp.

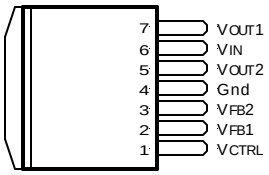
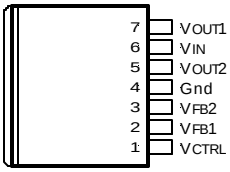
PACKAGE ORDER INFORMATION

T_J (°C)	7-PIN PLASTIC TO-263 (M)	7-PIN PLASTIC Ultra Thin-Pak™ (P)
0 To 150	IRU1260CM	IRU1260CP

ABSOLUTE MAXIMUM RATINGS

Input Voltage (V_{IN}) 7V
Power Dissipation ..... Internally Limited
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 150°C

PACKAGE INFORMATION

7-PIN PLASTIC TO-263 (M)	7-PIN ULTRA THIN-PAK (P)
	
θ_{JA}=30°C/W for 1"sq pad	θ_{JA}=30°C/W for 1"sq pad

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over C_{IN}=1µF, C_{OUT}=10µF and T_J=0 to 150°C. Typical values refer to T_J=25°C. I_{FL}=6A for output #1 and I_{FL}=1A for output #2. V_{FB}=V_{OUT} for both outputs. V_{CTRL}=V_{IN}=3.3V.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
V_{CTRL} Input Voltage			3.0			V
Reference Voltage	V_{REF}	Io=10mA, T_J=25°C	1.188	1.200	1.212	V
		Io=10mA	1.176	1.200	1.224	
Line Regulation		Io=10mA, V_{OUT}+1.3V<V_{IN}=V_{CTRL}<7V		0.2		%
Load Regulation (Note 1)		10mA<Io<I_{FL}		0.4		%
Dropout Voltage (Output #2)		Io=4A, V_{CTRL}=4.75V, V_{IN}=3.3V			1.0	V
(Note 2)		Io=3A, V_{CTRL}=4.75V, V_{IN}=3.3V			0.7	
		Io=2A, V_{CTRL}=4.75V, V_{IN}=3.3V		0.35	0.5	
Dropout Voltage (Output #1)		Io=1A, V_{CTRL}=4.75V, V_{IN}=3.3V		0.4	0.6	V
(Note 2)		Io=1A, V_{CTRL}=V_{IN}=4.75V			1.3	
Current Limit (Output #2)	I_{CL2}	ΔVo=100mV	6.1			A
Current Limit (Output #1)	I_{CL1}	ΔVo=100mV	1.1			A
Thermal Regulation		30ms pulse, Io=I_{FL}		0.01	0.02	%/W
Ripple Rejection		f=120Hz, Co=25µF Tantalum, Io=0.5 × I_{FL}		70		dB
Feedback Pin Input Current	I_{FB}	Io=10mA		0.02		µA
Temperature Stability		Io=10mA		0.5		%
Long Term Stability		T_A=125°C, 1000Hrs		0.3	1	%
RMS Output Noise		T_A=25°C, 10Hz<f<10KHz		0.003		%V_O
Minimum Load Current (Note 3)				5		mA

Note 1: Low duty cycle pulse testing with Kelvin connections is required in order to maintain accurate data.

Note 2: Dropout voltage is defined as the minimum differential voltage between V_{IN} and V_{OUT} required to maintain regulation at V_{OUT}. It is measured when the output voltage drops 1% below its nominal value.

Note 3: Minimum load current is defined as the minimum current required at the output in order for the output voltage to maintain regulation. Typically the resistor divider values are selected such that this current is automatically maintained.

PIN DESCRIPTIONS

PIN #	PIN SYMBOL	PIN DESCRIPTION
1	V_{CTRL}	The control input pin of the regulator. This pin via a 10Ω resistor is connected to the 5V supply to provide the base current for the pass transistor of both regulators. This allows the regulator to have very low dropout voltage which allows one to generate a well regulated 2.5V supply from the 3.3V input. A high frequency, 1µF capacitor is connected between this pin and V_{IN} pin to insure stability.
2	$V_{FB}1$	A resistor divider from this pin to $V_{OUT}1$ pin and ground sets the output voltage. See application circuit for the divider setting for 2.5V output.
3	$V_{FB}2$	A resistor divider from this pin to the $V_{OUT}2$ pin and ground sets the output voltage. See application circuit for the divider setting for 1.5V output.
4	Gnd	This pin is connected to ground. It is also the tab of the package.
5	$V_{OUT}2$	The output #2 (high current) of the regulator. A minimum of 100µF capacitor must be connected from this pin to ground to insure stability.
6	V_{IN}	The power input pin of the regulator. Typically a large storage capacitor is connected from this pin to ground to insure that the input voltage does not sag below the minimum dropout voltage during the load transient response. This pin must always be higher than both V_{OUT} pins by the amount of the dropout voltage in order for the device to regulate properly.(See data sheet)
7	$V_{OUT}1$	The output #1 (low current) of the regulator. A minimum of 100µF capacitor must be connected from this pin to ground to insure stability.

BLOCK DIAGRAM

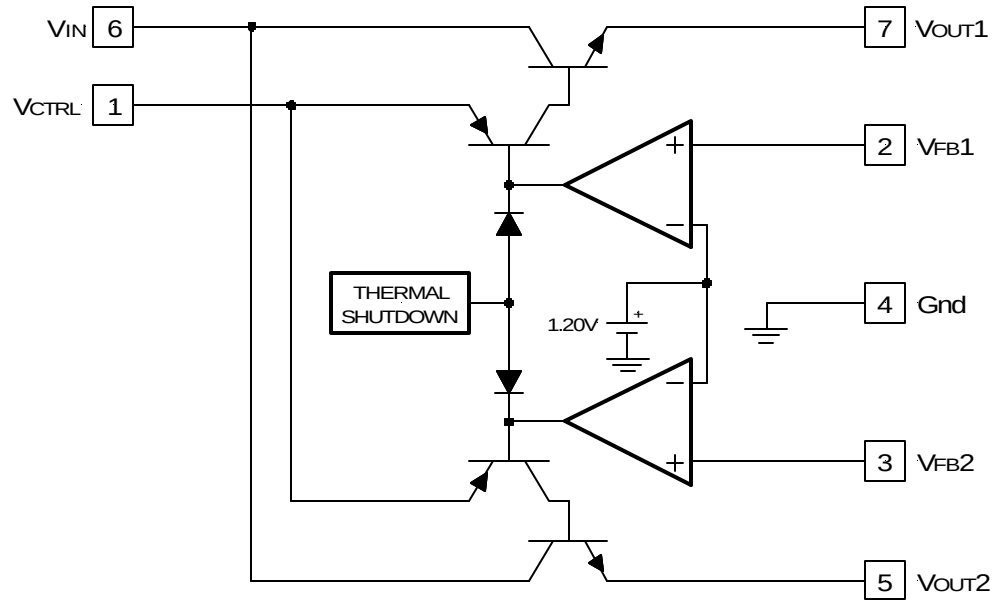


Figure 2 - Simplified block diagram of the IRU1260.

APPLICATION INFORMATION

Introduction

The IRU1260 is a dual adjustable Low Dropout (LDO) regulator which can easily be programmed with the addition of two external resistors to any voltages within the range of 1.20 to 5.5V. This voltage regulator is designed specifically for applications that require two separate regulators such as the Intel Pentium II™ processors requiring 1.5V and 2.5V supplies, eliminating the need for a second regulator which results in lower overall system cost. When V_{CTRL} pin is connected to a supply which is at least 1V higher than V_{IN}, the dropout voltage improves by 30% which makes it ideal for applications requiring less than the standard 1.3V dropout given in the LDO products such as IRU10XX series. The IRU1260 also provides an accurate 1.20V voltage reference common to both regulators for programming each output voltage. Other features of the device include: fast response to sudden load current changes, such as GTL+ termination application for Pentium II™ family of microprocessors. The IRU1260 also includes thermal shutdown protection to protect the device if an overload condition occurs.

Output Voltage Setting

The IRU1260 can be programmed to any voltages in the range of 1.20V to 5.5V with the addition of R1 and R2 external resistors according to the following formula:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_2}{R_1}\right) + R_2 \times I_B$$

Where:
V_{REF} = 1.20V Typically
I_B = 0.02μA Typical
R1 and R2 as shown in Figure 3:

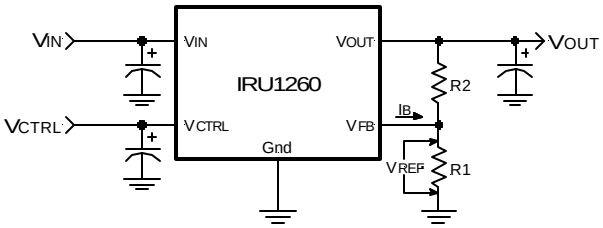


Figure 3 - Typical application of the IRU1260 for programming the output voltage. (Only one output is shown here)

The IRU1260 keeps a constant 1.2V between the V_{FB} pin and ground pin. By placing a resistor R1 across these two pins a constant current flows through R1, adding to the I_{FB} current and into the R2 resistor producing a voltage equal to the $(1.2/R1) \times R2 + I_{FB} \times R2$ which will be added to the 1.2V to set the output voltage as shown in the above equation. Since the input bias current of the amplifier (I_{FB}) is only 0.02μA typically, it adds a very small error to the output voltage and for most applications can be ignored. For example, in a typical 1.5V GTL+application if R1=10.2KΩ and R2=2.55KΩ the error due to the I_{ADJ} is only 0.05mV which is less than 0.004% of the nominal set point. The effective input impedance seen by the feedback pins (The parallel combination of R1 and R2) must always be higher than 1.8KΩ in order for the regulator to start up properly.

Load Regulation

Since the IRU1260 does not provide a separate ground pin for the reference voltage, it is not possible to provide true remote sensing of the output voltage at the load. Figure 4 shows that the best load regulation is achieved when the bottom side of R1 resistor is connected directly to the ground pin of IRU1260 (preferably to the tab of the device) and the top side of R2 resistor is connected to the load. In fact, if R1 is connected to the load side, the effective resistance between the regulator and the load is gained up by the factor of (1+R2/R1), or the effective resistance will be, $R_{P(eff)} = R_P \times (1+R2/R1)$. It is important to note that for high current applications, this can represent a significant percentage of the overall load regulation and one must keep the path from the regulator to the load as short as possible to minimize this effect.

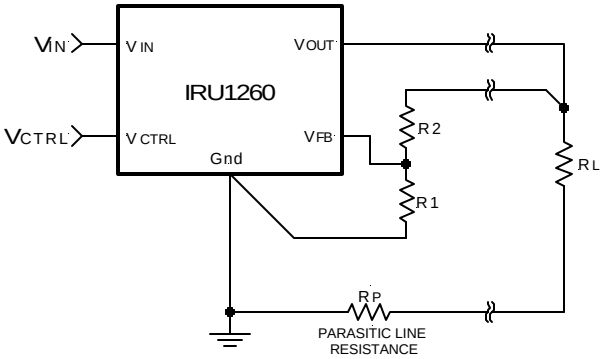


Figure 4 - Schematic showing connection for best load regulation. (Only one output is shown here)

Stability

The IRU1260 requires the use of an output capacitor as part of the frequency compensation in order to make the regulator stable. Typical designs for the microprocessor applications use standard electrolytic capacitors with typical ESR in the range of 50 to 100mΩ and the output capacitance of 500 to 1000μF. Fortunately as the capacitance increases, the ESR decreases resulting in a fixed RC time constant. The IRU1260 takes advantage of this phenomena in making the overall regulator loop stable. For most applications a minimum of 100μF aluminum electrolytic capacitor with the maximum ESR of 0.3Ω such as Sanyo, MVGX series, Panasonic FA series as well as the Nichicon PL series insures both stability and good transient response. The IRU1260 also requires a 1μF ceramic capacitor connected from V_{IN} to V_{CTRL} and a 10Ω, 0.1W resistor in series with V_{CTRL} pin in order to further insure stability.

Thermal Design

The IRU1260 incorporates an internal thermal shutdown that protects the device when the junction temperature exceeds the maximum allowable junction temperature. Although this device can operate with junction temperatures in the range of 150°C, it is recommended that the selected heat sink be chosen such that during maximum continuous load operation the junction temperature is kept below this number. The example given shows the steps in selecting the proper regulator heat sink for driving the Pentium II™ processor GTL+ termination resistors and the Clock IC using the IRU1260 TO-263 package.

Example**:**

Assuming the following specifications:

V_{IN} = 3.3V
V_{OUT1} = 2.5V
V_{OUT2} = 1.5V
$I_{OUT1(MAX)}$ = 0.2A
$I_{OUT2(MAX)}$ = 1.5A
T_A = 35°C

The steps for selecting a proper heat sink to keep the junction temperature below 135°C is given as:

1) Calculate the maximum power dissipation using:

$$P_D = I_{OUT1} \times (V_{IN} - V_{OUT1}) + I_{OUT2} \times (V_{IN} - V_{OUT2})$$

$$P_D = 0.2 \times (3.3 - 2.5) + 1.5 \times (3.3 - 1.5) = 2.86W$$

2) Assuming a TO-263 surface mount package, the junction to ambient thermal resistance of the package is:

θ_{JA} = 30°C/W for 1" square pad area

3) The maximum junction temperature of the device is calculated using the equation below:

$$T_J = T_A + P_D \times \theta_{JA}$$

$$T_J = 35 + 2.86 \times 30 = 121°C$$

Since this is lower than our selected 135°C maximum junction temperature (150°C is the thermal shutdown of the device), TO-263 package is a suitable package for our application.

Layout Consideration

The IRU1260 like all other high speed linear regulators need to be properly laid out to insure stable operation. The most important component is the output capacitor, which needs to be placed close to the output pin and connected to this pin using a plane connection with a low inductance path.

IRU1260 in Ultra LDO, Single Output Application

The IRU1260 can also be used in single supply applications where the difference between input and output is much lower than the standard 1.5V dropout that is obtainable with standard LDO devices. The schematic in Figure 7 shows the application of the IRU1260 in a single supply with the second LDO being disabled.

In this application, the IRU1260 is used on the VGA card to convert 3.3V supply to 2.7V to power the Intel 740 chip rather than the conventional LDO which due to its 1.5V minimum dropout spec must use the 5V supply to achieve the same result. The difference is a substantial decrease in the power dissipation as shown below.

The maximum power dissipation of the Intel 740 chip is 5.8W, which at 2.7V results in:

$$Io = \frac{5.8}{2.7} = 2.15A$$

a) Using standard LDO, the power dissipated in the device is:

$$P_D = (V_{IN} - Vo) \times Io = (5 - 2.7) \times 2.15 = 4.94W$$

Using surface mount TO-263 package with 25°C/W junction to air thermal resistance results in:

$$T_J = P_D \times \theta_{JA} + T_A = 4.94 \times 25 + 25 = 148°C$$

This is very close to the thermal shutdown of the IC.

b) Using IRU1260, the power dissipated in the device is drastically reduced by using 3.3V supply instead of 5V.

$$P_D = (V_{IN} - Vo) \times Io = (3.3 - 2.7) \times 2.15 = 1.3W$$

Using surface mount TO-263 package with 25°C/W junction to air thermal resistance results in:

$$T_J = P_D \times \theta_{JA} + T_A = 1.3 \times 25 + 25 = 57°C$$

A reduction of 91°C in junction temperature.

TYPICAL APPLICATION

PENTIUM II™ APPLICATION

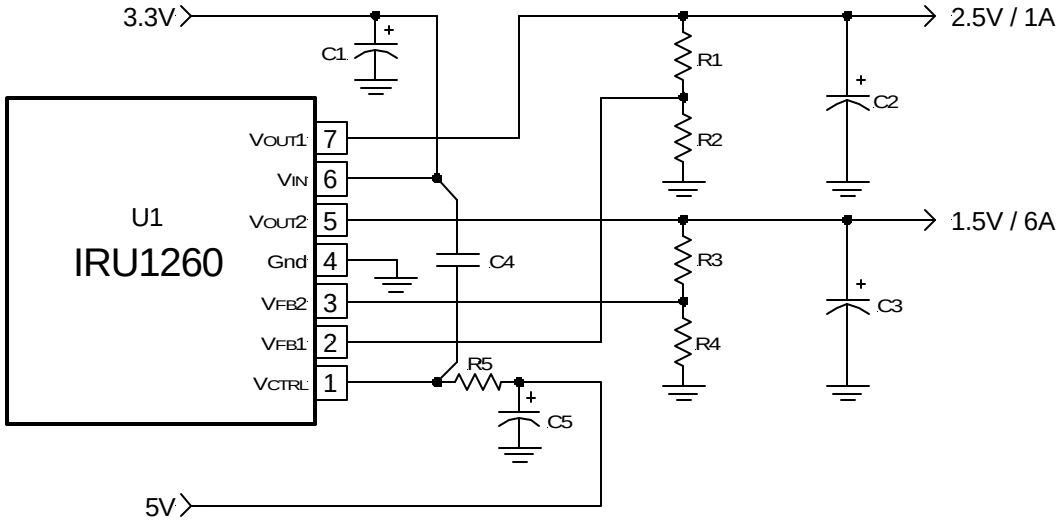


Figure 5 - Typical application of IRU1260 in the Pentium II™ design with the 1.5V output providing for GTL+ termination while 2.5V supplies the clock chip.

Note: Pentium II is trademark of Intel Corp.

Ref Desig	Description	Qty	Part #	Manuf
U1	Dual LDO Regulator	1	IRU1260CM	IR
C1, C3	Capacitor	2	Elect, 680µF, EEUFA1A681L	Panasonic
C2	Capacitor	1	Elect, 220µF, 6.3V, ECAOJFQ221	Panasonic
C4	Capacitor	1	Ceramic, 0.1µF, SMT, 0805	Panasonic
C5	Capacitor	1	Elect,100µF, 6.3V, ECAOJFQ101	Panasonic
R1	Resistor	1	11KΩ, 1%, SMT, 0805	Panasonic
R2, R4	Resistor	2	10.2KΩ, 1%, SMT, 0805	Panasonic
R3	Resistor	1	2.55KΩ, 1%, SMT, 0805	Panasonic
R5	Resistor	1	3Ω, 5%, SMT, 0805	Panasonic
HS1	Heat Sink		Use 1" Square Copper Pad area if I_{OUT2}<1.7A & I_{OUT1}<0.2A. For I_{OUT2}<3A & I_{OUT1}<0.5A, use IRU1260CT and Thermalloy 6030B	

TYPICAL APPLICATION

RAMBUS APPLICATION

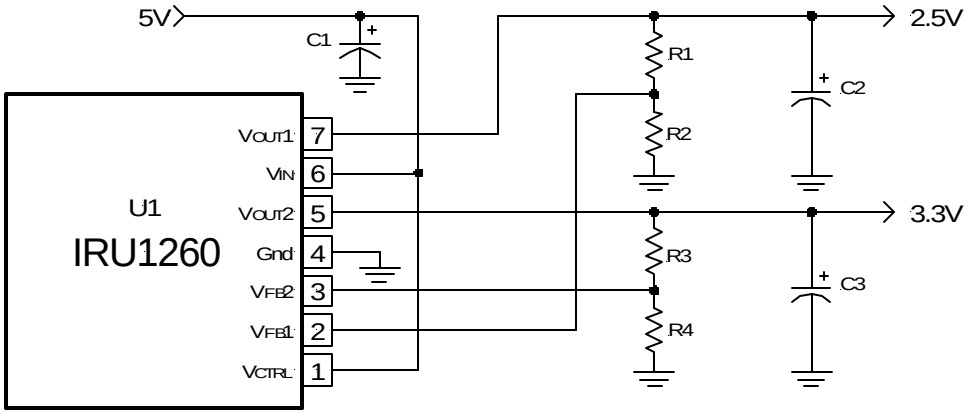


Figure 6 - Typical application of IRU1260 in the Rambus™ design with the 2.5V output providing for memory termination while 3.3V supplies the on board logic.

Note: Rambus™ is trademark of Rambus Corp.

Ref Desig	Description	Qty	Part #	Manuf
U1	Dual LDO Regulator	1	IRU1260CM	IR
C1, C2, C3	Capacitor	3	Elect, 220µF, 6.3V, ECAOJFQ221	Panasonic
R1	Resistor	1	11KΩ, 1%, SMT, 0805	Panasonic
R2, R4	Resistor	2	10.2KΩ, 1%, SMT, 0805	Panasonic
R3	Resistor	1	17.8KΩ, 1%, SMT, 0805	Panasonic
HS1	Heat Sink		1" Square Copper Pad area if I_{OUT2}<1.2A & I_{OUT1}<0.5A. For I_{OUT2}<3A & I_{OUT1}<0.5A, use Thermalloy 6030B	

TYPICAL APPLICATION

INTEL 740 GRAPHICS CHIP APPLICATION

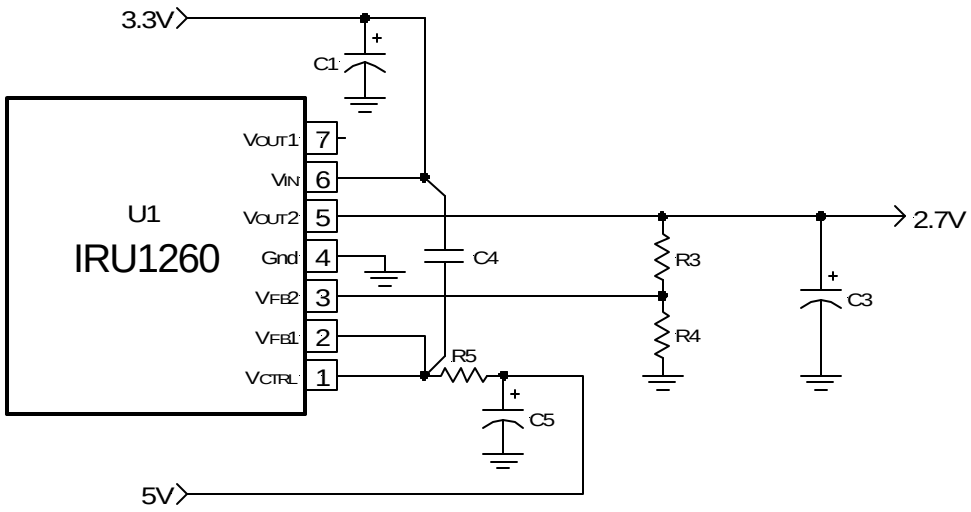


Figure 7 - Typical application of IRU1260 to provide 2.7V from the 3.3V bus for the Intel 740 graphics chip.

Ref Desig	Description	Qty	Part #	Manuf
U1	Dual LDO Regulator	1	IRU1260CM	IR
C1, C3	Capacitor	2	Elect, 680µF, EEUFA1A681L	Panasonic
C4	Capacitor	1	Ceramic, 0.1µF, SMT, 0805	Panasonic
C5	Capacitor	1	Elect,100µF, 6.3V, ECAOJFQ101	Panasonic
R4	Resistor	1	10.2KΩ, 1%, SMT, 0805	Panasonic
R3	Resistor	1	12.7KΩ, 1%, SMT, 0805	Panasonic
R5	Resistor	1	3Ω, 5%, SMT, 0805	Panasonic

International
IOR Rectifier

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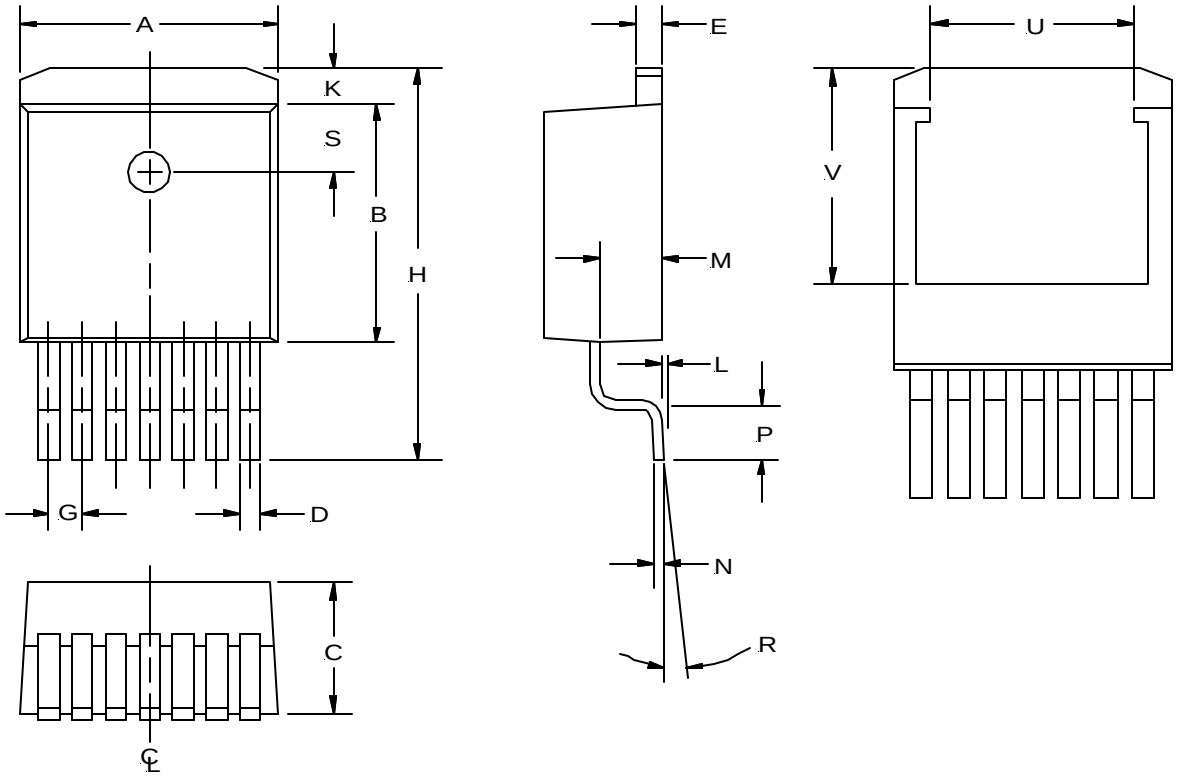
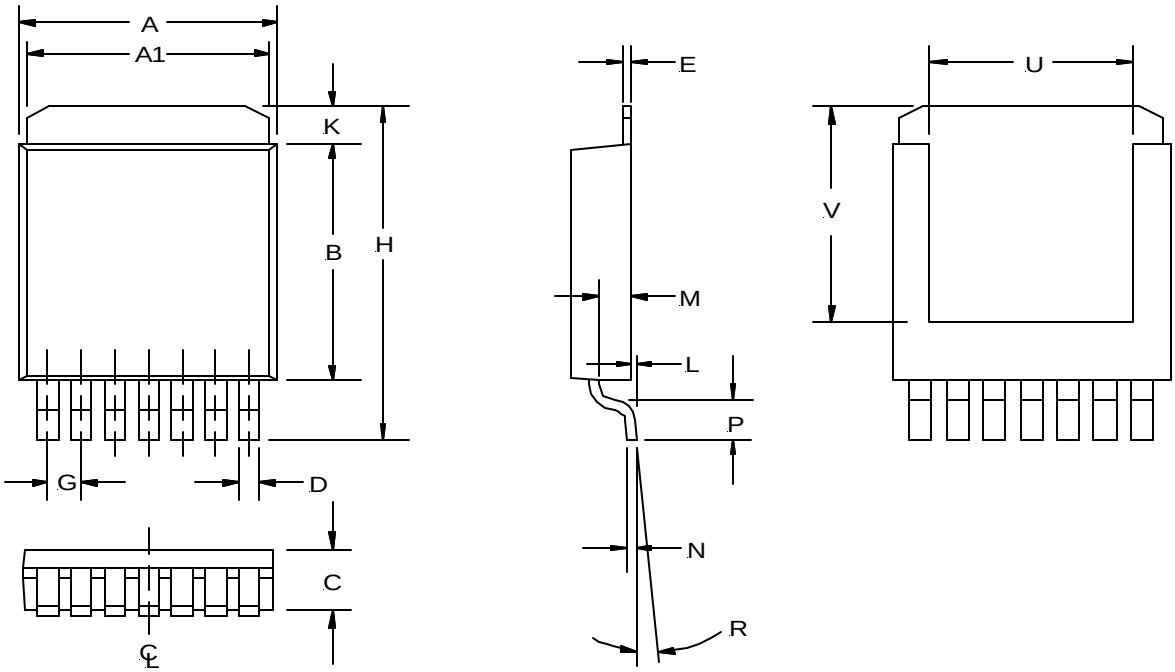
(M) TO-263 Package
7-Pin



SYMBOL	MIN	MAX
A	10.05	10.31
B	8.28	8.53
C	4.31	4.57
D	0.66	0.91
E	1.14	1.40
G	1.27 REF	
H	14.73	15.75
K	1.40	1.68
L	0.00	0.25
M	2.49	2.74
N	0.43	0.58
P	2.29	2.79
R	0°	8°
S	2.41	2.67
U	6.50 REF	
V	7.75 REF	

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

(P) Ultra Thin-Pak™
7-Pin

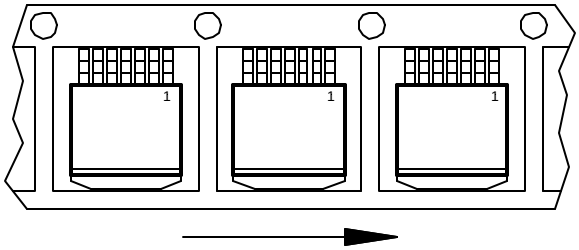


SYMBOL	MIN	MAX
A	9.27	9.52
A1	8.89	9.14
B	7.87	8.13
C	1.78	2.03
D	0.63	0.79
E	0.25 NOM	
G	1.27	
H	10.41	10.67
K	0.76	1.27
L	0.03	0.13
M	0.89	1.14
N	0.25	
P	0.79	1.04
R	3°	6°
U	5.59 NOM	
V	7.49 NOM	

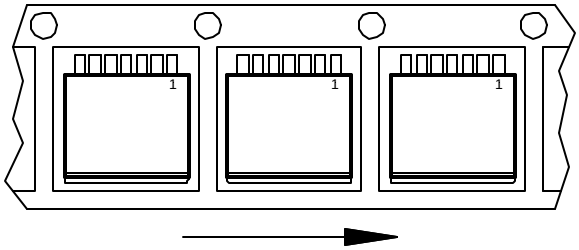
NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

PACKAGE SHIPMENT METHOD

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
M	TO-263	7	50	750	Fig A
P	Ultra Thin-Pak™	7	75	2500	Fig B



Feed Direction
Figure A



Feed Direction
Figure B

International
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