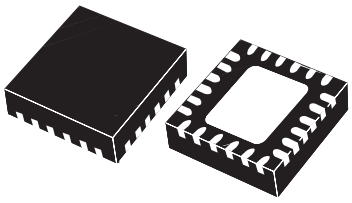
LNBH26

Dual LNB supply and control IC with step-up and I²C interface

Data brief

Features

- Complete interface between LNB and I²C bus
- Built-in DC-DC converter for single 12 V supply operation and high efficiency (typ. 93% @ 0.5 A)
- Selectable output current limit by external resistor
- Compliant with main satellite receiver output voltage specification
- Accurate built-in 22 kHz tone generator compliant with widely accepted standards
- Low-drop post regulator and high efficiency step-up PWM with integrated power N-MOS allows lower power losses
- LPM function (low power mode) to reduce dissipation
- Overload and overtemperature internal protections with I²C diagnostic bits
- LNB short-circuit dynamic protection
- +/- 4 kV ESD tolerance on output power pins



QFN24 (4 x 4 mm)

Applications

- STB satellite receivers
- TV satellite receivers
- PC card satellite receivers

Description

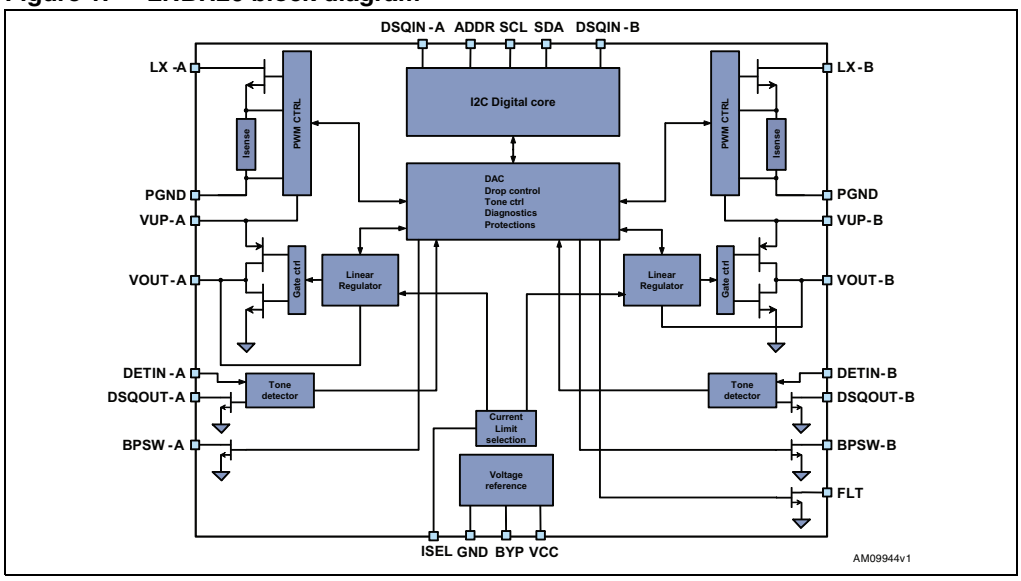
Intended for analog and digital dual satellite receivers/Sat-TV and Sat-PC cards, the LNBH26 is a monolithic voltage regulator and interface IC assembled in a QFN24 (4 x 4 mm) package, specifically designed to provide the 13/18 V power supply and the 22 kHz tone signal to the LNB down-converter in antenna dishes or to multi-switch boxes. This device offers a complete solution in a simple design for dual tuner satellite receivers, with the added benefit of extremely low component count, low power dissipation and I²C standard interfacing.

Table 1. Device summary

Order code	Package	Packaging
LNBH26PQR	QFN24 (4 x 4 mm)	Tape and reel

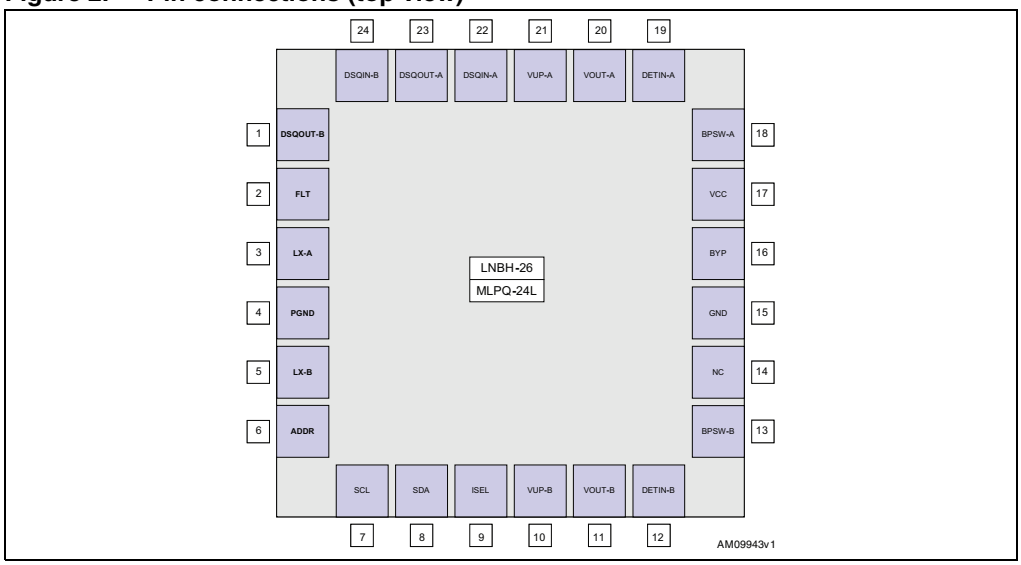
1 Block diagram

Figure 1. LNBH26 block diagram



2 Pin configuration

Figure 2. Pin connections (top view)



3 Maximum ratings

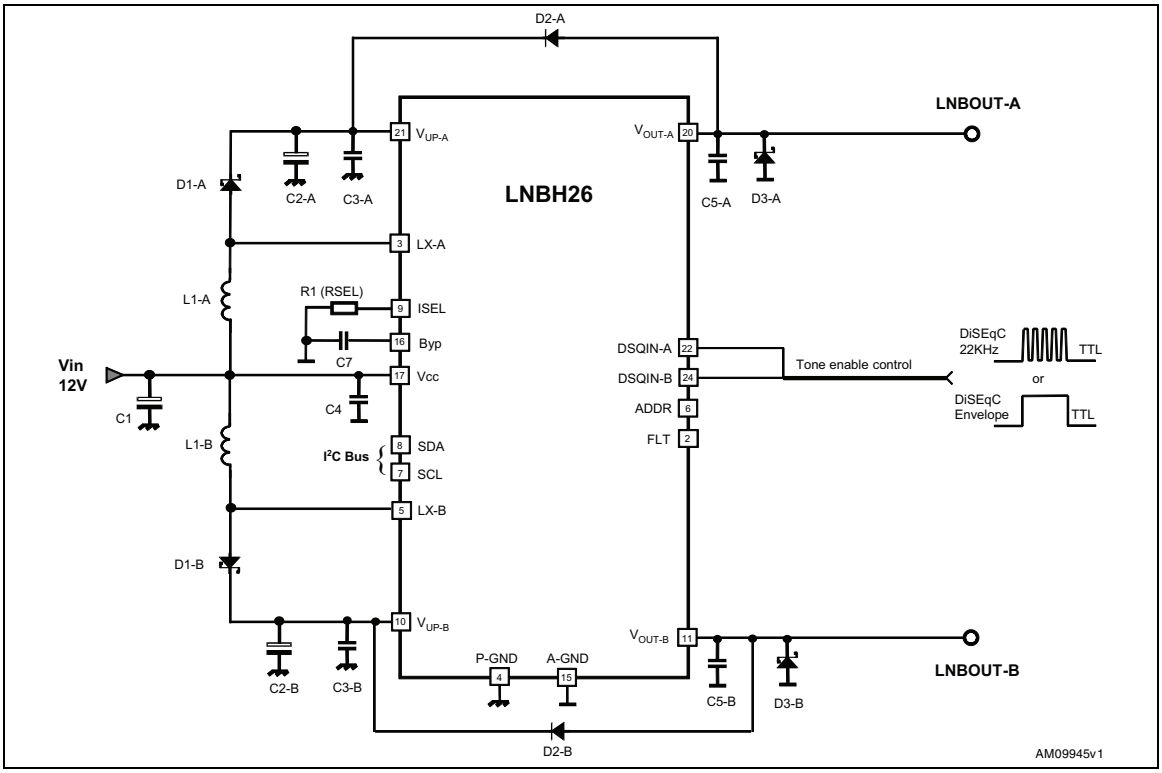
Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC power supply input voltage pins	- 0.3 to 20	V
V_{UP}	DC input voltage	- 0.3 to 40	V
I_{OUT}	Output current	Internally limited	mA
V_{OUT}	DC output pin voltage	- 0.3 to 40	V
V_I	Logic input pins voltage (SDA, SCL, DSQIN, ADDR pins)	- 0.3 to 7	V
V_O	Logic output pins voltage (FLT, DSQOUT)	- 0.3 to 7	V
V_{DETIN}	Detector input signal amplitude	TBD	V
V_{BPSW}	BPSW pin voltage	- 0.3 to 40	V
I_O	Logic output pins current (FLT, DSQOUT, BPSW)	10	mA
LX	LX input voltage	- 0.3 to 30	V
V_{BYP}	Internal reference pin voltage	- 0.3 to 4.6	V
ISEL	Current selection pin voltage	- 0.3 to 4.6	V
T_{STG}	Storage temperature range	- 50 to 150	°C
T_J	Operating junction temperature range	- 25 to 125	°C
ESD	ESD rating with human body model (HBM) for all pins, except power output pins	2	kV
	ESD rating with human body model (HBM) for power output pins	4	

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to network ground terminal.

4 Typical application circuit

Figure 3. DiSEqC 1.x application circuit



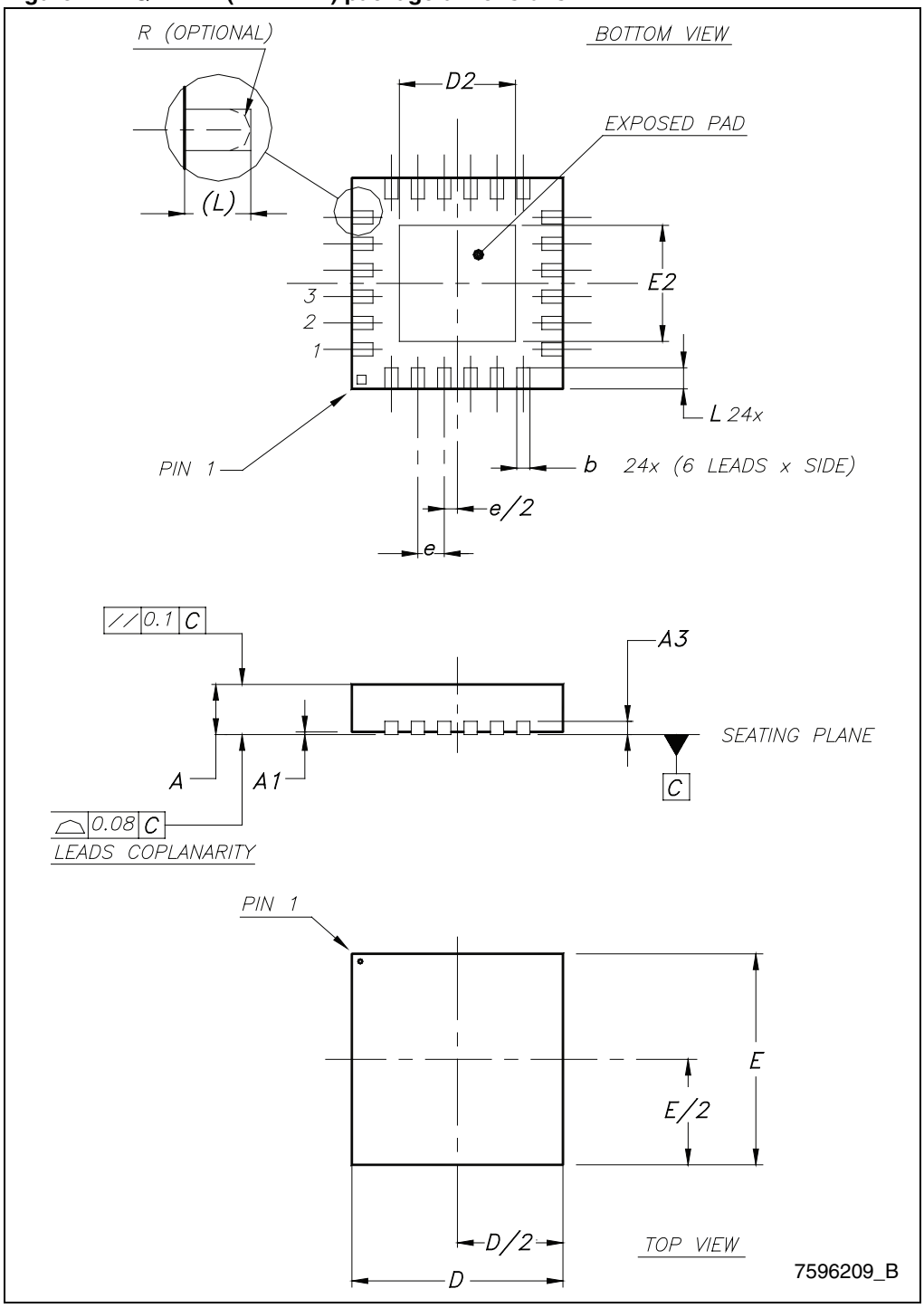
5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 3. QFN24L (4 x 4 mm) mechanical data

Dim.	(mm.)		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3		0.20	
b	0.18	0.25	0.30
D	3.85	4.00	4.15
D2	2.00	2.15	2.25
E	3.85	4.00	4.15
E2	2.00	2.15	2.25
e		0.50	
L	0.30	0.40	0.50

Figure 4. QFN24L (4 x 4 mm) package dimensions



6 Revision history

Table 4. Document revision history

Date	Revision	Changes
05-Sep-2011	1	Initial release.
02-Nov-2011	2	Modified order code *Table 1 on page 1*

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