SINGLE CHANNEL MOBILE PWM AND LDO CONTROLLER

PRELIMINARY DATA SHEET

Pb Free Product

DESCRIPTION

The NX2139A controller IC is a compact Buck controller IC with 16 lead MLPQ package designed for step down DC to DC converter in portable applications. It can be selected to operate in synchronous mode or non-synchronous mode to improve the efficiency at light load.Constant on time control provides fast response, good line regulation and nearly constant frequency under wide voltage input range. The NX2139A controller is optimized to convert single supply up to 24V bus voltage to as low as 0.75V output voltage. Over current protection and FB UVLO followed by latch feature. A built-in LDO controller can drive an external N-MOSFET to provide a second output voltage from either PWM output source or other power source. Both PWM controller and LDO controller have separate EN feature. Other features includes: 5V gate drive capability, power good indicator, over voltage protection, internal Boost schottky diode and adaptive dead band control.

FEATURES

- Internal Boost Schottky Diode
- Ultrasonic mode operation available
- Bus voltage operation from 4.5V to 24V
- Less than 1uA shutdown current with Enable low
- Excellent dynamic response with constant on time control
- Selectable between Synchronous CCM mode and diode emulation mode to improve efficiency at light load
- Programmable switching frequency
- Current limit and FB UVLO with latch off
- Over voltage protection with latch off
- LDO controller with seperate enable
- Two independent Power Good indicator available
- Pb-free and RoHS compliant

APPLICATIONS

- Notebook PCs and Desknotes
- Tablet PCs/Slates
- On board DC to DC such as 12V to 3.3V, 2.5V or 1.8V
- Hand-held portable instruments

TYPICAL APPLICATION

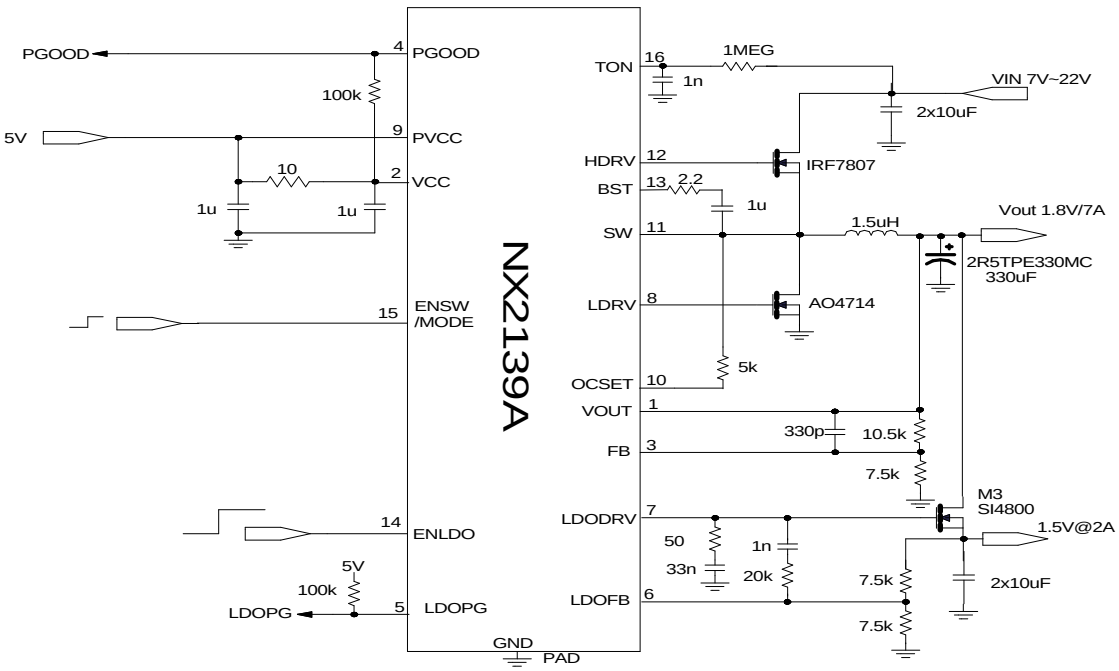

Figure1 - Typical application of NX2139A

ORDERING INFORMATION

Device	Temperature	Package	Pb-Free
NX2139ACMTR	-10°C to 100°C	3X3 MLPQ-16L	Yes

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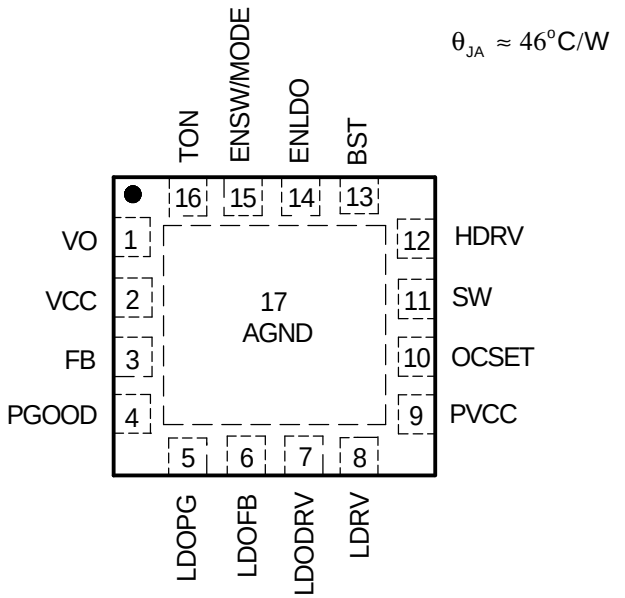
ABSOLUTE MAXIMUM RATINGS

VCC,PVCC to GND & BST to SW voltage ..... -0.3V to 6.5V
TON to GND ..... -0.3V to 28V
HDRV to SW Voltage ..... -0.3V to 6.5V
SW to GND ..... -2V to 30V
All other pins ..... VCC+0.3V
Storage Temperature Range .....-65°C to 150°C
Operating Junction Temperature Range .....-40°C to 150°C
ESD Susceptibility 2kV

CAUTION: Stresses above those listed in "ABSOLUTE MAXIMUM RATINGS", may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

PACKAGE INFORMATION

3x3 16-LEAD PLASTIC MLPQ



ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over Vcc =5V, VIN=15V and T_A=25°C, unless otherwise specified.

PARAMETER	SYM	Test Condition	Min	TYP	MAX	Units
VIN						
recommended voltage range	V_{IN}		4.5		24	V
Shut down current		ENLDO=GND, ENSW=GND		1		uA
VCC,PVCC Supply						
Input voltage range	V_{CC}		4.5		5.5	V
Operating quiescent current		VFB=0.85V, ENLDO=GND, ENSW=5V		1.8		mA
Shut down current		ENLDO=GND, ENSW=GND		1		uA

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PARAMETER	SYM	Test Condition	Min	TYP	MAX	Units
VCC UVLO						
Under-voltage Lockout threshold	V_{CC}_UVLO		3.9	4.1	4.5	V
Falling VCC threshold			3.7	3.9	4.3	V
ON and OFF time						
TON operating current		VIN=15V, Rton=1Mohm		15		uA
ON -time		VIN=9V,VOUT=0.75V, Rton=1Mohm	312	390	468	ns
Minimum off time			380	590	800	ns
FB voltage						
Internal FB voltage	Vref		0.739	0.75	0.761	V
Input bias current					100	nA
Line regulation		VCC from 4.5V to 5.5V	-1		1	%
OUTPUT voltage						
Output range			0.75		3.3	V
VOUT shut down discharge resistance		ENSW/MODE=GND		30		ohm
Soft start time				1.5		ms
PGOOD						
Pgood high rising threshold				90		% Vref
PGOOD delay after softstart		NOTE1		1.6		ms
PGOOD propagation delay filter		NOTE1		2		us
Power good hysteresis				5		%
Pgood output switch impedance				13		ohm
Pgood leakage current				1		uA
SW zero cross comparator						
Offset voltage				5		mV
High Side Driver (CL=3300pF)						
Output Impedance , Sourcing Current	R_{source}(Hdrv)	I=200mA		1.5		ohm
Output Impedance , Sinking Current	R_{sink}(Hdrv)	I=200mA		1.5		ohm
Rise Time	THdrv(Rise)	10% to 90%		50		ns
Fall Time	THdrv(Fall)	90% to 10%		50		ns
Deadband Time	Tdead(L to H)	Ldrv going Low to Hdrv going High, 10% to 10%		30		ns
Low Side Driver (CL=3300pF)						
Output Impedance, Sourcing Current	R_{source}(Ldrv)	I=200mA		1.5		ohm
Output Impedance, Sinking Current	R_{sink}(Ldrv)	I=200mA		0.5		ohm
Rise Time	TLdrv(Rise)	10% to 90%		50		ns
Fall Time	TLdrv(Fall)	90% to 10%		50		ns
Deadband Time	Tdead(H to L)	SW going Low to Ldrv going High, 10% to 10%		10		ns

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PARAMETER	SYM	Test Condition	Min	TYP	MAX	Units
ENSW/MODE threshold and bias current						
PFM/Non Synchronous Mode			80% VCC		VCC+0.3V	V
Ultrasonic Mode			60% VCC		80% VCC	V
Synchronous Mode		Leave it open or use limits in spec	2		60% VCC	V
Shutdown mode			0		0.8	V
Input bias current		ENSW/MODE=VCC		5		uA
		ENSW/MODE=GND		-5		uA
LDO Controller						
Quiescent current		PWM OFF, LDOEN=HI, IOUT=0mA		1		mA
LDOEN logic high voltage			2			V
LDOEN logic low voltage					0.8	V
LDOFB reference voltage			0.728	0.75	0.773	V
Output UVLO threshold				70		%Vref
Open loop gain		NOTE1		60		DB
LDOFB input bias current					1	uA
LDODrv sourcing current		LDOFB=0.72V		2		mA
LDODrv sinking current		LDOFB=0.78V		2		mA
LDO PGOOD threshold				90		%Vref
LDO PGOOD propagation delay filter		NOTE1		2		us
LDO PGOOD impedance				13		ohm
Current Limit						
Ocset setting current			20	24	28	uA
Over temperature						
Threshold		NOTE1		155		^{o}C
Hysteresis				15		^{o}C
Under voltage						
FB threshold				70		%Vref
Over voltage						
Over voltage tripp point				125		%Vref
Internal Schottky Diode						
Forward voltage drop		Forward current=50mA		500		mV

NOTE1: This parameter is guaranteed by design but not tested in production(GBNT).

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PIN DESCRIPTIONS

PIN NUMBER	PIN SYMBOL	PIN DESCRIPTION
1	VOUT	This pin is directly connected to the output of the switching regulator and senses the VOUT voltage. An internal MOSFET discharges the output during turn off.
2	VCC	This pin supplies the internal 5V bias circuit. A 1uF X7R ceramic capacitor is placed as close as possible to this pin and ground pin.
3	FB	This pin is the error amplifiers inverting input. This pin is connected via resistor divider to the output of the switching regulator to set the output DC voltage from 0.75V to 3.3V.
4	PGOOD	PGOOD indicator for switching regulator. It requires a pull up resistor to Vcc or lower voltage. When FB pin reaches 90% of the reference voltage PGOOD transitions from LO to HI state.
5	LDOPG	PGOOD indicator for LDO, requires a pull up resistor to Vcc or lower voltage. When LDOFB pin reaches 90% of the reference voltage PGOOD transitions from LO to HI state.
6	LDOFB	This pin is the error amplifiers inverting input. This pin is connected via resistor divider to the output of the LDO to set the output DC voltage.
7	LDODRV	The drive signal for external LDO N channel MOSFET.
8	LDRV	Low side gate driver output.
9	PVCC	Provide the voltage supply to the lower MOSFET drivers. Place a high frequency decoupling capacitor 1uF X5R to this pin.
10	OCSET	This pin is connected to the drain of the external low side MOSFET and is the input of over current protection(OCP) comparator. An internal current source is flown to the external resistor which sets the OCP voltage across the Rdson of the low side MOSFET.
11	SW	This pin is connected to source of high side FETs and provide return path for the high side driver. It is also the input of zero current sensing comparator.
12	HDRV	High side gate driver output.
13	BST	This pin supplies voltage to high side FET driver. A high freq 1uF X7R ceramic capacitor and 2.2ohm resistor in series are recommended to be placed as close as possible to and connected to this pin and SW pin.
14	ENLDO	LDO enable input functions only when ENSW/MODE is not shutdown.
15	ENSW/ MODE	Switching converter enable input. Connect to VCC for PFM/Non synchronous mode, connected to an external resistor divider equals to 70%VCC for ultrasonic, connected to GND for shutdown mode, floating or connected to 2V for the synchronous mode.
16	TON	VIN sensing input. A resistor connects from this pin to VIN will set the frequency. A 1nF capacitor from this pin to GND is recommended to ensure the proper operation.
PAD	GND	Power ground.

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BLOCK DIAGRAM

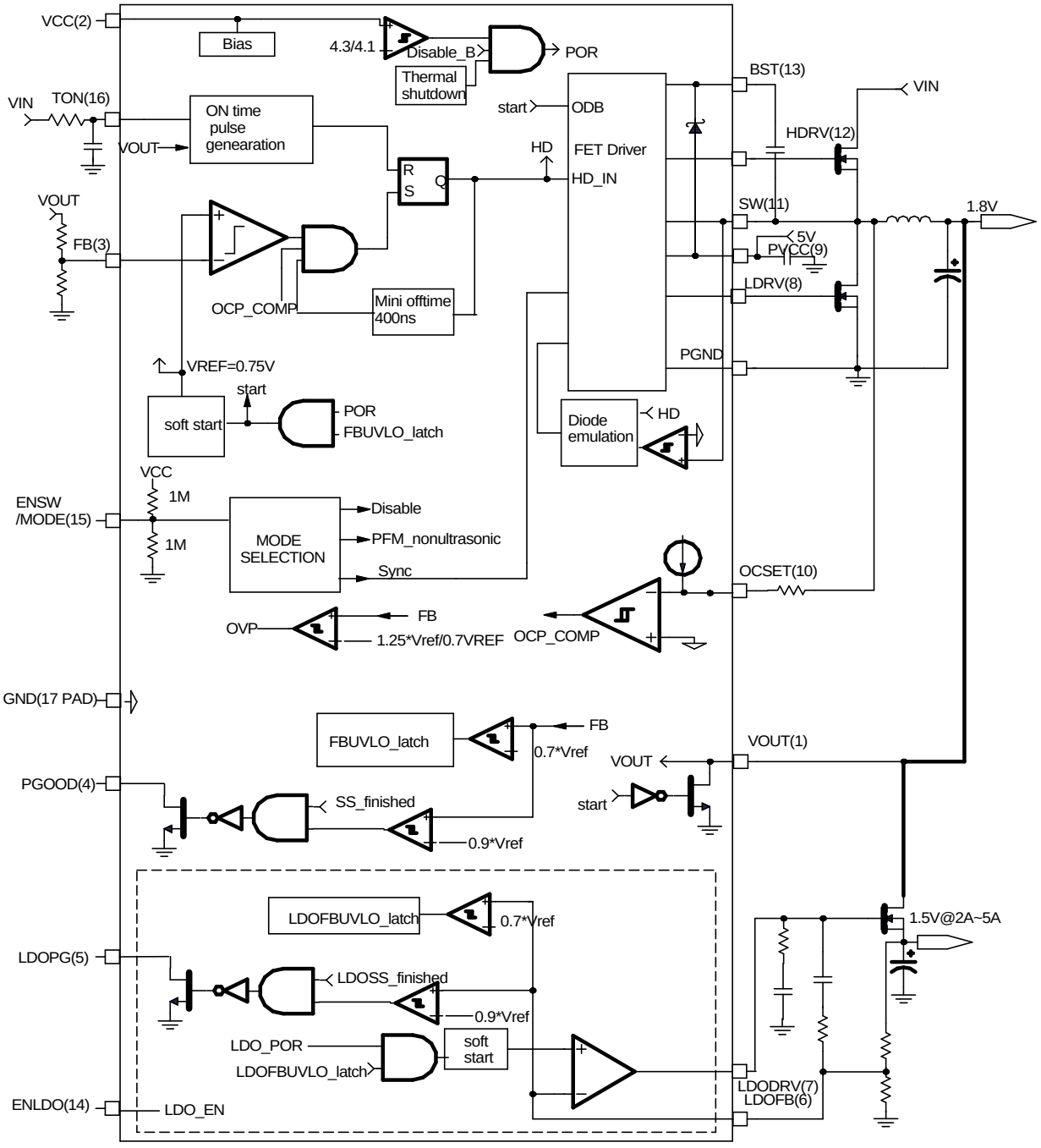

Figure 2 - Simplified block diagram of the NX2139A

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TYPICAL APPLICATION

(VIN=7V to 22V, SW VOUT=1.8V/7A, LDO VOUT=1.5V/2A)

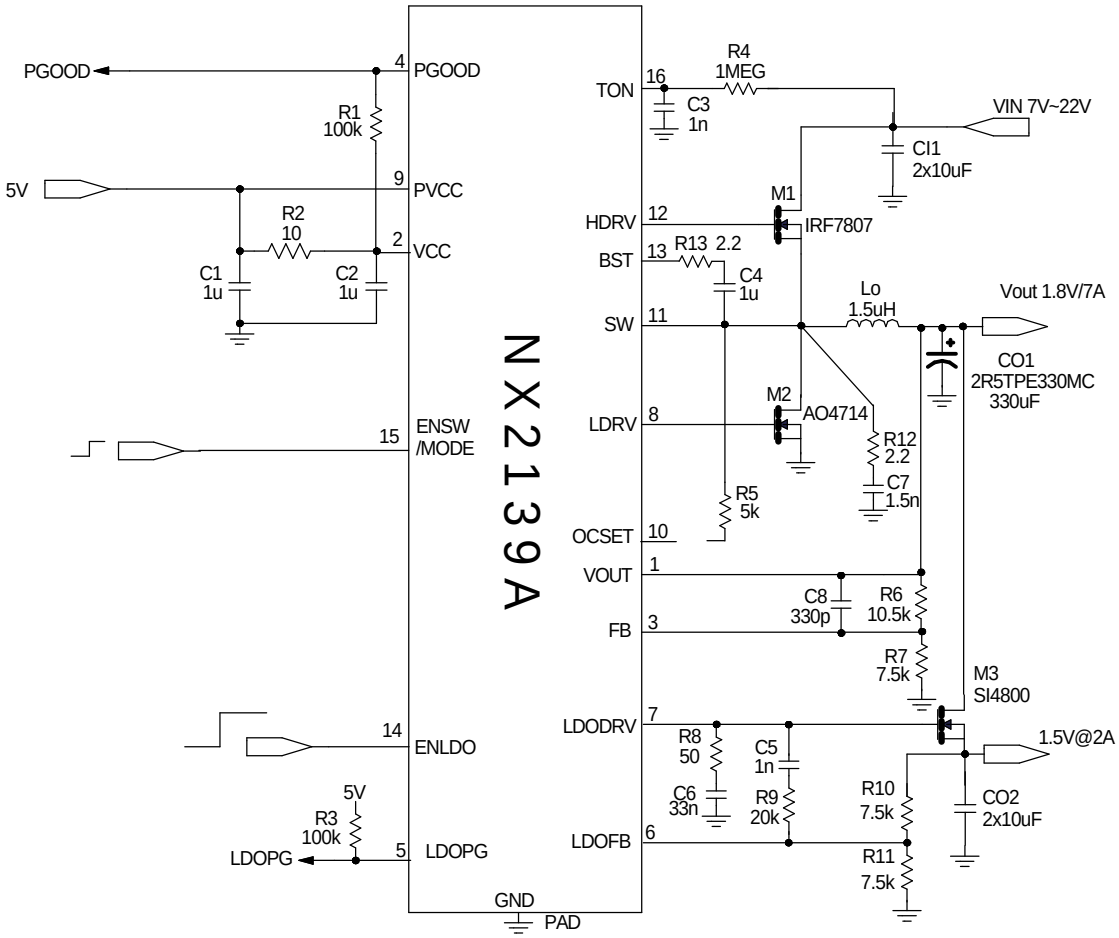

Figure 3 - Demo board schematic

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Bill of Materials

Item	Quantity	Reference	Value	Manufacture
1	2	CI1	10uF/25V/X5R	
2	2	CO2	10uF/6.3V/X5R	
3	1	CO1	2R5TPE330MC	SANYO
4	3	C1,C2,C4	1uF	
5	2	C3,C5	1nF	
6	1	C6	33nF	
7	1	C7	1.5nF	
8	1	C8	330pF	
9	1	Lo	DO5010H-152	COILCRAFT
10	1	M1	IRF7807	IR
11	1	M2	AO4714	AOS
12	1	M3	SI4800	PHILIPS
13	2	R1,R3	100k	
14	1	R2	10	
15	1	R4	1M	
16	1	R5	5k	
17	1	R6	10.5k	
18	3	R7,R10,R11	7.5k	
19	1	R8	50	
20	1	R9	20k	
21	2	R12,R13	2.2	
22	1	U1	NX2139A	NEXSEM INC.

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Demoboard Waveforms

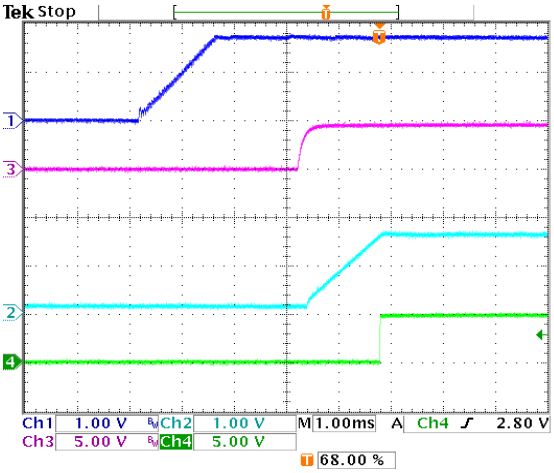

Fig.4 Startup (CH1 1.8V OUTPUT, CH2 1.5V LDO, CH3 SW PGOOD, CH4 LDO PGOOD)

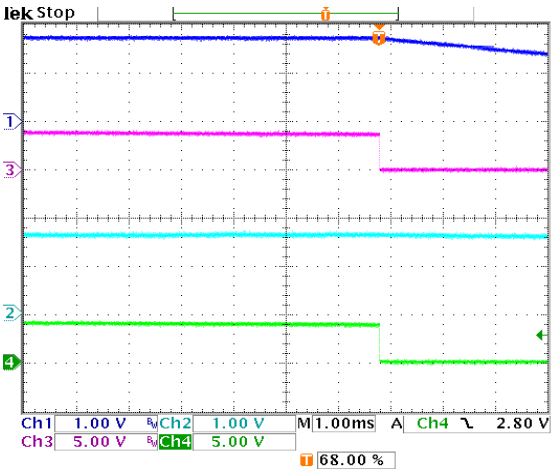

Fig.5 Turn off (CH1 1.8V OUTPUT, CH2 1.5V LDO, CH3 SW PGOOD, CH4 LDO PGOOD)

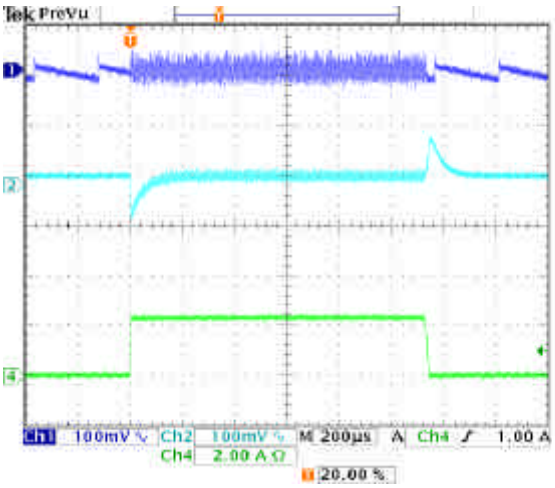

Fig.6 LDO output transient with SW in PFM mode (CH1 1.8V OUTPUT AC, CH2 1.5V LDO AC, CH4 LDO OUTPUT CURRENT)

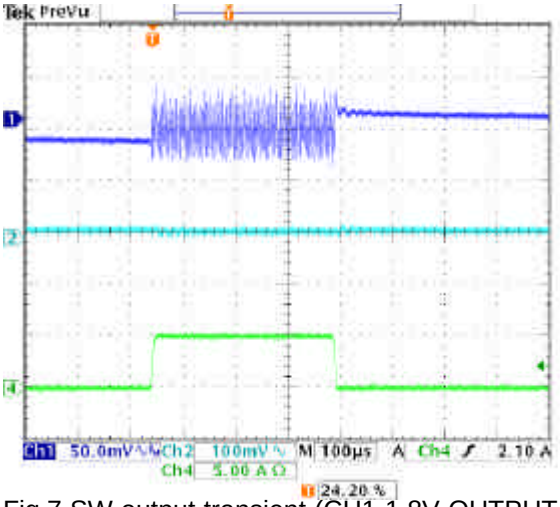

Fig.7 SW output transient (CH1 1.8V OUTPUT AC, CH2 1.5V LDO AC, CH4 1.8V OUTPUT CURRENT)

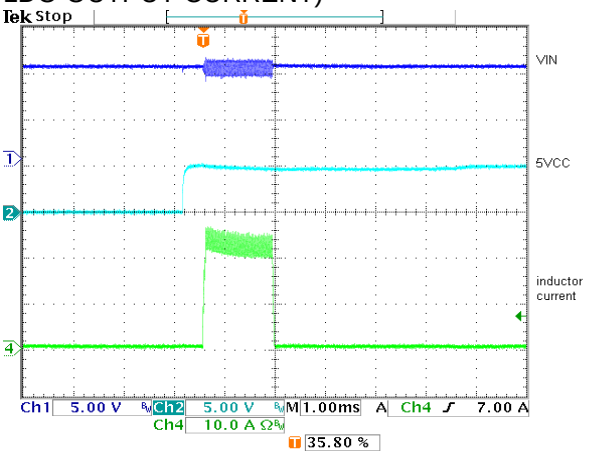

Fig.8 Start into short (CH1 VIN, CH2 5V VCC, CH4 INDUCTOR CURRENT)

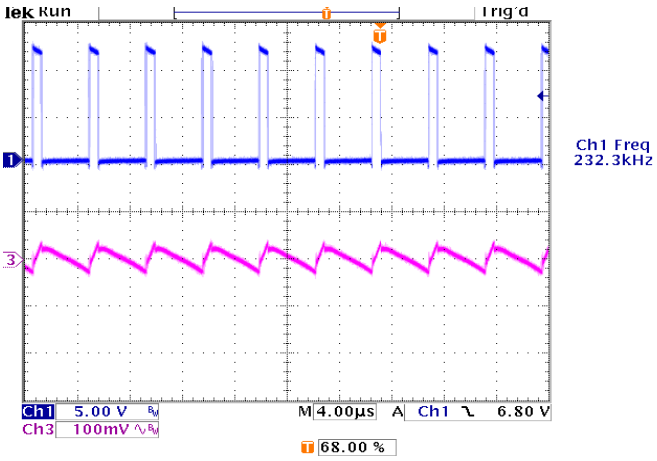

Fig. 9 VOUT ripple @ VIN=12V,IOUT=4A (CH1 SW, CH3 VOUT AC)

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VIN=12V, VOUT=1.8V

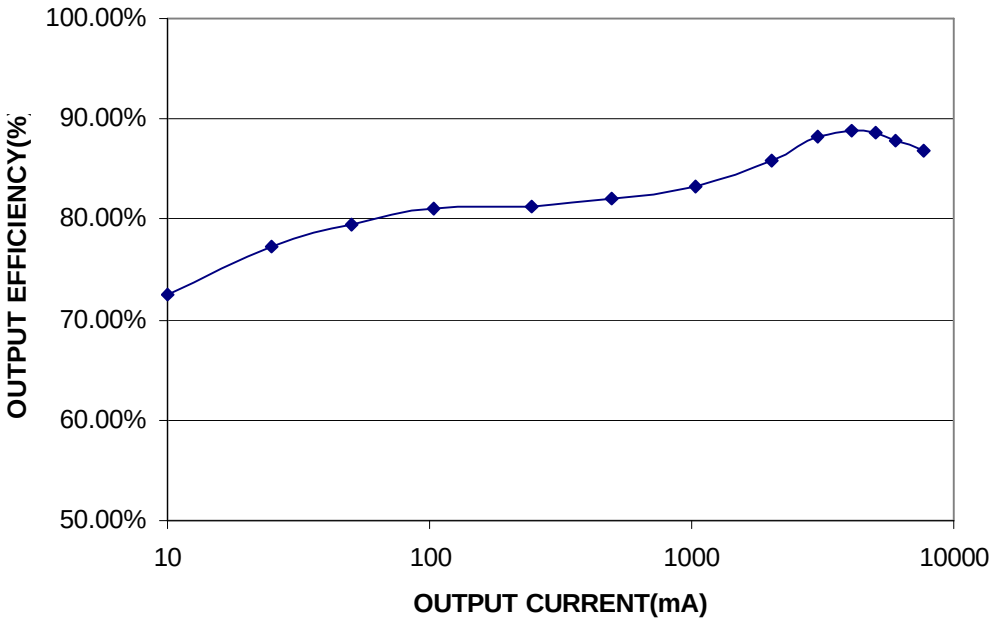

Fig. 10 Output efficiency

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APPLICATION INFORMATION

Symbol Used In Application Information:

V_{IN} - Input voltage
V_{OUT} - Output voltage
I_{OUT} - Output current
ΔV_{RIPPLE} - Output voltage ripple
F_S - Working frequency
ΔI_{RIPPLE} - Inductor current ripple

Design Example

The following is typical application for NX2139A, the schematic is figure 1.

V_{IN} = 7 to 22V
V_{OUT}=1.8V
F_S=220kHz
I_{OUT}=7A
ΔV_{RIPPLE} <=60mV
ΔV_{DROOP}<=60mV @ 3A step

On_Time and Frequency Calculation

The constant on time control technique used in NX2139A delivers high efficiency, excellent transient dynamic response, make it a good candidate for step down notebook applications.

An internal one shot timer turns on the high side driver with an on time which is proportional to the input supply V_{IN} as well inversely proportional to the output voltage V_{OUT}. During this time, the output inductor charges the output cap increasing the output voltage by the amount equal to the output ripple. Once the timer turns off, the Hdrv turns off and cause the output voltage to decrease until reaching the internal FB voltage of 0.75V on the PFM comparator. At this point the comparator trips causing the cycle to repeat itself. A minimum off time of 400nS is internally set.

The equation setting the On Time is as follows:

$$TON = \frac{4.45\times10^{-12}\times R_{TON}\times V_{OUT}}{V_{IN}-0.5V} \quad ...(1)$$

$$F_S = \frac{V_{OUT}}{V_{IN}\times TON} \quad ...(2)$$

In this application example, the RTON is chosen to be 1Mohm, when VIN=22V, the TON is 372nS and F_S is around 220kHz.

Output Inductor Selection

The value of inductor is decided by inductor ripple current and working frequency. Larger inductor value normally means smaller ripple current. However if the inductance is chosen too large, it brings slow response and lower efficiency. The ripple current is a design freedom which can be decided by design engineer according to various application requirements. The inductor value can be calculated by using the following equations:

$$L_{OUT} = \frac{(V_{IN}-V_{OUT})\times T_{ON}}{I_{RIPPLE}} \quad ...(3)$$
$$I_{RIPPLE} = k\times I_{OUTPUT}$$

where k is percentage of output current.

In this example, inductor from COILCRAFT DO5010H-152 with L=1.5uH is chosen.

Current Ripple is recalculated as below:

$$I_{RIPPLE} = \frac{(V_{IN}-V_{OUT})\times T_{ON}}{L_{OUT}} = \frac{(22V-1.8V)\times 372nS}{1.5uH} \quad ...(4)$$
$$=5A$$

Output Capacitor Selection

Output capacitor is basically decided by the amount of the output voltage ripple allowed during steady state(DC) load condition as well as specification for the load transient. The optimum design may require a couple of iterations to satisfy both conditions.

Based on DC Load Condition

The amount of voltage ripple during the DC load condition is determined by equation(5).

$$\Delta V_{RIPPLE} = ESR\times\Delta I_{RIPPLE} + \frac{\Delta I_{RIPPLE}}{8\times F_S\times C_{OUT}} \quad ...(5)$$

Where ESR is the output capacitors' equivalent series resistance,C_{OUT} is the value of output capacitors.

Typically POSCAP is recommended to use in NX2139's applications. The amount of the output voltage ripple is dominated by the first term in equation(5)

and the second term can be neglected.

For this example, one POSCAP 2R5TPE330MC is chosen as output capacitor, the ESR and inductor current typically determines the output voltage ripple. When VIN reach maximum voltage, the output voltage ripple is in the worst case.

$$ESR_{desire} = \frac{\Delta V_{RIPPLE}}{\Delta I_{RIPPLE}} = \frac{60mV}{5A} = 12m\Omega \quad ...(6)$$

If low ESR is required, for most applications, multiple capacitors in parallel are needed. The number of output capacitor can be calculate as the following:

$$N = \frac{ESR_E \times \Delta I_{RIPPLE}}{\Delta V_{RIPPLE}} \quad ...(7)$$

$$N = \frac{12m\Omega \times 5A}{60mV}$$

N =1

The number of capacitor has to be round up to a integer. Choose N =1.

Based On Transient Requirement

Typically, the output voltage droop during transient is specified as

$\Delta V_{droop} < \Delta V_{tran}$ @step load ΔI_{STEP}

During the transient, the voltage droop during the transient is composed of two sections. One section is dependent on the ESR of capacitor, the other section is a function of the inductor, output capacitance as well as input, output voltage. For example, for the overshoot when load from high load to light load with a DI_{STEP} transient load, if assuming the bandwidth of system is high enough, the overshoot can be estimated as the following equation.

$$\Delta V_{overshoot} = ESR \times \Delta I_{step} + \frac{V_{OUT}}{2 \times L \times C_{OUT}} \times \tau^2 \quad ...(8)$$

where t is the a function of capacitor,etc.

$$\tau = \begin{cases} 0 & \text{if} \quad L \le L_{crit} \\ \frac{L \times \Delta I_{step}}{V_{OUT}} - ESR \times C_{OUT} & \text{if} \quad L \ge L_{crit} \end{cases} \quad ...(9$$

where

$$L_{crit} = \frac{ESR \times C_{OUT} \times V_{OUT}}{\Delta I_{step}} = \frac{ESR_E \times C_E \times V_{OUT}}{\Delta I_{step}} \quad ...(10)$$

where ESR_E and C_E represents ESR and capacitance of each capacitor if multiple capacitors are used in parallel.

The above equation shows that if the selected output inductor is smaller than the critical inductance, the voltage droop or overshoot is only dependent on the ESR of output capacitor. For low frequency capacitor such as electrolytic capacitor, the product of ESR and capacitance is high and $L \le L_{crit}$ is true. In that case, the transient spec is mostly like to dependent on the ESR of capacitor.

Most case, the output capacitor is multiple capacitor in parallel. The number of capacitor can be calculated by the following

$$N = \frac{ESR_E \times \Delta I_{step}}{\Delta V_{tran}} + \frac{V_{OUT}}{2 \times L \times C_E \times \Delta V_{tran}} \times \tau^2 \quad ...(11)$$

where

$$\tau = \begin{cases} 0 & \text{if} \quad L \le L_{crit} \\ \frac{L \times \Delta I_{step}}{V_{OUT}} - ESR_E \times C_E & \text{if} \quad L \ge L_{crit} \end{cases} \quad ...(12)$$

For example, assume voltage droop during transient is 60mV for 3A load step.

If one POSCAP 2R5TPE330MC(330uF, 12mohm ESR) is used, the crticial inductance is given as

$$L_{crit} = \frac{ESR_E \times C_E \times V_{OUT}}{\Delta I_{step}} =$$

$$\frac{12m\Omega \times 3300\mu F \times 1.8V}{3A} = 23.76\mu H$$

The selected inductor is 1.5uH which is smaller than critical inductance. In that case, the output voltage transient mainly dependent on the ESR.

number of capacitor is

$$N = \frac{ESR_E \times \Delta I_{step}}{\Delta V_{tran}}$$

$$= \frac{12m\Omega \times 3A}{60mV}$$

$$= 0.6$$

Choose N=1.

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Based On Stability Requirement

ESR of the output capacitor can not be chosen too low which will cause system unstable. The zero caused by output capacitor's ESR must satisfy the requirement as below:

$$F_{ESR} = \frac{1}{2\times\pi\times ESR\times C_{OUT}} \le \frac{F_{SW}}{4} \quad ...(13)$$

Besides that, ESR has to be bigger enough so that the output voltage ripple can provide enough voltage ramp to error amplifier through FB pin. If ESR is too small, the error amplifier can not correctly dectect the ramp, high side MOSFET will be only turned off for minimum time 400nS. Double pulsing and bigger output ripple will be observed. In summary, the ESR of output capacitor has to be big enough to make the system stable, but also has to be small enough to satify the transient and DC ripple requirements.

Input Capacitor Selection

Input capacitors are usually a mix of high frequency ceramic capacitors and bulk capacitors. Ceramic capacitors bypass the high frequency noise, and bulk capacitors supply switching current to the MOSFETs. Usually 1uF ceramic capacitor is chosen to decouple the high frequency noise.The bulk input capacitors are decided by voltage rating and RMS current rating. The RMS current in the input capacitors can be calculated as:

$$I_{RMS} = I_{OUT}\times\sqrt{D}\times\sqrt{1-D}$$
$$D = T_{ON}\times F_S \quad ...(14)$$

When V_{IN} = 22V, V_{OUT}=1.8V, I_{OUT}=7A, the result of input RMS current is 1.9A.

For higher efficiency, low ESR capacitors are recommended. One 10uF/X5R/25V and two 4.7uF/X5R/25V ceramic capacitors are chosen as input capacitors.

Power MOSFETs Selection

The NX2139A requires at least two N-Channel power MOSFETs. The selection of MOSFETs is based on maximum drain source voltage, gate source voltage, maximum current rating, MOSFET on resistance and power dissipation. The main consideration is the power loss contribution of MOSFETs to the overall converter efficiency. In this application, one IRF7807 for high side and one AO4714 with integrated schottky diode for low side are used.

There are two factors causing the MOSFET power loss:conduction loss, switching loss.

Conduction loss is simply defined as:

$$P_{HCON} = I_{OUT}^2\times D\times R_{DS(ON)}\times K$$
$$P_{LCON} = I_{OUT}^2\times(1-D)\times R_{DS(ON)}\times K \quad ...(15)$$
$$P_{TOTAL} = P_{HCON} + P_{LCON}$$

where the $R_{DS(ON)}$ will increases as MOSFET junction temperature increases, K is $R_{DS(ON)}$ temperature dependency. As a result, $R_{DS(ON)}$ should be selected for the worst case. Conduction loss should not exceed package rating or overall system thermal budget.

Switching loss is mainly caused by crossover conduction at the switching transition. The total switching loss can be approximated.

$$P_{SW} = \frac{1}{2}\times V_{IN}\times I_{OUT}\times T_{SW}\times F_S \quad ...(16)$$

where I_{OUT} is output current, T_{SW} is the sum of T_R and T_F which can be found in mosfet datasheet, and F_S is switching frequency. Swithing loss P_{SW} is frequency dependent.

Also MOSFET gate driver loss should be considered when choosing the proper power MOSFET. MOSFET gate driver loss is the loss generated by discharging the gate capacitor and is dissipated in driver circuits.It is proportional to frequency and is defined as:

$$P_{gate} = (Q_{HGATE}\times V_{HGS} + Q_{LGATE}\times V_{LGS})\times F_S \quad ...(17)$$

where Q_{HGATE} is the high side MOSFETs gate charge,Q_{LGATE} is the low side MOSFETs gate charge,V_{HGS} is the high side gate source voltage, and V_{LGS} is the low side gate source voltage.

This power dissipation should not exceed maximum power dissipation of the driver device.

Output Voltage Calculation

Output voltage is set by reference voltage and external voltage divider. The reference voltage is fixed

at 0.75V. The divider consists of two ratioed resistors so that the output voltage applied at the Fb pin is 0.75V when the output voltage is at the desired value.

The following equation applies to figure 11, which shows the relationship between V_{OUT} , V_{REF} and voltage divider.

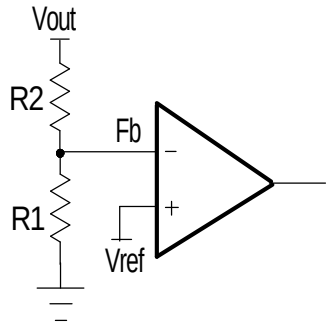

Figure 11 - Voltage Divider

$$R_1 = \frac{R_2 \times V_{REF}}{V_{OUT} - V_{REF}} \qquad ...(18)$$

where R_2 is part of the compensator, and the value of R_1 value can be set by voltage divider.

Mode Selection

NX2139A can be operated in PFM mode, ultrasonic PFM mode, CCM mode and shutdown mode by applying different voltage on ENSW/MODE pin.

When VCC applied to ENSW/MODE pin, NX2139A is In PFM mode. The low side MOSFET emulates the function of diode when discontinuous continuous mode happens, often in light load condition. During that time, the inductor current crosses the zero ampere border and becomes negative current. When the inductor current reaches negative territory, the low side MOSFET is turned off and it takes longer time for the output voltage to drop, the high side MOSFET waits longer to be turned on. At the same time, no matter light load and heavy load, the on time of high side MOSFET keeps the same. Therefore the lightier load, the lower the switching frequency will be. In ultrosonic PFM mode, the lowest frequency is set to be 25kHz to avoid audio frequency modulation. This kind of reduction of frequency keeps the system running at light light with high efficiency.

In CCM mode, inductor current zero-crossing sensing is disabled, low side MOSFET keeps on even when inductor current becomes negative. In this way the efficiency is lower compared with PFM mode at light load, but frequency will be kept constant.

Over Current Protection

Over current protection for NX2139A is achieved by sensing current through the low side MOSFET. An typical internal current source of 24uA flows through an external resistor connected from OCSET pin to SW node sets the over current protection threshold. When synchronous FET is on, the voltage at node SW is given as

$$V_{SW} = -I_L \times R_{DSON}$$

The voltage at pin OCSET is given as

$$I_{OCP} \times R_{OCP} + V_{SW}$$

When the voltage is below zero, the over current occurs as shown in figure below.

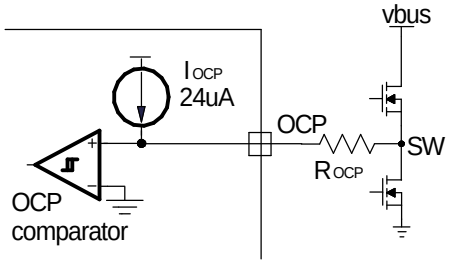

Figure 12 - Over Voltage Protection

The over current limit can be set by the following equation.

$$I_{SET} = I_{OCP} \times R_{OCP} / R_{DSON}$$

If the low side MOSFET R_{DSON}=10mΩ at the OCP occuring moment, and the current limit is set at 12A, then

$$R_{OCP} = \frac{I_{SET} \times R_{DSON}}{I_{OCP}} = \frac{12A \times 10m\Omega}{24uA} = 5k\Omega$$

Choose R_{OCP}=5kΩ

Power Good Output

Power good output is open drain output, a pull up resistor is needed. Typically when softstart is finised and FB pin voltage is over 90% of V_{REF}, the PGOOD pin is pulled to high after a 1.6ms delay.

Smart Over Output Voltage Protection

Active loads in some applications can leak current from a higher voltage than V_{OUT}, cause output voltage to rise. When the FB pin voltage is sensed over 112% of V_{REF}, the high side MOSFET will be turned off and low side MOSFET will be turned on to discharge the V_{OUT}. NX2139A resumes its switching operation after FB pin voltage drops to V_{REF}.

If FB pin voltage keeps rising and is sensed over 125% of V_{REF}, the low side MOSFET will be latched to be on to discharge the output voltage and over voltage protection is triggered. To resume the switching operation, resetting voltage on pin VCC or pin EN is necessary.

Under Output Voltage Protection

Typically when the FB pin voltage is under 70% of V_{REF}, the high side and low side MOSFET will be turned off. To resume the switching operation, VCC or ENSW has to be reset.

LDO Selection Guide

NX2139A offers a LDO controller. The selection of MOSFET to meet LDO is more straight forward. The MOSFET has to be logic level MOSFET and its Rdson at 4.5V should meet the dropout requirement. For example.

V_{LDOIN} =1.8V

V_{LDOOUT} =1.5V

I_{Load} =2A

The maximum Rdson of MOSFET should be

$$R_{RDSON} = (V_{LDOIN} - V_{LDOOUT}) \times I_{LOAD}$$
$$= (1.8V - 1.5V) / 2A = 0.15\Omega$$

Most of MOSFETs can meet the requirement. More important is that MOSFET has to be selected right package to handle the thermal capability. For LDO, maximum power dissipation is given as

$$P_{LOSS} = (V_{LDOIN} - V_{LDOOUT}) \times I_{LOAD}$$
$$= (1.8V - 1.5V) \times 2A = 0.6W$$

Select MOSFET SI4800 with 33mΩ R_{DSON} is sufficient.

LDO Compensation

The diagram of LDO controller including VCC regulator is shown in the following figure.

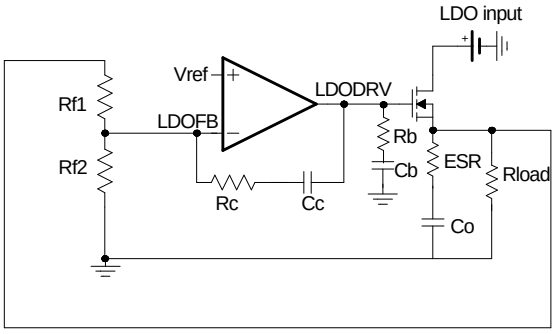

Figure 13 - NX2139A LDO controller.

Rb and Cb have fixed value which is used to compensate the comparater of the LDO controller. Set Rb=50ohm, Cb=33nF.

For most low frequency capacitor such as electrolytic, POSCAP, OSCON, etc, the compensation parameter can be calculated as follows.

$$C_C = \frac{1}{2 \times \pi \times F_O \times R_{f1}} \times \frac{g_m \times ESR}{1 + g_m \times ESR}$$

where F_O is the desired crossover frequency.

Typically, when the POSCAP and electrical capacitor is chosen as output capacitor, crossover frequency F_O has to be 2 to 3 times higher than zero caused by ESR. In this example, we select Fo=150kHz.

g_m is the forward trans-conductance of MOSFET. For SI4800, g_m=19.

Select Rf1=7.5kohm.

Output capacitor is Sanyo POSCAP 4TPE150MI with 150uF, ESR=18mohm.

$$C_C = \frac{1}{2 \times \pi \times 150kHz \times 7.5k\Omega} \times \frac{19S \times 18m\Omega}{1 + 19S \times 18m\Omega} = 36pF$$

Typically C_C is chosen to be 1 to 1.5 times smaller than calculated value to compensate parasitic effect.

Here C_C is chosen to be 33pF. For electrolytic or POSCAP, R_C is typically selected to be zero.

R_{f2} is determined by the desired output voltage.

$$R_{f2}=\frac{R_{f1}\times V_{REF}}{V_{LDOOUT}-V_{REF}}=\frac{7.5k\Omega\times 0.75V}{1.5V-0.75V}=7.5k\Omega$$

Choose R_{f2}=7.5kΩ.

When ceramic capacitors or some low ESR bulk capacitors are chosen as LDO output capacitors, the zero caused by output capacitor ESR is so high that crossover frequency F_O has to be chosen much higher than zero caused by R_C and C_C and much lower than zero caused by ESR. For example, 10uF ceramic is used as output capacitor. We select Fo=300kHz, R_{f1}=7.5kohm and select MOSFET SI4800(g_m=19). R_C and C_C can be calculated as follows.

$$R_C=R_{f1}\times\frac{2\times\pi\times F_O\times C_O}{g_m}\times\frac{1+g_m\times\frac{V_{OUT}}{I_{OUT}}}{g_m\times\frac{V_{OUT}}{I_{OUT}}}$$

$$=7.5k\Omega\times\frac{2\times\pi\times 300kHz\times 20uF}{19S}\times\frac{1+19S\times\frac{1.5V}{2A}}{19S\times\frac{1.5V}{2A}}$$

$$=14.9k\Omega$$

Typically R_C is chosen to be 1 to 1.5 times smaller than calculated value to compensate parasitic effect. Choose R_C=20kΩ.

$$C_C=\frac{10\times C_O}{R_C\times g_m}=\frac{10\times 20uF}{20k\Omega\times 19S}=0.53nF$$

Choose C_C=1000pF.

Current Limit for LDO

Current limit of LDO is achieved by sensing the LDO feedback voltage. When LDO_FB pin is below 70% of V_{REF}, the IC goes into latch mode. The IC will turn off all the channel until VCC or ENSW resets.

Power Good for LDO

Power good output is open drain output, a pull up resistor is needed. Typically when softstart is finised and LDOFB pin voltage is over 90% of V_{REF}, the LDOPGOOD pin is pulled to high.

Layout Considerations

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

There are two sets of components considered in the layout which are power components and small signal components. Power components usually consist of input capacitors, high-side MOSFET, low-side MOSFET, inductor and output capacitors. A noisy environment is generated by the power components due to the switching power. Small signal components are connected to sensitive pins or nodes. A multilayer layout which includes power plane, ground plane and signal plane is recommended .

Layout guidelines:

1. First put all the power components in the top layer connected by wide, copper filled areas. The input capacitor, inductor, output capacitor and the MOSFETs should be close to each other as possible. This helps to reduce the EMI radiated by the power loop due to the high switching currents through them.

2. Low ESR capacitor which can handle input RMS ripple current and a high frequency decoupling ceramic cap which usually is 1uF need to be practically touching the drain pin of the upper MOSFET, a plane connection is a must.

3. The output capacitors should be placed as close as to the load as possible and plane connection is required.

4. Drain of the low-side MOSFET and source of the high-side MOSFET need to be connected thru a plane and as close as possible. A snubber needs to be placed as close to this junction as possible.

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5. Source of the lower MOSFET needs to be connected to the GND plane with multiple vias. One is not enough. This is very important. The same applies to the output capacitors and input capacitors.

6. Hdrv and Ldrv pins should be as close to MOSFET gate as possible. The gate traces should be wide and short. A place for gate drv resistors is needed to fine tune noise if needed.

7. Vcc capacitor, BST capacitor or any other bypassing capacitor needs to be placed first around the IC and as close as possible. The capacitor on comp to GND or comp back to FB needs to be place as close to the pin as well as resistor divider.

8. The output sense line which is sensing output back to the resistor divider should not go through high frequency signals, should be kept away from the inductor and other noise sources. The resistor divider must be located as close as possible to the FB pin of the device.

9. All GNDs need to go directly thru via to GND plane.

10. In multilayer PCB, separate power ground and analog ground. These two grounds must be connected together on the PC board layout at a single point. The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function.

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Demoboard Schematic

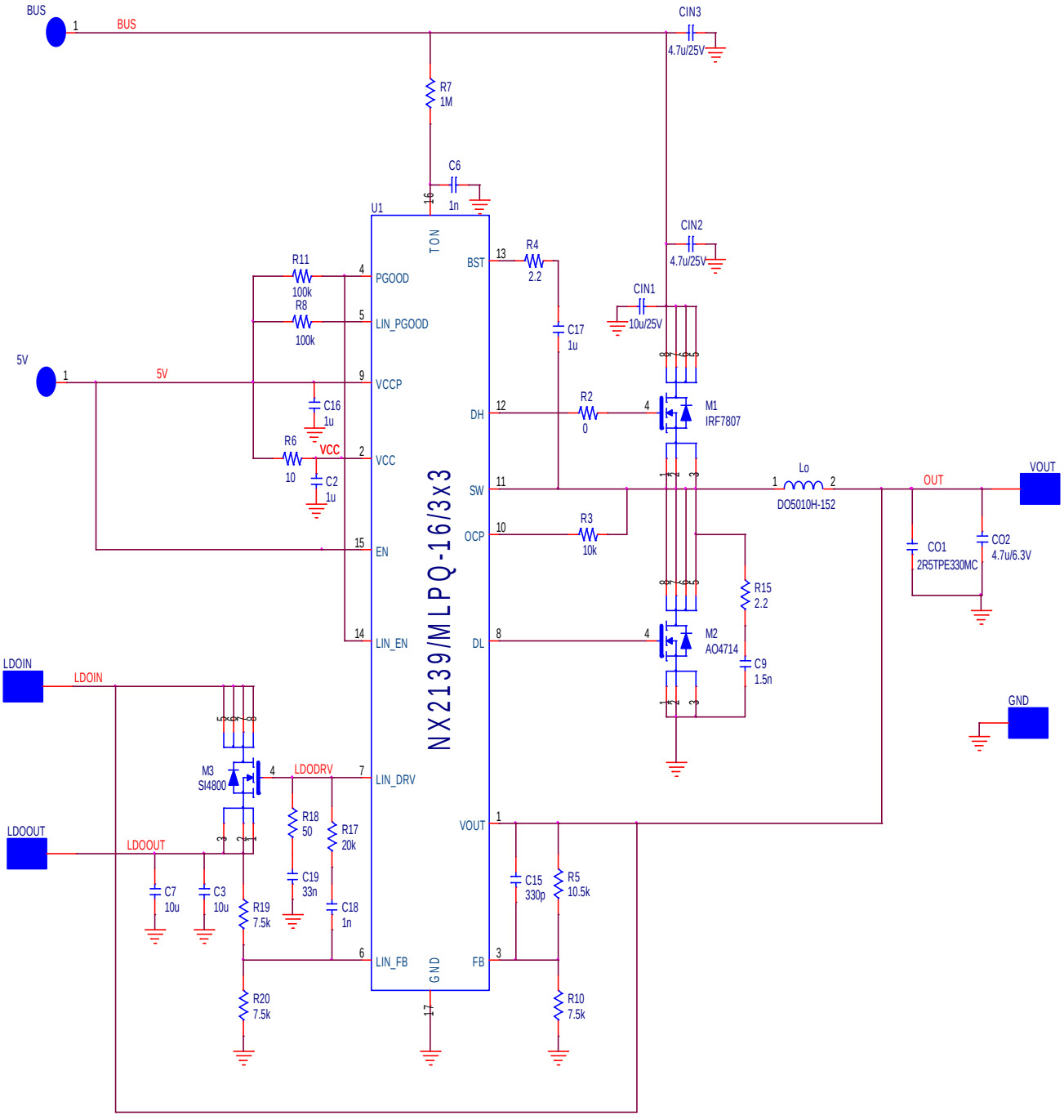

Figure 14 - NX2139A schematic for the demoboard layout

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Demoboard Layout

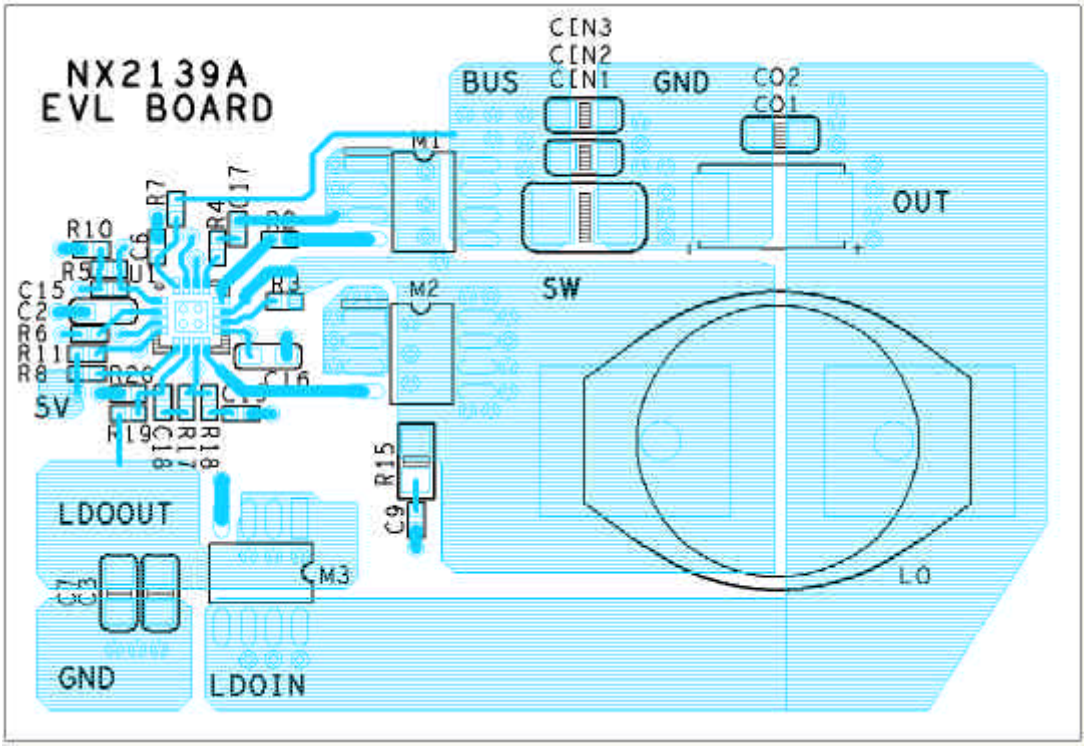

Figure 15 Top layer

Figure 16 Ground layer

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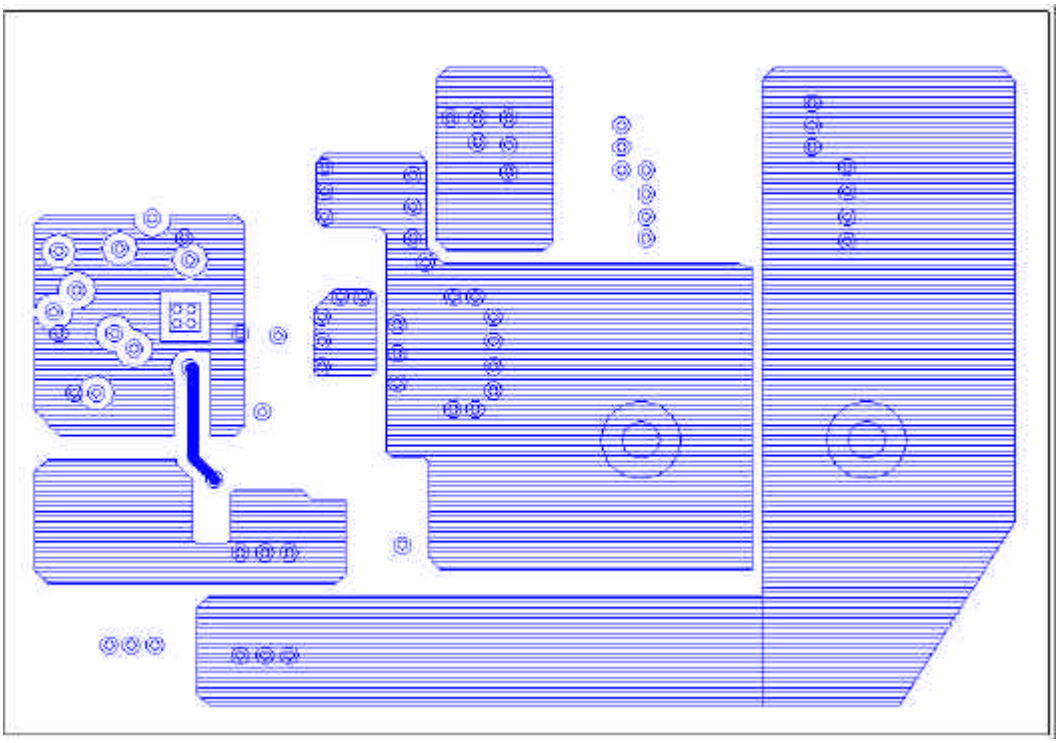

Figure 17 Power layer

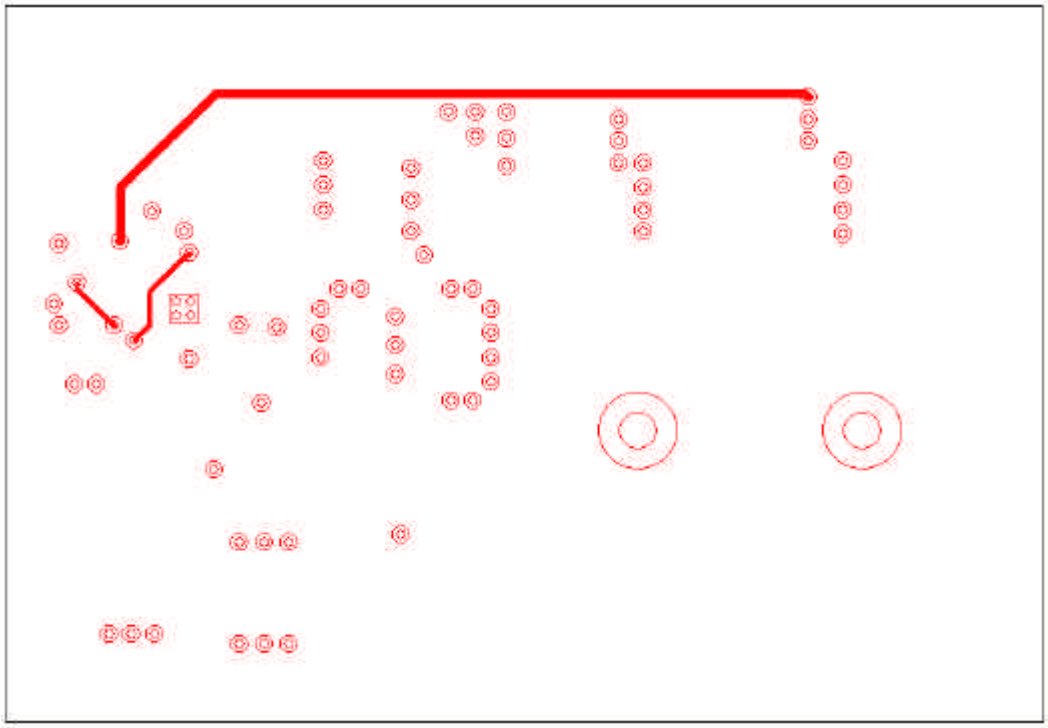

Figure 18 Bottom layer

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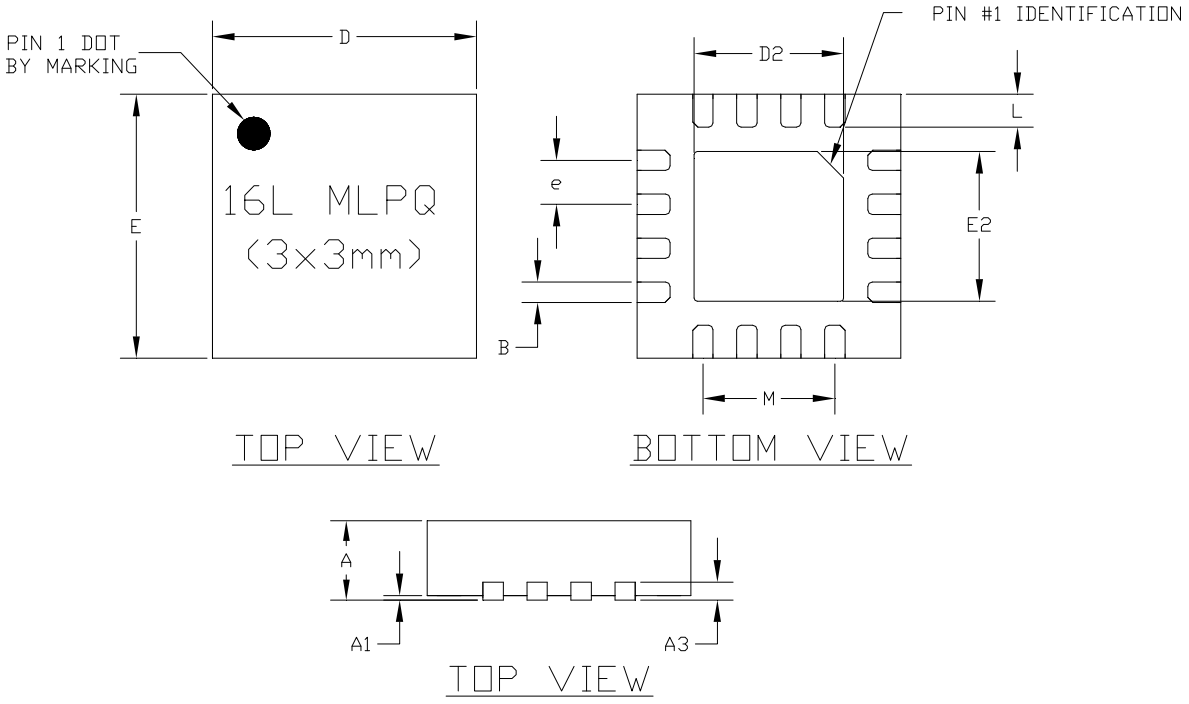
MLPQ 16 PIN 3 x 3 PACKAGE OUTLINE DIMENSIONS



SYMBOL NAME	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF		0.008REF	
B	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	1.600	1.750	0.063	0.069
E	2.950	3.050	0.116	0.120
E2	1.600	1.750	0.063	0.069
e	0.50BSC		0.50BSC	
L	0.325	0.450	0.013	0.018
M	1.5REF		0.059REF	

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