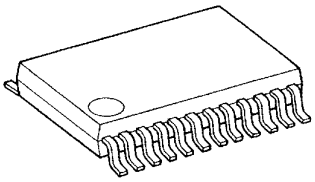
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC9470FN

Σ-Δ Modulation DA Converter with Built-in 8-Times Oversampling Digital Filter/Dynamic Digital Bass Boost/Analog Filter

The TC9470FN is a second-order Σ-Δ modulation system 1-bit DA converter incorporating an 8-times oversampling digital filter, dynamic digital bass boost function for use with compressor operations and an analog filter developed for digital audio equipment.

Because the IC includes an analog filter, it can output a direct analog waveform, thus reducing the size and cost of the DA converter.



SSOP24-P-300-0.65A

Weight: 0.14 g (typ.)

Features

- Built-in 8-times oversampling digital filter
- Low-voltage operations (2.4 V) possible
- Built-in digital de-emphasis filter
- Built-in dynamic digital bass boost function
- In serial control mode, output amplitude can be set in 4096 steps of resolution using microcontroller commands
- In parallel control mode, soft mute can be set for the output signal in 64 steps in 23 ms
- Built-in LR common digital zero detection output circuit
- Sampling frequency: 44.1 kHz
- Supports 384 fs/256 fs (automatic switching)
- DA converter oversampling ratio (OSR): 192 fs (at 384 fs)
- Stereo/monaural output selection possible
- Built-in third-order analog filter
- The digital filter and DA converter characteristics are shown on the next page

Digital Filter

	Digital Filter	Passband Ripple	Transient Bandwidth	Attenuation
Standard operation	8 fs	±0.11dB	20 k to 24.1 kHz	−26dB or less

DA Converter (V_{DD} = 2.7 V)

	OSR	Noise Distortion	S/N Ratio
Standard operation	192 fs	−82dB (typ.)	90dB (typ.)

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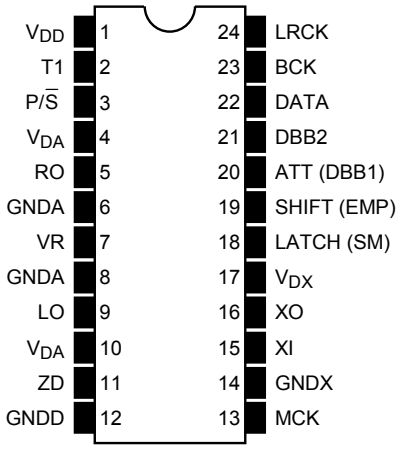
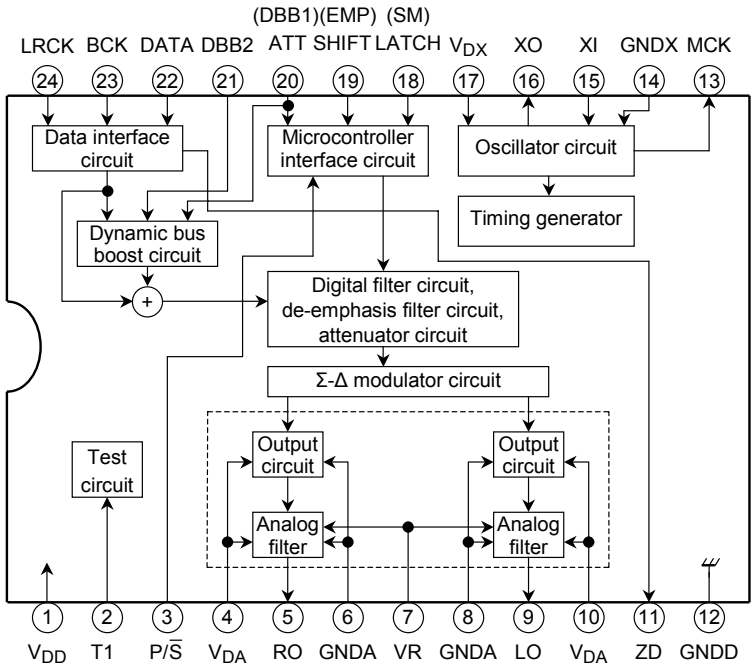
Pin Connection



Block Diagram



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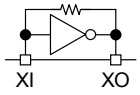
Pin Function

Pin No.	Symbol	I/O	Function	Remarks
1	V_{DD}	—	Digital block power supply pin	
2	T1	I	Test pin. Always set to “Low” level.	
3	P/$\overline{S}$	I	Parallel/serial mode select pin	
4	V_{DA}	—	Analog power supply pin	
5	RO	O	Right channel analog signal output pin	
6	GNDA	—	Analog GND pin	
7	VR	—	Reference voltage pin	
8	GNDA	—	Analog GND pin	
9	LO	O	Left channel analog signal output pin	
10	V_{DA}	—	Analog power supply pin	
11	ZD	O	Zero data detection output pin common to left and right channels	
12	GNDD	—	Digital GND pin	
13	MCK	O	System clock output pin	
14	GNDX	—	Crystal oscillator GND pin	
15	XI	I	Crystal oscillator connecting pins. Generate the clock required by the system.	
16	XO	O		
17	V_{DX}	—	Crystal oscillator power supply pin	
18	LATCH (SM)	I	In serial mode, data latch signal input pin In parallel mode, soft mute control pin	Schmidt input
19	SHIFT (EMP)	I	In serial mode, shift clock input pin In parallel mode, de-emphasis filter control pin	Schmidt input
20	ATT (DBB1)	I	In serial mode, data input pin In parallel mode, dynamic bass boost control pin 1	Schmidt input
21	DBB2	I	In parallel mode, dynamic bass boost control pin 2	
22	DATA	I	Audio data input pin	Schmidt input
23	BCK	I	Bit clock input pin	Schmidt input
24	LRCK	I	LR clock input pin	Schmidt input

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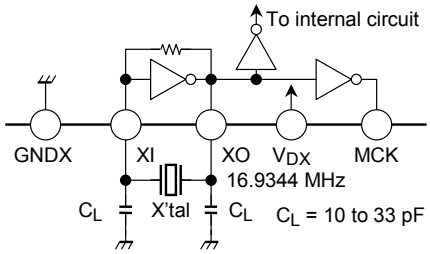
Description of Block Operations

1. Crystal Oscillator Circuit and Timing Generator

The clock required for internal operations is generated by connecting a crystal and condensers as shown in the diagram below.

The IC will also operate when a system clock is input from an external source through the XI pin (pin 15). However, in this situation, due consideration must be given to the fact that waveform characteristics, such as jitter and rising/falling characteristics of the system clock, significantly affect the DA converter's noise distortion and the S/N ratio.



Use a crystal with a low CI value and favorable start-up characteristics.

Figure 1 Crystal Oscillator Circuit Configuration (when in the 384 fs mode)

The timing generator generates the clocks and process timing signals required for such functions as digital filtering and de-emphasis filtering.

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2. Data Input Circuit

DATA and the LRCK are loaded to the LSI internal shift registers on the BCK signal rising edge. It is consequently necessary for the DATA and LRCK signals to be synchronized and input on the BCK signal falling edge as indicated in the timing example below. Also, as DATA has been designed so that the 16 bits before the change point of LRCK are regarded as valid data, the data must be input with Right-justified mode when the BCK is 48 fs or 64 fs, as shown in Figure 2a.

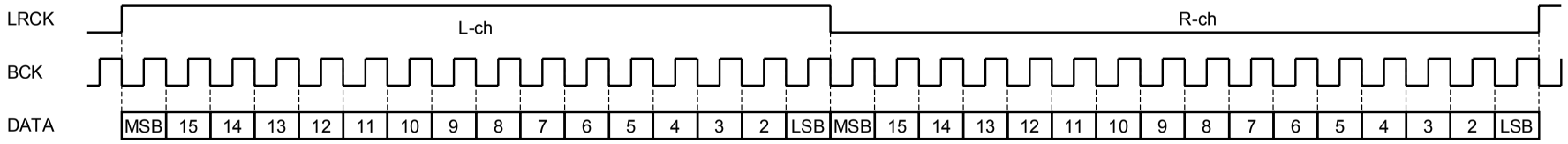

Figure 2a Example of Input Timing Chart

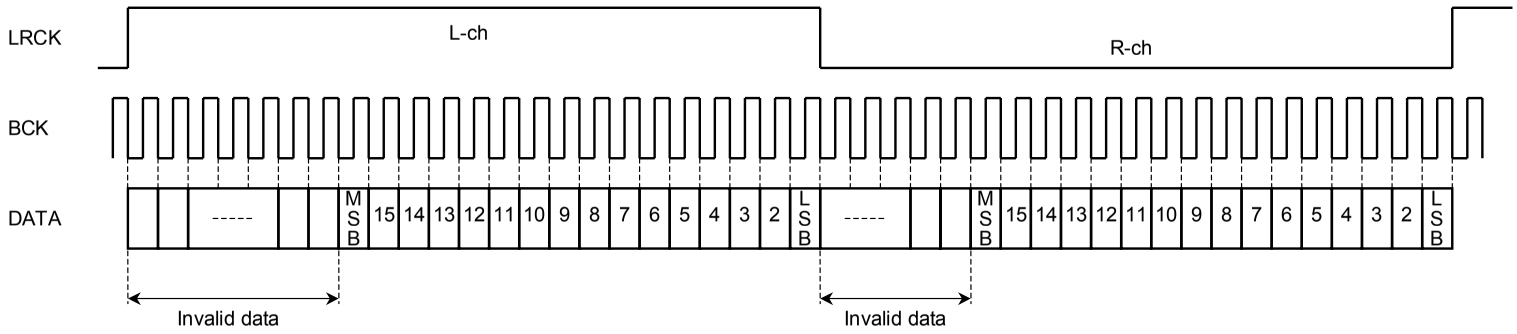

Figure 2b Example of Input Timing Chart

3. Digital Filter

The 8-times oversampling IIR digital filter eliminates the noise returned from outside the bandwidth during standard operations.

Table 1 Basic Characteristics of Digital Filter

Set Mode	Passband Ripple	Transient Bandwidth	Attenuation
Standard operations	±0.11dB	20 k to 24.1 kHz	−26dB or less

The characteristics of the digital filter frequencies are shown below.

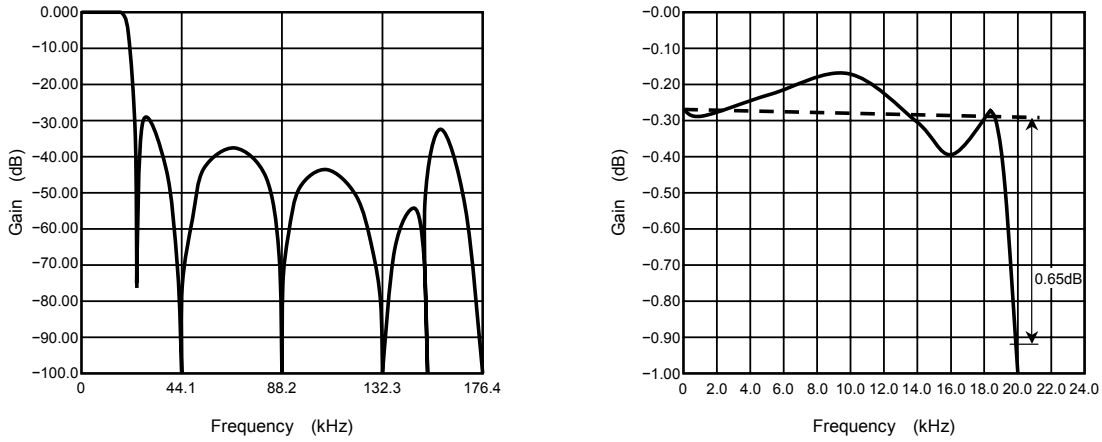

Figure 3 Digital Filter Frequency Characteristics

4. De-Emphasis Filter

ON/OFF is controlled in the parallel mode (P/$\overline{S}$ = "H") with the SHIFT (EMP) pin (pin 19).

This is set in the serial mode (P/$\overline{S}$ = "L") with a microcontroller or other equipment. (refer to 10.2 microcontroller setting mode for further details on serial mode settings.)

Table 2 De-Emphasis Filter Settings (when in the parallel mode)

Shift (EMP) Pin	H	L
De-emphasis filter	ON	OFF

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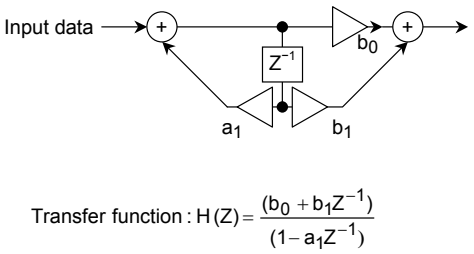
The digitalization of the de-emphasis filter eliminates the need for such external components as resistors, condensers and analog switches. In addition to this, the coefficients are aligned to reduce error in the de-emphasis filter characteristics.

The filter structure and characteristics are shown below.



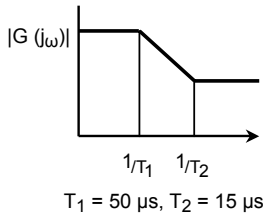


Figure 4 IIR Digital De-Emphasis Filter **Figure 5 Filter Characteristics**

5. Dynamic Digital Bass Boost Circuit

ON/OFF for the dynamic digital bass boost is controlled in the parallel mode ($P/\overline{S}$ = "H") with the DBB1 pin (pin 20) and the DBB2 pin (pin 21).

This is set in the serial mode ($P/\overline{S}$ = "L") with a microcontroller or other equipment. (refer to 10.2 microcontroller setting mode for further details on serial mode settings.)

A block diagram for the dynamic bass boost circuit is shown in Figure 6.

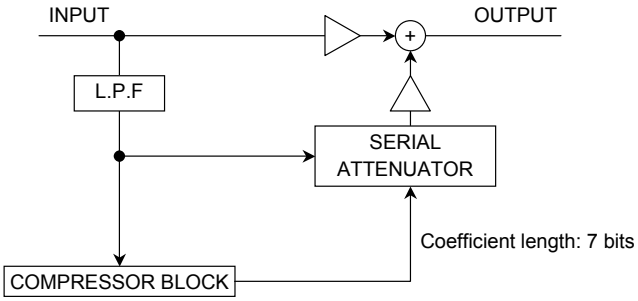


Figure 6 Dynamic Digital Bass Boost Circuit Block

The compressor's compression ratio when in the control mode for the parallel mode is shown below.

Table 3 Compressor Compression Ratio (when in the parallel mode)

DBB max	18dB
DBB MID	12dB

The compressor's compression characteristics are as follows:

Table 4 Compressor Compression Characteristics (when in the parallel mode)

DBB max	−36dB
DBB MID	−24dB

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The compressor I/O characteristics for the dynamic digital bass boost are shown in Figure 7.

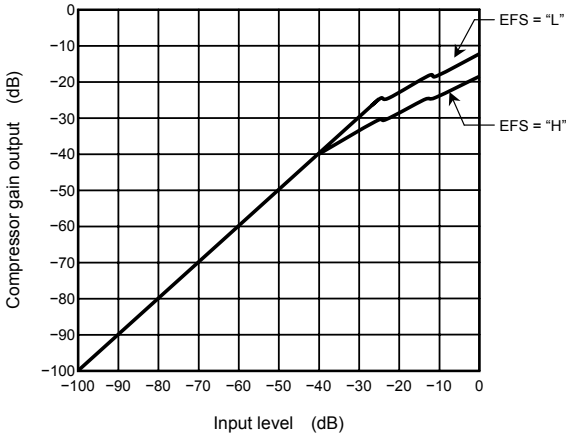

Figure 7 Dynamic Digital Bass Boost Compressor I/O Characteristics

The bass boost settings when in the parallel mode are shown below.

Table 5 Bass Boost Mode Settings

	MODE 1	MODE 2	MODE 3	MODE 4
DBB1 (pin 20)	L	L	H	H
DBB2 (pin 21)	L	H	L	H

MODE 1: DBB OFF
MODE 2: DBB MID
MODE 3: DBB max
MODE 4: DBB max + HB

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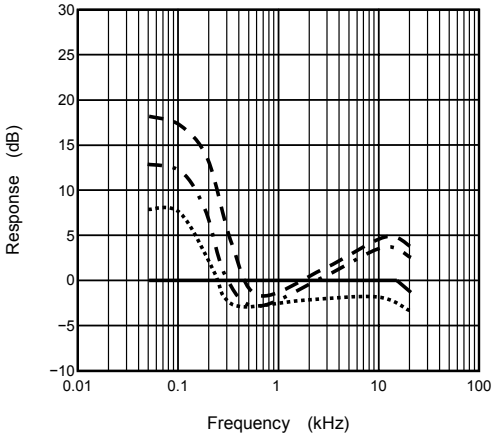
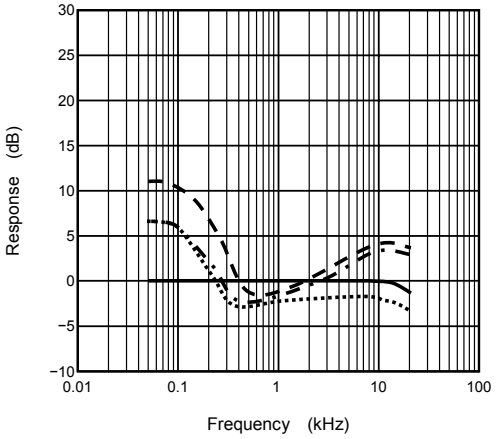
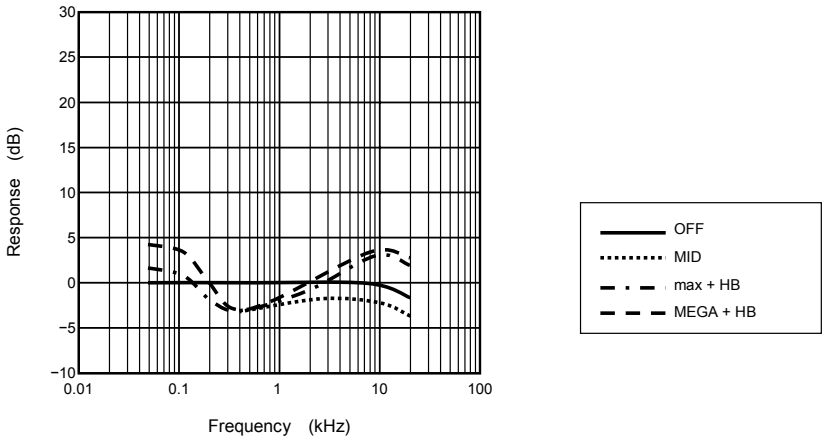
The bus boost characteristics are shown in Figure 8.



a) Vin = −36dB input, DBB OFF, 1 kHz = 0dB.



b) Vin = −20dB input, DBB OFF, 1 kHz = 0dB.
Compressor characteristics
MID: EFS = "L" (−24dB)
max: EFS = "H" (−36dB)
MAGA: EFS = "H" (−36dB)



c) Vin = 0dB input, DBB OFF, 1 kHz = 0dB.
Compressor's compression characteristics
MID: EFS = "L" (−24dB)
max: EFS = "H" (−36dB)
MAGA: EFS = "H" (−36dB)

Figure 8 Dynamic Bass Boost Frequency Characteristics (V_{DD} = 2.7 V)

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6. DA Conversion Circuit

The IC incorporates a second-order Σ-Δ modulation DA converter for two channels (simultaneous output type). The internal structure of this is shown in Figure 9.

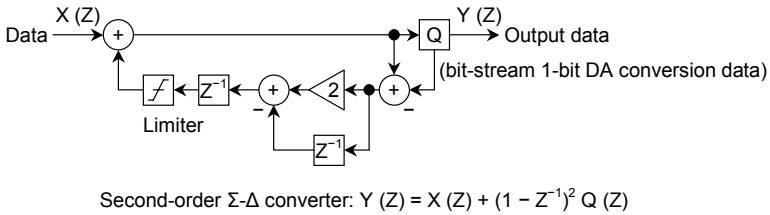

Figure 9 Σ-Δ Modulation DA Converter

The Σ-Δ modulation clock has been designed to operate at 192 fs (when 384 fs). The noise shaping characteristics are shown in Figure 10.

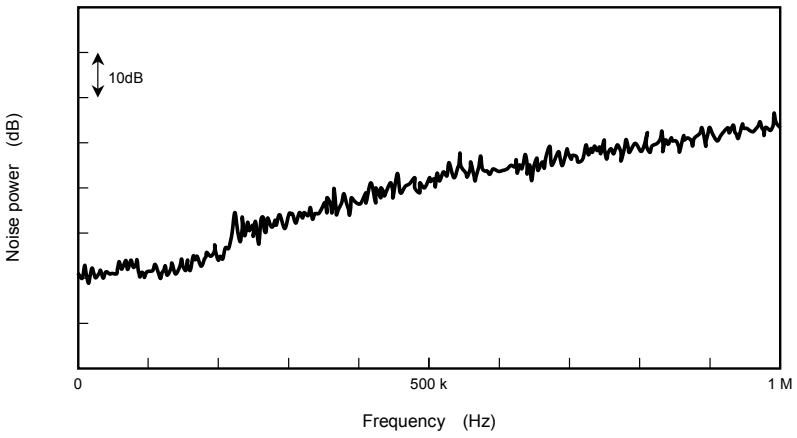

Figure 10 Noise Shaping Characteristics

7. Data Output Circuit

The output circuit is equipped with a third-order analog low-pass filter. This enables direct analog signals to be acquired from the IC's RO (pin 5) and LO (pin 9) output pins.

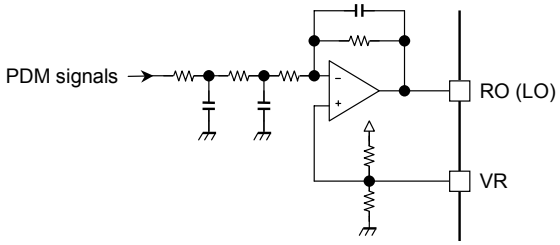

Figure 11 Analog Filter Circuit

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8. Soft Mute Circuit

The IC is equipped with a soft mute function, and this enables a soft mute to be set for the DA converter output by switching the SM pin (pin 18) from the "L" level to the "H" level when in the parallel mode ($P/\overline{S}$ = "H"). The soft mute's ON/OFF function and the DA converter output are shown in Figure 12.

The Soft mute ON/OFF control function is disabled during level transition.

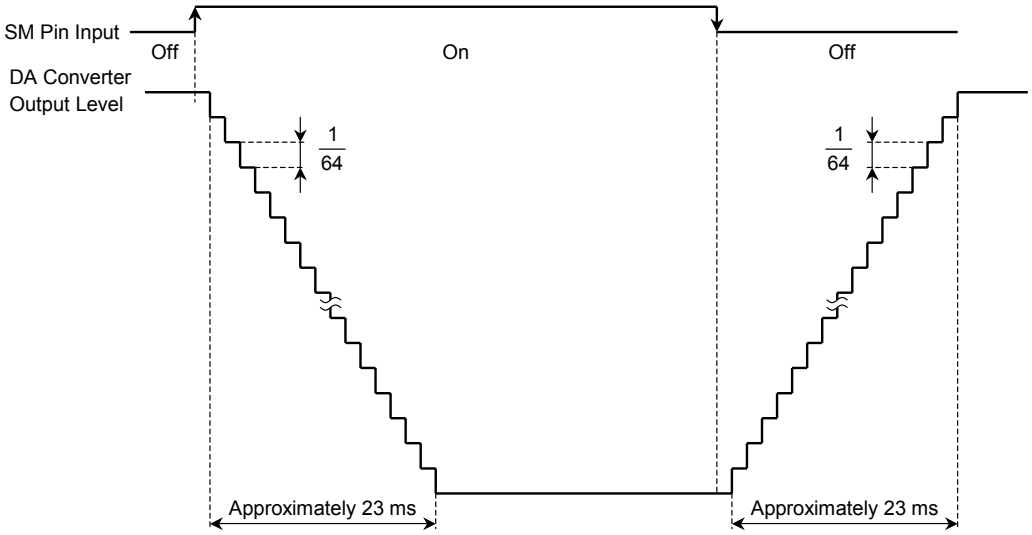

Figure 12 Changes in the Soft Mute DA Converter Output Level

9. Common Left Channel/Right Channel Digital Zero Data Detection Output Circuit

The IC is equipped with a common left channel/right channel digital zero data detection output circuit, and the ZD pin (pin 11) is switched from "L" to "H" when data for both the left channel and the right channel becomes zero data for approximately 350 ms or longer.

This is fixed at "L" when the data for the left channel and right channel is not zero data.

10. Description of Internal Control Signals

The $P/\overline{S}$ pin can be used to switch between the parallel mode ($P/\overline{S}$ pin = "H" in DC setting mode) and the serial mode ($P/\overline{S}$ pin = "L" with the microcontroller interface function).

10.1 Parallel Mode ($P/\overline{S}$ = "H": DC setting mode)

Pins 18, 19, 20 and 21 are used as the mode setting pins shown in the table below when in the parallel mode.

Table 6 Pin Names at the Parallel Mode

Pin No.	Pin Name	Pin Description
18	SM	Soft mute control pin
19	EMP	De-emphasis control pin
20	DBB1	Digital bass boost mode control pin 1
21	DBB2	Digital bass boost mode control pin 2

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10.2 Serial Mode ($P/\overline{S}$ = "L": microcontroller setting mode)

It is possible to make the various settings with a microcontroller when in the serial mode.

Pins 18, 19 and 20 are used as the command input pins shown in the table below when in the serial mode.

Table 7 Pin Names at the Serial Mode

Pin No.	Pin Name	Pin Description
18	LATCH	Data latch signal input pin
19	SHIFT	Shift clock signal input pin
20	ATT	Data input pin

The LATCH signals and ATT signals are loaded to the LSI internal shift registers on the SHIFT signal rising edge. It is consequently necessary for the data input from the ATT pin on the shift signal rising edge to be valid as indicated in the timing example in Figure 13. It is also necessary for the LATCH pulse to rise at least 1.5 μs after the final clock rising edge input from the SHIFT pin. Operating the shift clock with LATCH low destabilizes the internal state, which may lead to malfunctions, so it must therefore be set to the low level after loading D7 to the register.

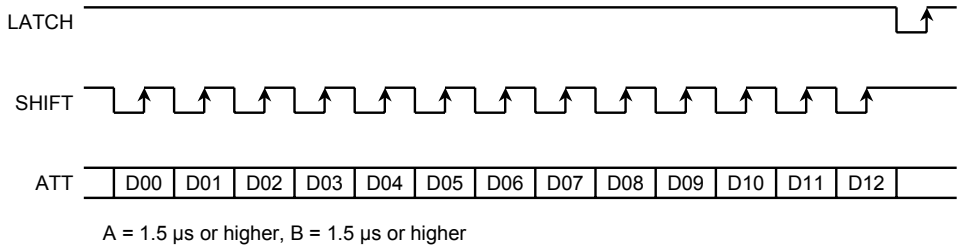

Figure 13 Example of Data Setting Timing in the Serial Mode

The various control settings when in the serial mode are shown in the table below.
Ensure that all control bits are set when the power supply is turned on.

Table 8 Serial Mode Control Settings

Serial Input Data	Control Signals		
	MODE 1	MODE 2	MODE 3
D12	0	1	1
D11	AT11	0	1
D10	AT10	EMP	DBB1
D09	AT09	MONO	DBB2
D08	AT08	CHS	DBB3
D07	AT07	RLS	BMUTE
D06	AT06	EFS	TCA
D05	AT05	DOFF	TCR
D04	AT04	—	—
D03	AT03	—	—
D02	AT02	—	—
D01	AT01	—	—
D00	AT00	—	—

AT11 to AT00: Attenuation level setting
EMP: De-emphasis ON/OFF switch
MONO, CHS: Stereo/monaural switch
RLS: LRCK polarity switch
EFS: Dynamic circuit compression characteristics switch
DOFF: Dynamic circuit ON/OFF switch
DBB1, DBB2: Digtal bass boost mode setting
DBB3: DBB MEGA max setting
BMUTE: Bass boost mute
TCA: Attack time switch
TCR: Recovery time switch

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10.2.1 Setting Mode 1

Serial setting mode 1 is enabled when D12 = "L".

(1) Digital attenuator

The digital attenuation command is enabled when D12 = L. The attenuation data can be set in 4096 different ways (coefficient: 12 bit, maximum attenuation: −72.245dB). The relationship with the command's output is shown below.

Table 9 Attenuation Data/Audio Data Output

Attenuation Data AT [11:00]	Audio Output
FFFH	−0.000dB
FFEH	−0.002dB
FFBH	−0.004dB
...	...
C80H	−2.142dB
...	...
640H	−8.163dB
...	...
002H	−66.224dB
001H	−72.245dB
000H	−∞

001 (HEX) to FFE (HEX): The attenuation value is obtained with the following equation.

ATT = 20 ℓog (input data/4095) dB

Example: When the attenuation data is EA0H

ATT = 20 ℓog (4000/4095) dB = −0.204dB

If an input level is set to −48dB or less when it is set as the amount (−72.245dB) of the maximum attenuation, the target effective attenuation data of digital attenuator of TC9470FN will be lost. The output data is set to "0" when an input level is set to −48dB or less. An effective input level is decided by the following formula.

Effective input data = −[120dB + Attenuation level (dB)]

10.2.2 Setting Mode 2

Serial setting mode 2 is enabled when D12 = "H" and D11 = "L".

(1) Digital de-emphasis filter

Controlled with EMP.

Table 10 Digital De-Emphasis Filter Setting

EMP	L	H
De-emphasis filter	OFF	ON

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(2) Stereo/monaural output channel settings
Set with MONO and CHS.

Table 11 Stereo, Monaural and Channel Select Settings

MONO	L	H	H
CHS	(Note)	L	H
L, R-ch output	Stereo output	L-ch monaural output	R-ch monaural output

Note: "H" or "L"

(3) LRCH (channel clock) polarity switch settings
Set with RLS.

Table 12 LRCK Polarity Switch Settings

RLS	L	H
Data input	R-ch data when LRCK = "L"	L-ch data when LRCK = "L"

(4) Compressor's compression characteristics switch settings
Set with EFS.

Table 13 Compressor Compression Characteristics (compression ratio) Settings

EFS	L	H
Compressor's compression characteristics	−24dB	−36dB
Compressor compression ratio	12dB	18dB

Compressor's compression characteristics and compression ratio are shown in Figure 7.

(5) Dynamic circuit ON/OFF switch settings
Set with DOFF.

Table 14 Dynamic Circuit ON/OFF Switch Settings

DOFF	L	H
Dynamic circuit	ON	OFF

The dynamic circuit's ON/OFF switch settings become invalid when DBB3 is set to "H" in the following mode 2 settings. The amount of boost when the dynamic circuit is OFF is shown in table 15.

Table 15 Amount of Boost when the Dynamic Circuit is OFF

	Amount of Boost
MID	10.6dB
max	15.2dB

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10.2.3 Setting Mode 3

Serial setting mode 3 is enabled when D7 = "H" and D6 = "H".

(1) Digital bass boost mode settings

Set with DBB1, DBB2 and DBB3.

Table 16 Bass Boost Mode Settings

	MODE 1	MODE 2	MODE 3	MODE 4
DBB1	L	L	H	H
DBB2	L	H	L	H
DBB3	L or H	L or H	L or H	L or H

The DBB3 settings are as follows.

DBB3 = "L"	DBB3 = "H"
MODE 1: DBB OFF	MODE 1': DBB OFF
MODE 2: DBB MID	MODE 2': DBB max
MODE 3: DBB max	MODE 3': DBB MEGA max
MODE 4: DBB max + HB	MODE 4': DBB MEGA max + HB

(2) Bass boost mute setting

Set with BMUTE. The bass boost mute to be set for bass boost signal by switching the BMUTE from the "L" level to the "H" level.

Table 17 Bass Boost Mute Setting

BMUTE	L	H
Bass boost mute	OFF	ON

Time constant of bass boost mute: Approximately 3.8 ms

(3) Attack time/recovery time switch settings

Set with TCA for attack time and TCR for recovery time.

Table 18 Attack Time Settings

TCA	L	H
Attack time	6.3 ms	24.3 ms

Table 19 Recovery Time Settings

TCA	L	H
Recovery time	12.3 s	24.6 s

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Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{DD}	−0.3 to 6.0	V
	V_{DA}	−0.3 to 6.0	
	V_{DX}	−0.3 to 6.0	
Input voltage	V_{in}	−0.3 to V_{DD} + 0.3	V
Power dissipation	P_D	200	mW
Operating temperature	T_{opr}	−15 to 50	°C
Storage temperature	T_{stg}	−55 to 150	°C

Electrical Characteristics
(unless otherwise specified, Ta = 25°C, V_{DD} = V_{DX} = V_{DA} = 2.7 V)

DC Characteristics

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Operating power supply voltage		V_{DD}	—	Ta = −15 to 50°C	2.4	2.7	3.5	V
		V_{DX}			2.4	2.7	3.5	
		V_{DA}			2.4	2.7	3.5	
Current consumption		I_{DD}	—	XI = 16.9344 MHz V_{DD} = V_{DX} = 2.4 V	—	4.0	5.5	mA
Input voltage	"H" level	V_{IH}	—		V_{DD} × 0.7	—	V_{DD}	V
	"L" level	V_{IL}			0	—	V_{DD} × 0.3	
Input current	"H" level	I_{IH}	—		−10	—	10	μA
	"L" level	I_{IL}						

AC Characteristics (oversampling ratio = 192 fs)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Noise distortion	THD + N	1	1 kHz sine wave, full-scale input V_{DD} = V_{DX} = V_{DA} = 2.7 V	—	−82	−77	dB
S/N ratio	S/N	1	V_{DD} = V_{DX} = V_{DA} = 2.7 V	85	90	—	dB
Dynamic range	DR	1	1 kHz sine wave, −60dB input conversion	85	90	—	dB
Crosstalk	CT	1	1 kHz sine wave, full-scale input	—	−90	−80	dB
Analog output level	Aout	1	1 kHz sine wave, full-scale input V_{DD} = V_{DX} = V_{DA} = 2.7 V	—	685	—	mV_{rms}
Operating frequency	f_{opr}	—	V_{DD} = V_{DX} = V_{DA} ≥ 2.4 V	11	16.9344	—	MHz
Input frequency	f_{LR}	—	LRCK duty cycle = 50%	—	44.1	—	kHz
	f_{BCK}		BCK duty cycle = 50%	1.4	2.1168	2.9	MHz
Rise time	t_r	—	LRCK, BCK pins (10% to 90%)	—	—	15	ns
Fall time	t_f	—		—	—	15	ns
Delay time	t_d	—	BCK ↓ edge → LRCK, DATA	—	—	50	ns

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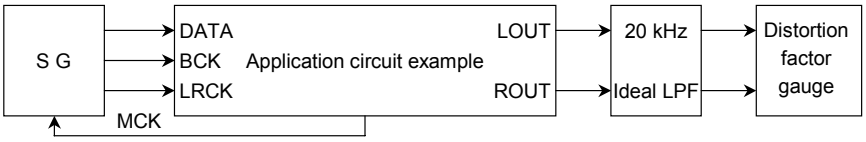
- Test circuit 1: With the use of a sample application circuit

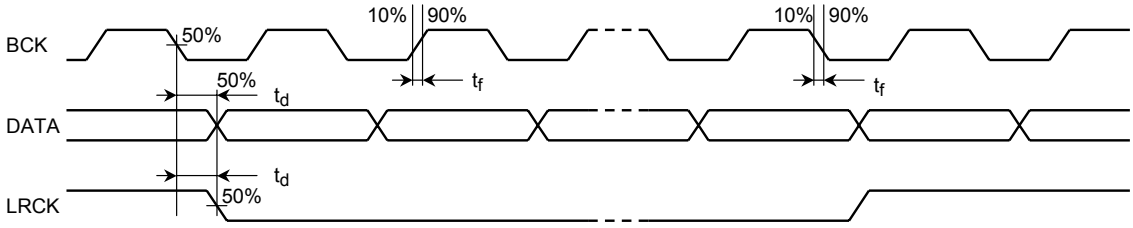


SG: Anritsu: MG-22A or equivalent
LPF: Shibasoku: Built-in 725C distortion factor gauge filter
Distortion: Shibasoku: 725C or equivalent

Parameter Measured	Distortion Factor Gauge Filter Setting A Weight
THD + N, CT	OFF
S/N, DR	ON

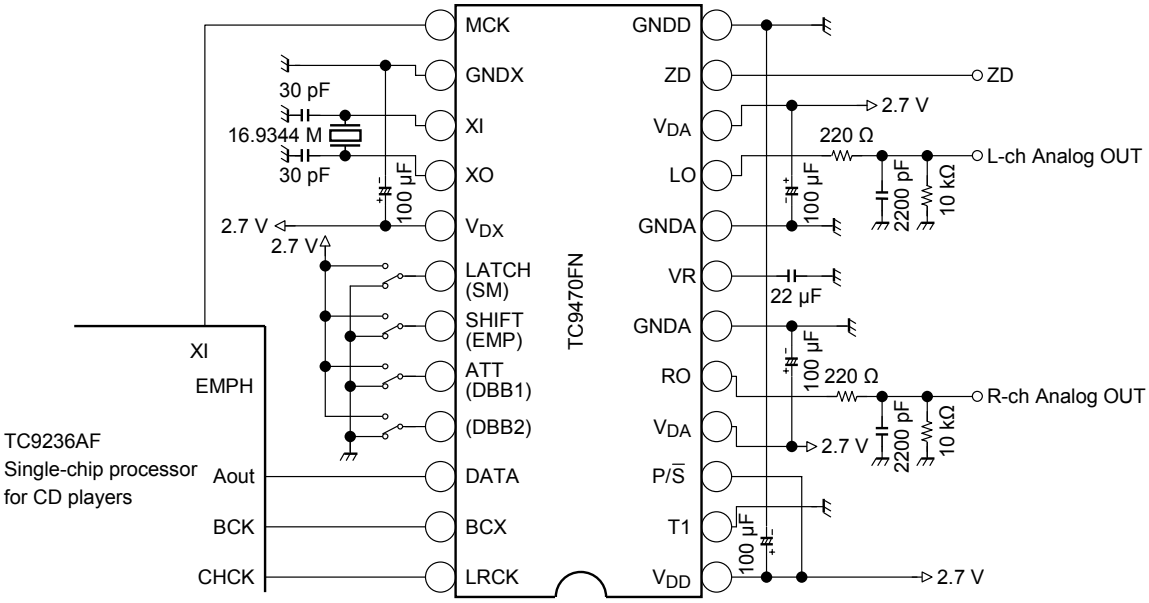
A weight: IEC-A or equivalent

- AC characteristics stipulated point (input signal stipulation: LRCK, BCK, DATA)



Application Circuit

The following diagram is for reference purposes only and does not guarantee operations.



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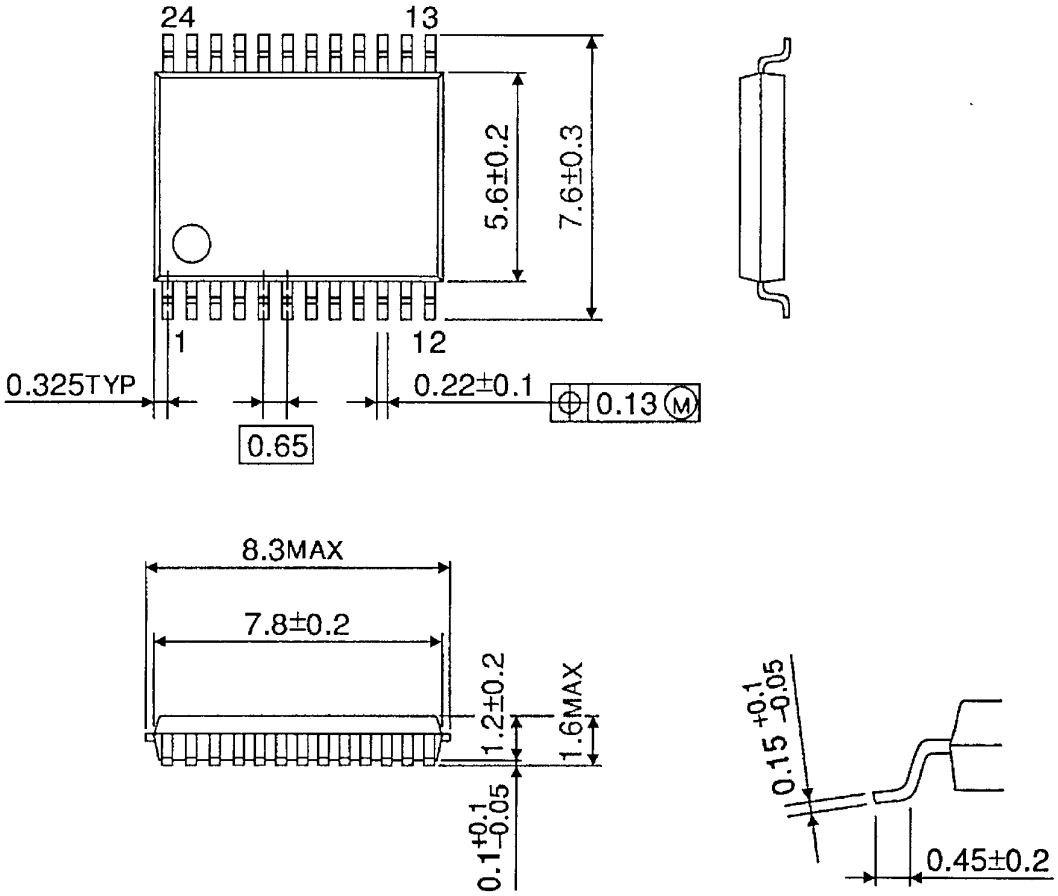
Package Dimensions

SSOP24-P-300-0.65A Unit : mm



Weight: 0.14 g (typ.)

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000707EBA

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