

# TC9465F

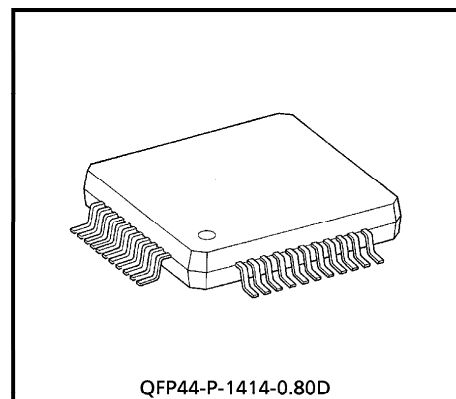
## SINGLE CHIP KARAOKE LSI

This IC is single chip KARAOKE LSI for LD/CD player, Mini compo, VTR.

As built-in ADC/DAC, Sound Field Control and bass treble (DSP effect), Mic echo, and Vocal cancel, this IC constructs KARAOKE function.

### FEATURES

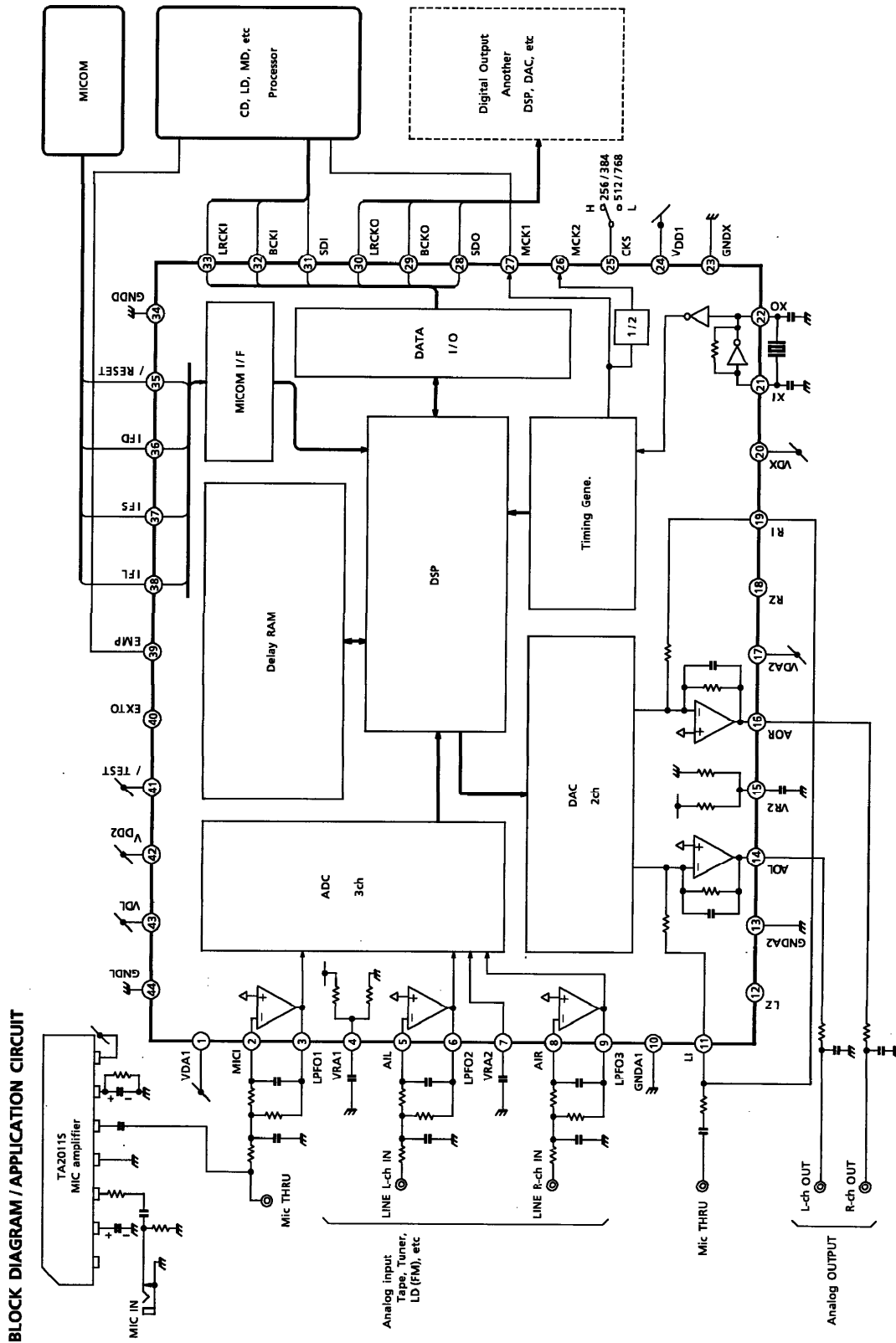
- Built-in 3channel AD converter.  
THD : -65dB S/N : 78dB (typ.)  
Built-in Ope Amp for Pre-filter.
- Built-in 2channel DA converter.  
THD : -85dB S/N : 93dB (typ.)  
Built-in 3rd Analog filter.
- Input : 3 Analog channel, 1 Digital stereo port.  
Digital Input format : MSB first 16, 18, 20bit effective data before change point of LRCK or I<sup>2</sup>S.
- Output : 2 Analog Output / 1 Digital stereo port.  
Digital Output format : MSB first 16, 20bit effective data before change point of LRCK or I<sup>2</sup>S.
- Built-in 64Kbit delay RAM.
- KARAOKE function
  - Mic echo or Sound field control : Delay time variable.
  - Vocal cancel : suppress vocal signal from stereo source.
  - Double Audio source : Digital input and Analog input (addition L-ch and R-ch)
  - Vocal change : According to Mic signal input or not input, effective vocal cancel or not effective vocal cancel.
  - Bass treble
- Package is QFP 44pins.



Weight : 1.07g (Typ.)

980910EBA1

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TC9465F-2

## TERMINAL DESCRIPTION

| No. | TERMINAL | I/O | FUNCTION  | REMARK           |
|-----|----------|-----|---|------------------|
| 1   | VDA1     | —   | ADC Voltage supply terminal.  |                  |
| 2   | MICI     | I   | MIC LPF input terminal.   |                  |
| 3   | LPFO1    | O   | MIC LPF output terminal.  |                  |
| 4   | VRA1     | —   | ADC reference voltage terminal.                                       |                  |
| 5   | AIL      | I   | LPF input terminal for L-ch Line input.                               |                  |
| 6   | LPFO2    | O   | LPF output terminal for L-ch Line input.                              |                  |
| 7   | VRA2     | —   | ADC reference voltage terminal.                                       |                  |
| 8   | AIR      | I   | LPF input terminal for R-ch Line input.                               |                  |
| 9   | LPFO3    | O   | LPF output terminal for L-ch Line input.                              |                  |
| 10  | GND A1   | —   | ADC GND terminal.   |                  |
| 11  | LI       | I   | L-ch Analog additional input terminal.<br>(When not using : OPEN)     |                  |
| 12  | LZ       | O   | L-ch Digital input 0 detect terminal.                                 |                  |
| 13  | GND A2   | —   | DAC GND terminal.   |                  |
| 14  | AOL      | O   | L-ch DAC output terminal.   |                  |
| 15  | VR2      | —   | DAC reference voltage terminal.                                       |                  |
| 16  | AOR      | O   | R-ch DAC output terminal.   |                  |
| 17  | VDA2     | —   | DAC voltage supply terminal.  |                  |
| 18  | RZ       | O   | R-ch Digital input 0 detect terminal.                                 |                  |
| 19  | RI       | I   | R-ch Analog additional input terminal.<br>(When not using : OPEN)     |                  |
| 20  | VDX      | —   | Crystal oscillator voltage supply terminal.                           |                  |
| 21  | XI       | I   | Crystal oscillator connection terminal.<br>(256, 384, 512, 768fs)     |                  |
| 22  | XO       | O   | Crystal oscillator connection terminal.                               |                  |
| 23  | GND X    | —   | Crystal oscillator GND terminal.                                      |                  |
| 24  | VDD1     | —   | Digital voltage supply terminal.                                      |                  |
| 25  | CKS      | I   | Master clock select terminal.<br>(H : 256/384fs, L : 512/768fs)       |                  |
| 26  | MCK2     | O   | 1/2 divider clock output terminal.                                    |                  |
| 27  | MCK1     | O   | Oscillator clock output terminal.                                     |                  |
| 28  | SDO      | O   | Digital Audio Data output terminal.                                   |                  |
| 29  | BCKO     | O   | Bit clock output terminal.  |                  |
| 30  | LRCKO    | O   | Channel clock output terminal.  |                  |
| 31  | SDI      | I   | Digital Audio Data input terminal.                                    |                  |
| 32  | BCKI     | I   | Bit clock input terminal.   |                  |
| 33  | LRCKI    | I   | Channel clock input terminal.   |                  |
| 34  | GND D    | —   | Digital GND terminal.   |                  |
| 35  | RESET    | I   | Reset terminal. ("L" Reset active)                                    | pull-up resistor |
| 36  | IFD      | I   | $\mu$ -COM I/F data input terminal.                                   |                  |
| 37  | IFS      | I   | $\mu$ -COM I/F data shift clock input terminal.                       |                  |
| 38  | IFL      | I   | $\mu$ -COM I/F latch pulse input terminal.                            |                  |
| 39  | EMP      | I   | De-emphasis filter setting terminal.<br>("H" : De-emphasis filter ON) |                  |

| No. | TERMINAL                 | I/O | FUNCTION                                  | REMARK           |
|-----|--------------------------|-----|---|------------------|
| 40  | EXTO                     | O   | Extend output terminal.                   |                  |
| 41  | $\overline{\text{TEST}}$ | I   | Test terminal. Usually "H"                | pull-up resistor |
| 42  | V <sub>DD2</sub>         | —   | Digital Voltage supply terminal.          |                  |
| 43  | V <sub>DL</sub>          | —   | Digital Voltage supply terminal for DRAM. |                  |
| 44  | GNDL                     | —   | Digital GND terminal for DRAM.            |                  |

## Block operating description

### 1. Operating Clock

Master clock (Input or oscillating XI terminal) is 768 / 512 / 384 / 256fs. These mode are selected by CKS terminal, and 256fs or 384fs, 768fs or 512fs select is auto detect by this IC.

But following internal synchronize mode can not use 384 / 768fs, can only use 256 / 512fs.

And DSP calculate steps don't concern master clock, but DA converter operating clock change by master clock. DAC is  $\Sigma\text{-}\Delta$  modulation method and operates oversampling, If 256fs is selected, Oversampling ratio is 128fs and so became worse S/N, THD + N.

Table.1-1 Master clock select and DAC oversampling ratio.

| CKS | MASTER CLOCK | DAC OVERSAMPLING RATIO |
|-----|--------------|------------------------|
| L   | 768fs        | 192fs                  |
|     | 512fs        | 256fs                  |
| H   | 384fs        | 192fs                  |
|     | 256fs        | 128fs                  |

### 2. Digital Audio Input/Output

#### 2.1 Synchronize mode

Data input/output Bit clock is selected internal synchronize or external synchronize by "SYNM1", "SYNM2". ( $\mu\text{-COM}$  I/F bit)

Table.2-1-1 Synchronize mode and Input/Output Bit clock.

| SYNM2 | SYNM1 | SYNCHRONIZE | BCKI | BCKO      |
|-------|-------|-------------|------|-----------|
| 0     | 0     | internal    | (*)  | 64fs (**) |
| 0     | 1     | external    | 32fs | BCKI      |
| 1     | 0     | external    | 48fs | BCKI      |
| 1     | 1     | external    | 64fs | BCKI      |

(\*) Table 2-2-1 shown.

(\*\*) Internal clock divider.

Input/Output channel clock (LRCKI, LRCKO) data is selected by  $\mu$ -COM I/F. (RLS bit)

Table.2-1-2 Channel clock

| RLS | OPERATE  |
|-----|--|
| 0   | LRCKI, LRCKO : "H" Level, L-ch data input/output |
| 1   | LRCKI, LRCKO : "L" Level, L-ch data input/output |

2.2 Data Input format

Data input format is Table.2-2-1 and Fig.1.

Selecting use IBIT1 and IBIT2. ( $\mu$ -COM I/F)

Table.2-2-1 Data input format

| SYNM2 | SYNM1 | IBIT2 | IBIT1 |                         | FORMAT         | BCKI       |
|-------|-------|-------|-------|-------------------------|----------------|------------|
| 0     | 0     | 0     | 0     | INTERNAL<br>SYNCHRONIZE | MSBfirst 16bit | 32fs~128fs |
| 0     | 0     | 0     | 1     |                         | MSBfirst 18bit | 36fs~128fs |
| 0     | 0     | 1     | 0     |                         | MSBfirst 20bit | 40fs~128fs |
| 0     | 0     | 1     | 1     |                         | IIS MAX20bit   | 64fs only  |
| 0     | 1     | 0     | 0     | EXTERNAL<br>SYNCHRONIZE | MSBfirst 16bit | 32fs       |
| 0     | 1     | 0     | 1     |                         | not use        | 32fs       |
| 0     | 1     | 1     | 0     |                         | not use        | 32fs       |
| 0     | 1     | 1     | 1     |                         | not use        | 32fs       |
| 1     | 0     | 0     | 0     |                         | MSBfirst 16bit | 48fs       |
| 1     | 0     | 0     | 1     |                         | MSBfirst 18bit | 48fs       |
| 1     | 0     | 1     | 0     |                         | MSBfirst 20bit | 48fs       |
| 1     | 0     | 1     | 1     |                         | not use        | 48fs       |
| 1     | 1     | 0     | 0     |                         | MSBfirst 16bit | 64fs       |
| 1     | 1     | 0     | 1     |                         | MSBfirst 18bit | 64fs       |
| 1     | 1     | 1     | 0     |                         | MSBfirst 20bit | 64fs       |
| 1     | 1     | 1     | 1     |                         | IIS MAX20bit   | 64fs       |

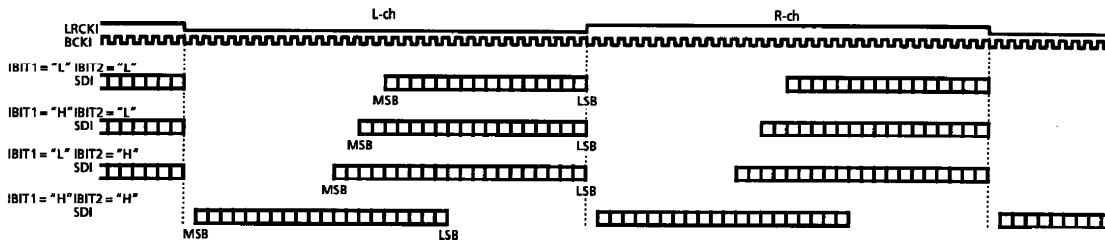


Fig.1 Example Data input timing (RLS = "H", SYNM1 = "H", SYNM2 = "H")

2.3 Digital Zero detect function

Table.2-3-1 Digital Zero detect judge time

| fs         | 32kHz  | 44.1kHz | 48kHz |
|------------|--------|---------|-------|
| Judge Time | 1024ms | 743ms   | 683ms |

2.4 Stereo / Mono setting

This IC can input Double music source by "MONO", "CHS" bit. ( $\mu$ -COM I/F)  
 And this IC can input Double music source by software coefficient, too. Please show Program manual.

Table.2-4-1 Stereo / Mono setting

| MONO | CHS | STEREO / MONO                         |
|------|-----|---------------------------------------|
| 0    | 0   | stereo                                |
| 0    | 1   | ZERO Detect not use ("L" output only) |
| 1    | 0   | L-ch (CH1) MONO OUTPUT                |
| 1    | 1   | R-ch (CH2) MONO OUTPUT                |

2.5 Data output formats

Table.2-5-1 Data Output formats

| SYNM2 | SYNM1 | OBIT2 | OBIT1 |                      | FORMAT         | BCKO          |
|-------|-------|-------|-------|----------------------|----------------|---------------|
| 0     | 0     | 0     | 0     | INTERNAL SYNCHRONIZE | MSBfirst 16bit | 64fs          |
| 0     | 0     | 0     | 1     |                      | MSBfirst 20bit | 64fs          |
| 0     | 0     | 1     | 0     |                      | IIS 16bit      | 64fs          |
| 0     | 0     | 1     | 1     |                      | IIS 20bit      | 64fs          |
| 0     | 1     | 0     | 0     | EXTERNAL SYNCHRONIZE | MSBfirst 16bit | 32fs (= BCKI) |
| 0     | 1     | 0     | 1     |                      | not use        | 32fs (= BCKI) |
| 0     | 1     | 1     | 0     |                      | IIS 16bit      | 32fs (= BCKI) |
| 0     | 1     | 1     | 1     |                      | not use        | 32fs (= BCKI) |
| 1     | 0     | 0     | 0     |                      | MSBfirst 16bit | 48fs (= BCKI) |
| 1     | 0     | 0     | 1     |                      | MSBfirst 20bit | 48fs (= BCKI) |
| 1     | 0     | 1     | 0     |                      | IIS 16bit      | 48fs (= BCKI) |
| 1     | 0     | 1     | 1     |                      | IIS 20bit      | 48fs (= BCKI) |
| 1     | 1     | 0     | 0     |                      | MSBfirst 16bit | 64fs (= BCKI) |
| 1     | 1     | 0     | 1     |                      | MSBfirst 20bit | 64fs (= BCKI) |
| 1     | 1     | 1     | 0     | IIS 16bit            | 64fs (= BCKI)  |               |
| 1     | 1     | 1     | 1     | IIS 20bit            | 64fs (= BCKI)  |               |

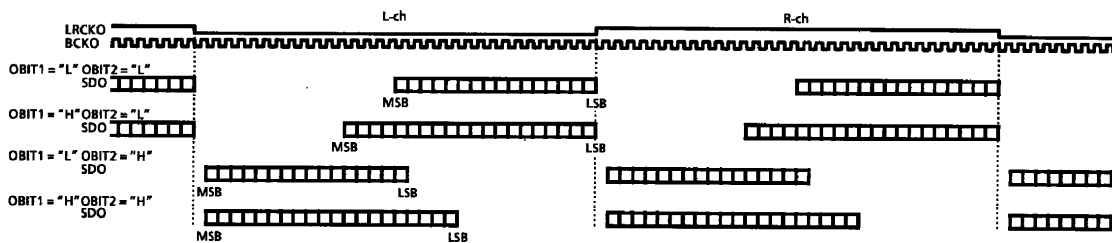


Fig.2 Example Data Output Timing (RL5="H", SYNM1="H", SYNM2="H")

3.  $\mu$ -COM I/F

3.1 Setting

$\mu$ -COM I/F setting is 4 Items.

Command is variable length 16~26bits. (effective data before change point Latch pulse)

When command is 8bits unit, setting is LSB first.

In this case, not using LSB data is not effective.

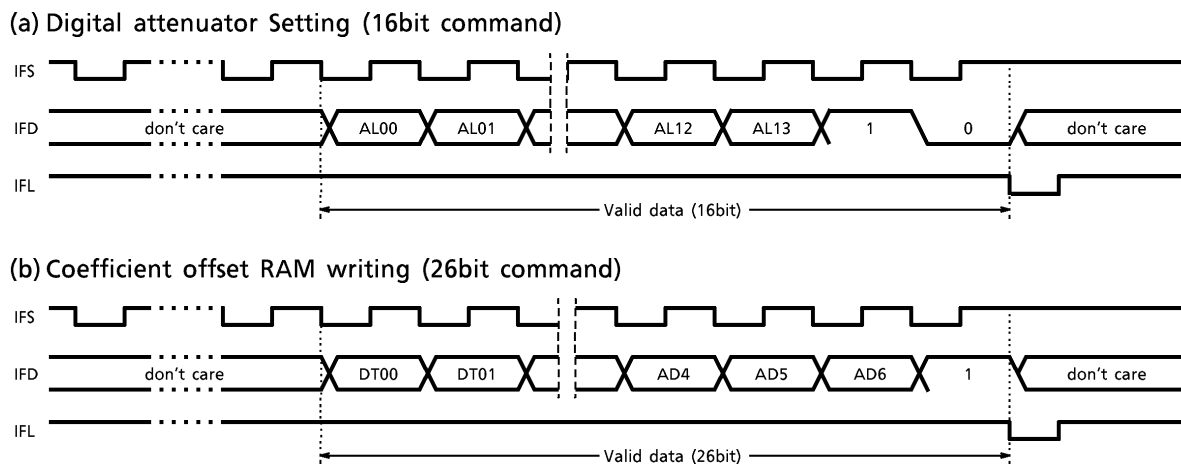
All this IC's setting change at internal program cycle beginning, but without digital attenuator setting, please mute output signal at changing program setting.

So Coefficient setting and offset RAM writing is one word at a fs.

When many word change, please by careful.

Table.3-1-1  $\mu$ -COM I/F setting

|     | MODE  | FUNC. | ATT. | CRAM |       |
|-----|-------|-------|------|------|-------|
| D25 | 0     | 0     | 0    | 1    |       |
| D24 | 0     | 0     | 1    | AD6  |       |
| D23 | 1     | 1     | AL13 | AD5  |       |
| D22 | 0     | 1     | AL12 | AD4  |       |
| D21 | CHS   | EMS   | AL11 | AD3  |       |
| D20 | MONO  | EM2   | AL10 | AD2  |       |
| D19 | OBIT2 | EM1   | AL09 | AD1  |       |
| D18 | OBIT1 | CEF2  | AL08 | AD0  | 1byte |
| D17 | IBIT2 | CEF1  | AL07 | DT17 |       |
| D16 | IBIT1 | CTDW  | AL06 | DT16 |       |
| D15 | SYNM2 | CTUP  | AL05 | DT15 |       |
| D14 | SYNM1 | MUTE  | AL04 | DT14 |       |
| D13 | RL5   | EXT0  | AL03 | DT13 |       |
| D12 | LSM   | VCS   | AL02 | DT12 |       |
| D11 | ADLIM | DF2   | AL01 | DT11 |       |
| D10 | ADPD  | DF1   | AL00 | DT10 | 2byte |
| D09 | --    | --    | --   | DT09 |       |
| D08 | --    | --    | --   | DT08 |       |
| D07 | --    | --    | --   | DT07 |       |
| D06 | --    | --    | --   | DT06 |       |
| D05 | --    | --    | --   | DT05 |       |
| D04 | --    | --    | --   | DT04 |       |
| D03 | --    | --    | --   | DT03 |       |
| D02 | --    | --    | --   | DT02 | 3byte |
| D01 | --    | --    | --   | DT01 |       |
| D00 | --    | --    | --   | DT00 |       |

Fig.3 Example  $\mu$ -COM I/F

### 3.2 Operating mode setting [MODE]

Please set these mode at voltage supply.

When  $\overline{\text{RESET}}$  is "L", these data is clear.

- ADPD : ADC power down (H : power down)
- ADLIM : "L"
- LSM : Digital Attenuator soft mute time select (H : twice)
- RLS : Channel clock select (H : LRCK = "L" is L-ch data)
- SYNM1, 2 : DATA input/output synchronize clock select
- IBIT1, 2 : Input DATA format select
- OBIT1, 2 : Output DATA format select
- MONO : MONO DATA input select
- CHS : At MONO Setting, channel select, At stereo setting, zero detect setting



3.3 DSP setting [FUNC]

At  $\overline{\text{RESET}}$  terminal is "L" level, these data is clear.

- DF1, 2 : SFC, Mic echo desimention ratio select
- VCS : Vocal cancel characteristic select
- EXTO : Expand output terminal OUTPUT DATA
- MUTE : OUTPUT mute ("H" : mute, ATT setting is hold)
- CTUP : Vocal change attack time select
- CTDW : Vocal change release time select
- CEF1 : "L"
- CEF2 : Vocal change effect select
- EM1, 2 : De-emphasis filter select
- EMS : De-emphasis filter block select

Table.3-4-1 De-emphasis setting

| TERMINAL | I / F SETTING |     |     | FUNCTION              |
|----------|---------------|-----|-----|-----------------------|
| EMP      | EMS           | EM2 | EM1 |                       |
| 0        | 0             | —   | —   | OFF                   |
| 1        | 0             | 0   | 0   | de-emphasis 1 44.1kHz |
| 1        | 0             | 0   | 1   | OFF                   |
| 1        | 0             | 1   | 0   | de-emphasis 1 48kHz   |
| 1        | 0             | 1   | 1   | de-emphasis 1 32kHz   |
| 0        | 1             | —   | —   | OFF                   |
| 1        | 1             | 0   | 0   | de-emphasis 2 44.1kHz |
| 1        | 1             | 0   | 1   | OFF                   |
| 1        | 1             | 1   | 0   | de-emphasis 2 48kHz   |
| 1        | 1             | 1   | 1   | de-emphasis 2 32kHz   |

3.4 Digital Attenuator Setting [ATT]

Table.3-5-1 Digital Attenuator level setting

| AL [13 : 00] | OUTPUT LEVEL |
|--------------|--------------|
| 3FFFH        | - 0.00dB     |
| 3FFDH        | - 0.001dB    |
| 3FFBH        | - 0.002dB    |
| ...          | ...          |
| 2D4EH        | - 3.00dB     |
| ...          | ...          |
| 2013H        | - 6.00dB     |
| ...          | ...          |
| 0002H        | - 78.268dB   |
| 0001H        | - 84.288dB   |
| 0000H        | - ∞ dB       |

[Level setting]

$$AL [13 : 00] = 3FFFH * 10^{(LEVEL / 20)}$$

Table.3-5-2 Digital Attenuator mute time

| LSM | 32kHz | 44.1kHz | 48kHz |
|-----|-------|---------|-------|
| 0   | 32ms  | 23ms    | 21ms  |
| 1   | 64ms  | 46ms    | 42ms  |

0dB (3FFFH) ~ - ∞ dB (0000H) Changing Time

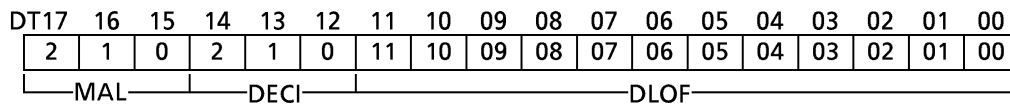
3.5 Coefficient, Offset RAM writing [CRAM]

Coefficient and offset RAM writing operate one word at a fs.

RAM is 128word x 18bit.

Delay RAM Address offset data format is as follows.

Detail setting, please show soft ware manual.



MAL [2 : 0] : Delay RAM setting select

DECI [2 : 0] : Decimation ratio select

DLOF [11 : 00] : Offset Address select

Fig.4 Coefficient, Offset RAM, Offset Address Setting

4. AD converter

Built-in Line input L-ch and R-ch AD converter, and Mic signal input AD converter.  
 Mic input signal convert Digital signal and DSP make digital echo signal.  
 Mic signal add this echo signal by LI, RI terminal or external Op-amp.  
 It is necessary to open LI and RI terminal at the using Op-amp. When not using AD converter,  
 please short circuit interval each terminal MICI-LPFO1, AIL-LPFO2 and AIR-LPFO3.

5. DA converter

This is  $\Sigma$ - $\Delta$  modulation 1bit DA converter.  
 Built-in 3'rd Analog Filter.  
 It is possible to add analog through signal (LI and RI Terminal) at the output portion of DAC.

6. Timing

6.1 Reset Timing

At power supply, please set  $\overline{\text{RESET}}$  terminal "L" level at one time.  
 Power ON Reset Timing is as follows.

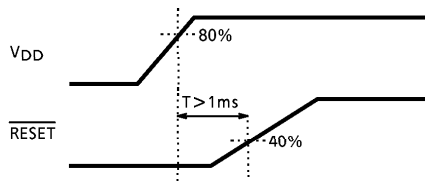
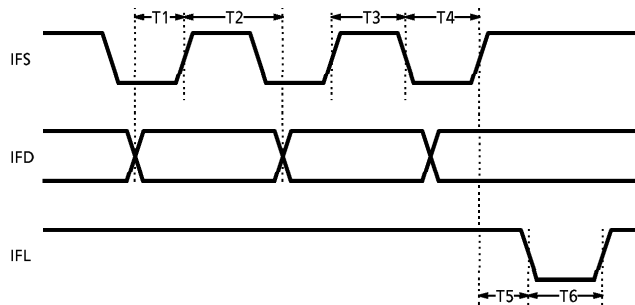


Fig.5 Power on Reset Timing

6.2  $\mu$ -COM I/F Timing



- T1 : Setup time > 1 $\mu$ s
- T2 : Hold time > 1 $\mu$ s
- T3, T4, T6 : Clock pulse width > 1 $\mu$ s
- T5 : Hold time > 1 $\mu$ s

Fig.6  $\mu$ -COM I/F Timing

## MAXIMUM RATINGS

| CHARACTERISTIC        | SYMBOL    | RATING               | UNIT |
|-----------------------|-----------|----------------------|------|
| Supply Voltage        | $V_{DD}$  | -0.3~6.0             | V    |
| Input Voltage         | $V_{in}$  | -0.3~ $V_{DD} + 0.3$ | V    |
| Power Dissipation     | $P_D$     | 500                  | mW   |
| Operating Temperature | $T_{opr}$ | -40~85               | °C   |
| Storage Temperature   | $T_{stg}$ | -55~150              | °C   |

## ELECTRICAL CHARACTERISTICS (DC)

| CHARACTERISTIC           | SYMBOL    | TEST CIR-CUIT | TEST CONDITION                         | MIN.                | TYP. | MAX.                | UNIT          |
|--------------------------|-----------|---------------|--|---------------------|------|---------------------|---------------|
| Operating Supply Voltage | $V_{DD}$  | —             | $T_a = -40\sim 85^\circ\text{C}$       | 4.5                 | 5.0  | 5.5                 | V             |
| Power Supply Current     | $I_{DD}$  | —             | $XI = 16.9\text{MHz}$ , Output No-load | —                   | 48   | 70                  | mA            |
| Input Voltage            | "H" Level | $V_{IH}$      | Digital input terminal                 | $V_{DD} \times 0.8$ | —    | $V_{DD}$            | V             |
|                          | "L" Level | $V_{IL}$      |  | 0                   | —    | $V_{DD} \times 0.2$ |               |
| Input Current            | "H" Level | $I_{IH}$      | Digital input terminal                 | —                   | —    | 1.0                 | $\mu\text{A}$ |
|                          | "L" Level | $I_{IL}$      |  | -1.0                | —    | —                   |               |
| Output Current 1         | "H" Level | $I_{OH1}$     | LRCKO, BCKO, SDO                       | -3.5                | —    | —                   | mA            |
|                          | "L" Level | $I_{OL1}$     |  | —                   | —    | 2.0                 |               |
| Output Current 2         | "H" Level | $I_{OH2}$     | MCK1, MCK2                             | -5.0                | —    | —                   | mA            |
|                          | "L" Level | $I_{OL2}$     |  | —                   | —    | 3.0                 |               |
| Output Current 3         | "H" Level | $I_{OH3}$     | EXTO                                   | -2.0                | —    | —                   | mA            |
|                          | "L" Level | $I_{OL3}$     |  | —                   | —    | 2.0                 |               |
| Pull-up Resistance       | RUP       | —             | RESET, TEST                            | —                   | 50   | —                   | $k\Omega$     |

## ELECTRICAL CHARACTERISTICS (AC)

## AD converter

| CHARACTERISTIC                    | SYMBOL     | TEST CIR-CUIT | TEST CONDITION                     | MIN. | TYP. | MAX. | UNIT             |
|-----------------------------------|------------|---------------|------------------------------------|------|------|------|------------------|
| Maximum Input Level               | Ain        | —             | V <sub>DD</sub> = 5.0V             | —    | 1.1  | —    | V <sub>rms</sub> |
| S / (N + D) Ratio                 | S / N (AD) | —             | - 30dB 1kHz<br>Sine wave input (*) | 68   | 78   | —    | dB               |
| Total Harmonic Distortion + Noise | THD (AD)   | —             | - 0dB 1kHz<br>Sine wave input      | —    | - 65 | - 55 | dB               |
| Cross-talk                        | CT (AD)    | —             | —                                  | —    | - 68 | - 60 | dB               |

(\*) A-Weight : ON (Typ.)

## DA converter

| CHARACTERISTIC                    | SYMBOL     | TEST CIR-CUIT | TEST CONDITION                 | MIN. | TYP. | MAX. | UNIT             |
|-----------------------------------|------------|---------------|--------------------------------|------|------|------|------------------|
| Output Level                      | Aout       | —             | —                              | —    | 1.2  | —    | V <sub>rms</sub> |
| S / N Ratio                       | S / N (DA) | —             | - 0dB 1kHz<br>Sine wave input  | 87   | 93   | —    | dB               |
| Total Harmonic Distortion + Noise | THD1 (DA)  | —             | - 0dB 1kHz<br>Sine wave input  | —    | - 83 | - 78 | dB               |
|                                   | THD2 (DA)  |               | - 0dB 10kHz<br>Sine wave input | —    | - 83 | - 75 |                  |
| Cross-talk                        | CT (DA)    | —             | —                              | —    | - 88 | - 83 | dB               |

Timing

| CHARACTERISTIC      | SYMBOL    | TEST CIR-CUIT | TEST CONDITION                              | MIN. | TYP. | MAX. | UNIT |
|---------------------|-----------|---------------|---|------|------|------|------|
| Rise Time           | $t_r$     | —             | LRCKO, BCKO, SDO, EXTO                      | —    | —    | 15   | ns   |
|                     |           | —             | MCK1, MCK2                                  | —    | —    | 8    |      |
| Fall Time           | $t_f$     | —             | LRCKO, BCKO, SDO, EXTO                      | —    | —    | 15   |      |
|                     |           | —             | MCK1, MCK2                                  | —    | —    | 8    |      |
| Delay Time          | $t_d$     | —             | LRCKI→LRCKO<br>(External clock synchronous) | —    | —    | 30   |      |
|                     |           | —             | BCKI→BCKO<br>(External clock synchronous)   | —    | —    | 20   |      |
|                     |           | —             | BCKO→SDO                                    | —    | —    | 10   |      |
|                     |           | —             | MCK1→LRCKO<br>(Internal clock synchronous)  | —    | —    | 50   |      |
|                     |           | —             | MCK1→BCKO<br>(Internal clock synchronous)   | —    | —    | 20   |      |
| Operating Frequency | $f_{opr}$ | —             | XI = 256fs                                  | 8.0  | 11.3 | 12.5 | MHz  |
|                     |           | —             | XI = 384fs                                  | 10.0 | 16.9 | 18.5 |      |
|                     |           | —             | XI = 512fs                                  | 16.0 | 22.6 | 25.5 |      |
|                     |           | —             | XI = 768fs                                  | 24.0 | 33.9 | 34.0 |      |

(Note 1) At the external clock synchronous, LRCKO and BCKO output signal are same as LRCKI and BCKI input signal.

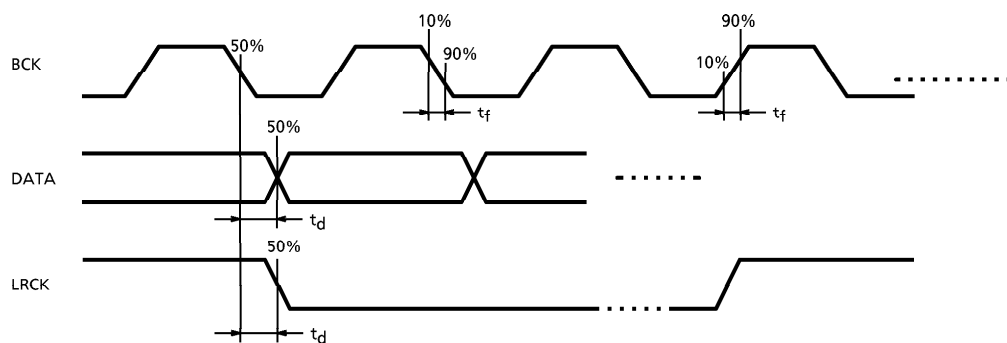
At the internal clock synchronous, LRCKO and BCKO output signal are output synchronously with the falling edge of MCK1.

(Note 2) Measured with the output load  $CL = 10pF$ .

(Note 3) At the XI clock is 256fs, 384fs and 512fs, it is operated with the  $f_s = 32kHz$ , 44.1kHz and 48kHz. At the XI clock is 768fs, it is operated with the  $f_s = 32kHz$  and 44.1kHz.

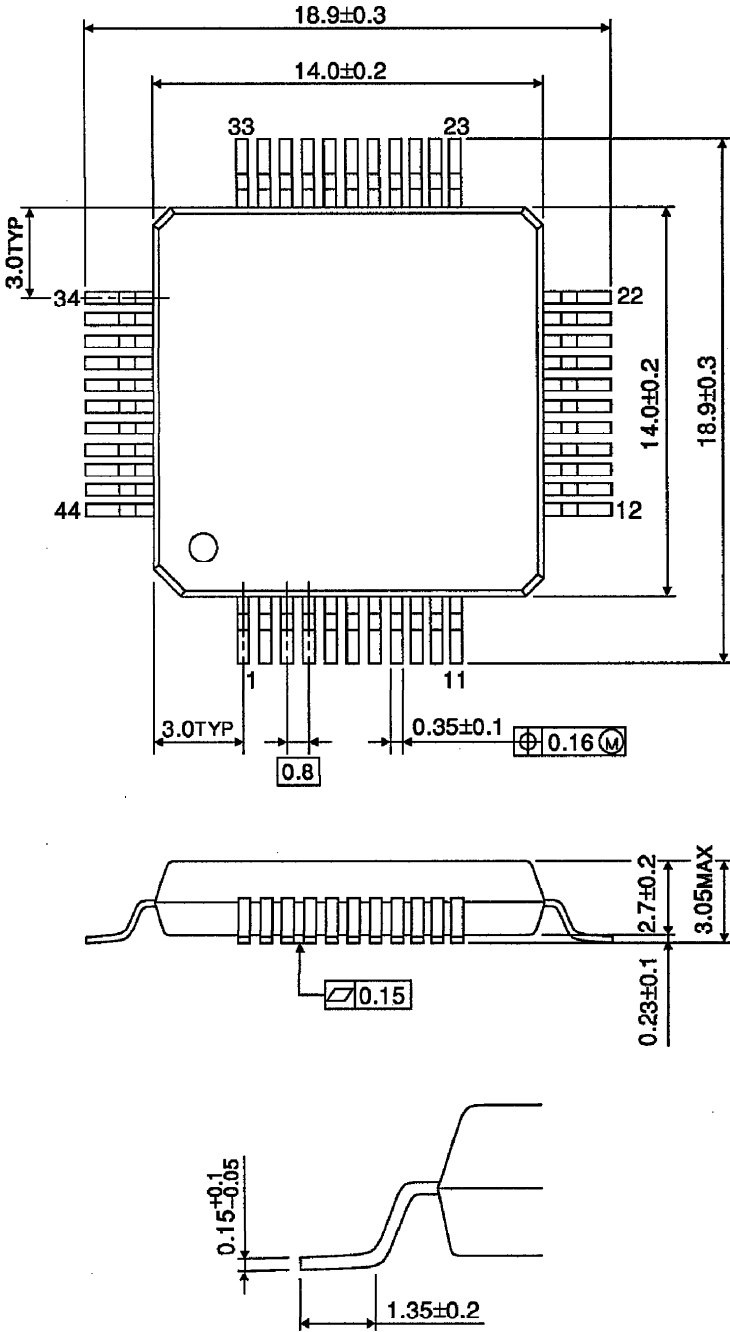
(Note 4) Delay RAM applications has limitations with the how to control the DRAM. Show the software manual.

AC CHARACTERISTIC POINT (Input signal : LRCK, BCK, DATA)



PACKAGE DIMENSIONS  
QFP44-P-1414-0.80D

Unit : mm



Weight : 1.07g (Typ.)