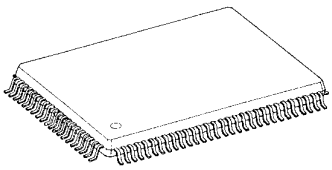
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC9447F

Single-Chip Audio Digital Signal Processor

The TC9447F is a single-chip audio digital signal processor incorporating an AD/DA converter. The built-in program memory (ROM) can contain a range of application programs for concert hall acoustic field simulation, for digital filters such as equalizers, and for dynamic range control. In addition, the device includes 64kb of data delay RAM, making external RAM unnecessary.



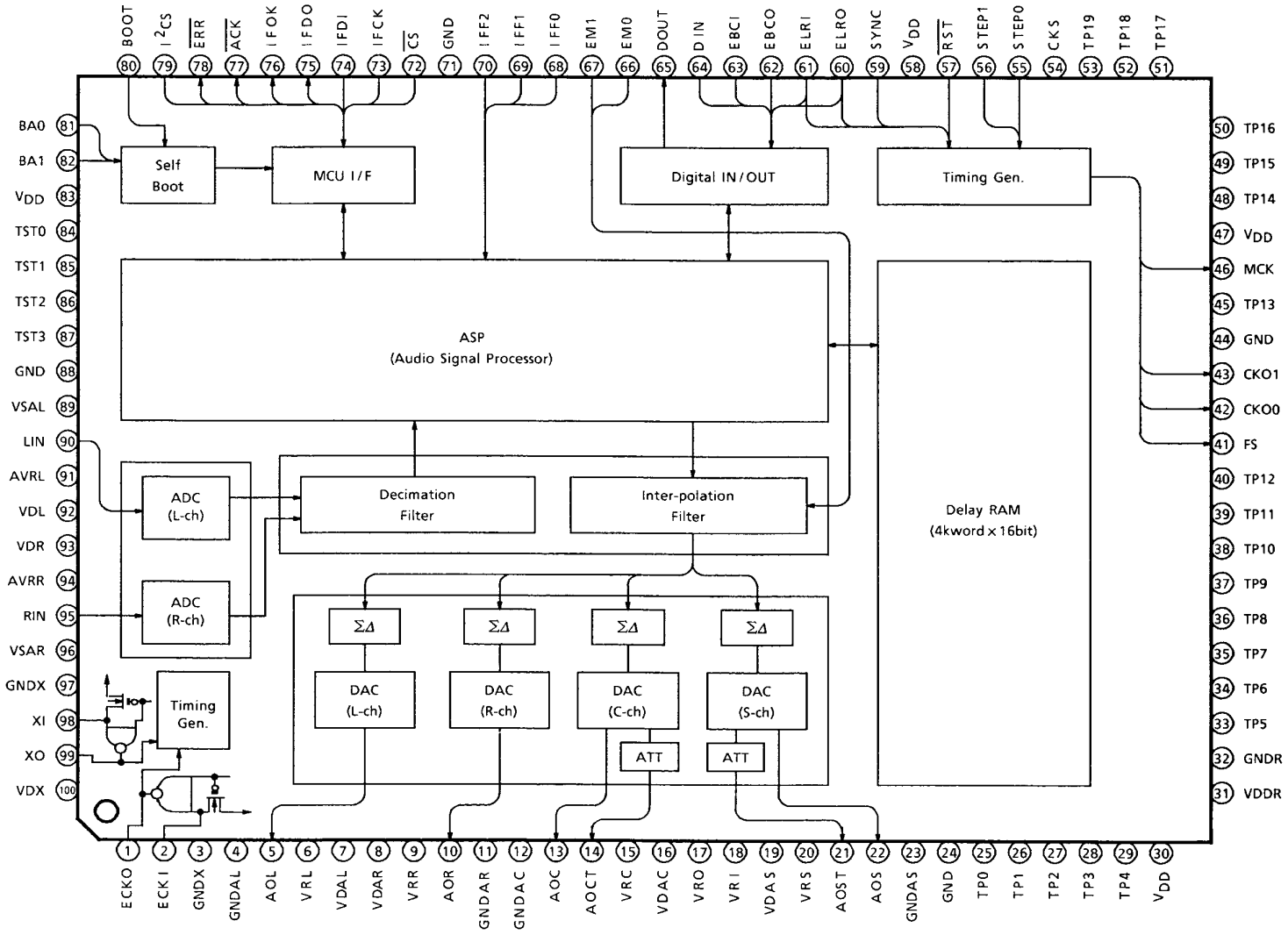
QFP100-P-1420-0.65A

Weight: 1.57g (typ.)

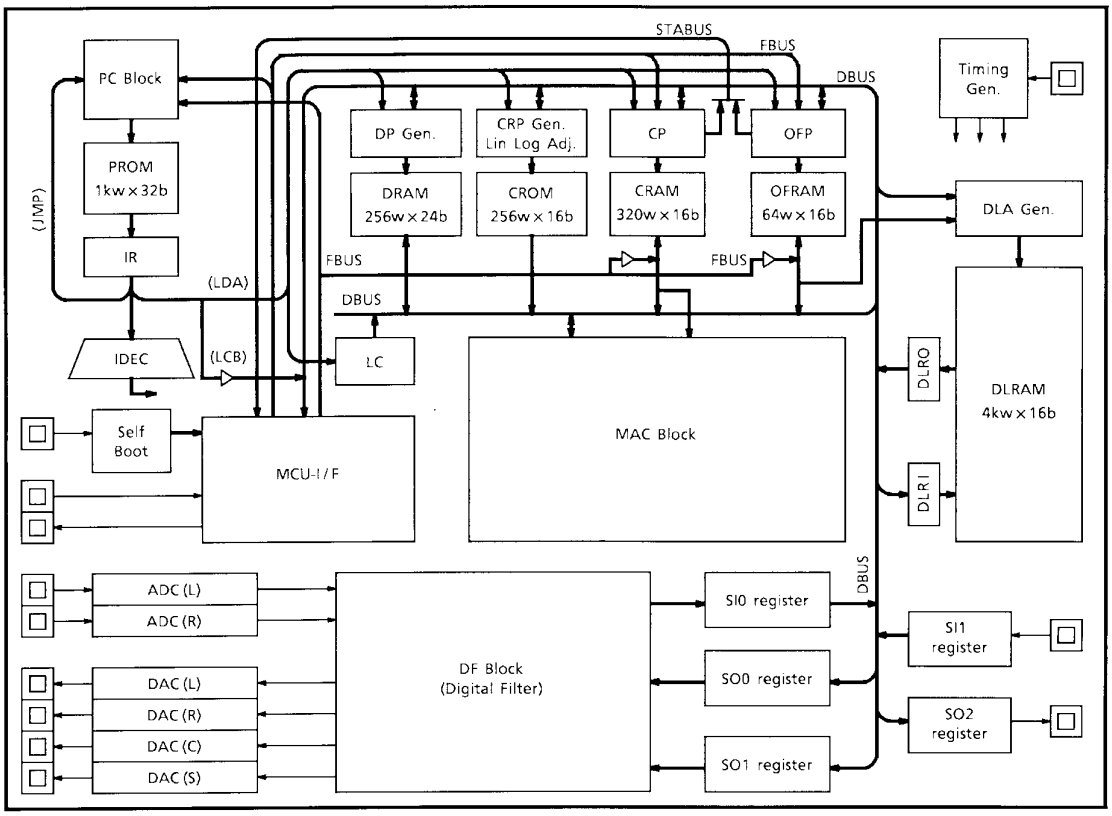
Features

- Incorporates a 1-bit ΣΔ-type AD converter (two channels).
  THD: −82dB, S/N ratio: 95dB (typ.)
- Incorporates a 1-bit ΣΔ-type DA converter (four channels).
  THD: −85dB, S/N ratio: 100dB (typ.)
- A ±10-dB attenuator is built into the DA converter output block (two channels only)
- Each port has a digital input/output (three lead-type)
- A built-in self-boot function automatically sets the coefficients and register values at initialization.
  Boot ROM : 1024 words × 18 bits
- The DSP block specifications are as follows:
  Data bus : 24 bits
  Multiplier/adder : 24 bits × 16 bits + 43 bits → 43 bits
  Accumulator : 43 bits (sign extension: 4 bits)
  Program ROM : 1024 words × 32 bits
  Coefficient RAM : 320 words × 16 bits
  Coefficient ROM : 256 words × 16 bits
  Offset RAM : 64 words × 16 bits
  Data RAM : 256 words × 24 bits
  Operation speed : 44ns (510-step (approx) operation per cycle at fs = 44.1 kHz)
  Interface buffer RAM : 32 words × 16 bits
- Incorporates data delay RAM.
  Delay RAM : 4096 words × 16 bits (64 kbits)
- The microcontroller interface can be selected between Standard Transmission mode and I^2C bus mode.
- CMOS silicon structure supports high speed.
- The package is a 100-pin flat package.

Pin Connection



Block Diagram



Pin Function

Pin No.	Symbol	I/O	Function	Remarks
1	ECKO	O	Amp output pin for external clock input	
2	ECKI	I	Amp input pin for external clock input	Pulled-down resistor (with on/off switching function)
3	GNDX	—	Ground pin for oscillator circuit	
4	GNDAL	—	Ground pin for DAC L channel	
5	AOL	O	DAC analog signal output pin (L channel)	
6	VRL	—	DAC reference voltage pin (L channel)	
7	VDAL	—	Power pin for DAC L channel	
8	VDAR	—	Power pin for DAC R channel	
9	VRR	—	DAC reference voltage pin (R channel)	
10	AOR	O	DAC analog signal output pin (R channel)	
11	GNDAR	—	Ground pin for DAC R channel	
12	GNDAC	—	Ground pin for DAC C channel	
13	AOC	O	DAC analog signal output pin (C channel)	
14	AOCT	O	DAC analog signal output pin with attenuator (C channel)	
15	VRC	—	DAC reference voltage pin (C channel)	
16	VDAC	—	Power pin for DAC C channel	
17	VRO	O	Reference voltage pin for attenuator (buffer output)	
18	VRI	I	Reference voltage pin for attenuator (buffer input)	
19	VDAS	—	Power pin for DAC S channel	
20	VRS	—	DAC reference voltage pin (S channel)	
21	AOST	O	DAC analog signal output pin with attenuator (S channel)	
22	AOS	O	DAC analog signal output pin (S channel)	
23	GNDAS	—	Ground pin for DAC S channel	
24	GND	—	Ground pin	
25~29	TP0~TP4	O	Test pins (leave open)	
30	VDD	—	Power pin	
31	VDDR	—	Power pin for DLRAM	
32	GNDR	—	Ground pin for DLRAM	
33~40	TP5~TP12	O	Test pins (leave open)	
41	FS	O	Clock output pin (1 fs)	
42	CKO0	O	Clock output pin 0	
43	CKO1	O	Clock output pin 1	
44	GND	—	Ground pin	
45	TP13	O	Test pin (leave open)	
46	MCK	O	MCK clock output pin (256 fs/512 fs/ (384/768 fs))	Push-pull output
47	V_{DD}	—	Power pin	
48~53	TP14~TP19	O	Test pin (leave open)	
54	CKS	I	Master clock switching pin	Schmitt input
55	STEP0	I	Execution step switching pin 0	Schmitt input
56	STEP1	I	Execution step switching pin 1	Schmitt input
57	$\overline{RST}$	I	Reset pin	Schmitt input

Pin No.	Symbol	I/O	Function	Remarks
58	V_{DD}	—	Power pin	
59	SYNC	I	Program SYNC signal input pin	Schmitt input
60	ELRO	I	LR clock input pin for serial data output	Schmitt input
61	ELRI	I	LR clock input pin for serial data input	Schmitt input
62	EBCO	I	Bit clock input pin for serial data output	Schmitt input
63	EBCI	I	Bit clock input pin for serial data input	Schmitt input
64	DIN	I	Serial data input pin	Schmitt input
65	DOUT	O	Serial data output pin	Push-pull output
66	EM0	I	De-emphasis setting pin 0	Schmitt input
67	EM1	I	De-emphasis setting pin 1	Schmitt input
68	IFF0	I	Interface flag pin 0	Schmitt input
69	IFF1	I	Interface flag pin 1	Schmitt input
70	IFF2	I	Interface flag pin 2	Schmitt input
71	GND	—	Ground pin	
72	$\overline{CS}$	I	Microcontroller interface chip select signal input pin	Schmitt input
73	IFCK	I	Microcontroller interface data shift clock input pin	Schmitt input
74	IFDI	I/O	Microcontroller interface data input pin (Data input/output pin when I^2C bus selected)	Schmitt input/ open drain output
75	IFDO	O	Microcontroller interface data output pin (Leave open when I^2C bus selected.)	Push-pull output
76	IFOK	O	Microcontroller interface operation flag output pin	Open drain output
77	$\overline{ACK}$	O	Microcontroller interface acknowledge output pin	Open drain output
78	$\overline{ERR}$	O	Microcontroller interface error flag output pin	Open drain output
79	I^2CS	I	Microcontroller interface I^2C bus switching pin	
80	BOOT	I	Self-boot control pin	Schmitt input
81	BA0	I	Boot address setting pin 0	Schmitt input
82	BA1	I	Boot address setting pin 1	Schmitt input
83	VDD	—	Power pin	
84~87	TST0~TST3	I	Test pins. Use fixed to low level.	Schmitt input
88	GND	—	Ground pin	
89	VSAL	—	Ground pin for analog mode (ADC L channel)	
90	LIN	I	ADC analog signal input pin (L channel)	
91	AVRL	—	ADC reference voltage pin (L channel)	
92	VDL	—	Power pin for analog mode (ADC L channel)	
93	VDR	—	Power pin for analog mode (ADC R channel)	
94	AVRR	—	ADC reference voltage pin (R channel)	
95	RIN	I	ADC analog signal input pin (R channel)	
96	VSAR	—	Ground pin for analog mode (ADC R channel)	
97	GNDX	—	Ground pin for oscillator circuit	
98	XI	I	Crystal oscillator connecting pin (input)	Pulled-down resistor (with on/off switching function)
99	XO	O	Crystal oscillator connecting pin (output)	
100	VDX	—	Power pin for oscillator circuit	

Operation

1. Pin operations

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Function</th></tr>
<tr><td>1</td><td>ECKO</td><td rowspan="2">Supplies an external clock to ECKI (for slave operations).
When CKS pin = H, oscillation activated. When CKS = L, pulled down internally.</td></tr>
<tr><td>2</td><td>ECKI</td></tr>
<tr><td>3~24</td><td>Omitted</td><td>—</td></tr>
<tr><td>25~40</td><td>TP [0:12]</td><td>Test pins (leave open) (TPx description is omitted.)</td></tr>
<tr><td>41</td><td>FS</td><td>1 fs output</td></tr>
<tr><td>42, 43</td><td>CKO [1:0]</td><td>Timing output pins. The output frequency is set from the microcontroller. (CMD-40h)
<table>
<tr><th colspan="3">CKOS0</th><th rowspan="2">CKO0</th></tr>
<tr><th>2</th><th>1</th><th>0</th></tr>
<tr><td rowspan="4">0</td><td rowspan="2">0</td><td>0</td><td>Fixed to L (initial value)</td></tr>
<tr><td>1</td><td>fs2</td></tr>
<tr><td rowspan="2">1</td><td>0</td><td>fs4</td></tr>
<tr><td>1</td><td>fs8</td></tr>
<tr><td rowspan="4">1</td><td rowspan="2">0</td><td>0</td><td>fs16</td></tr>
<tr><td>1</td><td>fs32</td></tr>
<tr><td rowspan="2">1</td><td>0</td><td>fs64</td></tr>
<tr><td>1</td><td>fs128</td></tr>
</table>
<table>
<tr><th colspan="3">CKOS1</th><th rowspan="2">CKO1</th></tr>
<tr><th>2</th><th>1</th><th>0</th></tr>
<tr><td rowspan="4">0</td><td rowspan="2">0</td><td>0</td><td>Fixed to L (initial value)</td></tr>
<tr><td>1</td><td>fs2</td></tr>
<tr><td rowspan="2">1</td><td>0</td><td>fs4</td></tr>
<tr><td>1</td><td>fs8</td></tr>
<tr><td rowspan="4">1</td><td rowspan="2">0</td><td>0</td><td>fs16</td></tr>
<tr><td>1</td><td>fs32</td></tr>
<tr><td rowspan="2">1</td><td>0</td><td>fs64</td></tr>
<tr><td>1</td><td>1/2 XI or 1/2 ECKI</td></tr>
</table></td></tr>
<tr><td>46</td><td>MCK</td><td>Master clock output pin. Output is validated/invalidated and the frequency is switched from the microcontroller. (CMD-4Dh)
<table>
<tr><th>MCKE</th><th>MCK</th></tr>
<tr><td>0</td><td>Fixed to L</td></tr>
<tr><td>1</td><td>Output valid (initial value)</td></tr>
</table>
<table>
<tr><th>MCKE</th><th>STEP1</th><th>MCK</th></tr>
<tr><td>0</td><td>don't care</td><td>256 fs</td></tr>
<tr><td rowspan="2">1</td><td>0</td><td>Source oscillation (XI/XO or ECKI)</td></tr>
<tr><td>1</td><td>For testing</td></tr>
</table></td></tr>
<tr><td>54</td><td>CKS</td><td>Source oscillation selector pin
<table>
<tr><th>CKS</th><th>Source Oscillation</th></tr>
<tr><td>0</td><td>XI/XO pin</td></tr>
<tr><td>1</td><td>ECKI/ECKO pin</td></tr>
</table></td></tr>
<tr><td>55, 56</td><td>STEP [1:0]</td><td>Source oscillation frequency/ASP operation speed switching pins
<table>
<tr><th>STEP1</th><th>STEP0</th><th>Source Oscillation Frequency</th><th>No. of ASP Operation Steps</th></tr>
<tr><td rowspan="2">0</td><td>0</td><td>512 fs</td><td>340/fs</td></tr>
<tr><td>1</td><td>768 fs</td><td>510/fs</td></tr>
<tr><td>1</td><td>*</td><td colspan="2">For testing</td></tr>
</table>
*: don't care</td></tr>
<tr><td>57</td><td>$\overline{\text{RST}}$</td><td>Reset input (L at initialization)</td></tr>
<tr><td>59</td><td>SYNC</td><td>Program operation SYNC signal input pin. Valid when program is executing a slave operation.</td></tr>
<tr><td>60</td><td>ELRO</td><td>LR clock signal input pin for serial output data. Valid when serial data are output in a slave operation.</td></tr>
<tr><td>61</td><td>ELRI</td><td>LR clock signal input pin for serial input data. Valid when serial data are input in a slave operation.</td></tr>
<tr><td>62</td><td>EBCO</td><td>Bit clock signal input pin for serial output data. Valid when serial data are output in a slave operation.</td></tr>
<tr><td>63</td><td>EBCI</td><td>Bit clock signal input pin for serial input data. Valid when serial data are input in a slave operation.</td></tr>
</table>

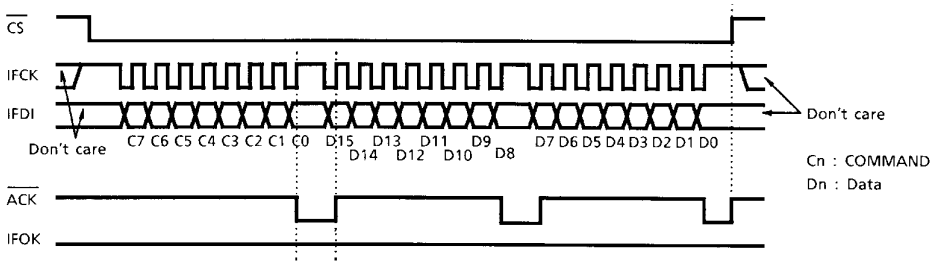
<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Function</th></tr>
<tr><td>64</td><td>DIN</td><td>Serial input data signal input pin. Normally connected to internal register SI2 in ASP block.</td></tr>
<tr><td>65</td><td>DOUT</td><td>Serial output data signal output pin. Normally connected to internal register SO2 in ASP block.</td></tr>
<tr><td>66, 67</td><td>EM [1:0]</td><td>De-emphasis control pins
<table>
<tr><th>EM1</th><th>EM0</th><th>De-Emphasis Settings</th></tr>
<tr><td rowspan="2">0</td><td>0</td><td>De-emphasis off</td></tr>
<tr><td>1</td><td>For fs = 48 kHz</td></tr>
<tr><td rowspan="2">1</td><td>0</td><td>For fs = 44.1 kHz</td></tr>
<tr><td>1</td><td>For fs = 32 kHz</td></tr>
</table></td></tr>
<tr><td>68~70</td><td>IFF [2:0]</td><td>IFF control input pins. This functions the same as the microcontroller IFF [2:0] setting.
The program uses the latest changes to the flags.</td></tr>
<tr><td>72</td><td>$\overline{CS}$</td><td rowspan="8">Microcontroller interface pins
<table>
<tr><th></th><th>Standard Transmission Mode (I^2CS = L)</th><th>I^2C Mode (I^2CS = H)</th></tr>
<tr><td>I^2CS</td><td colspan="2">Transmit/receive mode switching (Standard Transmission mode/I^2C mode)</td></tr>
<tr><td>$\overline{CS}$</td><td>Chip select (Control required)</td><td>Chip select (Can be fixed to L)</td></tr>
<tr><td>IFCK</td><td colspan="2">Transmit/receive clock</td></tr>
<tr><td>IFDI</td><td>MCU data input</td><td>MCU data input/output</td></tr>
<tr><td>IFDO</td><td>Monitor data output</td><td>Fixed to L output</td></tr>
<tr><td>$\overline{ACK}$</td><td>Acknowledge signal output</td><td>Fixed to HZ</td></tr>
<tr><td>$\overline{ERR}$</td><td colspan="2">Error flag signal output</td></tr>
<tr><td>IFOK</td><td colspan="2">Internal operation confirmation flag signal output</td></tr>
</table>
For details, see 2, microcontroller interface below.</td></tr>
<tr><td>73</td><td>IFCK</td></tr>
<tr><td>74</td><td>IFDI</td></tr>
<tr><td>75</td><td>IFDO</td></tr>
<tr><td>76</td><td>IFOK</td></tr>
<tr><td>77</td><td>$\overline{ACK}$</td></tr>
<tr><td>78</td><td>$\overline{ERR}$</td></tr>
<tr><td>79</td><td>I^2CS</td></tr>
<tr><td>80</td><td>BOOT</td><td>Self-boot select pin
<table>
<tr><th>BOOT</th><th>Operation</th></tr>
<tr><td>0</td><td>Does not boot at reset</td></tr>
<tr><td>1</td><td>Boot at reset</td></tr>
</table></td></tr>
<tr><td>81, 82</td><td>BA [1:0]</td><td>Self-boot start address pins (at reset)
<table>
<tr><th>BA1</th><th>BA0</th><th>Start Address</th></tr>
<tr><td rowspan="2">0</td><td>0</td><td>000h</td></tr>
<tr><td>1</td><td>001h</td></tr>
<tr><td rowspan="2">1</td><td>0</td><td>002h</td></tr>
<tr><td>1</td><td>003h</td></tr>
</table></td></tr>
<tr><td>84~87</td><td>TST [3:0]</td><td>Pins for inputting test settings. Use fixed to L.</td></tr>
<tr><td>88~97</td><td>Omitted</td><td>—</td></tr>
<tr><td>98</td><td>XI</td><td rowspan="2">Connect the crystal oscillator (master mode).
Setting CKS = L enables oscillation. Setting CKS = H pulls down XI/XO using the internal resistor.</td></tr>
<tr><td>99</td><td>XO</td></tr>
</table>

2. Microcontroller interface

(1) Standard transmission mode 1

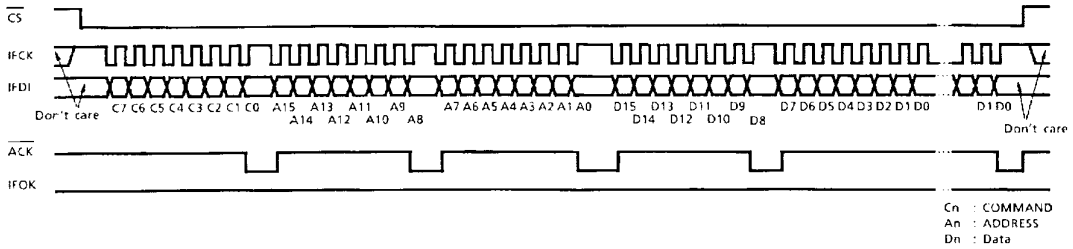
When I^2CS = L, data can be transmitted or received in Standard Transmission mode.
When the $\overline{CS}$ signal is Low, control from the microcontroller is enabled.
The IFCK signal is the transmit/receive clock. The IFDI signal is the data. The TC9447F loads the IFDI data on the IFCK signal rising edge. When $\overline{CS}$ = H, the IFCK and IFDI signals are don't care.

(1-1) Setting registers



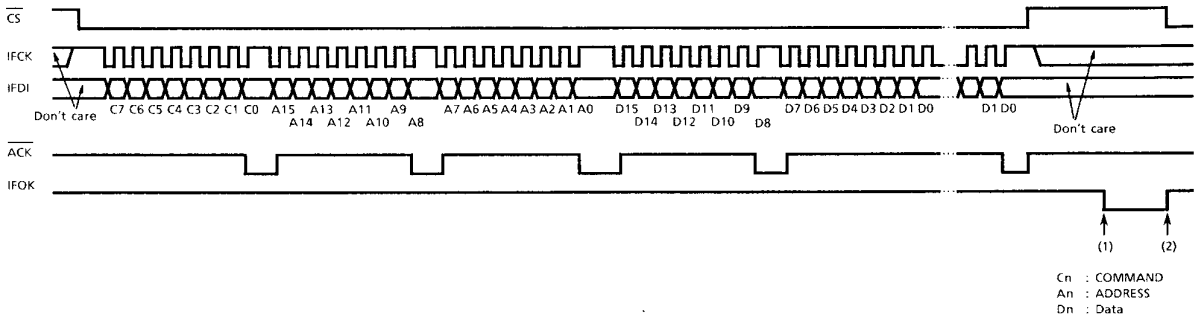
The registers are set by command data using the IFDI signal. The first byte is a command, which differs for each register. The data sent after that are fixed to two bytes. Both command and data are sent starting from the MSB.
The $\overline{ACK}$ signal is the acknowledge signal that the TC9447F returns to the microcontroller. Because the $\overline{ACK}$ signal is open drain output, it must be pulled up outside the pin. Data are loaded on the rising edge of the IFCK signal.
Note that commands or data that must be switched on the SYNC signal, such as the RUN command or the IFF flag, must be synchronized with the SYNC signal and loaded on that signal.

(1-2) Setting RAM (sequential)

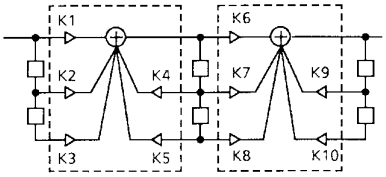


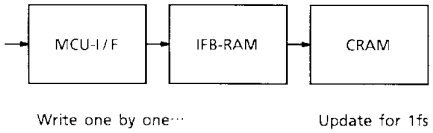
The RAMs are set by command data using the IFDI signal. The first byte is a command, which differs for each RAM. The next two bytes contain the start address for the RAM written.
The length of the data field following the RAM address bytes is 2 × n bytes. The address is automatically incremented by 1.

(1-3) Setting RAM (ACMP mode)

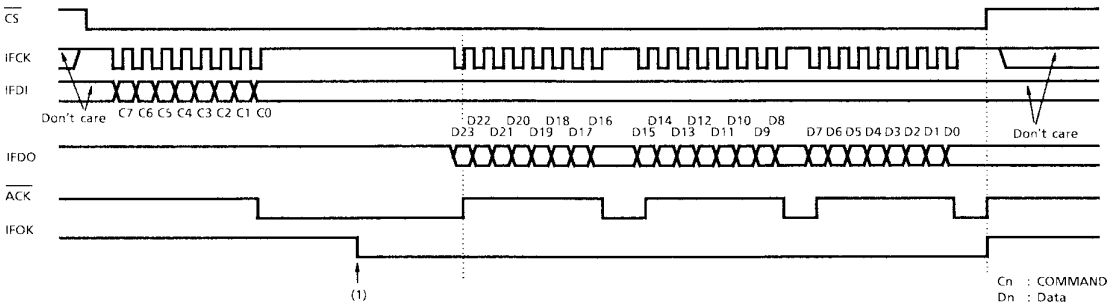


In ACMP mode, the TC9447F does not write data directly to coefficient RAM (CRAM) or offset RAM (OFRAM). In this mode, data must first be written to the interface buffer RAM (IFB-RAM). Then, all the data are updated together in a period of 1 fs.
For example, if a signal flow filter is designed as in the following diagram, unless the K1 to K5 data are batch-updated, the circuit may resonate. The same applies to the K6 to K10 data.
Using ACMP mode can reduce the noise caused by updating coefficients while the TC9447F is operating. This mode can suppress noise in almost all cases.
IFB-RAM is 32-word memory. Therefore, data can be updated at one time in units of up to 32 words.
The format of IFB-RAM is similar to the format of the RAM in 1-2 above. The length of the data field is $2 \times n$ bytes, where $n \leq 32$.
In ACMP mode, the IFOK pin outputs an ACMP operation end flag.
When ACMP operations complete, the flag is set to Low (1) and is initialized at the next low chip select $\overline{CS}$ signal (2).





(1-4) Monitor mode

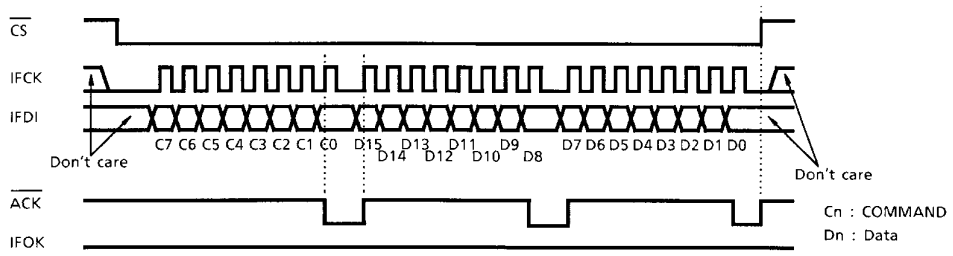


Monitor mode is used to monitor the data bus or pointers.
There are two further modes: a mode where the data bus or pointer (s) is monitored at a preset program counter (PC) and a mode where a loop counter (LC) is added to monitor conditions in addition to the PC. After the command is issued, when the TC9447F loads data to the IFDO register (IFDOR), the IFOK pin signal is set to Low (see (1) above).
Next, when the IFCK signal is sent, the data are output on the IFCK signal falling edge starting from the MSB. The data length is at its maximum (24 bits or three bytes) during monitoring of the data bus. In cases where transfer must be interrupted, such as where only eight or 16 bits of the MSB side are required, monitoring can be interrupted at any time by setting the $\overline{CS}$ signal to High. When the $\overline{CS}$ signal goes High, the IFOK signal also goes High.
When $\overline{CS}$ = H, all monitor circuits are initialized.

(2) Standard transmission mode 2

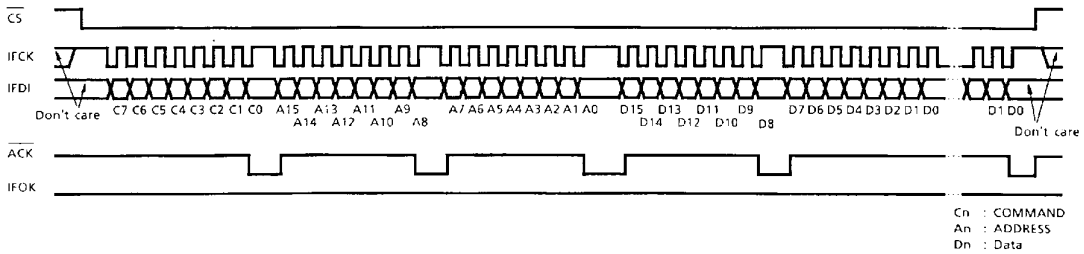
When I^2CS = L, data can be transmitted or received in Standard Transmission mode.
When the $\overline{CS}$ signal is Low, control from the microcontroller is enabled.
The IFCK signal is the transmit/receive clock. The IFDI signal is the data. The TC9447F loads the IFDI data on the IFCK signal rising edge. When $\overline{CS}$ = H, the IFCK and IFDI signals are don't care.

(2-1) Setting registers



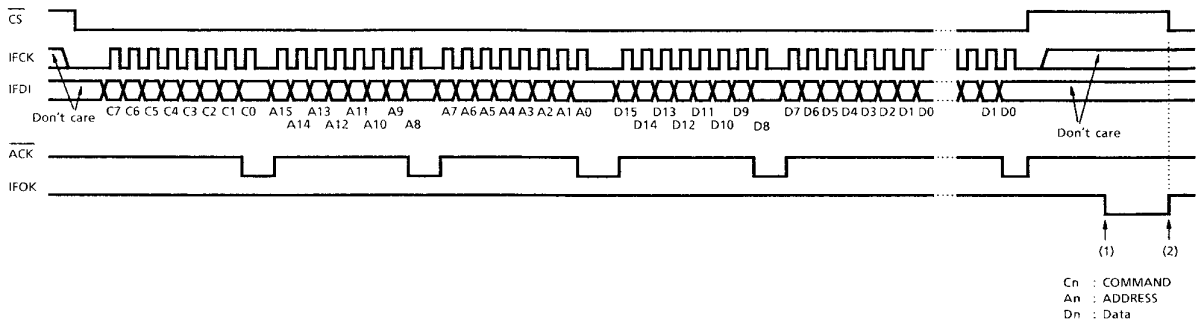
The registers are set by command data using the IFDI signal. The first byte is a command, which differs for each register. The data sent after that are fixed to two bytes. Both command and data are sent starting from the MSB.
The $\overline{ACK}$ signal is the acknowledge signal that the TC9447F returns to the microcontroller. As the $\overline{ACK}$ signal is open drain output, it must be pulled up outside the pin. The data are loaded on the rising edge of the IFCK signal.
Note that commands or data that must be switched on the SYNC signal, such as the RUN command or the IFF flag, must be synchronized with the SYNC signal and loaded on that signal.

(2-2) Setting RAM (sequential)

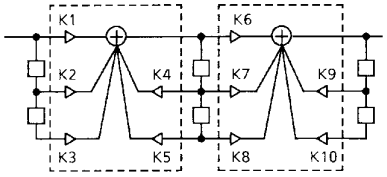


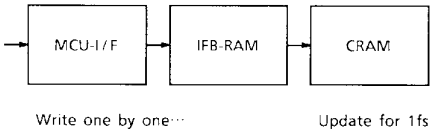
The RAMs are set by command data using the IFDI signal. The first byte is a command, which differs for each RAM. The next two bytes contain the start address for the RAM written.
The length of the data field following the RAM address bytes is 2 × n bytes. The address is automatically incremented by 1.

(2-3) Setting RAM (ACMP mode)

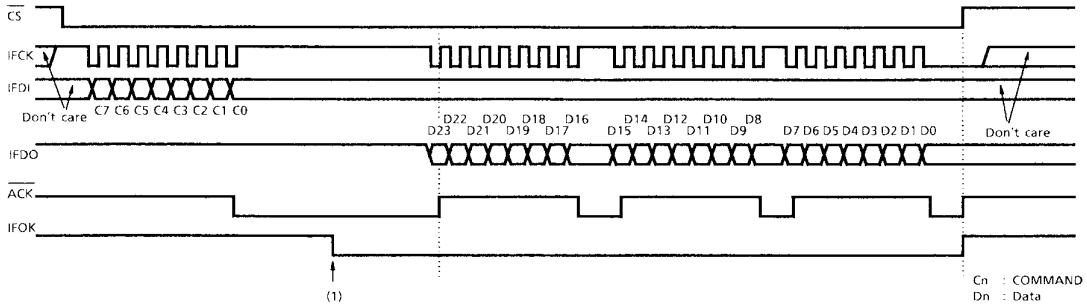


In ACMP mode, the TC9447F does not write data directly to coefficient RAM (CRAM) or offset RAM (OFRAM). In this mode, data must first be written to the interface buffer RAM (IFB-RAM). Then, all the data are updated together in a period of 1 fs.
For example, if a signal flow filter is designed as in the following diagram, unless the K1 to K5 data are batch-updated, the circuit may resonate. The same applies to the K6 to K10 data.
Using ACMP mode can reduce the noise caused by updating coefficients while the TC9447F is operating. This mode can suppress noise in almost all cases.
IFB-RAM is 32-word memory. Therefore, data can be updated at one time in units of up to 32 words. The format of IFB-RAM is similar to the format of the RAM in 2-2 above. The length of the data field is $2 \times n$ bytes, where $n \leq 32$.
In ACMP mode, the IFOK pin outputs an ACMP operation end flag.
When ACMP operations complete, the flag is set to Low (1) and is initialized at the next low chip select $\overline{CS}$ signal (2).





(2-4) Monitor mode

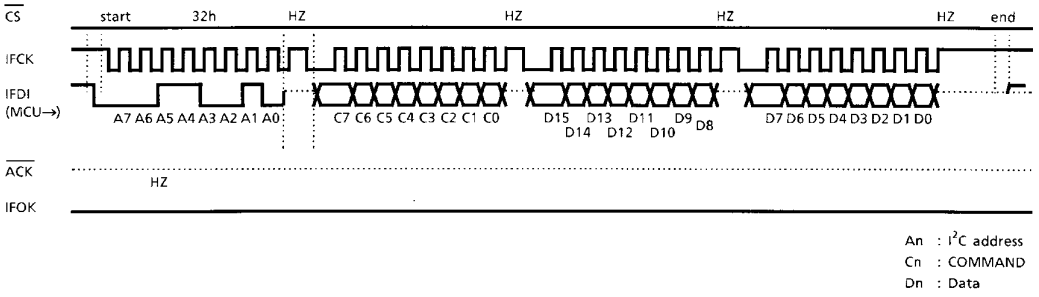


Monitor mode is used to monitor the data bus or pointers.
There are two further modes: a mode where the data bus or pointer (s) is monitored at a preset program counter (PC) and a mode where a loop counter (LC) is added to monitor conditions in addition to the PC. After the command is issued, when the TC9447F loads data to the IFDO register (IFDOR), the IFOK pin signal is set to Low (see (1) above).
Next, when the IFCK signal is sent, data are output on the IFCK signal falling edge from the MSB first. The data length is at its maximum (24 bits or three bytes) during monitoring of the data bus. In cases where transfer must be interrupted, such as where only eight or 16 bits of the MSB side are required, monitoring can be interrupted at any time by setting the $\overline{CS}$ signal to High. When the $\overline{CS}$ signal goes High, the IFOK signal also goes High.
When $\overline{CS}$ = H, all monitor circuits are initialized.

(3) I^2C bus mode

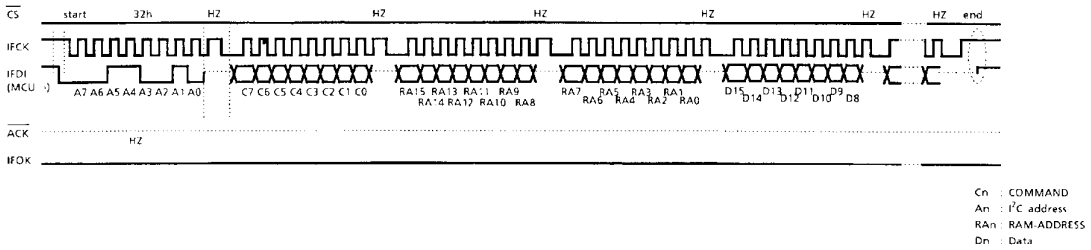
When I^2CS = H, data can be transmitted or received in Standard Transmission mode.
When the $\overline{CS}$ signal is Low, control from the microcontroller is enabled.
In I^2C mode, the $\overline{CS}$ signal can be used fixed to L.
The IFCK signal is the transmit/receive clock. The IFDI signal is the data. The TC9447F loads the IFDI data on the IFCK signal rising edge. When $\overline{CS}$ = H, the IFCK and IFDI signals are don't care.

(3-1) Setting registers



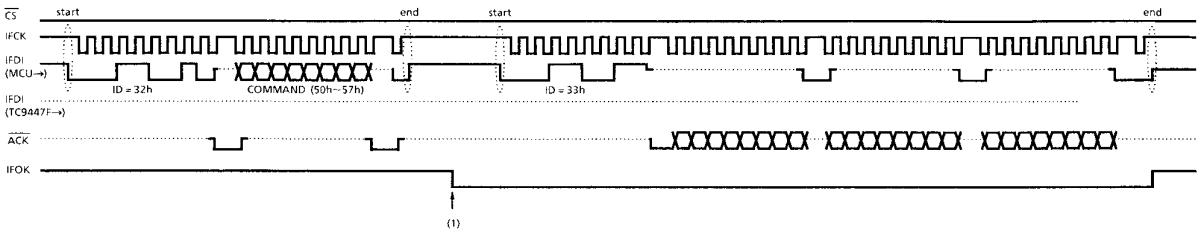
The registers are set by command data using the IFDI signal. The first byte after the I^2C address (32h) is a command, which differs for each register. The data sent after that are fixed to two bytes. Both command and data are sent starting from the MSB in I^2C format.
The $\overline{ACK}$ pin cannot be used in I^2C format. However, the acknowledge signal can be read by using data signals in I^2C format. The data are loaded internally every two bytes.
Note that commands or data that must be switched on the SYNC signal, such as the RUN command or the IFF flag, must be synchronized with the SYNC signal and loaded on that signal.

(3-2) Setting RAM (sequential)



The RAMs are set by command data using the IFDI signal.
The first byte after the I^2C address (32h) is a command, which differs for each RAM. The next two bytes contain the start address for the RAM to be written to. The length of the data field following the RAM address bytes is 2 × n bytes. The address is automatically incremented by 1.

(3-3) Monitor mode



Monitor mode is used to monitor the data bus or pointers.
There are two further modes: a mode where the data bus or pointer (s) is monitored at a preset program counter (PC) and a mode where a loop counter (LC) is added to monitor conditions in addition to the PC.
First, issue the monitoring command, which has no data.
When the TC9447F loads data to the IFDO register (IFDOR), the IFOK pin signal is set to Low (see (1) above).
Next, the I^2C read command (ID = 33h) is issued, then when the IFCK signal is sent, the data are output on the IFCK signal falling edge starting from the MSB. The data length is at its maximum (24 bits or three bytes) during monitoring of the data bus. In cases where transfer must be interrupted, such as where only eight or 16 bits of the MSB side are required, monitoring can be interrupted by sending the I^2C end condition (set data level to H while the clock = H).
After issuing a monitor command (50h~56h), be sure to perform a continuous read operation by issuing the I^2C read command (ID = 33h).

(3-4) MCU does not write data by ACMP mode at I^2C bus controlling.

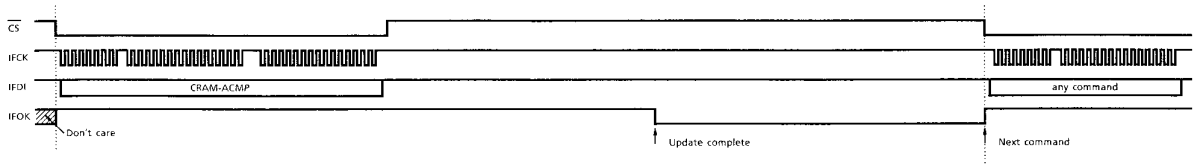
(4) IFOK pin description

The IFOK signal has the following three functions.

(4-1) ACMP mode end flag output

After the completion of a RAM data update with CRAM-ACMP (CMD: 47h) or OFRAM-ACMP (CMD: 49h), the IFOK pin goes Low. Setting the $\overline{CS}$ signal to Low changes the IFOK signal from Low to High.

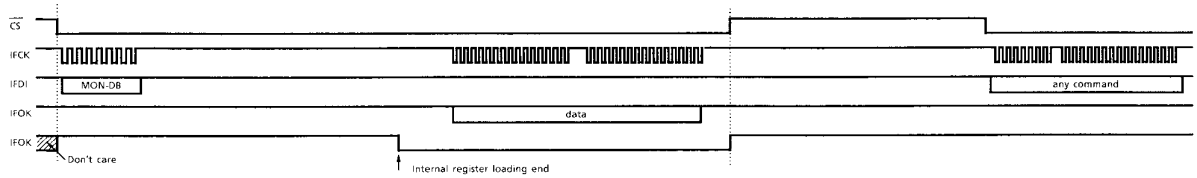
Example:



(4-2) Loading end flag output in Monitor mode

When monitoring using the bus monitor command (CMD: 50h), for example, after data are loaded to the internal register under the specified conditions, the IFOK signal goes Low. In monitor mode, when the $\overline{CS}$ signal goes High, the IFOK signal also goes High.

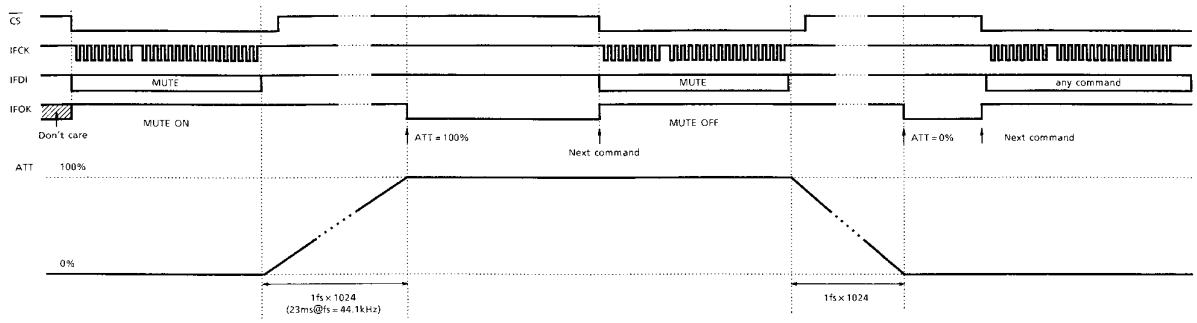
Example:



(4-3) Mute end flag output for digital filter (DF) block

When using a command to control the DF block mute on/off (CMD: 36h, bit 5), the mute end flag is output from the IFOK pin after the mute operation completes.

Example:



Note 1: At power on, the IFOK pin output is undefined. When the $\overline{CS}$ signal goes Low, the IFOK signal goes High.

3. Control commands

The following table lists the control commands that can be used from the microcontroller.

(1) Control commands

Table 1 Control commands

Command	Code	R/W	Description	RAM Sequential	Transfer Sync With/Async to Sync Signal
TIMING	40h	W	Timing	—	Async
BOOT	41h		Self-boot ROM start address	—	Async
DAC	42h		DAC output attenuator	—	Async
SIO	43h		SIO setting	—	Async
RUN-MUTE	44h		Program execution, mute	—	Sync (Note 2)
MSEQ	45h		Sequential RAM	Enable	Sync (RUN)/Async (STOP)
CRAM	46h		CRAM		Sync (RUN)/Async (STOP)
CRAM-ACMP	47h		CRAM (ACMP mode)		Async
OFRAM	48h		OFRAM		Sync (RUN)/Async (STOP)
OFRAM-ACMP	49h		OFRAM (ACMP mode)		Async
IFF	4Ah		Interface flag (IFF)	—	Sync (Note 2)
MONI-PC	4Bh		Monitor (PC conditions)	—	Async
MONI-LC	4Ch		Monitor (LC conditions)	—	Async
MISC	4Dh		Others	—	Async
—	4Eh		(Prohibited)	—	—
M-RST	4Fh		Initialization	—	Async
MONI-DB	50h	R	DB monitor	—	Async
MONI-CP	51h		CP monitor	—	Async
MONI-OFP	52h		OFP monitor	—	Async
MONI-DP	53h		DP monitor	—	Async
MONI-AR	54h		AR monitor	—	Async
MONI-CRP	55h		CRP monitor	—	Async
MONI-SR	56h		SR monitor	—	Async

Note 2: The command which is "Sync" in the transfer Sync with Sync signal needs to set the $\overline{CS}$ = H section to a minimum of 1 fs more until it transmits the following command.(It needs more than 22.68 μs at fs = 44.1 kHz)

(2) Control commands

COMMAND-40h (Timing)	0100 0000

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SYPD	SYD1	SYD0	SYPA	SYA1	SYA0	SYPS	SYS1	SYS0	Unas-signed	CKOS12	CKOS11	CKOS10	CKOS02	CKOS01	CKOS00

Name	Description	Value	Operation
SYPD	Digital block sync polarity switching	0	ASP program starts on falling edge
		1	ASP program starts on rising edge (initial value)
SYD [1:0]	ASP digital block SYNC signal input switching	0	Signal after SYNC output (initial value)
		1	SYNC pin
		2	ELRI pin
		3	ELRO pin
SYPA	Analog block sync polarity switching	0	Digital filter (DF) program starts on falling edge (initial value)
		1	Digital filter (DF) program starts on rising edge
SYA [1:0]	Analog block SYNC signal input switching	0	Signal after SYNC output (initial value)
		1	SYNC pin
		2	ELRI pin
		3	ELRO pin
SYPS	Overall system sync polarity switching	0	Operates at polarity for SYPD, SYPA settings above (initial value).
		1	Reverses all polarities for SYPD, SYPA settings above.
SYS [1:0]	SYNC circuit input switching	0	Internal SYNC signal (initial value)
		1	SYNC pin
		2	ELRI pin
		3	ELRO pin
CKOS1 [2:0]	CKO1 pin output selection	0	Fixed to L (initial value)
		1	fs2
		2	fs4
		3	fs8
		4	fs16
		5	fs32
		6	fs64
		7	Outputs XI or ECKI clock divided by 2
CKOS0 [2:0]	CKO0 pin output selection	0	Fixed to L (initial value)
		1	fs2
		2	fs4
		3	fs8
		4	fs16
		5	fs32
		6	fs64
		7	fs128

COMMAND-41h (BOOT) 0100 0001

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	BTA9	BTA8	BTA7	BTA6	BTA5	BTA4	BTA3	BTA2	BTA1	BTA0

Name	Description	Value	Operation
BTA [9:0]	Self-boot ROM start address	000h ~ 3FFh	Starts self-boot operation from specified address.

COMMAND-42h (DAC) 0100 0010

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	ATTC4	ATTC3	ATTC2	ATTC1	ATTC0	0	0	0	ATTS4	ATTS3	ATTS2	ATTS1	ATTS0

Name	Description	Value	Operation
ATTC	DAC C channel attenuator value	00h ~ 1Fh	00h → 0dB, 01h = −1dB, 02h = −2dB, ⋯, 15h~1Fh = −∞ (Initial value = 1Fh=−∞)
ATTS	DAC S channel attenuator value	00h ~ 1Fh	00h → 0dB, 01h = −1dB, 02h = −2dB, ⋯, 15h~1Fh = −∞ (Initial value = 1Fh = −∞)

COMMAND-43h (SIO)	0100 0011

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CHSI	0	ISLT 1	ISLT 2	IBCS 1	IBCS 0	IFMT 1	IFMT 0	CHSO 1	CHSO 0	OSLT 1	OSLT 0	OBCS 1	OBCS 0	OFMT 1	OFMT 0

Name	Description	Value	Operation
CHSI	Serial input switching	0	ADC → SI0 register, DIN pin → SI1 register (initial value)
		1	ADC → SI1 register, DIN pin → SI0 register
ISLT [1:0]	Number of serial input slots	0	16 bits/channel (initial value)
		1	20 bits/channel
		2	24 bits/channel
		3	32 bits/channel
IBCS [1:0]	Serial input bit length	0	16 bits (initial value)
		1	18 bits
		2	20 bits
		3	24 bits
IFMT [1:0]	Serial input format	0	Pads from the beginning (initial value)
		1	Pads from the end
		2	I^2S format
		3	
CHSO [1:0]	Serial output switching	0	SO0 register → DOUT pin
		1	SO1 register → DOUT pin
		2	SO2 register → DOUT pin (initial value = 2)
		3	
OSLT [1:0]	Number of serial output slots	0	16 bits/channel (initial value)
		1	20 bits/channel
		2	24 bits/channel
		3	32 bits/channel
OBCS [1:0]	Serial output bit length	0	16 bits (initial value)
		1	18 bits
		2	20 bits
		3	24 bits
OFMT [1:0]	Serial output format	0	Pads from the beginning (initial value)
		1	Pads from the end
		2	I^2S format
		3	

COMMAND-44h (RUN-MUTE) 0100 0100

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	RUN	0	DF MUTE	DA MUTE	IMUTE	SO-MUTE	OMUTE 1	OMUTE 0

Name	Description	Value	Operation
RUN	ASP program execution	0	Stops program (initial value).
		1	Runs program.
DF MUTE	DF block mute	0	Mute off
		1	Mute on (initial value)
DA MUTE	DAC mute (all four channels)	0	Mute off
		1	Mute on (initial value)
IMUTE	ASP block input mute (SI0, SI1)	0	Mute off
		1	Mute on (initial value)
SO-MUTE	ASP block serial output mute (Mutes DOUT output whichever register is selected in CHSO.)	0	Mute off
		1	Mute on (initial value)
OMUTE 1	ASP block output mute (SO1)	0	Mute off
		1	Mute on (initial value)
OMUTE 0	ASP block output mute (SO0)	0	Mute off
		1	Mute on (initial value)

COMMAND-45h (MSEQ) 0100 0101

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

Name	Description	Value	Operation
MSA [9:0]	Sequential RAM address	000h ~ 3FFh	Set sequential RAM. Enable a sequential write to RAM.

COMMAND-46h (MSEQ) 0100 0110

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Name	Description	Value	Operation
D [15:0]	CRAM	0000h ~ FFFFh	Set CRAM. Enable a sequential write to RAM.

COMMAND-47h (CRAM-ACMP) 0100 0111

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Name	Description	Value	Operation
D [15:0]	CRAM-ACMP	0000h ~ FFFFh	Set CRAM in ACMP mode.

COMMAND-48h (OFRAM) 0100 1000

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Name	Description	Value	Operation
D [15:0]	OFRAM	0000h ~ FFFFh	Set OFRAM. Enable a sequential write to RAM.

COMMAND-49h (OFRAM-ACMP) 0100 1001

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Name	Description	Value	Operation
D [15:0]	OFRAM-ACMP	0000h ~ FFFFh	Set OFRAM in ACMP mode.

COMMAND-4Ah (IFF) 0100 1010

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0	0	IFF2	IFF1	IFF0

Name	Description	Value	Operation
IFF [2:0]	Interface flag (IFF)	0	IFFn = 0 (initial value)
		1	IFFn = 1

COMMAND-4Bh (MONI-PC) 0100 1011

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
I2COS 1	I2COS 0	0	0	0	0	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

Name	Description	Value	Operation
I2COS [1:0]	Monitor data length in I^2C mode	0h ~ 3h	Set the data byte length when monitoring in I^2C mode. (3 = 3 byte, 2 = 2 byte, 1 or 0 = 1 byte)
A [9:0]	Monitor conditions (PC: program counter)	000h ~ 3FFh	Set the PC conditions when monitoring.

COMMAND-4Ch (MONI-LC) 0100 1100

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	LCE	LCS	LCDE	LCA7	LCA6	LCA5	LCA4	LCA3	LCA2	LCA1	LCA0

Name	Description	Value	Operation
LCE	Adds the LC (loop counter) value to the monitor conditions.	0	Does not add LC value to the conditions (initial value).
		1	Adds LC value to the conditions.
LCS	LC selection	0	Compares with LC0 value.
		1	Compares with LC1 value.
LCDE	Automatic LC decrement	0	After a match, does not change the value to be compared with the LC.
		1	After a match, automatically decrements by 1 the value to be compared with the LC.
LCA [7:0]	Monitor conditions (LC)	00h ~ FFh	Set the value to be compared with the LC.

COMMAND-4Dh (MISC) 0100 1101

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	SIS	SOS	ERDET	ZST	DP7F	SYRC	SYRO	MCKE	MCKS	DLSEP	DLAC4

Name	Description	Value	Operation
SIS	Serial input	0	Master (LRCK = FS, BCK = FSxx) (initial value)
		1	Slave (LRCK = ELRI, BCK = EBCI)
SOS	Serial output	0	Master (LRCK = FS, BCK = FSxx) (initial value)
		1	Slave (LRCK = ELRO, BCK = EBCO)
ERDET	Error detection	0	Invalid
		1	Valid (initial value)
ZST	Switches to access CROM using LOG-LIN adjustment.	0	2-cycle access
		1	1-cycle access (initial value)
DP7F	DATA-RAM 128/256 word switching	0	256 words (initial value)
		1	128 words
SYRC	Initializes CP at each SYNC.	0	Does not initialize.
		1	Initializes (initial value).
SYRO	Initializes OFP at each SYNC	0	Does not initialize.
		1	Initializes (initial value).
MCKE	MCK pin output enable	0	Fixes to L
		1	Output (initial value)
MCKS	MCK pin output switching	0	256 fs
		1	When STEP1 pin = 0, outputs source oscillation (initial value). When STEP1 pin = 1, used for testing.
DLSEP	Delay RAM table area switching	0	Does not use table.
		1	Uses 2-k word area as the table (initial value).
DLAC4	Delay RAM access method	0	One access/6 cycles (initial value)
		1	One access/4 cycles

COMMAND-4Fh (M-RST) 0100 1111

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MRST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Name	Description	Value	Operation
MRST	Initialization from the microcontroller	0	Does not initialize.
		1	Initializes (after initialization, automatically set to 0).

COMMAND-50h (MON-DB) 0101 0000

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Name	Description	Value	Operation
D [23:0]	Data bus monitor	000000h~FFFFFFh	Reads data bus on the condition CMD: 4Bh, 4Ch.

COMMAND-51h (MON-CP) 0101 0001

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CP8	CP7	CP6	CP5	CP4	CP3	CP2	CP1	CP0

Name	Description	Value	Operation
CP [8:0]	CP monitor	000000h~00013h	Reads CP on the condition CMD: 4Bh, 4Ch.

COMMAND-52h (MON-OFP) 0101 0010

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	OFP 5	OFP 4	OFP 3	OFP 2	OFP 1	OFP 0

Name	Description	Value	Operation
OFP [5:0]	OFP monitor	000000h~00003h	Reads OFP on the condition CMD: 4Bh, 4Ch.

COMMAND-53h (MON-BP) 0101 0011

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0	BP 11	BP 10	BP 9	BP 8	BP 7	BP 6	BP 5	BP 4	BP 3	BP 2	BP 1	BP 0

Name	Description	Value	Operation
BP [11:0]	BP monitor	000000h~000FFFh	Reads BP on the condition CMD: 4Bh, 4Ch.

COMMAND-54h (MON-AR) 0101 0100

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0	AR 11	AR 10	AR 9	AR 8	AR 7	AR 6	AR 5	AR 4	AR 3	AR 2	AR 1	AR 0

Name	Description	Value	Operation
AR [11:0]	Delay RAM address monitor	000000h~000FFFh	Reads delay RAM address on the condition CMD: 4Bh, 4Ch.

COMMAND-55h (MON-CRP) 0101 0101

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRP 8	CRP 7	CRP 6	CRP 5	CRP 4	CRP 3	CRP 2	CRP 1	CRP 0

Name	Description	Value	Operation
CRP [8:0]	CRP (LIN-LOG adjustment pointer) monitor	000000h~0001FFh	Reads CRP on the condition CMD: 4Bh, 4Ch.

COMMAND-56h (MON-SR) 0101 0110

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	LRF	GF3	GF2	GF1	GF0	LI LG	LG LI	OV 1E	OV 0E	RD 24	RD 16	V1F	V0F	ZF	SF

Name	Description	Value	Operation
SR	SR (status register) monitor	—	Reads SR on the condition CMD: 4Bh, 4Ch.

4. Self-boot function description

(1) Self-boot function

The TC9447F supports a self-boot function for setting coefficients and offsets. As Figure 1 shows, the data are set via the microcontroller interface circuit.
First saving the data to be set via the microcontroller in the self-boot ROM (SBROM) allows various modes to be set later. The microcontroller interface circuit supports two formats: I^2C and the original mode. However, the boot must be executed in Standard Transmission (the original) mode.

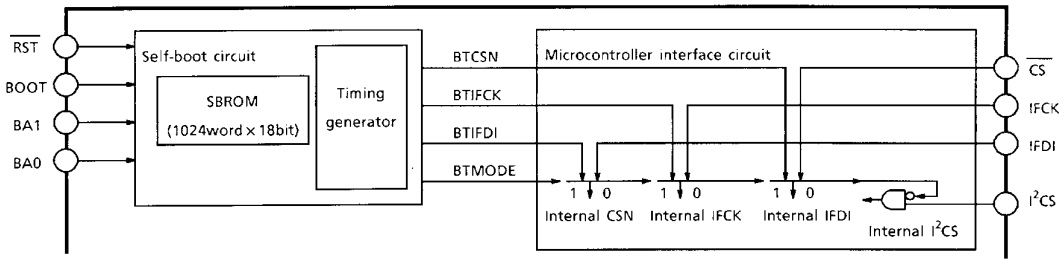


Figure 1 Self-boot system

(2) Boot ROM format

The following shows the breakdown of the 18 bits.

00	Data that are being sent
01	Command
10	Final data (after the data are sent, the $\overline{CS}$ signal is set to "H").
11	Jump address (jump to any address in the self-boot ROM).

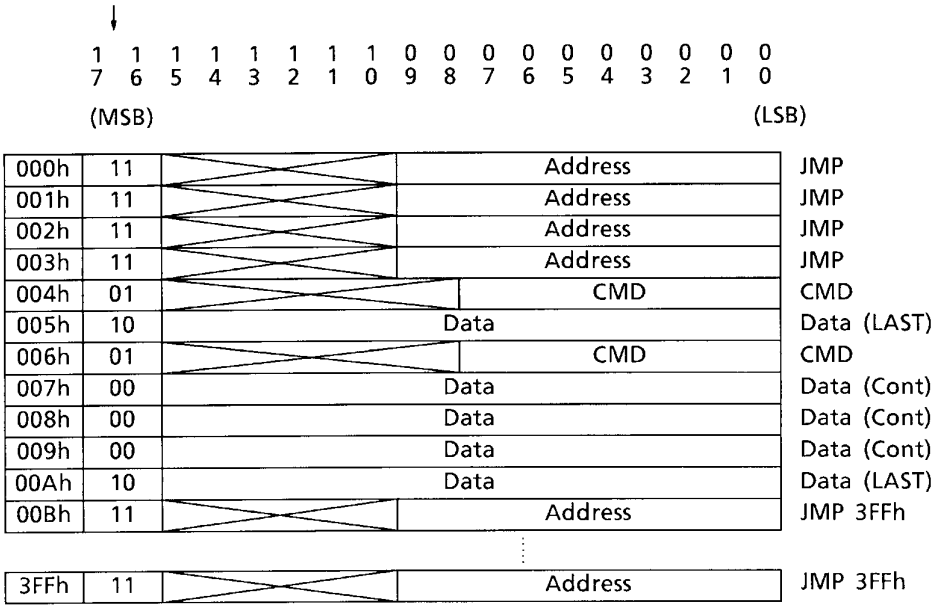


Figure 2 Boot ROM Format and Example

Boot mode completes when the address reaches 3FFh, the maximum value.
Therefore, for the final address, write JMP 3FFh (data = 303FFh).

(3) Self-boot operation

Self-boot operations support two modes: one for use at reset and one for setting the microcontroller. The modes can be used in combination.

(3-1) Self-boot operation at reset

To enter this mode, set the BOOT pin to High, then set the $\overline{RST}$ pin from Low to High. The 2048 fs period (46.4 ms when fs = 44.1 kHz) after a reset release is a wait period (for power-on reset). The boot operation starts at the end of this period.

When switching the setting according to the application, specify the start address using the BA [1:0] pin. At addresses 000h to 002h, set jump addresses.

The data setting speed is one word of SBROM per 1 fs. As up to 1024 words can be set in the SBROM, the maximum time required for setting the data is half of the wait period.

Table 2 Relationship between fs and wait period

fs	Wait Period	Boot Time (Maximum)
32 kHz	64.0 ms	32.0 ms
44.1 kHz	46.4 ms	23.2 ms
48 kHz	42.7 ms	21.3 ms

Table 3 Relationship between BA [1:0] pin value and start address

BA1	BA0	Start Address
0	0	000h
0	1	001h
1	0	002h
1	1	003h

(3-2) Self-boot operation when setting microcontroller

In this mode, the microcontroller can specify any address and the operation starts from that address. The BOOT pin can be set to either High or Low. Setting the self-boot ROM start address using the BOOT command (CMD: 41h) from the microcontroller starts the boot operation with no wait.
The boot operation when set from the microcontroller is the same as the self-boot operation at reset except that the boot operation can start from any address.

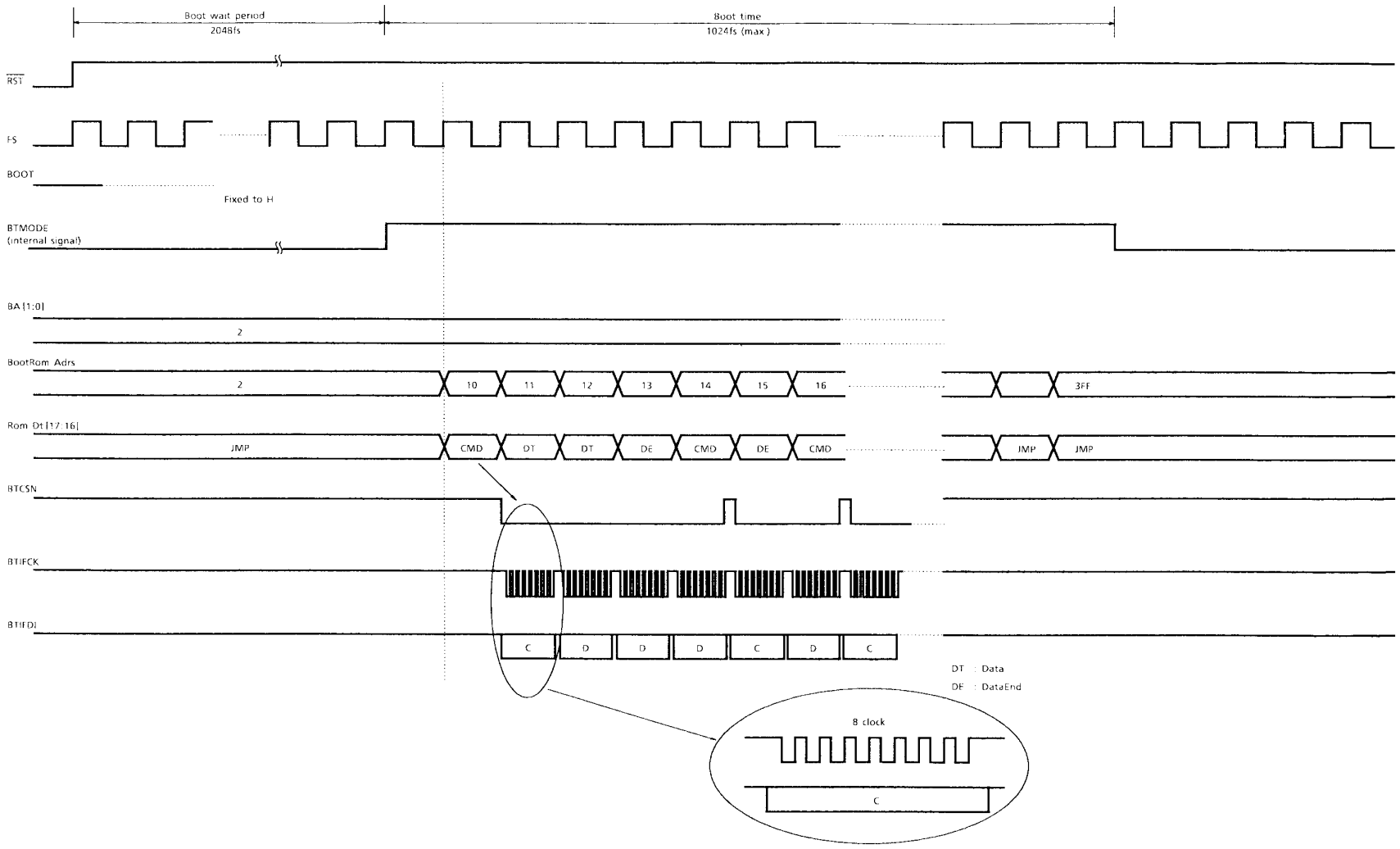


Figure 3 Boot timing chart (at reset)

Table 4 Differences depending on operating mode

Parameter	Boot Mode at Reset	Boot Mode Set from Microcontroller
Boot wait period	Yes	No
Boot start address	Select from 000h to 003h	Any address specified from microcontroller
Boot pin	"H" level	Don't care

(4) Programming examples

```
000:30040h    jmp  040h    ; Jump to 040h
001:30100h    jmp  100h    ; Jump to 100h
002:30200h    jmp  200h    ; Jump to 200h
003:30004h    jmp  004h    ; Jump to 004h
004:10040h    cmd  40h     ; Command 40h (TIMING)
005:28007h    data 8007h   ; CKOS0 = 7 (fs 128 output)
006:10043h    cmd  43h     ; Command 43h (SI0)
007:20039h    data 0039h   ; CHSO = 0 (SO0), OSLT = 3 (32 bits), OBCS = 2 (20 bits),
                           ; OFMT = 1 (Padded from the end)
008:10045h    cmd  45h     ; Command 45h (MSEQ)
009:00000h    data 0000h   ; Start address = 0h
00A:00001h    data 0001h   ; MSEQ [0] = 001h
00B:00123h    data 0123h   ; MSEQ [1] = 123h
00C:20320h    data 0320h   ; MSEQ [2] = 320h
00D:30300h    jmp  300h    ; Jump to 300h
   :
100:10046h    cmd  46h     ; Command 46h (CRAM)
101:00000h    data 0000h   ; Start address = 0h
102:00000h    data 0000h   ; CRAM [0] = 0000h
103:00000h    data 0000h   ; CRAM [1] = 0000h
104:00000h    data 0000h   ; CRAM [2] = 0000Fh
105:20000h    data 0000h   ; CRAM [3] = 0000h
106:30380h    jmp  380h    ; Jump to 380h
   :
300:10046h    cmd  46h     ; Command 46h (CRAM)
301:00000h    data 0000h   ; Start address = 0h
302:07FFFh    data 7FFFh   ; CRAM [0] = 7FFFh
303:08000h    data 8000h   ; CRAM [1] = 8000h
304:03FFFh    data 3FFFh   ; CRAM [2] = 3FFFh
305:24000h    data 4000h   ; CRAM [3] = 4000h
306:30380h    jmp  380h    ; Jump to 380h
:
380:10046h    cmd  46h     ; Command 46h (CRAM)
381:00080h    data 0080h   ; Start address = 80h
382:0FFFEh    data FFFEh   ; CRAM [80] = FFFEh
383:2FFFFh    data FFFFh   ; CRAM [81] = FFFFh
384:303FFh    jmp  3FFh    ; Jump to 3FFh
:
3FF:303FFh    jmp  3FFh    ; Jump to 3FFh
```

It is necessary to use JMP instruction while address 000 to 003.

(5) Code format example

The following shows the format for storing data in SBROM.

```
REM TC9447F SelfBootRomData Ver1.0 ;
REM DATA : XX/XX/XX(MON)12:12:12 ;
REM VERSION : 1.10b;
REM SBROM;
MODULE:RCA018A;
WORD  :1024,HEX;
BIT   :18,HEX
DATA  :
000/30040,30100,30200,10040,28007,10043,20039,10045;
008/00000,00001,00123,20320,30300,10040,20022,303FF;
100/10046,00000,00000,00000,00000,20000,30380,00000;
     :
3F8/30380,00000,00000,00000,00000,00000,00000,303FF;
END MODULE;
END;
```

Can use a REM statement.

Do not change these.

Write data between DATA; and END MODULE;.

Completes with END; statement.

5. Cautions on use

(1) The cautions at the time of using IFOK terminal

The timing which outputs IFOK signal is the signal which shows whether the command received from the microcomputer was performed normally.
Since the initial value of IFCK signal is unfixed when a control microcomputer is checking IFOK signal, before sending a command, it may stop performing control from a microcomputer.

(2) The cautions at the time of using ACMP (address comparing mode)

In rewriting coefficient data and offset data using ACMP mode, please do not use it the following condition.

(2-1) Please do not transmit the following command before completing rewriting of data.

Please do not send the following command before completing rewriting of data of CRAM or OFRAM.
Please check that waiting the term after rewriting of data is completed until it transmits the following command was carried out, or rewriting has been completed using IFOK signal.

(2-2) Please do not include data of an intact address.

Please do not include coefficient data of offset data of an address which are not used by the program under execution, into transmitting data.
When data of an intact address is contained, operation in ACMP mode cannot be ended.
If the following command is transmitted in this state, RAM data will become unfixed also by the command with the command unrelated to CRAM or OFRAM.
It needs to reset and all data needs to be re-set up to interrupt before completing rewriting of data in the rewriting processing.

(2-3) Please do not perform continuation transmission over the 0th address.

The transmission over the 0th address may incorrect-operate.
The same of this restriction is said not only of ACMP mode but continuation transmission of usual RAM data.
For example, when writing in 007h from 1BFh and 000h from 1B8h of CRAM, it must transmit in 2 steps.

(3) The following cautions are required when transmitting a reset command and a boot command in the cautions I^2C bus mode at the time of using the I^2C bus mode.

(3-1) At the time of reset command use

When transmitting a reset command (4Fh: M-RST) from a microcomputer, the acknowledgement signal in front of the end conditions outputted from IFDI terminal is not transmitted to a microcomputer.
Therefore, the acknowledgement signal of the last of IFDI signal should repeal at the time of reset command transmission.
The timing at the time of reset command transmission is shown if Figure 4.

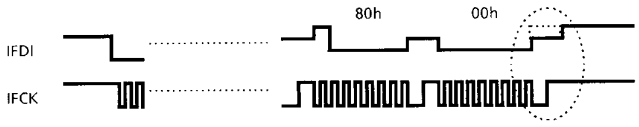


Figure 4 Timing at the time of command transmission

(3-2) At the time of self boot command use

When a self boot command (41h: BOOT) is transmitted, even if end conditions happen to the acknowledgement signal of the last of boot command data, please repeal.
If it becomes the boot mode, data will be transmitted internal boot ROM data using the internal circuit of a microcomputer interface.
Data is transmitted not in the I^2C bus mode but in the standard transmitting mode at the time of boot mode operation in that case.
Therefore, IFDI terminal will be in the state of H level, and operation of an I^2C bus and conditions may not be performed normally.
The timing at the time of self boot command transmission is shown if Figure 5.

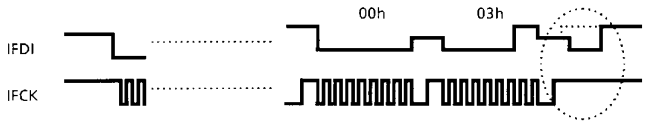
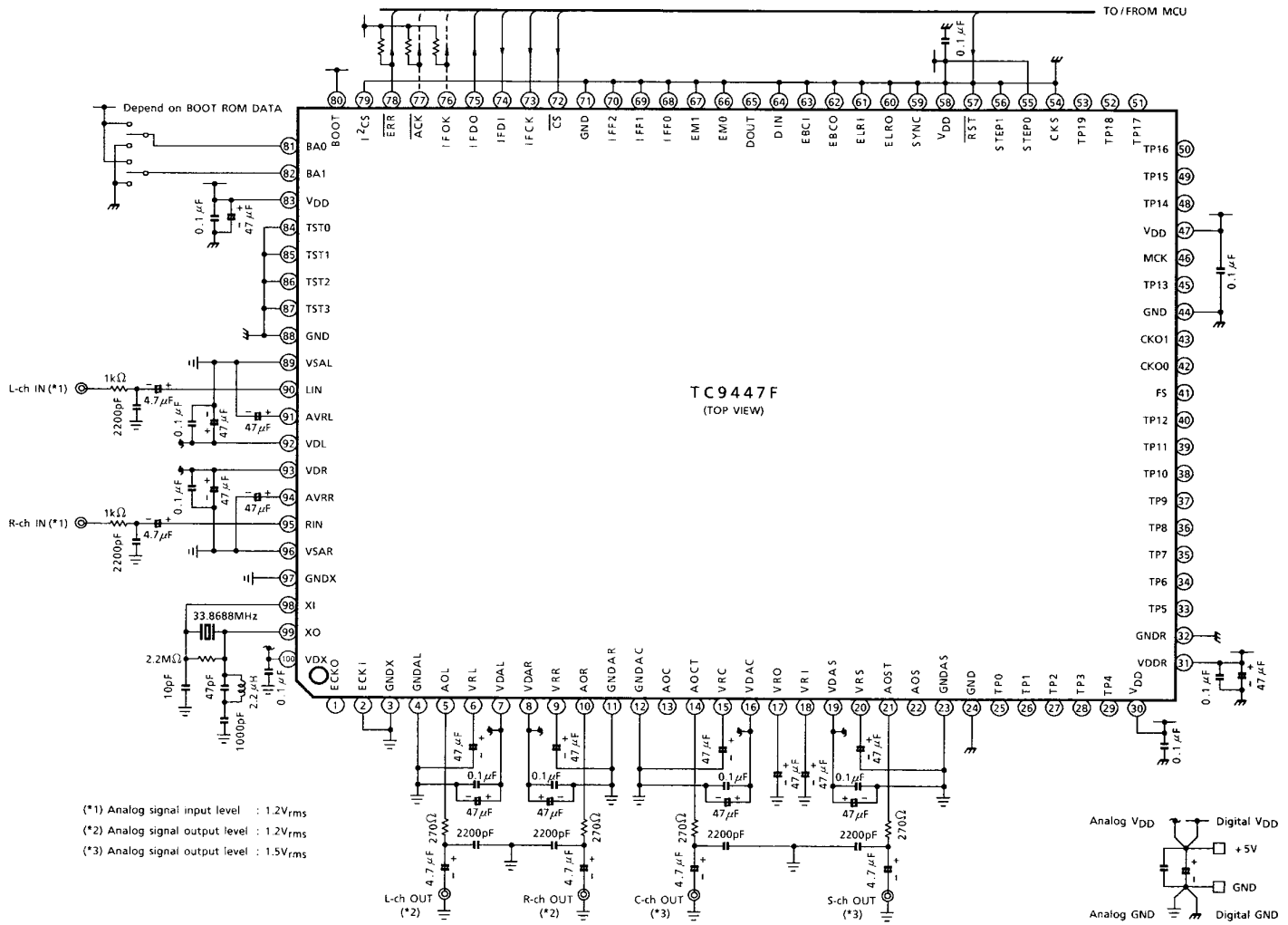


Figure 5 Timing at the time of self boot command transmission

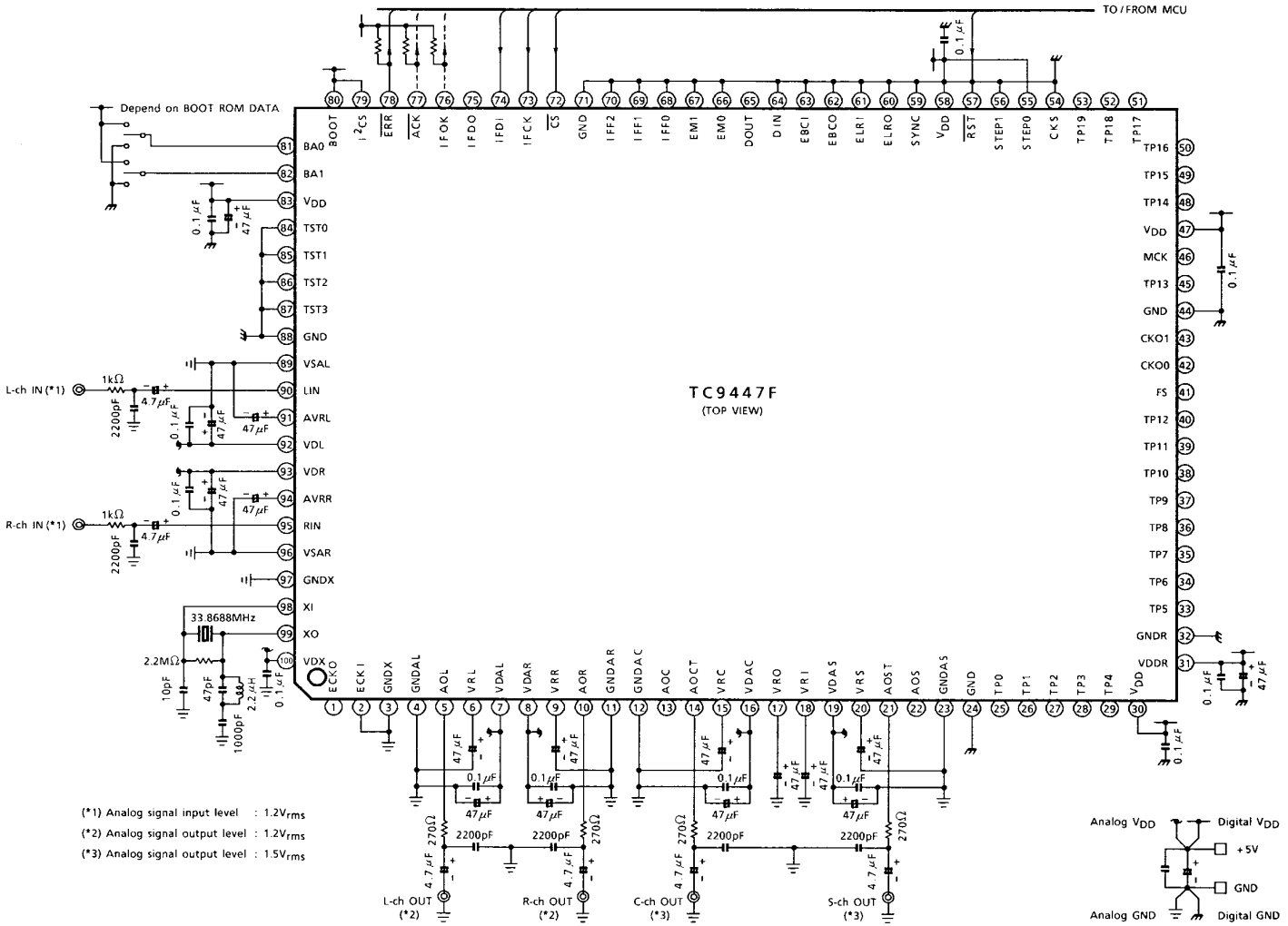
Peripheral Circuit Example 1 (standard transmission mode)

The circuit below is an example circuit only. The operation of this circuit is not guaranteed by Toshiba.



Peripheral Circuit Example 2 (I^2C bus mode)

The circuit below is an example circuit only. The operation of this circuit is not guaranteed by Toshiba.



Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{DD}	−0.3~6.0	V
Input voltage	V_{IN}	−0.3~V_{DD} + 0.3	V
Power dissipation	P_D	1500	mW
Operating temperature	T_{opr}	−40~75 (Note 3)	°C
Storage temperature	T_{stg}	−55~150	°C

Note 3: Only when frequency of operation is 340 step mode, a temperature of operation becomes Ta = −40~85°C.

Electrical Characteristics
(unless otherwise noted, Ta = 25°C, $V_{DD} = V_{DX} = V_{DDR} = V_{DL} = V_{DR} = V_{DAL} = V_{DAR} = V_{DAC} = V_{DAS}$ = 5 V)

DC characteristics

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Operating power supply voltage	V_{DD}	—	Ta = −40~75°C	4.5	5.0	5.25	V
Operating frequency range	f_{opr}	—	340-step mode	8	15	25	MHz
			511-step mode	12	33.8	34	
Operating power supply current	I_{DD}	—	f_{opr} = 33.8688 MHz 511-step mode	—	135	140	mA

Clock pins (XI, XO, ECKI, ECKO)

Characteristics		Symbol	Test Circuit	Test Condition		Min	Typ.	Max	Unit
Input voltage (1)	"H" level	V_{IH1}	—	XI, ECKI pin		3.5	—	—	V
	"L" level	V_{IL1}	—			—	—	1.5	
Output voltage (1)	"H" level	V_{OH1}	—	I_{OH} = −3.0 mA	XO, ECKO pin	4.5	—	—	V
	"L" level	V_{OL1}	—	I_{OL} = 5.0 mA		—	—	0.5	
Pull-down resistance		R_{XD}	—	XI, ECKI pin		—	3.0	5.0	kΩ

Input pins

Characteristics		Symbol	Test Circuit	Test Condition		Min	Typ.	Max	Unit
Input voltage (2)	"H" level	V_{IH2}	—	(Note 4)		4.2	—	—	V
	"L" level	V_{IL2}	—			—	—	0.8	
Input leakage current	"H" level	I_{IH2}	—	$V_{IN} = V_{DD}$	(Note 4)	—	—	10	μA
	"L" level	I_{IL2}	—	V_{IN} = 0 V		−10	—	—	
Threshold voltage	"H" level	V_P	—	(Note 5)		—	2.8	—	V
	"L" level	V_N	—			—	2.0	—	
Hysteresis voltage		V_H	—	(Note 5)		—	0.8	—	V

Note 4: CKS, STEP0, STEP1, $\overline{RST}$, SYNC, ELRO, ELRI, EBCO, EBCI, DIN, EM0, EM1, I^2CS, $\overline{CS}$, IFCK, IFDI, BOOT, BA0, BA1, TST0~3 (Normally input pins and Schmitt input pins)

Note 5: Pins excluding I^2CS pins in Note 1 above (Schmitt input pins)

Output pins

Characteristics		Symbol	Test Circuit	Test Condition		Min	Typ.	Max	Unit
Output voltage (2)	"H" level	V_{OH2}	—	I_{OH} = −2.0 mA	(Note 6)	4.5	—	—	V
	"L" level	V_{OL2}	—	I_{OL} = 2.0 mA		—	—	0.5	
Output voltage (3)	"H" level	V_{OH3}	—	I_{OH} = −4.0 mA	(Note 7)	4.5	—	—	V
	"L" level	V_{OL3}	—	I_{OL} = 4.0 mA		—	—	0.5	
Output voltage (4)	"L" level	V_{OL4}	—	I_{OL} = 4.0 mA	(Note 8)	—	—	0.5	V
Output open leakage current		I_{OZ4}	—	V_{OH} = V_{DD}		—	—	±10	μA

Note 6: FS, CKO0, CKO1, MCK, DOUT (Normally output)

Note 7: IFDO (Normally output)

Note 8: IFDI (When I^2C mode output), IFOK, $\overline{ACK}$, $\overline{ERR}$ (Open drain output)

AC Characteristics (1) Analog

AD converter characteristics

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Maximum input signal level	V_i	—	Input level that ADC digital output does not overflow (Note 9)	1.13	1.20	—	Vrms
Input impedance	Z_{in}	—	LIN, RIN pins (Note 9)	—	27.0	—	kΩ
S/(N + D) ratio	S/N_{a1}	—	A-Weight, When using X'tal oscillator at 33.8688 MHz (Note 9)	90	98	—	dB
	S/N_{a2}	—	CCIR-ARM, When using X'tal oscillator at 33.8688 MHz (Note 9)	88	94	—	
THD + N	THD_a	—	20 kHz LPF, When using X'tal oscillator at 33.8688 MHz (Note 9)	—	−77	−70	dB
Crosstalk	CT_a	—	A-Weight, When using X'tal oscillator at 33.8688 MHz (Note 9)	—	−95	−88	dB
Dynamic range	DR_a	—	A-Weight, When using X'tal oscillator at 33.8688 MHz (Note 9)	—	95	90	dB

Note 9: Input channels: LIN, RIN

DA converter characteristics

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output signal level	V_{O1}	—	Output voltage at full-scale digital input (Note 10)	1.10	1.21	1.32	Vrms
	V_{O2}	—	Output voltage at full-scale digital input (Trim output) (Note 11)	1.35	1.52	1.61	
Trim output pin: attenuation level	VO_{AL}	—	(Note 11)	0	—	−20	dB
Trim output pin: step level	VO_{AS}	—	(Note 11)	—	1	—	dB
S/N ratio	S/N_d	—	A-Weight, When using X'tal oscillator at 33.8688 MHz (Note 12)	90	100	—	dB
THD+N	THD_{d1}	—	20 kHz, When using X'tal oscillator at 33.8688 MHz (Note 10)	—	−87	−80	dB
	THD_{d2}	—	20 kHz, When using X'tal oscillator at 33.8688 MHz (Note 11)	—	−82	−75	
Crosstalk	CT_d	—	A-Weight, When using X'tal oscillator at 33.8688 MHz (Note 12)	—	−95	−88	dB
Dynamic range	DR_d	—	A-Weight, When using X'tal oscillator at 33.8688 MHz (Note 12)	—	95	90	dB

Note 10: Output channel: AOL, AOR, AOC, AOS

Note 11: Output channel: AOCT, AOST

Note 12: Output channel: AOL, AOR, AOC, AOS, AOCT, AOST

AC Characteristics (2) Timing

Clock input pins (XI, ECKI)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Clock cycle	t_{XI}	—	—	29	—	—	ns
Clock “H” cycle width	t_{XIH}	—	—	—	14.5	—	ns
Clock “L” cycle width	t_{XIL}	—	—	—	14.5	—	ns

Reset pin ($\overline{RST}$)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Standby time	t_{RRS}	—	—	10	—	—	ms
Reset pulse width	t_{WRS}	—	—	1.0	—	—	μs

Timing output

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
CKO output delay time	t_{DFC}	—	—	−150	—	150	ns

Audio serial interface (EBCI, DIN, EBCO, DOUT)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
ELRI hold time	t_{LIH}	—	C_L = 30 pF	−75	—	75	ns
DIN setup time	t_{SDI}	—	C_L = 30 pF	50	—	—	ns
DIN hold time	t_{HDI}	—	C_L = 30 pF	50	—	—	ns
EBCI clock cycle	t_{EBCI}	—	C_L = 30 pF	300	—	—	ns
EBCI clock “H” cycle width	t_{EBIH}	—	C_L = 30 pF	150	—	—	ns
EBCI clock “L” cycle width	t_{EBIL}	—	C_L = 30 pF	150	—	—	ns
ELRO hold time	t_{LOH}	—	C_L = 30 pF	−75	—	75	ns
DOUT output delay time (1)	t_{DO1}	—	C_L = 30 pF	—	—	60	ns
DOUT output delay time (2)	t_{DO2}	—	C_L = 30 pF	—	—	60	ns
EBCO clock cycle	t_{EBCO}	—	C_L = 30 pF	300	—	—	ns
EBCO clock “H” cycle width	t_{EBOH}	—	C_L = 30 pF	150	—	—	ns
EBCO clock “L” cycle width	t_{EBOL}	—	C_L = 30 pF	150	—	—	ns

Microcontroller Interface

Standard transmission mode ($\overline{CS}$, IFCK, IFDI, IFDO, $\overline{ACK}$)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Standby time	t_{STB}	—		1.0	—	—	μs
$\overline{CS}$ ↓ - IFCK↓ Setup time (Mode 1)	t_{CCD}	—		0.5	—	—	μs
IFCK "L" cycle width	t_{WLC}	—		0.5	—	—	μs
IFCK "H" cycle width	t_{WHC}	—		0.5	—	—	μs
IFCK↑ - $\overline{CS}$ ↑ Setup time	t_{CKC}	—		0.5	—	—	μs
$\overline{CS}$ "H" cycle width	t_{WCS}	—	(Note 13)	1.0	—	—	μs
IFCK↑ - $\overline{CS}$ ↑ Setup time (Mode 2)	t_{CCU}	—		0.5	—	—	μs
IFCK↓ - $\overline{CS}$ ↓ Setup time	t_{SCK}	—		0.5	—	—	μs
IFDI - IFCK↑ Setup time	t_{SCD}	—		0.5	—	—	μs
IFCK↑ - IFDI Hold time	t_{HCD}	—		0.5	—	—	μs
IFCK↓ - IFDO Propagation delay time	t_{DDO}	—	C_L = 30 pF	—	—	0.5	μs
IFCK↑ - $\overline{ACK}$ ↓ Propagation delay time	t_{DAKD}	—	C_L = 30 pF (Pull-up resistor) R_L = 1 kΩ	—	—	0.5	μs
IFCK↓ - $\overline{ACK}$ ↑ Propagation delay time	t_{DAKZ}	—	C_L = 30 pF (Pull-up resistor) R_L = 1 KΩ	—	—	0.5	μs

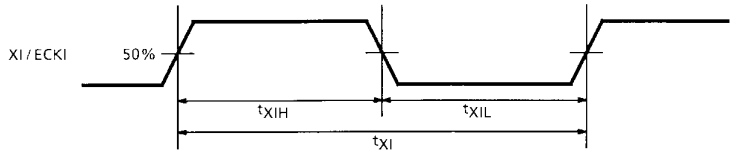
Note 13: The command which is "Sync" in the transfer Sync with Sync signal of a 17 page table 1 control command table needs to set the $\overline{CS}$ = H section to a minimum of 1 fs more until it transmits the following command.(It needs more than 22.68 μs at fs = 44.1 kHz)

I^2C mode ($\overline{CS}$, IFCK, IFDI)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
IFCK clock frequency	f_{IFCK}	—	C_L = 400 pF	0	—	400	kHz
IFCK "H" cycle width	t_H	—	C_L = 400 pF	0.6	—	—	μs
IFCK "L" cycle width	t_L	—	C_L = 400 pF	1.3	—	—	μs
Data setup time	t_{DS}	—	C_L = 400 pF	0.1	—	—	μs
Data hold time	t_{DH}	—	C_L = 400 pF	0	—	—	μs
Transmission start condition hold time	t_{SCH}	—	C_L = 400 pF	0.6	—	—	μs
Repeat transmission start condition setup time	t_{SCS}	—	C_L = 400 pF	0.6	—	—	μs
Transmission end condition setup time	t_{ECS}	—	C_L = 400 pF	0.6	—	—	μs
Data transmission interval	t_{BUF}	—	C_L = 400 pF	1.3	—	—	μs
I^2C rise time	t_R	—	C_L = 400 pF	—	—	0.3	μs
I^2C fall time	t_F	—	C_L = 400 pF	—	—	0.3	μs

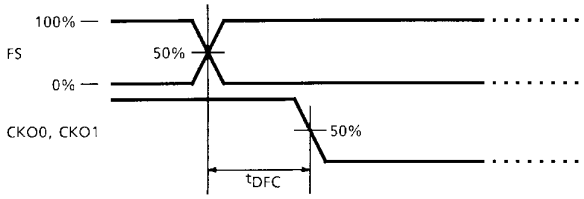
AC Characteristics Test Points

1. Clock pins (XI, ECKI)

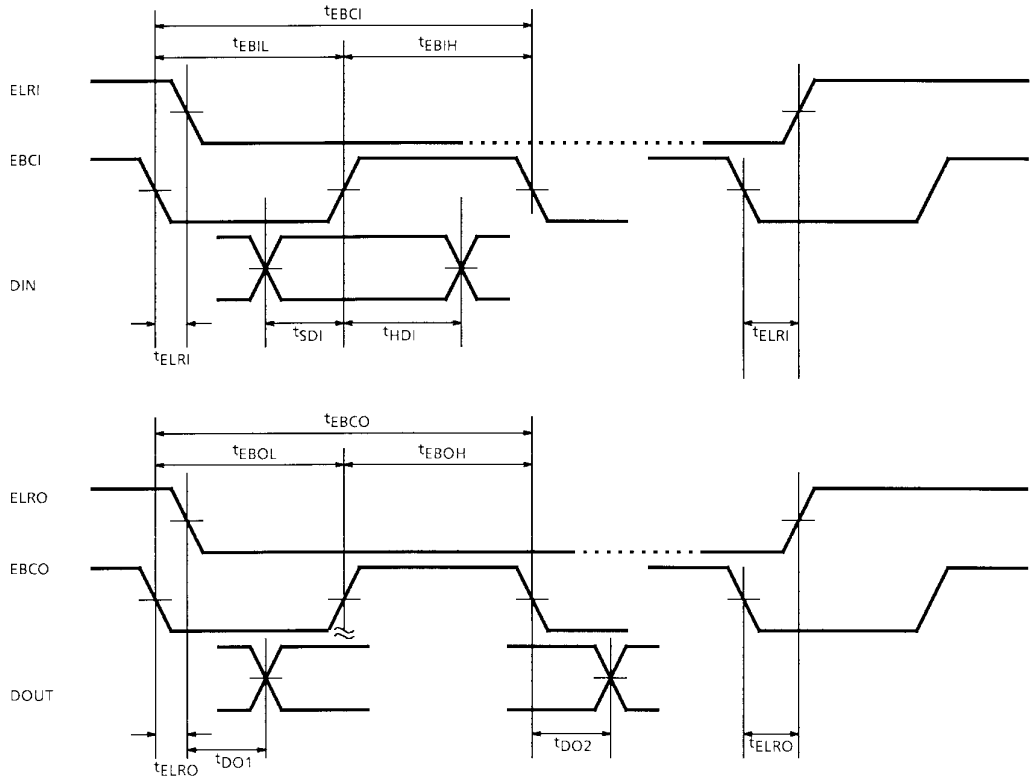


2. Reset

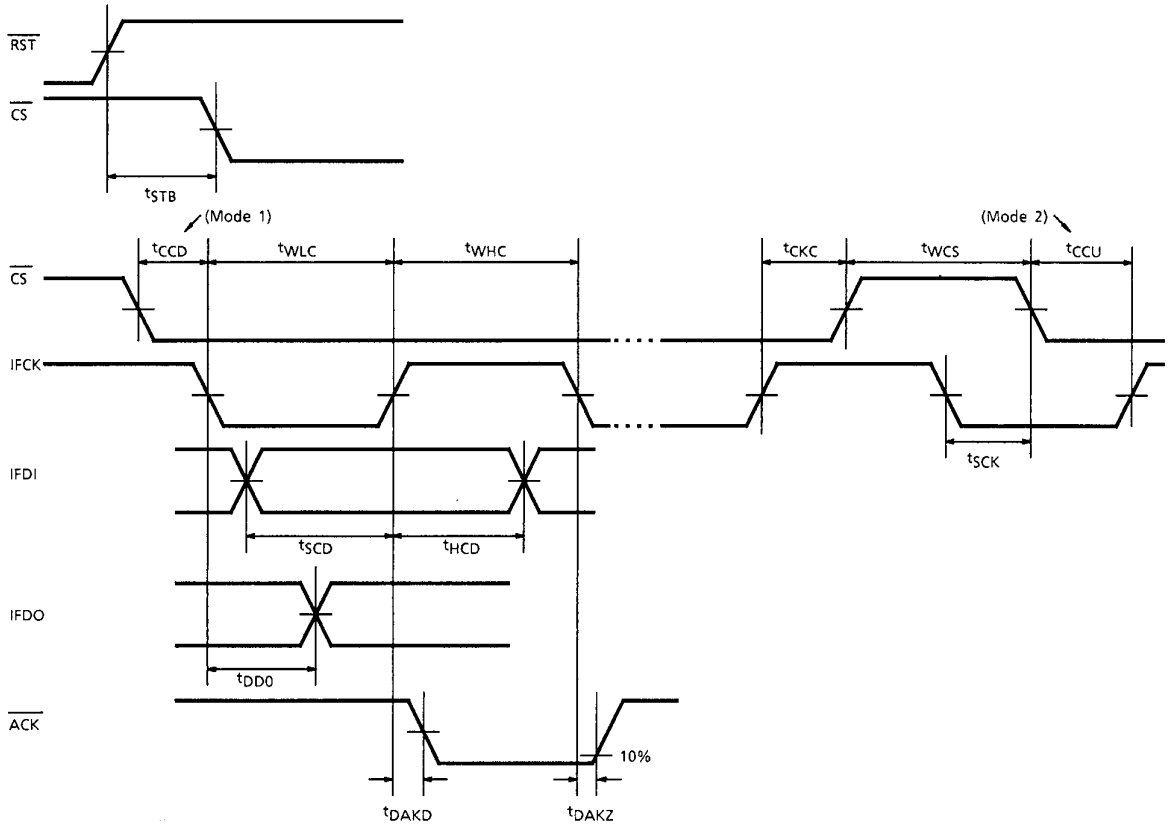
3. Timing output



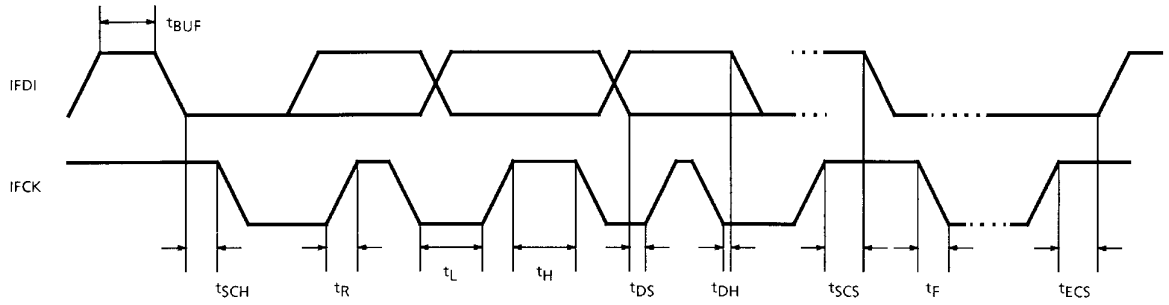
4. Audio serial interface (ELRI, EBCI, DIN, ELRO, EBCO, DOUT)



5. Microcontroller interface in standard transmission mode ($\overline{CS}$, IFCK, IFDI, IFDO, $\overline{ACK}$)



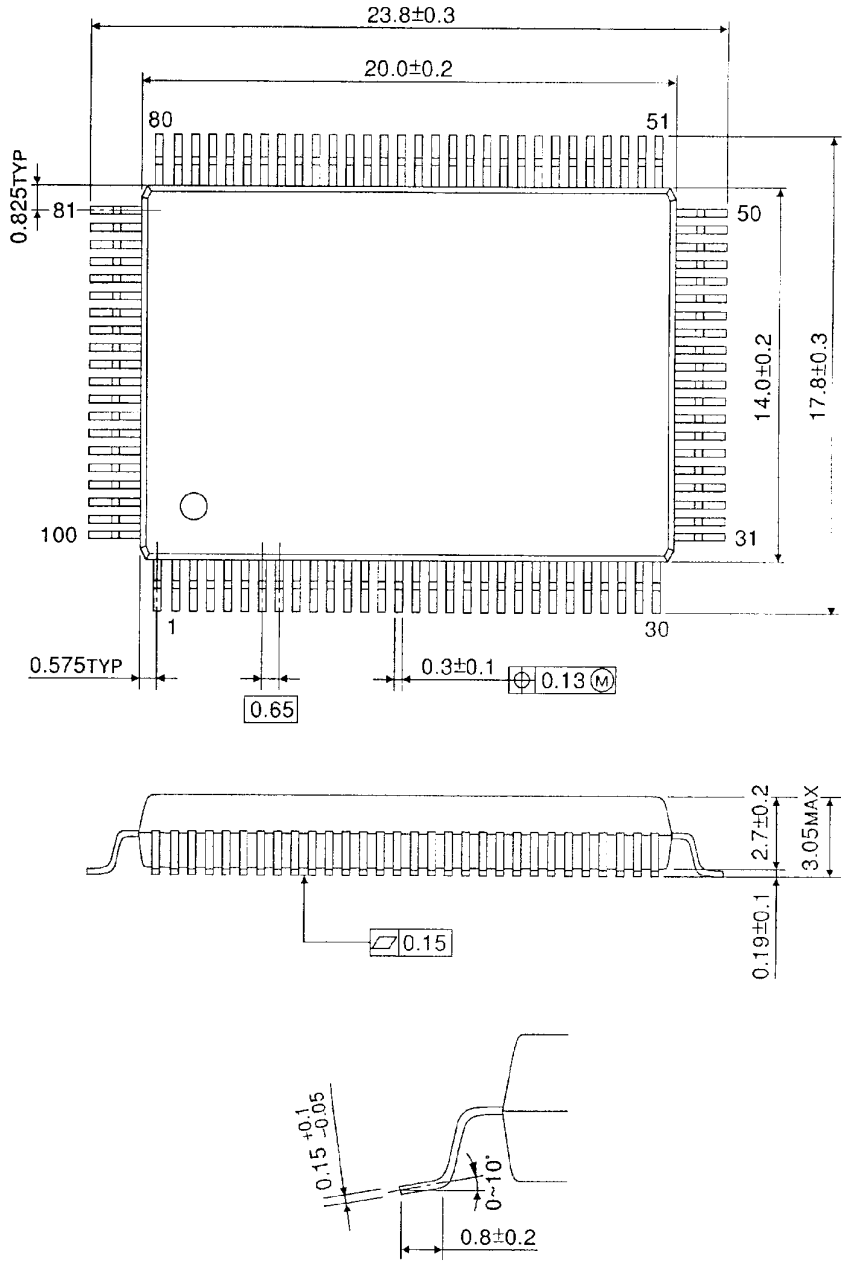
6. Microcontroller interface in I^2C mode (IFCK, IFDI)



Purchase of TOSHIBA I^2C components conveys a license under the Philips I^2C Patent Right to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by Philips.

Package Dimensions

QFP100-P-1420-0.65A Unit : mm



Weight: 1.57 g (typ.)

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000707EBA

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