TOSHIBA CMOS Digital Integrated Circuit   Silicon Monolithic
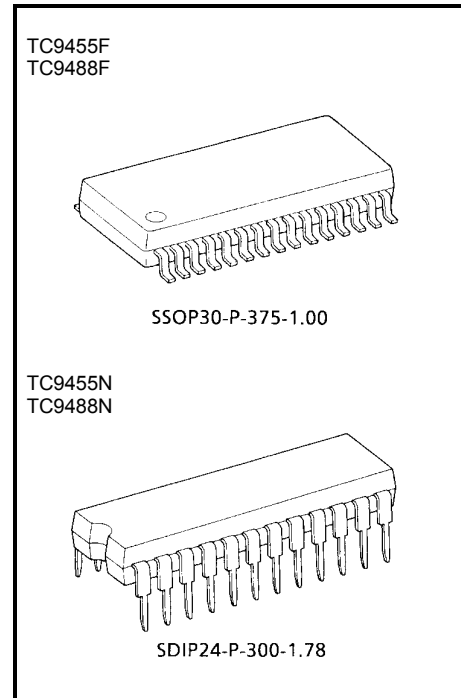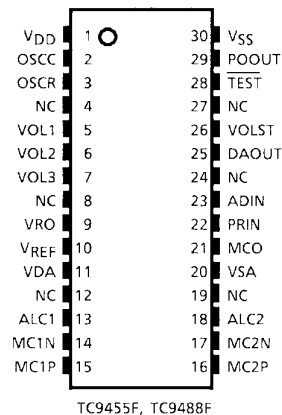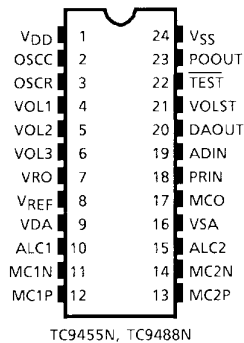
TC9455F,TC9455N,TC9488F,TC9488N

Digital Echo IC for Karaoke

The TC9455 series are digital echo ICs for karaoke. The ICs incorporate microphone amps and volume controllers, enabling a digital echo system to be configured on a single chip.
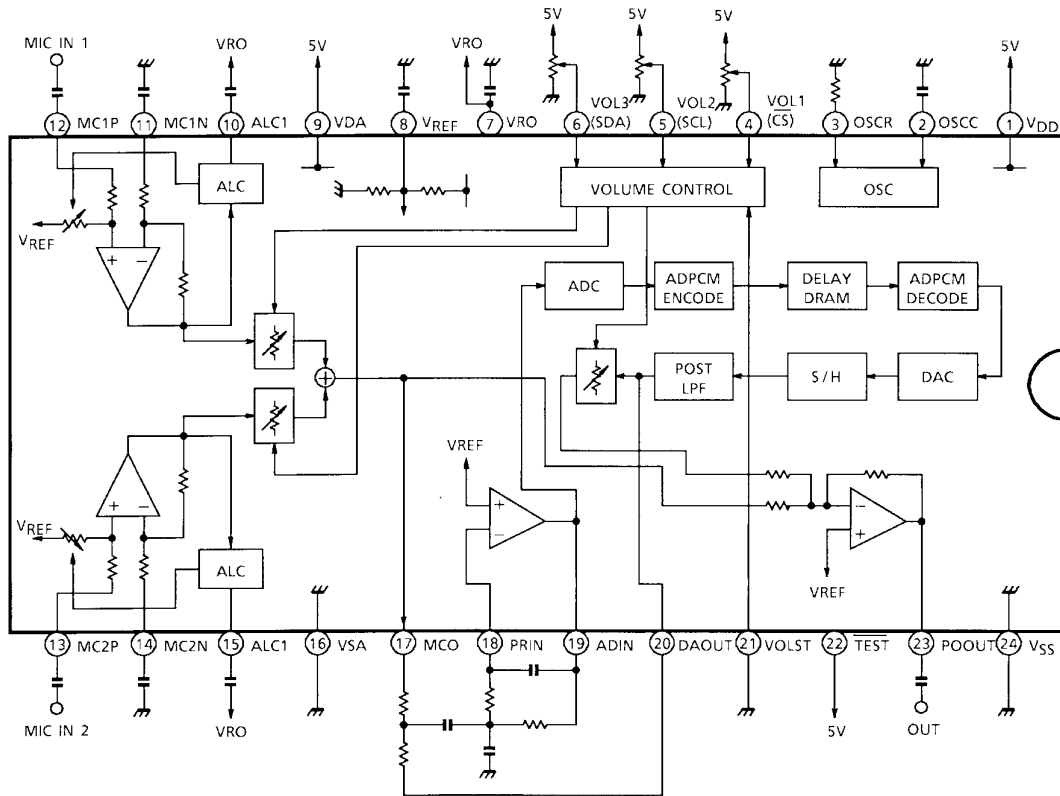
Features

- Incorporates a two-channel microphone amp with auto level control (ALC), AD/DA converter, delay memory, and electronic volume controllers.
- Incorporates a 32-kHz sampling, 12-bit successive comparison AD/DA converter.
- Incorporates a delay memory (16-Kbit DRAM) which enables 128-ms (typ.) delay.
- Microphone and echo levels are controlled by built-in volume controllers. They are controlled either by DC voltage or controlled in serial by the MCU.

    TC9455F/N: Supports I^2C bus interface
    TC9488F/N: Supports three-lead interface

- The system clock is generated by the CR oscillator circuit.
- The echo feedback amount is configured using analog circuits. The feedback level can be freely set.
- The IC comes in 30-pin flat package or 24-pin shrink DIP.

TC9455F
TC9488F
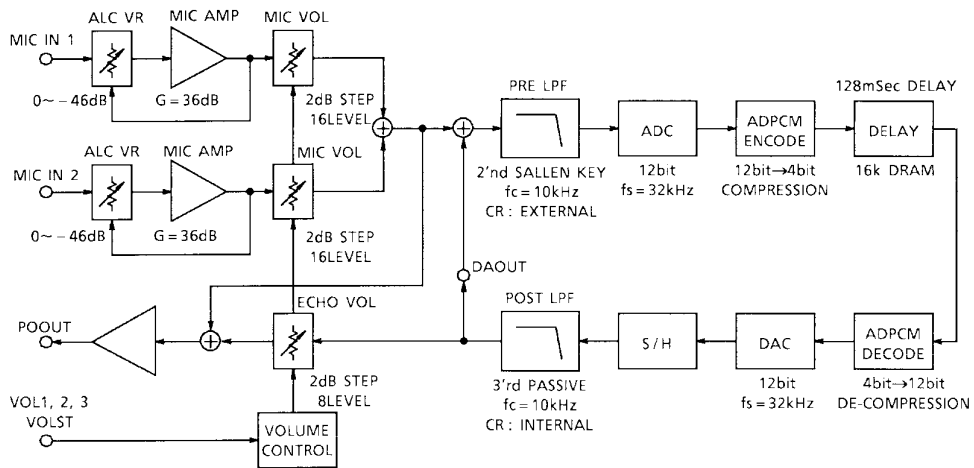
SSOP30-P-375-1.00

TC9455N
TC9488N

SDIP24-P-300-1.78

Weight:
SSOP30-P-375-1.00: 1.08 g (typ.)
SDIP24-P-300-1.78: 1.2 g (typ.)

Pin Connection

V_{DD}	1	24 V_{SS}
OSCC	2	23 POOUT
OSCR	3	22 $\overline{TEST}$
VOL1	4	21 VOLST
VOL2	5	20 DAOUT
VOL3	6	19 ADIN
VRO	7	18 PRIN
V_{REF}	8	17 MCO
VDA	9	16 VSA
ALC1	10	15 ALC2
MC1N	11	14 MC2N
MC1P	12	13 MC2P

TC9455N, TC9488N

V_{DD}	1	30 V_{SS}
OSCC	2	29 POOUT
OSCR	3	28 $\overline{TEST}$
NC	4	27 NC
VOL1	5	26 VOLST
VOL2	6	25 DAOUT
VOL3	7	24 NC
NC	8	23 ADIN
VRO	9	22 PRIN
V_{REF}	10	21 MCO
VDA	11	20 VSA
NC	12	19 NC
ALC1	13	18 ALC2
MC1N	14	17 MC2N
MC1P	15	16 MC2P

TC9455F, TC9488F

Block Diagram

System Block Diagram

Pin Description (Note 1)

Pin Number TC9455N TC9488N	Pin Number TC9455F TC9488F	Symbol	I/O	Function	Remarks
1	1	V_{DD}	—	Digital supply voltage pin	
2	2	CSCC	I	Capacitor connecting pin for CR oscillator (C = 68 pF)	
3	3	OSCR	I	Resistor connecting pin for CR oscillator (R = 5.6 kΩ)	
4	5	VOL1 ($\overline{CS}$)	I	When VOLST = "H" level, $\overline{CS}$ signal input pin When VOLST = "L" level, DC control pin for MIC1 volume	
5	6	VOL2 (SCL)	I	When VOLST = "H" level, clock input pin When VOLST = "L" level, DC control pin for MIC2 volume	Open drain output
6	7	VOL3 (SDA)	I	When VOLST = "H" level, data input pin When VOLST = "L" level, DC control pin for echo volume	Open drain output
7	9	VRO	—	Reference voltage pin	
8	10	V_{REF}	—	Reference voltage pin (1/2 V_{DD})	
9	11	VDA	—	Analog supply voltage pin	
10	13	ALC1	I	Auto level control pin 1	
11	14	MC1N	I	MIC1 feedback signal input pin	
12	15	MC1P	I	MIC1 signal input pin	
13	16	MC2P	I	MIC2 signal input pin	
14	17	MC2N	I	MIC2 feedback signal input pin	
15	18	ALC2	I	Auto level control pin 2	
16	20	VSA	—	Analog ground pin	
17	21	MCO	O	MIC addition signal output pin	
18	22	PRIN	I	Pre-filter input pin	
19	23	ADIN	I	Pre-filter output signal or DC input pin	
20	25	DAOUT	O	Post-filter output pin	
21	26	VOLST	I	Electronic volume control mode select pin When VOLST = "H" level, serial control (I^2C bus/three-lead) When VOLST = "L" level, DC level control	
22	28	$\overline{TEST}$	I	Test pin. Fix to "H" level for normal use	
23	29	POOUT	O	Microphone echo signal output pin	
24	30	V_{SS}	—	Digital ground pin	

Note 1: With the TC9455F and TC9488F, pins 4, 8, 12, 19, 24, and 27 are not connected (NC pins).
NC pins are normally open.

Operation

1. Oscillator circuit

The TC9455F/N and TC9488F/N generate an internal system clock using the CR oscillator circuit.
Connecting a capacitance (C) of 68 pF and a resistance (R) of 5.6 kΩ sets the oscillator frequency to approx. 4 MHz and the sampling frequency to 32 kHz.
Varying the external capacitance enables the oscillator frequency and sampling frequency for the system clock to be adjusted. Varying the system clock enables the delay time to be adjusted.
Figure 1 shows the CR oscillator circuit.

1.1 How to determine oscillator frequency (f)

$$f \,[\text{MHz}] = 1532/(C \,[\text{pF}] \times R \,[\text{k}\Omega])$$
$$= 1532/(68 \times 5.6)$$
$$\approx 4.0 \text{ MHz (Note 2)}$$

Note 2: The oscillator frequency is a typical value (Ta = 25°C). Set the resistance to between 4.7 kΩ and 6.8 kΩ.

1.2 How to determine sampling frequency (fs)

$$fs \,[\text{kHz}] = f/128$$
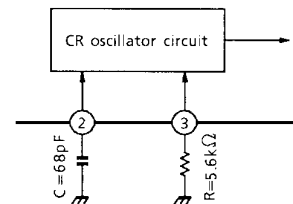$$= 4.0/128$$
$$\approx 32 \text{ kHz}$$

Figure 1
CR Oscillator circuit

2. Microphone amps

The IC incorporates microphone amps with auto level control (ALC).
The microphone amp gain is typically 36dB.
When a signal from 0 to −46dB is input, the ALC circuit can control the output signal level.
Changing the external capacitor connected to the ALC circuit to a resistor sets the ALC circuit to off.
Figure 2 shows the microphone amp circuit.

When C = 4.7 µF, the attack and release times are as follows:

Attack time = Approx. 29 ms
Release time = Approx. 1.6 s

Setting the capacitance (C) to a smaller value enables the attack and release times to be adjusted. When the ALC circuit is not used, change the capacitor (*1) to a resistor (approx. 10 kΩ), and connect to GND line.
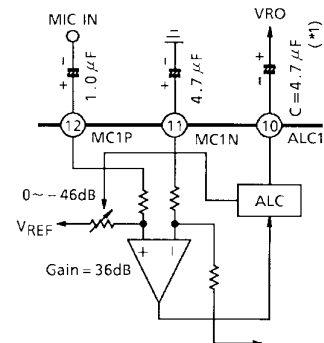At power on, while the capacitor is being charged, no sound is output. So, use a capacitance of 4.7 µF or less.

Figure 2
Microphone amp with ALC

3. AD/DA converter and digital delay circuit

The AD/DA converter is a 12-bit successive comparison type. The sampling frequency when the system clock operates at 4 MHz is 32 kHz.

The analog signal input from the AD converter is converted to 12-bit digital data. The digital delay circuit compresses the 12-bit signal to 4-bit, writes it to delay RAM, then reads it. The 4-bit data read from delay RAM is de-compressed to 12-bit. The 12-bit data are converted to analog signals by the DA converter and output.

The area for delay RAM memory is 4096 words × 4 bits.

The echo delay time is 4096 words × (1/32 kHz) = 128 ms.
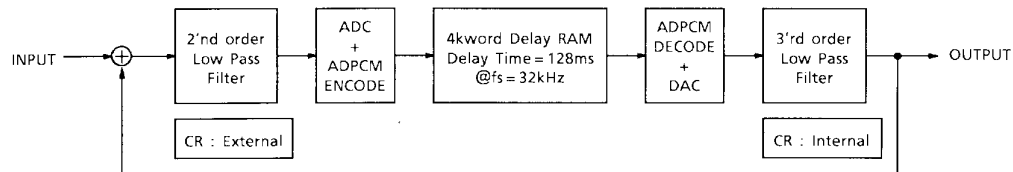
Figure 3 is a block diagram of the echo circuit.

Figure 3   Block diagram of echo circuit

4. Electronic volume controllers

The IC incorporates microphone input 1 (MIC1) and microphone input 2 (MIC2) volume and echo volume controllers. The built-in volume controller operates in 16 steps. Using an external variable resistor, volume can be controlled by the DC level or from the MCU using serial data.

The TC9455F/N supports an I^2C bus interface; the TC9488F/N, a three-lead interface.

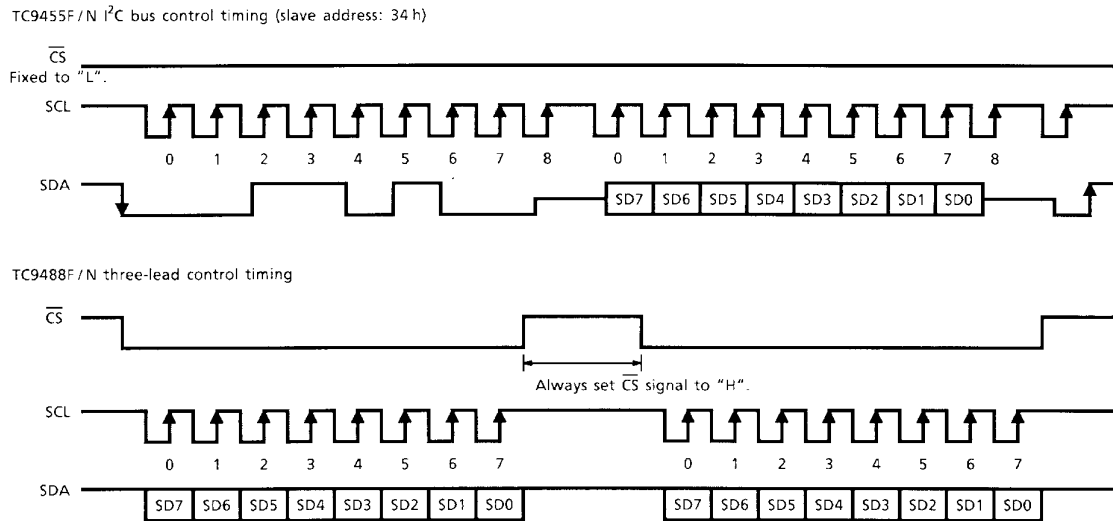### 4.1 Serial control timing

Figure 4 shows the serial control timing.

TC9455F/N I^{2}C bus control timing (slave address: 34 h)

TC9488F/N three-lead control timing

Figure 4   Serial control timing

Table 1 lists bits used to set the volume.

Table 1   Volume setting bits

MODE	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
VOL1 setting	M3	M2	M1	M0	0	0	0	0
VOL2 setting	M3	M2	M1	M0	0	1	0	0
VOL3 setting	M3	M2	M1	M0	1	0	0	0
VOL1, 2, 3 setting	M3	M2	M1	M0	1	1	0	0

M3, M2, M1, M0: Volume setting data

4.2 Setting of microphone and echo volumes

Table 2 lists the microphone setting values and attenuation; Table 3 lists the echo volume setting values and attenuation. The DC level settings are typical values.

Table 2   Microphone volume (VOL1, VOL2) attenuation

DC Level Setting (V)	Serial Data Setting				Attenuation (dB)
	M3	M2	M1	M0	
5.0					
4.4	0	0	0	0	0
4.2	0	0	0	1	−2
3.9	0	0	1	0	−4
3.7	0	0	1	1	−6
3.5	0	1	0	0	−8
3.2	0	1	0	1	−10
3.0	0	1	1	0	−12
2.7	0	1	1	1	−14
2.5	1	0	0	0	−16
2.3	1	0	0	1	−18
2.0	1	0	1	0	−20
1.8	1	0	1	1	−22
1.5	1	1	0	0	−24
1.3	1	1	0	1	−26
1.1	1	1	1	0	−28
0.0	1	1	1	1	−∞

Table 3   Echo volume (VOL3) attenuation

DC Level Setting (V)	Serial Data Setting				Attenuation (dB)
	M3	M2	M1	M0	
5.0					
4.4	0	0	0	0	0
4.2	0	0	0	1	−1
3.9	0	0	1	0	−2
3.7	0	0	1	1	−3
3.5	0	1	0	0	−4
3.2	0	1	0	1	−5
3.0	0	1	1	0	−6
2.7	0	1	1	1	−7
2.5	1	0	0	0	−8
2.3	1	0	0	1	−9
2.0	1	0	1	0	−10
1.8	1	0	1	1	−11
1.5	1	1	0	0	−12
1.3	1	1	0	1	−13
1.1	1	1	1	0	−14
0.0	1	1	1	1	−∞

Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating		Unit
Supply voltage	V_{DD}	−0.3~6.0		V
Input voltage	V_{in}	−0.3~V_{DD} + 0.3		V
Power dissipation	P_D	TC9455/88F	200	mW
		TC9455/88N	300	
Operating temperature	T_{opr}	−25~85		°C
Storage temperature	T_{stg}	−55~150		°C

Electrical Characteristics (unless otherwise specified, Ta = 25°C , V_{DD} = 5.0 V)
DC characteristics

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Operating supply voltage		V_{DD}	—	Ta = −25~85°C	4.5	5.0	5.5	V
Operating supply current		I_{DD}	—	Fmck = 4 MHz	—	20	30	mA
Operating frequency		Fmck	—	fs = 32 kHz typ.	—	4.0	—	MHz
Power-on reset voltage		V_{por}	—		—	4.0	4.25	V
Input voltage	"H" level	V_{IH}	—		V_{DD} × 0.8	—	V_{DD}	V
	"L" level	V_{IL}	—		0	—	V_{DD} × 0.2	
Input current	"H" level	I_{IH}	—		—	—	1.0	μA
	"L" level	I_{IL}	—		−1.0	—	—	

Volume control (when VOLST = "L")

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Hysteresis voltage	VH	—		—	0.12	—	V
Input step width	VST	—		—	0.26	—	V
Min level input voltage	VImin	—		—	1.1	0.8	V
Max level input voltage	VImax	—		4.95	4.8	—	V

AC Characteristics

Microphone amps and volumes

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Microphone amp gain	MICG	—	Input 1-kHz sine wave, −50dBV, MCO pin measured.	47.5	49.5	51.5	dBV
MCO Output at ALC Operation	VM	—	Input 1-kHz sine wave, −25dBV.	−0.8	1.7	3.2	dBV
Maximum Input at No ALC Operation	VL	—	Input 1-kHz sine wave.	—	−47.5	—	dBV
Maximum Input 1 at ALC Operation	VA1	—	Input 1-kHz sine wave. MCO output clip limit vale at max volume	—	−4.0	—	dBV
Maximum Input 2 at ALC Operation	VA2	—	Input 1-kHz sine wave. MCO output clip limit value at microphone amp output point	—	6.5	—	dBV
POOUT output noise 1	NO1	—	VOL1~3: min	—	−90	−85	dBV
POOUT output noise 2	NO2	—	VOL1: max, VOL2: min, VOL3: min	—	−63	−58	dBV
POOUT output noise 3	NO3	—	VOL1: min, VOL2: max, VOL3: min	—	−64	−59	dBV
POOUT output noise 4	NO4	—	VOL1: min, VOL2: min, VOL3: max	—	−65	−54	dBV
POOUT output noise 5	NO5	—	VOL1: max, VOL2: max, VOL3: min	—	−60	−54	dBV
POOUT output noise 6	NO6	—	VOL1: max, VOL2: min, VOL3: min	—	−62	−54	dBV
POOUT output noise 7	NO7	—	VOL1: min, VOL2: max, VOL3: max	—	−62	−54	dBV
POOUT output noise 8	NO8	—	VOL1~3: max	—	−59	−52	dBV
Volume 1, 2 attenuation	ATT1	—	Ratio with one level higher (excluding the minimum level)	—	−2.0	—	dB
Volume 3 attenuation	ATT2	—	Ratio with one level higher (excluding the minimum level)	—	−1.0	—	dB
Attack time	T_{ATK}	—	1 kHz Sine wave input, −20dBV → −10dBV C = 47 µF (Note 3)	—	120	—	ms
			C = 0.47 µF (Note 3)	—	10	—	
Release time	T_{RLS}	—	1 kHz Sine wave input, −10dBV → −20dBV C = 47 µF (Note 3)	—	1.6	—	s
			C = 0.47 µF (Note 3)	—	0.15	—	

Note 3: External capacitor of ALC pin

Microcontroller interface (when VOLST = "H")

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Interface setup time	tIFS	—	(Note 4)	0.25	—	—	µs
Shift clock "L" duration	tL	—		0.25	—	—	µs
Shift clock "H" duration	tH	—		0.25	—	—	µs
Data setup time	tDS	—		0.25	—	—	µs
Data hold time	tDH	—		0.25	—	—	µs
Interface hold time	tIFH	—	(Note 4)	1.0	—	—	µs
$\overline{CS}$ "H" duration	tCSH	—	(Note 4)	0.25	—	—	µs

Note 4: With TC9488F and TC9488N

2002-02-05

AC Characteristics Test Points

1. TC9488F/N three-lead interface
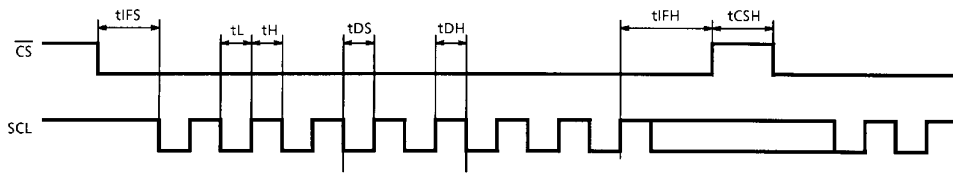
2. TC9455F/N I^{2}C bus interface
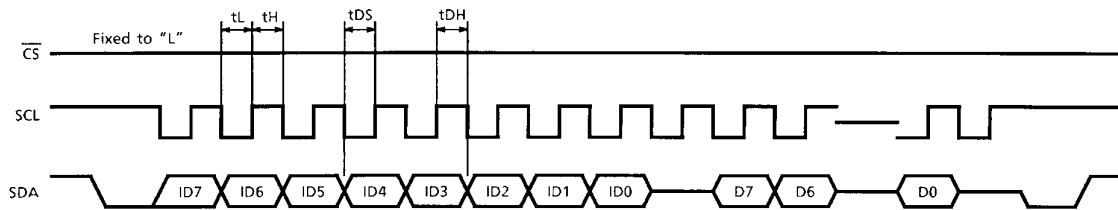
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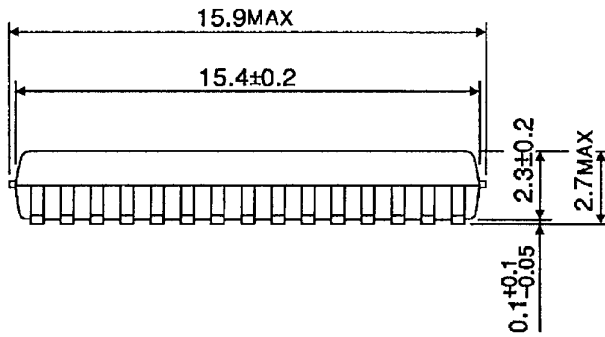|			
tIFS	>	0.25 μs	interface setup time
tL	>	0.25 μs	shift clock L time
tH	>	0.25 μs	shift clock H time
tDS	>	0.25 μs	data setup time
tDH	>	0.25 μs	data hold time
tIFH	>	1.0 μs	interface hold time
tCSH	>	0.25 μs	$\overline{CS}$ signal H duration

TC9455/88F AC Test Circuit
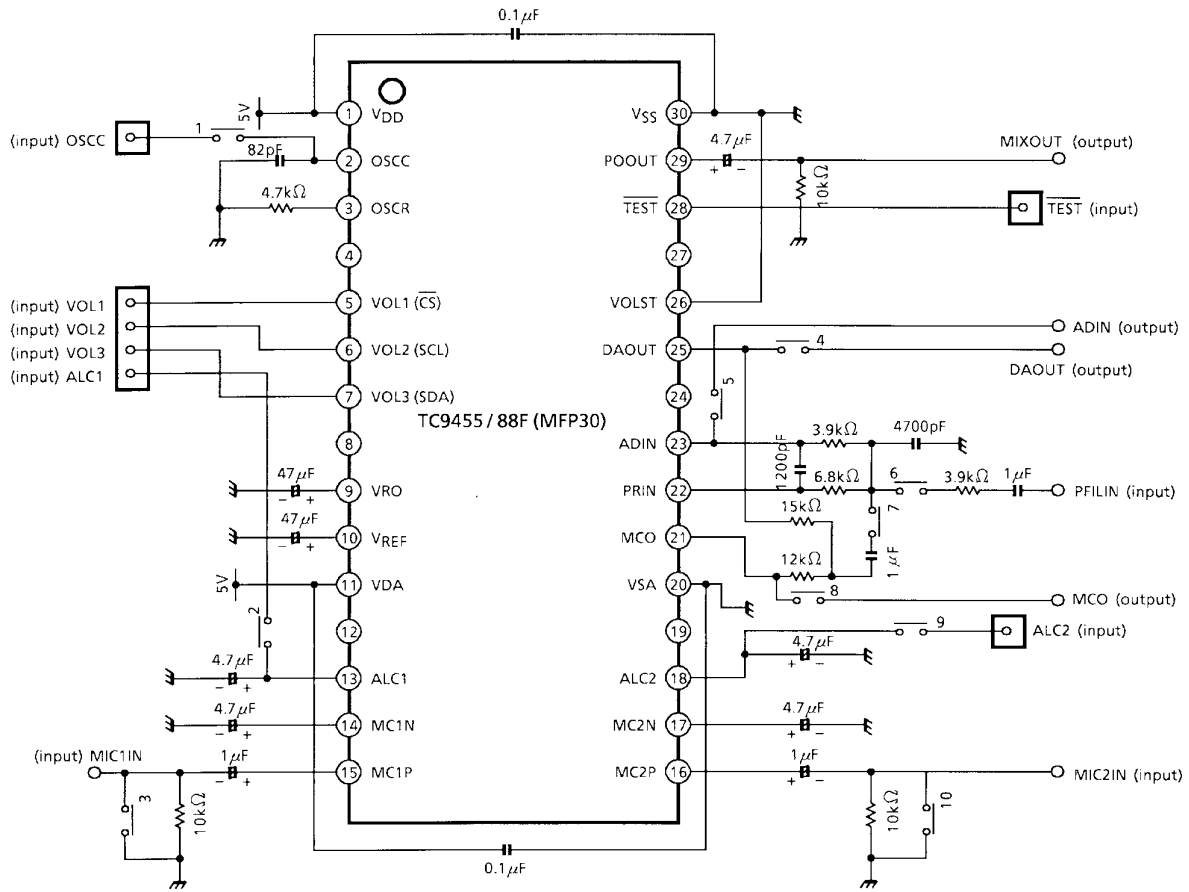
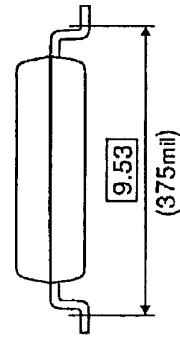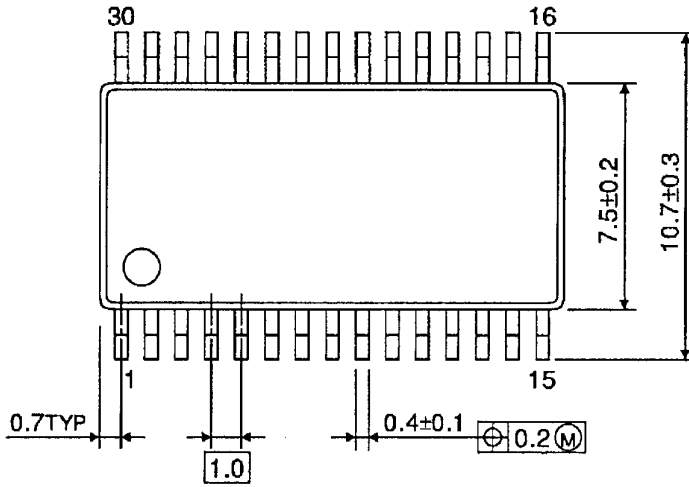## Package Dimensions

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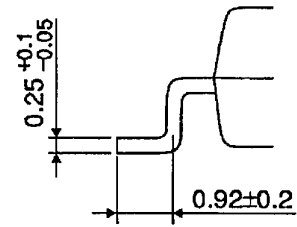
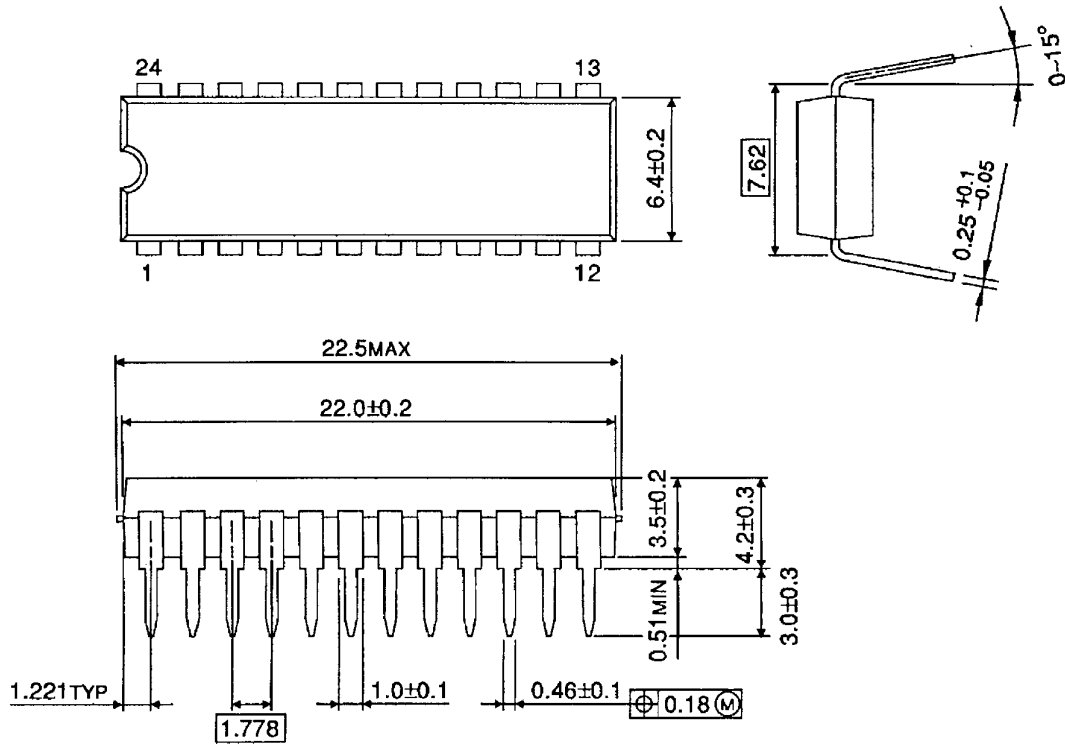Weight: 1.08 g (typ.)

Package Dimensions

SDIP24-P-300-1.78   Unit : mm

Weight: 1.2 g (typ.)

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