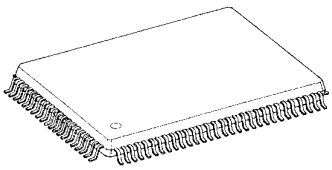
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC9496AF

1 Chip Audio Digital Signal Processor

TC9496AF is the 1 chip audio DSP which built in 24-bits, a 22.5 MIPS DSP core, 3 ch AD converter, 5 ch DA converter, and electronic volume for trims, and corresponds to a Multi-speaker system.

It is possible to realize many application, such as sound field control-hall simulation, for example-, digital filter for equalizers, dynamic range control, KARAOKE and something.



QFP100-P-1420-0.65A

Weight: 1.57 g (typ.)

Features

- Incorporates 3 ch AD converter, 2 ch is 1 bit Σ-Δ type AD converter for HiFi-Audio and 1 ch is 16 bit Multi-bit type AD converter for Microphone.
  2 ch HiFi-ADC (1 bitΣ-Δ type) S/N: 96dB (typ.)
  1 ch Mic. ADC (16 bit Multi-bit type) S/N: 80dB (typ.)
- Incorporates 1 bitΣ-Δ type DA converter, and the attenuator for trims is built in each DAC output. In case of the use which does not use a trim, It is possible to output the analog signal of DAC directly.
  5 ch DAC (1 bitΣ-Δ type) S/N: 96dB (typ.)
  Attenuator for trim 0dB to −24dB (1dB step)
- Each port has a digital input/output.
- A built-in self-boot function automatically sets the coefficients and register values at initialization.
  Moreover, four kinds of boot data can be chosen by pin setup.
  Boot ROM: 1024 word × 18 bit
- The DSP block specification are as follows:
  Data bus: 24 bit
  Multiplier/adder: 24 bit × 16 bit + 43 bit → 43 bit
  Accumulator: 43 bit (sign extension: 4 bit)
  Program ROM: 2048 word × 32 bit
  Coefficient RAM: 448 word × 16 bit
  Coefficient ROM: 256 word × 16 bit
  Offset RAM: 64 word × 16 bit
  Data RAM: 256 word × 24 bit
  Operation speed: 44 ns (510-step (approx.) operation per cycle at fs = 44.1 kHz)
  Interface buffer RAM: 32 word × 16 bit
- Incorporates data delay RAM of 64 kbit.
  Delay RAM: 4096 word × 16 bit (64 kbit)
- The microcontroller interface can be selected between TOSHIBA original 3 line type and I²C bus format.
- CMOS silicon structure supports high speed.
- The package is a 100-pin flat package.

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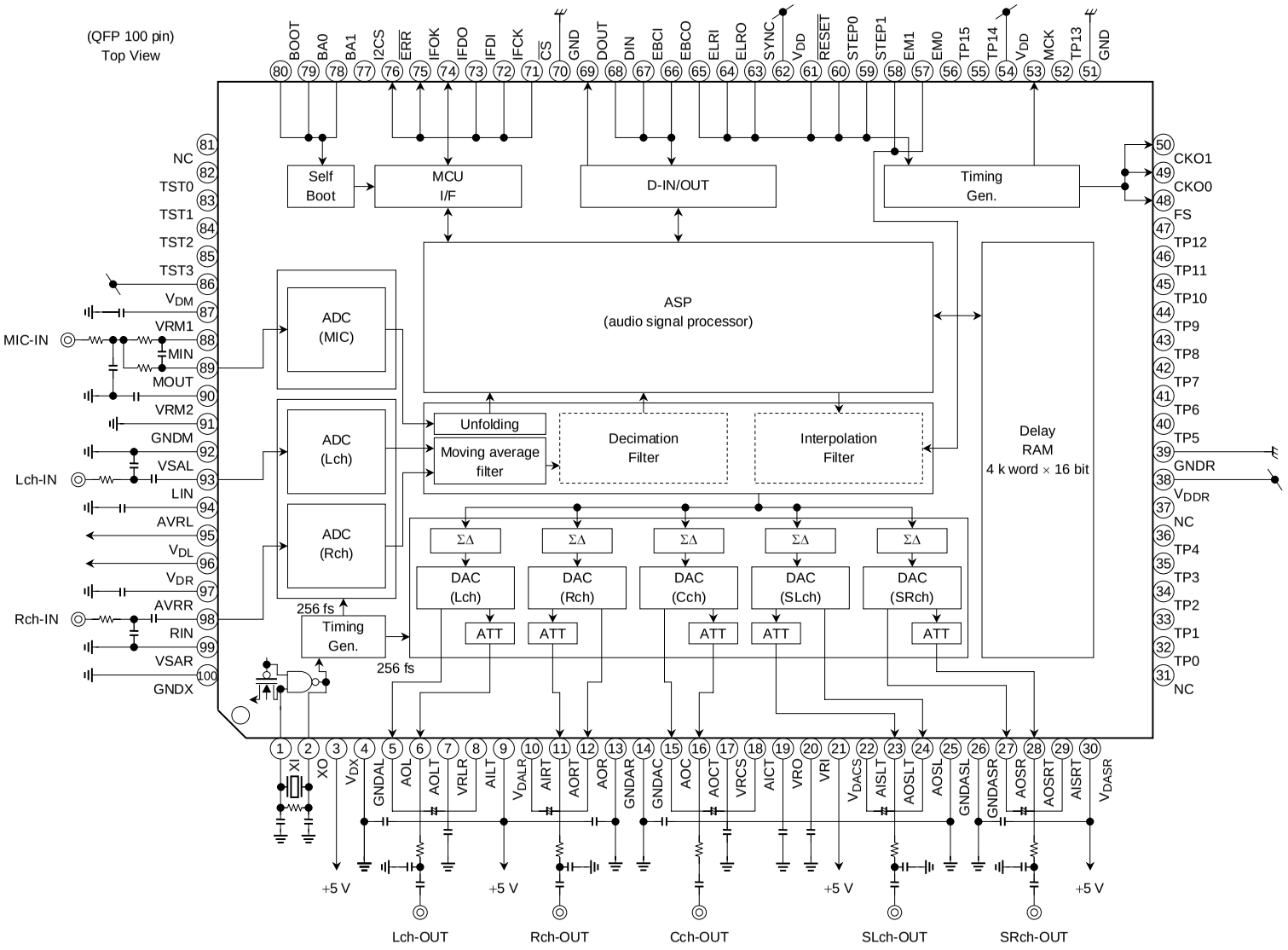
Block Diagram/Pin Connection



Pin Function

Pin No.	Symbol	I/O	Function	Remarks
1	XI	I	Crystal oscillator connecting or external clock input pin	
2	XO	O	Crystal oscillator connecting pin	
3	V_{DX}	—	Power pin for oscillator circuit	
4	GNDAL	—	Ground pin for DAC Left channel	
5	AOL	O	DAC Left channel signal output pin	
6	AOLT	O	DAC Left channel attenuator output pin	
7	VRLR	—	Reference voltage pin for DAC L/R channel	
8	AILT	I	DAC Left channel attenuator input pin	
9	V_{DALR}	—	Power pin for DAC L/R channel	
10	AIRT	I	DAC Right channel attenuator input pin	
11	AORT	O	DAC Right channel attenuator output pin	
12	AOR	O	DAC Right channel signal output pin	
13	GNDAR	—	Ground pin for DAC Right channel	
14	GNDAC	—	Ground pin for DAC Center channel	
15	AOC	O	DAC Center channel signal output pin	
16	AOCT	O	DAC Center channel attenuator output pin	
17	VRCS	—	Reference power pin for DAC C/SL/SR channel	
18	AICT	I	DAC Center channel attenuator input pin	
19	VRO	O	Reference voltage pin for attenuator (buffer output)	
20	VRI	I	Reference voltage pin for attenuator (buffer input)	
21	V_{DACS}	—	Power pin for DAC C/SL channel	
22	AISLT	I	DAC SL channel attenuator input pin	
23	AOSLT	O	DAC SL channel attenuator output pin	
24	AOSL	O	DAC SL channel signal output pin	
25	GNDASL	—	Ground pin for DAC SL channel	
26	GNDASR	—	Ground pin for DAC SR channel	
27	AOSR	O	DAC SR channel signal output pin	
28	AOSRT	O	DAC SR channel attenuator output pin	
29	AISRT	I	DAC SR channel attenuator input pin	
30	V_{DASR}	—	Power pin for DAC SR channel	
31	NC	—	Non-Connecting	Select the open state, V_{DD} connecting or GND connecting
32	TP0	O	Test pin 0	
33	TP1	O	Test pin 1	
34	TP2	O	Test pin 2	
35	TP3	O	Test pin 3	
36	TP4	O	Test pin 4	
37	NC	—	Non-Connecting	Select the open state, V_{DD} connecting or GND connecting
38	V_{DDR}	—	Power pin for delay RAM	
39	GNDR	—	Ground pin for delay RAM	
40	TP5	O	Test pin 5	

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Pin No.	Symbol	I/O	Function	Remarks
41	TP6	O	Test pin 6	
42	TP7	O	Test pin 7	
43	TP8	O	Test pin 8	
44	TP9	O	Test pin 9	
45	TP10	O	Test pin 10	
46	TP11	O	Test pin 11	
47	TP12	O	Test pin 12	
48	FS	O	Clock out pin (sampling frequency)	
49	CKO0	O	Clock output pin 0	
50	CKO1	O	Clock output pin 1	
51	GND	—	Ground pin	
52	TP13	O	Test pin 13	
53	MCK	O	MCK clock output pin	
54	V_{DD}	—	Power pin	
55	TP14	O	Test pin 14	
56	TP15	O	Test pin 15	
57	EM0	I	De-emphasis setting pin 0	Schmitt input
58	EM1	I	De-emphasis setting pin 1	Schmitt input
59	STEP1	I	ASP execution step switching pin 1	Schmitt input
60	STEP0	I	ASP execution step switching pin 0	Schmitt input
61	$\overline{\text{RESET}}$	I	Reset pin	Schmitt input
62	V_{DD}	—	Power pin	
63	SYNC	I	Program synchronous signal input pin	Schmitt input
64	ELRO	I	LR clock input pin for serial data output (DOUT)	Schmitt input
65	ELRI	I	LR clock input pin for serial data input (DIN)	Schmitt input
66	EBCO	I	Bit clock input pin for serial data output (DOUT)	Schmitt input
67	EBCI	I	Bit clock input pin for serial data input (DIN)	Schmitt input
68	DIN	I	Serial data input pin	Schmitt input
69	DOUT	O	Serial data output pin	
70	GND	—	Ground pin	
71	$\overline{\text{CS}}$	I	Microcontroller interface chip select signal input pin	Schmitt input
72	IFCK	I	Microcontroller interface data shift clock signal input pin	Schmitt input
73	IFDI	I	3 line bus mode: Microcontroller interface data input pin	Schmitt input/ Open drain output
		I/O	I^2C bus mode: Microcontroller interface data input/output pin	
74	IFDO	O	Microcontroller interface data output pin	
75	IFOK	O	Microcontroller interface operation flag pin	Open drain output
76	$\overline{\text{ERR}}$	O	Error flag output pin	Open drain output
77	I2CS	I	Microcontroller interface I^2C bus/3 line bus switching pin	
78	BA1	I	Boot address setting pin 1	Schmitt input
79	BA0	I	Boot address setting pin 0	Schmitt input
80	BOOT	I	Self boot control pin	Schmitt input
81	NC	—	Non-connecting	Select the open state, V_{DD} connecting or GND connecting
82	TST0	I	Test pin T0	Schmitt input

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Pin No.	Symbol	I/O	Function	Remarks
83	TST1	I	Test pin T1	Schmitt input
84	TST2	I	Test pin T2	Schmitt input
85	TST3	I	Test pin T3	Schmitt input
86	V_{DM}	—	Power pin for microphone ADC	
87	VRM1	—	Reference voltage pin 1 for microphone ADC	
88	MIN	I	Microphone ADC amplifier input pin	
89	MOUT	O	Microphone ADC amplifier output pin	
90	VRM2	—	Reference voltage pin 2 microphone ADC	
91	GNDM	—	Ground pin for microphone ADC	
92	VSAL	—	Ground pin for ADC L channel	
93	LIN	I	ADC L channel signal input pin	
94	AVRL	—	Reference voltage pin for ADC L channel	
95	V_{DL}	—	Power pin for ADC L channel	
96	V_{DR}	—	Power pin for ADC R channel	
97	AVRR	—	Reference voltage pin for ADC R channel	
98	RIN	I	ADC R ch signal input pin	
99	VSAR	—	Ground pin for ADC R channel	
100	GNDX	—	Ground pin for oscillator circuit	

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Operation

1. Pin Operation

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Function</th></tr>
<tr><td>1</td><td>XI</td><td rowspan="2">Connect the crystal oscillator.</td></tr>
<tr><td>2</td><td>XO</td></tr>
<tr><td>3 to 30</td><td>Omitted</td><td>—</td></tr>
<tr><td>31</td><td>NC</td><td>Non-connecting. Select the open state, V_{DD} connecting or GND connecting.</td></tr>
<tr><td>32 to 36</td><td>TP0 to TP4</td><td>Test pin. (leave open)</td></tr>
<tr><td>37</td><td>NC</td><td>Non-connecting. Select the open state, V_{DD} connecting or GND connecting.</td></tr>
<tr><td>38</td><td>V_{DDR}</td><td>Power pin for delay RAM</td></tr>
<tr><td>39</td><td>GNDR</td><td>Ground pin for delay RAM</td></tr>
<tr><td>40 to 47</td><td>TP5 to TP12</td><td>Test pin (leave open)</td></tr>
<tr><td>48</td><td>FS</td><td>Clock out pin (sampling frequency)</td></tr>
<tr><td>49
50</td><td>CKO0
CKO1</td><td>Timing output pins. The output frequency is set from the microcontroller (command-40h)
<table>
<tr><th colspan="3">Command (set the command-40h)</th><th rowspan="2">CKO0 Output Frequency</th></tr>
<tr><th>CKOS02</th><th>CKOS01</th><th>CKOS00</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Fixed to L</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>fs × 2</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>fs × 4</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>fs × 8</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>fs × 16</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>fs × 32</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>fs × 64</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>fs × 128</td></tr>
</table>
<table>
<tr><th colspan="3">Command (set the command-40h)</th><th rowspan="2">CKO1 Output Frequency</th></tr>
<tr><th>CKOS12</th><th>CKOS11</th><th>CKOS10</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Fixed to L</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>fs × 2</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>fs × 4</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>fs × 8</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>fs × 16</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>fs × 32</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>fs × 64</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>XI × 1/2</td></tr>
</table></td></tr>
<tr><td>51</td><td>GND</td><td>Ground pin</td></tr>
<tr><td>52</td><td>TP13</td><td>Test pin (leave open)</td></tr>
<tr><td>53</td><td>MCK</td><td>Master clock output pin. Validated/Invalidated of an output, and the frequency is switched from in the of microcontroller command (command-4Dh) and STEP1 pin (59 pin).
<table>
<tr><th colspan="2">Command (set the command-4Dh)</th><th>Pin</th><th rowspan="2">MCK Output</th></tr>
<tr><th>MCKE</th><th>MCKS</th><th>STEP1</th></tr>
<tr><td>0</td><td>(Note 1)</td><td>(Note 1)</td><td>Fixed to L</td></tr>
<tr><td>1</td><td>0</td><td>(Note 1)</td><td>fs × 256</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Source oscillation (XI)</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Prohibited</td></tr>
</table>
Note 1: Don’t care</td></tr>
<tr><td>54</td><td>V_{DD}</td><td>Power pin</td></tr>
<tr><td>55
56</td><td>TP14
TP15</td><td>Test pin (leave open)</td></tr>
</table>

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<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Function</th></tr>
<tr><td>57
58</td><td>EM0
EM1</td><td>De-emphasis control pins
<table>
<tr><th>EM1</th><th>EM0</th><th>De-Emphasis Setting</th></tr>
<tr><td>0</td><td>0</td><td>De-emphasis off</td></tr>
<tr><td>0</td><td>1</td><td>fs = 48 kHz</td></tr>
<tr><td>1</td><td>0</td><td>fs = 44.1 kHz</td></tr>
<tr><td>1</td><td>1</td><td>fs = 32 kHz</td></tr>
</table></td></tr>
<tr><td>59
60</td><td>STEP1
STEP0</td><td>Source oscillation frequency/ASP operation speed switching pins
<table>
<tr><th>STEP1</th><th>STEP0</th><th>Source Oscillation Frequency</th><th>No. of ASP Operation Steps</th></tr>
<tr><td>0</td><td>0</td><td>fs × 512</td><td>340/fs</td></tr>
<tr><td>0</td><td>1</td><td>fs × 768</td><td>510/fs</td></tr>
<tr><td>1</td><td>*</td><td colspan="2">Prohibited</td></tr>
</table></td></tr>
<tr><td>61</td><td>$\overline{\text{RESET}}$</td><td>Reset pin. L at initialization.</td></tr>
<tr><td>62</td><td>V_{DD}</td><td>Power pin</td></tr>
<tr><td>63</td><td>SYNC</td><td>Program operation SYNC signal input pin.</td></tr>
<tr><td>64</td><td>ELRO</td><td>LR clock signal input pin for serial output data.
Valid when serial data are output in a slave operation (set the command-4Dh).</td></tr>
<tr><td>65</td><td>ELRI</td><td>LR clock signal input pin for serial input data.
Valid when serial data are input in a slave operation (set the command-4Dh).</td></tr>
<tr><td>66</td><td>EBCO</td><td>Bit clock signal input pin for serial output data.
Valid when serial data are output in a slave operation (set the command-4Dh).</td></tr>
<tr><td>67</td><td>EBCI</td><td>Bit clock signal input pin for serial input data.
Valid when serial data are input in a slave operation (set the command-4Dh).</td></tr>
<tr><td>68</td><td>DIN</td><td>Serial input data signal input pin. Connected to internal register in ASP block.
The internal register connected is set up by the microcomputer command (command-43h).</td></tr>
<tr><td>69</td><td>DOUT</td><td>Serial input data signal input pin. Connected to internal register in ASP block.
The internal register connected is set up by the microcomputer command (command-43h).</td></tr>
<tr><td>70</td><td>GND</td><td>Ground pin</td></tr>
</table>

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<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Function</th></tr>
<tr><td>71
72
73
74
75
76
77</td><td>$\overline{CS}$
IFCK
IFDI
IFDO
IFOK
$\overline{ERR}$
I2CS</td><td>Microcontroller interface pins.
<table>
<tr><th>I2CS</th><th>Transmission Mode</th></tr>
<tr><td>0</td><td>Standard Transmission mode</td></tr>
<tr><td>1</td><td>I^2C mode</td></tr>
</table>
<table>
<tr><th></th><th>Standard Transmission Mode</th><th>I^2C Mode</th></tr>
<tr><td>$\overline{CS}$</td><td>Chip select</td><td>Chip select (can be fixed to L)</td></tr>
<tr><td>IFCK</td><td>Transmit/receive clock</td><td>Transmit/receive clock</td></tr>
<tr><td>IFDI</td><td>Data or command input</td><td>Data input/output</td></tr>
<tr><td>IFDO</td><td>Data output (monitor mode)</td><td>Fixed to L output</td></tr>
<tr><td>$\overline{ERR}$</td><td>Error flag signal output</td><td>Error flag signal output</td></tr>
<tr><td>IFOK</td><td>Internal operation confirmation flag signal output</td><td>Internal operation confirmation flag signal output</td></tr>
</table></td></tr>
<tr><td>78
79</td><td>BA1
BA0</td><td>Self-boot start address setting pins (at reset)
<table>
<tr><th>BA1</th><th>BA0</th><th>Start Address</th></tr>
<tr><td>0</td><td>0</td><td>000h</td></tr>
<tr><td>0</td><td>1</td><td>001h</td></tr>
<tr><td>1</td><td>0</td><td>002h</td></tr>
<tr><td>1</td><td>1</td><td>003h</td></tr>
</table></td></tr>
<tr><td>80</td><td>BOOT</td><td>Self-boot control pin
<table>
<tr><th>BOOT</th><th>Operation</th></tr>
<tr><td>0</td><td>Does not Self-boot at reset</td></tr>
<tr><td>1</td><td>Self-boot at reset</td></tr>
</table></td></tr>
<tr><td>81</td><td>NC</td><td>Non-connecting. Select the open state, V_{DD} connecting or GND connecting.</td></tr>
<tr><td>82 to 85</td><td>TST0 to TST3</td><td>Test pin. Use fixed to L.</td></tr>
<tr><td>86 to 100</td><td>Omitted</td><td>—</td></tr>
</table>

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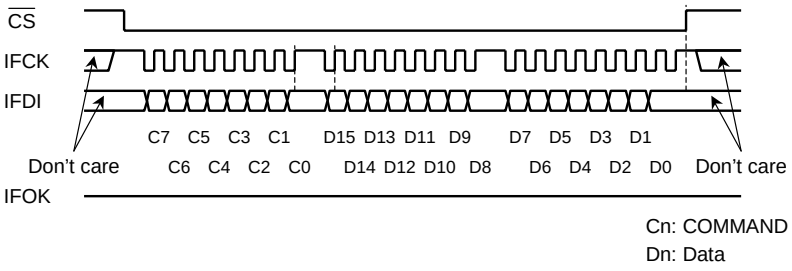
2. Microcontroller interface

2.1 Standard Transmission Mode

When I2CS = L, data can be transmitted or received in Standard Transmission mode.
When the $\overline{CS}$ signal is Low, control from the microcontroller is enabled.
The IFCK signal is the transmit/receive clock, the IFDI signal is the data.
The TC9496AF loads the IFDI data on the IFCK signal rising edge.
When $\overline{CS}$ = H, the IFCK and IFDI signals are don't care.

2.1.1 Setting Registers



The registers are set by command data using IFDI signal.

The first byte is a command, which differs for each register. The data sent after that are fixed to two bytes. Both command and data are sent starting from the MSB.

Data are loaded the rising edge of the IFCK signal. Note that commands or data that must be switched, such as the RUN-MUTE command (command-44h) or the IFF flag, must be synchronized with the SYNC signal and loaded on that signal.

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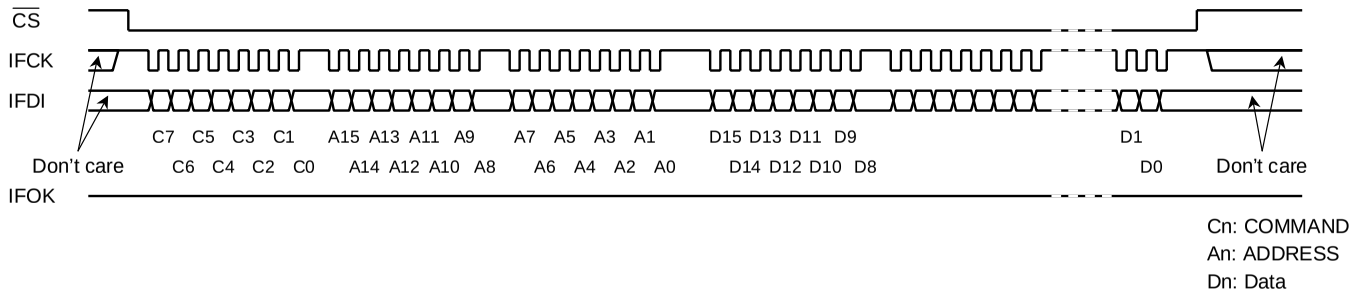
2.1.2 Setting RAM (sequential)



The RAMs are set by command data using the IFDI signal.

The first byte is a command, which differs for each RAM. The next two bytes contain the start address for the RAM written.

The length of the data field following the RAM address bytes is 2 × n bytes. The address is automatically incremented by 1.

During program running, 1 word of data is written at a time in internal RAM synchronizing with a SYNC signal.

Therefore, when performing continuously two or more write to word, unless it applies more than 1/fs [s] per 1 word and it sets up, taking in of data is not performed correctly.

At the time of program STOP, it is written in asynchronous.

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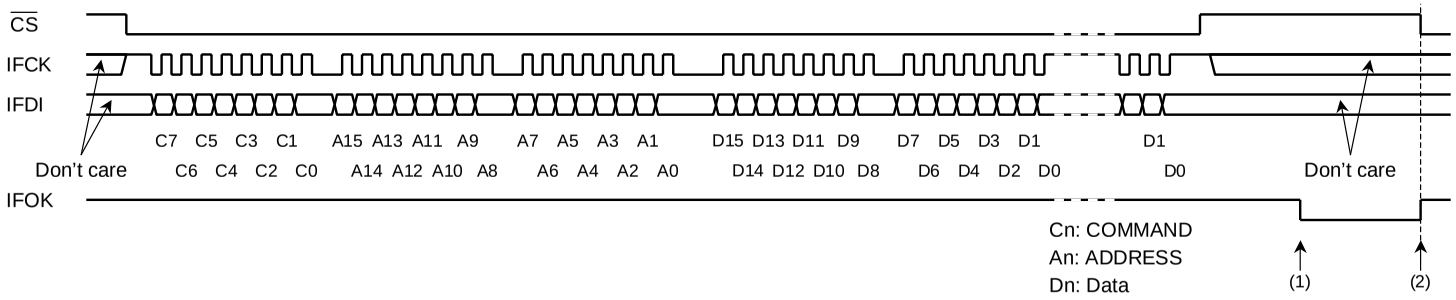
2.1.3 Setting RAM (ACMP mode)



In ACMP mode, the TC9496AF does not write data directly to coefficient RAM (CRAM) or offset RAM (OFRAM). In this mode, data must be written to the interface buffer RAM (IFB-RAM). Then, all the data are updated together in a period of 1 fs.

For example, if a signal flow filter is designed as in the following diagram, unless the K1 to K5 data are batch-updated, the circuit may resonate. The same applies to the K6 to K10 data.

Using ACMP mode can reduce the noise caused by updating coefficients while the TC9496AF is operating.

IFB-RAM is 32-word memory. Therefore, data can be updated at one time in units of up to 32-words.

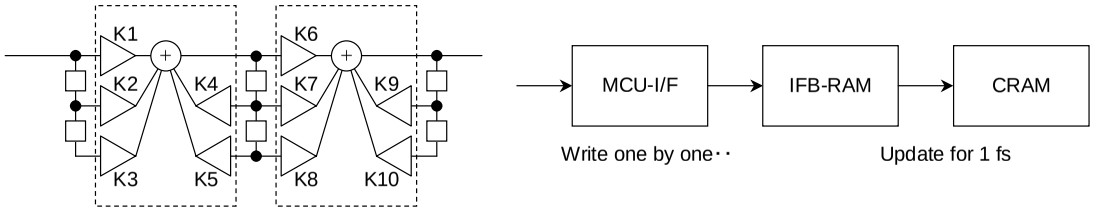
The length of the data field is $2 \times n$ bytes, where $n \leqq 32$.

In ACMP mode, the IFOK pin outputs an ACMP operation end flag.

When ACMP operations complete, the flag is set to LOW ((1)) and is initialized at the next low chip select signal ((2)).

Operation at the time of transmitting other commands, before IFOK terminal was set to "L" level cannot be guaranteed.

Please set up again after initializing by $\overline{\text{RESET}}$ terminal or the initialization command.



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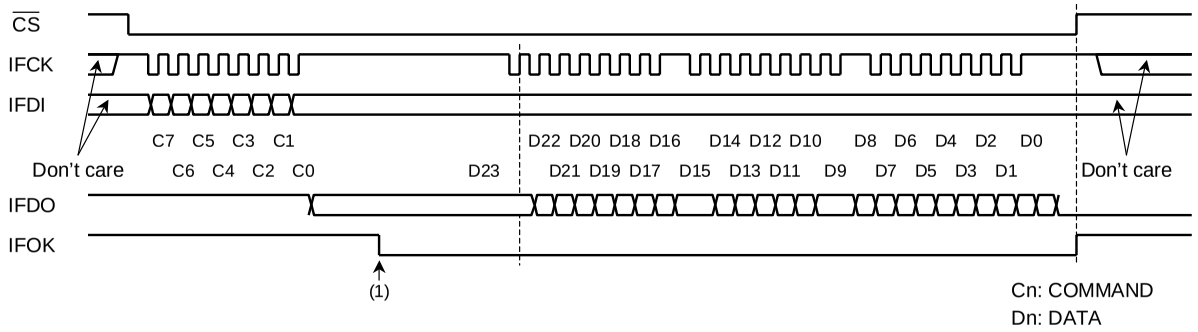
2.1.4 Monitor Mode



Monitor mode is used to monitor the data bus or pointers.

There are two further modes: a mode where the data bus or pointer (s) is monitored at a present program counter (PC) and a mode where a loop counter (LC) is added to monitor conditions in addition to PC. After the command is issued, when the TC9496AF loads data to the IFDO register (IFDOR), the IFOK pin signal is set to LOW (see (1) above).

Next, when the IFCK signal is sent, the data are output on the IFCK signal falling edge starting from the MSB.

The data length is at its maximum (24 bits or three bytes) during monitoring of the data bus. In cases where transfer must be interrupted, such as where only eight or 16 bits of the MSB side are required, monitoring can be interrupted at any time by setting the $\overline{CS}$ signal to High, the IFOK signal also goes High.

2.2 I^2C Bus Mode

When I2CS = H, data can be transmitted or received in I^2C bus mode.

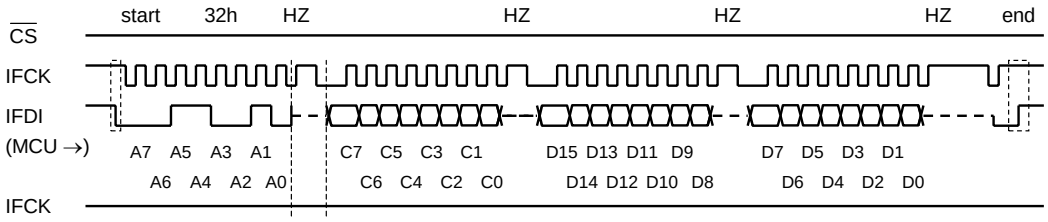
When the $\overline{CS}$ signal is Low, control from the microcontroller is enabled.

In I^2C mode, the $\overline{CS}$ signal can be used fixed to L. The IFCK signal is the transmit/receive clock. The IFDI signal is the data.

The TC9496AF loads the IFDI data on the IFCK signal rising edge.

When $\overline{CS}$ = H, IFCK and IFD signal are don't care.

2.2.1 Setting Registers



An: I^2C ADDRESS
Cn: COMMAND
Dn: Data

The register are set by command data using the IFDI signal.

The first byte after the I^2C address (= 32h) is a command, which differs for each register. The data sent after that are fixed to two bytes. Both command and data are sent starting from the MSB in I^2C format.

The data loaded internally every two bytes. Note that commands or data that must be switched on the SYNC signal, such as the RUN command or the IFF flag, must be synchronized with the SYNC signal and loaded on that signal.

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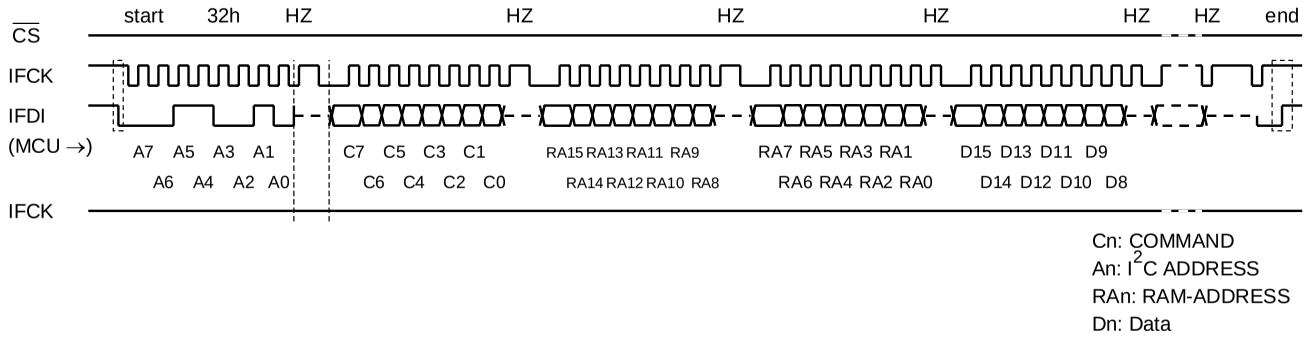
2.2.2 Setting RAM (sequential)



The RAMs are set by command data using the IFDI signal.

The first byte after the I^2C address (= 32h) is a command, which differs for each RAM. The next two bytes contain the start address for each RAM.

The length of the data field following the RAM address bytes is 2 × n bytes. The address is automatically incremented by 1.

During program running, 1 word of data is written at a time in internal RAM synchronizing with a SYNC signal.

Therefore, when performing continuously two or more write to word, unless it applies more than 1/fs [s] per 1 word and it sets up, taking in of data is not performed correctly.

At the time of program STOP, it is written in asynchronous.

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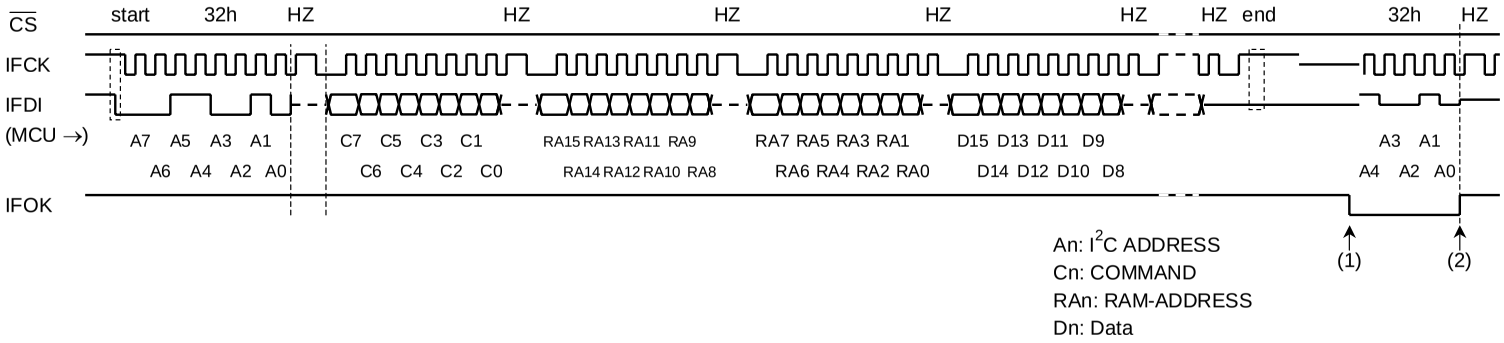
2.2.3 Setting RAM (ACMP mode)



In ACMP mode, the TC9496AF does not write data directly to coefficient RAM (CRAM) or offset RAM (OFRAM). In this mode, data must be written to the interface buffer RAM (IFB-RAM). Then, all the data are updated together in a period of 1 fs.

For example, if a signal flow filter is designed as in the following diagram, unless the K1 to K5 data are batch-updated, the circuit may resonate. The same applies to the K6 to K10 data.

Using ACMP mode can reduce the noise caused by updating coefficients while the TC9496AF is operating.

IFB-RAM is 32-word memory. Therefore, data can be updated at one time in units of up to 32-words.

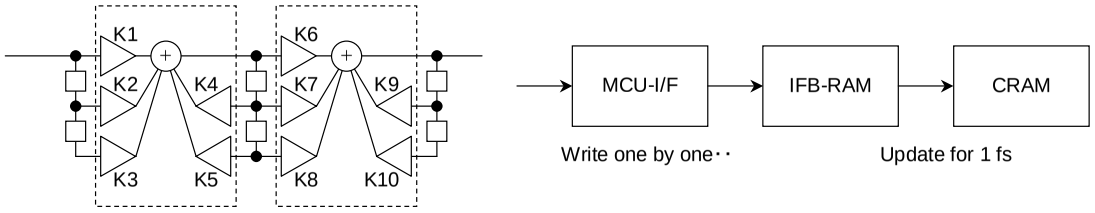
The length of the data field is $2 \times n$ bytes, where $n \leqq 32$.

In ACMP mode, the IFOK pin outputs an ACMP operation end flag.

When ACMP operations complete, the flag is set to LOW ((1)) and is initialized at the next low chip select signal ((2)).

Operation at the time of transmitting other commands, before IFOK terminal was set to "L" level cannot be guaranteed.

Please set up again after initializing by $\overline{\text{RESET}}$ terminal or the initialization command.



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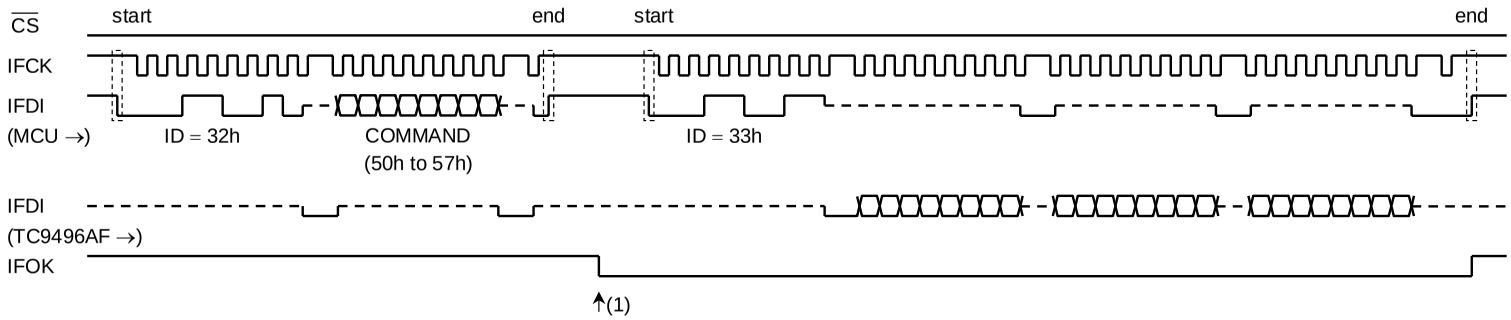
2.2.4 Monitor Mode



Monitor mode is used to monitor the data bus or pointers.

There are two further modes: a mode where the data bus or pointer (s) monitored at a preset program counter (PC) and a mode where a loop counter (LC) is added to monitor conditions in addition to the PC. First, issue the monitoring command, which has no data.

When the TC9496AF loads data to the IFDO register (IFDOR), the IFOK pin signal is set to LOW (see (1) above).

Next, the I^2C read command (ID = 33h) is issued, then when the IFCK signal is sent, the data are output on the IFCK signal falling edge from the MSB. The data length is at its maximum (24 bits or three byte) during monitoring of the data bus.

Although it is possible per byte to read only 8 or 16 bits by the side of MSB, MCU has to make it the number of bytes which specified I2COS of command 4Bh at that time.

After issuing a monitor command (50h to 56h), be sure to perform a continuous read operation by issuing the I^2C read comman (ID = 33h).

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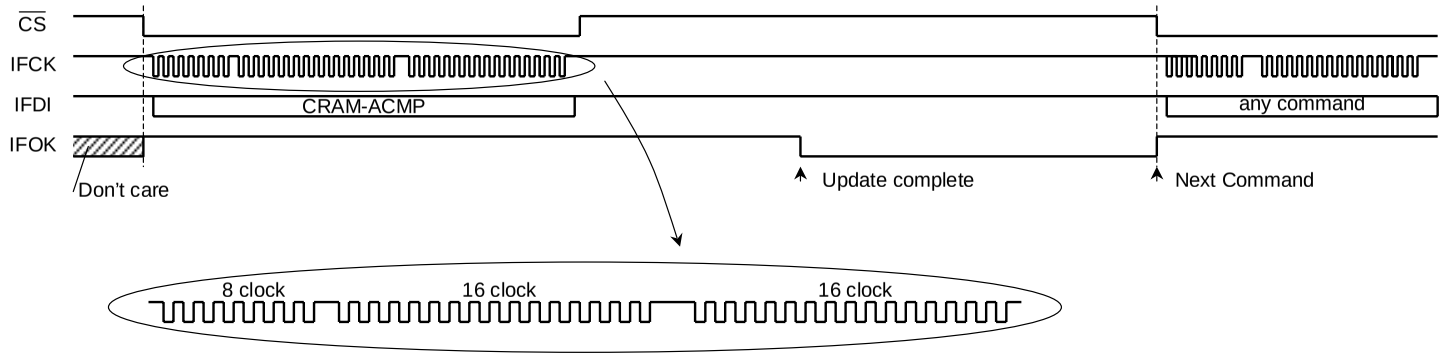
2.3 IFOK Pin Description

The IFOK signal has the following three functions.

2.3.1 ACMP Mode End Flag Output

After the completion of a RAM data update with CRAM-ACMP (command-47h) or OFRAM-ACMP (command- 49h), the IFOK pin goes Low. Setting the $\overline{CS}$ signal to Low changes the IFOK signal from Low to High.

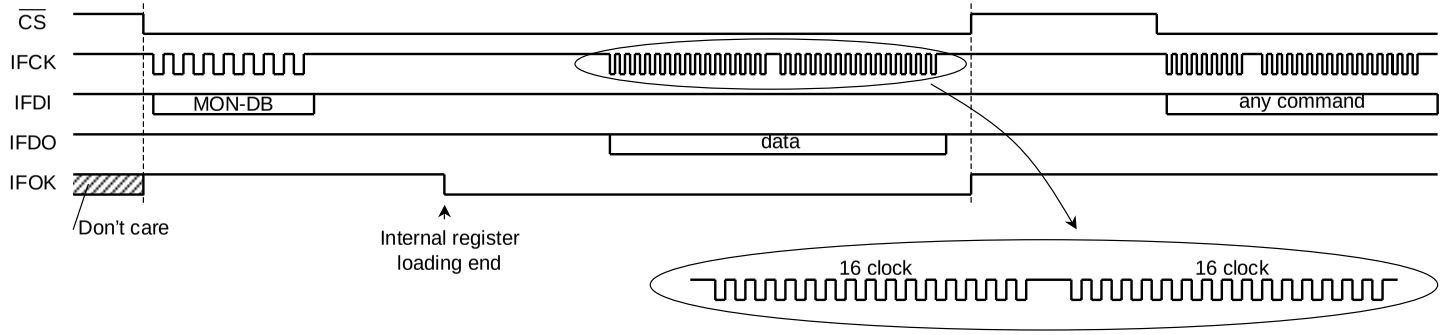
Example:



2.3.2 Loading End Flag Output in Monitor Mode

When monitoring using the bus monitor command (command-50h), for example, after data are loaded to the internal register under the specified conditions, the IFOK signal goes Low. In this mode, if $\overline{CS}$ signal is made into "H" level, IFOK signal will also be set to "H" level.

Example:



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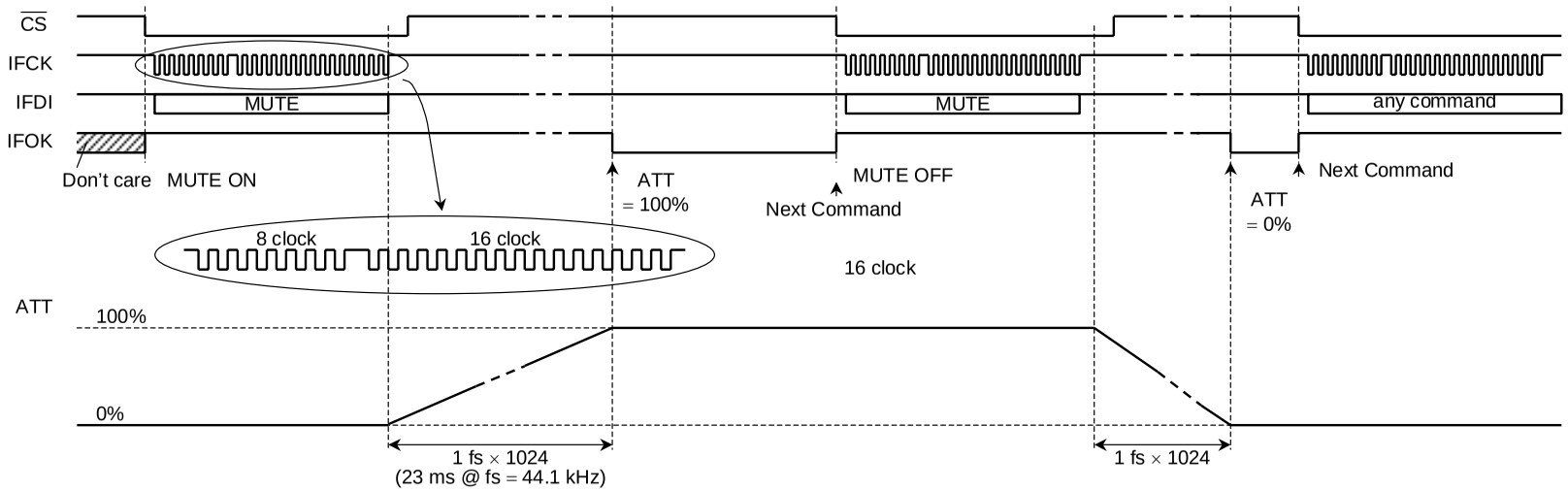
2.3.3 Attenuator Operation End Flag Output of the Digital-Filter Section

When using a command to control the DF block mute ON/OFF (command-44h, bit5), the mute end flag is output from the IFOK pin after the mute operation completes.

Moreover, when the amount of attenuators by DF attenuator command (command-58h) is changed, IFOK terminal is set to "L" level as a flag which attenuator operation completed.



Note

At power on, the IFOK pin output is undefined. When the $\overline{CS}$ signal goes Low, the IFOK signal goes High.

3. Control Commands

The following table lists the control commands that can be used from the microcontroller.

3.1 Control Commands

Table 1 Control Commands

Command	Code	R/W	Description	RAM Sequential	Transfer Sync/ Async to SYNC Signal
TIMING	40h	W	Timing	—	Async
BOOT	41h		Self Boot ROM start address	—	Async
DAC-LR	42h		DAC output trim level (L, R)	—	Async
SIO	43h		SIO setting	—	Async
RUN-MUTE	44h		Program execution, mute	—	Sync
MSEQ	45h		Sequential RAM	Enable	Sync: RUN/Async: STOP
CRAM	46h		CRAM		
CRAM-ACMP	47h		CRAM (ACMP mode)		Async
ORAM	48h		ORAM		Sync: RUN/Async: STOP
ORAM-ACMP	49h		ORAM (ACMP mode)		Async
IFF	4Ah		IFF setting	—	Sync
MONI-PC	4Bh		Monitor: PC condition	—	Async
MONI-LC	4Ch		Monitor: LC condition	—	Async
MISC	4Dh		Others	—	Async
—	4Eh		Prohibited	—	—
M-RST	4Fh		Initialization	—	Async
MONI-DB	50h	R	DBUS monitor	—	Async
MONI-CP	51h		CP monitor	—	Async
MONI-OFP	52h		OFP monitor	—	Async
MONI-DP	53h		DP monitor	—	Async
MONI-AR	54h		AR monitor	—	Async
MONI-CRP	55h		CRP monitor	—	Async
MONI-SR	56h		SR monitor	—	Async
DF-ATT	58h	W	DF attenuator level (all channel)	—	Async
DAC-S	59h		DAC output trim level (SL, SR-ch)	—	Async
DAC-C	5Ah		DAC output trim level (C-ch)	—	Async

Note 2: The command which is “Sync” in the transfer Sync with Sync signal needs to set the $\overline{CS}$ = H section to a minimum of 1 fs more until it transmits the follwing command. (It need more than 22.68 μs at fs = 44.1 KHz.)

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3.2 Commands Description

Each command explanation is shown below. * mark in each command explanation table shows the initial value at the time of reset.

Command-40h (0100 0000): TIMING

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SYPD	SYD1	SYD0	SYPA	SYA1	SYA0	SYPS	SYS1	SYS0	0	CKOS 12	CKOS 11	CKOS 10	CKOS 02	CKOS 01	CKOS 00

Bit	Name	Description	Value	Operation
D15	SYPD	ASP digital block sync polarity switching	0*	ASP program starts on falling edge
			1	ASP program starts on rising edge
D14 D13	SYD [1:0]	ASP digital block SYNC signal input switching	0*	Signal after SYNC output
			1	SYNC pin
			2	ELRI pin
			3	ELRO pin
D12	SYPA	DF block sync polarity switching	0*	DF-processing starts in a falling
			1	DF-processing starts in a rising
D11 D10	SYA [1:0]	DF block SYNC signal input switching	0*	Signal after SYNC output
			1	SYNC pin
			2	ELRI pin
			3	ELRO pin
D9	SYPS	Overall system sync polarity switching	0*	Operates at polarity for SYPD, SYPA settings above.
			1	Reverses all polarities for SYPD, SYPA settings above.
D8 D7	SYS [1:0]	SYNC circuit input signal switching selection	0*	Internal SYNC signal
			1	SYNC pin
			2	ELRI pin
			3	ELRO pin
D6	—	Fixed to 0 (zero)	—	—
D5 D4 D3	CKOS1 [2:0]	CKO1 (50 pin) pin output selection	0*	Fixed to L output
			1	fs2 (internal fs × 2)
			2	fs4 (internal fs × 4)
			3	fs8 (internal fs × 8)
			4	fs16 (internal fs × 16)
			5	fs32 (internal fs × 32)
			6	fs64 (internal fs × 64)
			7	Output XI divided by 2
D2 D1 D0	CKOS0 [2:0]	CKO0 (49 pin) pin output selection	0*	Fixed to L output
			1	fs2 (internal fs × 2)
			2	fs4 (internal fs × 4)
			3	fs8 (internal fs × 8)
			4	fs16 (internal fs × 16)
			5	fs32 (internal fs × 32)
			6	fs64 (internal fs × 64)
			7	fs128 (internal fs × 128)

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Command-41h (0100 0001): BOOT

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	BTA9	BTA8	BTA7	BTA6	BTA5	BTA4	BTA3	BTA2	BTA1	BTA0

Bit	Name	Description	Value	Operation
D9 to D0	BTA [9:0]	Self-boot ROM start address	000h to 3FEh	Starts self-boot operation from specified address

Command-42h (0100 0010): DAC-LR

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	ATTL 4	ATTL 3	ATTL 2	ATTL 1	ATTL 0	0	0	0	ATTR 4	ATTR 3	ATTR 2	ATTR 1	ATTR 0

Bit	Name	Description	Value	Operation
D12 to D8	ATTL [4:0]	DAC L channel attenuator value	00h to 1Fh*	Code: 00h 01h 02h ··· 18h 19h ··· 1Fh ATT (dB): 0 –1 –2 –24 ca.–60 ca.–60 Initial value: 1Fh
D4 to D0	ATTR [4:0]	DAC R channel attenuator value	00h to 1Fh*	Code: 00h 01h 02h ··· 18h 19h ··· 1Fh ATT (dB): 0 –1 –2 –24 ca.–60 ca.–60 Initial value: 1Fh

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Command-43h (0100 0011): SIO

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CHSI	0	ISLT1	ISLT0	IBCS1	IBCS0	IFMT1	IFMT0	CHSO 1	CHSO 0	OSLT 1	OSLT 0	OBCS 1	OBCS 0	OFMT 1	OFMT 0

Bit	Name	Description	Value	Operation
D15	CHSI	Serial input (SI) switching	0*	SI0 register ← ADC, SI1 register ← DIN pin
			1	SI1 register ← ADC, SI0 register ← DIN pin
D14	—	Fixed to 0 (zero)	—	—
D13 D12	ISLT [1:0]	Number of serial input slots	0*	16 slots (bit clock = 32 fs)
			1	20 slots (bit clock = 40 fs)
			2	24 slots (bit clock = 48 fs)
			3	32 slots (bit clock = 64 fs)
D11 D10	IBCS [1:0]	Serial input bit length	0*	16 bits
			1	18 bits
			2	20 bits
			3	24 bits
D9 D8	IFMT [1:0]	Serial input format	0*	Pads from the beginning
			1	Pads from the end
			2	I2S format
			3	
D7 D6	CHSO [1:0]	Serial output (SO) switching	0	DOUT pin ← SO0 register
			1	DOUT pin ← SO1 register
			2*	DOUT pin ← SO2 register
			3	
D5 D4	OSLT [1:0]	Number of serial output slots	0*	16 slots (bit clock = 32 fs)
			1	20 slots (bit clock = 40 fs)
			2	24 slots (bit clock = 48 fs)
			3	32 slots (bit clock = 64 fs)
D3 D2	OBCS [1:0]	Serial output bit length	0*	16 bits
			1	18 bits
			2	20 bits
			3	24 bits
D1 D0	OFMT [1:0]	Serial output format	0*	Pads from the beginning
			1	Pads from the end
			2	I2S format
			3	

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Command-44h (0100 0100): RUN-MUTE

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	RUN	MADOFF	DFMUTE	0	IMUTE	OMUTE 2	OMUTE 1	OMUTE 0

Bit	Name	Description	Value	Operation
D15 to D8	—	Fixed to 0 (zero)	—	—
D7	RUN	ASP program execution	0*	Stops program
			1	Runs program
D6	MADOFF	Microphone ADC OFF	0*	Microphone ADC ON
			1	Microphone ADC OFF
D5	DFMUTE	DF block mute	0	Mute OFF
			1*	Mute ON
D4	—	Fixed to 0 (zero)	—	—
D3	IMUTE	ASP block input mute (SI0, SI1 register mute)	0	Mute OFF
			1*	Mute ON
D2	OMUTE2	ASP block output mute (SO2 register mute)	0	Mute OFF
			1*	Mute ON
D1	OMUTE1	ASP block output mute (SO1 register mute)	0	Mute OFF
			1*	Mute ON
D0	OMUTE0	ASP block output mute (SO0 register mute)	0	Mute OFF
			1*	Mute ON

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Command-45h (0100 0101): MSEQ

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0	MSA3	MSA2	MSA1	MSA0

Bit	Name	Description	Value	Operation
D3 to D0	MSA [3:0]	Module sequential RAM first address	0h to Fh	The address of the head to write in is set up.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	MSEQ 10	MSEQ 9	MSEQ 8	MSEQ 7	MSEQ 6	MSEQ 5	MSEQ 4	MSEQ 3	MSEQ 2	MSEQ 1	MSEQ 0

Bit	Name	Description	Value	Operation
D10 to D0	MSEQ [10:0]	Module sequential RAM data	000h to 7FFh	The data written in module sequence RAM are set up. (PC value at the time of SQRET)

Data are sent continuously after transmitting the module sequence RAM head address (2 bytes).
Enable a sequential write to RAM.
45h-MSEQ RAM address (2 bytes)-Data (2 bytes)-Data (2 bytes)-.....-Data (2 bytes)
(module sequential RAM: 16 words)

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Command-46h (0100 0110): CRAM

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	CRAMA 9	CRAMA 8	CRAMA 7	CRAMA 6	CRAMA 5	CRAMA 4	CRAMA 3	CRAMA 2	CRAMA 1	CRAMA 0

Bit	Name	Description	Value	Operation
D9 to D0	CRAMA [9:0]	CRAM (coefficient RAM) head address	000h to 1BFh	CRAM address of the head at the time of writing in by 46h command is set up.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CRAMD 15	CRAMD 14	CRAMD 13	CRAMD 12	CRAMD 11	CRAMD 10	CRAMD 9	CRAMD 8	CRAMD 7	CRAMD 6	CRAMD 5	CRAMD 4	CRAMD 3	CRAMD 2	CRAMD 1	CRAMD 0

Bit	Name	Description	Value	Operation
D15 to D0	CRAMD [15:0]	CRAM data	7FFFh to 8000h	Set CRAM data (two-complement-form formula)

The data written in continuously are sent after transmitting CRAM head address (2 bytes).
Enable a sequential write to RAM.
46h-CRAM address (2 bytes)-Data (2 bytes)-Data (2 bytes)-.....-Data (2 bytes)

Command-47h (0100 0111): CRAM-ACMP

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	CRAMA 9	CRAMA 8	CRAMA 7	CRAMA 6	CRAMA 5	CRAMA 4	CRAMA 3	CRAMA 2	CRAMA 1	CRAMA 0

Bit	Name	Description	Value	Operation
D9 to D0	CRAMA [9:0]	CRAM first address	000h to 1BFh	CRAM address of the head at the time of writing in by 47h command is set up.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CRAMD 15	CRAMD 14	CRAMD 13	CRAMD 12	CRAMD 11	CRAMD 10	CRAMD 9	CRAMD 8	CRAMD 7	CRAMD 6	CRAMD 5	CRAMD 4	CRAMD 3	CRAMD 2	CRAMD 1	CRAMD 0

Bit	Name	Description	Value	Operation
D15 to D0	CRAMD [15:0]	CRAM data	7FFFh to 8000h	Set CRAM data (two-complement-form formula)

It is CRAM write-in command which used the address compare mode. A maximum of 32 words is written at once.

The data written in continuously are sent after transmitting CRAM head address (2 bytes).
Enable a sequential write to RAM.
47h-CRAM address (2 bytes)-Data (2 bytes)-Data (2 bytes)-.....-Data (2 bytes)

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Command-48h (0100 1000): ORAM

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	ORAMA 5	ORAMA 4	ORAMA 3	ORAMA 2	ORAMA 1	ORAMA 0

Bit	Name	Description	Value	Operation
D5 to D0	ORAMA [5:0]	ORAM first address	00h to 3Fh	ORAM address of the head at the time of writing in by 48h command is set up.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ORAMD 15	ORAMD 14	ORAMD 13	ORAMD 12	ORAMD 11	ORAMD 10	ORAMD 9	ORAMD 8	ORAMD 7	ORAMD 6	ORAMD 5	ORAMD 4	ORAMD 3	ORAMD 2	ORAMD 1	ORAMD 0

Bit	Name	Description	Value	Operation
D15 to D0	ORAMD [15:0]	ORAM data	7FFFh to 0000h	Set ORAM data

The data written in continuously are sent after transmitting ORAM head address (2 bytes).
Enable a sequential write to RAM.
48h-ORAM address (2 bytes)-Data (2 bytes)-Data (2 bytes)-.....-Data (2 bytes)
(ORAM: 64 word)

Command-49h (0100 1001): ORAM-ACMP

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	ORAMA 5	ORAMA 4	ORAMA 3	ORAMA 2	ORAMA 1	ORAMA 0

Bit	Name	Description	Value	Operation
D5 to D0	ORAMA [5:0]	ORAM first address	00h to 3Fh	ORAM address of the head at the time of writing in by 49h command is set up.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ORAMD 15	ORAMD 14	ORAMD 13	ORAMD 12	ORAMD 11	ORAMD 10	ORAMD 9	ORAMD 8	ORAMD 7	ORAMD 6	ORAMD 5	ORAMD 4	ORAMD 3	ORAMD 2	ORAMD 1	ORAMD 0

Bit	Name	Description	Value	Operation
D15 to D0	ORAMD [15:0]	ORAM Data	7FFFh to 0000h	Set ORAM data (two-complement-form formula)

It is ORAM write-in command which used the address compare mode. A maximum of 32 words is written at once.
The data written in continuously are sent after transmitting ORAM head address (2 bytes)
Enable a sequential write to RAM.
49h-ORAM address (2 bytes)-Data (2 bytes)-Data (2 bytes)-.....-Data (2 bytes)
(ORAM: 64 word)

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Command-4Ah (0100 1010): IFF

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0	0	IFF2	IFF1	IFF0

Bit	Name	Description	Value	Operation
D2 to D1	IFF [2:0]	Set IFFn n = 2, 1, 0	0*	IFFn = 0
			1	IFFn = 1

Command-4Bh (0100 1011): MONI-PC

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
I2COS 1	I2COS 0	0	0	0	MPC 10	MPC9	MPC8	MPC7	MPC6	MPC5	MPC4	MPC3	MPC2	MPC1	MPC0

Bit	Name	Description	Value	Operation
D15 to D14	I2COS [2:0]	Monitor data length in I^2C mode	0h to 3h	Set the data byte length when monitoring in I^2C mode. Code: 3h 2h 1h, 0h Byte: 3 byte 2 byte 1 byte
D13 to D11	—	Fixed to 0 (zero)	—	—
D10 to D0	MPC [10:0]	Monitor condition (command-50h to 56h)	000h to 7FFh	Set the Program Counter (PC) conditions (PC value) when carrying out a monitor by command-50h to 56h.

Command-4Ch (0100 1100): MONI-LC

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	LCE	LCS	LCDE	LCD7	LCD6	LCD5	LCD4	LCD3	LCD2	LCD1	LCD0

Bit	Name	Description	Value	Operation
D15 to D11	—	Fixed to 0 (zero)	—	—
D10	LCE	Whether LC (loop counter) value applied to monitor conditions or not.	0*	Does not add LC value to the conditions.
			1	Adds LC value to the condition.
D9	LCS	LC selection	0	Compares with LC0 value.
			1	Compares with LC1 value.
D8	LCDE	Automatic LC decrement	0	After a match, does not change the value to be compared with the LC.
			1	After a match, automatically decrements by −1 the value to be compared with the LC.
D7 to D0	LCD [7:0]	Value in comparison with the loop counter when carrying out a monitor	00h to FFh	Set the LC conditions (loop counter value) when carrying out a monitor by command-50h to 56h.

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Command-4Dh (0100 1101): MISC

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	SIS	SOS	ERDET	ZST	DP7F	SYRC	SYRO	MCKE	MCKS	DLSEP	0

Bit	Name	Description	Value	Operation
D15 to D11	—	Fixed to 0 (zero)	—	—
D10	SIS	Serial Input	0*	Master (synchronized with the internal clock)
			1	Slave (synchronized with the external clock (ELRI, EBCI))
D9	SOS	Serial output	0*	Master (synchronized with the internal clock)
			1	Slave (synchronized with the external clock (ELRO, EBCO))
D8	ERDET	Error detection	0	Invalid
			1*	Valid
D7	ZST	Switches to access CROM using Log-Linear adjustment	0	2-cycle access
			1*	1-cycle access
D6	DP7F	128/256 word of DRAM (DATA RAM) switching	0*	256 word
			1	128 word
D5	SYRC	Set CP at each SYNC	0	Does not reset
			1*	Reset
D4	SYRO	Set OFP at each SYNC	0	Does not reset
			1*	Reset
D3	MCKE	MCK pin output enable	0	Disable (fixed to L)
			1*	Enable (output)
D2	MCKS	MCK pin output switching	0	256 fs
			1*	Source oscillation
D1	DLSEP	Delay RAM table area switching	0	Does not use table
			1*	Use 2-k word area as the table
D0	—	Fixed to 0 (zero)	—	—

Command-4Fh (0100 1111): M-RST

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MRST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description	Value	Operation
D15	MRST	Initialization from the micro controller command	0*	Does not initialize
			1	Initializes (set to initial value.)
D14 to D0	—	Fixed to 0 (zero)	—	—

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Command-50h (0101 0000): MON-DB

O 23	O 22	O 21	O 20	O 19	O 18	O 17	O 16	O 15	O 14	O 13	O 12	O 11	O 10	O9	O8	O7	O6	O5	O4	O3	O2	O1	O0
DB 23	DB 22	DB 21	DB 20	DB 19	DB 18	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0

Bit	Name	Description	Value	Operation
O23 to O0	DB [23:0]	Data bus monitor	000000h to FFFFFFh	Reads data bus on the condition: Command-4Bh, 4Ch

Command-51h (0101 0001): MON-CP

O 23	O 22	O 21	O 20	O 19	O 18	O 17	O 16	O 15	O 14	O 13	O 12	O 11	O 10	O9	O8	O7	O6	O5	O4	O3	O2	O1	O0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CP 7	CP 6	CP 5	CP 4	CP 3	CP 2	CP 1	CP 0

Bit	Name	Description	Value	Operation
O23 to O9	—	Fixed to 0 (zero)	—	—
O8 to O0	CP [8:0]	CP monitor (coefficient RAM pointer)	000000h to 0001BFh	Reads CP on the condition: Command-4Bh, 4Ch

Command-52h (0101 0010): MON-OFP

O 23	O 22	O 21	O 20	O 19	O 18	O 17	O 16	O 15	O 14	O 13	O 12	O 11	O 10	O9	O8	O7	O6	O5	O4	O3	O2	O1	O0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	QFP 5	QFP 4	QFP 3	QFP 2	QFP 1	QFP 0

Bit	Name	Description	Value	Operation
O23 to O6	—	Fixed to 0 (zero)	—	—
O5 to O0	OFP [5:0]	OFP monitor (offset RAM pointer)	000000h to 00003Fh	Reads OFP on the condition: Command-4Bh, 4Ch

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Command-53h (0101 0011): MON-DP

O 23	O 22	O 21	O 20	O 19	O 18	O 17	O 16	O 15	O 14	O 13	O 12	O 11	O 10	O9	O8	O7	O6	O5	O4	O3	O2	O1	O0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DP 7	DP 6	DP 5	DP 4	DP 3	DP 2	DP 1	DP 0

Bit	Name	Description	Value	Operation
O23 to O8	—	Fixed to 0 (zero)	—	—
O7 to O0	DP [7:0]	DP monitor (data RAM pointer)	000000h to 0000FFh	Reads DP on the condition: Command-4Bh, 4Ch

Selection (DP0/DP1/DP2/DP3) of DP is DP chosen by command executed at the time of PC set up as conditions.

Command-54h (0101 0100): MON-AR

O 23	O 22	O 21	O 20	O 19	O 18	O 17	O 16	O 15	O 14	O 13	O 12	O 11	O 10	O9	O8	O7	O6	O5	O4	O3	O2	O1	O0
0	0	0	0	0	0	0	0	0	0	0	0	AR 11	AR 10	AR 9	AR 8	AR 7	AR 6	AR 5	AR 4	AR 3	AR 2	AR 1	AR 0

Bit	Name	Description	Value	Operation
O23 to O12	—	Fixed to 0 (zero)	—	—
O11 to O0	AR [11:0]	AR monitor (delay RAM address)	000000h to 000FFFh	Reads delay RAM address on the condition: Command-4Bh, 4Ch

Command-55h (0101 0101): MON-CRP

O 23	O 22	O 21	O 20	O 19	O 18	O 17	O 16	O 15	O 14	O 13	O 12	O 11	O 10	O9	O8	O7	O6	O5	O4	O3	O2	O1	O0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRP 8	CRP 7	CRP 6	CRP 5	CRP 4	CRP 3	CRP 2	CRP 1	CRP 0

Bit	Name	Description	Value	Operation
O23 to O9	—	Fixed to 0 (zero)	—	—
O8 to O0	CRP [8:0]	CRP monitor (CROM pointer)	000000h to 0001FFh	Reads CRP on the condition: Command-4Bh, 4Ch

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Command-56h (0101 0110): MON-SR

O 23	O 22	O 21	O 20	O 19	O 18	O 17	O 16	O 15	O 14	O 13	O 12	O 11	O 10	O9	O8	O7	O6	O5	O4	O3	O2	O1	O0
0	0	0	0	0	0	0	0	0	LRF	GF 3	GF 2	GF 1	GF 0	LI -LG	LG -LI	OV -1E	OV -0E	RD -23	RD -16	V1F	V0F	ZF	SF

Bit	Name	Description	Value	Operation
O23 to O15	—	Fixed to 0 (zero)	—	—
O14 to O0	SR	SR monitor (status register)	—	Reads SR on the condition: Command-4Bh, 4Ch

Command-58h (0101 1000): DF-ATT

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	ATL6	ATL5	ATL4	ATL3	ATL2	ATL1	ATL0

Bit	Name	Description	Value	Operation
D6 to D0	ATL [6:0]	DF attenuator value	00h to 7Fh*	Initial value: 7Fh (level = 0dB) LEVEL = 20 × log (ATL/128)

Code	Level
7Fh	0.00dB
7Eh	−0.14dB
7Dh	−0.21dB
~	~
72h	−1.01dB
65h	−2.06dB
5Ah	−3.06dB
~	~
40h	−6.02dB
~	~
02h	−36.12dB
01h	−42.14dB
00h	−∞dB

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Command-59h (0101 1001): DAC-S

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	ATTSL 4	ATTSL 3	ATTSL 2	ATTSL 1	ATTSL 0	0	0	0	ATTSR 4	ATTSR 3	ATTSR 2	ATTSR 1	ATTSR 0

Bit	Name	Description	Value	Operation
D12 to D8	ATTSL [4:0]	DAC SL-ch attenuator value	00h to 1Fh*	Code: 00h 01h 02h ··· 18h 19h ··· 1Fh ATT (dB): 0 –1 –2 –24 ca.–60 ca.–60 Initial value: 1Fh
D4 to D0	ATTSR [4:0]	DAC SR-ch attenuator value	00h to 1Fh*	Code: 00h 01h 02h ··· 18h 19h ··· 1Fh ATT (dB): 0 –1 –2 –24 ca.–60 ca.–60 Initial value: 1Fh

Command-5Ah (0101 1010): DAC-C

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	ATTC 4	ATTC 3	ATTC 2	ATTC 1	ATTC 0

Bit	Name	Description	Value	Operation
D4 to D0	ATTC [4:0]	DAC C-ch attenuator value	00h to 1Fh*	Code: 00h 01h 02h ··· 18h 19h ··· 1Fh ATT (dB): 0 –1 –2 –24 ca.–60 ca.–60 Initial value: 1Fh

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4. Self-Boot Function Description

4.1 Self-Boot Function

The TC9496AF supports a self-boot function for setting coefficients and offsets.

As Figure 1 shows, the data are set via the microcontroller interface circuit.

First saving the data to be set via the microcontroller in the self-boot ROM (SBROM) allows various modes to be set later. The microcontroller interface circuit supports two format: I^2C and the original mode. However, the boot must be executed in Standard Transmission.

All the command inputs from the exterior are disregarded during a boot term.

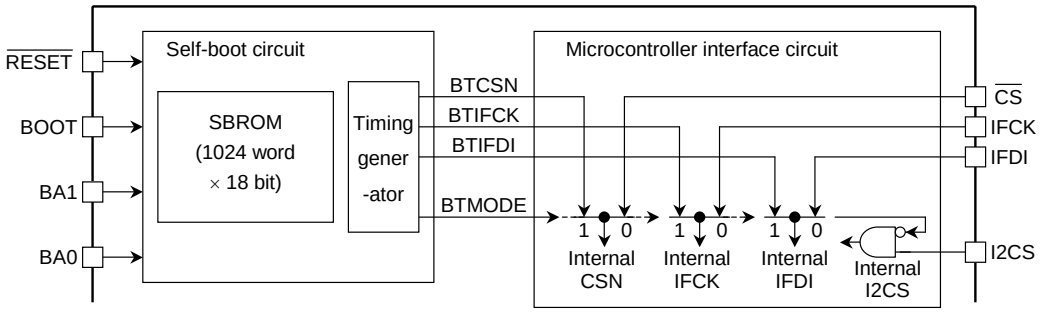

Figure 1 Self-Boot System

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4.2 Boot ROM Format

The following shows the brake down of the 18 bits.

00	Data that are being sent
01	Command
10	Final data (after the data are sent, the $\overline{CS}$ signal is set to "H").
11	Jump address (jump to any address in the self-boot ROM).

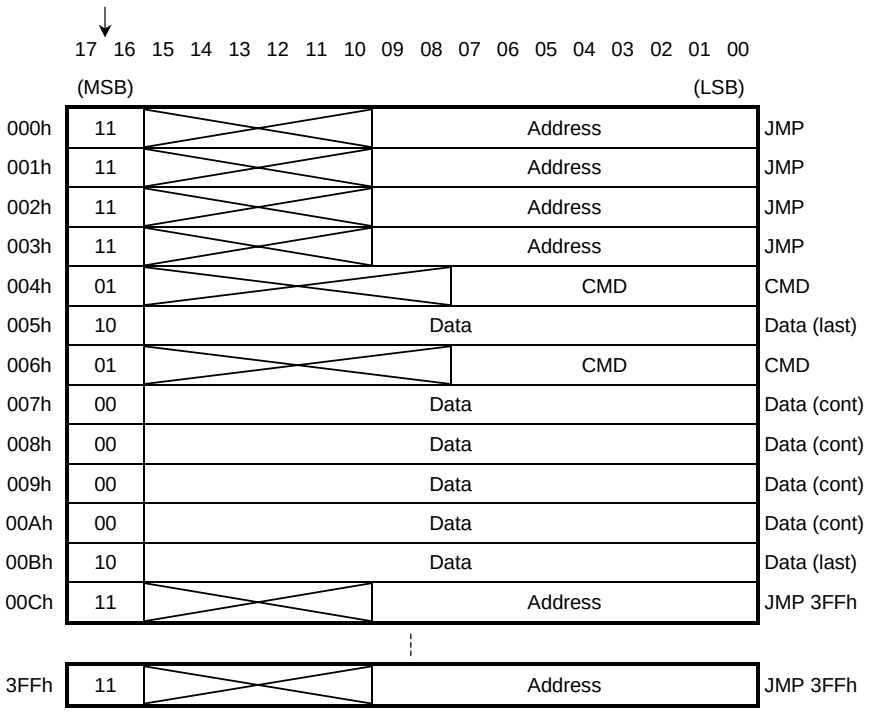

Figure 2 Boot ROM Format and Example

Note 3: Boot mode completes when the address reaches 3FFh, the maximum value. Therefore, for the final address, write JMP 3FFh (data = 303FFh).

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4.3 Self-Boot Operation

Self-boot operations support two modes: one for use at reset and for setting the microcontroller. The modes can be used in combination.

4.3.1 Self-Boot Operation

To enter this mode, set the Boot pin to High, then set the $\overline{\text{RESET}}$ pin to Low or send initialized command.

The 2048 fs period (46.4 ms when fs = 44.1 kHz) after a reset release is wait period. The boot operation starts at the end of this period.

When switching the setting according to application, specify the start address using the BA [1:0] pin. At addresses 000h to 002h, set jump addresses.

The data setting speed is one of SBROM per 1 fs. As up to 1024 words can be set in the SBROM, the maximum time required for setting the data is the 1024 fs period.

Table 1 Relationship between fs and Wait Period

fs	Wait Period	Boot Time (max.)
32 kHz	64.0 ms	32.0 ms
44.1 kHz	46.4 ms	23.2 ms
48 kHz	42.7 ms	21.3 ms

Table 2 Relationship between BA [1:0] Pin Value and Start Address

BA1	BA2	Start Address
0	0	000h
0	1	001h
1	0	002h
1	1	003h

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4.3.2 Self-Boot Operation when Setting Microcontroller

In this mode, the microcontoroller can specify any address and the boot operation starts from that address.

The BOOT pin can be set to either High or Low. Setting the self-boot ROM start address using the BOOT command (command: 41h) from the microcontroller starts the boot operation with no wait. The boot operation when set from the microcontroler is the same as the self-boot operation at reset except that the boot operation can start from any address.

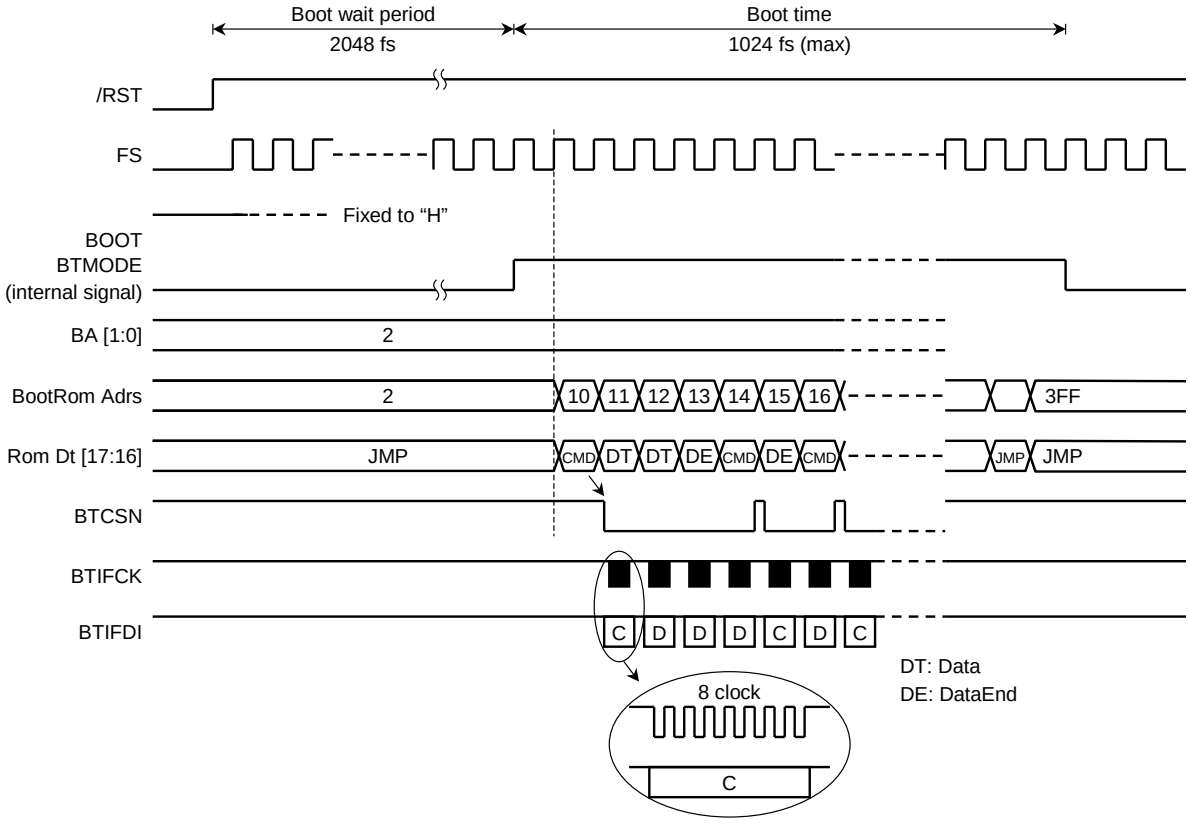

Figure 3 Boot Timing Chart (at reset)

Table 3 Differences Depending on Operation Mode

Parameter	$\overline{\text{RESET}}$ Pin or Initialized Command	BOOT Command
Boot Wait Period	Yes	No
Boot Start Address	Select from 000h to 003h with BA0 and BA1 terminal	Any address specified from microcontroller
BOOT pin	"H" Level	Any (don't care)

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4.4 Programming Examples

The following shows the programming example in Self-boot mode.

```
000: 30040h     jmp   040h       ; Jump to 040h
001: 30100h     jmp   100h       ; Jump to 100h
002: 30200h     jmp   200h       ; Jump to 200h
003: 30004h     jmp   004h       ; Jump to 004h
004: 10040h     cmd   40h        ; Command 40h (TIMING)
005: 28007h     data  8007h      ; CKOS0 = 7 (fs128 output)
006: 10043h     cmd   43h        ; Command 43h (SIO)
007: 20039h     date  0039h      ; CHSO = 0 (SO0), OSLT = 3 (32 bit), OBCS = 2 (20 bit),
                                   OFMT = 1 (padded from the end)
008: 10045h     cmd   45h        ; Command 45h (MSEQ)
009: 00000h     data  0000h      ; Start address = 0h
00A: 00001h     data  0001h      ; MSEQ [0] = 001h
00B: 00123h     data  0123h      ; MSEQ [1] = 123h
00C: 20320h     data  0320h      ; MSEQ [2] = 320h
00D: 30300h     jmp   300h       ; Jump to 300h
  :
100: 10046h     cmd   46h        ; Command 46h (CRAM)
101: 00000h     data  0000h      ; Start address = 0h
102: 00000h     data  0000h      ; CRAM [0] = 0000h
103: 00000h     data  0000h      ; CRAM [1] = 0000h
104: 00000h     data  0000h      ; CRAM [2] = 0000h
105: 20000h     data  0000h      ; CRAM [3] = 0000h
106: 30380h     jmp   380h       ; Jump to 380h
  :
300: 10046h     cmd   46h        ; Command 46h (CRAM)
301: 00000h     date  0000h      ; Start address = 0h
302: 07FFFh     data  7FFFh      ; CRAM [0] = 7FFFh
303: 08000h     data  8000h      ; CRAM [1] = 8000h
304: 03FFFh     data  3FFFh      ; CRAM [2] = 3FFFh
305: 24000h     data  4000h      ; CRAM [3] = 4000h
306: 30380h     jmp   380h       ; Jump to 380h
  :
380: 10046h     cmd   46h        ; Command 46h (CRAM)
381: 00080h     data  0080h      ; Start address = 80h
382: 0FFFEh     data  FFFEh      ; CRAM [80h] = FFFEh
383: 2FFFFh     data  FFFFh      ; CRAM [81h] = FFFFh
384: 303FFh     jmp   3FFh       ; Jump to 3FFh
  :
3FF: 303FFh     jmp   3FFh       ; Jump to 3FFh
```


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5. Cautions on Use

5.1 Initial Reset

After a power-supply injection, once at least, please set up a required register after applying reset which makes $\overline{\text{RESET}}$ terminal "L" level and making the value of an internal register data.

5.2 The Cautions at the Time of Using IFOK Terminal

The timing which outputs IFOK signal is the signal which shows whether the command received from the microcomputer was performed normally.

Since the initial value of IFOK signal is unfixed when a control microcomputer is checking IFOK signal, before sending a command, it may stop performing control from a microcomputer.

5.3 The Cautions at the Time of Using ACMP (address compare mode)

In rewriting coefficient data and offset data using ACMP mode, please do not use it the following condition.

5.3.1 Please do not Transmit the Following Command before Completing Rewriting of Data.

Please do not send the following command before completing rewriting of data of CRAM or ORAM.

Please check that waiting the term after rewriting has been completed until it transmits the following command was carried out, or rewriting has been completing using IFOK signal.

5.3.2 Please do not Include Data of an Intact Address.

Please do not include coefficient data of offset data of address which are not used by the program under execution, into transmitting data. When data of an intact address is contained, operation in ACMP mode cannot de ended. If the following command is transmitted in this state, RAM data will become unfixed also by the command with the command unrelated to CRAM or ORAM.

It needs to reset and all data needs to be reset up to interrupt before completing rewriting of data in the rewriting processing.

5.3.3 Please do not Perform Continuation Transmission Over the 0^{th} Address.

The transmission over the 0^{th} address may incorrect-operate.

The same of this restriction is said not only of ACMP mode but continuation transmission of usual RAM data.

For example, when writing in 1B8h from 1BFh and 007h from 000h or CRAM, it must transmit in two steps.

5.4 The Handling of NC Terminal

Please use NC terminal by either of the following.

31 pin and 37 pin

- Open (non-connection)
- Connect to V_{DD}
- Connect to GND

81 pin

- Open (non-connection)
- Connect to V_{DD}

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Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{DD}	−0.3 to 6.0	V
Input voltage	V_{in}	−0.3 to V_{DD} + 0.3	V
Power dissipation	P_D	1500	mW
Operating temperature	T_{opr}	−40 to 75	°C
Storage temperature	T_{stg}	−55 to 150	°C

Electrical Characteristics
(unless otherwise noted, Ta = 25°C, V_{DD} = V_{DX} = V_{DDR} = V_{DM} = V_{DL} = V_{DR} = V_{DX} = V_{DAL} = V_{DAR} = V_{DAC} = V_{DAS} = V_{DASR} = 5.0 V)

DC Characteristics

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Operating power supply voltage	V_{DD}	—	Ta = −40 to 75° C	4.75	5.0	5.25	V
Operating frequency range	f_{opr}	—	340 step mode	8	15	25	MHz
			511 step mode	12	33.8	37	
Operating power supply current	I_{DD}	—	f_{opr} = 36.864 MHz, 511-step mode	—	150	165	mA

Clock pins (XI, XO)

Characteristics		Symbol	Test Circuit	Test Condition		Min	Typ.	Max	Unit
Input voltage (1)	"H" level	V_{IH1}	—	XI pin		V_{DD} × 0.7	—	V_{DD} + 0.3	V
	"L" level	V_{IL1}				—	—	V_{DD} × 0.3	
Output voltage (1)	"H" level	V_{OH1}	—	I_{OH} = −3.0 mA	XO pin	V_{DD} − 0.5	—	—	V
	"L" level	V_{OL1}		I_{OL} = 5.0 mA		—	—	0.5	

Input Pins

Characteristics		Symbol	Test Circuit	Test Condition		Min	Typ.	Max	Unit
Input voltage (2)	"H" level	V_{IH2}	—	(Note 4)		V_{DD} × 0.8	—	—	V
	"L" level	V_{IL2}				—	—	V_{DD} × 0.2	
Input leakage current	"H" level	I_{IH2}	—	V_{IN} = V_{DD}	(Note 4) (Note 5)	—	—	10	μA
	"L" level	I_{IL2}		V_{IN} = 0 V		−10	—	—	

Note 4: STEP0 to 1, $\overline{\text{RESET}}$, SYNC, ELRO, ELRI, EBCO, EBCI, DIN, EM0 to 1, I2CS, $\overline{\text{CS}}$, IFCK, IFDI, BOOT, BA0 to BA1, TST0 to 3 (normally input pins and schmitt input pins)

Note 5: XI

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Output Pins

Characteristics		Symbol	Test Circuit	Test Condition		Min	Typ.	Max	Unit
Output voltage (2)	"H" level	V_{OH2}	—	I_{OH} = −2.0 mA	(Note 6)	V_{DD} − 0.5	—	—	V
	"L" level	V_{OL2}		I_{OL} = 2.0 mA		—	—	0.5	
Output voltage (3)	"L" level	V_{OL3}	—	I_{OL} = 4.0 mA	(Note 7)	—	—	0.5	V
Output open leakage current		I_{OZ4}	—	$V_{OH} = V_{DD}$	(Note 7)	—	—	±10	μA

Note 6: FS, CKO0 to 1, MCK, DOUT, IFDO (normally output)

Note 7: IFDI (when I^2C mode output), IFOK, $\overline{ERR}$ (open drain output)

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AC Characteristic

AD Converter (1): LIN, RIN pins

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Maximum input signal level	V_i	—	Input level that ADC output at full-scale digital output (Note 8)	1.18	1.27	—	Vrms
Input impedance	Z_{in}	—	LIN, RIN pins (Note 8)	—	27	—	kΩ
S/(N + D) ratio	S/N_{a1}	—	A-Weight, X'tal: 36.864 MHz (Note 8)	88	96	—	dB
	S/N_{a2}	—	CCIR-ARM, X'tal: 36.864 MHz (Note 8)	85	93	—	dB
THD + N	THD_a	—	20 kHz LPF, X'tal: 36.864 MHz (Note 8)	—	−80	−72	dB
Cross-talk	CT_a	—	20 kHz LPF, X'tal: 36.864 MHz (Note 8)	—	−90	−83	dB
Dynamic range	DR_a	—	A-Weight, X'tal: 36.864 MHz (Note 8)	85	92	—	dB

Note 8: Input channels: LIN, RIN

AD Converter (2): MIN pin

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Maximum input signal level	V_{iM}	—	Input level that ADC output at full-scale digital output (Note 9)	—	1.1	1.15	Vrms
Input impedance	Z_{inM}	—	MIN pin (Note 9)	—	1	—	kΩ
S/(N + D) ratio	S/N_{aM}	—	A-Weight, X'tal: 36.864 MHz (Note 9)	70	80	—	dB
THD + N	THD_{aM}	—	20 kHz LPF, X'tal: 36.864 MHz (Note 9)	—	−62	−53	dB
Cross-talk	CT_{aM1}	—	X'tal: 36.864 MHz LIN, RIN → MIN (Note 10)	—	−76	−60	dB
	CT_{aM2}	—	X'tal: 36.864 MHz MIN → LIN, RIN (Note 10)	—	−90	−83	dB
Dynamic range	DR_{aM}	—	A-Weight, X'tal: 36.864 MHz (Note 9)	70	80	—	dB

Note 9: Input channels: MIN

Note 10: Input channels: LIN, RIN, MIN

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DA Converter

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output signal level	A_o	—	Output voltage at full-scale digital input (Note 10)	1.23	1.33	1.43	Vrms
S/Nratio	S/N_d	—	A-Weight, X'tal: 36.864 MHz	90	98	—	dB
THD + N	THD_d	—	20 kHz LPF, X'tal: 36.864 MHz	—	−84	−75	dB
Cross-talk	CT_d	—	20 kHz LPF, X'tal: 36.864 MHz	—	−90	−83	dB
Dynamic range	DR_d	—	A-Weight, X'tal: 36.864 MHz	87	95	—	dB

Timing

Clock Input Pins (XI)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Clock cycle	t_{XI}	—	—	29	—	—	ns
Clock "H" cycle width	t_{XIH}	—	—	—	14.5	—	ns
Clock "L" cycle width	t_{XIL}	—	—	—	14.5	—	ns

Reset Pin ($\overline{\text{RESET}}$)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Standby time	t_{RRS}	—	—	10	—	—	ms
Reset pulse width	t_{WRS}	—	—	1.0	—	—	μs

Timing Output

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
CKO output delay time	t_{DFC}	—	—	−150	—	150	ns

Audio Serial Interface (EBCI, DIN, EBCO, DOUT)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
ELRI hold time	t_{LIH}	—	—	−75	—	75	ns
DIN setup time	t_{SDI}	—	—	50	—	—	ns
DIN hold time	t_{HDI}	—	—	50	—	—	ns
EBCI clock cycle	t_{EBCI}	—	—	300	—	—	ns
EBCI clock "H" cycle width	t_{EBIH}	—	—	150	—	—	ns
EBCI clock "L" cycle width	t_{EBIL}	—	—	150	—	—	ns
ELRO hold time	t_{LOH}	—	—	−75	—	75	ns
DOUT output delay time (1)	t_{DO1}	—	—	—	—	60	ns
DOUT output delay time (2)	t_{DO2}	—	—	—	—	60	ns
EBCO clock cycle	t_{EBCO}	—	—	300	—	—	ns
EBCO clock "H" cycle width	t_{EBOH}	—	—	150	—	—	ns
EBCO clock "L" cycle width	t_{EBOL}	—	—	150	—	—	ns

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Microcontroller Interface

(1) Standard transmission mode ($\overline{CS}$, IFCK, IFDI, IFDO)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Standby time	t_{STB}	—	—	1.0	—	—	μs
$\overline{CS}$ (fall)-IFCK (fall) setup time	t_{CCD}	—	—	0.2	—	—	μs
IFCK "L" cycle width	t_{WLC}	—	—	0.25	—	—	μs
IFCK "H" cycle width	t_{WHC}	—	—	0.25	—	—	μs
IFCK (rise)-$\overline{CS}$ (rise) setup time	t_{CKC}	—	—	0.2	—	—	μs
$\overline{CS}$ "H" cycle time	t_{WCS}	—	(Note 11)	0.5	—	—	μs
IFDI-IFCK (rise) setup time	t_{SCD}	—	—	0.2	—	—	μs
IFCK (rise)-IFDI hold time	t_{HCD}	—	—	0.2	—	—	μs
IFCK (fall)-IFDO propagation delay time	t_{DDO}	—	C_L = 30 pF	—	—	0.2	μs

Note 11: The command which is "Sync" in the transfer Sync with Sync signal of a 19 page table 1 control command table needs to set the $\overline{CS}$ = H section to a minimum of 1 fs more until it transmits the follwing command. (It needs more than 22.68 μs at fs = 44.1 KHz.)

(2) I^2C mode ($\overline{CS}$, IFCK, IFDI)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
IFCK clock frequency	t_{IFCK}	—	C_L = 400 pF	0	—	400	kHz
IFCK "H" cycle width	t_H	—	C_L = 400 pF	0.6	—	—	μs
IFCK "L" cycle width	t_L	—	C_L = 400 pF	1.3	—	—	μs
Data setup time	t_{DS}	—	C_L = 400 pF	0.1	—	—	μs
Data hold time	t_{DH}	—	C_L = 400 pF	0	—	—	μs
Transmission start condition hold time	t_{SCH}	—	C_L = 400 pF	0.6	—	—	μs
Repeat transmission start setup time	t_{SCS}	—	C_L = 400 pF	0.6	—	—	μs
Transmission end condition setup time	t_{ECS}	—	C_L = 400 pF	0.6	—	—	μs
Data transmission interval	t_{BUF}	—	C_L = 400 pF	1.3	—	—	μs
I^2C rising time	t_R	—	C_L = 400 pF	—	—	0.3	μs
I^2C falling time	t_F	—	C_L = 400 pF	—	—	0.3	μs

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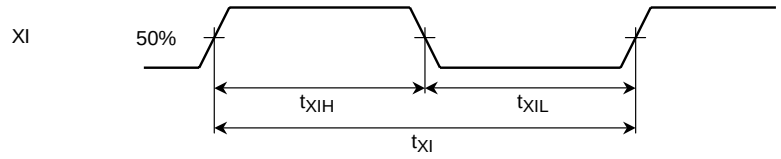
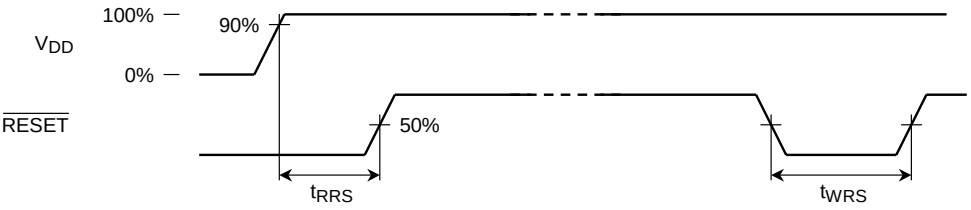
AC Characteristic Measurement Point

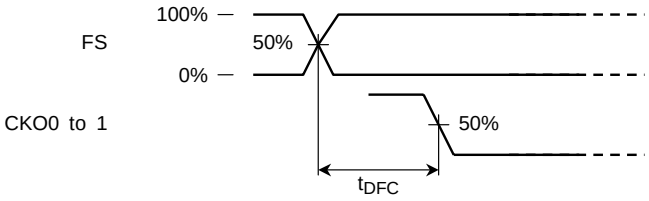
(1) Clock Pin (XI)



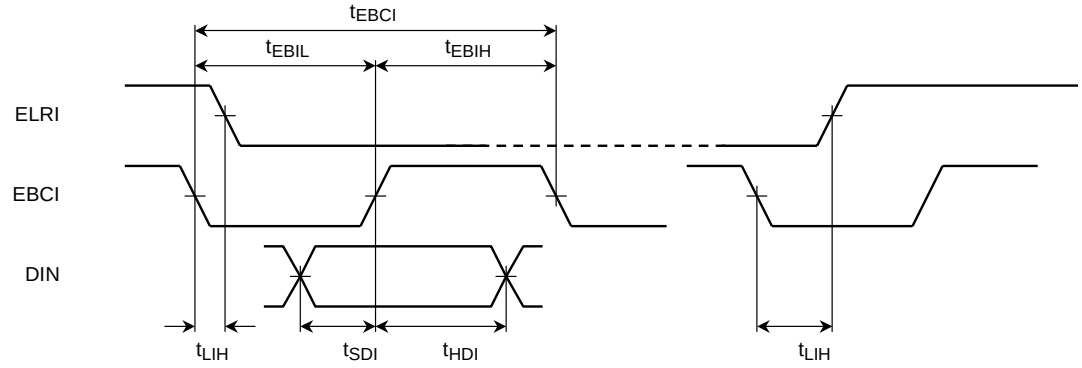
(2) Reset

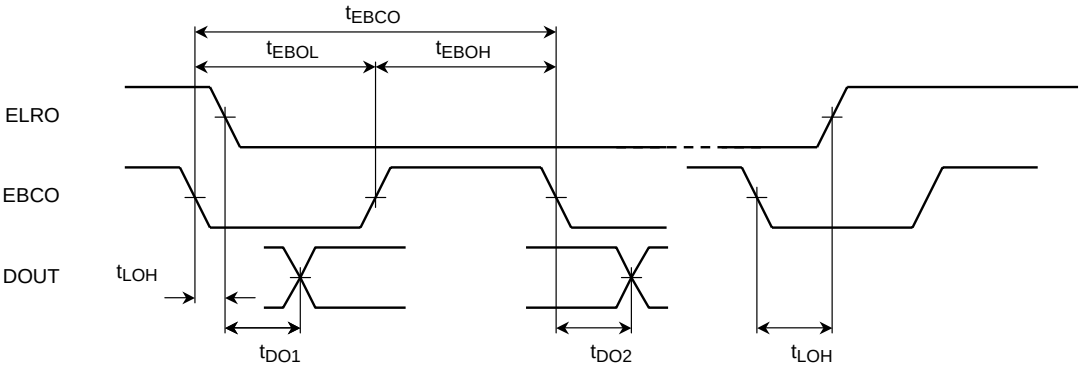


(3) Timing output



(4) Audio serial interface (ELRI, EBCI, DIN, ELRO, EBCO, DOUT)





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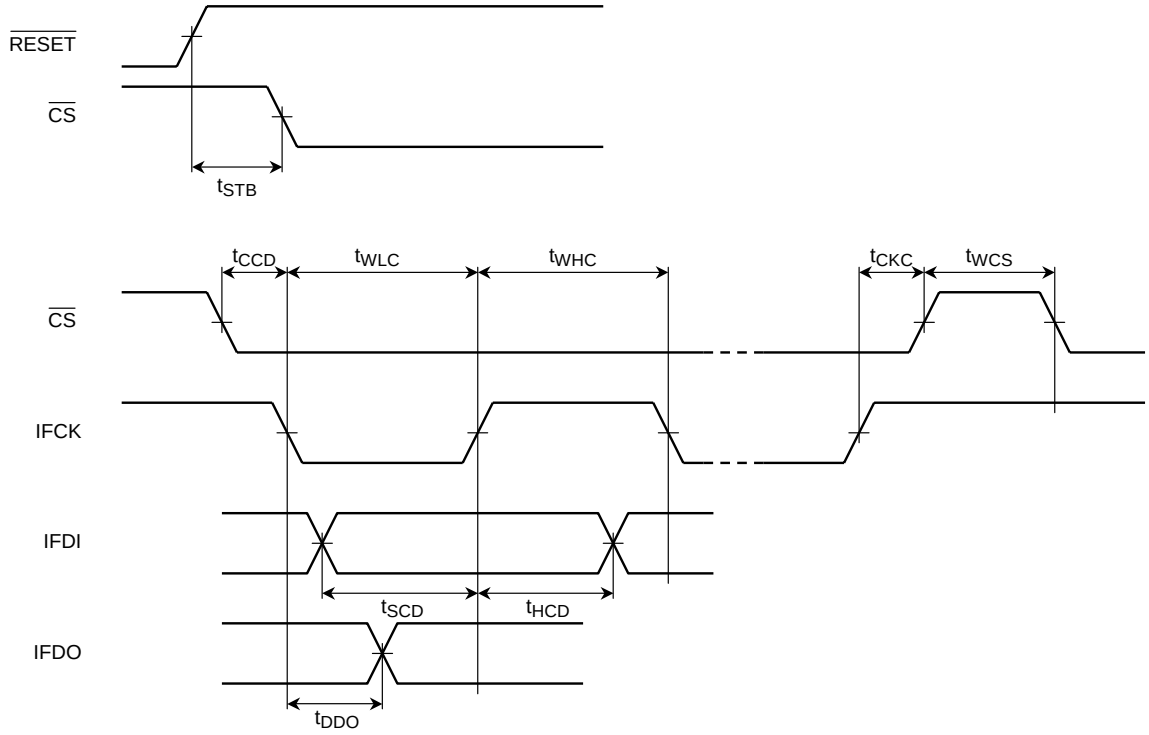
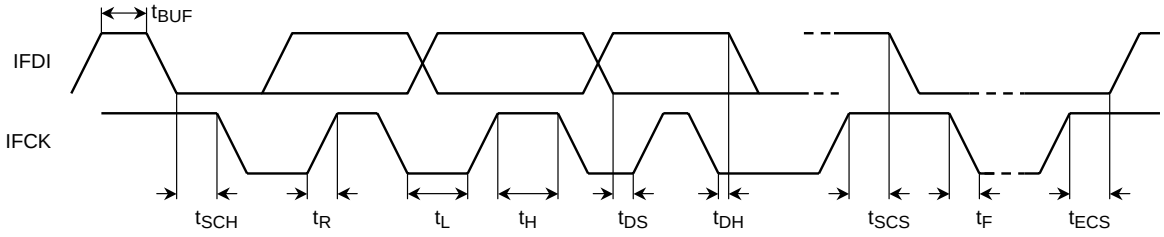
(5) Microcontroller interface in standard transmission mode ($\overline{CS}$, IFCK, IFDI, IFDO)



(6) Microcontroller interface in I^2C mode (IFCK, IFDI)



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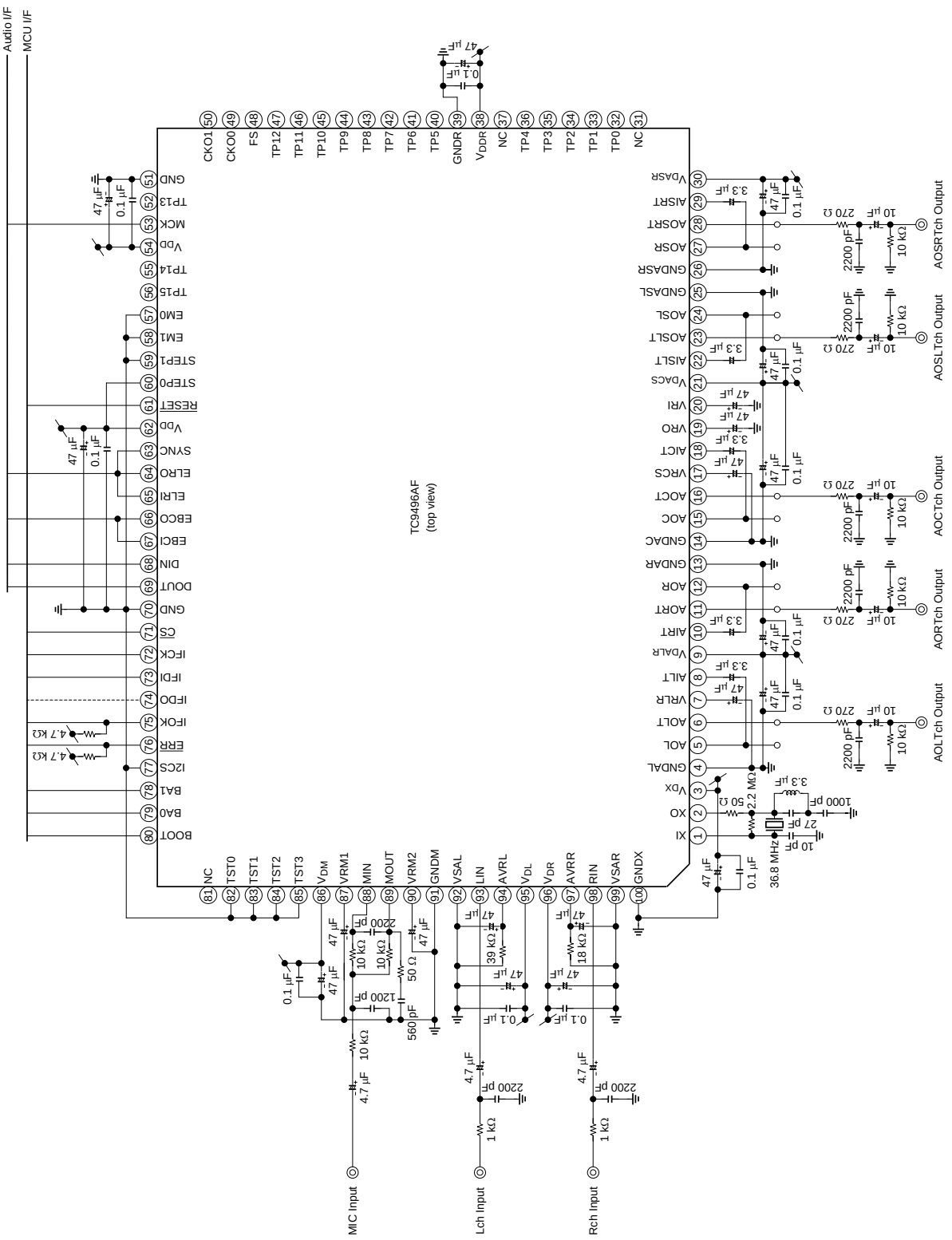
Peripheral Circuit Example

The circuit below is an example circuit only. The operation of this circuit is not guaranteed by Toshiba.



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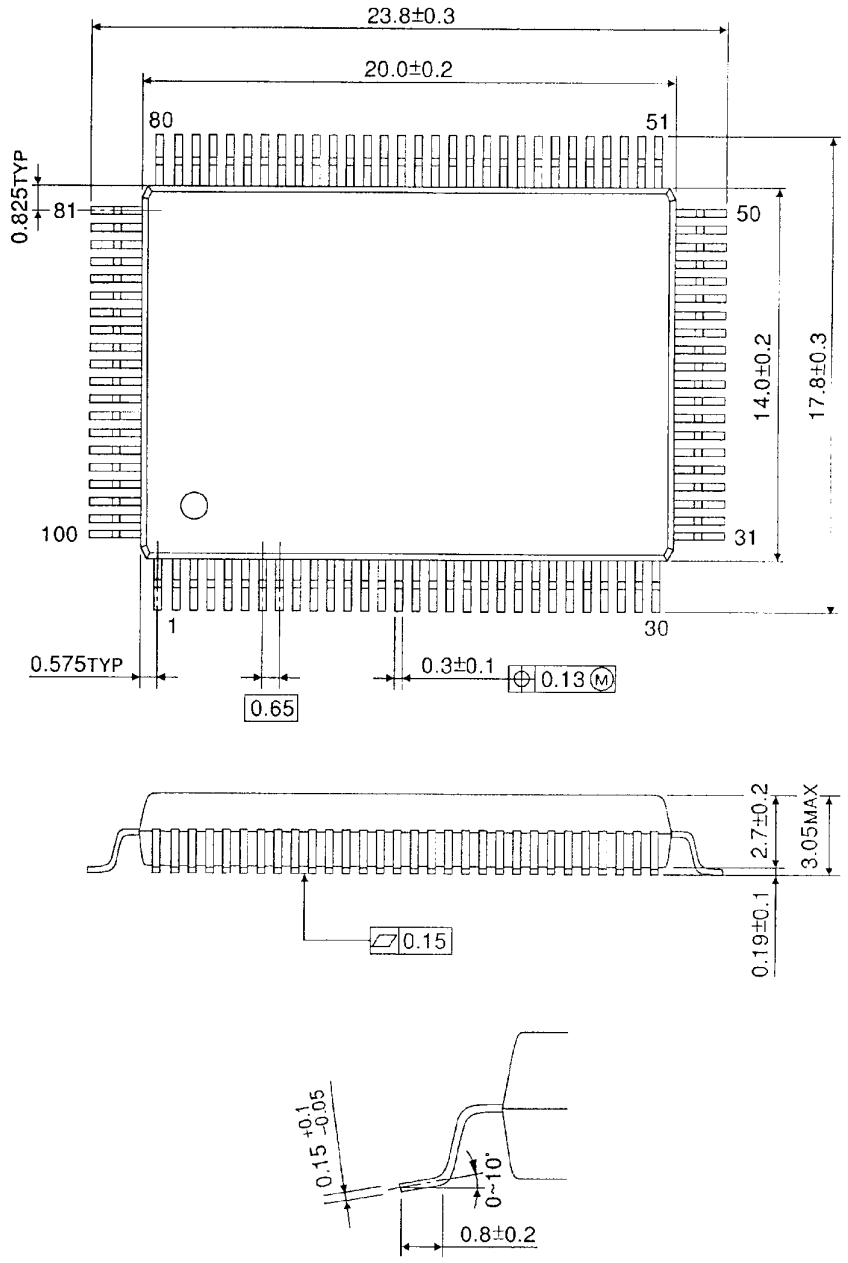
Package Dimensions

QFP100-P-1420-0.65A Unit : mm



Weight: 1.57 g (typ.)

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