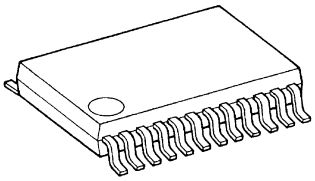
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC9404FNG

Σ-Δ Modulation System DA Converter with Analog Filter

TC9404FNG is a 2'nd order Σ-Δ modulation system 1-bit DA converter incorporating an 8-times over sampling digital filter and analog filter developed for digital audio equipment.

Because the IC includes an analog filter, it can output a direct analog waveform, thus reducing the size and cost of the DA converter.



P-SSOP24-300-0.65A

Weight: 0.14 g (typ.)

Features

- Built-in 8-times over sampling digital filter
- Low-voltage operates (3.0 V) possible
- Built-in digital de-emphasis filter
- In serial mode, output amplitude can be set in 128 steps of resolution using microcontroller command.
- In parallel mode, soft mute can beset for the output signal in 64 steps in 20 ms.
- Built-in LR common digital zero detection output circuit
- Over sampling ratio (OSR) of Σ-Δ modulation circuit is 192 fs
- Support double speed operation
- Sampling frequency: 44.1 kHz, 32 kHz, 48 kHz
- Built-in 3'rd order analog filter
- The digital filter and DA converter characteristics are as follows:

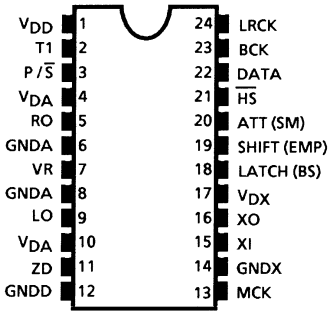
Digital Filter (fs = 44.1 kHz)

	DIGITAL FILTER	PASS-BAND RIPPLE	TRANSIENT BAND WIDTH	STOP BAND SUPPRESSION
Standard Operation	8 fs	±0.11 dB	20 k~24.1 kHz	−26 dB or less
Double Speed Operation	8 fs	±0.11 dB	20 k~24.1 kHz	−26 dB or less

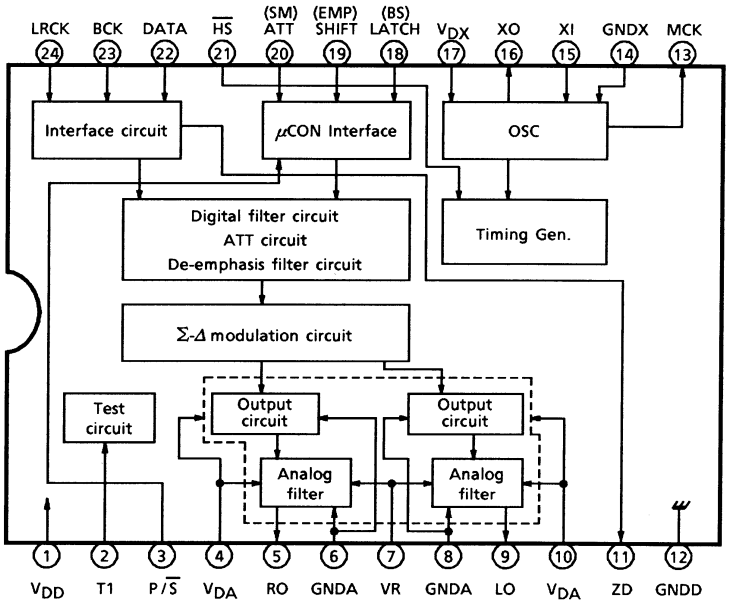
DA Converter (V_{DD} = 5 V)

	OSR	NOISE DISTORTION	S/N
Standard Operation	192 fs	−85 dB (Typ.)	96 dB (Typ.)
Double Speed Operation	96 fs	−85 dB (Typ.)	86 dB (Typ.)

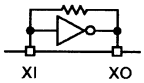
Pin Assignment



Block Diagram



Pin Function

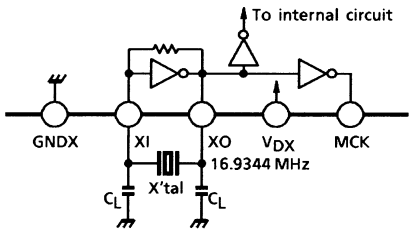
Pin No.	Symbol	I/O	Function	Remarks
1	V_{DD}	—	Digital block power supply pin.	
2	T1	I	Test pin. Always set to “Low” level.	
3	P/$\overline{S}$	I	Parallel/serial mode select pin.	
4	V_{DA}	—	Analog power supply pin.	
5	RO	O	Right channel analog signal output pin.	
6	GNDA	—	Analog GND pin.	
7	VR	—	Reference voltage pin.	
8	GNDA	—	Analog GND pin.	
9	LO	O	Left channel analog signal output pin.	
10	V_{DA}	—	Analog power supply pin.	
11	ZD	O	Digital zero detection output pin.	
12	GNDD	—	Digital GND pin.	
13	MCK	O	System clock output pin.	
14	GNDX	—	Crystal oscillator GND pin.	
15	XI	I	Crystal oscillator connecting pin. Generates the clock required by the system.	
16	XO	O		
17	V_{DX}	—	Crystal oscillator power supply pin.	
18	LATCH (BS)	I	Serial mode: Data latch signal input pin. Parallel mode: De-emphasis filter mode select pin.	Schmitt input
19	SHIFT (EMP)	I	Serial mode: Shift clock input pin. Parallel mode: De-emphasis filter control pin.	Schmitt input
20	ATT (SM)	I	Serial mode: Data input pin. Parallel mode: Soft mute control pin.	Schmitt input
21	$\overline{HS}$	I	Standard/double speed operation mode switching pin. Standard operation at “H”, double speed operation at “L”.	
22	DATA	I	Audio data input pin.	
23	BCK	I	Bit clock input pin.	
24	LRCK	I	LR clock input pin.	

Description of Block Operations

1. Crystal Oscillator Circuit and Timing Generator

The clock required for internal operations is generated by connecting a crystal and condensers as shown in the diagram below.

The IC will also operate when a system clock is input from an external source through the XI pin (pin 15). However, in this situation, due consideration must be given to the fact that waveform characteristics, such as jitter and rising/falling characteristics of the system clock, significantly affect the DA converter's noise distortion and the S/N ratio.



C_L = 10~33 pF

Use a crystal with a low CI value and favorable start-up characteristics.

Figure 1 Crystal Oscillation Circuit Configuration (when in the 384 fs mode)

The timing generator generates the clocks and process timing signals required for such functions as digital filtering and de-emphasis filtering.

2. Data Input Circuit

DATA and the LRCK are loaded to the LSI internal shift registers on the BCK signal rising edge. It is consequently necessary for the DATA and LRCK signals to be synchronized and input on the BCK signal falling edge as indicated in the timing example below. Also, as DATA has been designed so that the 16 bits before the change point of LRCK are regarded as valid data, the data must be input with Right-justified mode when the BCK is 48 fs or 64 fs, as shown in Figure 2b.

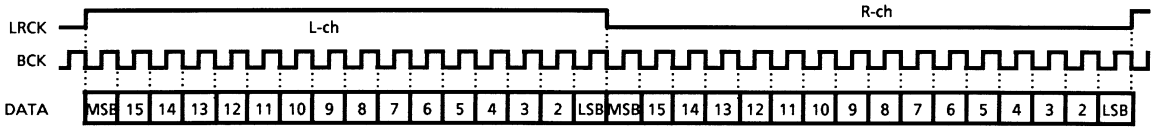


Figure 2a Example of Input Timing Chart

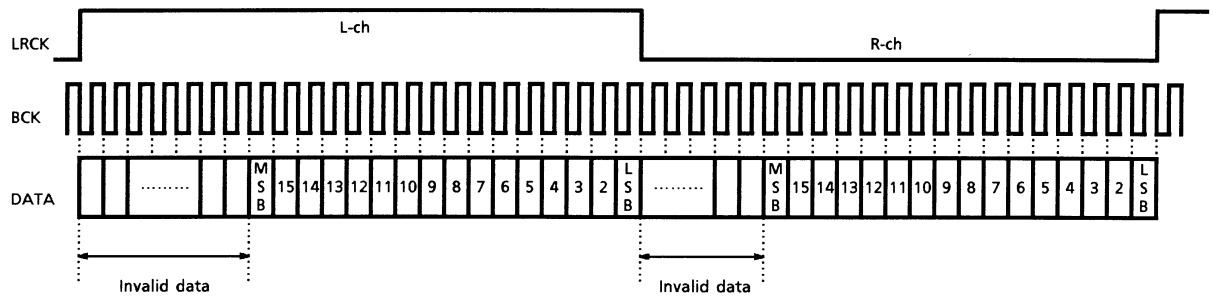


Figure 2b Example of Input Timing Chart

3. Digital Filter

The 8-times oversampling IIR digital filter eliminates the noise returned from outside the bandwidth during standard and double speed operations.

Table 1 Basic Characteristics of Digital Filter

	Pass-Band Ripple	Transient Bandwidth	Attenuation
Standard operation	±0.11dB	20.0 k~24.1 kHz	−26dB or less
Double speed operation	±0.11dB	20.0 k~24.1 kHz	−26dB or less

The characteristics of the digital filter frequencies are shown below.

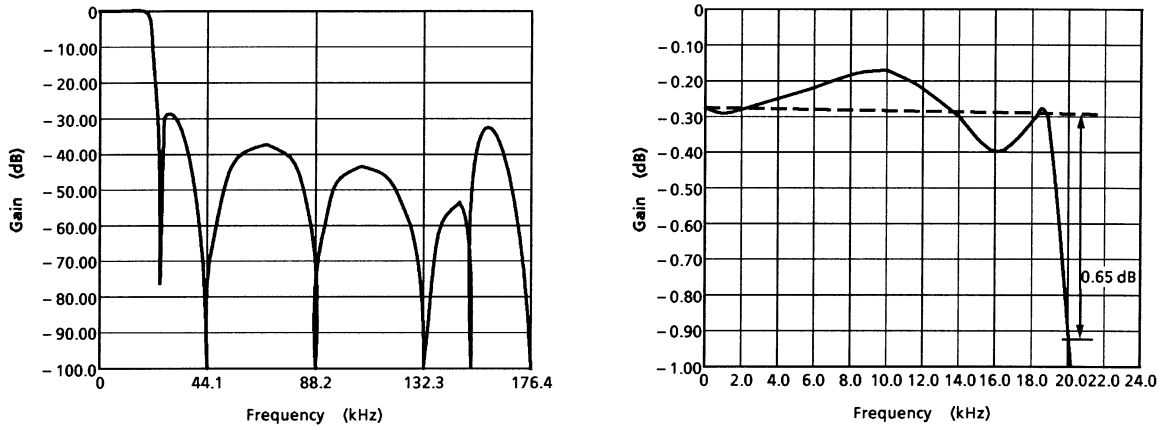


Figure 3 Digital Filter Frequency Characteristics (fs = 44.1 kHz)

4. De-Emphasis Filter

The built-in digital de-emphasis circuit is available for three kind of sampling frequency, fs of 32 kHz, 44.1 kHz, and 48 kHz. These setting controlled in the parallel mode ($P/\overline{S}$ = "H") with the LATCH (BS) pin (pin 18) and SHIFT (EMP) pin (pin 19).

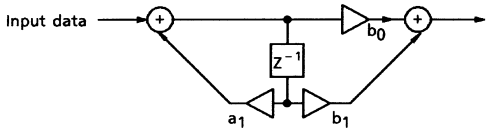
This is set in the serial mode ($P/\overline{S}$ = "L") with a microcontroller or other equipment. (refer to 9-2 microcontroller setting mode for further details on serial mode settings.)

Table 2 De-Emphasis Filter Setting (when in the parallel mode)

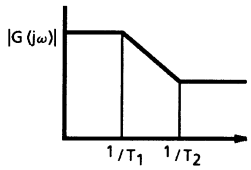
LATCH (BS)	H	H	L	L	
SHIFT (EMP)	H	L	H	L	
MODE (fs SELECT)	32	48	44.1	OFF	(kHz)

The digitalization of the de-emphasis filter eliminates the need for such external components as resistors, condensers and analog switches. In addition to this, the coefficients are aligned to reduce error in the de-emphasis filter characteristics.

The filter structure and characteristics are shown below.



Transfer function: $H(Z) = \dfrac{(b_0 + b_1 Z^{-1})}{(1 - a_1 Z^{-1})}$



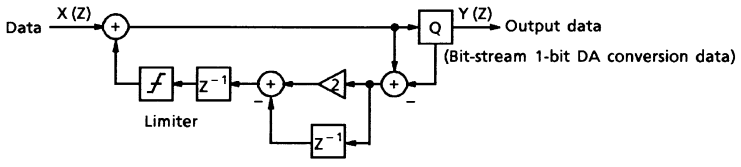
$T_1 = 50\ \mu s$, $T_2 = 15\ \mu s$

Figure 4 IIR Digital De-Emphasis Filter

Figure 5 Filter Characteristics

5. DA Conversion Circuit

The IC incorporates a 2'nd Σ-Δ modulation DA converter for two channels (simultaneous output type). The internal structure of this is shown in Figure 6.



2'nd ∑-Δ converter: $Y(Z) = X(Z) + (1 - Z^{-1})^2 Q(Z)$

Figure 6 Σ-Δ Modulation DA Converter

The Σ-Δ modulation clock has been designed to operate at 192 fs. The noise shaping characteristics are shown in Figure 7.

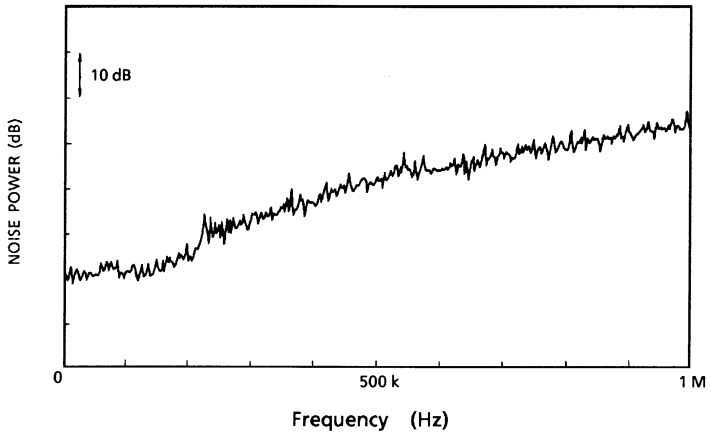


Figure 7 Noise Shaping Characteristics

6. Data Output Circuit

The output circuit is equipped with a 3'rd analog low-pass filter. This enables direct analog signals to be acquired from the IC's RO (pin 5) and LO (pin 9) output pins.

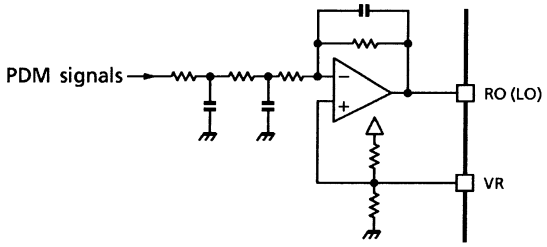


Figure 8 Analog Filter Circuit

7. Soft Mute Circuit

The IC is equipped with a soft mute function, and this enables a soft mute to be set for the DA converter output by switching the SM pin (pin 18) from the "L" level to the "H" level when in the parallel mode (P/$\overline{S}$ = "H"). The soft mute's ON/OFF function and the DA converter output are shown in Figure 9.
The Soft mute ON/OFF control function is disabled during level transition.

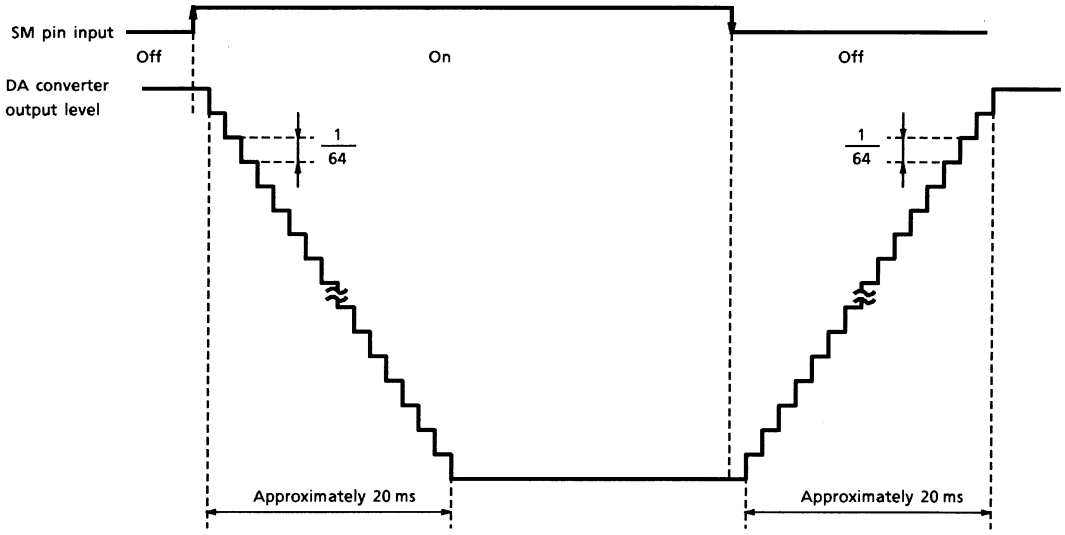


Figure 9 Changes in The Soft Mute DA Converter Output Level

8. Common left Channel/Right Channel Digital Zero Data Detection Output Circuit

The IC is equipped with a common left channel/right channel digital zero data detection output circuit, and the ZD pin (pin 11) is switched from "L" to "H" when data for both the left channel and the right channel becomes zero data for approximately 350 ms or longer.

This is fixed at "L" when the data for the left channel and right channel is not zero data.

9. Description of Internal Control Signals

The P/$\overline{S}$ pin can be used to switch between the parallel mode (P/$\overline{S}$ pin = "H" in DC setting mode) and the serial mode (P/$\overline{S}$ pin = "L" with the microcontroller interface function).

9-1 Parallel Mode (P/$\overline{S}$ = "H": DC setting mode)

Pins 18, 19 and 20 are used as the mode setting pins shown in the table below when in the parallel mode.

Table 3 Pin Names at the Parallel Mode

Pin No.	Pin Name	Function
18	BS	De-emphasis filter mode select pin
19	EMP	De-emphasis filter control pin
20	SM	Soft mute control pin

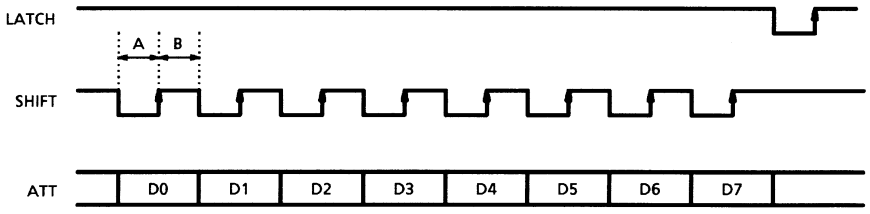
9-2 Serial Mode ($P/\overline{S}$ = "L": microcontroller setting mode)

It is possible to make the various settings with a microcontroller when in the serial mode. Pins 18, 19 and 20 are used as the command input pins shown in the table below when in the serial mode.

Table 4 Pin Names at The Serial Mode

Pin No.	Pin Name	Function
18	LATCH	Data latch signal input pin
19	SHIFT	Shift clock signal input pin
20	ATT	Data input pin

The LATCH signals and ATT signals are loaded to the LSI internal shift registers on the SHIFT signal rising edge. It is consequently necessary for the data input from the ATT pin on the shift signal rising edge to be valid as indicated in the timing example in Figure 10. It is also necessary for the LATCH pulse to rise at least 1.5 μs after the final clock rising edge input from the SHIFT pin. Operating the shift clock with LATCH low destabilizes the internal state, which may lead to malfunctions, so it must therefore be set to the low level after loading D7 to the register.



A = 1.5 μs or higher, B = 1.5 μs or higher

Figure 10 Example of Data Setting Timing in the Serial Mode

The various control settings when in the serial mode are shown in the table below. Ensure that all control bits are set when the power supply is turned on.

Table 5 Serial Mode Control Settings

Serial Input Data	Control Signal	
D7	0	1
D6	AT6	μBS
D5	AT5	μEMP
D4	AT4	—
D3	AT3	—
D2	AT2	—
D1	AT1	—
D0	AT0	—

AT0~6: Attenuation level setting

μBS: De-emphasis mode select

μEMP: De-emphasis ON/OFF switch

(1) Digital attenuator

The digital attenuation command is enabled when D7 = "L". The attenuation data can be set in 128 different ways. The relationship with the command's output is shown below.

Table 6 Attenuation Data/Audio Data Output

Attenuation Data D6~D0	Audio Output
7F (HEX)	−0.000dB
7E (HEX)	−0.069dB
:	:
01 (HEX)	−42.076dB
00 (HEX)	−∞

01 (HEX) to 7E (HEX): The attenuation value is obtained with the following equation.

ATT = 20 ℓog (input data/127) dB

Example: In case of attenuator = 7 A

ATT = 20 ℓog (122/127) dB = −0.349dB

(2) Digital de-emphasis filter

The Digital De-emphasis setting mode is enabled when D7 = "H".

Controlled with μEMP and μBS signal.

Table 7 Digital De-Emphasis Filter Setting

μBS	H	H	L	L	
μEMP	H	L	H	L	
Mode	32	48	44.1	OFF	(kHz)

Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{DD}	−0.3~6.0	V
	V_{DA}	−0.3~6.0	
	V_{DX}	−0.3~6.0	
Input voltage	V_{in}	−0.3~V_{DD} + 0.3	V
Power dissipation	P_D	200	mW
Operating temperature	T_{opr}	−35~85	°C
Storage temperature	T_{stg}	−55~150	°C

Electrical Characteristics (unless otherwise specified, Ta = 25°C, V_{DD} = V_{DX} = V_{DA} = 5 V)

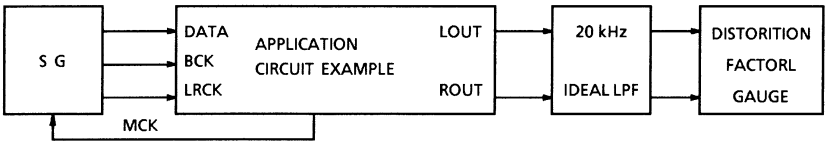
DC Characteristics

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Operating supply voltage (1)		V_{DD}	—	Ta = −35~85°C	4.5	5.0	5.5	V
		V_{DX}			4.5	5.0	5.5	
		V_{DA}			4.5	5.0	5.5	
Operating supply voltage (2)		V_{DD}	—	Ta = −15~55°C Operation frequency 12 MHz ≦ f_{opr} ≦ 18.5 MHz	2.7	3.0	5.5	V
		V_{DX}			2.7	3.0	5.5	
		V_{DA}			2.7	3.0	5.5	
Power dissipation		I_{DD}	—	XI = 16.9 MHz	—	12	20	mA
Input voltage	"H" level	V_{IH}	—	—	V_{DD} × 0.7	—	V_{DD}	V
	"L" level	V_{IL}			0	—	V_{DD} × 0.3	
Input current	"H" level	I_{IH}	—	—	−10	—	10	μA
	"L" level	I_{IL}						

AC Characteristics (over-sampling ratio = 192 fs)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Table harmonic distortion + noise 1	THD + N1	1	1 kHz sine wave, full-scale input $V_{DD} = V_{DX} = V_{DA} = 5.0$ V	—	−85	−80	dB
Table harmonic distortion + noise 2	THD + N2	1	1 kHz sine wave, full-scale input $V_{DD} = V_{DX} = V_{DA} = 3.0$ V	—	−85	−78	dB
S/N ratio	S/N	1	—	88	96	—	dB
Dynamic range	DR	1	1 kHz sine wave, −60dB input conversion	90	95	—	dB
Cross-talk	CT	1	1 kHz sine wave, full-scale input	—	−95	−90	dB
Analog output level 1	Aout 1	1	1 kHz sine wave, full-scale input $V_{DD} = V_{DX} = V_{DA} = 5.0$ V	—	1250	—	mV_{rms}
Analog output level 2	Aout 2	1	1 kHz sine wave, full-scale input $V_{DD} = V_{DX} = V_{DA} = 3.0$ V	—	750	—	mV_{rms}
Operating frequency	f_{opr}	—	$V_{DD} = V_{DA} = V_{DX} \geqq 4.5$ V	10	16.9344	18.5	MHz
Input frequency	f_{LR}	—	LRCK duty cycle = 50%	30	44.1	100	kHz
	f_{BCK}		BCK duty cycle = 50%	0.96	2.1168	4.3	MHz
Rise time	t_r	—	LRCK, BCK (10%~90%)	—	—	15	ns
Fall time	t_f			—	—	15	ns
Delay time	t_d	—	BCK ↓ Edge → LRCK, DATA	—	—	40	ns

Test Circuit-1: With the Use of a Sample Application Circuit



SG: ANRITSU MG-22A or equivalent

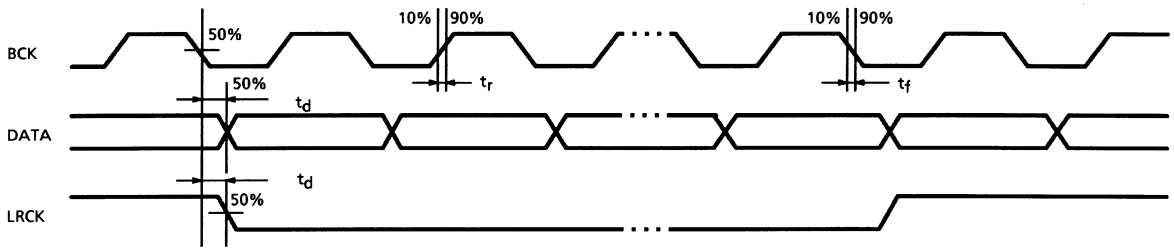
LPF: SHIBASOKU 725C built-in Filter

Distortion factor gauge: SHIBASOKU 725C or equivalent

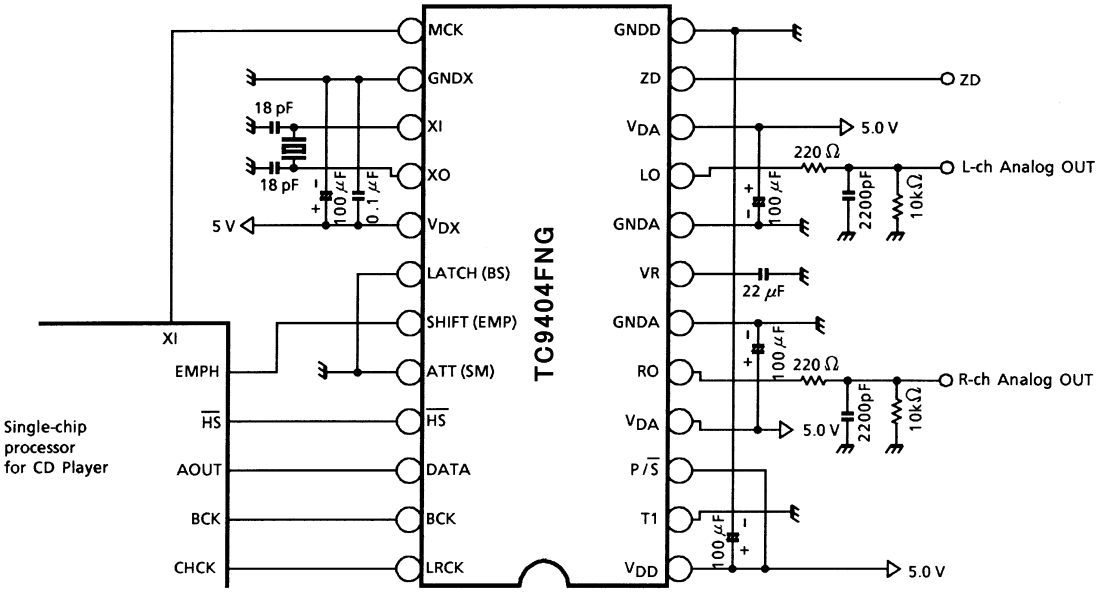
Measuring Item	Distortion Factor Gauge Filter Setting A Weight
THD + N, CT	OFF
S/N, DR	ON

A weight: IEC-A or equivalent

AC Characteristics Stipulated Point (input signal stipulation: LRCK, BCK, DATA)



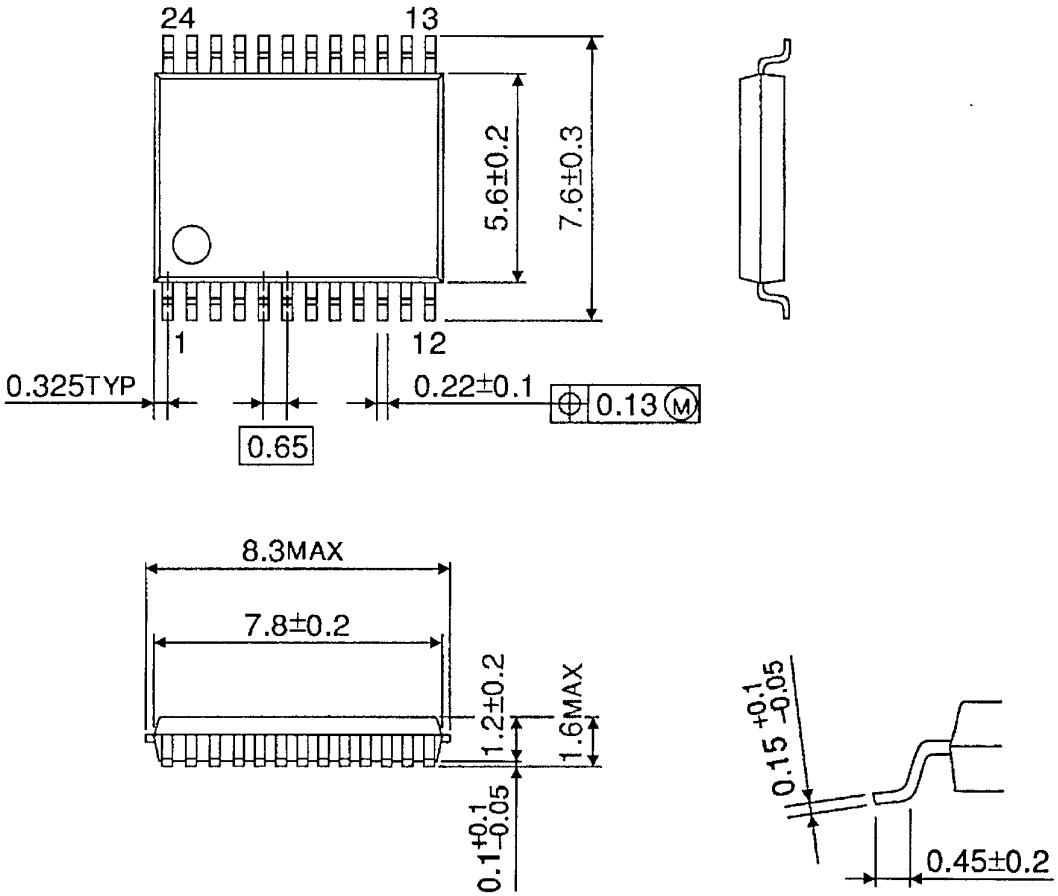
Application Circuit



Package Dimensions

P-SSOP24-300-0.65A

Unit : mm



(Note) Sn-Ag plate

Weight: 0.14 g (typ.)

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About solderability, following conditions were confirmed

- Solderability

  (1) Use of Sn-37Pb solder Bath
  - solder bath temperature = 230°C
  - dipping time = 5 seconds
  - the number of times = once
  - use of R-type flux

  (2) Use of Sn-3.0Ag-0.5Cu solder Bath
  - solder bath temperature = 245°C
  - dipping time = 5 seconds
  - the number of times = once
  - use of R-type flux