

Devices

## High-Performance, Step-Up DC-DC Converter for High-Power Applications in Mobile Devices

## **General Description**

LM8850 is a step-up DC-DC converter optimized for use with a supercapacitor to protect a battery from power surges and enable new high power applications in mobile device architectures. The device creates an ideal rail from 3.6V to 5.7V boosting from a single Li-Ion cell with an input voltage range of 2.3V to 5.5V; Target V<sub>OUT</sub> must be at least 10% higher than V<sub>IN</sub>.

An I<sup>2</sup>C interface controlling multiple output voltage settings, input current limits, and load currents up to 1A provides superior user flexibility. The LM8850 operates in Auto mode, where the converter is in PFM mode at light loads and switches to PWM mode at heavy loads. Hysteretic PFM extends the battery life by reduction of the quiescent current to 6µA (typ.) during light load and standby conditions. Synchronous operation provides true shutdown isolation and improves its efficiency at medium-to-full load conditions.

High-switching frequency enables smaller passive components. Internal compensation is used for a broader range of inductor and output capacitor values to meet system demand and achieve small system solution size.

LM8850 is available in a 9-bump ultra-thin micro SMD package. Only four external surface-mount components, a 1.0  $\mu$ H inductor, a 4.7  $\mu$ F for input capacitor, 4.7  $\mu$ F for output capacitor and 0.05F-1.0F supercapacitor for energy storage are required.

### **Features**

- 6µA typ. quiescent current
- $V_{OUT} = 3.6V$  to 5.7V (max  $V_0 = 5.7V$ )
- Operates from a single lithium ion cell (2.3V to 5.5V)
- 8 user-selectable output voltages via I<sup>2</sup>C
- High-speed 3.4 MHz I<sup>2</sup>C-compatible interface
- Up to 1.0A maximum load current capability
- 4 levels of current limiting
- Auto-mode operation and Forced PWM
- 2.5 MHz switching frequency (typ.)
- ±2.5% DC output voltage precision
- 1.0 µH inductor (2520 case size)
- 4.7 µF input and output capacitors (0603 case size)
- PGOOD signal
- True shutdown isolation
- Output over-voltage protection
- Internal active voltage balancing for supercapacitors
- micro SMD 9-bump package (1.58 mm x 1.62 mm x 0.35 mm)(0.5 mm pitch)

## Applications

- Flash LED
- Mobile Phones
- WiMAX
- USB
- Audio Amplifier



M8850 High-Performance, Step-Up DC-DC Converter for High-Power Applications in Mobile

**Typical Application Circuit** 



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## **Connection Diagram and Package Mark Information**



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FIGURE 1. 9-Bump ultra-thin micro SMD Package

Note: The package marking "X" denotes the date code, "V" is a National Semiconductor internal code of die traceability.

## **Pin Descriptions**

Pin #	Name	Description
A1	VIN	Power Supply Input. Connect to input filter capacitor (See Typical Application Circuit)
A2	SW	Switching node. Connection to the internal NFET switch and PFET synchronous rectifier
A3	GND	Ground Pin
B1	SDA	I <sup>2</sup> C data (Use a $2k\Omega$ pull-up resistor)
B2	PG	Power Good indicator
B3	VOUT	Output pin.
C1	SCLK	I <sup>2</sup> C Clock (Use a $2k\Omega$ pull-up resistor)
C2	EN	Enable pin. The device is in shutdown when voltage to this pin is <0.4V and enabled when >1.2V. Do not leave this pin floating.
C3	BAL	Balancing pin for active voltage balancing of supercapacitor

#### Ordering Information (9-Bump micro SMD)

Order Number 9-bump Micro SMD	Package Marking	Supplied As
LM8850 URE	SK	250 units, Tape-and-Reel
LM8850 URX	SK	3000 units, Tape-and-Reel

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

VIN Pin to GND	–0.2V to 6.5V
EN, PG, SDA, SCLK pins to GND	-0.2V to 6.0V
VOUT to GND	(GND-0.2V) to
SW pin to GND	-0.2V to 6.5V
BAL to GND	-0.2V to 6.0V
Junction Temperature (T <sub>J-MAX</sub> )	+150°C
Storage Temperature Range	-65°C to +150°C
Continuous Power Dissipation ( <i>Note 3</i> )	Internally Limited
Maximum Lead Temperature (Soldering, 10 sec.)	260°C
ESD Rating (Note 4)	
Human Body Model	2kV
Machine Model	200V
Charged Device Model	1250V

## **Operating Ratings** (Note 1, Note 2)

Input Voltage Range	2.3V to 5.5V
Recommended Load	0mA to 1.0A
Current	
Junction Temperature (T <sub>J</sub> )	–40°C to +125°C
Range	
Ambient Temperature (T <sub>△</sub> )	-40°C to +85°C
Range ( <i>Note 5</i> )	

## **Thermal Properties**

Junction-to-Ambient Thermal Resistance ( $\theta_{JA}$ ) (micro SMD) (*Note 6*) 70°C/W

LM8850

**Electrical Characteristics** (*Note 2, Note 7, Note 8, Note 9*) Limits in standard typeface are for  $T_A = 25^{\circ}$ C. Limits in **boldface** type apply over the operating junction temperature range ( $-40^{\circ}$ C  $\leq T_J = T_A \leq +85^{\circ}$ C). Unless otherwise noted, specifications apply to the LM8850 open loop Typical Application Circuit with  $V_{IN} = EN = 3.6V$ .

Symbol	Parameter	Condition	Min	Тур	Max	Units	
V <sub>OUT</sub>	Output Voltage	I <sub>OUT</sub> = 0mA, V <sub>OUT</sub> = 5V	-2.5		+2.5	%	
		VSEL bits = 0 0 0		3.6		-	
	Output Voltage Range	VSEL bits = 0 0 1		3.9			
	Register 0	VSEL bits = 0 1 0		4.2			
V		VSEL bits = 0 1 1		4.5			
<b>V</b> OUT		VSEL bits = 1 0 0		4.7		v	
	Output Voltage Range	VSEL bits = 1 0 1		5.0			
	Register 1	VSEL bits = 1 1 0		5.3			
		VSEL bits = 1 1 1		5.7			
I <sub>SHDN</sub>	Shutdown Supply Current			0.4	3		
I <sub>Q_PFM</sub>	Quiescent Current in PFM Mode			6	10	μA	
I <sub>Q_PWM</sub>	Quiescent Current in PWM Mode			330	500		
R <sub>DSON (NFET)</sub>	Pin-Pin Resistance for Sync NFET	$V_{IN} = V_{GS} = 3.6V$		200			
R <sub>DSON (PFET)</sub>	Pin-Pin Resistance for PFET	$V_{IN} = V_{GS} = 5.0V$		215		- mΩ	
		ISEL bits = 111 VIN = 4.5V	1350	1500	1650	- mA	
		ISEL bits = 101 VIN = 4.5V	923	1025	1128		
LIM	Switch Peak Current Limit	ISEL bits = 011 VIN = 4.5V	666	740	814		
		ISEL bits = 001 VIN = 4.5V	477	530	583		

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Symbol	Parameter	Condition	Min	Тур	Max	Units
		$T_{ON} = 00$		5		secs.
т	Turn on Time	T <sub>ON</sub> = 01		7.5		
ON	Turn on Time	T <sub>ON</sub> = 10		10		
		T <sub>ON</sub> = 11		12.5		
I <sub>EN</sub>	Pin Input current	EN		0.01	1	μA
F <sub>OSC</sub>	Internal Oscillator Frequency		2.25	2.5	2.75	MHz
V <sub>IH</sub>	Logic High Input		1.2			
V <sub>IL</sub>	Logic Low Input				0.4	v
V <sub>OH</sub>	Logic Output High		1.2			
V <sub>OL</sub>	Logic Output Low				0.4	]

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: All voltages are with respect to the potential at the GND pin.

Note 3: Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at  $T_J = 150^{\circ}C$  (typ.) and disengages at  $T_J = 140^{\circ}C$  (typ.).

Note 4: The Human Body Model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin. MIL-STD-883–3015.7.

**Note 5:** In applications where high power dissipation and/or poor package resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ( $T_{A-MAX}$ ) is dependent on the maximum operating junction temperature ( $T_{J-MAX-OP} = 125^{\circ}C$ ), the maximum power dissipation of the device in the application ( $P_{D-MAX}$ ) and the junction-to-ambient thermal resistance of the part/package ( $\theta_{JA}$ ) in the application, as given by the following equation:  $T_{A-MAX} = T_{J-MAX} - (\theta_{JA}X P_{D-MAX})$ .

Note 6: Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high power dissipation exists, special care must be given to thermal dissipation issues in board design.

Note 7: Min and Max limits are guaranteed by design, test or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm.

Note 8: The parameters in the electrical characteristic table are tested under open loop conditions at  $V_{IN}$  = 3.6V unless otherwise specified. For performance over the input voltage range and closed loop condition, refer to the datasheet curves.

Note 9: Open-loop Electrical Characteristics taken without supercapacitor.

## **Dissipation Rating Table**

$\theta_{JA}$	T <sub>A</sub> ≤ 25°C	T <sub>A</sub> ≤ 60°C	T <sub>A</sub> ≤ 85°C
	Power Rating	Power Rating	Power Rating
70°C/W	1500 mW	980 mW	600 mW

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## **Typical Performance Characteristics** Unless otherwise noted: $V_{OUT} = 5.0V$ , $T_A = 25^{\circ}C$ , Supercapacitor = TDK EDLC272020–501–2F-50).





30113245

30113243



Efficiency Room temp, 100 mV PFM ripple





30113242

Efficiency, V<sub>OUT</sub> = 5V, PWM Mode, 25°C



Efficiency over PFM ripple,  $V_{IN}$  = 3.9V, Room Temp



30113233

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Line Regulation, V<sub>OUT</sub> 5V, 250 mA Load, 100 mV Ripple, Auto Mode













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LM8850



## **Operation Description**

#### LM8850 FUNCTIONALITY

The LM8850, a high-efficiency, step-up DC-DC switching boost converter, delivers a constant voltage from a stable DC input voltage source. Using a voltage mode architecture with synchronous rectification, the LM8850 has the ability to deliver up to 600 mA of load current, depending on the input voltage, output voltage, ambient temperature, and the inductor chosen.

There are three modes of operation depending on the current required - PWM (Pulse Width Modulation), PFM (Pulse Frequency Modulation), and shutdown. The device operates in PWM mode at load currents of approximately 200 mA or higher. Lighter output current loads cause the device to automatically switch into PFM for reduced current consumption ( $I_q = 6\mu$ A typ). Shutdown mode turns off the voltage regulation and offers the lowest current consumption ( $I_{SHUTDOWN} = 0.4 \mu$ A typ).

Once enabled, the LM8850 charges the supercapacitor utilizing all of the default settings in the registers. The I<sup>2</sup>C must be used to change the default settings and this can only be done with the LM8850 enabled. Once a register is written to, the changes will transition immediately. Every time the EN pin transitions from VIL to VIH, registers 0 and 1 are reset to their defaults settings and any settings need to be rewritten into the appropriate registers.

#### **AUTO MODE**

The LM8850 utilizes AUTO mode to reduce the amount of energy required to maintain the regulated output voltage under light load conditions. The transition from Auto mode to PWM mode varies depending on input voltage and output voltage. For an output voltage of 5.0V and an input voltage of 3.6V, the transition will occur around 225 mA.

Auto mode can only be used with a supercapacitor. If no supercapacitor is being used in the circuit, Auto-Mode must be disabled via I<sup>2</sup>C.

#### VRIPPLE

The ripple voltage used in Auto-Mode is programmable via I<sup>2</sup>C. The ripple voltage can be set to 50, 100, 200 and 250 mV. The larger the ripple voltage, the more constant energy will be supplied by the supercapacitor. The regulator will remain asleep until the effective energy to reduce the supercapacitor's voltage by the ripple value has been used by the load.

#### POWER GOOD

The Power Good signal is both an output and a read only register bit. The Power Good signal will have a  $V_{OH}$  value if the  $V_{OUT}$  is greater than 85% of its programmed value. This

is a typical value for 5.0V and 3.6V  $\rm V_{\rm IN}.$  The typical value will vary based on input and output voltage.

#### PROGRAMMABLE V<sub>OUT</sub>

The output voltage of the LM8850 can be programmed via I<sup>2</sup>C to any of 8 different values: 3.6, 3.9, 4.2, 4.5, 4.7, 5.0, 5.3, and 5.7V. The only requirement is that the input voltage must remain 10% below the desired output voltage for it to remain in regulation. The output voltage can be changed while the part is enabled and regulating. The transition time will depend on load conditions.

#### **TURN-ON TIME**

The LM8850 has four programmable turn time values, 5, 7.5, 10, and 12.5 seconds. During the turn on time, the LM8850 is ramping to the output voltage while limiting the inrush current which charges the supercapacitor.

#### **BALANCING CIRCUIT**

The LM8850 has an internal balancing circuit that helps maintain voltage balance between the two capacitors within the super capacitor. The BAL pin regulates a voltage of VOUT/2 between the two capacitors. If one capacitor is overcharged or less charged, the LM8850 will use the balancing circuit to correct this charge inbalance. The balancing circuit can be turned off/on via the I<sup>2</sup>C registers (BALMODE – Control Reg01, bit 3). The balancing circuit also has the ability to stay ON even after the LM8850 is shutting down (BAL – Control Reg00, bit 4).

### I<sup>2</sup>C Interface

Control of LM8850 is done via I<sup>2</sup>C compatible interface. This includes switch over from AUTO to PWM mode, adjustment of current limit, output voltage, PFM Hysteresis voltage, and start-up time. The I<sup>2</sup>C interface can also switch the active voltage balance circuit ON during shutdown. Additionally, there is a flag bit that reads back PGOOD condition.

#### **I<sup>2</sup>C SIGNALS**

In I<sup>2</sup>C-compatible mode, the SCL pin is used for the I<sup>2</sup>C clock and the SDA pin is used for the I<sup>2</sup>C data. Both these signals need a pull-up resistor according to I<sup>2</sup>C specification. The values of the pull-up resistors are determined by the capacitance of the bus. See I<sup>2</sup>C specification from Philips for further details. Signal timing specifications are according to the I<sup>2</sup>C bus specification. Maximum frequency is 400 kHz or 3.4 MHz if in High-Speed Mode.

#### **I<sup>2</sup>C DATA VALIDITY**

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when CLK is LOW.



#### I<sup>2</sup>C START AND STOP CONDITIONS

START and STOP bits classify the beginning and the end of the I<sup>2</sup>C session. START condition is defined as SDA signal transitioning from HIGH to LOW while SCL line is HIGH. STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I<sup>2</sup>C master always generates START and STOP bits. The I<sup>2</sup>C bus is considered to be busy after START condition and free after STOP condition. During data transmission, I<sup>2</sup>C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise. \_M8850



#### **START and STOP Conditions**

#### **TRANSFERRING DATA**

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. All clock pulses are generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the ninth clock pulse, signifying an acknowledge. A receiver which has been addressed must generate an acknowledge after each byte has been received. After the START condition, the I<sup>2</sup>C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The LM8850 address is 0x60. the eighth bit, a "0" indicates a WRITE and a "1" indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.





#### When a READ function is to be accomplished, a WRITE function must precede the READ function as shown in the Read Cycle waveform.



- 5. Send read or writes in HS mode. (Remember to use "repeated starts" between commands.); then
- 6. When you are done with the last command send a "stop" condition to put the part back into regular 400 kHz mode.

#### **Register Information and Details**

Register name	Location	Туре	Register
CONTROL	0	R/W	Control Register 1
CONTROL	1	R/W	Control Register 2







Physical Dimensions inches (millimeters) unless otherwise noted



Devices

Pro	oducts	Design Support		
Amplifiers	www.national.com/amplifiers	WEBENCH® Tools	www.national.com/webench	
Audio	www.national.com/audio	App Notes	www.national.com/appnotes	
Clock and Timing	www.national.com/timing	Reference Designs	www.national.com/refdesigns	
Data Converters	www.national.com/adc	Samples	www.national.com/samples	
Interface	www.national.com/interface	Eval Boards	www.national.com/evalboards	
LVDS	www.national.com/lvds	Packaging	www.national.com/packaging	
Power Management	www.national.com/power	Green Compliance	www.national.com/quality/green	
Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts	
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality	
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback	
Voltage References	www.national.com/vref	Design Made Easy	www.national.com/easy	
PowerWise® Solutions	www.national.com/powerwise	Applications & Markets	www.national.com/solutions	
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero	
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