W83795G/ADG
Nuvoton H/W Monitor

Date: Aug/2/2010 Revision: 1.41

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1. GENERAL DESCRIPTION (W83795G)

W83795G is an evolving version of the Nuvoton popular Hardware Monitor IC family. W83795G provides several innovative features, such as ASF 2.0 compliant specification, SMBus 2.0 ARP compatible command, Intel PECI2.0 interface, AMD SB-TSI interface, PROCESSOR HOT, parallel VID input, and serial VID input. Conventionally, W83795G can be used to monitor several critical hardware parameters of the system, including power supply voltages, fan speeds, and temperatures, which are very important for a high-end computer system, such as server, workstation…etc, to work stably and efficiently.

A 10-bit analog-to-digital converter (ADC) is built inside W83795G. W83795G can simultaneously monitor 15 (up to 21) analog voltage inputs (including power VDD / 3VSB / VBAT / VTT monitoring), 8 (up to 14) fan tachometer inputs, 8 fan output control, 6 remote temperature sensor inputs, 4 of which support current mode (dual current source) temperature measurement method, caseopen detection, Watch Dog Timer function, and GPIO pins. The sense of remote temperature can be performed by thermistors, or directly from Intel® / AMD™ CPU with thermal diode output. W83795G provides 8 PWM (pulse width modulation) / DC fan output modes for SMART FAN™ control - " Thermal Cruise™ " mode and " SMART FAN™ IV " mode. Under " Thermal Cruise™ " mode, temperatures of CPU and the system can be maintained within specific programmable ranges under the hardware control. As for SMART FAN™ IV, which provides 8 sets of temperatures setting point each could control fan's duty cycle, depends on this construction, fan could be operated at the lowest possible speed so that the acoustic noise could be balanced. As for warning mechanism, W83795G provides SMI#, OVT#, VOLT_FAULT#, FAN_FAULT#, and BEEP signals to protect the system. W83795G has 2 specific pins to provide address selection so that 4 W83795G could be wired through I^2C interface at the same time.

W83795G can uniquely serve as an ASF sensor to respond to ASF master's request for the implementation of network management in OS-absent status. Through W83795G's compliance with ASF2.0 sensor specification, network server is able to monitor the environmental status of each client in OS-absent state by PET (Platform Event Trap) frame values returned from W83795G, such as temperatures, voltages, fan speed and case open. Moreover, W83795G supports SMBus 2.0 ARP command to solve the problem of address conflicts by dynamically assigning a new unique address for W83795G ASF Function after W83795G's UDID is sent.

Through the application software or BIOS, the users can read all the monitored parameters of the system from time to time. A pop-up warning can also be activated when the monitored item is out of the proper/preset range. The application software could be Nuvoton's Hardware Doctor™ or other management application software. Besides, the users can set up the upper and lower limits (alarm thresholds) of these monitored parameters and activate corresponding maskable interrupts.

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2. GENERAL DESCRIPTION (W83795ADG)

W83795ADG is an evolving version of the Nuvoton popular Hardware Monitor IC family. W83795ADG provides several innovative features, such as ASF 2.0 compliant specification, SMBus 2.0 ARP compatible command, Intel PECI2.0 interface, and PROCESSOR HOT. Conventionally, W83795ADG can be used to monitor several critical hardware parameters of the system, including power supply voltages, fan speeds, and temperatures, which are very important for a high-end computer system, such as server, workstation…etc, to work stably and efficiently.

A 10-bit analog-to-digital converter (ADC) is built inside W83795ADG. W83795ADG can simultaneously monitor 12 (up to 18) analog voltage inputs (including power VDD / 3VSB / VBAT / VTT monitoring), 8 (up to 14) fan tachometer inputs, 2 fan output control, 6 remote temperature sensor inputs, 4 of which support current mode (dual current source) temperature measurement method, caseopen detection, Watch Dog Timer function, and GPIO pins. The sense of remote temperature can be performed by thermistors, or directly from Intel® CPU with thermal diode output. W83795ADG provides 2 PWM (pulse width modulation) / DC fan output modes for SMART FAN™ control - **“** Thermal Cruise™ **”** mode and **“** SMART FAN™ IV **”** mode. Under **“** Thermal Cruise™ **”** mode, temperatures of CPU and the system can be maintained within specific programmable ranges under the hardware control. As for SMART FAN™ IV, which provides 8 sets of temperatures setting point each could control fan’s duty cycle, depends on this construction, fan could be operated at the lowest possible speed so that the acoustic noise could be balanced. As for warning mechanism, W83795ADG provides SMI#, OVT#, and BEEP signals to protect the system. W83795ADG has 2 specific pins to provide address selection so that 4 W83795ADG could be wired through I^2C interface at the same time.

W83795ADG can uniquely serve as an ASF sensor to respond to ASF master’s request for the implementation of network management in OS-absent status. Through W83795ADG’s compliance with ASF2.0 sensor specification, network server is able to monitor the environmental status of each client in OS-absent state by PET (Platform Event Trap) frame values returned from W83795ADG, such as temperatures, voltages, fan speed and case open. Moreover, W83795ADG supports SMBus 2.0 ARP command to solve the problem of address conflicts by dynamically assigning a new unique address for W83795ADG ASF Function after W83795ADG’s UDID is sent.

Through the application software or BIOS, the users can read all the monitored parameters of the system from time to time. A pop-up warning can also be activated when the monitored item is out of the proper/preset range. The application software could be Nuvoton's Hardware Doctor™ or other management application software. Besides, the users can set up the upper and lower limits (alarm thresholds) of these monitored parameters and activate corresponding maskable interrupts.

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3. FEATURES (W83795G)

■ Monitoring Items

VOLTAGE

Up to 21 voltage sensing inputs.

- 11 general voltage inputs.
- 4 power pins.
- 2 multi-function with thermistor temperature inputs.
- 4 multi-function with thermal diode pair.

VID

- Provide parallel VID input and serial VID (AMD™) input monitoring.

TEMPERATURE

Up to 6 temperature monitoring.

- 4 pairs thermal diode (current mode) temperature.
- 2 thermistor mode temperature.
- Support Intel® PECI interfaces for reading CPU temperature. (Including PECI_REQ# mechanism)
- Support AMD™ SB-TSI for reading CPU temperature

PECI (PLATFORM ENVIRONMENT CONTROL INTERFACE)

- Support PECI 2.0 Specification
- Support 8 CPU Address and 2 domains per CPU address

AMD™ SB-TSI INTERFACE

- Support AMD™ SB-TSI Specification

FAN

Up to 8 Fan Control output and Up to 14 fan tachometer input.

- 6 pure fan control output pins (PWM / DC mode supported).
- 2 fan control output multi-function (FANCTL7 and FANCTL8).
- 8 pure fan tachometer input (FANIN1-FANIN8).
- 5 fan tachometer input multi-function (FANIN9-FANIN14)

SMART FAN™ CONTROL

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- Support the SMART FAN™ control – "Thermal Cruise™" mode and "SMART FAN™ IV" mode.
- Multi-temperature source vs. Multi-fan-control output.
- 6 mapping table for temperature vs. fan control output (based on temperature's behavior).
- 8 tables for Speed Cruise Mode for fan control output.
- Item 2 and item 3 could both control fan control output behavior.

CASEOPEN

- Case open detection input. (low active).

■ Address Resolution Protocol and Alert Standard Format

- Support System Management Bus (SMBus) version 2.0 specification.
- Comply with hardware sensor slave ARP (Address Resolution Protocol).
- Response ASF 2.0 command -- Get Event Data, Get Event Status, Device Type Poll.
- Comply with ASF 2.0 sensors (Monitoring fan speed, voltage, temperature, thermal trip and case open event/status).
- Support Remote Control subset: Remote Power-on/ Power-off/ Reset.

■ Alarm Output

- Issue SMI#, OVT#, VOLT_FAULT#, FAN_FAULT# signals to activate system protection.
- Issue BEEP signal to activate system speaker or buzzer.

■ General

- Provide up to 8 GPIO pins (multi-function with parallel VID).
- I^2C / SMBus2.0 serial bus interface (max. 400KHz Clock).
- Watch Dog Timer function: WDTRST#, SYSRST_IN.
- 2 address selection pins provide selectable address settings for application of 4 W83795G wired together through I^2C interface.
- 3.3V operation.

■ Package

- 64-LQFP Package type
- Pb-free / RoHS-Compliant

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4. FEATURES (W83795ADG)

■ Monitoring Items

VOLTAGE

Up to 18 voltage sensing inputs.

- 8 general voltage inputs.
- 4 power pins.
- 2 multi-function with thermistor temperature inputs.
- 4 multi-function with thermal diode pair.

TEMPERATURE

Up to 6 temperature monitoring.

- 4 pairs thermal diode (current mode) temperature
- 2 thermistor mode temperature.
- Support Intel® PECI interfaces for reading CPU temperature. (Including PECI_REQ# mechanism).

PECI (PLATFORM ENVIRONMENT CONTROL INTERFACE)

- Support PECI 2.0 Specification
- Support 8 CPU Address and 2 domains per CPU address

FAN

Up to 2 Fan Control output and Up to 14 fan tachometer input.

- 2 pure fan control output pins (PWM / DC mode supported).
- 8 pure fan tachometer input (FANIN1-FANIN8).
- 5 fan tachometer input multi-function (FANIN9-FANIN14).

SMART FAN™ CONTROL

- Support the SMART FAN™ control – "Thermal Cruise™" mode and "SMART FAN™ IV" mode.
- Multi-temperature source vs. Multi-fan-control output.
- 6 mapping table for temperature vs. fan control output (based on temperature's behavior).
- 8 tables for Speed Cruise Mode for fan control output.
- Item 2 and item 3 could both control fan control output behavior.

CASEOPEN

- Case open detection input. (low active).

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Address Resolution Protocol and Alert Standard Format

- Support System Management Bus (SMBus) version 2.0 specification.
- Comply with hardware sensor slave ARP (Address Resolution Protocol).
- Response ASF 2.0 command -- Get Event Data, Get Event Status, Device Type Poll.
- Comply with ASF 2.0 sensors (Monitoring fan speed, voltage, temperature, thermal trip and case open event/status).
- Support Remote Control subset: Remote Power-on/ Power-off/ Reset.

Alarm Output

- Issue SMI# and OVT# signals to activate system protection.
- Issue BEEP signal to activate system speaker or buzzer (multi-function with OVT#)

General

- Provide up to 4 GPIO pins (multi-function with FANIN).
- I^2C / SMBus2.0 serial bus interface (max. 400KHz Clock).
- Watch Dog Timer function: WDTRST#, SYSRST_IN.
- 2 address selection pins provide selectable address settings for application of 4 W83795ADG wired together through I^2C interface.
- 3.3V operation.

Package

- 48-LQFP Package type
- Pb-free / RoHS-Compliant

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5. KEY SPECIFICATIONS

- Voltage monitoring accuracy ±10mV
- Temperature Sensor Accuracy
  - Remote Diode Sensor Accuracy (25~90°C) ± 1°C typ.
  - Resolution 0.25 ℃
- Supply Voltage 3VDD and 3VSB 3.3V ± 10%
- Operating Supply Current 15 mA typ.

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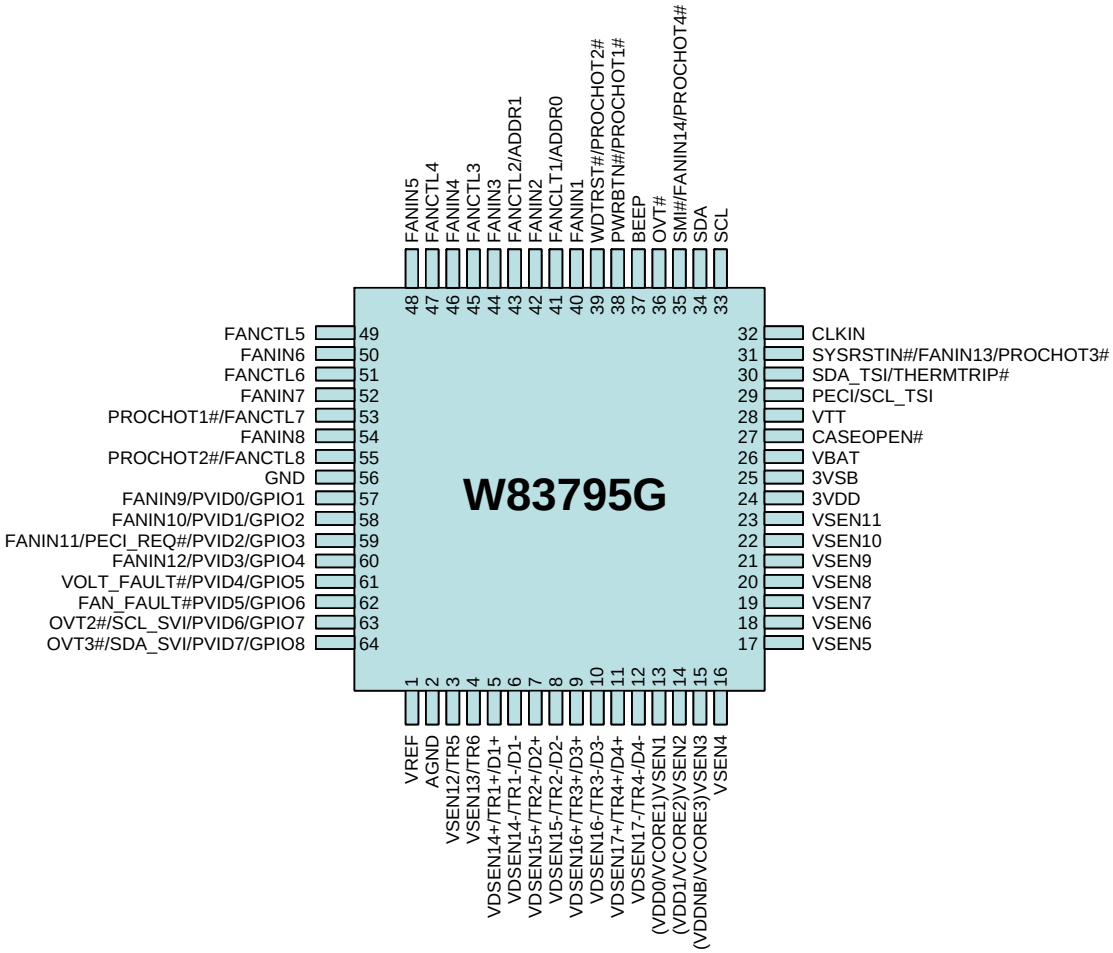
6. PIN CONFIGURATION

W83795G



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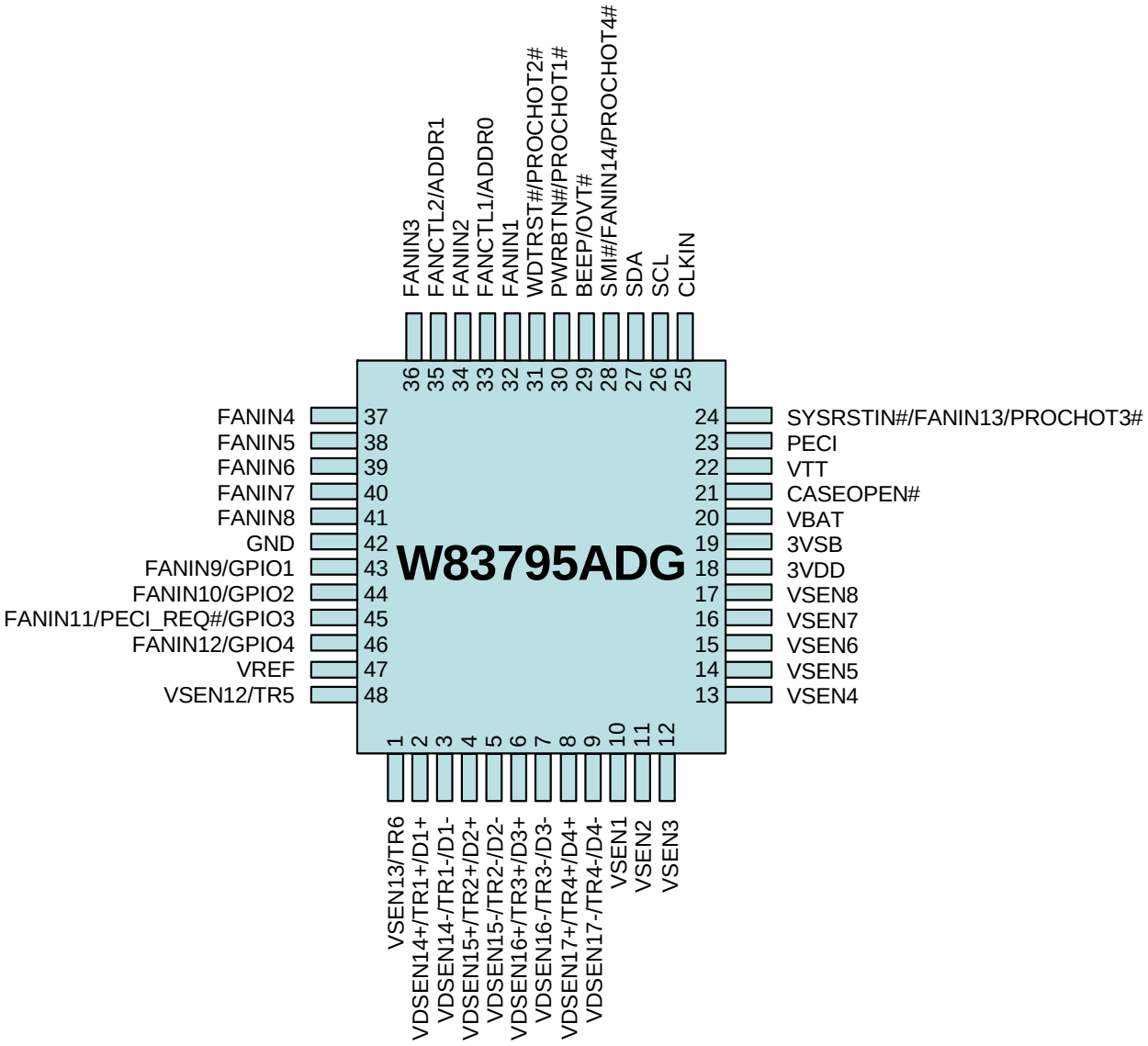
W83795ADG



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7. PIN DESCRIPTION

7.1 Pin Type Description

SYMBOL	DESCRIPTION
t	TTL level
V1	Type of INTELPVID
V2	Type of AMDPVID
V3	Type of AMDSVID
V4	Type of PECI
V5	Type of PROCHOT
s	Schmitt trigger
12	12mA sink/source capability
OUT	Output pin
OD	Open-drain output pin
AOUT	Output pin (Analog)
IN	Input pin (digital)
AIN	Input pin(Analog)

7.2 W83795G Pin Description List

Pin Name	Pin No.	Power Plane	Type	Description
VREF	1	3VSB	AOUT	Reference voltage output. (2.048V)
AGND	2	GND	Power	Ground for Analog Circuit
TR5	3	3VSB	AIN	Thermistor 5 sensing input. (default)
VSEN12				Voltage sensing input. Detection range is 0~2.048V.
TR6	4	3VSB	AIN	Thermistor 6 sensing input. (default)
VSEN13				Voltage sensing input. Detection range is 0~2.048V.
D1+	5	3VSB	AIN	Thermal diode 1 D+. (default)

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Pin Name	Pin No.	Power Plane	Type	Description
TR1+				Thermistor 1 sensing input.
VDSEN14+				Voltage sensing input. Detection range is 0~2.048V.
D1-	6	3VSB	AIN	Thermal diode 1 D-. (default)
TR1-				Thermistor 1 sensing input.
VDSEN14-				Voltage sensing input, it has to connect to GND.
D2+	7	3VSB	AIN	Thermal diode 2 D+. (default)
TR2+				Thermistor 2 sensing input.
VDSEN15+				Voltage sensing input. Detection range is 0~2.048V.
D2-	8	3VSB	AIN	Thermal diode 2 D-. (default)
TR2-				Thermistor 2 sensing input.
VDSEN15-				Voltage sensing input, it has to connect to GND.
D3+	9	3VSB	AIN	Thermal diode 3 D+. (default)
TR3+				Thermistor 3 sensing input.
VDSEN16+				Voltage sensing input. Detection range is 0~2.048V.
D3-	10	3VSB	AIN	Thermal diode 3 D-. (default)
TR3-				Thermistor 3 sensing input.
VDSEN16-				Voltage sensing input, it has to connect to GND.
D4+	11	3VSB	AIN	Thermal diode 4 D+. (default)
TR4+				Thermistor 4 terminal input.

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Pin Name	Pin No.	Power Plane	Type	Description
VDSEN17+				Voltage sensing input. Detection range is 0~2.048V.
D4-	12	3VSB	AIN	Thermal diode 4 D-. (default)
TR4-				Thermistor 4 sensing input.
VDSEN17-				Voltage sensing input, it has to connect to GND.
VDD0/VCORE1/ VSEN1	13	3VSB	AIN	Voltage sensing input. Detection range is 0~2.048V. When Dynamic VID (DVID) function is enable. VCORE1 sensing input for PVID or VDD0 sensing input for SVID.
VDD1/VCORE2/ VSEN2	14	3VSB	AIN	Voltage sensing input. Detect range is 0~2.048V. When Dynamic VID (DVID) function is enable. VCORE2 sensing input for PVID or VDD1 sensing input for SVID.
VDDNB/VCORE3/ VSEN3	15	3VSB	AIN	Voltage sensing input. Detect range is 0~2.048V. When Dynamic VID (DVID) function is enable. VDDNB sensing input for SVID. VCORE3 sensing input for PVID or VDDNB sensing input for SVID.
VSEN4	16	3VSB	AIN	Voltage sensing input. Detect range is 0~2.048V
VSEN5	17	3VSB	AIN	Voltage sensing input. Detect range is 0~2.048V
VSEN6	18	3VSB	AIN	Voltage sensing input. Detect range is 0~2.048V
VSEN7	19	3VSB	AIN	Voltage sensing input. Detect range is 0~2.048V
VSEN8	20	3VSB	AIN	Voltage sensing input. Detect range is 0~2.048V
VSEN9	21	3VSB	AIN	Voltage sensing input. Detect range is 0~2.048V
VSEN10	22	3VSB	AIN	Voltage sensing input. Detect range is 0~2.048V
VSEN11	23	3VSB	AIN	Voltage sensing input. Detect range is 0~2.048V

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Pin Name	Pin No.	Power Plane	Type	Description
3VDD	24	-	POWER	+3V VDD power. It is also a voltage monitor channel. This pin has internal divider resistors to scale down the input voltage for analog voltage measurement. Bypass with the parallel combination of 10μF (electrolytic or tantalum) and 0.1μF (ceramic) bypass capacitors.
3VSB	25	-	POWER	This pin is power for W83795G. It is also a voltage monitor channel. This pin has internal divider resistors to scale down the input voltage for analog voltage measurement. Bypass with the parallel combination of 10μF (electrolytic or tantalum) and 0.1μF (ceramic) bypass capacitors.
VBAT	26	-	POWER	VBAT supplies power for CASEOPEN. Besides, it is also a voltage monitor channel for +3V on-board battery. This pin has internal divider resistors to scale down the input voltage for analog voltage measurement.
CASEOPEN#	27	VBAT	IN_{ts}	CASEOPEN detection. An active low input from an external device when chassis is Intruded. This signal will be latched even the chassis is closed.
VTT	28	VTT	POWER	Intel® CPU Vtt power. It is also a voltage monitor channel. Detect range is 0~2.048V
PECI	29	3VSB	V4	Intel® CPU PECI interface. (default)
SCL_TSI			V3	AMD® CPU SB-TSI interface.
SDA_TSI	30	3VSB	V3	AMD® CPU SB-TSI interface
THERMTRIP#			V5	CPU THERMTRIP# signal. (default) When CPU assert THERMTRIP# signal, W83795G will latch this event.
SYSRSTIN#	31	3VSB	IN_{ts}	System reset input. (default) When this pin is asserted to low, Watch-dog timer will be reset.
FANIN13			IN_{ts}	Fan tachometer input
PROCHOT3#			V5	This is a bi-directional pin. As an input signal, when it is pull-ed to low, the

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Pin Name	Pin No.	Power Plane	Type	Description
				corresponding fan control output pins will be set to a preset value.
CLKIN	32	3VSB	IN_{ts}	System clock input. PECI ,AMD-TSI ,VID and FAN functions will use this clock to drive logics.
SCL	33	3VSB	IN_{ts}	I^2C Serial Bus Clock.
SDA	34	3VSB	IN_{ts}/ OD_{12}	I^2C Serial Bus bi-directional data.
SMI#	35	3VSB	OD_{12}	System Management Interrupt. (default)
FANIN14			IN_{ts}	Fan tachometer input
PROCHOT4#			V5	This is a bi-directional pin. As an input signal, when it is pull-ed to low, the corresponding fan control output pins will be set to a preset value.
OVT#	36	3VSB	OD_{12}	Over temperature alert. Low active.
BEEP	37	3VSB	OD_{12}	BEEP output when abnormal event occurs. When this is no abnormal events, this pin asserts high.
PWRBTN#	38	3VSB	OD_{12}	Power Button output for enable/disable power supply. (default) This pin is related to ASF commands.
PROCHOT1#			V5	This is a bi-directional pin. As an input signal, when it is pull-ed to low, the corresponding fan control output pins will be set to a preset value.
WDTRST#	39	3VSB	OD_{12}	Output signal for system reset. (default) There are two reset sources: Watch-dog timer and ASF RESET command. When reset event occurs, this pin will assert 100ms low pulse for system reset.
PROCHOT2#			V5	This is a bi-directional pin. As an input signal, when it is pull-ed to low, the corresponding fan control output pins will be set to a preset value.

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Pin Name	Pin No.	Power Plane	Type	Description
FANIN1	40	3VSB	IN_{ts}	Fan tachometer input
FANCTL1	41	3VSB	OUT_{12}/ AOUT	Fan speed control PWM/DC output. When the power of 3VDD is 0V, this pin will drive logic 0. The power of this pin is supplied by 3VSB. It can be configured to PWM/DC mode by registers. Default is PWM output. As DC output, 256 steps output voltage scaled to 0~3VSB.
ADDR0			IN_{ts}	I^2C device address bit0 trapping during 3VSB power on.
FANIN2	42	3VSB	IN_{ts}	Fan tachometer input
FANCTL2	43	3VSB	OUT_{12}/ AOUT	Fan speed control PWM/DC output. When the power of 3VDD is 0V, this pin will drive logic 0. The power of this pin is supplied by 3VSB. It can be configured to PWM/DC mode by registers. Default is PWM output. As DC output, 256 steps output voltage scaled to 0~3VSB.
ADDR1			IN_{ts}	I^2C device address bit1 trapping during 3VSB power on.
FANIN3	44	3VSB	IN_{ts}	Fan tachometer input
FANCTL3	45	3VSB	OD_{12}/ AOUT	Fan speed control PWM/DC output. When the power of 3VDD is 0V, this pin will drive logic 0. The power of this pin is supplied by 3VSB. It can be configured to PWM/DC mode by registers. Default is PWM output. As DC output, 256 steps output voltage scaled to 0~3VSB.
FANIN4	46	3VSB	IN_{ts}	Fan tachometer input
FANCTL4	47	3VSB	OD_{12}/ AOUT	Fan speed control PWM/DC output. When the power of 3VDD is 0V, this pin will drive logic 0. The power of this pin is supplied by 3VSB. It can be configured to PWM/DC mode by registers. Default is PWM output. As DC output, 256 steps output voltage scaled to 0~3VSB.
FANIN5	48	3VSB	IN_{ts}	Fan tachometer input

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Pin Name	Pin No.	Power Plane	Type	Description
FANCTL5	49	3VSB	OD_{12}/ AOUT	Fan speed control PWM/DC output. When the power of 3VDD is 0V, this pin will drive logic 0. The power of this pin is supplied by 3VSB. It can be configured to PWM/DC mode by registers. Default is PWM output. As DC output, 256 steps output voltage scaled to 0~3VSB.
FANIN6	50	3VSB	IN_{ts}	Fan tachometer input
FANCTL6	51	3VSB	OD_{12}/ AOUT	Fan speed control PWM/DC output. When the power of 3VDD is 0V, this pin will drive logic 0. The power of this pin is supplied by 3VSB. It can be configured to PWM/DC mode a by registers. Default is PWM output. As DC output, 256 steps output voltage scaled to 0~3VSB.
FANIN7	52	3VSB	IN_{ts}	Fan tachometer input
FANCTL7	53	3VSB	OD_{12}/ AOUT	Fan speed control PWM/DC output. (default) When the power of 3VDD is 0V, this pin will drive logic 0. The power of this pin is supplied by 3VSB. It can be configured to PWM/DC mode by registers. Default is PWM output. As DC output, 256 steps output voltage scaled to 0~3VSB.
PROCHOT1#			V5	This is a bi-directional pin. As an input signal, when it is pull-ed to low, the corresponding fan control output pins will be set to a preset value.
FANIN8	54	3VSB	IN_{ts}	Fan tachometer input
FANCTL8	55	3VSB	OD_{12}/ AOUT	Fan speed control PWM/DC output. (default) When the power of 3VDD is 0V, this pin will drive logic 0. The power of this pin is supplied by 3VSB. It can be configured to PWM/DC mode by registers. Default is PWM output. As DC output, 256 steps output voltage scaled to 0~3VSB.

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Pin Name	Pin No.	Power Plane	Type	Description
PROCHOT2#			V5	This is a bi-directional pin. As an input signal, when it is pull-ed to low, the corresponding fan control output pins will be set to a preset value.
GND	56		POWER	System Ground.
PVID0	57	3VSB	V1/V2	Voltage Supply readouts bit 0 from CPU.
GPIO1			INts /OD12	General purpose I/O function. (default)
FANIN9			INts	Fan tachometer input
PVID1	58	3VSB	V1/V2	Voltage Supply readouts bit 1 from CPU.
GPIO2			INts /OD12	General purpose I/O function. (default)
FANIN10			INts	Fan tachometer input
PVID2	59	3VSB	V1/V2	Voltage Supply readouts bit 2 from CPU.
GPIO3			INts /OD12	General purpose I/O function. (default)
FANIN11			INts	Fan tachometer input
PECI_REQ#			OD12	PECI control signal for CPU entering C3/C4 state.
PVID3	60	3VSB	V1/V2	Voltage Supply readouts bit 3 from CPU.
GPIO4			INts /OD12	General purpose I/O function. (default)
FANIN12			INts	Fan tachometer input
PVID4	61	3VSB	V1/V2	Voltage Supply readouts bit 4 from CPU.
GPIO5			INts /OD12	General purpose I/O function. (default)
VOLT_FAULT#			OD12	Active-Low output. This pin will be a logic Low when the voltage exceeds its high/low limit.

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Pin Name	Pin No.	Power Plane	Type	Description
PVID5	62	3VSB	V1/V2	Voltage Supply readouts bit 5 from CPU.
GPIO6			INts /OD12	General purpose I/O function. (default)
FAN_FAULT#			OD12	Active-Low output. This pin will be a logic Low when any Fan is abnormally stopped.
PVID6	63	3VSB	V1	Voltage Supply readouts bit 6 from CPU.
GPIO7			INts /OD12	General purpose I/O function. (default)
OVT2#			OD12	Over temperature alert. Low active
SCL_SVI			V3	AMD® CPU SVI interface
PVID7	64	3VSB	V1	Voltage Supply readouts bit 7 from CPU.
GPIO8			INts /OD12	General purpose I/O function. (default)
OVT3#			OD12	Over temperature alert. Low active
SDA_SVI			V3	AMD® CPU SVI interface IN: monitor SDA_SVI interface. OD12: response ACK command

7.3 W83795ADG Pin Description List

Pin Name	Pin No.	Power Plane	Type	Description
TR6	1	3VSB	AIN	Thermistor 6 sensing input. (default)
VSEN13				Voltage sensing input. Detection range is 0~2.048V.
D1+	2	3VSB	AIN	Thermal diode 1 D+.(default)

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Pin Name	Pin No.	Power Plane	Type	Description
TR1+				Thermistor 1 sensing input.
VDSEN14+				Voltage sensing input. Detection range is 0~2.048V.
D1-	3	3VSB	AIN	Thermal diode 1 D-. (default)
TR1-				Thermistor 1 sensing input.
VDSEN14-				Voltage sensing input, it has to connect to GND.
D2+	4	3VSB	AIN	Thermal diode 2 D+. (default)
TR2+				Thermistor 2 sensing input.
VDSEN15+				Voltage sensing input. Detection range is 0~2.048V.
D2-	5	3VSB	AIN	Thermal diode 2 D-. (default)
TR2-				Thermistor 2 sensing input.
VDSEN15-				Voltage sensing input, it has to connect to GND.
D3+	6	3VSB	AIN	Thermal diode 3 D+. (default)
TR3+				Thermistor 3 sensing input.
VDSEN16+				Voltage sensing input. Detection range is 0~2.048V.
D3-	7	3VSB	AIN	Thermal diode 3 D-. (default)
TR3-				Thermistor 3 sensing input.
VDSEN16-				Voltage sensing input, it has to connect to GND.
D4+	8	3VSB	AIN	Thermal diode 4 D+. (default)
TR4+				Thermistor 4 terminal input.

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Pin Name	Pin No.	Power Plane	Type	Description
VDSEN17+				Voltage sensing input. Detection range is 0~2.048V.
D4-	9	3VSB	AIN	Thermal diode 4 D-. (default)
TR4-				Thermistor 4 sensing input.
VDSEN17-				Voltage sensing input, it has to connect to GND.
VSEN1	10	3VSB	AIN	Voltage sensing input. Detection range is 0~2.048V.
VSEN2	11	3VSB	AIN	Voltage sensing input. Detect range is 0~2.048V.
VSEN3	12	3VSB	AIN	Voltage sensing input. Detect range is 0~2.048V.
VSEN4	13	3VSB	AIN	Voltage sensing input. Detect range is 0~2.048V
VSEN5	14	3VSB	AIN	Voltage sensing input. Detect range is 0~2.048V
VSEN6	15	3VSB	AIN	Voltage sensing input. Detect range is 0~2.048V
VSEN7	16	3VSB	AIN	Voltage sensing input. Detect range is 0~2.048V
VSEN8	17	3VSB	AIN	Voltage sensing input. Detect range is 0~2.048V
3VDD	18	-	POWER	+3V VDD power. It is also a voltage monitor channel. This pin has internal divided resistors to scale down the input voltage for analog voltage measurement. Bypass with the parallel combination of 10μF (electrolytic or tantalum) and 0.1μF (ceramic) bypass capacitors.
3VSB	19	-	POWER	This pin is power for W83795ADG. It is also a voltage monitor channel. This pin has internal divided resistors to scale down the input voltage for analog voltage measurement. Bypass with the parallel combination of 10μF (electrolytic or tantalum) and 0.1μF (ceramic) bypass capacitors.
VBAT	20	-	POWER	VBAT supplies power for CASEOPEN. Besides, it is also a voltage monitor channel for +3V on-board battery. This pin has internal divided resistors to scale down the input

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Pin Name	Pin No.	Power Plane	Type	Description
				voltage for analog voltage measurement.
CASEOPEN#	21	VBAT	IN_{ts}	CASEOPEN detection. An active low input from an external device when chassis is Intruded. This signal will be latched even the chassis is closed.
VTT	22	VTT	POWER	Intel® CPU Vtt power. It is also a voltage monitor channel. Detect range is 0~2.048V
PECI	23	3VSB	V4	Intel® CPU PECI interface. (default)
SYSRSTIN#	24	3VSB	IN_{ts}	System reset input. (default) When this pin is asserted to low, Watch-dog timer will be reset.
FANIN13			IN_{ts}	Fan tachometer input
PROCHOT3#			V5	This is a bi-directional pin. As an input signal, when it is pulled to low, the corresponding fan control output pins will be set to a preset value.
CLKIN	25	3VSB	IN_{ts}	System clock input. PECI and FAN functions will use this clock to drive logics.
SCL	26	3VSB	IN_{ts}	I^2C Serial Bus Clock.
SDA	27	3VSB	IN_{ts}/ OD_{12}	I^2C Serial Bus bi-directional data.
SMI#	28	3VSB	OD_{12}	System Management Interrupt. (default)
FANIN14			IN_{ts}	Fan tachometer input
PROCHOT4#			V5	This is a bi-directional pin. As an input signal, when it is pull-ed to low, the corresponding fan control output pins will be set to a preset value.
OVT#	29	3VSB	OD_{12}	Over temperature alert. Low active.
BEEP				BEEP output when abnormal event occurs. When this is no abnormal events, this pin asserts high. (default)
PWRBTN#	30	3VSB	OD_{12}	Power Button output for enable/disable power supply. (default)

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Pin Name	Pin No.	Power Plane	Type	Description
				This pin is related to ASF commands.
PROCHOT1#			V5	This is a bi-directional pin. As an input signal, when it is pull-ed to low, the corresponding fan control output pins will be set to a preset value.
WDTRST#	31	3VSB	OD_{12}	Output signal for system reset. (default) There are two reset sources: Watch-dog timer and ASF RESET command. When reset event occurs, this pin will assert 100ms low pulse for system reset.
PROCHOT2#			V5	This is a bi-directional pin. As an input signal, when it is pull-ed to low, the corresponding fan control output pins will be set to a preset value.
FANIN1	32	3VSB	IN_{ts}	Fan tachometer input
FANCTL1	33	3VSB	OUT_{12}/ AOUT	Fan speed control PWM/DC output. When the power of 3VDD is 0V, this pin will drive logic 0. The power of this pin is supplied by 3VSB. It can be configured to PWM/DC mode by registers. Default is PWM output. As DC output, 256 steps output voltage scaled to 0~3VSB.
ADDR0			IN_{ts}	I^2C device address bit0 trapping during 3VSB power on.
FANIN2	34	3VSB	IN_{ts}	Fan tachometer input
FANCTL2	35	3VSB	OUT_{12}/ AOUT	Fan speed control PWM/DC output. When the power of 3VDD is 0V, this pin will drive logic 0. The power of this pin is supplied by 3VSB. It can be configured to PWM/DC mode by registers. Default is DC output. As DC output, 256 steps output voltage scaled to 0~3VSB.

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Pin Name	Pin No.	Power Plane	Type	Description
ADDR1			IN_{ts}	I^2C device address bit1 trapping during 3VSB power on.
FANIN3	36	3VSB	IN_{ts}	Fan tachometer input
FANIN4	37	3VSB	IN_{ts}	Fan tachometer input
FANIN5	38	3VSB	IN_{ts}	Fan tachometer input
FANIN6	39	3VSB	IN_{ts}	Fan tachometer input
FANIN7	40	3VSB	IN_{ts}	Fan tachometer input
FANIN8	41	3VSB	IN_{ts}	Fan tachometer input
GND	42		POWER	System Ground.
GPIO1	43	3VSB	INts /OD_{12}	General purpose I/O function. (default)
FANIN9			IN_{ts}	Fan tachometer input
GPIO2	44	3VSB	INts /OD_{12}	General purpose I/O function. (default)
FANIN10			IN_{ts}	Fan tachometer input
GPIO3	45	3VSB	INts /OD_{12}	General purpose I/O function. (default)
FANIN11			IN_{ts}	Fan tachometer input
PECI_REQ#			OD_{12}	PECI control signal for CPU entering C3/C4 state.
GPIO4	46	3VSB	INts /OD_{12}	General purpose I/O function. (default)
FANIN12			IN_{ts}	Fan tachometer input
VREF	47	3VSB	AOUT	Reference voltage output. (2.048V)

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Pin Name	Pin No.	Power Plane	Type	Description
TR5	48	3VSB	AIN	Thermistor 5 sensing input.(default)
VSEN12				Voltage sensing input. Detection range is 0~2.048V.

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8. REGISTER SUMMARY – BANK0

NNEMONIC	ADD (Hex)	POR (Hex)	TYPE	Description
ID, Bank Select Registers				
Bank Select	00	80	RW	Bank Select
Vender ID	FD	5C	RO	Nuvoton Vender ID
Chip ID	FE	79	RO	Nuvoton Chip ID
Device ID	FB	5x	RO	Nuvoton Device ID (x = 0,1,2…)
Configuration and Address Select Registers				
I2CADDR	FC	*	RO	I^2C Address
CONFIG	01	1x	RW	Configuration (64Pin=11h,48Pin=15h)
Multi-Function Pin Control Registers				
VOLT CTRL1/2	02/03	FF/38	RW	Voltage monitoring control registers
TEMP CTRL1/2	04/05	1F/55	RW	Temperature monitoring control registers
FANIN CTRL1/2	06/07	FF/00	RW	FANIN monitoring control registers
VMIGB CTRL	08	0F	RW	Voltage monitoring input gain buffer control
GPIO MODE	09	00	RW	GPIO I/O mode control
GPIO IN	0A	*	RO	GPIO input data
GPIO OUT	0B	FF	RW	GPIO output data
Watch Dog Timer Registers				
WDT LOCK	0C	00	WO	Lock Watch Dog
WDT ENABLE	0D	00	RW	Watch Dog Enable
WDT STS	0E	00	RW	Watch Dog Status
WDT TIMER	0F	00	RW	Watch Dog Timeout Timer
Voltage/Temperature/FANIN Reading Registers				
Voltage/ Temperature/ FANIN Reading	10-3B	*	RO	Monitored channel VSEN1- VSEN11, VTT, 3VDD, 3VSB, VBAT, TR5/VSEN12, TR6/VSEN13, TD1/TR1/VDSEN14, TD2/TR2/VDSEN15, TD3/TR3/VDSEN16, TD4/TR4/VDSEN17, DTS1-DTS8, and FANIN1-FANIN8 readout high byte.
VR LSB	3C	*	RO	Monitored channel readout low byte.
SMI# Control and Status Registers				
SMI CTRL	40	10	RW	SMI control
SMI STS 1 - SMI STS 7	41-47	00	RO	SMI status register 1-7
SMI MASK 1 -	48-4E	*	RW	SMI mask register 1-7

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NNEMONIC	ADD (Hex)	POR (Hex)	TYPE	Description
SMI MASK7				
OVT and BEEP Control Registers				
BEEP CTRL1 - BEEP CTRL6	50-55	00	RW	BEEP control register 1-6
OVT GLB	58	00	RW	OVT global enable
OVT1 CTRL1 **OVT1 CTRL2**	59 5A	00 00	RW	OVT1 control register 1-2
OVT2 CTRL1 **OVT2 CTRL2**	5B 5C	00 00	RW	OVT2 control register 1-2
OVT2 CTRL1 **OVT2 CTRL2**	5D 5E	00 00	RW	OVT3 control register 1-2
THERMTRIP and PROCHOT Control Registers				
THERM CTRL	5F	00	RW	THERMTRIP control and status
PROC STS	60	00	RW	PROCHOT processor hot status
PROC1 CTRL **PROC4 CTRL**	61 64	00 00	RW	PROCHOT1# - PROCHOT4 processor hot control
Voltage Fault Control Registers				
VOLT FAULT1- VOLT FAULT3	65-67	00	RW	VOLT_FAULT# control register 1-3
Fan Fault Control Registers				
FAN FAULT1 **FAN FAULT2**	68 69	00 00	RW	FAN_FAULT# control register 1-2
VID Control and Status Registers				
VID CTRL	6A	00	RW	VID control
DVID LIMHI/LIMLO	6B/6C	64/64	RW	Dynamic VID high / low tolerance
VSEN1-VSEN3 VIDIN	6D-6F	*	RO	VSEN1-VSEN3 VID input value
Voltage/Temperature/FANIN Limitation Registers				
VSEN1_HL/LL~ VSEN11_HL/LL	70-85	FF/00	RW	VSEN1 - VSEN11 voltage high / low limit
VTT_HL/LL	86/87	FF/00	RW	VTT voltage high / low limit
3VDD_HL/LL	88/89	FF/00	RW	3VDD voltage high / low limit
3VSB_HL/LL	8A/8B	FF/00	RW	3VSB voltage high / low limit
VBAT_HL/LL	8C/8D	FF/00	RW	VBAT voltage high / low limit
VOLT1_HL/LL_LSB	8E/8F	FF/00	RW	voltage high / low limit low byte register1
VOLT2_HL/LL_LSB	90/91	FF/00	RW	voltage high / low limit low byte register2
VOLT3_HL/LL_LSB	92/93	3F/00	RW	voltage high / low limit low byte register3

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NNEMONIC	ADD (Hex)	POR (Hex)	TYPE	Description
VOLT4_HL/LL_LSB	94/95	FF/00	RW	voltage high / low limit low byte register4
TD1/TR1 Critical/ Critical Hystersis	96/97	64/5F	RW	TD1/TR1 critical, critical hystersis
TD1/TR1 Warning/ Warning Hystersis	98/99	55/50	RW	TD1/TR1 warning, warning hystersis
TD2/TR2 Critical/ Critical Hystersis	9A/9B	64/5F	RW	TD2/TR2 critical, critical hystersis
TD2/TR2 Warning/ Warning Hystersis	9C/9D	55/50	RW	TD2/TR2 warning, warning hystersis
TD3/TR3 Critical/ Critical Hystersis	9E/9F	64/5F	RW	TD3/TR3 critical, critical hystersis
TD3/TR3 Warning/ Warning Hystersis	A0/A1	55/50	RW	TD3/TR3 warning, warning hystersis
TD4/TR4 Critical/ Critical Hystersis	A2/A3	64/5F	RW	TD4/TR4 critical, critical hystersis
TD4/TR4 Warning/ Warning Hystersis	A4/A5	55/50	RW	TD4/TR4 warning, warning hystersis
TR5 Critical/ Critical Hystersis	A6/A7	64/5F	RW	TR5 critical, critical hystersis
TR5 Warning/ Warning Hystersis	A8/A9	55/50	RW	TR5 warning, warning hystersis
TR6 Critical/ Critical Hystersis	AA/AB	64/5F	RW	TR6 critical, critical hystersis
TR6 Warning/ Warning Hystersis	AC/AD	55/50	RW	TR6 warning, warning hystersis
DTS Critical/ Critical Hystersis	B2/B3	64/5F	RW	DTS1-DTS8 (Digital Temperature Sensor) critical, critical hystersis
DTS Warning/ Warning Hystersis	B4/B5	55/50	RW	DTS1-DTS8 (Digital Temperature Sensor) warning, warning hystersis
FANIN1_HL - FANIN14_HL	B6-C3	FF	RW	FANIN1-FANIN14 fan tachometer high limit
FHL1_LSB - FHL7_LSB	C4-CA	EE	RW	FANIN1-FANIN14 fan tachometer high limit low byte

*: See registers description,

8.1 ID, Bank Select Registers

Inside the W83795G/ADG resides three banks of registers. Customers must set the banks correctly to access correct registers. All the registers described here can be accessed in all banks.

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8.1.1.1. Bank Select Register (Bank Select)

Three banks of registers are inside the W83795G/ADG. The register bank could be selected by programming the Bank Select register. All 00_{HEX} Addresses in these three banks are defined as Bank Select register.

Location: Bank 0, 1, 2, 3 Address 00_{HEX}
Type: Read / Write
Reset: 3VSB Rising,
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.
Default Value: 80_{HEX}

BIT	DESCRIPTION
7	**HBACS** (High Byte Access) 0 = Return the low byte while reading Nuvoton Vendor ID. 1 = Return the high byte while reading Nuvoton Vendor ID.
6-3	**Reserved.**
2-0	**Bank Select.** 000_{BIN} = Bank 0 is selected. 001_{BIN} = Bank 1 is selected. 010_{BIN} = Bank 2 is selected. 011_{BIN} = Bank 3 is selected.

8.1.1.2. Nuvoton Vender ID Register (Vender ID)

The Nuvoton Vender ID contains two-byte data. By programming register **HBACS**, the customer can choose to access either the high or the low byte of Nuvoton Vender ID.

Location: Bank 0, 1, 2, 3 Address FD_{HEX}
Type: Read Only
Reset: No Reset
Default Value: $5C_{HEX}$ / $A3_{HEX}$

BIT	DESCRIPTION
7-0	**Vendor ID.** Return $5C_{HEX}$ if **HBACS** = 1; return $A3_{HEX}$ if **HBACS** = 0.

8.1.1.3. Nuvoton Chip ID Register (Chip ID)

Location: Bank 0, 1, 2, 3 Address FE_{HEX}
Type: Read Only
Reset: No Reset
Default Value: 79_{HEX}

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BIT	DESCRIPTION
7-0	**Chip ID.** Chip ID of W83795G/ADG is 79_{HEX}

8.1.1.4. Nuvoton Device Version ID Register (Device ID)

Location: Bank 0, 1, 2, 3 Address FB_{HEX}
Type: Read Only
Reset: No Reset
Default Value: 51_{HEX}

BIT	DESCRIPTION
7-0	**Device ID.** Device is W83795G/ADG and 51_{HEX} is for B Version , 52_{HEX} is for C Version *A version chip Device ID is 50_{HEX} in Address FF_{HEX}.

8.2 Configuration and Address Select Registers

8.2.1.1. I²C Address Register (I2CADDR)

There are four Addresses (58_{HEX}, $5A_{HEX}$, $5C_{HEX}$, $5E_{HEX}$) that can be assigned for the I^2C interface. These four addresses can be set by strapping ADDR0 & ADDR1 input value at 100ms after power ready.

Location: Bank 0 Address FC_{HEX}
Type: Read Only
Reset: 100ms after 3VSB Rising.
Default Value: NA

BIT	DESCRIPTION
7	**Reserved.** **Nuvoton Test Mode**. Test modes for production. Nuvoton strongly suggests the customer not to use these registers to avoid system malfunction.
6-0	**ADDR_HM.** The value of **ADDR_HM** is W83795G/ADG SMBus slave address that strapped from ADDR0 and ADDR1 at 100ms after 3VSB power ready.

ADDR1	ADDR0	I^2C Address
0	0	58_{HEX}
0	1	$5A_{HEX}$

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	1	0	$5C_{HEX}$	
	1	1	$5E_{HEX}$	

8.2.1.2. Configuration Register (CONFIG)

Configuration Register controls the system reset source, stop, power down and warning output mode.

Location: Bank 0 Address 01_{HEX}
Type: Read / Write
Reset: Bit 0~1 & 3~4 & 7:
3VSB Rising,
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.
Bit 5 & 6:
3VSB Rising,
Default Value: 11_{HEX} is for W83795G
15_{HEX} is for W83795ADG

BIT	DESCRIPTION
7	**INIT.** Setting to one restores power-on default values to all registers, except the Serial Bus Address register. This bit clears itself since the power-on default is zero.
6	**SYSRST_MD.** 0 = no operation when the SYSRSTIN# input signal is issued. 1 = the whole chip will be reset when the SYSRSTIN# input signal is issued.
5	**RST_VDD_MD.** 0 = no operation when 3VDD is up. 1 = the whole chip will be reset when 3VDD is up.
4-3	**CLKSel.** Select CLKIN clock input. 00_{BIN} = CLKIN clock input is 14.318MHz. 01_{BIN} = CLKIN clock input is 24MHz. 10_{BIN} = CLKIN clock input is 33MHz. (Default) 11_{BIN} = CLKIN clock input is 48MHz.
2	**Config48.** Package version (power on trapping), 0 = 64 pin package for W83795G 1 = 48 pin package for W83795ADG
1	**INT_Clear.** A one disables the SMI# outputs without affecting the contents of Interrupt Status Registers. The device will stop monitoring at last channel. It will resume upon clearing of this bit.
0	**START.**

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BIT	DESCRIPTION
	0 = Disable monitoring operations. 1 = Enable monitoring operations.

8.3 Multi-Function Pin Control Registers

Many functions exhibited in the W83795G/ADG are not default functions, and might share pin out with other functions. Here lists three registers that define the function enable registers.

8.3.1.1. Monitoring Control Register

Setting to one will enable the corresponding monitoring Channels. Clearing to 0 will disable that monitoring channels.

Location:

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VOLT CTRL1 - Bank 0 Address 02_{HEX}
VOLT CTRL2 - Bank 0 Address 03_{HEX}
TEMP CTRL1 - Bank 0 Address 04_{HEX}
TEMP CTRL2 - Bank 0 Address 05_{HEX}
FANIN CTRL1 - Bank 0 Address 06_{HEX}
FANIN CTRL2 - Bank 0 Address 07_{HEX}

Type: Read / Write
Reset: 3VSB Rising.
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

VOLT CTRL1 – Voltage Monitoring Control Register
Location: Bank 0 Address 02_{HEX}
Default Value: FF_{HEX}

BIT	DESCRIPTION
7	**EN_VSEN8** – Enable VSEN8 voltage monitoring. 0 = Disable 1 = Enable
6	**EN_VSEN7** – Enable VSEN7 voltage monitoring. 0 = Disable 1 = Enable
5	**EN_VSEN6** – Enable VSEN6 voltage monitoring. 0 = Disable 1 = Enable
4	**EN_VSEN5** – Enable VSEN5 voltage monitoring. 0 = Disable 1 = Enable
3	**EN_VSEN4** – Enable VSEN4 voltage monitoring. 0 = Disable 1 = Enable
2	**EN_VSEN3** – Enable VSEN3 voltage monitoring. 0 = Disable 1 = Enable
1	**EN_VSEN2** – Enable VSEN2 voltage monitoring. 0 = Disable 1 = Enable
0	**EN_VSEN1** – Enable VSEN1 voltage monitoring. 0 = Disable 1 = Enable

VOLT CTRL2 – Voltage Monitoring Control Register
Location: Bank 0 Address 03_{HEX}

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Default Value: 38_{HEX}

BIT	DESCRIPTION
7	**Reserved**
6	**EN_VBAT** – Enable VBAT voltage monitoring. 0 = Disable (Default) 1 = Enable
5	**EN_3VSB** – Enable 3VSB voltage monitoring. 0 = Disable 1 = Enable
4	**EN_3VDD** – Enable 3VDD voltage monitoring. 0 = Disable 1 = Enable
3	**EN_VTT** – Enable VTT voltage monitoring. 0 = Disable 1 = Enable
2	**EN_VSEN11** – Enable VSEN11 voltage monitoring. 0 = Disable (Default) 1 = Enable (This function is not for W83795ADG)
1	**EN_VSEN10** – Enable VSEN10 voltage monitoring. 0 = Disable (Default) 1 = Enable (This function is not for W83795ADG)
0	**EN_VSEN9** – Enable VSEN9 voltage monitoring. 0 = Disable (Default) 1 = Enable (This function is not for W83795ADG)

TEMP CTRL1 – Temperature Monitoring Control Register

Location: Bank 0 Address 04_{HEX}

Default Value: $1F_{HEX}$

BIT	DESCRIPTION
7	**Reserved**
6	**Reserved**
5	**EN_DTS** – Enable DTS (Digital Temperature Sensor) interface from INTEL PECI or AMD SB-TSI. 0 = Disable (Default) 1 = Enable. Note: Program all registers about DTS in Bank 3 before enabling DTS.
4	**Reserved**
3-2	**TR6/VSEN13_MD** – TR6/VSEN13 monitoring selection mode. $0X_{BIN}$ = Disable TR6/VSEN13 monitoring 10_{BIN} = Enable VSEN13 voltage monitoring

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BIT	DESCRIPTION
	11 BIN = Enable TR6 thermistor temperature monitoring (Default)
1-0	**TR5/VSEN12_MD** – TR5/VSEN12 monitoring selection mode. 0X BIN = Disable TR5/VSEN12 monitoring 10 BIN = Enable VSEN12 voltage monitoring 11 BIN = Enable TR5 thermistor temperature monitoring (Default)

TEMP CTRL2 – Temperature Monitoring Control Register
Location: Bank 0 Address 05_{HEX}
Default Value: 55_{HEX}

BIT	DESCRIPTION
7-6	**TD4/TR4/VDSEN17_MD** – TD4/TR4/VDSEN17 monitoring selection mode. Note that it needs refer the application to set register. 00 BIN = Disable TD4/TR4/VDSEN17 monitoring 01 BIN = Enable TD4 thermal diode temperature monitoring (Default) 10 BIN = Enable VDSEN17 different mode voltage monitoring 11 BIN = Enable TR4 thermistor temperature monitoring
5-4	**TD3/TR3/VDSEN16_MD** – TD3/TR3/VDSEN16 monitoring selection mode. Note that it needs refer the application to set register. 00 BIN = Disable TD3/TR3/VDSEN16 monitoring 01 BIN = Enable TD3 thermal diode temperature monitoring (Default) 10 BIN = Enable VDSEN16 different mode voltage monitoring 11 BIN = Enable TR3 thermistor temperature monitoring
3-2	**TD2/TR2/VDSEN15_MD** – TD2/TR2/VDSEN15 monitoring selection mode. Note that it needs refer the application to set register. 00 BIN = Disable TD2/TR2/VDSEN15 monitoring 01 BIN = Enable TD2 thermal diode temperature monitoring (Default) 10 BIN = Enable VDSEN15 different mode voltage monitoring 11 BIN = Enable TR2 thermistor temperature monitoring
1-0	**TD1/TR/VDSEN14_MD** – TD1/TR1/VDSEN14 monitoring selection mode. Note that it needs refer the application to set register. 00 BIN = Disable TD1/TR1/VDSEN14 monitoring 01 BIN = Enable TD1 thermal diode temperature monitoring (Default) 10 BIN = Enable VDSEN14 different mode voltage monitoring 11 BIN = Enable TR1 thermistor temperature monitoring

FANIN CTRL1 – FANIN Monitoring Control Register
Location: Bank 0 Address 06_{HEX}
Default Value: FF_{HEX}

BIT	DESCRIPTION
7	**EN_FANIN8** – Enable FANIN8 monitoring.

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	0 = Disable 1 = Enable
6	**EN_FANIN7** – Enable FANIN7 monitoring. 0 = Disable 1 = Enable
5	**EN_FANIN6** – Enable FANIN6 monitoring. 0 = Disable 1 = Enable
4	**EN_FANIN5** – Enable FANIN5 monitoring. 0 = Disable 1 = Enable
3	**EN_FANIN4** – Enable FANIN4 monitoring. 0 = Disable 1 = Enable
2	**EN_FANIN3** – Enable FANIN3 monitoring. 0 = Disable 1 = Enable
1	**EN_FANIN2** – Enable FANIN2 monitoring. 0 = Disable 1 = Enable
0	**EN_FANIN1** – Enable FANIN1 monitoring. 0 = Disable 1 = Enable

FANIN CTRL2 – FANIN Monitoring Control Register
Location: Bank 0 Address 07_{HEX}
Default Value: 00_{HEX}

BIT	DESCRIPTION
7-6	**Reserved**
5	**EN_FANIN14** – Select and enable SMI#/FANIN14/PROCHOT4# multi-function pin. 0 = Disable FANIN14 monitoring. Then SMI# and PROCHOT4# can be selected by EN_PROCHOT4. 1 = Enable FANIN14 monitoring.
4	**EN_FANIN13** – Select and enable SYSRSTIN#/FANIN13/PROCHOT3# multi-function pin. 0 = Disable FANIN13 monitoring. Then SYSRSTIN# and PROCHOT3# can be selected by EN_PROCHOT3. 1 = Enable FANIN13 monitoring.
3	**EN_FANIN12** – Select and enable FANIN12/PVID3/GPIO4 multi-function pin. 0 = Disable FANIN12 monitoring. Then PVID3 and GPIO4 can be selected by VID_TAB. 1 = Enable FANIN12 monitoring. PVID3 function is not for W83795ADG.
2	**EN_FANIN11** – Select and enable FANIN11/PECI_REQ#/PVID2/GPIO3 multi-function

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BIT	DESCRIPTION
	pin. 0 = Disable FANIN11 monitoring. Then PECI_REQ#, PVID2 and GPIO3 can be selected by VID_TAB and EN_VOLTFAULT. 1 = Enable FANIN11 monitoring. PVID2 function is not for W83795ADG.
1	**EN_FANIN10** – Select and enable FANIN10/PVID1/GPIO2 multi-function pin. 0 = Disable FANIN10 monitoring. Then PVID1 and GPIO2 can be selected by VID_TAB. 1 = Enable FANIN10 monitoring. PVID1 function is not for W83795ADG.
0	**EN_FANIN9** – Select and enable FANIN9/PVID0/GPIO1 multi-function pin. 0 = Disable FANIN9 monitoring. Then PVID0 and GPIO1 can be selected by VID_TAB. 1 = Enable FANIN9 monitoring. PVID0 function is not for W83795ADG.

8.3.1.2. Voltage Monitoring Input Gain Buffer Control Register (VMIGB CTRL)

Clear to 0 will enable x8 input gain buffer for the corresponding voltage monitoring Channels. Set to 1 will enable x1 input gain buffer for the corresponding voltage monitoring channels.

Location: Bank 0 Address 08_{HEX}
Type: Read / Write
Reset: 3VSB Rising.
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.
Default Value: $0F_{HEX}$

BIT	DESCRIPTION
7-4	**Reserved**
3	**GAIN_VDSEN17** – Enable VDSEN17 voltage monitoring input gain buffer. 0 = x8 1 = x1
2	**GAIN_VDSEN16** – Enable VDSEN16 voltage monitoring input gain buffer. 0 = x8 1 = x1
1	**GAIN_VDSEN15** – Enable VDSEN15 voltage monitoring input gain buffer. 0 = x8 1 = x1
0	**GAIN_VDSEN14** – Enable VDSEN14 voltage monitoring input gain buffer. 0 = x8 1 = x1

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8.3.1.3. GPIO Control Register (GPIO CTRL)

Reset: 3VSB Rising.
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

GPIO MODE – GPIO I/O Mode Control Register
Location: Bank 0 Address 09_{HEX}
Default Value: 00_{HEX}
Type: Read / Write

BIT	DESCRIPTION
7-0	**GPIO MODE** – Select GPIO8-GPIO1 I/O mode. 0 = GPIO8-1 are programming as input pins. (Default) 1 = GPIO8-1 are programming as output pins. BIT7 is for GPIO8 and BIT6 is for GPIO7, etc… BIT[7:4] are reserved functions for W83795ADG.

GPIO IN – GPIO Input Data Register
Location: Bank 0 Address $0A_{HEX}$
Default Value: N.A.
Type: Read Only

BIT	DESCRIPTION
7-0	**GPIO IN** – Input GPIO8-GPIO1 Data. The respective bits can be read only from pins. Write accesses will be ignored. BIT7 is for GPIO8 and BIT6 is for GPIO7, etc… BIT[7:4] are reserved functions for W83795ADG.

GPIO OUT – GPIO Output Data Register
Location: Bank 0 Address $0B_{HEX}$
Default Value: FF_{HEX}
Type: Read / Write

BIT	DESCRIPTION
7-0	**GPIO OUT** – Output GPIO8-GPIO1 Data. For output ports, it needs to set GPIO_MOD register and the respective bits can be read/written and produced to pins. BIT7 is for GPIO8 and BIT6 is for GPIO7, etc… BIT[7:4] are reserved functions for W83795ADG.

8.4 Watch Dog Timer Registers

The W83795G/ADG is integrated with a Watch Dog Timer, which enables users to reset the system by WDTRST# (Pin 39) while the system is in an abnormal state. Once Watch Dog Timer is enabled, the

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W83795G/ADG starts to count down, and the host should set the timer for further count down or clear/disable the timer to prevent the W83795G/ADG from issuing reset signals.

Watch Dog Timer consists of four registers. WDT LOCK (Bank0, CR0C) and WDT ENABLE (Bank0, CR0D) are used to activate Soft-WDT and Hard-WDT, respectively. WDT STS (Bank0, CR0E) and WDT TIMER (Bank0, CR0F) can inform the host whether the system time is up or not.

Two kinds of watchdog timer functions are supported by the W83795G/ADG. One is so-called Soft Watch Dog Timer, and the other is Hard Watch Dog Timer.

Hard Watch Dog timer, if enabled, will start a 4-minute WDT after the system reset is completed. (A low-to-high transition on SYSRSTIN# pin). BIOS needs to write a 00_{HEX} into WDT TIMER (Bank0, CR0F) to disable the timer within 4 minutes. Otherwise, WDTRST# will assert to reset the system.

Soft Watch Dog Timer will start counting down whenever Timeout Time is set and Soft Watch Dog Timer is enabled. WDTRST# will be issued when the time runs out.

Soft Watch Dog Timer will be disabled automatically after receiving SYSRSTIN # low signal.

WDT ENABLE (Bank0, CR0D [2]/**ENWDT**) must be set to 1 if wish to program the four Watch Dog Timer Registers.

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8.4.1 Watch Dog Timer Register Details

8.4.1.1. Lock Watch Dog Register (WDT LOCK)

Writing this register enables the Soft or Hard Watch Dog Timer. This register type is write-only and WDT ENABLE confirms whether the write is successful.

Location: Bank 0 Address $0C_{HEX}$
Type: Write Only
Reset: 3VSB Rising.
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.
Default Value: 00_{HEX}

BIT	DESCRIPTION
7-0	**UNLOCK CODE** Write 55_{HEX}, Enables Soft Watch Dog Timer. Write AA_{HEX}, Disables Soft Watch Dog Timer. Write 33_{HEX}, Enables Hard Watch Dog Timer. Write CC_{HEX}, Disables Hard Watch Dog Timer.

8.4.1.2. Watch Dog Enable Register (WDT ENABLE)

Location: Bank 0 Address $0D_{HEX}$
Type: Read/Write
Reset: 3VSB Rising.
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.
Default Value: 00_{HEX}

BIT	DESCRIPTION
7-3	**Reserved.**
2	**ENWDT.** Setting this bit to 1 will enable the Watch Dog Timer function, which WDTRST# resets the system while the time is out.
1	**HARD.** 0 = Hard Watch Dog is disabled. 1 = Hard Watch Dog is enabled.
0	**SOFT.** 0 = Soft Watch Dog is disabled. 1 = Soft Watch Dog is enabled.

8.4.1.3. Watch Dog Status Register (WDT STS)

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Location: Bank 0 Address $0E_{HEX}$
Type: Read / Write
Reset: 3VSB Rising.
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.
Default Value: 00_{HEX}

BIT	DESCRIPTION
7-4	**Reserved.**
3-2	**WDT_ST.** These 2 bits record last WDT stage for BIOS readout. The information is used to help BIOS to identify WDT timeout issuance.
1	**HARD_TO.** 1 = A hard timeout occurs. This bit will be cleared after reading.
0	**SOFT_TO.** 1 = A soft timeout occurs. This bit will be cleared after reading.

8.4.1.4. Watch Dog Timer Register (WDT TIMER)

Location: Bank 0 Address $0F_{HEX}$
Type: Read / Write
Reset: 3VSB Rising.
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.
Default Value: 00_{HEX}

BIT	DESCRIPTION
7-0	**WDT TIMER –** Timeout timer To write 00_{HEX} can disable the timer while in Hard Watch Dog Timer mode. To set Timeout Time for SOFT Watch Dog Timer, the unit is minute.

Timeout Time is unit in minutes. 0 represents time is up or the timer is cleared. 1 represents there is still 1 minute time for this timer. Similarly, 2 means there is still 2 minutes left.

The second time will automatically be reset to 0 second when Timeout Time register is set.

8.5 Voltage/Temperature/FANIN Reading Registers

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8.5.1 Voltage Channel Register Details

8.5.1.1. Voltage Channel Monitored Value

Location:

VSEN1 - Bank 0 Address 10_{HEX}
VSEN2 - Bank 0 Address 11_{HEX}
VSEN3 - Bank 0 Address 12_{HEX}
VSEN4 - Bank 0 Address 13_{HEX}
VSEN5 - Bank 0 Address 14_{HEX}
VSEN6 - Bank 0 Address 15_{HEX}
VSEN7 - Bank 0 Address 16_{HEX}
VSEN8 - Bank 0 Address 17_{HEX}
VSEN9 - Bank 0 Address 18_{HEX}
VSEN10 - Bank 0 Address 19_{HEX}
VSEN11 - Bank 0 Address $1A_{HEX}$
VTT - Bank 0 Address $1B_{HEX}$
3VDD - Bank 0 Address $1C_{HEX}$
3VSB - Bank 0 Address $1D_{HEX}$
VBAT - Bank 0 Address $1E_{HEX}$
VR LSB - Bank 0 Address $3C_{HEX}$

Type: Read Only
Reset: 3VSB Rising.

VOLTAGE READOUT

BIT	7	6	5	4	3	2	1	0
NAME	Voltage Readout Value (high byte). 10-bit voltage value bit[9:2] (**VSEN9-VSEN11** Bank0 Address 18_{HEX} -$1A_{HEX}$ functions are not for W83795ADG)							

VR LSB

BIT	7	6	5	4	3	2	1	0
NAME	Voltage Readout Value (low byte). 10-bit voltage value bit[1:0]		Reserved					

VOLTAGE VALUE CALCULATION

VR LSB together with VOLTAGE READOUT forms the 10-bit count value. If VOLTAGE READOUT (Temperature readout high byte) is read successively, the W83795G/ADG will latch the VR LSB (Temperature readout low byte) for next read. Then voltage readout high byte and low byte are combined to *10-bitVoltageValue*.

For VSEN1-VSEN13 and VDSEN14-VDSEN17 and VTT voltage monitoring, real voltage calculations should follow the formula:

$$Voltage(V) = 10 - bitCountValue \times 0.002$$

And the rest voltage 3VSB, 3VDD and VBAT voltage monitoring, real voltage calculations should follow the formula:

$$Voltage(V) = 10 - bitCountValue \times 0.006$$

8.5.1.2. Temperature/Voltage Channel Monitored Value

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W83795G/ADG have multi-function pins for temperature and voltage monitoring. It needs set TEMP CRL1 and TEMP CRL2 registers to select temperature or voltage monitoring.
If select temperature monitoring, the effective width of Temperature Readout Value (high byte) and VR LSB (low byte) is for temperature data format is 10-bit 2's complement (9-bit plus sign).

Location:

TR5/VSEN12 - Bank 0 Address $1F_{HEX}$
TR6/VSEN13 - Bank 0 Address 20_{HEX}
TD1/TR1/VDSEN14 - Bank 0 Address 21_{HEX}
TD2/TR2/VDSEN15 - Bank 0 Address 22_{HEX}
TD3/TR3/VDSEN16 - Bank 0 Address 23_{HEX}
TD4/TR4/VDSEN17 - Bank 0 Address 24_{HEX}
VR LSB - Bank 0 Address $3C_{HEX}$

Type: Read Only
Reset: 3VSB Rising.

FOR TEMPERATURE MONITORING SELECTION:

TEMPERATURE READOUT

BIT	7	6	5	4	3	2	1	0
NAME	Temperature Readout Value (high byte). The real temperature value calculation is referred to TEMPERAUTRE VALUE CACLULATION description. 10-bit 2's complement bit[9:2]							
VALUE	SIGN	64	32	16	8	4	2	1

VR LSB

BIT	7	6	5	4	3	2	1	0
NAME	Temperature Readout Value (low byte). 10-bit 2's complement bit[1:0]		Reserved					
VALUE	0.5	0.25	0					

FOR VOLTAGE MONITORING SELECTION:

VOLTAGE READOUT

BIT	7	6	5	4	3	2	1	0
NAME	Voltage Readout Value (high byte). The real voltage value calculation is referred to VOLTAGE VALUE CACLULATION description. 10-bit voltage value bit[9:2]							

VR LSB

BIT	7	6	5	4	3	2	1	0
NAME	Voltage Readout Value (low byte). 10-bit voltage value bit[1:0]		Reserved					

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8.5.1.3. Temperature Channel Monitored Value

Before W83795G/ADG reads the DTS1-DTS8 (Digital Temperature Sensor) temperature from INTEL PECI or AMD SB-TSI, it needs initial relative registers in BANK3. The effective width of Temperature Readout Value (high byte) and VR LSB (low byte) is for temperature data format is 10-bit 2's complement (9-bit plus sign).

Location:

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DTS1 - Bank 0 Address 26_{HEX}
DTS2 - Bank 0 Address 27_{HEX}
DTS3 - Bank 0 Address 28_{HEX}
DTS4 - Bank 0 Address 29_{HEX}
DTS5 - Bank 0 Address $2A_{HEX}$
DTS6 - Bank 0 Address $2B_{HEX}$
DTS7 - Bank 0 Address $2C_{HEX}$
DTS8 - Bank 0 Address $2D_{HEX}$
VR LSB - Bank 0 Address $3C_{HEX}$

Type: Read Only
Reset: 3VSB Rising.

TEMPERATURE READOUT

BIT	7	6	5	4	3	2	1	0
NAME	Temperature Readout Value (high byte). 10-bit 2's complement bit[9:2]							
VALUE	SIGN	64	32	16	8	4	2	1

VR LSB

BIT	7	6	5	4	3	2	1	0
NAME	Temperature Readout Value (low byte). 10-bit 2's complement bit[1:0]		Reserved.					
VALUE	0.5	0.25	0					

TEMPERAUTRE VALUE CALCULATION

VR LSB together with TEMPERAUTRE READOUT forms the 10-bit count value. If TEMPERAUTRE READOUT (Temperature readout high byte) is read successively, the W83795G/ADG will latch the VR LSB (Temperature readout low byte) for next read. Then temperature readout high byte and low byte are combined to 10bits. Temperature readout is represented 10-bit 2's complement (9-bit plus sign) data format.

NOTE that it means thermal diode open when temperature value is -128℃.

The following table shows some examples.

TEMPERATURE	TEMPERAUTRE READOUT (HIGH BYTE)								VR LSB (LOW BYTE)							
	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
+127.75℃	0	1	1	1	1	1	1	1	1	1	X	X	X	X	X	X
0.25℃	0	0	0	0	0	0	0	0	0	1	X	X	X	X	X	X
0℃	0	0	0	0	0	0	0	0	0	0	X	X	X	X	X	X
-1.25℃	1	1	1	1	1	1	1	0	1	1	X	X	X	X	X	X
-25.75℃	1	1	1	0	0	1	1	0	0	1	X	X	X	X	X	X
-128℃	1	0	0	0	0	0	0	0	0	0	X	X	X	X	X	X

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8.5.2 Fan Register Details

8.5.2.1. Fan Tachometer Readout high/low Byte Register (FANIN COUNT)

The FANIN_COUNT maintains current count value of corresponding fan inputs. When 3VSB is on, it is cleared (00_{HEX}). The effective width of FANIN_COUNT (high byte) and VR LSB (low byte) is 12-bit.

Location:

FANIN1 COUNT - Bank 0 Address $2E_{HEX}$
FANIN2 COUNT - Bank 0 Address $2F_{HEX}$
FANIN3 COUNT - Bank 0 Address 30_{HEX}
FANIN4 COUNT - Bank 0 Address 31_{HEX}
FANIN5 COUNT - Bank 0 Address 32_{HEX}
FANIN6 COUNT - Bank 0 Address 33_{HEX}
FANIN7 COUNT - Bank 0 Address 34_{HEX}
FANIN8 COUNT - Bank 0 Address 35_{HEX}
FANIN9 COUNT - Bank 0 Address 36_{HEX}
FANIN10 COUNT - Bank 0 Address 37_{HEX}
FANIN11 COUNT - Bank 0 Address 38_{HEX}
FANIN12 COUNT - Bank 0 Address 39_{HEX}
FANIN13 COUNT - Bank 0 Address $3A_{HEX}$
FANIN14 COUNT - Bank 0 Address $3B_{HEX}$
VR LSB - Bank 0 Address $3C_{HEX}$

Type: Read Only
Reset: 3VSB Rising.
Default Value: 00_{HEX}

FANIN1_COUNT~FANIN14_COUNT

BIT	7	6	5	4	3	2	1	0
NAME	FANIN_COUNT (FANIN tachometer readout high byte). The real FANIN RPM value calculation is referred to FANIN COUNT CACLULATION description. 12-bitCount Value bit[11:4]							

VR LSB

BIT	7	6	5	4	3	2	1	0
NAME	FANIN_COUNT (FANIN tachometer readout low byte) 12-bitCount Value bit [3:0]				Reserved.			

FANIN COUNT CALCULATION

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VR LSB together with FANIN COUNT is form the 12-bit count value. If FANIN COUNT (FANIN tachometer readout high byte) is read successively, the W83795G/ADG will latch the VR LSB (FANIN tachometer readout low byte) for next read. Then FANIN tachometer high byte and low byte are combined to *12-bitCountValue*. Real RPM (Rotate per Minute) calculations should follow the formula:

$$FanSpeed(RPM) = \frac{1.35 \times 10^6}{(12 - bitCountValue) \times (FanPoles/4)}$$

In this formula, *FanPoles* stands for the number of NS pole pairs inside the fan. Normally an N-S-N-S Fan (*FanPoles* = 4) generates 2 pulses after completing one rotation.

The frequency range for the fan tachometer is below 4.5 KHz (if FanPoles=4, it means 135KRPM). It is almost impossible, but a fan working faster than this will cause the malfunction of the W83795G/ADG.

8.6 SMI# Control and Status Registers

Several mechanisms are provided to alarm the system when monitored channels are abnormal. In this paragraph, three kinds of control/status registers are introduced. “Real time status” shows the current status of each channel; “Channel Mask” defines which channel needs to issue warning when abnormal operation occurs, and when the warning should be ignored due to floating or in other circumstances. The final one is “Interrupt Status,” which gives the host information of which channel is issuing alert, and the host can base on this channel and do proper process to ensure a reliable system.

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8.6.1 SMI Control/Status Register Map

The interrupt mode for voltage and FANIN is only two-time interrupt mode.

For temperature, there are three modes to serve: <1> Comparator mode, <2>One-Time Interrupt mode, and <3> Two-Time Interrupt mode.

8.6.1.1. SMI Control Register (SMI CTRL)

Location: Bank 0 Address 40_{HEX}

Type: Read / Write

Reset: 3VSB Rising.
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

Default Value: 10_{HEX}

BIT	DESCRIPTION
7	**RTSACS.** 0 = Read Interrupt status from CR41~CR47. (Default) 1 = Read real-time status from CR41~CR47.
6-5	**Reserved.**
4	**SMI_MD.** 0 = SMI# outputs low level signal and active high. 1 = SMI# outputs 200 us low pulse signal. (Default)
3-2	**TEMP_SMI_MD.** Temperature SMI Mode Select. **00_{BIN} = Comparator Interrupt Mode: (Default)** Temperature sensors exceeding T_O (Critical temperature) limit causes an interrupt and this interrupt will be cleared by reading all the Interrupt Status. **01_{BIN} = Two Time Interrupt Mode:** Temperature sensors are used in the interrupt mode with hysteresis. Temperature exceeding T_O (Critical Temperature) causes an interrupt. Temperatures that fall below T_{HYST} (Critical Temperature Hysteresis) will also cause an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. Once the temperature exceeds T_O (Critical Temperature), an interrupt will be issued and the bit will be reset before the temperature falls to T_{HYST} (Critical Temperature Hysteresis). **10_{BIN} = One Time Interrupt Mode:** Temperature sensors are used in the interrupt mode with hysteresis. Temperature exceeding T_O (Critical Temperature) causes an interrupt and then temperature going below T_{HYST} (Critical Temperature Hysteresis) will not cause an interrupt. Once an interrupt event has occurred by exceeding T_O (Critical Temperature), then going below T_{HYST} (Critical Temperature Hysteresis), and interrupt will not occur again until the temperature exceeding T_O (Critical Temperature). **11_{BIN} = Two Time Non-related Interrupt Mode:** Temperature sensors are used in the interrupt mode with hysteresis. Temperature exceeding T_O, causes an interrupt and then temperature going below T_{HYST} will also cause an interrupt. Once an interrupt event has occurred by exceeding T_O, then reset, if the temperature remains above the T_{HYST}. If this mode is selected, for all monitor channels (it is not necessary to read the status

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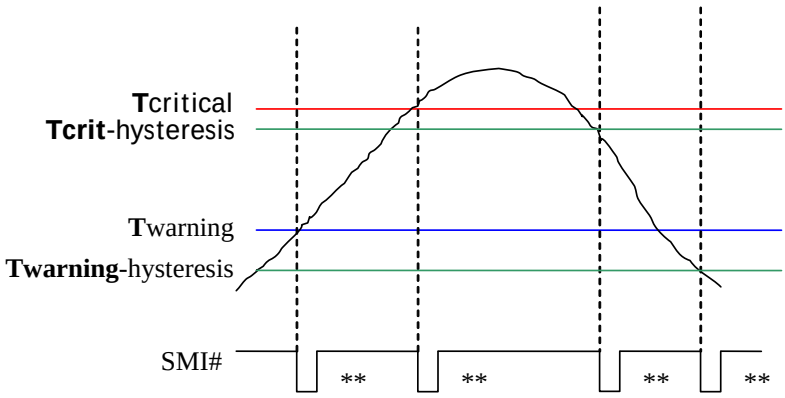
BIT	DESCRIPTION
	for generating the next IRQ/SMI# pulse.  Two-Time Intrrupt Mode ** : Interrupt Status is read Note: It can be programmed to be as not necessary to read the status for generating the next SMI# pulse by setting TEMP_SMI_MD = 2'b11.
1	**EN_SMI.** 0 = disable SMI# signal output. (Default) 1 = enable SMI# signal output.
0	**SMI_POL.** 0 = Default polarity. 1 = Polarity inverted.

8.6.1.2. SMI Status Register (SMI STS)

Status register can be read by interrupt or real-time mode and the function selected by SMI control register CR40.Bit7.

If status register is read by interrupt mode and SMI control register CR40.Bit7 is set as 0 (Default). Then a one represents corresponding channel have been exceed its limit. Status registers will clear the interrupt flag.

If status register is read by real-time mode and SMI control register CR40.Bit7 is set as 1. Then status registers show whether the values of related channels exceed the limit or not at the polling moment. The returning of 1 indicates the limit of related channel defined in limit registers has been exceeded.

Location:

SMI STS1 - Bank 0 Address 41_{HEX}
SMI STS2 - Bank 0 Address 42_{HEX}
SMI STS3 - Bank 0 Address 43_{HEX}
SMI STS4 - Bank 0 Address 44_{HEX}
SMI STS5 - Bank 0 Address 45_{HEX}
SMI STS6 - Bank 0 Address 46_{HEX}
SMI STS7 - Bank 0 Address 47_{HEX}

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Type: Read Only
Reset: 3VSB Rising.

SMI STS1

BIT	7	6	5	4	3	2	1	0
NAME	VSEN8	VSEN7	VSEN6	VSEN5	VSEN4	VSEN3	VSEN2	VSEN1
DEFAULT	0	0	0	0	0	0	0	0

SMI STS2

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	VBAT	3VSB	3VDD	VTT	VSEN11	VSEN10	VSEN9
DEFAULT	0	0	0	0	0	0	0	0

(Bit 2:0 **VSEN9-VSEN11** are not for W83795ADG)

SMI STS3

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Reserved	TD4/TR4 VDSEN17	TD3/TR3 VDSEN16	TD2/TR2 VDSEN15	TD1/TR1 VDSEN14	TR6 VSEN13	TR5 VSEN12
DEFAULT	0	0	0	0	0	0	0	0

SMI STS4

BIT	7	6	5	4	3	2	1	0
NAME	DTS8	DTS7	DTS6	DTS5	DTS4	DTS3	DTS2	DTS1
DEFAULT	0	0	0	0	0	0	0	0

SMI STS5

BIT	7	6	5	4	3	2	1	0
NAME	FANIN8	FANIN7	FANIN6	FANIN5	FANIN4	FANIN3	FANIN2	FANIN1
DEFAULT	0	0	0	0	0	0	0	0

SMI STS6

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Chassis	FANIN14	FANIN13	FANIN12	FANIN11	FANIN10	FANIN9
DEFAULT	0	0	0	0	0	0	0	0

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SMI STS7

BIT	7	6	5	4	3	2	1	0
NAME	Reserved		TART6	TART5	TART4	TART3	TART2	TART1
DEFAULT	0	0	0	0	0	0	0	0

8.6.1.3. SMI Mask Register (SMI MASK)

Setting to one will disable the corresponding interrupt sources. Clearing to 0 will enable that interrupt source.

SMI MASK6 CR4D.Bit7 is CLR_CHS (Clear Chassis), writing this bit to one will clear the internal caseopen latch. After the latch is cleared, CLR_CHS will self-reset to 0.

Location:

SMI MASK1 - Bank 0 Address 48_{HEX}
SMI MASK2 - Bank 0 Address 49_{HEX}
SMI MASK3 - Bank 0 Address $4A_{HEX}$
SMI MASK4 - Bank 0 Address $4B_{HEX}$
SMI MASK5 - Bank 0 Address $4C_{HEX}$
SMI MASK6 - Bank 0 Address $4D_{HEX}$
SMI MASK7 - Bank 0 Address $4E_{HEX}$

Type: Read / Write
Reset: 3VSB Rising.
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

SMI MASK1

BIT	7	6	5	4	3	2	1	0
NAME	VSEN8	VSEN7	VSEN6	VSEN5	VSEN4	VSEN3	VSEN2	VSEN1
DEFAULT	0	0	0	0	0	0	0	0

SMI MASK2

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	VBAT	3VSB	3VDD	VTT	VSEN11	VSEN10	VSEN9
DEFAULT	0	1	0	0	0	0	0	0

(Bit 2:0 **VSEN9-VSEN11** are not for W83795ADG)

SMI MASK3

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BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Reserved	TD4/TR4 VDSEN17	TD3/TR3 VDSEN16	TD2/TR2 VDSEN15	TD1/TR1 VDSEN14	TR6 VSEN13	TR5 VSEN12
DEFAULT	0	0	0	0	0	0	0	0

SMI MASK4

BIT	7	6	5	4	3	2	1	0
NAME	DTS8	DTS7	DTS6	DTS5	DTS4	DTS3	DTS2	DTS1
DEFAULT	1	1	1	1	1	1	1	1

SMI MASK5

BIT	7	6	5	4	3	2	1	0
NAME	FANIN8	FANIN7	FANIN6	FANIN5	FANIN4	FANIN3	FANIN2	FANIN1
DEFAULT	0	0	0	0	0	0	0	0

SMI MASK6

BIT	7	6	5	4	3	2	1	0
NAME	CLR_CHS	Chassis	FANIN14	FANIN13	FANIN12	FANIN11	FANIN10	FANIN9
DEFAULT	0	1	1	1	1	1	1	1

(The CLR_CHS must write 1 to clear internal caseopen latch status when VBAT input.)

SMI MASK7

BIT	7	6	5	4	3	2	1	0
NAME	Reserved		TART6	TART5	TART4	TART3	TART2	TART1
DEFAULT	0	0	1	1	1	1	1	1

8.7 OVT and BEEP Control Registers

Another solution to deal with abnormal situation is through OVT (Over Temperature) or Beep.

OVT, as the name suggests, represents abnormal temperatures. In some applications, it can work with Fan control to throttle the Fan Speed.

Beep can directly use sound of two tones to inform the user of abnormal system operation. Unlike OVT, Beep can be issued due to abnormal operations of any channel.

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8.7.1 BEEP/OVT Control Registers Details

8.7.1.1. BEEP Control Register (BEEP CTRL)

Setting to one will enable the corresponding BEEP output. Clearing to 0 will disable that BEEP output. The BEEP alarm function is enabled or disabled by the EN_BEEP control bit at CR55.Bit7.

Location:

BEEP CTRL1 - Bank 0 Address 50_{HEX}
BEEP CTRL2 - Bank 0 Address 51_{HEX}
BEEP CTRL3 - Bank 0 Address 52_{HEX}
BEEP CTRL4 - Bank 0 Address 53_{HEX}
BEEP CTRL5 - Bank 0 Address 54_{HEX}
BEEP CTRL6 - Bank 0 Address 55_{HEX}

Type: Read / Write
Reset: 3VSB Rising.
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

BEEP CTRL1

BIT	7	6	5	4	3	2	1	0
NAME	VSEN8	VSEN7	VSEN6	VSEN5	VSEN4	VSEN3	VSEN2	VSEN1
DEFAULT	0	0	0	0	0	0	0	0

BEEP CTRL2

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	VBAT	3VSB	3VDD	VTT	VSEN11	VSEN10	VSEN9
DEFAULT	0	0	0	0	0	0	0	0

(Bit 2:0 **VSEN9-VSEN11** are not for W83795ADG)

BEEP CTRL3

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Reserved	TD4/TR4 VDSEN17	TD3/TR3 VDSEN16	TD2/TR2 VDSEN15	TD1/TR1 VDSEN14	TR6 VSEN13	TR5 VSEN12
DEFAULT	0	0	0	0	0	0	0	0

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BEEP CTRL4

BIT	7	6	5	4	3	2	1	0
NAME	DTS8	DTS7	DTS6	DTS5	DTS4	DTS3	DTS2	DTS1
DEFAULT	0	0	0	0	0	0	0	0

BEEP CTRL5

BIT	7	6	5	4	3	2	1	0
NAME	FANIN8	FANIN7	FANIN6	FANIN5	FANIN4	FANIN3	FANIN2	FANIN1
DEFAULT	0	0	0	0	0	0	0	0

BEEP CTRL6

BIT	7	6	5	4	3	2	1	0
NAME	EN_BEEP	Chassis	FANIN14	FANIN13	FANIN12	FANIN11	FANIN10	FANIN9
DEFAULT	0	0	0	0	0	0	0	0

The BEEP alarm function is enabled or disabled by the EN_BEEP control bit at CR55.Bit7.
If EN_BEEP is set to 0, it is disabled BEEP output. (Default)
If EN_BEEP is set to 1, it is enabled BEEP output.

8.7.1.2. OVT Global Enable Register (OVT GLB)

Location: Bank 0 Address 58_{HEX}
Type: Read / Write
Reset: 3VSB Rising.
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.
Default Value: 00_{HEX}

BIT	DESCRIPTION
7	**OVT_SEL.** Function select of BEEP for W83795ADG 1 = OVT# 0 = BEEP (Default)
6	**OVT_POL.** 0 = OVT1#, OVT2# and OVT3# polarity is active low. (Default) 1 = OVT1#, OVT2# and OVT3# polarity is active high. (OVT2# and OVT3# are not for W83795ADG)
5-4	**Reserved.**
3	**OVT_MD.**

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BIT	DESCRIPTION
	There are two OVT# signal output types. **0_{BIN} : Comparator Mode: (Default)** Temperature exceeding Tcritical (Critical Temperature) activates the OVT# output until the temperature is lower than T_{HYST} (Critical Temperature Hysteresis). **1_{BIN} : Interrupt Mode:** Temperatures exceeding Tcritical (Critical Temperature) will activate the OVT# output until temperature sensors registers are read. If the current temperature rises from T_{HYST} (Critical Temperature Hysteresis) and exceeds Tcritical (Critical Temperature), the OVT# pin will be de-asserted. If the temperature falls below T_{HYST}, the OVT# pin will also generates an interrupt until it is reset by reading temperature sensors (interrupt status). Once the interrupt is generated, the OVT# pin does not issue additional interrupts even it the temperature remains above Tcritical.
2	**EN_OVT3.** 0 = Disable OVT3# output 1 = Enable OVT3# output (OVT3# is not for W83795ADG)
1	**EN_OVT2.** 0 = Disable OVT2# output 1 = Enable OVT2# output (OVT2# is not for W83795ADG)
0	**EN_OVT1.** 0 = Disable OVT1# output 1 = Enable OVT1# output

8.7.1.3. OVT1 Control Register (OVT1 CTRL)

Setting to one will enable the corresponding OVT1# output. Clearing to 0 will disable that OVT1# output.

The OVT1# function is enabled or disabled by the EN_OVT1 control bit at CR58.Bit0.

The OVT1# signal will be issued when the selected temperature channel detects the temperature exceeds the allowed range 4 times in a row.

Location:

OVT1 CTRL1 - Bank 0 Address 59_{HEX}
OVT1 CTRL2 - Bank 0 Address $5A_{HEX}$

Type: Read / Write
Reset: 3VSB Rising.
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

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OVT1 CRL1

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Reserved	TD4/TR4	TD3/TR3	TD2/TR2	TD1/TR1	TR6	TR5
DEFAULT	0	0	0	0	0	0	0	0

OVT1 CRL2

BIT	7	6	5	4	3	2	1	0
NAME	DTS8	DTS7	DTS6	DTS5	DTS4	DTS3	DTS2	DTS1
DEFAULT	0	0	0	0	0	0	0	0

8.7.1.4. OVT2 Control Register (OVT2 CTRL)

Setting to one will enable the corresponding OVT2# output. Clearing to 0 will disable that OVT2# output. The OVT2# function is enabled or disabled by the EN_OVT2 control bit at CR58.Bit1.
OVT2# is not for W83795ADG, it is reserved register.

Location:

OVT2 CTRL1 - Bank 0 Address $5B_{HEX}$
OVT2 CTRL2 - Bank 0 Address $5C_{HEX}$

Type: Read / Write
Reset: 3VSB Rising.
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

OVT2 CTRL1

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Reserved	TD4/TR4	TD3/TR3	TD2/TR2	TD1/TR1	TR6	TR5
DEFAULT	0	0	0	0	0	0	0	0

OVT2 CTRL2

BIT	7	6	5	4	3	2	1	0
NAME	DTS8	DTS7	DTS6	DTS5	DTS4	DTS3	DTS2	DTS1
DEFAULT	0	0	0	0	0	0	0	0

8.7.1.5. OVT3 Control Register (OVT3 CTRL)

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Setting to one will enable the corresponding OVT3# output. Clearing to 0 will disable that OVT3# output.

The OVT3# function is enabled or disabled by the EN_OVT3 control bit at CR58.Bit2.

OVT3# is not for W83795ADG, it is reserved register.

Location:

OVT3 CTRL1 - Bank 0 Address $5D_{HEX}$
OVT3 CTRL2 - Bank 0 Address $5E_{HEX}$

Type: Read / Write
Reset: 3VSB Rising.
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

OVT3 CTRL1

BIT	7	6	5	4	3	2	1	0
NAME	**Reserved**	**Reserved**	**TD4/TR4**	**TD3/TR3**	**TD2/TR2**	**TD1/TR1**	**TR6**	**TR5**
DEFAULT	0	0	0	0	0	0	0	0

OVT3 CTRL2

BIT	7	6	5	4	3	2	1	0
NAME	**DTS8**	**DTS7**	**DTS6**	**DTS5**	**DTS4**	**DTS3**	**DTS2**	**DTS1**
DEFAULT	0	0	0	0	0	0	0	0

8.8 THERMTRIP and PROCHOT Control Registers

8.8.1.1. THERMTRIP Control and Status Register (THERM CTRL)

Setting to one will enable the corresponding THRMTRIP# . Clearing to 0 will disable that THRMTRIP# .

Location: Bank 0 Address $5F_{HEX}$
Default Value: 00_{HEX}
Type: Read / Write
Reset: 3VSB Rising.
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

BIT	DESCRIPTION

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7-3	**Reserved.**
2	**CLR_THRM** – Clear the thermal trip status. If write 1, to clear thermal trip status.
1	**EN_THRM** – Enable thermal trip event. 0 = Disable 1 = Enable
0	**THRM_STS** – Thermal trip event status. (Read Only) 1 = Thermal trip event occurred. Power by VBAT

8.8.1.2. PROCHOT Control and Status Registers

When PROCHOT# is set to be output and the corresponding temperature channel detects a temperature higher than the critical temperature, the PROCHOT# signal will be issued.

When PROCHOT# is set to be input, it will be auto mapping to the table as below:

PROCHOT Channel	PROCHOT1#	PROCHOT2#	PROCHOT3#	PROCHOT4#
Corresponding DTS Channel	DTS1 DTS5	DTS2 DTS6	DTS3 DTS7	DTS4 DTS8

In Smart Fan control mode, if the PROCHOT# is asserted by CPU, the Fan which maps to corresponding DTS channel will be full speed. For the Fan mapping, also refer to 10.1.2.2 Temperature to Fan mapping Relationships Register and 10.1.2.3 Temperature Source Selection Register.

PROC STS – PROCHOT Processor Hot Status Register
Location: Bank 0 Address 60_{HEX}
Default Value: 00_{HEX}
Type: Bit 5 & 4: Read / Write
Bit 3~0: Read only
Reset: Bit 5 & 4:
3VSB Rising,
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.
Bit 3~0:
3VSB Rising,

BIT	DESCRIPTION
7-6	**Reserved.**
5	**SET_PROCHOT2** – Set the PROCHOT2# function. For W83795G 0 = Pin 39 is PROCHOT2# 1 = Pin 55 is PROCHOT2# For W83795ADG 0 = Pin 31 is PROCHOT2# 1 = Disable
4	**SET_PROCHOT1** – Set the PROCHOT1# function.

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BIT	DESCRIPTION
	For W83795G 0 = Pin 38 is PROCHOT1# 1 = Pin 53 is PROCHOT1# For W83795ADG 0 = Pin 30 is PROCHOT1# 1 = Disable
3	**STS_PROCHOT4** – Status of PROCHOT4# . 1 = Meet CPU PROCHOT# active.
2	**STS_PROCHOT3** – Status of PROCHOT3# . 1 = Meet CPU PROCHOT# active.
1	**STS_PROCHOT2** – Status of PROCHOT2#. 1 = Meet CPU PROCHOT# active.
0	**STS_PROCHOT1** – Status of PROCHOT1#. 1 = Meet CPU PROCHOT# active.

PROC1 CTRL – PROCHOT1# Processor Hot Control Register
Location: Bank 0 Address 61_{HEX}
Default Value: 00_{HEX}
Type: Read / Write
Reset: 3VSB Rising.
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

BIT	DESCRIPTION
7	**EN_PROCHOT1** – Enable PROCHOT1# function. 0 = Disable 1 = Enable
6	**PROCHOT1_MOD** – Set the PROCHOT1# mode. 0 = Input mode 1 = Output mode
5	**EN_PH1_TD4** – Enable PROCHOT1# for TD4/TR4. 0 = Disable 1 = Enable
4	**EN_PH1_TD3** – Enable PROCHOT1# for TD3/TR3. 0 = Disable 1 = Enable
3	**EN_PH1_TD2** – Enable PROCHOT1# for TD2/TR2. 0 = Disable 1 = Enable
2	**EN_PH1_TD1** – Enable PROCHOT1# for TD1/TR1. 0 = Disable 1 = Enable

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BIT	DESCRIPTION
1	**EN_PH1_TR2** – Enable PROCHOT1# for TR6. 0 = Disable 1 = Enable
0	**EN_PH1_TR1** – Enable PROCHOT1# for TR5. 0 = Disable 1 = Enable

PROC2 CTRL – PROCHOT2# Processor Hot Control Register

Location: Bank 0 Address 62_{HEX}
Default Value: 00_{HEX}
Type: Read / Write
Reset: 3VSB Rising.
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

BIT	DESCRIPTION
7	**EN_PROCHOT2** – Enable PROCHOT2# function. 0 = Disable 1 = Enable
6	**PROCHOT2_MOD** – Set the PROCHOT2# mode. 0 = Input mode 1 = Output mode
5	**EN_PH2_TD4** – Enable PROCHOT2# for TD4/TR4. 0 = Disable 1 = Enable
4	**EN_PH2_TD3** – Enable PROCHOT2# for TD3/TR3. 0 = Disable 1 = Enable
3	**EN_PH2_TD2** – Enable PROCHOT2# for TD2/TR2. 0 = Disable 1 = Enable
2	**EN_PH2_TD1** – Enable PROCHOT2# for TD1/TR1. 0 = Disable 1 = Enable
1	**EN_PH2_TR2** – Enable PROCHOT2# for TR6. 0 = Disable 1 = Enable
0	**EN_PH2_TR1** – Enable PROCHOT2# for TR5. 0 = Disable 1 = Enable

PROC3 CTRL – PROCHOT3# Processor Hot Control Register

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Location: Bank 0 Address 63_{HEX}
Default Value: 00_{HEX}
Type: Read / Write
Reset: 3VSB Rising.
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

BIT	DESCRIPTION
7	**EN_PROCHOT3** – Enable PROCHOT3# function. 0 = Disable 1 = Enable
6	**PROCHOT3_MOD** – Set the PROCHOT3# mode. 0 = Input mode 1 = Output mode
5	**EN_PH3_TD4** – Enable PROCHOT3# for TD4/TR4. 0 = Disable 1 = Enable
4	**EN_PH3_TD3** – Enable PROCHOT3# for TD3/TR3. 0 = Disable 1 = Enable
3	**EN_PH3_TD2** – Enable PROCHOT3# for TD2/TR2. 0 = Disable 1 = Enable
2	**EN_PH3_TD1** – Enable PROCHOT3# for TD1/TR1. 0 = Disable 1 = Enable
1	**EN_PH3_TR2** – Enable PROCHOT3# for TR6. 0 = Disable 1 = Enable
0	**EN_PH3_TR1** – Enable PROCHOT3# for TR5. 0 = Disable 1 = Enable

PROC4 CTRL – PROCHOT4# Processor Hot Control Register
Location: Bank 0 Address 64_{HEX}
Default Value: 00_{HEX}
Type: Read / Write
Reset: 3VSB Rising.
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

BIT	DESCRIPTION

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BIT	DESCRIPTION
7	**EN_PROCHOT4** – Enable PROCHOT4# function. 0 = Disable 1 = Enable
6	**PROCHOT4_MOD** – Set the PROCHOT4# mode. 0 = Input mode 1 = Output mode
5	**EN_PH4_TD4** – Enable PROCHOT4# for TD4/TR4. 0 = Disable 1 = Enable
4	**EN_PH4_TD3** – Enable PROCHOT4# for TD3/TR3. 0 = Disable 1 = Enable
3	**EN_PH4_TD2** – Enable PROCHOT4# for TD2/TR2. 0 = Disable 1 = Enable
2	**EN_PH4_TD1** – Enable PROCHOT4# for TD1/TR1. 0 = Disable 1 = Enable
1	**EN_PH4_TR2** – Enable PROCHOT4# for TR6. 0 = Disable 1 = Enable
0	**EN_PH4_TR1** – Enable PROCHOT4# for TR5. 0 = Disable 1 = Enable

8.8.1.3. Voltage Fault Control Registers

Setting to one will enable the corresponding VOLT_FAULT# output. Clearing to 0 will disable that VOLT_FAULT# output.

VOLT_FAULT# is not for W83795ADG, they are reserved registers.

VOLT FAULT1 – Voltage Fault Control Register 1

Location: Bank 0 Address 65_{HEX}

Default Value: 00_{HEX}

Type: Read / Write

Reset: 3VSB Rising.
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

VOLT FAULT1

BIT	7	6	5	4	3	2	1	0
NAME	VSEN8	VSEN7	VSEN6	VSEN5	VSEN4	VSEN3	VSEN2	VSEN1
DEFAULT	0	0	0	0	0	0	0	0

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VOLT FAULT2 – Voltage Fault Control Register 2
Location: Bank 0 Address 66_{HEX}
Default Value: 00_{HEX}
Type: Read / Write
Reset: 3VSB Rising.
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

VOLT FAULT2

BIT	7	6	5	4	3	2	1	0
NAME	**Reserved**	**VBAT**	**3VSB**	**3VDD**	**VTT**	**VSEN11**	**VSEN10**	**VSEN9**
DEFAULT	0	0	0	0	0	0	0	0

VOLT FAULT3 – Voltage Fault Control Register 3
Location: Bank 0 Address 67_{HEX}
Default Value: 00_{HEX}
Type: Read / Write
Reset: 3VSB Rising.
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

VOLT FAULT3

BIT	DESCRIPTION
7	**EN_VOLTFAULT** – Enable VOLT_FAULT# function. 0 = Disable 1 = Enable
6	**Reserved.**
5-0	**SET_VOLT_CFG** – Set the VOLT_FAULT# configuration. Setting to one will enable the corresponding VOLT_FAULT# output. Clearing to 0 will disable that VOLT_FAULT# output. Bit5 is for **VDSEN17.** Bit4 is for **VDSEN16.** Bit3 is for **VDSEN15.** Bit2 is for **VDSEN14.** Bit1 is for **VSEN13.** Bit0 is for **VSEN12.**

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8.8.1.4. FAN Fault Control Registers

Setting to one will enable the corresponding FAN_FAULT# output. Clearing to 0 will disable that FAN_FAULT# output.

FAN_FAULT# is not for W83795ADG, they are reserved registers.

FAN CTRL1 – FAN Fault Control Register 1

Location: Bank 0 Address 68_{HEX}

Default Value: 00_{HEX}

Type: Read / Write

Reset: 3VSB Rising.
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

FAN FAULT1

BIT	7	6	5	4	3	2	1	0
NAME	FANIN8	FANIN7	FANIN6	FANIN5	FANIN4	FANIN3	FANIN2	FANIN1
DEFAULT	0	0	0	0	0	0	0	0

FAN CTRL2 – FAN Fault Control Register 2

Location: Bank 0 Address 69_{HEX}

Default Value: 00_{HEX}

Type: Read / Write

Reset: 3VSB Rising.
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

FAN FAULT1

BIT	DESCRIPTION
7	**EN_FANFAULT** – Enable FAN_FAULT# function. 0 = Disable 1 = Enable
6	**Reserved.**
5-0	**SET_FAN_CFG** – Set the FAN_FAULT# configuration. Setting to one will enable the corresponding FAN_FAULT# output. Clearing to 0 will disable that FAN_FAULT# output. Bit5 is for **FANIN14.** Bit4 is for **FANIN13.** Bit3 is for **FANIN12.** Bit2 is for **FANIN11.** Bit1 is for **FANIN10.** Bit0 is for **FANIN9.**

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8.9 VID Control and Status Registers

The W83795G/ADG provides VSEN1, VSEN2 and VSEN3 monitoring channels. VSEN1, VSEN2 and VSEN3 Channels are automatically monitored once 3VSB is applied onto the W83795G/ADG, but the W83795G/ADG will issue alert information only when the corresponding high/low limits of VSEN1, VSEN2 and VSEN3 channels are being violated. ASF is also based on these limit registers to judge the current channel status and report to the host.

Two methods are used to assign the VSEN1, VSEN2 and VSEN3 Limits, manually or automatically by VID inputs. The following register sets allow users to choose their preferred method.

The W83795G/ADG supplies one set of VID input pins for VSEN1, VSEN2 and VSEN3 channels. If dynamic VID function is enabled, the high/low limit of VSEN1, VSEN2 and VSEN3 channel will auto-update when the VID input value changes.

Some VID input pins are multi-function pin. Programming Multi-Function Pin Control Registers properly is required to make these pins function.

VID function is not for W83795ADG, they are reserved registers.

8.9.1.1. VID Control Register (VID CTRL)

Location: Bank 0 Address $6A_{HEX}$

Type: Read / Write

Reset: 3VSB Rising.

Init Reset (CR01.Bit7) is set,

3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,

SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

Default Value: 00_{HEX}

BIT	DESCRIPTION
7	**Latch_VID.** If write 1 (write clear), CR6D~CR6F latches the current pin value of VID.
6	**VIDL_ACS.** VID read out source CR6D~CR6F 0 = Read VID input data 1 = Read VID latch data
5	**EN_DVID3.** If write 1, enable dynamic VID function for VSEN3 If VID is changed, the high/low limit of corresponding VSEN3 sensing voltage will be auto-updated. If manually programming High/Low limit of VSEN3 sensing voltage is required, this bit has to be cleared as 0.
4	**EN_DVID2.** If write 1, enable dynamic VID function for VSEN2 If VID is changed, the high/low limit of corresponding VSEN2 sensing voltage will be auto-updated. If manually programming High/Low limit of VSEN2 sensing voltage is required, this bit has to be cleared as 0.
3	**EN_DVID1.** If write 1, enable dynamic VID function for VSEN1 If VID is changed, the high/low limit of corresponding VSEN1 sensing voltage will be auto-updated. If manually programming High/Low limit of VSEN1 sensing voltage is required, this bit has to be cleared as 0.

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BIT	DESCRIPTION
2-0	**VID_SEL.** VID function enable and VID Table Select: 000_{BIN} = Disable VID function and function of Pin 57~64 are not about VID. (Default) 001_{BIN} = Enable VRM9 table and Pin 61~57 are VID[4:0]. 010_{BIN} = Enable VRM10 table and Pin 63~57 are VID[6:0]. 011_{BIN} = Enable VRM11 table and Pin 64~57 are VID[7:0]. 100_{BIN} = Enable AMD Opteron™ 5 bit VID Codes and Pin 61~57 are VID[4:0]. 101_{BIN} = Enable AMD Opteron™ 6 bit VID Codes and Pin 62~57 are VID[5:0]. 110_{BIN} = Enable AMD SVID table and Pin 63~64 are SCL_SVI and SDA_SVI. 111_{BIN} = Disable VID function and function of Pin 57~64 are not about VID.

8.9.1.2. Dynamic VID High Tolerance Register (DVID LIMHI)

Location: Bank 0 Address $6B_{HEX}$
Type: Read / Write
Reset: 3VSB Rising.
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.
Default Value: 64_{HEX}

BIT	DESCRIPTION
7-0	**Dynamic VID High Tolerance.** If the dynamic VID function (set Bank0 CR6A bit5-3 to 1) is enabled, writing Tolerance register will force VSEN1, VSEN2 and VSEN3 Limit to update with new voltage limits for VSEN1, VSEN2 and VSEN3. The unit is 2mV

8.9.1.3. Dynamic VID Low Tolerance Register (DVID LIMLO)

Location: Bank 0 Address $6C_{HEX}$
Type: Read / Write
Reset: 3VSB Rising.
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.
Default Value: 64_{HEX}

BIT	DESCRIPTION
7-0	**Dynamic VID Low Tolerance.** If the dynamic VID function (set Bank0 CR6A bit5-3 to 1) is enabled, writing Tolerance register will force VSEN1, VSEN2 and VSEN3 Limit Generator to generate new voltage limits for VSEN1, VSEN2 and VSEN3. The unit is 2mV

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8.9.1.4. VSEN1 VID Input Value Register (VSEN1 VIDIN)

Location: Bank 0 Address $6D_{HEX}$
Type: Read Only
Default Value: NA

BIT	DESCRIPTION
7-0	**VIDIN_VSEN1** The value of VIDIN_VSEN1 is determined by setting VID Control Register CR6A.

8.9.1.5. VSEN2 VID Input Value Register (VSEN2 VIDIN)

Location: Bank 0 Address $6E_{HEX}$
Type: Read Only
Default Value: NA

BIT	DESCRIPTION
7-0	**VIDIN_VSEN2** The value of VIDIN_VSEN2 is determined by setting VID Control Register CR6A.

8.9.1.6. VSEN3 VID Input Value Register (VSEN3 VIDIN)

Location: Bank 0 Address $6F_{HEX}$
Type: Read Only
Default Value: NA

BIT	DESCRIPTION
7-0	**VIDIN_VSEN3** The value of VIDIN_VSEN3 is determined by setting VID Control Register CR6A.

8.10 Voltage/Temperature/FANIN Limitation Registers

VSEN9-VSEN11 functions are not for W83795ADG, they are reserved registers.

8.10.1.1. Voltage Channel Limitation Registers

Location:

VSEN1_HL - Bank 0 Address 70_{HEX}
VSEN1_LL - Bank 0 Address 71_{HEX}
VSEN2_HL - Bank 0 Address 72_{HEX}
VSEN2_LL - Bank 0 Address 73_{HEX}
VSEN3_HL - Bank 0 Address 74_{HEX}
VSEN3_LL - Bank 0 Address 75_{HEX}
VSEN4_HL - Bank 0 Address 76_{HEX}
VSEN4_LL - Bank 0 Address 77_{HEX}
VSEN5_HL - Bank 0 Address 78_{HEX}
VSEN5_LL - Bank 0 Address 79_{HEX}
VSEN6_HL - Bank 0 Address $7A_{HEX}$
VSEN6_LL - Bank 0 Address $7B_{HEX}$
VSEN7_HL - Bank 0 Address $7C_{HEX}$

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VSEN7_LL - Bank 0 Address $7D_{HEX}$
VSEN8_HL - Bank 0 Address $7E_{HEX}$
VSEN8_LL - Bank 0 Address $7F_{HEX}$
VSEN9_HL - Bank 0 Address 80_{HEX}
VSEN9_LL - Bank 0 Address 81_{HEX}
VSEN10_HL - Bank 0 Address 82_{HEX}
VSEN10_LL - Bank 0 Address 83_{HEX}
VSEN11_HL - Bank 0 Address 84_{HEX}
VSEN11_LL - Bank 0 Address 85_{HEX}
VTT_HL - Bank 0 Address 86_{HEX}
VTT_LL - Bank 0 Address 87_{HEX}
3VDD_HL - Bank 0 Address 88_{HEX}
3VDD_LL - Bank 0 Address 89_{HEX}
3VSB_HL - Bank 0 Address $8A_{HEX}$
3VSB_LL - Bank 0 Address $8B_{HEX}$
VBAT_HL - Bank 0 Address $8C_{HEX}$
VBAT_LL - Bank 0 Address $8D_{HEX}$
VOLT1_HL_LSB - Bank 0 Address $8E_{HEX}$
VOLT1_LL_LSB - Bank 0 Address $8F_{HEX}$
VOLT2_HL_LSB - Bank 0 Address 90_{HEX}
VOLT2_LL_LSB - Bank 0 Address 91_{HEX}
VOLT3_HL_LSB - Bank 0 Address 92_{HEX}
VOLT3_LL_LSB - Bank 0 Address 93_{HEX}
VOLT4_HL_LSB - Bank 0 Address 94_{HEX}
VOLT4_LL_LSB - Bank 0 Address 95_{HEX}

Reset: 3VSB Rising.
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

VOLTAGE HL/LL (HIGH BYTE)

BIT	7	6	5	4	3	2	1	0
NAME	**VSEN1_HL, VSEN1_LL, VSEN2_HL, VSEN2_LL, VSEN3_HL, VSEN3_LL, VSEN4_HL, VSEN4_LL, VSEN5_HL, VSEN5_LL, VSEN6_HL, VSEN6_LL, VSEN7_HL, VSEN7_LL, VSEN8_HL, VSEN8_LL, VSEN9_HL, VSEN9_LL, VSEN10_HL, VSEN10_LL, VSEN11_HL, VSEN11_LL, VTT_HL, VTT_LL, 3VDD_HL, 3VDD_LL, 3VSB_HL, 3VSB_LL, VBAT_HL, VBAT_LL.** Voltage High / Low Limit (high byte). The real voltage value calculation is referred to VOLTAGE VALUE CACLULATION description. 10-bit voltage value bit[9:2] High Limit default Value is FF_{HEX} Low Limit default Value is 00_{HEX} VSEN9-VSEN11 functions are not for W83795ADG, they are reserved registers.							

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VOLT1_HL/LL_LSB (LOW BYTE)

BIT	7	6	5	4	3	2	1	0
NAME	VSEN4_LSB		VSEN3_LSB		VSEN2_LSB		VSEN1_LSB	
	Voltage High / Low Limit (low byte). 10-bit voltage value bit[1:0] VOLT1_HL_LSB default value is FF_{HEX} VOLT1_LL_LSB default value is 00_{HEX}							

VOLT2_HL/LL_LSB (LOW BYTE)

BIT	7	6	5	4	3	2	1	0
NAME	VSEN8_LSB		VSEN7_LSB		VSEN6_LSB		VSEN5_LSB	
	Voltage High / Low Limit (low byte). 10-bit voltage value bit[1:0] VOLT2_HL_LSB default value is FF_{HEX} VOLT2_LL_LSB default value is 00_{HEX}							

VOLT3_HL/LL_LSB (LOW BYTE)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved		VSEN11_LSB		VSEN10_LSB		VSEN9_LSB	
	Voltage High / Low Limit (low byte). 10-bit voltage value bit[1:0] VOLT3_HL_LSB default value is $3F_{HEX}$ VOLT3_LL_LSB default value is 00_{HEX} VSEN9-VSEN11 functions are not for W83795ADG, they are reserved registers.							

VOLT4_HL/LL_LSB (LOW BYTE)

BIT	7	6	5	4	3	2	1	0
NAME	VBAT_LSB		3VSB_LSB		3VDD_LSB		VTT_LSB	
	Voltage High / Low Limit (low byte). 10-bit voltage value bit[1:0] VOLT4_HL_LSB default value is FF_{HEX} VOLT4_LL_LSB default value is 00_{HEX}							

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8.10.1.2. Temperature/Voltage Channel Limitation Registers

W83795G/ADG have multi-function pins for temperature and voltage monitoring. It needs set TEMP CRL1 and TEMP CRL2 registers to select temperature or voltage monitoring.

If select temperature monitoring, the effective width of data format is 10-bit 2's complement (9-bit plus sign).

Location:

FOR SELECT TEMPERATURE MONITORING:

TD1/TR1 Critical - Bank 0 Address 96_{HEX}
TD1/TR1 Critical Hystersis - Bank 0 Address 97_{HEX}
TD1/TR1 Warning - Bank 0 Address 98_{HEX}
TD1/TR1 Warning Hystersis - Bank 0 Address 99_{HEX}
TD2/TR2 Critical - Bank 0 Address $9A_{HEX}$
TD2/TR2 Critical Hystersis - Bank 0 Address $9B_{HEX}$
TD2/TR2 Warning - Bank 0 Address $9C_{HEX}$
TD2/TR2 Warning Hystersis - Bank 0 Address $9D_{HEX}$
TD3/TR3 Critical - Bank 0 Address $9E_{HEX}$
TD3/TR3 Critical Hystersis - Bank 0 Address $9F_{HEX}$
TD3/TR3 Warning - Bank 0 Address $A0_{HEX}$
TD3/TR3 Warning Hystersis - Bank 0 Address $A1_{HEX}$
TD4/TR4 Critical - Bank 0 Address $A2_{HEX}$
TD4/TR4 Critical Hystersis - Bank 0 Address $A3_{HEX}$
TD4/TR4 Warning - Bank 0 Address $A4_{HEX}$
TD4/TR4 Warning Hystersis - Bank 0 Address $A5_{HEX}$
TR5 Critical - Bank 0 Address $A6_{HEX}$
TR5 Critical Hystersis - Bank 0 Address $A7_{HEX}$
TR5 Warning - Bank 0 Address $A8_{HEX}$
TR5 Warning Hystersis - Bank 0 Address $A9_{HEX}$
TR6 Critical - Bank 0 Address AA_{HEX}
TR6 Critical Hystersis - Bank 0 Address AB_{HEX}
TR6 Warning - Bank 0 Address AC_{HEX}
TR6 Warning Hystersis - Bank 0 Address AD_{HEX}

Reset: 3VSB Rising.
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

CRITICAL TEMPERATURE

BIT	7	6	5	4	3	2	1	0
NAME	**TD1/TR1, TD2/TR2, TD3/TR3, TD4/TR4, TR5, TR6 Critical** Critical Temperature Value. The format of Temperature is 8-bit 2's complement and the range is –128℃~127℃.							
VALUE	SIGN	64	32	16	8	4	2	1
DEFAULT	64_{HEX} (100℃)							

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CRITICAL TEMPERATURE HYSTERSIS

BIT	7	6	5	4	3	2	1	0
NAME	**TD1/TR1, TD2/TR2, TD3/TR3, TD4/TR4, TR5, TR6 Critical Hystersis** Critical Temperature Hysteresis Value. The format of Temperature is 8-bit 2's complement and the range is –128℃~127℃.							
VALUE	SIGN	64	32	16	8	4	2	1
DEFAULT	$5F_{HEX}$ (95℃)							

WARNING TEMPERATURE

BIT	7	6	5	4	3	2	1	0
NAME	**TD1/TR1, TD2/TR2, TD3/TR3, TD4/TR4, TR5, TR6 Warning** Warning Temperature Value. The format of Temperature is 8-bit 2's complement and the range is –128℃~127℃.							
VALUE	SIGN	64	32	16	8	4	2	1
DEFAULT	55_{HEX} (85 ℃)							

WARNING TEMPERATURE HYSTERSIS

BIT	7	6	5	4	3	2	1	0
NAME	**TD1/TR1, TD2/TR2, TD3/TR3, TD4/TR4, TR5, TR6 Warning Hystersis** Warning Temperature Hysteresis Value. The format of Temperature is 8-bit 2's complement and the range is –128℃~127℃.							
VALUE	SIGN	64	32	16	8	4	2	1
DEFAULT	50_{HEX} (80 ℃)							

FOR SELECT VOLTAGE MONITORING:

VDSEN14_HL - Bank 0 Address 96_{HEX}
VDSEN14_LL - Bank 0 Address 97_{HEX}
VDSEN14_HL_LSB - Bank 0 Address 98_{HEX}
VDSEN14_LL_LSB - Bank 0 Address 99_{HEX}
VDSEN15_HL - Bank 0 Address $9A_{HEX}$
VDSEN15_LL - Bank 0 Address $9B_{HEX}$
VDSEN15_HL_LSB - Bank 0 Address $9C_{HEX}$
VDSEN15_LL_LSB - Bank 0 Address $9D_{HEX}$
VDSEN16_HL - Bank 0 Address $9E_{HEX}$
VDSEN16_LL - Bank 0 Address $9F_{HEX}$
VDSEN16_HL_LSB - Bank 0 Address $A0_{HEX}$
VDSEN16_LL_LSB - Bank 0 Address $A1_{HEX}$

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VDSEN17_HL - Bank 0 Address $A2_{HEX}$
VDSEN17_LL - Bank 0 Address $A3_{HEX}$
VDSEN17_HL_LSB - Bank 0 Address $A4_{HEX}$
VDSEN17_LL_LSB - Bank 0 Address $A5_{HEX}$
VSEN12_HL - Bank 0 Address $A6_{HEX}$
VSEN12_LL - Bank 0 Address $A7_{HEX}$
VSEN12_HL_LSB - Bank 0 Address $A8_{HEX}$
VSEN12_LL_LSB - Bank 0 Address $A9_{HEX}$
VSEN13_HL - Bank 0 Address AA_{HEX}
VSEN13_LL - Bank 0 Address AB_{HEX}
VSEN13_HL_LSB - Bank 0 Address AC_{HEX}
VSEN13_LL_LSB - Bank 0 Address AD_{HEX}

Reset: 3VSB Rising.
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

VDSEN_HL/LL (HIGH BYTE)

BIT	7	6	5	4	3	2	1	0
NAME	**VDSEN14_HL, VDSEN14_LL, VDSEN15_HL, VDSEN15_LL, VDSEN16_HL, VDSEN16_LL, VDSEN17_HL, VDSEN17_LL VSEN12_HL, VSEN12_LL, VSEN13_HL, VSEN13_LL** Voltage High / Low Limit (high byte). The real voltage value calculation is referred to VOLTAGE VALUE CACLULATION description. 10-bit voltage value bit[9:2]							
DEFAULT	VDSEN_HL default Value is 64_{HEX} VDSEN_LL default Value is $5F_{HEX}$							

VDSEN_HL/LL_LSB (LOW BYTE)

BIT	7	6	5	4	3	2	1	0
NAME	**VDSEN_HL/LL_LSB**		**Unused.**					
	VDSEN14_HL_LSB, VDSEN14_LL_LSB, VDSEN15_HL_LSB, VDSEN15_LL_LSB, VDSEN16_HL_LSB, VDSEN16_LL_LSB, VDSEN17_HL_LSB, VDSEN17_LL_LSB VSEN12_HL_LSB, VSEN12_LL_LSB, VSEN13_HL_LSB, VSEN13_LL Voltage High / Low Limit (low byte). 10-bit voltage value bit[1:0]							
DEFAULT	VDSEN_HL_LSB default value is 50_{HEX} VDSEN_LL_LSB default value is 64_{HEX}							

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8.10.1.3. Temperature Channel Limitation Registers

Before W83795G/ADG reads DTS1-DTS8 (Digital Temperature Sensor) temperature from INTEL PECI or AMD SB-TSI, it needs initial relative registers in BANK3. The effective width of Temperature Readout Value (high byte) and VR LSB (low byte) is for temperature data format is 10-bit 2's complement (9-bit plus sign).

Location:

DTS Critical - Bank 0 Address $B2_{HEX}$
DTS Critical Hystersis - Bank 0 Address $B3_{HEX}$
DTS Warning - Bank 0 Address $B4_{HEX}$
DTS Warning Hystersis - Bank 0 Address $B5_{HEX}$

Reset: 3VSB Rising.
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

CRITICAL TEMPERATURE

BIT	7	6	5	4	3	2	1	0
NAME	**DTS Critical** Critical Temperature Value. The format of Temperature is 8-bit 2's complement and the range is –128℃~127℃.							
VALUE	SIGN	64	32	16	8	4	2	1
DEFAULT	64_{HEX} (100℃)							

CRITICAL TEMPERATURE HYSTERSIS

BIT	7	6	5	4	3	2	1	0
NAME	**DTS Critical Hystersis** Critical Temperature Hysteresis Value. The format of Temperature is 8-bit 2's complement and the range is –128℃~127℃.							
VALUE	SIGN	64	32	16	8	4	2	1
DEFAULT	$5F_{HEX}$ (95℃)							

WARNING TEMPERATURE

BIT	7	6	5	4	3	2	1	0
NAME	**DTS Warning** Warning Temperature Value. The format of Temperature is 8-bit 2's complement and the range is –128℃~127℃.							
VALUE	SIGN	64	32	16	8	4	2	1

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DEFAULT	55_{HEX} (85 ℃)

WARNING TEMPERATURE HYSTERSIS

BIT	7	6	5	4	3	2	1	0
NAME	**DTS Warning Hysteresis** Warning Temperature Hysteresis Value. The format of Temperature is 8-bit 2's complement and the range is –128℃~127℃.							
VALUE	SIGN	64	32	16	8	4	2	1
DEFAULT	50_{HEX} (80 ℃)							

8.10.1.4. FANIN Count Limitation Registers

The **FANIN_HL** and **FHL_LSB** are combined to 12-bit FANIN limit. It sets up the limit range for the FANIN count values. If the counter counts value larger than what the registers indicate, the W83795G/ADG will show alert in the real-time status and may take further actions based on user setups.

Location:

FANIN1_HL - Bank 0 Address $B6_{HEX}$
FANIN2_HL - Bank 0 Address $B7_{HEX}$
FANIN3_HL - Bank 0 Address $B8_{HEX}$
FANIN4_HL - Bank 0 Address $B9_{HEX}$
FANIN5_HL - Bank 0 Address BA_{HEX}
FANIN6_HL - Bank 0 Address BB_{HEX}
FANIN7_HL - Bank 0 Address BC_{HEX}
FANIN8_HL - Bank 0 Address BD_{HEX}
FANIN9_HL - Bank 0 Address BE_{HEX}
FANIN10_HL - Bank 0 Address BF_{HEX}
FANIN11_HL - Bank 0 Address $C0_{HEX}$
FANIN12_HL - Bank 0 Address $C1_{HEX}$
FANIN13_HL - Bank 0 Address $C2_{HEX}$
FANIN14_HL - Bank 0 Address $C3_{HEX}$
FHL1_LSB - Bank 0 Address $C4_{HEX}$
FHL2_LSB - Bank 0 Address $C5_{HEX}$
FHL3_LSB - Bank 0 Address $C6_{HEX}$
FHL4_LSB - Bank 0 Address $C7_{HEX}$
FHL5_LSB - Bank 0 Address $C8_{HEX}$
FHL6_LSB - Bank 0 Address $C9_{HEX}$
FHL7_LSB - Bank 0 Address CA_{HEX}

Reset: 3VSB Rising.
Init Reset (CR01.Bit7) is set,

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3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

FANIN1_HL ~ FANIN14_HL

BIT	7	6	5	4	3	2	1	0
NAME	**FANIN1_HL ~ FANIN14_HL** FANIN tachometer count limit (high byte). The real FANIN RPM count limit value calculation is referred to FANIN COUNT CACLULATION description. 12-bitCount Value bit[11:4]							
DEFAULT	FF_{HEX}							

FHL1_LSB

BIT	7	6	5	4	3	2	1	0
NAME	**FANIN2_HL_LSB**				**FANIN1_HL_LSB**			
	FANIN1 and FANIN2 tachometer count limit (lowe byte). 12-bitCount Value bit [3:0]							
DEFAULT	EE_{HEX}							

FHL2_LSB

BIT	7	6	5	4	3	2	1	0
NAME	**FANIN4_HL_LSB**				**FANIN3_HL_LSB**			
	FANIN3 and FANIN4 tachometer count limit (lowe byte). 12-bitCount Value bit [3:0]							
DEFAULT	EE_{HEX}							

FHL3_LSB

BIT	7	6	5	4	3	2	1	0
NAME	**FANIN6_HL_LSB**				**FANIN5_HL_LSB**			
	FANIN5 and FANIN6 tachometer count limit (lowe byte). 12-bitCount Value bit [3:0]							
DEFAULT	EE_{HEX}							

FHL4_LSB

BIT	7	6	5	4	3	2	1	0

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NAME	FANIN8_HL_LSB	FANIN7_HL_LSB
	FANIN7 and FANIN8 tachometer count limit (lowe byte). 12-bitCount Value bit [3:0]	
DEFAULT	EE_{HEX}	

FHL5_LSB

BIT	7	6	5	4	3	2	1	0
NAME	FANIN10_HL_LSB				FANIN9_HL_LSB			
	FANIN9 and FANIN10 tachometer count limit (lowe byte). 12-bitCount Value bit [3:0]							
DEFAULT	EE_{HEX}							

FHL6_LSB

BIT	7	6	5	4	3	2	1	0
NAME	FANIN12_HL_LSB				FANIN11_HL_LSB			
	FANIN11 and FANIN12 tachometer count limit (lowe byte). 12-bitCount Value bit [3:0]							
DEFAULT	EE_{HEX}							

FHL7_LSB

BIT	7	6	5	4	3	2	1	0
NAME	FANIN14_HL_LSB				FANIN13_HL_LSB			
	FANIN13 and FANIN14 tachometer count limit (lowe byte). 12-bitCount Value bit [3:0]							
DEFAULT	EE_{HEX}							

8.11 Temperature Sensors Offset Registers

8.11.1.1. Temperature Offset Register

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Each temperature channel has a corresponding offset register. In some situations, the customer may want to shift the offset. The default is 00_{HEX}.

Location:

TD1 Offset - Bank 0 Address $D0_{HEX}$
TD2 Offset - Bank 0 Address $D1_{HEX}$
TD3 Offset - Bank 0 Address $D2_{HEX}$
TD4 Offset - Bank 0 Address $D3_{HEX}$
TR5/6 Offset - Bank 0 Address $D4_{HEX}$

Reset: 3VSB Rising.
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

TD1-TD4 OFFSET TEMPERATURE

BIT	7	6	5	4	3	2	1	0
NAME	**TD1, TD2, TD3, TD4 Offset** Offset Temperature Value. The format of Temperature is 6-bit 2's complement and the range is –32℃~31℃.							
VALUE	Reserved		SIGN	16	8	4	2	1
DEFAULT	00_{HEX} (0℃)							

TR1/2 OFFSET TEMPERATURE

BIT	7	6	5	4	3	2	1	0
NAME	**TR6 Offset**				**TR5 Offset**			
	Offset Temperature Value. The format of Temperature is 4-bit 2's complement and the range is –8℃~7℃.							
VALUE	SIGN	4	2	1	SIGN	4	2	1
DEFAULT	00_{HEX} (0℃)							

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9. REGISTER SUMMARY – BANK1

NNEMONIC	ADD (Hex)	POR (Hex)	TYPE	Description
UDIDDDevCap	20	C1	RO	UDID Device Capability.
UDIDVersion	21	08	RO	UDID Version Number
UDIDVendor	22/23	10/50	RO	UDID Vendor ID
UDIDDev	24/25	79/5A	RW	UDID Device ID
UDIDIF	26/27	00/24	RW	UDID Interface
UDIDSubVen	28/29	00/00	RW	UDID Subsystem Vendor ID
UDIDSubDev	2A/2B	00/00	RW	UDID Subsystem Device ID
UDIDSpecID	2C-2F	*	RW	UDID Vendor-Specific ID
RNG	30-33	*	RO	Random Number Generator
ASFAdd	3F	00	RO	ASF Assigned Address
ENTY	40-72	*	RW	ASF Entity
ENTINS	80-A3	*	RW	ASF Entity Instance
PwrOnOption	B0	00	RW	Power On Control Option
PwrOnCmd	B1	11	RW	Power On Command
PwrDnCmd	B2	12	RW	Power Down Command
RstCmd	B3	10	RW	Remote Reset Command
ASFTM	B4	FF	WO	ASF Test Mode

*: See registers description

9.1 ASF Control Registers

ASF or Alert Standard Format provides remote system abilities to monitor, discover and manage the local platform. All ASF control registers are located in Bank 1*.

*About the Bank Selection, please refer to the Bank Select register located at address $00_{Hex.}$

9.1.1.1. SMBus ARP UDID Control Registers

Before activating ASF, the user must go through the ARP (Address Resolution Protocol) to dynamically obtain a valid address to manipulate ASF commands. In ARP, it is very important that UDID (Unique Device Identifier) is defined to distinguish different devices. Registers in this section are used to set up UDID.

For detailed operation of ARP and UDID, please refer to SMBus Specification version 2.0 (http://www.smbus.org/specs/smbus20.pdf) section 5.6 in page 34.

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9.1.1.2. ASF Sensor Entity Definition Registers

In ASF Sensor, each sensor channel has 2 parameters, entity Instance and entity ID, to tell the ASF host its related location information on the platform. If the user uses the temperature sensor in locations different from the default, the W83795G/ADG provides all channel parameters that can be programmed to fit customers' application.

For details of entity ID, please refer to Platform Event Trap Format Specification Version 1.0 Table 6 in page 13.

Entity Instance is a sequential number which helps identify the sensor's location. The customer can set preferable sequence orders.

The summary of Entity and Entity Instance is in the following table.

Note that all channels can be disabled by multi-function pin selection or control registers.

VSEN9-VSEN11 functions are not for W83795ADG, they are reserved registers.

Sensor in W83795G/ADG	Event Status Index	Event Sensor Type	Event Number	Entity ID (Programmable)	Entity Instance (Programmable)
VSEN1	00h	02h (Voltage)	01h	03h (Processor)	01h
VSEN2	01h		02h		02h
VTT	02h		03h		03h
DTS1	03h	01h (Temperature)	04h		01h
DTS2	04h		05h		02h
DTS3	05h		06h		03h
DTS4	06h		07h		04h
DTS5	07h		08h		05h
DTS6	08h		09h		06h
DTS7	09h		0Ah		07h
DTS8	0Ah		0Bh		08h
TD1/TR1	0Bh	01h (Temperature)	0Ch	07h (System Board)	01h
TD2/TR2	0Ch		0Dh		02h
TD3/TR3	0Dh		0Eh		03h
TD4/TR4	0Eh		0Fh		04h
TR5	0Fh		10h		05h
TR6	10h		11h		06h
Reserved	11h		12h		07h
3VDD	12h	02h (Voltage)	13h		01h
3VSB	13h		14h		02h
VBAT	14h		15h		03h
VSEN3	15h		16h		04h
VSEN4	16h		17h		05h

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Sensor in W83795G/ADG	Event Status Index	Event Sensor Type	Event Number	Entity ID (Programmable)	Entity Instance (Programmable)
VSEN5	17h		18h		06h
VSEN6	18h		19h		07h
VSEN7	19h		1Ah		08h
VSEN8	1Ah		1Bh		09h
VSEN9	1Bh		1Ch		0Ah
VSEN10	1Ch		1Dh		0Bh
VSEN11	1Dh		1Eh		0Ch
VSEN12	1Eh		1Fh		0Dh
VSEN13	1Fh		20h		0Eh
VDSEN14	20h		21h		0Fh
VDSEN15	21h		22h		10h
VDSEN16	22h		23h		11h
VDSEN17	23h		24h		12h
FANIN1	24h	04h (Fan)	25h		01h
FANIN2	25h		26h		02h
FANIN3	26h		27h		03h
FANIN4	27h		28h		04h
FANIN5	28h		29h		05h
FANIN6	29h		2Ah		06h
FANIN7	2Ah		2Bh		07h
FANIN8	2Bh		2Ch		08h
FANIN9	2Ch		2Dh		09h
FANIN10	2Dh		2Eh		0Ah
FANIN11	2Eh		2Fh		0Bh
FANIN12	2Fh		30h		0Ch
FANIN13	30h		31h		0Dh
FANIN14	31h		32h		0Eh
Case OPEN / Intrusion	32h	05h (Physical Security)	33h	23h (System Chassis)	01h

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The channels in light-green can be disabled by multi-function pin selection or control registers. The channels are described in the following terms according to the status of each channel.

Description	Status	Event Sensor Type	Event Type	Event Offset	Event Severity
TEMPERATURE SENSORS					
Upper-Critical Going High	3h Assert	01h Temperature	01h Threshold-Based	09h	10h Critical
Upper-Critical Going Low				08h	
Upper-Non-critical Going High				07h	08h Non-critical
Upper-Non-critical Going Low				06h	
Lower-Non-critical Going High	2h Deassert			01h	01h Monitor
Lower-Non-critical Going Low				00h	
VOLTAGE SENSORS					
Generic Over Voltage Problem	3h	02h Voltage	07h Generic-Severity	02h	10h
Normal Voltage	2h			07h	01h
Generic Under Voltage Problem	3h			02h	10h
FAN SENSORS					
Normal FAN Speed	2h	04h Fan	07h	07h	01h
Generic FAN Failure	3h			02h	10h
CASEOPEN/ CASE INTRUSION					
Case Intruded	3h	05h Physical Security	6Fh Sensor Specific	00h	10h
Case Normal	2h			80h	01h

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9.1.1.3. ASF Remote Control Definition Registers

ASF function in the W83795G/ADG also supports Remote Control. This function enables Management Information System (MIS) to remotely power on, power down, or reset the client's computer when there is abnormal operation.

The Remote Control function in the W83795G/ADG enables MIS to use side-band of Network Interface Controller to send ASF commands with SMBus. The format looks like

1	7	1	1	8	1	8	1	8	1	1
S	Slave Address	Wr	A	Command	A	Write Data	A	PEC	A	P
	Control Device Address	0	0	Control Command	0	Control Data Value	0	CRC Checksum	0	

"S" represents "Start" Cycle of SMBus transaction; "Wr" means "Write" Flag; "A" means "Acknowledge" from the W83795G/ADG, and "P" indicates a "Stop" Cycle. Letters in shadow mean responses from the W83795G/ADG. Otherwise, it is a host transmitted signal.

The last row above shows the meaning of each data. Control Device Address is the address assigned in the ARP process; Control Command is specified in the above registers. Control Data option is not supported in the W83795G/ADG. Thus with any value in this field, the W83795G/ADG will perform the same action.

Please refer to Section 5.4 in page 76 and Section 3.2.4.1 in page 33 in Alert Standard Format Specification v2.0 for more details.

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9.1.2 ASF Register Details

9.1.2.1. UDID Device Capability Register (UDIDDDevCap)

SMBus Specification Working Group intends to use device capability to distinguish the arbitration priority of GeneralGetUDID() first. Thus the very first byte of the UDID is device capability, because SMBus is a MSB first serial protocol and if the client was pulled low, it wins the arbitration. It is set as $C1_{HEX}$.

Location: **UDIDDDevCap** - Bank 1 Address 20_{HEX}

Type: Read Only
Reset: No Reset.
Default Value: $C1_{HEX}$

BIT	DESCRIPTION
7-6	**Address Type.** 00_{BIN} = Fixed address device. It's the highest priority device. 01_{BIN} = Dynamic and persistent address device. 10_{BIN} = Dynamic and volatile address device. If powered-down, the address needs to be reassigned at next power on. The W83795G/ADG ASF address will be lost if 3VSB does not exist. 11_{BIN} = Random number device. (Default)
5-1	**Reserved.**
0	**PEC** – PEC Support 0 = PEC (Packet Error Code) is not supported on this device. 1 = PEC is supported on this device.

9.1.2.2. UDID Version Number Register (UDIDVersion)

This field defines the version of UDID and Silicon for the W83795G/ADG. The default is $08_{HEX.}$

Location: **UDIDVersion** - Bank 1 Address 21_{HEX}
Type: Read Only
Reset: No Reset
Default Value: 08_{HEX}

BIT	DESCRIPTION
7-6	**Reserved.**
5-3	**UDID Version.** 000_{BIN} = Reserved. 001_{BIN} = UDID version 1. (Default) 010_{BIN}-111_{BIN} = Reserved for future use.
2-0	**Silicon Version.** For the identification of the W83795G/ADG silicon version. 000_{BIN} stands for Version A/B.

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9.1.2.3. UDID Vendor ID High/Low Byte Register (UDIDVendor)

This field defines Nuvoton vendor ID. The default is $1050_{HEX.}$

Location: **UDIDVendorH** - Bank 1 Address 22_{HEX}
UDIDVendorL - Bank 1 Address 23_{HEX}
Type: Read Only
Reset: No Reset

UDIDVendorH

BIT	7	6	5	4	3	2	1	0
NAME	Vendor ID High Byte							
VALUE	0	0	0	1	0	0	0	0

UDIDVendorL

BIT	7	6	5	4	3	2	1	0
NAME	Vendor ID Low Byte							
VALUE	0	1	0	1	0	0	0	0

9.1.2.4. UDID Device ID High/Low Byte Register (UDIDDev)

This field defines Nuvoton device ID. The default is $795A_{HEX.}$

Location:
UDIDDevH - Bank 1 Address 24_{HEX}
UDIDDevL - Bank 1 Address 25_{HEX}
Type: Read / Write
Reset: 3VSB Rising.
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

UDIDDevH

BIT	7	6	5	4	3	2	1	0
NAME	Device ID High Byte							
VALUE	0	1	1	1	1	0	0	1

UDIDDevL

BIT	7	6	5	4	3	2	1	0
NAME	Device ID Low Byte							
VALUE	0	1	0	1	1	0	1	0

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9.1.2.5. UDID Interface High/Low Byte Register (UDIDIF)

This field defines SMBus version and the supported protocol. It is reset to $0024_{HEX.}$

Location:

UDIDIFH - Bank 1 Address 26_{HEX}

UDIDIFL - Bank 1 Address 27_{HEX}

Type: Read Write

Reset: 3VSB Rising.
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

UDIDIFH

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							
VALUE	0	0	0	0	0	0	0	0

UDIDIFL

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	IPMI	ASF	OEM	SMBus Version			
VALUE	0	0	1	0	0	1	0	0

BIT	DESCRIPTION
15-7	**Reserved.**
6	**IPMI.** This device supports additional interface access capability per IPMI specification. 0 = Not supported. (Default) 1 = Supported.
5	**ASF**. This device supports additional interface access capability per ASF specification. 0 = Not supported. 1 = Supported. (Default)
4	**OEM**. Device supports vendor specific access capability per Subsystem Vendor ID and Subsystem Device ID. 0 = Not supported. (Default) 1 = Supported.
3-0	**SMBus Version.** 0_{HEX} = SMBus 1.0, not ARP available. 1_{HEX} = SMBus 1.1, not ARP available. 4_{HEX} = SMBus 2.0. (Default)

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9.1.2.6. UDID Subsystem Vendor ID High/Low Byte Register (UDIDSubVen)

This field defines UDID support for Subsystems. If no subsystem is supported, it must be written with 0000_{HEX}. It is reset to $0000_{HEX.}$

Location: **UDIDSubVenH** - Bank 1 Address 28_{HEX}
UDIDSubVenL - Bank 1 Address 29_{HEX}
Type: Read / Write
Reset: 3VSB Rising.
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

UDIDSubVenH

BIT	7	6	5	4	3	2	1	0
NAME	UDID Subsystem Vendor ID High Byte							
VALUE	0	0	0	0	0	0	0	0

UDIDSubVenL

BIT	7	6	5	4	3	2	1	0
NAME	UDID Subsystem Vendor ID Low Byte							
VALUE	0	0	0	0	0	0	0	0

9.1.2.7. UDID Subsystem Device ID High/Low Byte Register (UDIDSubDev)

This field defines UDID support for Subsystems. If no subsystem is supported, it must be written with 0000_{HEX}. It is reset to $0000_{HEX.}$

Location: **UDIDSubDevH** - Bank 1 Address $2A_{HEX}$
UDIDSubDevL - Bank 1 Address $2B_{HEX}$
Type: Read / Write
Reset: 3VSB Rising.
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

UDIDSubDevH

BIT	7	6	5	4	3	2	1	0
NAME	UDID Subsystem Device ID High Byte							
VALUE	0	0	0	0	0	0	0	0

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UDIDSubDevL

BIT	7	6	5	4	3	2	1	0
NAME	UDID Subsystem Device ID Low Byte							
VALUE	0	0	0	0	0	0	0	0

9.1.2.8. UDID Vendor-Specific ID Register (UDIDSpecID)

This field defines unique Vendor-Specific ID for different versions of the W83795G/ADG. With this field, different W83795G/ADG will be identified on the same SMBus interface. This register will be loaded with a random number when receiving the reset signal.

Location:
UDIDSpecID4 - Bank 1 Address $2C_{HEX}$
UDIDSpecID3 - Bank 1 Address $2D_{HEX}$
UDIDSpecID2 - Bank 1 Address $2E_{HEX}$
UDIDSpecID1 - Bank 1 Address $2F_{HEX}$
Type: Read Write
Reset: 3VSB Rising.
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.
ARP ResetDevice Command.

UDIDSpecID4 – UDIDSpecID1

BIT	7	6	5	4	3	2	1	0
NAME	UDID Specific Vendor ID							
VALUE	default value is load from RNG							

9.1.2.9. Random Number Generator Register (RNG)

The W83795G/ADG internally generates pseudo random numbers by using CRC generator and internal clock. Due to the deviations of the internal clock, different IC and different power-on time will affect the results of the random numbers. It is reset to $FFFF_{HEX.}$

Location:
RNG4 - Bank 1 Address 30_{HEX}
RNG3 - Bank 1 Address 31_{HEX}

RNG2 - Bank 1 Address 32_{HEX}
RNG1 - Bank 1 Address 33_{HEX}
Type: Read Only
Reset: None.

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RNG4 – RNG1

BIT	7	6	5	4	3	2	1	0
NAME	**Random Number Code**							
VALUE	random number							

9.1.2.10. ASF Assigned Address Register (ASFAdd)

After the ARP host obtains related device UDID, it will start to assign each device for later use. The W83795G/ADG will record this assigned address and set it as the default address for ASF transactions. It is reset to $00_{HEX.}$

Location: **ASFAdd** - Bank 1 Address $3F_{HEX}$
Type: Read Only
Reset: 3VSB Rising,
Init Reset (CR01.Bit7) is set.

ASFAdd

BIT	7	6	5	4	3	2	1	0
NAME	**ASF Address** This register will be assigned while ARP AssignAddress command issued.							
VALUE	0	0	0	0	0	0	0	0

9.1.2.11. ASF Entity/Instance Registers (ENTY/ENTINS)

The W83795G/ADG supports various channels which can be reported to the host through ASF protocol. Each sensor channel is associated with an entity (or location on the motherboard) and entity instance. The Table provides an overall look for these registers. The registers are located in Bank 1*.

*About the Bank Selection, please refer to the Bank Select register located at address $00_{Hex.}$

Type: Read / Write
Reset: 3VSB Rising.
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

Entity Registers: Entity of each sensor channel. For other entity types, please refer to PET Spec.
03_{HEX}: Processor
07_{HEX}: System Board.
23_{HEX}: Chassis Back Panel Board.

NNEMONIC	ADD (Hex)	VALUE (Hex)	DESCRIPTION
VSEN1_ENTY	40	03	VSEN1 Entity ID
VSEN2_ENTY	41	03	VSEN2 Entity ID
VSEN3_ENTY -	42-4C	07	VSEN3 - VSEN13 Entity ID

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NNEMONIC	ADD (Hex)	VALUE (Hex)	DESCRIPTION
VSEN13_ENTY			
VDSEN14_ENTY - VDSEN17_ENTY	4D-50	07	VDSEN14 - VDSEN17 Entity ID
VTT_ENTY	51	03	VTT Entity ID
3VDD_ENTY	52	07	3VDD Entity ID
3VSB_ENTY	53	07	3VDD Entity ID
VBAT	54	07	VBAT Entity ID
FANIN1_ENTY - FANIN14_ENTY	55-62	07	FANIN1 – FANIN14 Entity ID
TD1_ENTY - TD4_ENTY	63-66	07	TD1 – TD4 Entity ID
TR1_ENTY - TR2_ENTY	67-68	07	TR1 – TR2 Entity ID
DTS1_ENTY - DTS8_ENTY	69-70	03	DTS1 – DTS8 Entity ID
Reserved	71		
CHS_ENTY	72	23	Chassis Entity ID

Entity Instance Registers:

NNEMONIC	ADD (Hex)	VALUE (Hex)	DESCRIPTION
VSEN1_ ENTINS	80	01	Bit[4:0] is VSEN1 Entity instance
VSEN2_ ENTINS	81	02	Bit[4:0] is VSEN2 Entity instance
VSEN3_ ENTINS - VSEN13_ENTINS	82-8C	04-0E	Bit[4:0] is VSEN3 – VSEN13 Entity instance VSEN9-VSEN11 Entity functions are not for W83795ADG.
VDSEN14_ ENTINS - VDSEN17_ ENTINS	8D-90	0F-12	Bit[4:0] is VDSEN14 – VDSEN17 Entity instance
VTT_ ENTINS	91	03	Bit[4:0] is VTT Entity instance
3VDD_ ENTINS	92	01	Bit[4:0] is 3VDD Entity instance
3VSB_ ENTINS	93	02	Bit[4:0] is 3VSB Entity instance
VBAT_ ENTINS	94	03	Bit[4:0] is VBAT Entity instance
FANIN1_ENTINS - FANIN2_ENTINS	95	21	Bit[7:4] is FANIN2 Entity instance. Bit[3:0] is FANIN1 Entity instance.
FANIN3_ENTINS - FANIN4_ENTINS	96	43	Bit[7:4] is FANIN4 Entity instance. Bit[3:0] is FANIN3 Entity instance.

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NNEMONIC	ADD (Hex)	VALUE (Hex)	DESCRIPTION
FANIN5_ENTINS - FANIN6_ENTINS	97	65	Bit[7:4] is FANIN6 Entity instance. Bit[3:0] is FANIN5 Entity instance.
FANIN7_ENTINS - FANIN8_ENTINS	98	87	Bit[7:4] is FANIN8 Entity instance. Bit[3:0] is FANIN7 Entity instance.
FANIN9_ENTINS - FANIN10_ENTINS	99	A9	Bit[7:4] is FANIN10 Entity instance. Bit[3:0] is FANIN9 Entity instance.
FANIN11_ENTINS - FANIN12_ENTINS	9A	CB	Bit[7:4] is FANIN12 Entity instance. Bit[3:0] is FANIN11 Entity instance.
FANIN13_ENTINS - FANIN14_ENTINS	9B	ED	Bit[7:4] is FANIN14 Entity instance. Bit[3:0] is FANIN13 Entity instance.
TD1_ENTINS - TD2_ENTINS	9C	21	Bit[7:4] is TD2 Entity instance. Bit[3:0] is TD1 Entity instance.
TD3_ENTINS - TD4_ENTINS	9D	43	Bit[7:4] is TD4 Entity instance. Bit[3:0] is TD3 Entity instance.
TR1_ENTINS - TR2_ENTINS	9E	65	Bit[7:4] is TR2 Entity instance. Bit[3:0] is TR1 Entity instance.
DTS1_ENTINS - DTS2_ENTINS	9F	21	Bit[7:4] is DTS2 Entity instance. Bit[3:0] is DTS1 Entity instance.
DTS3_ENTINS - DTS4_ENTINS	A0	43	Bit[7:4] is DTS4 Entity instance. Bit[3:0] is DTS3 Entity instance.
DTS5_ENTINS - DTS6_ENTINS	A1	65	Bit[7:4] is DTS6 Entity instance. Bit[3:0] is DTS5 Entity instance.
DTS7_ENTINS - DTS8_ENTINS	A2	87	Bit[7:4] is DTS8 Entity instance. Bit[3:0] is DTS7 Entity instance.
CHS_ENTY	A3	17	Bit[7:4] is Chassis Entity instance. Bit[3:0] is Reserved.

9.1.2.12. Power on Control Option Register (PwrOnOption)

The W83795G/ADG supports 2 ways to power the system. One is to power the system only one time, no matter 3VDD rises or not. The other is the W83795G/ADG continues to issues power-on cycles until it detects 3VDD is already powered on.

Location: **PwrOnOption** - Bank 1 Address $B0_{HEX}$
Type: Read / Write
Reset: 3VSB Rising.
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

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PwrOnOption

BIT	7	6	5	4	3	2	1	0
NAME	Nuvoton Test Modes							PWR1T
VALUE	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**Nuvoton Test Modes.** Test modes for production. Nuvoton strongly suggests the customer not use these registers to avoid system malfunction.
0	**PWR1T** – Power on One Time. 0 = Continues to issue power-on cycles, PWRBTN# assert 0.1sec every 1sec until 3VDD is powered-on.

9.1.2.13. Power on Command Register (PwrOnCmd)

ASF Remote Control Command supports Remote Power on features. Here defines the Power on commands supported by the W83795G/ADG.

Location: **PwrOnCmd** - Bank 1 Address $B1_{HEX}$
Type: Read / Write
Reset: 3VSB Rising.
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

PwrOnCmd

BIT	7	6	5	4	3	2	1	0
NAME	Remote Power On Command							
VALUE	11_{HEX}							

9.1.2.14. Power down Command Register (PwrDnCmd)

ASF Remote Control Command supports Remote Power Down features. Here defines the Power off commands supported by the W83795G/ADG.

Location: **PwrDnCmd** - Bank 1 Address $B2_{HEX}$
Type: Read / Write
Reset: 3VSB Rising.
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

PwrOffCmd

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Bit	7	6	5	4	3	2	1	0
Name	**Remote Power Down Command**							
Reset	12_{HEX}							

9.1.2.15. Remote Reset Command Register (RstCmd)

ASF Remote Control Command supports Remote Reset features. Here defines the Reset commands supported by the W83795G/ADG.

Location: **RstCmd** - Bank 1 Address $B3_{HEX}$
Type: Read / Write
Reset: 3VSB Rising.
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

RstCmd

Bit	7	6	5	4	3	2	1	0
Name	**Remote Reset Command**							
Reset	10_{HEX}							

9.1.2.16. ASF Test Mode (ASFTM)

Location: **ASFTM** - Bank 1 Address $B4_{HEX}$
Type: Write Only
Reset: 3VSB Rising.
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

ASFTM

Bit	7	6	5	4	3	2	1	0
Name	**ASFTM -** ASF Test Mode Test modes for production. Nuvoton strongly suggests the customer not use these registers to avoid system malfunction.							
Reset	FF_{HEX}							

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10. REGISTER SUMMARY – BANK2

NNEMONIC	ADD (Hex)	POR (Hex)	TYPE	Description
FCMS	01/08	00/00	RW	Fan Control Mode Selection
TFMR	02-07	00	RW	Temperature to Fan mapping Relationships
TSS	09-0B	00	RW	Temperature Source Selection
DFSP	0C	4D	RW	Default Fan Speed at Power-on
SFOSUT	0D	80	RW	SmartFan Output Step Up Time
SFOSDT	0E	80	RW	SmartFan Output Step Down Time
FOMC	0F	*	RW	Fan Output Mode Control
FOV	10-17	4D	RW or RO	Fan Output Value
FOPFP	18-1F	84	RW	Fan Output PWM Frequency Prescalar
FOSV	20-27	30	RW	Fan Output Start-up Value
FONV	28-2F	10	RW	Fan Output Nonstop Value
FOST	30-37	FF	RW	Fan Output Stop Time
FOPPC	38	FF	RW	Fan Output PWM Polarity Control
FTS	40-4F	*	RW	FANIN Target Speed
TFTS	50	10	RW	Tolerance of FANIN Target Speed
TTTI	60-65	28	RW	Target Temperature of Temperature Inputs
CTFS	68-6D	50	RW	Critical Temperature to Full Speed all fan
HT	70-75	53	RW	Hystersis of Temperature
SFIV	80-DE	*	RW	SMART FAN^{TM} IV Temperature and DC/PWM Registers
CRPE	E0/E1	00	RW	Configure Register of PECI Error
FOMV	E2-E9	80	RW	Fan Output Min Value when PECI Error

*: See registers description

10.1.1.1. Smart Fan Setup/Status registers

In SmartFan Mode, a specific temperature will be defined in **Critical Temperature to Full Speed all fan (CTFS)** Bank2 Address 68_{HEX} – $6D_{HEX.}$ If any temperature input detected is higher than this, all fans will operate at full speed simultaneously. The definitions of the control parameters in normal use are shown in the following graph.

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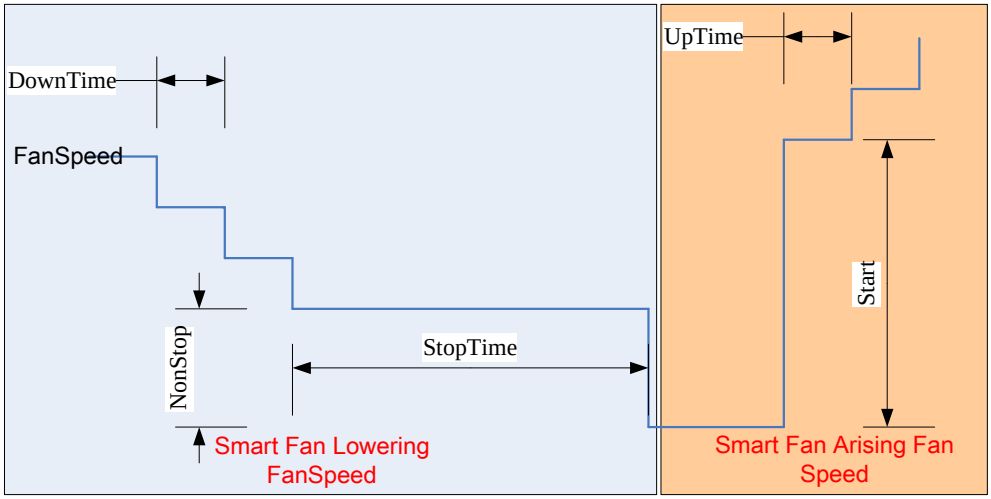


Smart Fan Control Parameters Figure

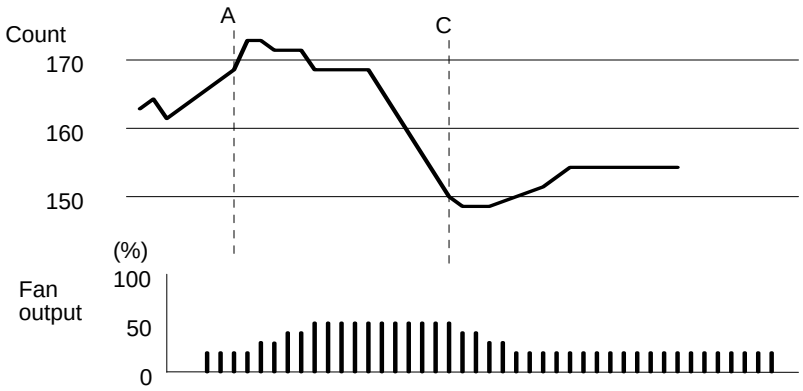
10.1.1.2. Speed Cruise Mode

Eight pairs of fan input sensors (FANIN8-FANIN1) and fan outputs (FANCTL8-FANCTL1) in Fan Speed Cruise mode. FANCTL8-FANCTL1 and FANIN8-FANIN1 mapping are one-by-one relationship. FANCTL8 is applies to FANIN8. FANCTL7 is applies to FANIN7…etc.

FANCTL3-FANCTL8 functions are not for W83795ADG.

- Set the fan output (FANCTL1 – FANCTL8) controlled mode by **Fan Control Mode Selection Registers (FCMS)** Bank2 Address 01_{HEX} and 08_{HEX}
- Set **FANIN Target Speed (FTS)** Bank2 Address 40_{HEX} – $4F_{HEX}$
- Set **Tolerance of FANIN Target Speed (TFTS)** Bank2 Address 50_{HEX}

Fan Speed Cruise mode keeps the fan speed in a specified range. First, this range is defined in BIOS by a fan speed count (the amount of time between clock input signals, not the number of clock input signals in a period of time) and an interval (e.g., 160 ± 10). As long as the fan speed count is in the specified range, fan output remains the same. If the fan speed count is higher than the high end (e.g., 170), fan output increases to make the count lower. If the fan speed count is lower than the low end (e.g., 150), fan output decreases to make the count higher. One example is illustrated in this figure.



Mechanism of Fan Speed Cruise™ Mode

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10.1.1.3. Thermal Cruise Mode

Thermal Cruise mode is an algorithm to control the fan speed to keep the temperature source around the **TTTI** (Target Temperature of Temperature Inputs). If the temperature source detects temperatures higher or lower than the target temperatures with **HT** (Hystersis of Temperature), Smart Fan Control will take actions to speed up or slow down the fan to keep the temperature within the tolerance range.

FANCTL3-FANCTL8 functions are not for W83795ADG.

- The temperature sensor selected by **Temperature Source Selection Register (TSS)** Bank 2 Address 09_{HEX} – $0B_{HEX}$
- The fan output (FANCTL1 – FANCTL8) selected by **Temperature to Fan mapping Relationships Register (TFMR)** Bank2 Address 09_{HEX} – $0B_{HEX}$
- Set the fan output (FANCTL1 – FANCTL8) controlled mode by **Fan Control Mode Selection Registers (FCMS)** Bank2 Address 01_{HEX} and 08_{HEX}
- Set **Critical Temperature to Full Speed all fan (CTFS)** Bank2 Address 68_{HEX} – $6D_{HEX}$
- Set **Target Temperature of Temperature Inputs (TTTI)** Bank2 Address 60_{HEX} – 65_{HEX}
- Set **Hystersis of Temperature (HT)** Bank2 Address 70_{HEX} – 75_{HEX}

Thermal Cruise mode controls the fan speed to keep the temperature in a specified range. First, this range is defined in BIOS by a temperature and the interval (e.g., 55 °C ± 3 °C). As long as the current temperature remains below the low end of this range (i.e., 52 °C), the fan is off. Once the temperature exceeds the low end, the fan turns on at a speed defined in BIOS (e.g., 20% output). Thermal Cruise mode then controls the fan output according to the current temperature. Three conditions may occur:

(1) If the temperature still exceeds the high end, fan output increases slowly. If the fan is operating at full speed but the temperature still exceeds the high end, a warning message is issued to protect the system.

(2) If the temperature falls below the high end (e.g., 58°C) but remains above the low end (e.g., 52 °C), fan output remains the same.

(3) If the temperature falls below the low end (e.g., 52 °C), fan output decreases slowly to zero or to a specified “stop value”. This stop value is enabled by Bank0 Index12h, bits 3 ~ 5, and the value itself is specified in Bank0 Index08h, Index09h, Index15h and Index 64h. The fan remains at the stop value for the period of time defined in Bank0 Index0Ch, Index0Dh, Index17h and Index 66h.

In general, Thermal Cruise mode means

- if the current temperature is higher than the high end, increase the fan speed;
- if the current temperature is lower than the low end, decrease the fan speed;
- otherwise, keep the fan speed the same.

The following figures illustrate two examples of Thermal Cruise mode.

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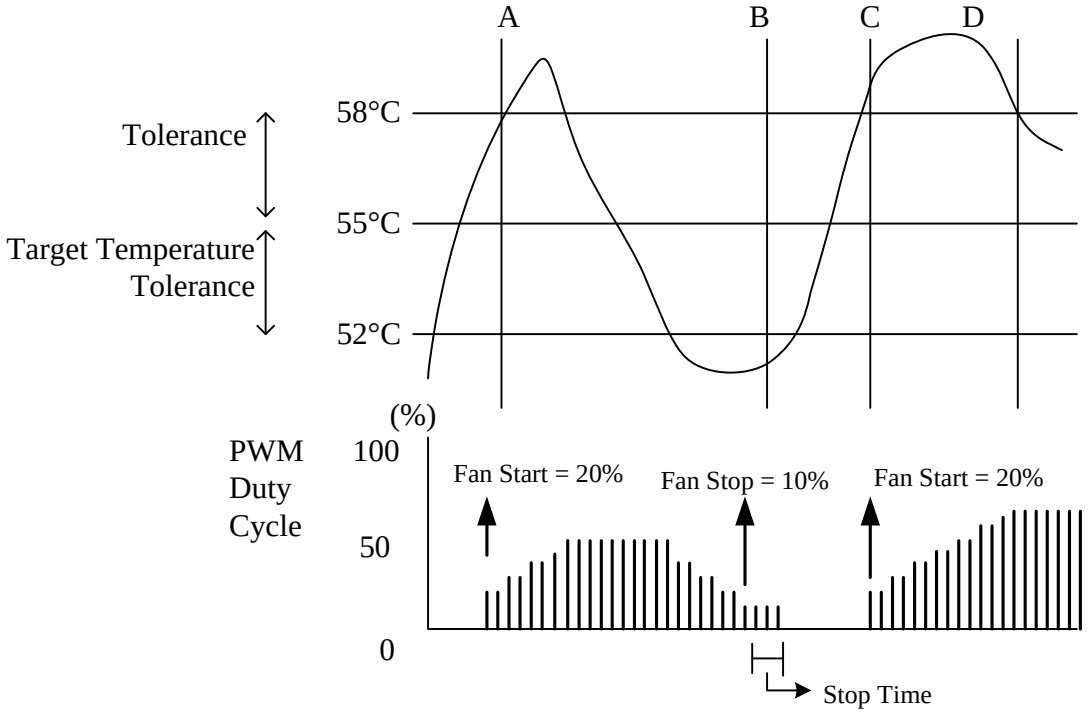

Figure 10-1 Mechanism of Thermal Cruise™ Mode (PWN Duty Cycle)

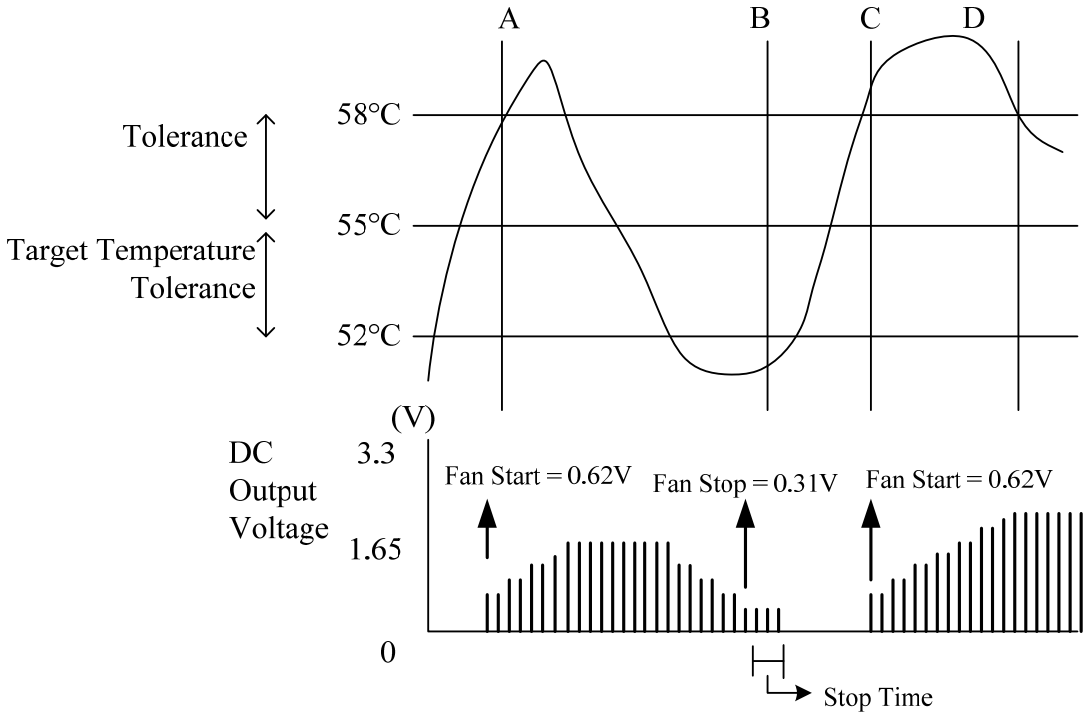

Figure 10-2 Mechanism of Thermal Cruise™ Mode (DC Output Voltage)

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10.1.1.4. SMART FAN™ IV

SMART FAN™ IV offers 6 slopes to control the fan speed. There are eight fan outputs and six temperature sensors in SMART FAN™ IV mode.

FANCTL3-FANCTL8 functions are not for W83795ADG.

- The temperature sensor selected by **Temperature Source Selection Register (TSS)** Bank 2 Address 09_{HEX} – $0B_{HEX}$
- The fan output (FANCTL1 – FANCTL8) selected by **Temperature to Fan mapping Relationships Register (TFMR)** Bank2 Address 09_{HEX} – $0B_{HEX}$
- Set the fan output (FANCTL1 – FANCTL8) controlled mode by **Fan Control Mode Selection Registers (FCMS)** Bank2 Address 01_{HEX} and 08_{HEX}
- Set **Critical Temperature to Full Speed all fan (CTFS)** Bank2 Address 68_{HEX} – $6D_{HEX}$
- Set the **Relative Register-at SMART FAN™ IV Control Mode Table**
- Set **Hystersis of Temperature (HT)** Bank2 Address 70_{HEX} – 75_{HEX}

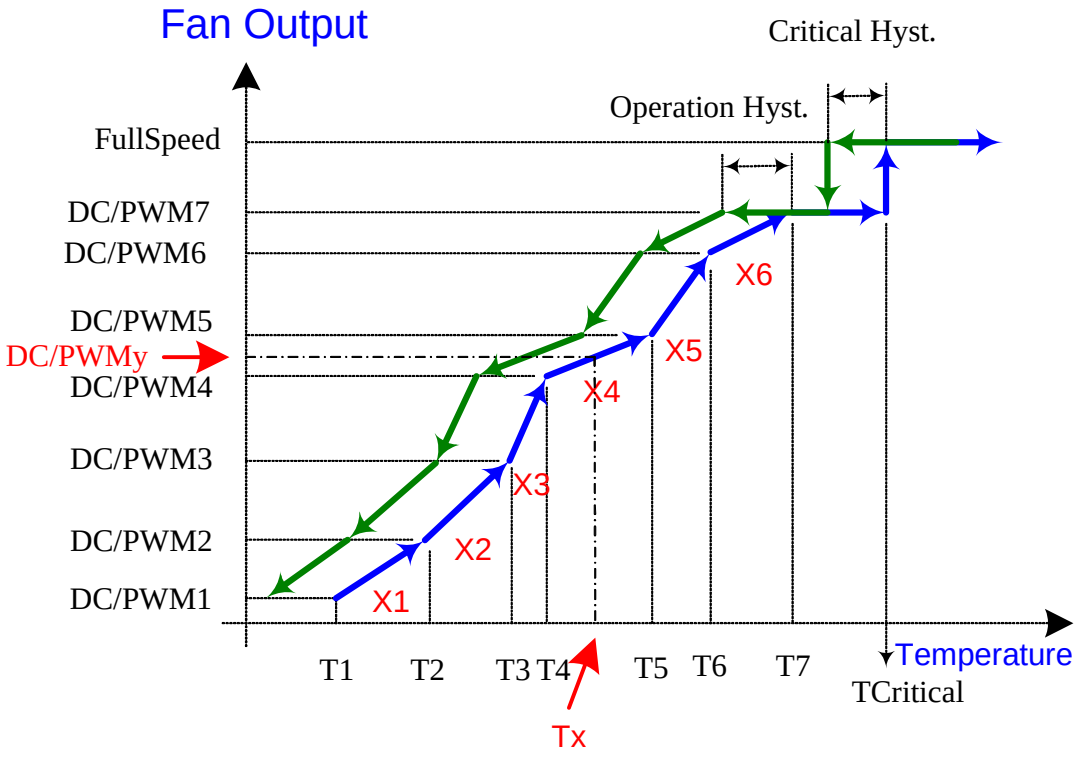
The 6 slopes can be obtained by setting DC/PWM1~DC/PWM7 and T1~T7 through the registers. When the temperature rises, FAN Output will calculate the DC/PWM output based on the current slope. For example, in the following figure, T1~T7 are the temperature set and DC/PWM1 ~ DC/PWM7 are the fan output set. Assume Tx is the current temperature and DC/PWMy is the fan output, then

The slope:

$$X4 = \frac{(DC/PWM5) - (DC/PWM4)}{(T5 - T4)}$$

Fan Output:

$$DC/PWMy = (DC/PWM4) + (Tx - T4) \cdot X4$$



SMART FAN™ IV Mechanism

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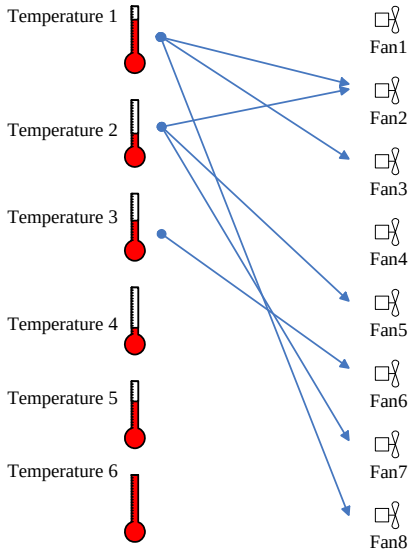
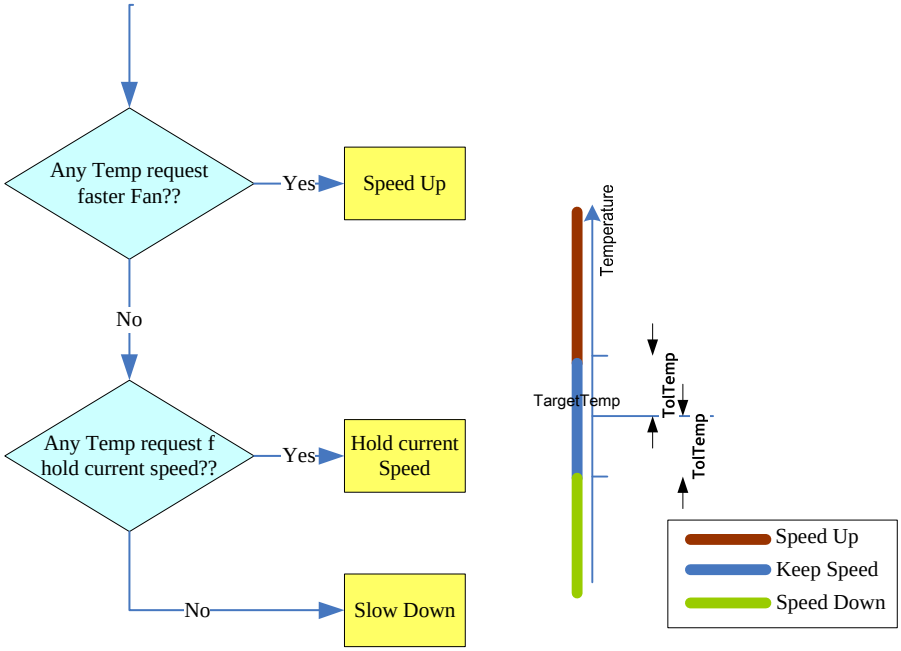
In addition, SMART FAN™ IV can also set up Critical Temperature and Hysteresis. If the current temperature exceeds Critical Temperature, Fan Output outputs DC/PWM7 value, no matter what the slope is. Once the temperature exceeds Critical Temperature, Fan Output value will be determined in accordance to the slope only when the temperature falls below (TCritical – Criticl Hyst.)



The right graph gives a picture of how the mapping relationship is made by this setting.

In this example, Fan2 retrieves information from Temperature 1 and Temperature 2, and decides the next fan output value applied to Fan2. To speed up or to slow down the fan is based on the analysis of the W83795G/ADG. Basically, the W83795G/ADG sorts and analyzes the information from each temperature sensor and SmartFan Controls. The analysis may be like, “Temperature 1 needs to speed up the fan”; “Temperautre 2 does not need so fast fan speed”; “Temperuatre 1 does not need fast fans any more”, and “Temperautre 2 hopes to keep the current fan speed”. Then, the algorithm will make a decision to control the fan by the following simple rule.

If Temperautre 1 says, “I need a faster fan”, and Temperuatre 2 says, “No fast fan needed”. The W83795G/ADG will take request of TD1 and start to speed up the fan. In short, the W83795G/ADG always takes the most critical request and applies it to the related fan.



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The concept is quite simple. When the temperature is higher than **TargetTemp+ Hystersis Temp**, the fan will be speeded up. When the temperature is lower than **TargetTemp- Hystersis Temp**, the fan will be slowed down. Otherwise, the fan keeps its current speed.

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10.1.2 Fan Register Details

10.1.2.1. Fan Control Mode Selection Registers (FCMS)

Once the SmartFan function is enabled, the W83795G/ADG supports three SmartFan modes, Speed Cruise™, Thermal Cruise™ and SMART FAN™IV mode

Location:

Location: **FCMS1** - Bank 2 Address 01_{HEX}

Location: **FCMS2** - Bank 2 Address 08_{HEX}

Type: Read / Write

Reset: 3VSB Rising,
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

FCMS1

BIT	7	6	5	4	3	2	1	0
NAME	**F8SC**	**F7SC**	**F6SC**	**F5SC**	**F4SC**	**F3SC**	**F2SC**	**F1SC**
DEFAULT	00_{HEX}							

BIT	DESCRIPTION
7-0	**F8SC – F1SC:** Enable FANCTL8 – FANCTL1 Speed Cruise™ mode. 0 = FANCTL8 –FANCTL1 is applies fan control by **FCMS2** register. (Default) 1 = FANCTL8 – FANCTL1 is applies Speed Cruise™ control for FANIN8-FANIN1 speed inputs respectively. FANCTL3-FANCTL8 functions are not for W83795ADG.

FCMS2

BIT	7	6	5	4	3	2	1	0
NAME	**Reserved**		**T6FC**	**T5FC**	**T4FC**	**T3FC**	**T2FC**	**T1FC**
DEFAULT	00_{HEX}							

BIT	DESCRIPTION
7-6	**Reserved.**
5-0	**T6FC – T1FC:** Select Temp6 – Temp1 for Smart Fan mode. 0 = Thermal Cruise™ Mode. 1 = SMART FAN™IV Mode. NOTE: See also **TFMR** (Temperature to Fan mapping Relationships) register.

10.1.2.2. Temperature to Fan mapping Relationships Register (TFMR)

T1FMR – T6FMR is six temperature (temp1-temp6) sources to deal with the fan relationship. While reset it is cleared (00_{HEX}).

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Location:
T1FMR - Bank 2 Address 02_{HEX}
T2FMR - Bank 2 Address 03_{HEX}
T3FMR - Bank 2 Address 04_{HEX}

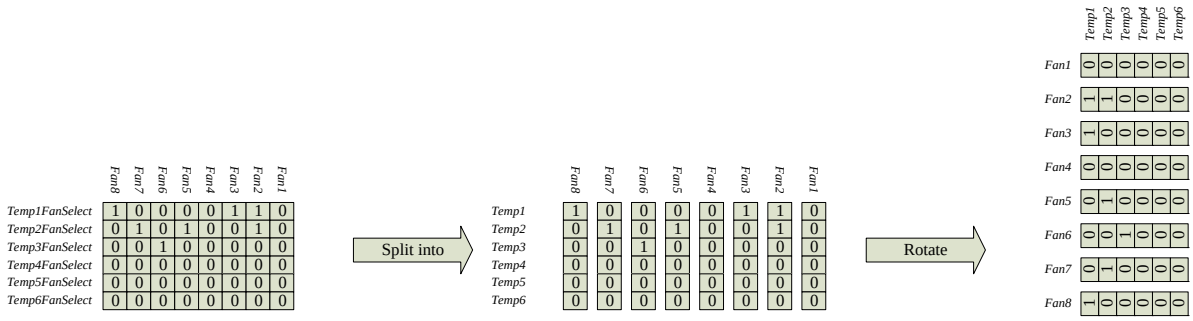
T4FMR - Bank 2 Address 05_{HEX}
T5FMR - Bank 2 Address 06_{HEX}
T6FMR - Bank 2 Address 07_{HEX}
Type: Read / Write
Reset: 3VSB Rising,
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

T1FMR – T6FMR

BIT	7	6	5	4	3	2	1	0
NAME	**F8SF**	**F7SF**	**F6SF**	**F5SF**	**F4SF**	**F3SF**	**F2SF**	**F1SF**
DEFAULT	00_{HEX}							

BIT	DESCRIPTION
7-0	**F8SF – F1SF:** Enable FANCTL8 – FANCTL1 Smart Fan. 0 = FANCTL has no relation with this temperature source. FANCTL is controlled by manual mode. (Default) 1 = Applies SmartFan control for Thermal Cruise™ or SMART FAN™IV on FANCTL and this temperature. FANCTL3-FANCTL8 functions are not for W83795ADG.

The following example explains the concept of **T1FMR – T6FMR** Mapping. In this case, **T1FMR** is set to 86_{HEX}; **T2FMR** is set to 52_{HEX}; **T3FMR** is set 20_{HEX}, and the other 3 are left unset.



Splitting and rotating the six registers bit by bit as the figure above helps to understand the relationship better. For the rows of Fan1 and Fan4, all of the temperatures are de-asserted, which means Fan1/Fan4 and the temperature are irrelevant. Thus they are in the manual mode under this setting. For Fan2, it is clear that it is relative to temperature 1 and 2, so it will activate SmartFan control with temperature 1/2 as its input.

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10.1.2.3. Temperature Source Selection Register (TSS)

W83795G/ADG has six temperature sources (Temp1-Temp6) to control SmartFan Mode, user can select Thermal Cruise mode or SMART FAN™ IV.

Location:
T12TSS - Bank 2 Address 09_{HEX}
T34TSS - Bank 2 Address $0A_{HEX}$
T56TSS - Bank 2 Address $0B_{HEX}$
Type: Read / Write
Reset: 3VSB Rising,
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

T12TSS

BIT	7	6	5	4	3	2	1	0
NAME	**Temp2 temperature source selection BIT [3-0]** Refer the Temperature Source Selection Table to select temperature source.				**Temp1 temperature source selection BIT [3-0]** Refer the Temperature Source Selection Table to select temperature source.			
DEFAULT	00_{HEX}							

T34TSS

BIT	7	6	5	4	3	2	1	0
NAME	**Temp4 temperature source selection BIT [3-0]** Refer the Temperature Source Selection Table to select temperature source.				**Temp3 temperature source selection BIT [3-0]** Refer the Temperature Source Selection Table to select temperature source.			
DEFAULT	00_{HEX}							

T56TSS

BIT	7	6	5	4	3	2	1	0
NAME	**Temp6 temperature source selection BIT [3-0].** Refer the Temperature Source Selection Table to select temperature source.				**Temp5 temperature source selection BIT [3-0]** Refer the Temperature Source Selection Table to select temperature source.			
DEFAULT	00_{HEX}							

Temperature Source Selection Table:

BIT [3-0]	Temperature Source					
	Temp1	**Temp2**	**Temp3**	**Temp4**	**Temp5**	**Temp6**
0000_{BIN}	TD1/TR1	TD2/TR2	TD3/TR3	TD4/TR4	TR5	TR6
0001_{BIN}	DTS1	DTS2	DTS3	DTS4	TD1/TR1	TD2/TR2
0010_{BIN}	DTS5	DTS6	DTS7	DTS8	TD3/TR3	TD4/TR4
0011_{BIN}	TR5	TR6	TR5	TR6	Reserved	Reserved
0100_{BIN} -1111_{BIN}	127℃	127℃	127℃	127℃	127℃	127℃

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10.1.2.4. Default Fan Speed at Power-on (DFSP)

DFSP (default fan peed at power-on) sets the initial speed of every fan. When the system is turned on, a default will be given to all fan outputs according to the register content. This register is specially designed to be reset by VSB only, so at the second system power on, the system will use the last setup speed to turn on all of the fans.

Location: **DFSP** - Bank 2 Address $0C_{HEX}$
Type: Read / Write
Reset: 3VSB Rising,

DFSP

BIT	7	6	5	4	3	2	1	0
NAME	**DefaultSpeed** (Default Fan Speed at Power-on). Specifies the fan duty at next power on.							
DEFAULT	$4D_{HEX}$							

10.1.2.5. SmartFan Output Step Up Time (SFOSUT)

SFOSUT adjusts the time interval of the fan speed up by a unit. The default setting is 12.8sec.

Location: **SFOSUT** - Bank 2 Address $0D_{HEX}$
Type: Read / Write
Reset: 3VSB Rising,
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

SFOSUT

BIT	7	6	5	4	3	2	1	0
NAME	**UpTime** (SmartFan Step Up Time). Unit in 0.1sec. Programmed as the interval of continuous Fan ramping up.							
DEFAULT	80_{HEX}							

SmartFan is designed for the smooth operation of the fan. The fan duty is seldom suddenly increased or decreased. Instead, most often the duty is increased or decreased by 1 LSB. The Up Time / Down Time register defines the time interval between successive duty increases or decreases. If this value is set too small, the fan will not have enough time to speed up after tuning the duty and sometimes may result in unstable fan speed. On the other hand, if Up Time / Down Time is set too large, the fan may not work fast enough to dissipate the heat. This register should never be set to 0. Otherwise, the fan duty will be abnormal.

Only in the following cases will the fan duty soar or plummet.
→3VDD Power – on/off
→Fan Turn off state to Start
→Fan at **FONV** (Fan Output Nonstop Value) to turn off state

10.1.2.6. SmartFan Output Step Down Time (SFOSDT)

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Down Time reduces the time interval of the fastest fan speed by a unit. The default setting is 12.8sec.

Location: **SFOSDT** - Bank 2 Address $0E_{HEX}$

Type: Read / Write
Reset: 3VSB Rising,
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

SFOSUT

BIT	7	6	5	4	3	2	1	0
NAME	**DownTime** (SmartFan Step Down Time). Unit in 0.1sec. Programmed as the interval of continuous Fan ramping Down.							
DEFAULT	80_{HEX}							

This register should never be set to 0. Otherwise, the fan duty will be abnormal.

10.1.2.7. Fan Output Mode Control (FOMC)

Location:
FOMC - Bank 2 Address $0F_{HEX}$

Type: Read / Write
Reset: 3VSB Rising,
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

FOMC

BIT	7	6	5	4	3	2	1	0
NAME	**F8OMC**	**F7OMC**	**F6OMC**	**F5OMC**	**F4OMC**	**F3OMC**	**F2OMC**	**F1OMC**
DEFAULT	W83795G default value is 00_{HEX} W83795ADG default value is 02_{HEX}							

BIT	DESCRIPTION
7-0	**F8OMC – F1OMC:** FANCTL8 – FANCTL1 output mode control. 0 = PWM output duty cycle. (Default) 1 = DC output. FANCTL3-FANCTL8 functions are not for W83795ADG.

10.1.2.8. Fan Output Value (FOV)

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F1OV – F8OV is FANCTL1-FANCTL8 current fan output. In the manual mode, the user can set preferred fan output value. However, in the Smart Fan mode, it is read-only.

Fans that are not set to be in Speed Cruise™, Thermal Cruise™ or SMART FAN™IV are in Manual Mode.

Location:

F1OV - Bank 2 Address 10_{HEX}
F2OV - Bank 2 Address 11_{HEX}
F3OV - Bank 2 Address 12_{HEX}
F4OV - Bank 2 Address 13_{HEX}
F5OV - Bank 2 Address 14_{HEX}
F6OV - Bank 2 Address 15_{HEX}
F7OV - Bank 2 Address 16_{HEX}
F8OV - Bank 2 Address 17_{HEX}

Type: Read / Write (in Manual Mode)
Read Only (in the Smart Fan mode)
Reset: 3VSB Rising,
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

F1OV – F8OV

BIT	7	6	5	4	3	2	1	0
NAME	Output Value							
DEFAULT	Depend on DefaultSpeed. $4D_{HEX.}$							

BIT	DESCRIPTION
7-0	**Output Value –** Current fan output value. Specifies the current fan output value of the fan (FANCTL8-FANCTL1). If 3VDD is low, this register is set to zero by the hardware. FANCTL3-FANCTL8 functions are not for W83795ADG.

F1OV – F8OV also has a special characteristic- sequential power-on respectively. This function is used to avoid over loads of the system current when the system is powered-on and all fans start to spin. The W83795G/ADG takes 0.1 second (12.5ms intervals for 8 fans) to turn on all of the fans one by one.

10.1.2.9. Fan Output PWM Frequency Prescalar (FOPFP)

F1OPFP – **F8OPFP** control the FANCTL1-FANCTL8 fan output frequency in the PWM mode. A wide range of clocks can be selected to satisfy customer needs. The default output frequency is 26 KHz.
FANCTL3-FANCTL8 functions are not for W83795ADG.

Location:

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F1OPFP - Bank 2 Address 18_{HEX}
F2OPFP - Bank 2 Address 19_{HEX}
F3OPFP - Bank 2 Address $1A_{HEX}$
F4OPFP - Bank 2 Address $1B_{HEX}$
F5OPFP - Bank 2 Address $1C_{HEX}$
F6OPFP - Bank 2 Address $1D_{HEX}$
F7OPFP - Bank 2 Address $1E_{HEX}$
F8OPFP - Bank 2 Address $1F_{HEX}$

Type: Read / Write
Reset: 3VSB Rising,
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

F1OPFP – F8OPFP

BIT	7	6	5	4	3	2	1	0
NAME	CKSEL	Divisor						
DEFAULT	1	0	0	0	0	1	0	0

* The default value of B version W83795G/ADG is 85h.

BIT	DESCRIPTION
7	**CKSEL –** Clock source select. CLKIN Frequency CLKSEL / 14.318MHz / 24MHz / 33MHz / 48MHz 0 / 1.024KHz / 1.024KHz / 1.024KHz / 1KHz 1 / 55.93Kz / 93.75KHz / 130.21KHz / 125KHz
6-0	**Divisor –** Clock frequency Divisor.

The clock source selected by CKSEL will be divided by the divisor and used as a fan PWM output frequency. There are 2 divisors depending on CKSEL.

If CKSEL equals 1, then the output clock is simply equal to 130.21/ (Divisor+1) KHz (@ frequency of CLKIN is 33MHz).

If CKSEL equals 0, the output clock is 1KHz/MappedDivisor. MappedDivisor depends on Divisor[3:0] and is described in the table below.

Divisor[3:0]	Mapped Divisor	Output Frequency	Divisor[3:0]	Mapped Divisor	Output Frequency
0000	1	1024Hz	1000	12	85Hz
0001	2	512Hz	1001	16	64Hz
0010	3	341Hz	1010	32	32Hz
0011	4	256Hz	1011	64	16Hz
0100	5	205Hz	1100	128	8Hz
0101	6	171Hz	1101	256	4Hz
0110	7	146Hz	1110	512	2Hz
0111	8	128Hz	1111	1024	1Hz

10.1.2.10. Fan Output Start-up Value (FOSV)

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From still to rotate, the fan usually needs a higher fan output value to generate enough torque to conquer the restriction force. Thus the W83795G/ADG includes a **FOSV** (Fan Output Start-up Value) to turn on the fan with the specified output value. (Please refer to **Smart Fan Control Parameters Figure)**

Location:
F1OSV - Bank 2 Address 20_{HEX}
F2OSV - Bank 2 Address 21_{HEX}
F3OSV - Bank 2 Address 22_{HEX}
F4OSV - Bank 2 Address 23_{HEX}
F5OSV - Bank 2 Address 24_{HEX}
F6OSV - Bank 2 Address 25_{HEX}
F7OSV - Bank 2 Address 26_{HEX}
F8OSV - Bank 2 Address 27_{HEX}

Type: Read / Write
Reset: 3VSB Rising,
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

F1OSV – F8OSV

BIT	7	6	5	4	3	2	1	0
NAME	FanStart							
DEFAULT	30_{HEX}							

BIT	DESCRIPTION
7-0	**FanStart –**control the FANCTL1-FANCTL8 fan output start-up value. FANCTL3-FANCTL8 functions are not for W83795ADG.

10.1.2.11. Fan Output Nonstop Value (FONV)

It takes some time to bring a fan from still to working state. Therefore, **F1ONV - F8ONV** are designed with a minimum fan output to keep the fan working when the system does not require the fan to help reduce heat but still want to keep the fast response time to speed up the fan. (Please refer to **Smart Fan Control Parameters Figure)**

Location:
F1ONV - Bank 2 Address 28_{HEX}
F2ONV - Bank 2 Address 29_{HEX}
F3ONV - Bank 2 Address $2A_{HEX}$
F4ONV - Bank 2 Address $2B_{HEX}$
F5ONV - Bank 2 Address $2C_{HEX}$
F6ONV - Bank 2 Address $2D_{HEX}$
F7ONV - Bank 2 Address $2E_{HEX}$

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F8ONV - Bank 2 Address $2F_{HEX}$

Reset: 3VSB Rising,
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

F1ONV – F8ONV

BIT	7	6	5	4	3	2	1	0
NAME	**FanNonStop**							
DEFAULT	10_{HEX}							

BIT	DESCRIPTION
7-0	**FanNonStop –** control the FANCTL1-FANCTL8 fan output nonstop value. FANCTL3-FANCTL8 functions are not for W83795ADG.

10.1.2.12. Fan Output Stop Time (FOST)

A time interval is specified to tell the W83795G/ADG when to turn off the fan if SmartFan continuously requests to slow down the fan which has already reached the **F1ONV – F8ONV**. The default is 10 sec. (Please refer to **Smart Fan Control Parameters Figure)**

Location:
F1OST - Bank 2 Address 30_{HEX}
F2OST - Bank 2 Address 31_{HEX}
F3OST - Bank 2 Address 32_{HEX}
F4OST - Bank 2 Address 33_{HEX}
F5OST - Bank 2 Address 34_{HEX}
F6OST - Bank 2 Address 35_{HEX}
F7OST - Bank 2 Address 36_{HEX}
F8OST - Bank 2 Address 37_{HEX}

Reset: 3VSB Rising,
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

F1OST – F8OST

BIT	7	6	5	4	3	2	1	0
NAME	**FanStopTime**							
DEFAULT	FF_{HEX}							

BIT	DESCRIPTION

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7-0	**FanStopTime –** control the FANCTL1-FANCTL8 fan stop time from **FONV** (Fan Output Nonstop Value) to the off state. Unit in 0.1sec. Ranges from 0.1sec to 25.5sec. If set to 0, the fan will never stop. FANCTL3-FANCTL8 functions are not for W83795ADG.

10.1.2.13. Fan Output PWM Polarity Control (FOPPC)

Location: **FOPPC** - Bank 2 Address 38_{HEX}

Reset: 3VSB Rising,
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

FOPPC

BIT	7	6	5	4	3	2	1	0
NAME	**F8POL**	**F7POL**	**F6POL**	**F5POL**	**F4POL**	**F3POL**	**F2POL**	**F1POL**
DEFAULT	FF_{HEX}							

BIT	DESCRIPTION
7-0	**F8POL – F1POL:** control FANCTL8 - FANCTL1 PWM output polarity. 0 = Low active. PWM is controlled by negative duty cycle. 1 = High active. (Default). PWM is controlled by positive duty cycle. FANCTL3-FANCTL8 functions are not for W83795ADG.

10.1.2.14. FANIN Target Speed (FTS)

In Fan Speed Cruise™ mode, each FANIN tachometer has to have a target fan speed. The W83795G/ADG will try to tune relative fan output to keep the fan speed of target. The default target speed for FANIN tachometer is 6000h.

Location:

F1TSH - Bank 2 Address 40_{HEX}
F1TSL - Bank 2 Address 41_{HEX}
F2TSH - Bank 2 Address 42_{HEX}
F2TSL - Bank 2 Address 43_{HEX}
F3TSH - Bank 2 Address 44_{HEX}
F3TSL - Bank 2 Address 45_{HEX}
F4TSH - Bank 2 Address 46_{HEX}
F4TSL - Bank 2 Address 47_{HEX}
F5TSH - Bank 2 Address 48_{HEX}
F5TSL - Bank 2 Address 49_{HEX}
F6TSH - Bank 2 Address $4A_{HEX}$
F6TSL - Bank 2 Address $4B_{HEX}$
F7TSH - Bank 2 Address $4C_{HEX}$
F7TSL - Bank 2 Address $4D_{HEX}$
F8TSH - Bank 2 Address $4E_{HEX}$

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F8TSL - Bank 2 Address $4F_{HEX}$

Type: Read / Write
Reset: 3VSB Rising,
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

F1TSH – F8TSH

BIT	7	6	5	4	3	2	1	0
NAME	**F1TSH – F8TSH**: FANIN1 – FANIN8 tachometer target speed high byte. The real FANIN RPM value calculation is referred to FANIN COUNT CACLULATION description. 12-bitCount Value bit[11:4]							
DEFAULT	60_{HEX}							

F1TSL – F8TSL

BIT	7	6	5	4	3	2	1	0
NAME	**F1TSL – F8TSL**: FANIN1 – FANIN8 tachometer target speed low byte. 12-bitCount Value bit [3:0]				Reserved.			
DEFAULT	00_{HEX}							

See also: TFTS and Fan Speed Cruise™

10.1.2.15. Tolerance of FANIN Target Speed (TFTS)

Location: **TFTS** - Bank 2 Address 50_{HEX}
Type: Read / Write
Reset: 3VSB Rising,
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

TFTS

BIT	7	6	5	4	3	2	1	0
NAME	**Reserved**		**Tolerance of FANIN Target Speed**					
DEFAULT	0	0	0	1	0	0	0	0

BIT	DESCRIPTION
7-6	**Reserved.**
5-0	**Tolerance of FANIN Target Speed**

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	Tolerance of FANIN1 – FANIN8 tachometer target speed. Tolerance range is 00h~3Fh

10.1.2.16. Target Temperature of Temperature Inputs (TTTI)

In Thermal Cruise™ mode, each temperature source has to have a target temperature. The W83795G/ADG will try to tune the fan output to keep the temperature of the target device around the target temperature. The default target temperature is 40℃.

Location:
T1TTI - Bank 2 Address 60_{HEX}
T2TTI - Bank 2 Address 61_{HEX}
T3TTI - Bank 2 Address 62_{HEX}
T4TTI - Bank 2 Address 63_{HEX}
T5TTI - Bank 2 Address 64_{HEX}
T6TTI - Bank 2 Address 65_{HEX}

Type: Read / Write
Reset: 3VSB Rising,
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

T1TTI –T6TTI

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Target Temperature.						
DEFAULT	0	28_{HEX} (40℃)						

BIT	DESCRIPTION
7	**Reserved.**
6-0	**Target Temperature.** Temp1 – Temp6 target temperature inputs. Unit in ℃

See also: HT and Thermal Cruise™

10.1.2.17. Critical Temperature to Full Speed all fan (CTFS)

CTFS defines a system critical temperature. Temperatures exceeding this threshold may lead to system damage or crash. When the W83795G/ADG detects any temperature input exceeding **CTFS**, it will speed up all of the fans to lower the temperature.

When the temperature exceeds Critical Temperature, all FANOUT influenced by this temperature will have a 100% output duty. The other FANOUT will not have 100% duty.

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Location:

T1CTFS - Bank 2 Address 68_{HEX}
T2CTFS - Bank 2 Address 69_{HEX}
T3CTFS - Bank 2 Address $6A_{HEX}$
T4CTFS - Bank 2 Address $6B_{HEX}$
T5CTFS - Bank 2 Address $6C_{HEX}$
T6CTFS - Bank 2 Address $6D_{HEX}$

Type: Read / Write
Reset: 3VSB Rising,
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

T1CTFS – T6CTFS

BIT	7	6	5	4	3	2	1	0
NAME	Critical Temperature							
DEFAULT	50_{HEX} (80℃)							

BIT	DESCRIPTION
7-0	**Critical Temperature.** Temp1 – Temp6 temperature exceed the critical temperature, FANCTL8 – FANCTL1 will work at full speed. Unit in ℃. the range is 0℃~127℃. FANCTL3-FANCTL8 functions are not for W83795ADG.

10.1.2.18. Hystersis of Temperature (HT)

In Thermal Cruise and SMART FAN™ IV mode, to prevent unstable temperatures from throttling the fan speed, the W83795G/ADG employs a hysteresis temperature to separate the speed-up/slow-down temperature points.

Location:

HT1 - Bank 2 Address 70_{HEX}
HT2 - Bank 2 Address 71_{HEX}
HT3 - Bank 2 Address 72_{HEX}
HT4 - Bank 2 Address 73_{HEX}
HT5 - Bank 2 Address 74_{HEX}
HT6 - Bank 2 Address 75_{HEX}

Type: Read / Write
Reset: 3VSB Rising,
Init Reset (CR01.Bit7) is set,

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3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

HT1 – HT6

BIT	7	6	5	4	3	2	1	0
NAME	Hysteresis of Critical Temperature				Hysteresis of Operation Temperature			
DEFAULT	5_{HEX} (5℃)				3_{HEX} (3℃)			

BIT	DESCRIPTION
7-5	**Hysteresis of Critical Temperature.** Hysteresis of critical temperature Temp1-Temp6 temperature. The range is 0℃~15℃
4-0	**Hysteresis of Operation Temperature.** Hysteresis of operation temperature for SMART FAN™ IV and Thermal Cruise™ Temp1-Temp6 temperature. The range is 0℃~15℃

10.1.2.19. SMART FAN™ IV Temperature and DC/PWM Registers (SFIV)

SMART FAN™IV is an algorithm providing a table mapping mechanism to translate the temperature information into output fan duties. The mapping table requires 2 domains for the translation. In the table, a certain temperature corresponds to a certain duty. **T1-T7** (Temperature) and **DC/PWM1-DC/PWM7** (DC/PWM fan output values) are used to define the table. There are totally six tables reside in the W83795G/ADG, one table per temperature channel and 7 entries per table. Therefore, **T1-T7** will have 42 registers, and another 42 registers for **DC/PWM1-DC/PWM7** in this and next section

Location:

Relative Register-at SMART FAN™ IV Control Mode Table

RELATIVE TEMPERAUTRE	NNEMONIC	ADD (Hex)	POR (Hex)	TYPE
Temp1	**T1 – T7**	80-86	00	RW
	DC/PWM1 – DC/PWM7	88-8E	FF	RW
Temp2	**T1 – T7**	90-96	00	RW
	DC/PWM1 – DC/PWM7	98-9E	FF	RW
Temp3	**T1 – T7**	A0-A6	00	RW
	DC/PWM1 – DC/PWM7	A8-AE	FF	RW
Temp4	**T1 – T7**	B0-B6	FF	RW
	DC/PWM1 – DC/PWM7	B8-BE	FF	RW
Temp5	**T1 – T7**	C0-C6	FF	RW
	DC/PWM1 – DC/PWM7	C8-CE	FF	RW
Temp6	**T1 – T7**	D0-D6	FF	RW
	DC/PWM1 – DC/PWM7	D8-DE	FF	RW

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Reset: 3VSB Rising,
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

T1 – T7

BIT	7	6	5	4	3	2	1	0
NAME	**SMART FAN™ IV Temperature**							
DEFAULT	00_{HEX} (0℃)							

DC/PWM1 – DC/PWM7

BIT	7	6	5	4	3	2	1	0
NAME	**SMART FAN™ IV DC/PWM**							
DEFAULT	FF_{HEX} (0℃)							

10.1.2.20. Configure Register of PECI Error (CRPE)

Location:

CRPE1 - Bank 2 Address $E0_{HEX}$
CRPE2 - Bank 2 Address $E1_{HEX}$

Type: Read / Write
Reset: 3VSB Rising,
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

CRPE1

BIT	7	6	5	4	3	2	1	0
NAME	**FANCTL4 BIT[1-0]**		**FANCTL3 BIT[1-0]**		**FANCTL2 BIT[1-0]**		**FANCTL1 BIT[1-0]**	
	Refer the PECI Error Condition Table to fan output value.							
DEFAULT	00_{HEX}							

CRPE2

BIT	7	6	5	4	3	2	1	0
NAME	**FANCTL8 BIT[1-0]**		**FANCTL7 BIT[1-0]**		**FANCTL6 BIT[1-0]**		**FANCTL5 BIT[1-0]**	
	Refer the PECI Error Condition Table to fan output value.							
DEFAULT	00_{HEX}							

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PECI Error Condition Table:

FANCTL1-FANCTL8 fan output value. FANCTL3-FANCTL8 functions are not for 83795ADG.

BIT [1-0]	PECI Error Condition
00_{BIN}	Fan output value keeps at its current value.
01_{BIN}	Fan output value will be set to **FOMV** (Fan Output Min Value when PECI Error).
$1x_{BIN}$	Fan output value will be set to the full speed value (FFh).

10.1.2.21. Fan Output Min Value when PECI Error (FOMV)

Location:

F1OMV - Bank 2 Address $E2_{HEX}$
F2OMV - Bank 2 Address $E3_{HEX}$
F3OMV - Bank 2 Address $E4_{HEX}$
F4OMV - Bank 2 Address $E5_{HEX}$
F5OMV - Bank 2 Address $E6_{HEX}$
F6OMV - Bank 2 Address $E7_{HEX}$
F7OMV - Bank 2 Address $E8_{HEX}$
F8OMV - Bank 2 Address $E9_{HEX}$

Reset: 3VSB Rising,
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

F1OMV – F8OMV

BIT	7	6	5	4	3	2	1	0
NAME	**FanMin**							
DEFAULT	80_{HEX}							

BIT	DESCRIPTION
7-0	**FanMin –** control the FANCTL1-FANCTL8 fan output min value when PECI error condition is occurred. Also see **CRPE** (Configure Register of PECI Error) FANCTL3-FANCTL8 functions are not for W83795ADG.

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11. PECI CONTROL AND SB-TSI FUNCTION

11.1 PECI Control Registers

Intel® new generation CPUs such as Presler begin to support new single wire digital temperature monitoring interface which is called Platform Environment Control Interface or PECI. The W83795G/ADG supports the PECI* version 2.0 for these new generation CPUs. All PECI control registers are located in Bank 3.

The W83795G/ADG PECI configuration, including the PECI address and number of domains, must match the CPU type. BIOS have to detect which kind of CPU it is and program the correct configuration in the W83795G/ADG.

PECI (Platform Environment Control Interface) is a new digital interface to read the CPU temperature of Intel® CPUs. With a bandwidth ranging from 2 Kbps to 2 Mbps, PECI uses a single wire for self-clocking and data transfer. By interfacing to the Digital Thermal Sensor (DTS) in the Intel® CPU, PECI reports a negative temperature (in counts) relative to the processor's temperature at which the thermal control circuit (TCC) is activated. At the TCC Activation temperature, the Intel CPU will operate at reduced performance to prevent the device from thermal damage.

PECI is one of the temperature sensing methods that the W83795G/ADG supports. The W83795G/ADG contains a PECI master and reads the CPU PECI temperature. The CPU is a PECI client.

The PECI temperature values returning from the CPU are in "counts" which are approximately linear in relation to changes in temperature in degrees centigrade. However, this linearity is approximate and cannot be guaranteed over the entire range of PECI temperatures. For further information, refer to the PECI specification. All references to "temperature" in this section are in "counts" instead of "°C".

Figure-1 shows a typical fan speed (PWM duty cycle) and PECI temperature relationship.

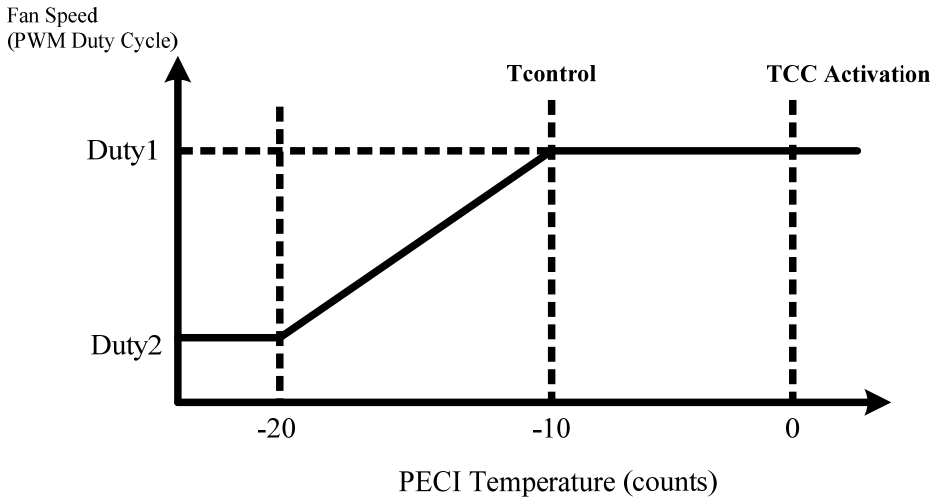

Figure-1 PECI Temperature

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In this illustration, when PECI temperature is -20, the PWM duty cycle for fan control is at Duty2. When CPU is getting hotter and the PECI temperature is -10, the PWM duty cycle is at Duty1.

At TControl PECI temperature, the recommendation from Intel is to operate the CPU fan at full speed. Therefore Duty1 is 100% if this recommendation is followed. The value of TControl can be obtained by reading the related Machine Specific Register (MSR) in the Intel CPU. The TControl MSR address is usually in the BIOS Writer's guide for the CPU family in question. Refer to the relevant CPU documentation from Intel for more information. In this example, TControl is -10.

When the PECI temperature is below -20, the duty cycle is fixed at Duty2 to maintain a minimum (and constant) RPM for the CPU fan.

W83795G/ADG's fan control circuit can only accept positive real-time temperature inputs and limits setting (in Smart Fan ™ mode). The device provides offset registers to 'shift' the negative PECI readings to positive values otherwise the fan control circuit will not function properly. The offset registers are the TBase registers located at Logical Device C, CR[E1h]~CR[E4h]. These registers should be programmed with (positive) values so that the resultant value (Tbase + PECI) is always positive. The unit of the TBase register contents is "count" to match that of PECI values. The resultant value (TBase + PECI) should not be interpreted as the "temperature" (whether in count or °C) of the PECI client (CPU).

Figure-2 shows the temperature/fan speed relationship after Tbase offsets are applied (based on **Figure-1**). This view is from the perspective of the W83795G/ADG fan control circuit.

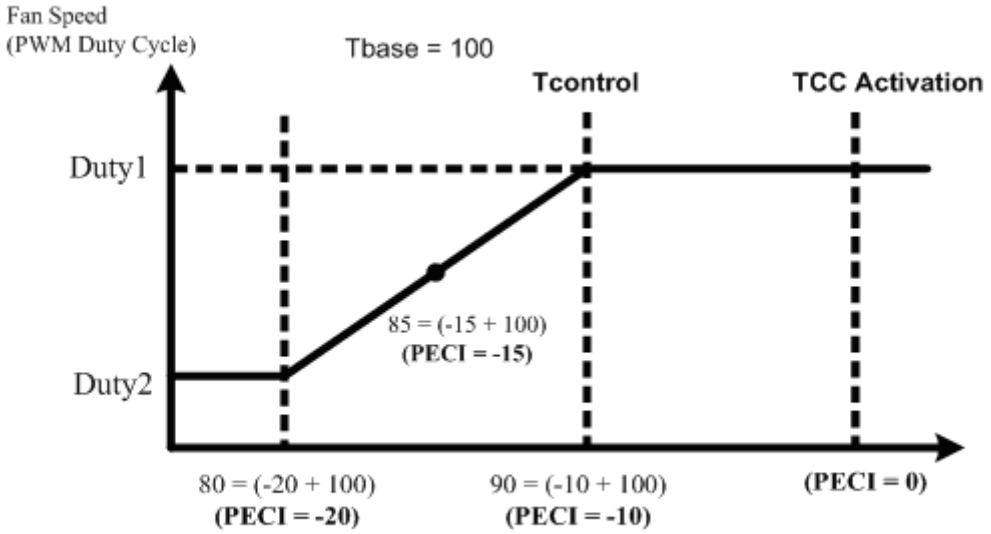

Figure-2 Temperature and Fan Speed Relation after TBase Offsets

Assuming TBase is set to 100 and the PECI temperature is -15 , the real-time temperature value to the fan control circuit will be 85 (-15 + 100). The value of 55 (hex) will appear in the relevant real-time temperature register.

While using Smart Fan control function of W83795G/ADG, BIOS/software must include Tbase in determining the thresholds (limits). In this example, assuming TControl is -10 and Tbase is set to 100 [(1)],

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the threshold temperature value corresponding to the “100% fan duty cycle” event is 90 (-10+100). The value of 5A (hex) should be written to the relevant threshold register.

(1) *TControl is typically -10 to -20 for PECI-enabled CPUs. Base on that, a value of 85 ~100 for Tbase could be set for proper operation of the fan control circuit. This recommendation is applicable for most designs. In general, the concept presented in this section could be used to determine the optimum value of TControl to match the specific application.*

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11.2 SB Temperature Sensor Interface (SB-TSI)

The W83795G/ADG is equipped with a built-in temperature sensor which uses the SBI Temperature Sensor Interface (SB-TSI) interface. SB-TSI function is not for W83795ADG.

The SB-TSI largely follows SMBus v2.0 specification except:

- The statement “An SMBus device must always acknowledge (ACK) its own address “does not apply since a processor may NACK on repeated start conditions even if the address matches its own SMBus address.
- Only 7-bits SMBus addresses are supported.
- SB-TSI implements the Send/Receive Byte and Read/Write Byte protocols.
- SB-TSI registers can only by written using a write byte command.
- Address Resolution Protocol (ARP) is not implemented.
- Packet Error Checking (PEC) is not supported.

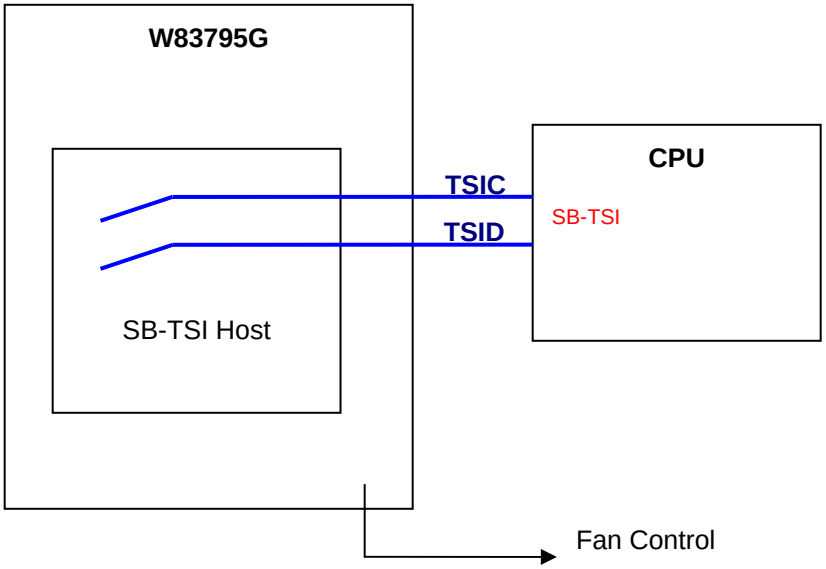

Figure-3 SB-TSI Illustration

SB-TSI temperature readings and limit registers encode the temperature in increments of one eighth of a degree from 0 to 255.875. The high byte represents the integer portion of the temperature from 0 to 255. One increment in the high byte is equivalent to a step of 1°C. The upper three bits of the low byte represent the decimal portion of the temperature. One increment of these bits is equivalent to a step of 0.125°C.

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Table-1 SB-TSI Temperature Encoding Examples

TEMPERATURE	TEMPERATURE HIGH BYTE	TEMPERATURE LOW BYTE
0.000°C	0000_0000b	0000_0000b
1.000°C	0000_0001b	0000_0000b
25.125°C	0001_1001b	0010_0000b
50.500°C	0011_0010b	1000_0000b
127.875°C	0111_1111b	1110_0000b
128.000°C	1000_0000b	0000_0000b
255.875°C	1111_1111b	1110_0000b

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12. REGISTER SUMMARY – BANK3

NNEMONIC	ADD (Hex)	POR (Hex)	TYPE	Description
DTSC	01	00	RW	Digital Temperature Sensor Configuration
DTSE	02	00	RW	Digital Temperature Sensor Enable
PCR	10	84	RW	PECI Control Register
WATP	13	81	RW	Waiting Available Time for PECI 1.1 only
PAC	16-18	*	RW	PECI Agent Configuration register
PRTS	19-1A	00	RW	PECI Report Temperature Style
PMMC	1B-1D	*	RW	PECI Manual Mode Control registers
PATB	20-27	00	RW	PECI Agent Tbase temperature registers
GDC	30-37	00	RO	GetDIB Command
ACR	38-3A	*	RO	Agent Characteristic Registers
ARTR	40-5F	*	RO	Agent Relative Temperature Registers
ATTR	60-6F	*	RO	Agent Tcontrol Temperature Registers
PCAR	70-73	00	RW	PCI Configuration Address Registers
PCWD	74-77	00	RW	PCI Configuration Write Data
PCRD	78-7B	00	RO	PCI Configuration Read Data
MSC	80-84	00	RW	MbxSend Command
CC	85	00	RO	Completion Code
MGC	86-8A	00	RO	MbxGet Command
STCR	A0	10	RW	SB-TSI Configuration Register
STARP	A1	19	RW	SB-TSI Auto Read Period
STSE	A2	00	RO	SB-TSI Slave Enable
STOSS	A3	00	RW	SB-TSI One Shot Start register
STMMCR	A4-A6	*	RW	SB-TSI Manual Mode Configuration Registers
STRD	A8	00	RO	SB-TSI Read Data

*: See registers description

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12.1 Digital Temperature Sensor Configuration (DTSC)

Location:

DTSC - Bank 3 Address 01_{HEX}

Type: Read / Write

Reset: 3VSB Rising,
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

DTSC

BIT	7	6	5	4	3	2	1	0
NAME	SR	Reserved						DIS
DEFAULT	00_{HEX}							

BIT	DESCRIPTION
7	Software Reset. **(SR)** 0 = PWM output duty cycle. (Default) 1 = Software reset INTEL PECI or AMD SB-TSI interface.
6-1	**Reserved.**
0	DTS Interface Select. **(DIS)** 0 = Intel PECI. (Default) 1 = AMD SB-TSI.

12.2 Digital Temperature Sensor Enable (DTSE)

Location:

DTSE - Bank 3 Address 02_{HEX}

Type: Read / Write

Reset: 3VSB Rising,
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

DTSE

BIT	7	6	5	4	3	2	1	0
NAME	D8E	D7E	D6E	D5E	D4E	D3E	D2E	D1E
DEFAULT	00_{HEX}							

BIT	DESCRIPTION
7	DTS8 Enable **(D8E)**

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BIT	DESCRIPTION
	0 = Disable. (Default) 1 = Enable. In Intel PECI, DTS8 device address is 37h. In AMD SB-TSI, DTS8 slave address is 96h.
6	DTS7 Enable **(D7E)** 0 = Disable. (Default) 1 = Enable. In Intel PECI, DTS7 device address is 36h. In AMD SB-TSI, DTS7 slave address is 94h.
5	DTS6 Enable **(D6E)** 0 = Disable. (Default) 1 = Enable. In Intel PECI, DTS6 device address is 35h. In AMD SB-TSI, DTS6 slave address is 92h.
4	DTS5 Enable **(D5E)** 0 = Disable. (Default) 1 = Enable. In Intel PECI, DTS5 device address is 34h. In AMD SB-TSI, DTS5 slave address is 90h.
3	DTS4 Enable **(D4E)** 0 = Disable. (Default) 1 = Enable. In Intel PECI, DTS4 device address is 33h. In AMD SB-TSI, DTS4 slave address is 9Eh.
2	DTS3 Enable **(D3E)** 0 = Disable. (Default) 1 = Enable. In Intel PECI, DTS3 device address is 32h. In AMD SB-TSI, DTS3 slave address is 9Ch.
1	DTS2 Enable **(D2E)** 0 = Disable. (Default) 1 = Enable. In Intel PECI, DTS2 device address is 31h. In AMD SB-TSI, DTS2 slave address is 9Ah.
0	DTS1 Enable **(D1E)** 0 = Disable. (Default) 1 = Enable. In Intel PECI, DTS1 device address is 30h. In AMD SB-TSI, DTS1 slave address is 98h.

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12.3 PECI Control Register (PCR)

Location:

PCR - Bank 3 Address 10_{HEX}

Type: Read / Write

Reset: 3VSB Rising,
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

PCR

BIT	7	6	5	4	3	2	1	0
NAME	MMC	ATR		ADJ			EPF	EN_PECI
DEFAULT	84_{HEX}							

BIT	DESCRIPTION
7	Manual Mode Command. **(MMC)** 0 = Auto repeat. 1 = Manual Mode Command Only do one time (Default)
6-5	Adjust Transaction Tbit Rate. **(ATR)** CLKIN / 14.318MHz / 24MHz / 33MHz / 48MHz 00_{BIN} / Tbit = 1.1us / Tbit = 0.67us / Tbit = 0.5us / Tbit = 0.5us 01_{BIN} / Tbit = 2.2us / Tbit = 1.33us / Tbit = 1us / Tbit = 1us 10_{BIN} / Tbit = 4.5us / Tbit = 2.67us / Tbit = 2us / Tbit = 2us 11_{BIN} / Tbit = 8.9us / Tbit = 5.33us / Tbit = 4us / Tbit = 4us
4-2	Compensate the effect of rising time on physical bus. **(ADJ)** **Adjusting the Tbit counter number to adapt the various agent loading** **Default is 001_{BIN}** (Ideal timing : 001)
1	Enable PECI 1.1a Function. **(EPF)** 0 = Disable PECI1.1a function. 1 = Enable PECI 1.1a function. PECI_REQ# function is enabled. Enable FANIN11/PECI_REQ#/PVID2/GPIO3 multi-function pin for PECI1.1a. VID function is not for W83795ADG.
0	Enable PECI Host Function. **(EN_PECI)** Read only. If Enable **Digital Temperautre Sensor Enable (DTSE)** & **DTS Interface Select (DIS)** bit =0, PECI host function will be enabled and **EN_PECI** will be set to "1".

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12.4 Waiting Available Time for PECI 1.1 only (WATP)

Location:

WATP - Bank 3 Address 13_{HEX}

Type: Read / Write

Reset: 3VSB Rising,
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

The command will be sent 2ms (default) after PECI_REQUEST is pulled low. The time interval can be adjusted by setting this register.

WATP

BIT	7	6	5	4	3	2	1	0
NAME	Wait_Ava_Time [7:0]							
DEFAULT	81_{HEX}							

12.5 PECI Agent Configuration registers (PAC)

This register commands the PECI host to process related agents and domains. Only the agent or domain specified in this register will process PECI transactions. It is reset to 00_{HEX}.

Location:

PAC1 - Bank 3 Address 16_{HEX}

PAC2 - Bank 3 Address 17_{HEX}

PAC3 - Bank 3 Address 18_{HEX}

Type: Read / Write

Reset: 3VSB Rising,

PAC1 - Bank 3 Address 16_{HEX}

BIT	7	6	5	4	3	2	1	0
NAME	A8D1	A7D1	A6D1	A5D1	A4D1	A3D1	A2D1	A1D1
DEFAULT	FF_{HEX}							

BIT	DESCRIPTION
7-0	Agent 8 – Agent1 Domain 1 Enable Bit. **(A8D1 – A1D1)** 0 = Agent does not have domain 1. 1 = Agent has domain 1. (Default)

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PAC2 - Bank 3 Address 17_{HEX}

PECI host to process related agents version (1.0 or 2.0).

BIT	7	6	5	4	3	2	1	0
NAME	**A8P2**	**A7P2**	**A6P2**	**A5P2**	**A4P2**	**A3P2**	**A2P2**	**A1P2**
DEFAULT	00_{HEX}							

BIT	DESCRIPTION
7-0	Agent 8 – Agent1 PECI2.0 enable. **(A8P2 – A1P2)** 0 = Agent does not supply PECI 2.0. (Default) 1 = Agent supplies PECI 2.0.

PAC3 - Bank 3 Address 18_{HEX}

BIT	7	6	5	4	3	2	1	0
NAME	**Reserved**					**PECI_DC**	**Manual_Dmn1**	**Manual_Ver20**
DEFAULT	00_{HEX}							

BIT	DESCRIPTION
7-3	**Reserved.**
2	Adjust PECI Tbit Duty cycle selection. **(PECI_DC)** 0 = 75% Tbit high duty cycle time. (Default) 1 = 68% Tbit high duty cycle time.
1	External control of 2domains. **(Manual_Dmn1)** Enable external control of Domain1 existence 0 = Disable. (Default) 1 = Enable.
0	External control of version 2.0. **(Manual_Ver20**) Enable external control of PECI 2.0 version 0 = Disable. (Default) 1 = Enable.

12.6 PECI Report Temperature Style registers (PRTS)

Location:

PRTS1 - Bank 3 Address 19_{HEX}

PRTS2 - Bank 3 Address $1A_{HEX}$

Type: Read / Write

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Reset: 3VSB Rising,
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

PRTS1 - Bank 3 Address 19_{HEX}

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						Clamp	RtHigh
DEFAULT	00_{HEX}							

BIT	DESCRIPTION
7-2	**Reserved.**
1	PECI clamping function to filter the unreasonable DTS value. **(Clamp)** 0 = DTS values are fully transparent. 1 = DTS values are clamped in -128 ~ 0.
0	Return High Temperature of doamin0 or domain1. **(RtHigh)** Return agent higher temperature between domain0 and domain1 0 = The temperature of each agent is returned from domain 0 or domain 1, which is controlled by **PRTS2** (Bank 3 Address $1A_{HEX}$) 1 = Return the highest temperature in domain 0 and domain 1 of individual Agent.

PRTS2 - Bank 3 Address $1A_{HEX}$

BIT	7	6	5	4	3	2	1	0
NAME	A8RT	A7RT	A6RT	A5RT	A4RT	A3RT	A2RT	A1RT
DEFAULT	00_{HEX}							

BIT	DESCRIPTION
0	Agent 8 – Agent 1 always return the relative Temperature. **(A8RT-A1RT)** Report specific domain temperature for individual agent. It is only available when **RtHigh** = 0. 0 = Agent always returns the relative temperature from domain 0. 1 = Agent always returns the relative temperature from domain 1.

12.7 PECI Manual Mode Control Registers (PMMC)

Type: Read / Write
Reset: 3VSB Rising,
Init Reset (CR01.Bit7) is set,

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3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

MM1 (Manual Mode 1) - Bank 3 Address $1B_{HEX}$

BIT	7	6	5	4	3	2	1	0
NAME	**Reserved**	**Auto**	**PBC**		**MD**	**MA**		
DEFAULT	40_{HEX}							

BIT	DESCRIPTION
7	Reserved.
6	Command Code assignment mode. **(Auto)** 0 = Disable. 1 = Automatically assign command code for transportation.
5-4	PCIByteCount[1:0] **(PBC)** Indicate how many data bytes would be delivered or received in PCIConfig command. 00:1 byte, 01: 2 bytes, 10:4 bytes The number of data byte for PCIWr() and PCIRd() commands. 00_{BIN} = one byte. 01_{BIN} = two bytes. 10_{BIN} = four bytes.
3	Manual_Domain. **(MD)** 0: Manual command execution will target domain0. In other word, 1 for domain1
2-0	Manual_Agent[2:0] **(MA)** 000_{BIN} = Manual command execution will target agent1 001_{BIN} = Manual command execution will target agent2 010_{BIN} = Manual command execution will target agent3 011_{BIN} = Manual command execution will target agent4 100_{BIN} = Manual command execution will target agent5 101_{BIN} = Manual command execution will target agent6 110_{BIN} = Manual command execution will target agent7 111_{BIN} = Manual command execution will target agent8

MM2 (Manual Mode 2) - Bank 3 Address $1C_{HEX}$

BIT	7	6	5	4	3	2	1	0
NAME	**Reserved**	**Reserved**	**PECI2.0_CMD**					
DEFAULT	00_{HEX}							

BIT	DESCRIPTION
7	**Reserved.**

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BIT	DESCRIPTION
6	**Reserved.**
5-0	PECI2.0 command Enable. **(PECI2.0_CMD)** W83795G/ADG supports PECI2.0 commands. If manual mode command enable, it will be clear while relative commands are finished. Bit 5 is applies for Ping() command. Bit 4 is applies for GetDIB() command. Bit 3 is applies for GetTemp() command. Bit 2 is applies for PCIWr() command. Bit 1 is applies for PCIRd() command. Bit 0 is applies for MailBox() command. When bit is set 1, the command is enabled.

UDCC (User Defined Command Code) - Bank 3 Address $1D_{HEX}$

BIT	7	6	5	4	3	2	1	0
NAME	**Command_Code[7:0]**							
DEFAULT	00_{HEX}							

BIT	DESCRIPTION
7-0	**Command_Code [7:0]** If Auto bit is set to 1, user can't define, PECI host will send relative command code. If Auto bit is set to 0, user can define command code to get PECI command. The Client Address, Write Length and Read Length are defined by **PECI2.0_CMD** (Bank 3 Address $1C_{HEX}$ bit 5-0)

12.8 PECI Agent Tbase Temperature registers (PATB)

Location:
PATB1 - Bank 3 Address 20_{HEX}
PATB2 - Bank 3 Address 21_{HEX}
PATB3 - Bank 3 Address 22_{HEX}
PATB4 - Bank 3 Address 23_{HEX}
PATB5 - Bank 3 Address 24_{HEX}
PATB6 - Bank 3 Address 25_{HEX}
PATB7 - Bank 3 Address 26_{HEX}
PATB8 - Bank 3 Address 27_{HEX}

Type: Read / Write

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Reset: 3VSB Rising,
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

PATB1 – PATB8

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Agent 1 – Agent 8 Tbase Temperature						
DEFAULT	00_{HEX}							

BIT	DESCRIPTION
7	**Reserved.**
6-0	**Agent 1 – Agent 8 Tbase Temperature.** Agent base temperature for calculating agent0 absolute temperature Range:0~127℃ (Note 1)

12.9 GetDIB Command (GDC)

Location:
GDC_DIB7 - Bank 3 Address 30_{HEX}
GDC_DIB6 - Bank 3 Address 31_{HEX}
GDC_DIB5 - Bank 3 Address 32_{HEX}
GDC_DIB4 - Bank 3 Address 33_{HEX}
GDC_DIB3 - Bank 3 Address 34_{HEX}
GDC_DIB2 - Bank 3 Address 35_{HEX}
GDC_DIB1 - Bank 3 Address 36_{HEX}
GDC_DIB0 - Bank 3 Address 37_{HEX}
DIB0 bit2 includes agent's information of the domain number
DIB1 includes agent's information of PECI version
Type: Read Only
Reset: 3VSB Rising,

GDC_DIB7 – GDC_DIB0

BIT	7	6	5	4	3	2	1	0
NAME	GetDIB() command read back data							
DEFAULT	00_{HEX}							

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12.10 Agent Characteristic Registers (ACR)

Location:
ACR1 - Bank 3 Address 38_{HEX}
ACR2 - Bank 3 Address 39_{HEX}
ACR3 - Bank 3 Address $3A_{HEX}$

Type: Read Only
Reset: 3VSB Rising,

Record which agent is able to respond to Ping() command.

ACR1

BIT	7	6	5	4	3	2	1	0
NAME	**Alive_Agt[7:0]**							
DEFAULT	FF_{HEX}							

BIT	DESCRIPTION
7-0	**Alive_Agt[7:0]** Result of Ping() command. 1: Agent is able to respond to Ping() command. Agent is alive. 0: Agent isn't able to respond to Ping() command. Agent is not alive.

ACR2

BIT	7	6	5	4	3	2	1	0
NAME	**Dmn1_Agt[7:0]**							
DEFAULT	00_{HEX}							

BIT	DESCRIPTION
7-0	**Dmn1_Agt[7:0]** Result of GetDIB command. PECI host will run according to this information before register AliveDmn1_Agt have been programmed. Indicate that which agent is with domain1. 1: Agent with domain1 0: Agent without domain1

ACR3

BIT	7	6	5	4	3	2	1	0
NAME	**Vern20_Agt[7:0]**							

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DEFAULT	00_{HEX}

BIT	DESCRIPTION
7-0	**Vern20_Agt[7:0]** Result of GetDIB command. PECI host will run according to this information before register AliveDmn1_Agt have been programmed. Indicate which agent supports PECI2.0 version. 1: Support (agent's version is PECI 2.0) 0: Non support (agent's version is PECI 1.0 or PECI 1.1)

12.11 Agent Relative Temperature Registers (ARTR)

These registers return the raw data retrieved from PECI GetTemp(). The data may be the error code (range: 8000H~81FFH) or relative temperatures to process the defined **Tbase**. The error code will only be update in **ARTR** and absolute Temperature will not be updated when the error code is received. If the **RtHigh** mechanism is activated, the normal temperature will always be returned first. In case both 2 domains return errors, the return priority will be Overflow Error > Underflow Error > Missing Diode > General Error. The reset value is $8001_{HEX,}$ in that PECI is defaulted to be off. In PECI, 8001_{HEX} means the diode is missing.

Location:

A1D0RTH- Bank 3 Address 40_{HEX}
A1D0RTL - Bank 3 Address 41_{HEX}
A1D1RTH- Bank 3 Address 42_{HEX}
A1D1RTL - Bank 3 Address 43_{HEX}
A2D0RTH - Bank 3 Address 44_{HEX}
A2D0RTL - Bank 3 Address 45_{HEX}
A2D1RTH - Bank 3 Address 46_{HEX}
A2D1RTL - Bank 3 Address 47_{HEX}
A3D0RTH - Bank 3 Address 48_{HEX}
A3D0RTL - Bank 3 Address 49_{HEX}
A3D1RTH - Bank 3 Address $4A_{HEX}$
A3D1RTL - Bank 3 Address $4B_{HEX}$
A4D0RTH - Bank 3 Address $4C_{HEX}$
A4D0RTL - Bank 3 Address $4D_{HEX}$
A4D1RTH - Bank 3 Address $4E_{HEX}$
A4D1RTL - Bank 3 Address $4F_{HEX}$
A5D0RTH - Bank 3 Address 50_{HEX}
A5D0RTL - Bank 3 Address 51_{HEX}
A5D1RTH - Bank 3 Address 52_{HEX}
A5D1RTL - Bank 3 Address 53_{HEX}
A6D0RTH - Bank 3 Address 54_{HEX}
A6D0RTL - Bank 3 Address 55_{HEX}

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A6D1RTH - Bank 3 Address 56_{HEX}
A6D1RTL - Bank 3 Address 57_{HEX}
A7D0RTH - Bank 3 Address 58_{HEX}
A7D0RTL - Bank 3 Address 59_{HEX}
A7D1RTH - Bank 3 Address $5A_{HEX}$
A7D1RTL - Bank 3 Address $5B_{HEX}$
A8D0RTH - Bank 3 Address $5C_{HEX}$
A8D0RTL - Bank 3 Address $5D_{HEX}$
A8D1RTH - Bank 3 Address $5E_{HEX}$
A8D1RTL - Bank 3 Address $5F_{HEX}$

Type: Read Only
Reset: 3VSB Rising,

BIT	15	14	13	12	11	10	9	8
NAME	**A1D0RTH – A8D0RTH :** Agent 1- Agent 8 Domain0 Relative Temperature High byte **A1D1RTH – A8D1RTH :** Agent 1- Agent 8 Domain1 Relative Temperature High byte Refer the PECI Temperature format to calculate temperature data.							
	Sign	**Temperature[8:2]**						
DEFAULT	$F8_{HEX}$							

BIT	7	6	5	4	3	2	1	0
NAME	**A1D0RTL – A8D0RTL :** Agent 1- Agent 8 Domain0 Relative Temperature Low byte **A1D1RTL – A8D1RTL :** Agent 1- Agent 8 Domain1 Relative Temperature Low byte Refer the PECI Temperature format to calculate temperature data.							
	Temperature[1:0]	**TEMP_2**	**TEMP_4**	**TEMP_8**	**TEMP_16**	**TEMP_32**	**TEMP_64**	
DEFAULT	80_{HEX}							

GetTemp() PECI Temperature format:

BIT	DESCRIPTION
15	Sign Bit. **(Sign)** In PECI Protocol, this bit should always be 1 to represent a negative temperature.
14-6	The integer part of the relative temperature. (**Temperature[8:0]**)
5	**TEMP_2**. 0.5℃ unit.
4	**TEMP_4**. 0.25℃ unit.
3	**TEMP_8**. 0.125℃ unit.
2	**TEMP_16**. 0.0625℃ unit.
1	**TEMP_32**. 0.03125℃ unit.
0	**TEMP_64**. 0.015625℃ unit.

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GetTemp() Response Definition:

RESPONSE	MEANING
General Sensor Error (GSE)	Thermal scan did not complete in time. Retry is appropriate.
0x0000	Processor is running at its maximum temperature or is currently being reset.
All other data	Valid temperature reading, reported as a negative offset from the TCC activation temperature. The valide temperature reading is referred to GetTemp() PECI Temperature format

On some occasions, PECI will return the abnormal states of the PECI bus in addition to the temperature. All the information will be recorded. In some cases, the W83795G/ADG will also do further processing for the alert mechanism. The following describes these codes and their effects to the W83795G/ADG.

Error Code	Description	W83795G/ADG host operation
8000_{HEX}	General Sensor Error	No further processing.
8001_{HEX}	Sensing Device Missing	
8002_{HEX}	Operational, but the temperature is lower than the sensor operation range.	Compulsorily write 0℃ back to the temperature readouts.(Bank 0 Index $1C_{HEX}$ ~ $1F_{HEX}$)
8003_{HEX}	Operational, but the temperature is higher than the sensor operation range.	compulsorily write 127℃ back to the temperature readouts.(Bank 0 Index $1C_{HEX}$ ~ $1F_{HEX}$)
8004_{HEX} ' $81FF_{HEX}$	Reserved.	No further operation.

Besides error conditions or invalid FCS, the normal temperature will be written back to Temperature Readouts with the sum of ARTR value and Tbase value.

12.12 Agent Tcontrol Temperature Registers (ATTR)

Location:

A1TTH- Bank 3 Address 60_{HEX}
A1TTL- Bank 3 Address 61_{HEX}
A2TTH- Bank 3 Address 62_{HEX}
A2TTL- Bank 3 Address 63_{HEX}
A3TTH- Bank 3 Address 64_{HEX}
A3TTL- Bank 3 Address 65_{HEX}
A4TTH- Bank 3 Address 66_{HEX}
A4TTL- Bank 3 Address 67_{HEX}
A5TTH- Bank 3 Address 68_{HEX}
A5TTL- Bank 3 Address 69_{HEX}
A6TTH- Bank 3 Address $6A_{HEX}$

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A6TTL- Bank 3 Address $6B_{HEX}$
A7TTH- Bank 3 Address $6C_{HEX}$
A7TTL- Bank 3 Address $6D_{HEX}$
A8TTH- Bank 3 Address $6E_{HEX}$
A8TTL- Bank 3 Address $6F_{HEX}$

Type: Read Only
Reset: 3VSB Rising,

BIT	15	14	13	12	11	10	9	8
NAME	**A1TTH – A8TTH :** Agent 1- Agent 8 Tcontrol Temperature High byte Refer the PECI Temperature format to calculate temperature data.							
	Sign	**Temperature[8:2]**						
DEFAULT	FD_{HEX}							

BIT	7	6	5	4	3	2	1	0
NAME	**A1TTL – A1TTL :** Agent 1- Agent 8 Tcontrol Temperature Low byte Refer the PECI Temperature format to calculate temperature data.							
	Temperature[1:0]		**TEMP_2**	**TEMP_4**	**TEMP_8**	**TEMP_16**	**TEMP_32**	**TEMP_64**
DEFAULT	80_{HEX}							

12.13 PCI Configuration Address Registers (PCAR)

Refer to PCI Configuration Address defined format to set **PC Address4 – PC Address1** registers value for PCIConfigRd() or PCIConfWr() command.
PCI bus address assignment
Type: Read / Write
Reset: 3VSB Rising,
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.
Location:
PC Address4 (MSB) - Bank 3 Address 70_{HEX}
PC Address3 - Bank 3 Address 71_{HEX}
PC Address2 - Bank 3 Address 72_{HEX}
PC Address1 (LSB) - Bank 3 Address 73_{HEX}

BIT	PCI Configuration Address [31:0]

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NAME	PC Address4	PC Address3	PC Address2	PC Address1
DEFAULT	00_{HEX}	00_{HEX}	00_{HEX}	00_{HEX}

PCI Configuration Address defined format:

BIT	DESCRIPTION
31-28	Reserved.
27-20	Bus
19-15	Device
14-12	Function
11 - 0	Register

12.14 PCI Configuration Write Data (PCWD)

Type: Read / Write

Reset: 3VSB Rising,
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

Location:

PCW Data4 (MSB) - Bank 3 Address 74_{HEX}
PCW Data3 - Bank 3 Address 75_{HEX}
PCW Data2 - Bank 3 Address 76_{HEX}
PCW Data1 (LSB) - Bank 3 Address 77_{HEX}

BIT	PCI Configuration Write Data [31:0]			
NAME	PCW Data4	PCW Data3	PCW Data2	PCW Data1
DEFAULT	00_{HEX}	00_{HEX}	00_{HEX}	00_{HEX}

PCIConfigWr() Response Definition: 'CC' indicates Completion Code.

RESPONSE	MEANING
Bad FCS	Electrical error or Assured Write FCS (AW FCS) failure.
Abort FCS	Illegal command formatting (mismatched RL/WL/Command Code)
CC: 0x40	Command passed, data is valid.
CC: 0x80	Error causing a response timeout. Either due to a rare, internal timing condition or a processor RESET condition or processor S1 state. Retry is appropriate outside of the RESET or S1 states.

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12.15 PCI Configuration Read Data (PCRD)

Type: Read Only
Reset: 3VSB Rising,
Location:
PCR Data4 (MSB) - Bank 3 Address 78_{HEX}
PCR Data3 - Bank 3 Address 79_{HEX}
PCR Data2 - Bank 3 Address $7A_{HEX}$
PCR Data1 (LSB) - Bank 3 Address $7B_{HEX}$

BIT	PCI Configuration Read Data [31:0]			
NAME	PCR Data4	PCR Data3	PCR Data2	PCR Data1
DEFAULT	00_{HEX}	00_{HEX}	00_{HEX}	00_{HEX}

PCIConfigRd() Response Definition: 'CC' indicates Completion Code.

RESPONSE	MEANING
Abort FCS	Illegal command formatting (mismatched RL/WL/Command Code)
CC: 0x40	Command passed, data is valid.
CC: 0x80	Error causing a response timeout. Either due to a rare, internal timing condition or a processor RESET condition or processor S1 state. Retry is appropriate outside of the RESET or S1 states.

12.16 MbxSend Command (MSC)

Type: Read / Write
Reset: 3VSB Rising,
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.
Location:
MbxSend Request Type - Bank 3 Address 80_{HEX}

BIT	7	6	5	4	3	2	1	0
NAME	MbxSend Request Type							
DEFAULT	00_{HEX}							

Location:
MbxSend Data4 (MSB) - Bank 3 Address 81_{HEX}
MbxSend Data3 - Bank 3 Address 82_{HEX}
MbxSend Data2 - Bank 3 Address 83_{HEX}
MbxSend Data1 (LSB) - Bank 3 Address 84_{HEX}

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BIT	MbxSend Data [31:0]			
NAME	MbxSend Data4	MbxSend Data3	MbxSend Data2	MbxSend Data1
DEFAULT	00_{HEX}	00_{HEX}	00_{HEX}	00_{HEX}

MbxSend() Response Definition: 'CC' indicates Completion Code.

RESPONSE	MEANING
Bad FCS	Electrical error.
CC: 0x80	Error causing a response timeout. Either due to a rare, internal timing condition or a processor RESET condition or processor S1 state. Retry is appropriate outside of the RESET or S1 states.
CC: 0x86	Mailbox interface is unavailable or busy.

12.17 Completion Code (CC)

Location:

CC- Bank 3 Address 85_{HEX}

Type: Read Only

Reset: 3VSB Rising,

BIT	7	6	5	4	3	2	1	0
NAME	Completion Code							
DEFAULT	00_{HEX}							

12.18 MbxGet Command (MGC)

Type: Read Only

Reset: 3VSB Rising,

Location:

MbxGet Data4 (MSB) - Bank 3 Address 86_{HEX}

MbxGet Data3 - Bank 3 Address 87_{HEX}

MbxGet Data2 - Bank 3 Address 88_{HEX}

MbxGet Data1 (LSB) - Bank 3 Address 89_{HEX}

BIT	MbxGet Data [31:0]			
NAME	MbxGet Data4	MbxGet Data3	MbxGet Data2	MbxGet Data1
DEFAULT	00_{HEX}	00_{HEX}	00_{HEX}	00_{HEX}

MbxGet Transaction ID - Bank 3 Address 8A

BIT	7	6	5	4	3	2	1	0

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NAME	Reserved	Transaction ID
DEFAULT	00_{HEX}	

MbxGet() Response Definition: 'CC' indicates Completion Code.

RESPONSE	MEANING
Abort Write FCS	Response data is not ready. Command retry is appropriate.
CC: 0x40	Command passed, data is valid.
CC: 0x80	Error causing a response timeout. Either due to a rare, internal timing condition or a processor RESET condition or processor S1 state. Retry is appropriate outside of the RESET or S1 states.
CC: 0x81	Thermal configuration data was malformed or exceeded limits.
CC: 0x82	Thermal status mask is illegal.
CC: 0x83	Invalid counter select.
CC: 0x85	Failure due to lack of Mailbox lock or invalid Transaction ID.
CC: 0x86	Mailbox interface is unavailable or busy.

12.19 SB-TSI Configuration Register (STCR)

Location:

STCR - Bank 3 Address $A0_{HEX}$

Type: Read / Write

Reset: 3VSB Rising,
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

STCR

BIT	7	6	5	4	3	2	1	0
NAME	**Reserved**			**FSB_TSI[3:0]**				**STHE**
DEFAULT	10_{HEX}							

BIT	DESCRIPTION
7-5	**Reserved.**
4-1	Set the frequency of SB-TSI SCL (**FSB_TSI[3:0]**) SB-TSI SCL frequency is 225KHz / (FSB_TSI [3:0] +1). Note that FSB_TSI[3:0] can not be set to $000_{BIN.}$
0	SB-TSI Host Enable. (**STHE**) If Digital Temperature Sensor Enable (**DTSE**) = 1 & DTS Interface Select (**DIS**) =1, SB-TSI

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	host function will be enabled and SB-TSI Host Enable (**STHE)** will be set to 1. This bit is Read Only.

12.20 SB-TSI Auto Read Period (STARP)

Location:

STARP - Bank 3 Address $A1_{HEX}$

Type: Read / Write

Reset: 3VSB Rising,
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

STARP

BIT	7	6	5	4	3	2	1	0
NAME	**TSIAutoReadCycle[7:0]**							
DEFAULT	19_{HEX}							

BIT	DESCRIPTION
7-0	SB-TSI Auto Read Cycle (**TSIAutoReadCycle[7:0]**) Tp = 1ms * TSIAutoReadCycle[7:0] SB-TSI host will read one slave's temperature in Tp time. Note that TSIAutoReadCycle[7:0] can not set to 00_{HEX}

12.21 SB-TSI Slave Enable (STSE)

Location:

STSE - Bank 3 Address $A2_{HEX}$

Type: Read Only

Reset: 3VSB Rising,

STSE

BIT	7	6	5	4	3	2	1	0
NAME	**STSE8**	**STSE7**	**STSE6**	**STSE5**	**STSE4**	**STSE3**	**STSE2**	**STSE1**
DEFAULT	00_{HEX}							

BIT	DESCRIPTION
7-0	SB-TSI DTS8 – DTS1 Enable **(STSE8-STSE1)**

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BIT	DESCRIPTION
	0 = Disable. (Default) 1 = Enable. If Digital Temperature Sensor Enable (**DTSE**) = 1 & DTS Interface Select (**DIS**) **=**1, SB-TSI slave address will be enabled and SB-TSI DTS8 – DTS1 Enable **(STSE8-STSE1)** will be set to 1. In AMD SB-TSI, DTS1 slave address is 98h. DTS2 slave address is 9Ah. DTS3 slave address is 9Ch. DTS4 slave address is 9Eh. DTS5 slave address is 90h. DTS6 slave address is 92h. DTS7 slave address is 94h. DTS8 slave address is 96h. This register is Read Only.

12.22 SB-TSI One Shot Start register (STOSS)

Location:

STOSS - Bank 3 Address $A3_{HEX}$

Type: Read / Write

Reset: 3VSB Rising,
Init Reset (CR01.Bit7) is set,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set,
SYSRSTIN# Falling @ SYSRST_MD (CR01.Bit6) set.

STOSS

BIT	7	6	5	4	3	2	1	0
NAME	**Reserved**							**OneShot**
DEFAULT	00_{HEX}							

BIT	DESCRIPTION
7-1	**Reserved.**
0	SB-TSI One Shot Start (**OneShot**). 0 = This bit will return 0 when SB-TSI host finished one shot start SB-TSI command. 1 = Writing a 1 to this bit, SB-TSI host will one shot start SB-TSI command.

12.23 SB-TSI Manual Mode Configuration Registers (STMMCR)

Type: Read / Write

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Reset: 3VSB Rising,
3VDD Rising @ RST_VDD_MD (CR01.Bit5) set.

STMMCR1 - Bank 3 Address $A4_{HEX}$

BIT	7	6	5	4	3	2	1	0
NAME	MME	OSE	Reserved					RWC
DEFAULT	01_{HEX}							

BIT	DESCRIPTION
7	SB-TSI Manual Mode Enable. (**MME**) 0 = Disable. (Default) 1 = Enable.
6	SB-TSI One Shot Enable. **(OSE)** 0 = Disable. (Default) 1 = Enable.
5-1	**Reserved.**
0	Set SB-TSI Read / Write Command **(RWC)** 0 = Write Command. 1 = Read Command. (Default)

BIT[7:6]		MEANING
MME	OSE	
0	0	SB-TSI host always read SB-TSI 01h and SB-TSI 10h command code data continually and stored in the **Bank0 DTS1~8 and VR LSB** registers.
0	1	After writing a 1 to SB-TSI One Shot Start (**OneShot**), SB-TSI host read one time SB-TSI 01h and SB-TSI 10h command code data and stored in the **Bank0 DTS1~8 and VR LSB** registers.
1	0	After writing a 1 to SB-TSI One Shot Start (**OneShot**), SB-TSI host read or write one time the data and stored in the SB-TSI Read Data High Byte (**STRD)** register. The data command code will depend on SB-TSI Command Code (**STCC**) register.

STMMCR2 - Bank 3 Address $A5_{HEX}$

BIT	7	6	5	4	3	2	1	0
NAME	STCC							
DEFAULT	01_{HEX}							

BIT	DESCRIPTION

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BIT	DESCRIPTION
7-0	SB-TSI Command Code. (**STCC**) Refer the AMD SB-TSI specification to set command code. 01_{HEX} = CPU Temperature High Byte Register. 02_{HEX} = SB-TSI Status Register. 03_{HEX} = SB-TSI Configuration Register. 04_{HEX} = Update Rate Register. 07_{HEX} = High Temperature Threshold High Byte Register. 08_{HEX} = Low Temperature Threshold High Byte Register. 09_{HEX} = SB-TSI Configuration Register. 10_{HEX} = CPU Temperature Low Byte Register. 11_{HEX} = CPU Temperature Offset High Byte Register. 12_{HEX} = CPU Temperature Offset Low Byte Register. 13_{HEX} = High Temperature Threshold Low Byte Register. 14_{HEX} = Low Temperature Threshold Low Byte Register. 22_{HEX} = Timeout Configuration Register. 32_{HEX} = Alert Threshold Register. BF_{HEX} = Alert Configuration Register. FE_{HEX} = Manufacture ID Register. FF_{HEX} = SB-TSI Revision Register.

STMMCR3 - Bank 3 Address $A6_{HEX}$

BIT	7	6	5	4	3	2	1	0
NAME	**SB-TSI Write Data**							
DEFAULT	00_{HEX}							

12.24 SB-TSI Read Data (STRD)

Location:

STRD - Bank 3 Address $A8_{HEX}$

Type: Read Only

Reset: 3VSB Rising,

STRD

BIT	7	6	5	4	3	2	1	0
NAME	SB-TSI Read Data Byte of Manual Mode. If read data are indicated to temperature, refer the Table-1 SB-TSI Temperature Encoding Example to calculate temperature data.							
DEFAULT	00_{HEX}							

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13. ELECTRICAL CHARACTERISTICS

13.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage	-0.3 to +3.6	V
Input Voltage	-0.3 to +3.6	V
Operating Temperature	0 to +70	° C
Storage Temperature	-55 to +150	° C

13.2 DC Characteristics

(Ta = 0° C to 70° C, 3VDD= 3.3V ± 10%, 3VSB =3.3V ± 10%, GND = 0V)

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
OD_{12} – Open-drain output pin with source-sink capability of 12 mA						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
OUT_{12} - Output buffer pin with source-sink capability of 12 mA						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
V1 - VID input pin for INTEL™ VRM design						
Input Low Voltage	V_{IL}			0.4	V	
Input High Voltage	V_{IH}	0.6			V	
V2 - VID input pin for AMD™ VRM design						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	1.4			V	
V3 –Bi-direction pin for AMD™ SVID design						
Input Low Voltage	V_{IL}		0.6		V	

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PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input High Voltage	V_{IH}		1		V	
Output Low Voltage	V_{OL}			0.285	V	
V4 – Bi-direction pin for INTEL™ PECI						
Input Low Voltage	V_{IL}	$0.275V_{tt}$		$0.5V_{tt}$	V	
Input High Voltage	V_{IH}	$0.55V_{tt}$		$0.725V_{tt}$	V	
Output Low Voltage	V_{OL}			$0.25V_{tt}$	V	
Output High Voltage	V_{OH}	$0.75V_{tt}$			V	
Hysterisis	V_{Hys}	$0.1V_{tt}$			V	
V5 – Bi-direction pin for PROCHOT						
Input Low Voltage	V_{IL}			0.4	V	
Input High Voltage	V_{IH}	0.8			V	
Output Low Voltage	V_{OL}			0.2	V	
IN_{ts} - TTL level Schmitt-triggered input pin						
Input Low Voltage	V_{IL}			0.8	V	3VSB = 3.3V
Input High Voltage	V_{IH}	2.0			V	3VSB = 3.3V
Input High Leakage	I_{LIH}			+10	μA	VIN=3.3V
Input Low Leakage	I_{LIL}			-10	μA	VIN=0V
AIN - Analog input pin						
Input High Leakage	I_{LIH}			+1	μA	VIN=3.3V
Input Low Leakage	I_{LIL}			-1	μA	VIN=0V

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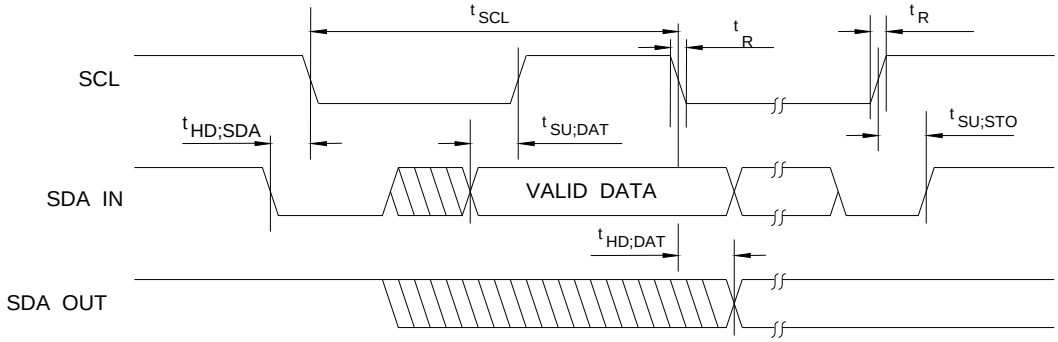
13.3 AC Characteristics

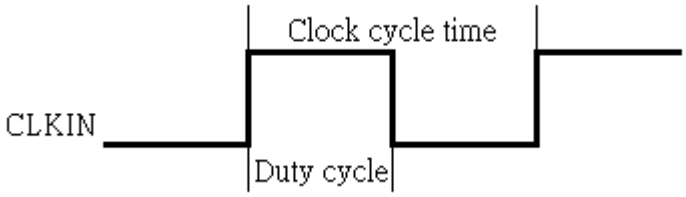
SMBus Interface



Serial Bus Timing Diagram

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
SCL clock period	t_{SCL}	10		uS
Start condition hold time	$t_{HD;SDA}$	4.0		uS
Stop condition setup-up time	$t_{SU;STO}$	4.0		uS
DATA to SCL setup time	$t_{SU;DAT}$	150		nS
DATA to SCL hold time	$t_{HD;DAT}$	270		nS
SCL and SDA rise time	t_R		1.0	uS
SCL and SDA fall time	t_F		300	nS

Clock Input Timing



DESCRIPTION	CLKIN		
	MIN	TYP	MAX
Clock cycle time	(1/CLKIN) x0.97	1/CLKIN	(1/CLKIN) x1.03
Duty cycle	45%		55%

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14. ORDER INFORMATION

PART NO.	PACKAGE	REMARKS
W83795G	64-pin LQFP	Pb-free Package
W83795ADG	48-pin LQFP	Pb-free Package

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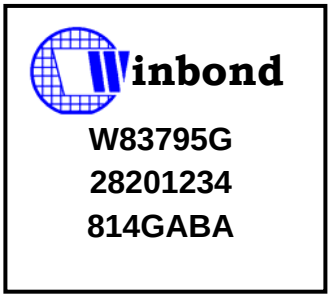
15. TOP MARKING SPECIFICATIONS



First Line	Nuvoton Logo, and company name.
Second Line	IC part number: W83795G W83795ADG
Third Line	Serial number
Forth Line	Tracking Code: 8 14 G A BA for Package information

8	Package is made in 2008
14	Week: 14
G	Assembly house ID; G means Greatek; A means ASE; O means OSE
A	IC version; A means A version; B means B version; C means C version
BA	Mask version

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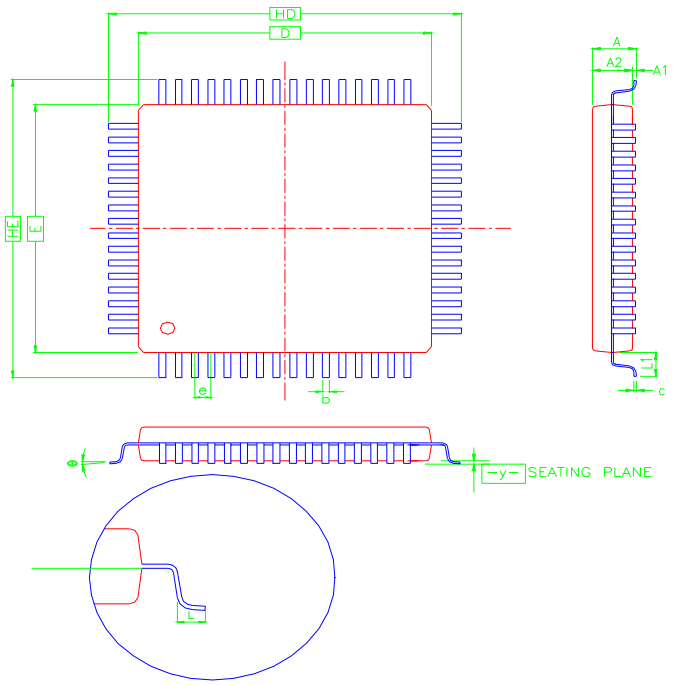
16. PACKAGE DRAWING AND DIMENSIONS

W83795G (64-pin LQFP 10X10X1.4mm)



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A_1	0.002	—	0.006	0.05	—	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.008	0.011	0.17	0.20	0.27
c	0.004	—	0.008	0.09	—	0.20
D	—	0.393	—	—	10.00	—
E	—	0.393	—	—	10.00	—
e	—	0.020	—	—	0.50	—
H_D	—	0.472	—	—	12.00	—
H_E	—	0.472	—	—	12.00	—
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
y	—	0.004	—	—	0.10	—
θ	0°	3.5°	7°	0°	3.5°	7°

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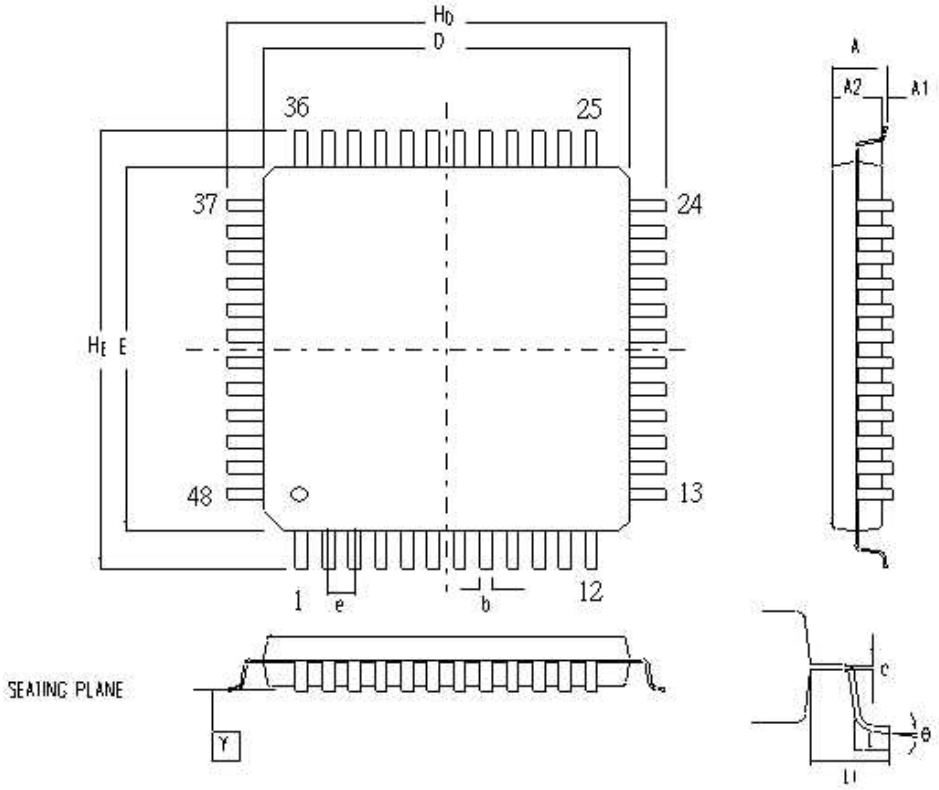
W83795ADG (48-pin LQFP)



Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A1	0.002	0.004	0.006	0.05	0.10	0.15
A2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
HD	0.350	0.354	0.358	8.90	9.00	9.10
HE	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°

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17. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
1.0	12/12/2008	N.A.	The Initial Formal Release.
1.1	05/05/2009	147	Added DC characteristic and revised typos.
1.2	06/03/2009	17,25,126,149	1. Modified CLKIN pin description. 2. Modified PECI ATR register. 3. Added CLKIN specification.
1.3	10/21/2009	32,108,129	1. Added C version chip information. 2. Modified PWM Fan output prescalar default value. 3. Added PECI read value clamping function. 4. Revised typos in the document.
1.4	6/3/2010	61~64,148	1. Revised register description of PROCHOT. 2. Modified AC Characteristic. 3. Revised typos in the document.
1.41	8/2/2010	51	1. Modified the SMI_POL description.

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