

CMOS 4-BIT MICROCONTROLLER

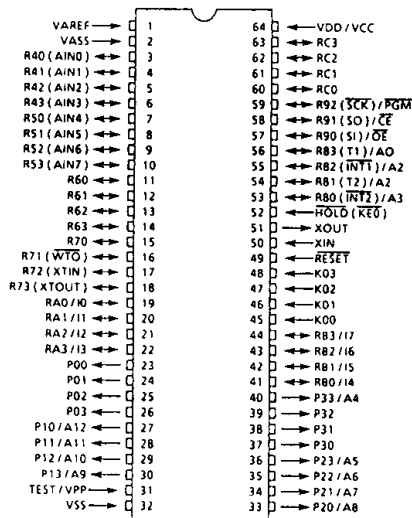
TMP47P860N
TMP47P860F

The 47P860 is the OTP microcontroller with 64Kbits EPROM. For program operation, the programming is achieved by using with EPROM programmer (TMM2764D type) and adapter socket (BM1102, BM1109). The function of this device is exactly same as the 47C860.

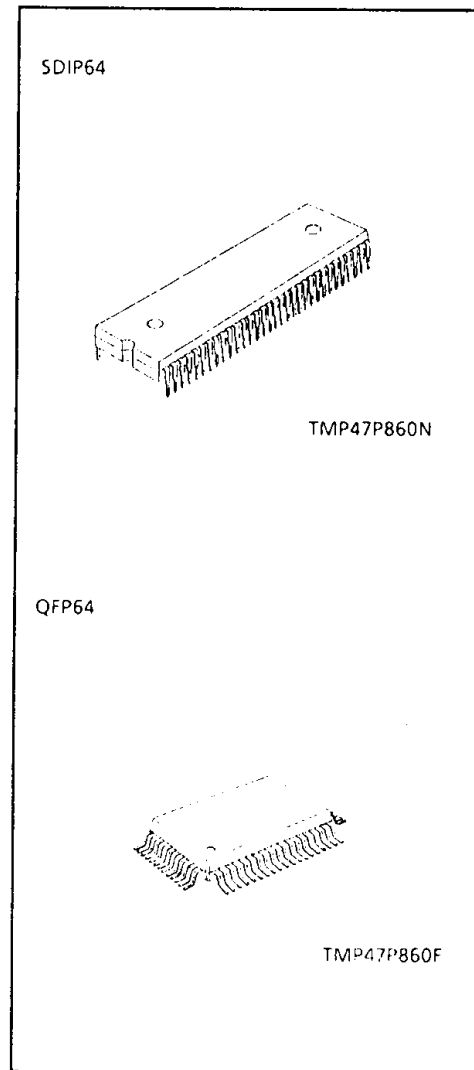
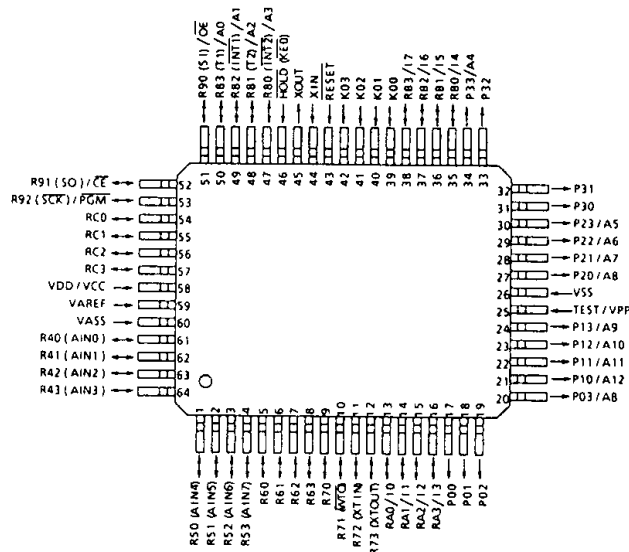
PART No.	EPROM	RAM	PACKAGE
TMP47P860N	OTP	512 x 4-bit	SDIP64
TMP47P860F	8192 x 8-bit		QFP64

PIN ASSIGNMENT (TOP VIEW)

SDIP64



QFP64



PIN FUNCTION

The 47P860 has MCU mode and PROM mode.

(1) MCU mode

The 47C660/860 and the 47P860 are pin compatible (TEST pin for out-going test. Be fixed to low level.).

(2) PROM mode

PIN NAME	INPUT / OUTPUT	FUNCTIONS	PIN NAME(MCU mode)
A12 - A9	INPUT	Address inputs	P10 - P13
A8 - A5			P20 - P23
A4			P33
A3 - A0			R80 - R83
I7 - I4	I/O	Data outputs (Inputs)	RB3 - RB0
I3 - I0			RA3 - RA0
$\overline{\text{PGM}}$	Input	Program control input	R92
$\overline{\text{CE}}$		Chip Enable input	R91
$\overline{\text{OE}}$		Output Enable input	R90
VPP	Power supply	+ 21V / 5V (Program supply voltage)	TEST
VCC		+ 5V	VDD
VSS		0V	VSS
P03 - P00	output	Open	
P32 - P30			
RC3 - RC0	I/O		
R43 - R40	I/O	Be fixed to Low Level	
R53 - R50			
R63 - R60			
R73 - R70			
K03, K02	Input	PROM mode setting pin. Be fixed to low level.	
K01, K00			
$\overline{\text{RESET}}$	Input		
$\overline{\text{HOLD}}$	Input		
XIN	Input	Resonator connecting pin	
XOUT	output		
VAREF	Power supply	Be fixed to low level	
VASS			

OPERATIONAL DESCRIPTION

The following is an explanation of hardware configuration and operation in relation to the 47P860. The 47P860 is the same as the 47C660/860 except that an EPROM or OTP is used instead of a built-in mask ROM.

1. OPERATION mode

The 47P860 has an MCU mode and a PROM mode.

1.1 MCU mode

The MCU mode is set by fixing the TEST/VPP pin at the "L" level. Operation in the MCU mode is the same as for the 47C660/860, except that the TEST/VPP pin does not have built in pull-down resistor and cannot be used open.

1.1.1 Program Memory

The program storage area is the same as for the 47C860. Data conversion tables must be set in two locations when using the 47P860 to check 47C660 operation.

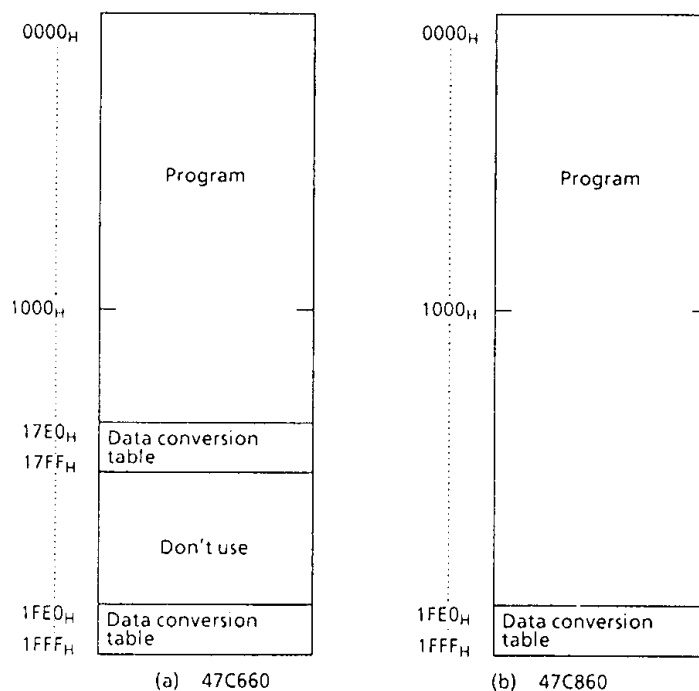


Figure 1-1. Program area

1.1.2 Data Memory

The 47P860 has two built-in 256 × 4-bit data memory banks (DMB0, DMB1).

When using the 47P860 as a 47C660 evaluator, do not write data to address 80H and following, even though the DMB1 addresses are 00~FFH. There is no necessity to take into consideration a special common function area because one is built in DMB0.

1.1.3 Input/Output Circuitry

- (1) Control pins
This is the same as for the 47C660/860 except that there is no built-in pull-down resistance for the TEST pin.
- (2) I/O Ports
The input/output circuit of the 47P860 is the same as I/O code IA of the 47C660/860. External resistance, for example, is required when using as evaluator of other I/O codes (IB, IC), (Refer to Figure 1.2)

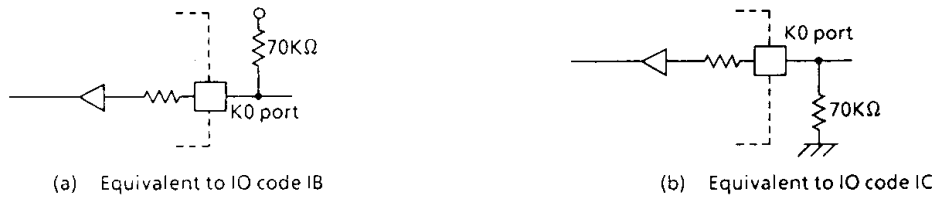


Figure 1-2. I/O code and external circuitry

1.2 PROM mode

The PROM mode is set by setting the $\overline{\text{RESET}}$, $\overline{\text{HOLD}}$, K00 and K01 pins to the "L" level. The PROM mode can be used as a general-purpose PROM writer for program writing and verification. (A high-speed program mode is used set the ROM type the same as for the TMM 2764D.)

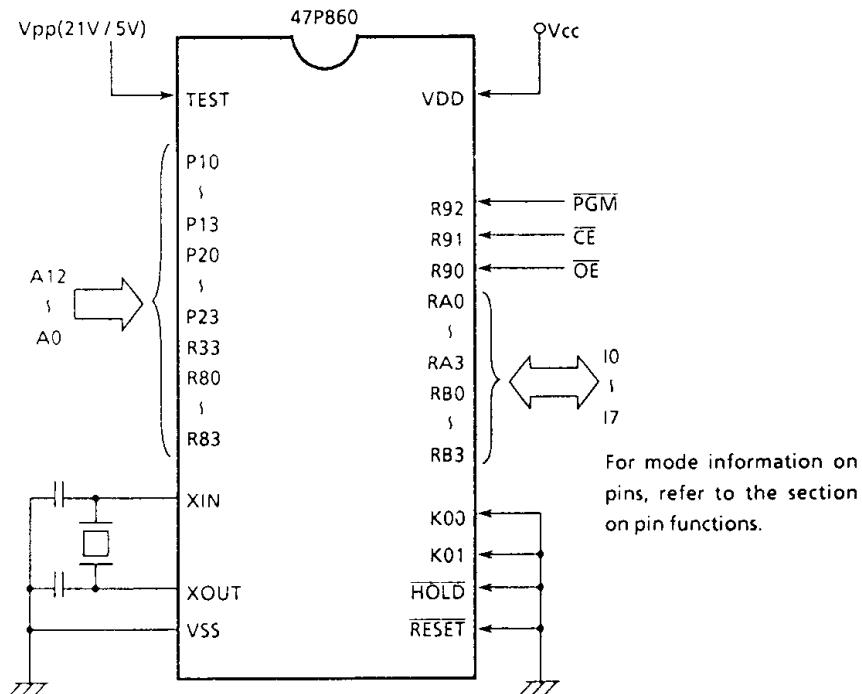


Figure 1-3. Setting for PROM mode

An adapter socket is available for connecting a PROM writer.

- BM1102 : TMP47P860N
- BM1109 : TMP47P860F

1.2.1 High Speed Programming Mode

The device is set up in the high speed programming mode when the programming voltage (21.0V) is applied to the Vpp pin with Vcc = 6V and PGM = VIH4. The programming is achieved by applying a single TTL low level 1 msec, pulse the PGM input after addresses and data are stable. Then the programmed data is verified by using Program Verify mode. If the programmed data is not correct, another programmed pulse of 1 msec is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 15 times) After correctly programming the selected address, one additional program pulse with pulse width 4 times that needed for programming is applied. When programming has been completed, the data in all addresses should be verified with Vcc = Vpp = 5V.

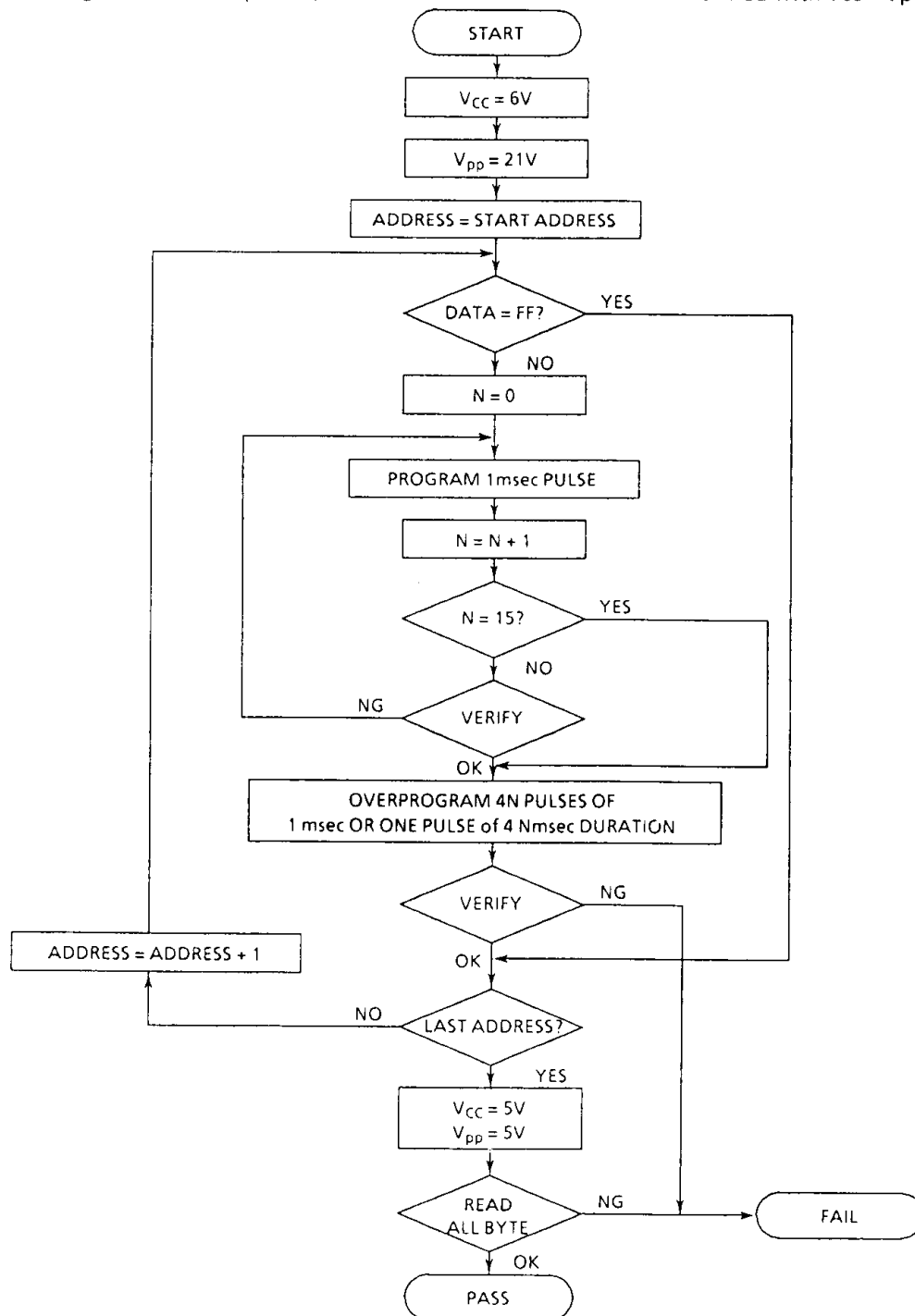


Figure1-4. FLOW CHART

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS ($V_{SS} = 0V$)

PARAMETER	SYMBOL	PINS	RATING	UNIT
Supply Voltage	V_{DD}		- 0.3 to 7	V
Program Voltage	V_{PP}	TEST / VPP pin	- 0.3 to 22.0	V
Input Voltage	V_{IN}		- 0.3 to $V_{DD} + 0.3$	V
Output Voltage	V_{OUT1}	Ports R4, R5, R7, push-pull	- 0.3 to $V_{DD} + 0.3$	V
	V_{OUT2}	Ports P1, P2, R6, R8, R9	- 0.3 to 10	
Output (Per 1 pin)	I_{OUT1}	Port R	3.2	mA
	I_{OUT2}	Ports P1, P2	30	
	I_{OUT2}	Ports P0, P3	15	
Output Current (Total)	ΣI_{OUT1}	Ports P0, P1	120	mA
	ΣI_{OUT2}	Ports P2, P3	120	
Power Dissipation	PD		600	mW
Soldering Temperature (time)	T_{sld}		260 (10sec)	°C
Storage Temperature	T_{stg}		- 55 to 125	°C
Operating Temperature	T_{opr}		- 40 to 70	°C

RECOMMENDED OPERATING CONDITIONS ($V_{SS} = 0V$, $T_{opr} = -40$ to $70^{\circ}C$)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}		in the Normal mode	4.5	6.0	V
			in the SLOW mode			
			in the HOLD mode	2.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input	$V_{DD} \geq 4.5V$	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis Input				
	V_{IH3}		$V_{DD} < 4.5V$	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Hysteresis Input	$V_{DD} \geq 4.5V$	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis Input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5V$	$V_{DD} \times 0.1$		
Clock Frequency	f_c		High-freq.clock	0.4	6.0	MHz
	f_s		Low-freq.clock	30	34	KHz

Note. Input Voltage V_{IH3} , V_{IL3} : in the SLOW mode or HOLD mode

D.C. CHARACTERISTICS (VSS = 0V, T_{opr} = -40 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V _{HS}	Hysteresis input		—	0.7	—	V
Input Current	I _{IN1}	port K0, TEST, RESET, HOLD	V _{DD} = 5.5V	—	—	± 2	μA
	I _{IN2}	ports R (open-drain)	V _{IN} = 5.5V / 0V				
Input Resistance	R _{IN2}	RESET		100	220	450	kΩ
Low Level Input Current	I _{IL}	ports R (push-pull)	V _{DD} = 5.5V, V _{IN} = 0.4V	—	—	-2	mA
Output Leakage Current	I _{LO}	ports R (open drain)	V _{DD} = 5.5V, V _{OUT} = 5.5V	—	—	2	μA
Output Level High Voltage	V _{OH}	push-pull ports	V _{DD} = 4.5V, I _{OH} = -200μA	2.4	—	—	V
Output Level Low Voltage	V _{OL}	Except XOUT, P ports	V _{DD} = 4.5V, I _{OL} = 1.6mA	—	—	0.4	
Low Level Output Current	I _{OL2}	ports P1, P2	V _{DD} = 4.5V, V _{OL} = 1.0V	—	20	—	mA
	I _{OL3}	ports P0, P3		—	7	—	
Supply Current (in the Nomal mode)	I _{DD}		V _{DD} = 5.5V f _c = 4MHz	—	5	10	mA
Supply Current (in the SLOW mode)	I _{DDS}		V _{DD} = 5.0V f _s = 32.768KHz	—	5	8	mA
Supply Current (in the HOLD mode)	I _{DDH}		V _{DD} = 5.5V	—	0.5	10	μA

Note 1. Typ. values show those at T_{opr} = 25°C, V_{DD} = 5V.

Note 2. Input Current I_{IN1}; The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.

Note 3. I_{DD}, I_{DDH}; V_{IN} = 5.3V / 0.2V

The K0 port is opened when the input resistor is contained.

The voltage applied to the R port is within the valid range.

I_{DDS}; V_{IN} = 2.8V / 0.2V, low frequency clock is only oscillated (connecting XTIN, XTOUT).

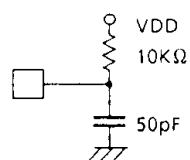
A / D CONVERSION CHARACTERISTICS (T_{opr} = -40 to 70°C)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Analog Reference	V _{AREF}		V _{DD} - 1.5	—	V _{DD}	V
	V _{ASS}		V _{SS}	—	1.5	
Analog Reference Voltage Range	ΔV _{AREF}	V _{AREF} - V _{ASS}	2.5	—	—	V
Analog input Voltage	V _{AIN}		V _{ASS}	—	V _{AREF}	V
Analog Supply Current	I _{REF}		—	0.5	1.0	mA
Nonlinearity Error		V _{DD} = 5.0V, V _{SS} = 0.0V	—	—	± 1	LSB
Zero point Error			—	—	± 1	
Full scale Error			—	—	± 1	
Total Error			—	—	± 2	

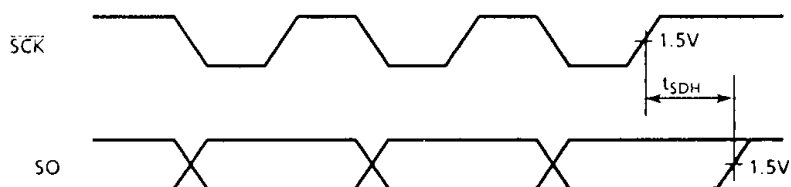
A.C. CHARACTERISTICS ($V_{SS} = 0V$, $V_{DD} = 4.5$ to $6.0V$, $T_{opr} = -40$ to $70^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}	in the Normal mode	1.9	-	20	μs
		in the SLOW mode	235	-	267	
High level Clock Pulse Width	t_{WCH}	For external clock operation	80	-	-	ns
Low level Clock Pulse Width	t_{WCL}					
A / D Conversion Sampling Time	t_{AIN}	$f_c = 4MHz$	-	2	-	μs
Shift Data Hold Time	t_{SDH}		$0.5t_{cy} - 300$	-	-	ns

Note. Shift data Hold Time:
External circuit for \overline{SCK} pin and SO pin



Serial port (completion of transmission)



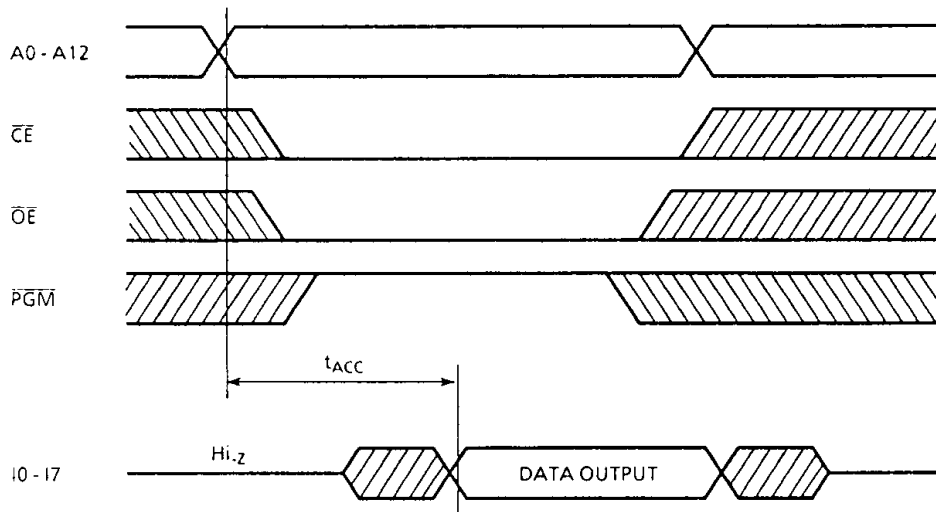
RECOMMENDED OSCILLATING CONDITIONS ($V_{SS} = 0V$, $V_{DD} = 4.5$ to $6.0V$, $T_{opr} = -40$ to $70^{\circ}C$)

Recommended oscillating conditions of the 47P860 are equal to the 47C860's.

DC/AC CHARACTERISTICS ($V_{SS} = 0V$)

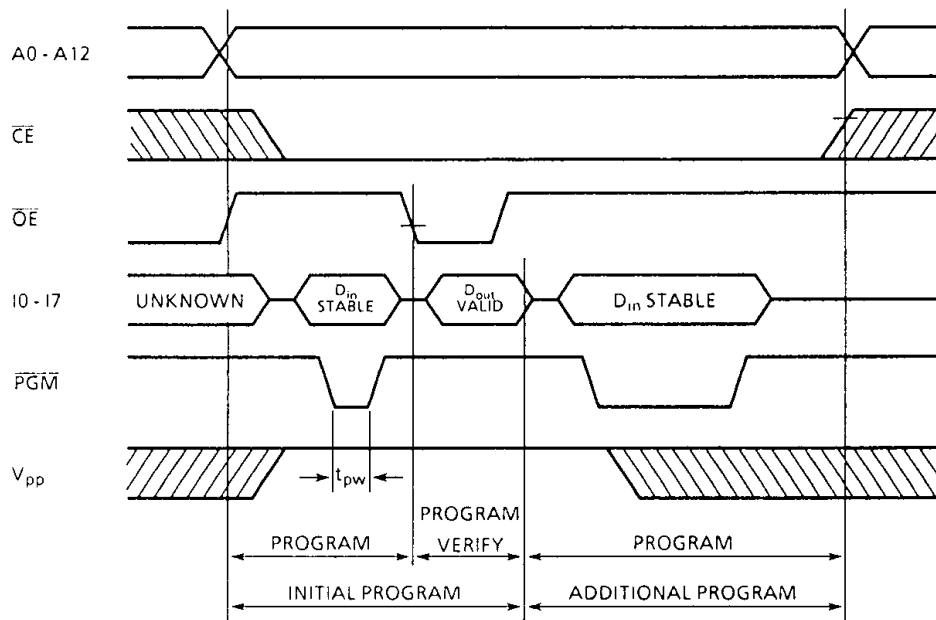
(1) Read Operation

PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Output Level High Voltage	V_{IH4}		$V_{CC} \times 0.7$	-	V_{CC}	V
Output Level Low Voltage	V_{IL4}		0	-	$V_{CC} \times 0.1$	V
Supply Voltage	V_{CC}		4.75	-	6.0	V
Programming Voltage	V_{PP}					
Address Access Time	t_{ACC}	$V_{CC} = 5.0 \pm 0.25V$	0	-	350	ns



(2) High Speed Programming Operation

PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Input High Voltage	V_{IH4}		$V_{CC} \times 0.7$	-	V_{CC}	V
Input Low Voltage	V_{IL4}		0	-	$V_{CC} \times 0.1$	V
Supply Voltage	V_{CC}		4.75	-	6.0	V
V_{PP} Power Supply Voltage	V_{PP}		20.5	21.0	21.5	V
Programming Pulse Width	t_{PW}	$V_{CC} = 6.0 \pm 0.25V$	0.95	1.0	1.05	ms



※ Difference compared with the 47C860
 The 47P860 is different from the 47C860 with respect to the following spec points.

PARAMETER	SYMBOL	CONDITION	TMP47C860			TMP47P860			UNIT
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply Voltage	VDD	in the Normal operation	4.5	—	6.0	4.5	—	6.0	V
		in the SLOW operation	2.7	—					
Supply Current	IDD	in the Normal operation	—	3	6	—	5	10	mA
	IDDS	in the SLOW operation	—	30μA (VDD = 3V)	T.B.D	—	5mA (VDD = 5V)	8mA (VDD = 5V)	—

Note: Be fixed low level at MCU mode because of TEST pin does not have pull-down resistor.

TYPICAL CHARACTERISTICS

