CMOS 4-BIT MICROCONTROLLER

TMP47C662N, TMP47C862N

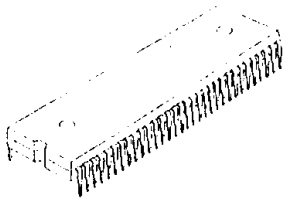
The 47C662/862 have extended I/O ports, A/D converter, programmable pulse generator, and high breakdown voltage outputs based on the TLCS-470 series.

PART No.	ROM	RAM	RACKAGE
TMP47C662N	6144 x 8-bit	384 x 4-bit	SDIP64
TMP47C862N	8192 x 8-bit	512 x 4-bit	

FEATURES

- ◆4-bit single chip microcomputer
- ◆Instruction execution time: 1.3μs(at 6MHz), 244μs (at 32.8KHz)
- ◆92 basic instructions
- ◆Table look-up instructions
- ◆5-bit to 8-bit data conversion instruction
- ◆Subroutine nesting: 15 levels max.
- ◆6 interrupt sources (External: 2, Internal: 4)
  All sources have independent latches each, and multiple interrupt control is available.
- ◆I/O port (55 pins)
  - Input 2 ports 5 pins
  - Output 1 port 3 pins
  - I/O 12 ports 47 pins
- ◆Interval Timer
- ◆Two 12-bit Timer/Counters
  Timer, event counter,and pulse width measurement mode
- ◆Watchdog Timer
- ◆Serial Interface with 8-bit buffer
  - Simultaneous transmission and reception capability
  - 8/4-bit transfer, external/internal clock, and leading/trailing edge shift mode
- ◆Two 12-bit Programmable Pulse Generator
  One-shot/continuous output, external/internal trigger, rising/falling edge trigger (external) mode
- ◆8-bit successive approximate type A/D converter
  - With sample and hold
  - 8 analog inputs
  - Conversion time : 32 μs(at 6 MHz)
- ◆Remote control signal pre-processing capability
- ◆High current outputs
  LED direct drive capability (typ. 20mA × 4 bits)
- ◆High breakdown voltage outputs
  VFT direct drive capability (max.42V x 27 bits)
- ◆Dual-clock operation
  High-speed/Low-power-consumption operating mode
- ◆Hold function
  Battery/Capacitor back-up
- ◆Real Time Emulator : BM47C862

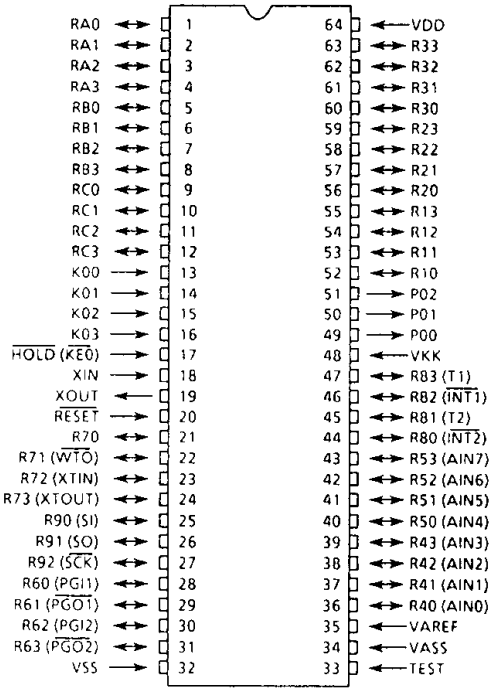
SDIP64



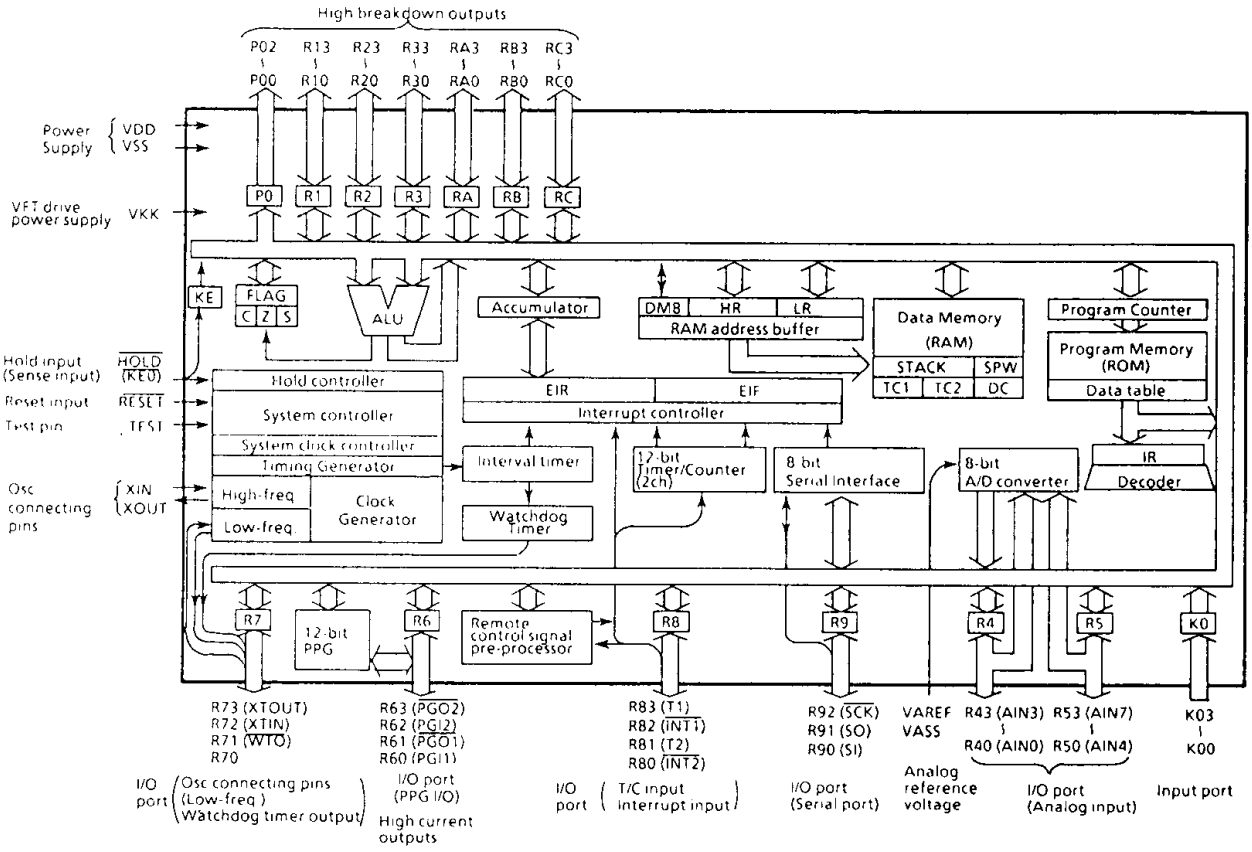
TMP47C662N
TMP47C862N

PIN ASSIGNMENT (TOP VIEW)

SDIP64



BLOCK DIAGRAM



PIN FUNCTION

PIN NAME	Input/Output	FUNCTIONS	
K03 - K00	Input	4-bit input port	
R53 (AIN7) - R40 (AIN0)	I/O (Input)	4-bit I/O port with latch. When using as input port, watchdog timer output, analog input, PPG (programmable pulse generator) output, or PPG trigger input, the latch must be set to "1". Set to Dual-clock operating mode, when R73, R72 pin use as clock generator. Can be set, cleared, and tested for each bit as specified by L register indirect addressing bit manipulation instructions.	A/Dconverter analog input
R63 ($\overline{PGO2}$)	I/O (Output)		PPG2 output
R62 (PGI2)	I/O (Input)		PPG2 external trigger input
R61 ($\overline{PGO1}$)	I/O (Output)		PPG1 output
R60 (PGI1)	I/O (Input)		PPG1 external trigger input
R73 (XTOUT)	I/O (Output)		Resonator connecting pin (Low-freq.). For inputting external clock, XTIN is used and XTOUT is opened.
R72 (XTIN)	I/O (Input)		
R71 ($\overline{WTO}$)	I/O (Output)		Watchdog timer output
R70	I/O		
R83 (T1)	I/O (Input)	4-bit I/O port with latch. When using as input port, external interrupt input pin, or timer/counter external input pin, the latch must be set to "1".	Timer/Counter 1 external input
R82 ($\overline{INT1}$)			External interrupt 1 input
R81 (T2)			Timer/Counter 2 external input
R80 ($\overline{INT2}$)			External interrupt 2 or REMO-CON input
R92 ($\overline{SCK}$)	I/O (I/O)	3-bit I/O port with latch. When using as input port or serial port, the latch must be set to "1".	Serial clock I/O
R91 (SO)	I/O (Output)		Serial data output
R90 (SI)	I/O (Input)		Serial data input
P02 - P00	Output	3-bit high breakdown voltage output port with latch	
R13 - R10	I/O	4-bit high breakdown voltage I/O port with latch. 8-bit data are output by the 5-bit to 8-bit data conversion instruction [OUTB @HL]. When using as input port, the latch must be cleared to "0".	
R23 - R20			
R33 - R30	I/O	4-bit high breadown voltage I/O port with latch. When using as input port, the latch must be cleared to "0".	
RA3 - RA0			
RB3 - RB0			
RC3 - RC0			
XIN, XOUT	Input, Output	Resonator connecting pin (High-frequency). For inputting external clock, XIN is used and XOUT is opened.	
$\overline{RESET}$	Input	Reset signal input	
$\overline{HOLD}$ ($\overline{KE0}$)	Input (Input)	Hold request/release signal input	Sence input
TEST	Input	Test pin for out-going test. Be opened or fixed to low level.	
VDD, VSS	Power supply	+ 5V, 0V (GND)	
VAREF, VASS		A/D converter analog reference voltage	
VKK		VFT drive power supply	

OPERATIONAL DESCRIPTION

Concerning the 47C662/862, the hardware configuration and operation are described.
As the description include mainly differences from the 47C660/860, the technical data sheets for the 47C660/860 shall also be referred to.

1. SYSTEM CONFIGURATION

(1) I/O Ports
(2) Programmable Pulse Generator

2. PERIPHERAL HARDWARE FUNCTION

2.1 I/O Ports

47C662/862 have 15 I/O ports (55pins) each as follows:

① K0	;	4-bit input
② P0	;	3-bit output
③ R1, R2	;	4-bit input/output
④ R4, R5	;	4-bit input/output (shared with A/D converter analog inputs)
⑤ R6	;	4-bit input/output (shared with programmable pulse generator I/O)
⑥ R7	;	4-bit input/output (shared with the low-frequency resonator connecting pins and the watchdog timer output)
⑦ R8	;	4-bit input/output (shared with external interrupt request input and timer/counter input)
⑧ R9	;	3-bit input/output (shared with serial port)
⑨ R3, RA, RB, RC	;	4-bit input/output
⑩ KE	;	1-bit sense input (shared with hold request/release signal input)

This section describes ports of ②, ③, ⑤ and ⑨ which are changed from the 47C660/860.
Table 2-1 lists the port address assignments and the I/O instructions that can access the ports.

(1) Ports P0 (P03-P00)

Ports P0 is 3-bit high breakdown voltage output ports with latch. The latch is initialized to "0" during reset.

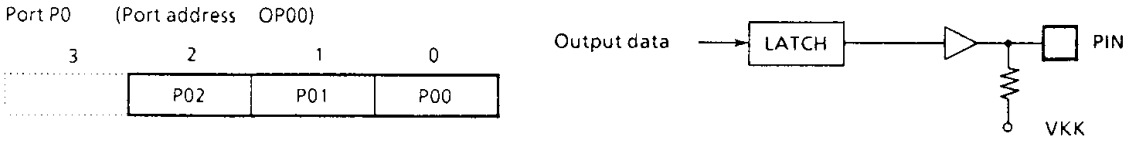


Figure 2-1. Ports P0

(2) Ports R1 (R13~R10), R2 (R23~R20)

The 4-bit high breakdown voltage I/O ports with latch, which can directly Vacume Fuolrescent Tubes (VFT) . The latch should be cleared to "0" when used as an inuput port. The latch is initialized to "0" during reset.

8-bit data can be output through ports R1 and R2 by using the 5-bit to 8-bit data conversion instruction; therefore, ports can also be effectively utilized as segment output pins.

Ports R2 (Port address OP02 / IP02)

3	2	1	0
R23	R22	R21	R20

Ports R1 (Port address OP01 / IP01)

3	2	1	0
R13	R12	R11	R10

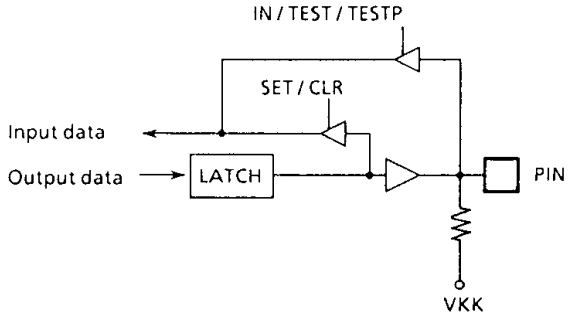


Figure 2-2. Ports R1, R2

(3) Ports R3 (R33~R30), RA (RA3~RA0), RB (RB3~RB0), RC (RC3~RB0)

The 4-bit high breakdown voltage I/O ports with latch, which can directly Vacume Fluorescent Tubes (VFT) . The latch should be cleared to "0" when used as an inuput port. The latch is initialized to "0" during reset.

Port R* (Port address OP0* / IP0*)

3	2	1	0
R*3	R*2	R*1	R*0

* ; 3, A, B, C

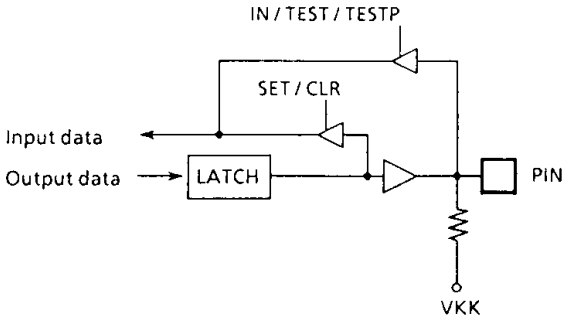


Figure2-3. Ports R3, RA, RB, RC

※ Connecting VKK (power supply for driving Vacume Fluorescent Tube) pin.

The 27 pins of the R1, R2, R3, RA, RB, RC and P0 ports are P-channel open drain construction with pulldown resistor. Each pin is connected to a VKK pin via a pulldown resistor (TYP. 80kΩ) . Thus, Vacume Fluorescent Tubes (VFT) can be driven by applying a negative (–) voltage (– 35V max) to the VKK pin, without using external resistor.

(4) Port R6 (R63~R60)

Port R6 is 4 bit I/O ports with latch shared with the PPG (programmable pulse generator) I/O ports. When used as an input ports or PPG I/O, the latch should be set to "1". The latch is initialized to "1"during reset.

Port R6 (Port address OP06 / IP06)

3	2	1	0
R63 ($\overline{PGO2}$)	R62 (PGI2)	R61 ($\overline{PGO1}$)	R60 (PGI1)

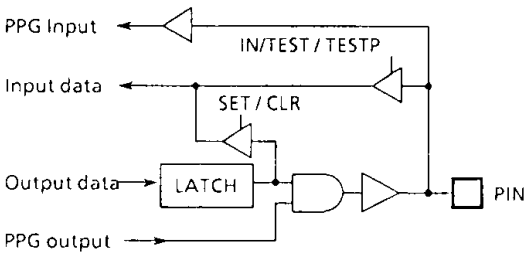


Figure 2-4. Port R6

Port address (**)	Port		Input/Output instruction						
	Input (IP**)	Output (OP**)	IN %p, A IN %p, @HL	OUT A, %p OUT @HL, %p	OUT #k, %p	OUTB @HL	SET %p, b CLR %p, b	TEST %p, b TESTP %p, b	SET @L CLR @L TEST @L
00_H	K0 input port	P0 output port	○	○	○	–	–	○	–
01	R1 input port	R1 output port	○	○	○	○ (Note2)	○	○	–
02	R2 input port	R2 output port	○	○	○	○ (Note2)	○	○	–
03	R3 input port	R3 output port	○	○	○	–	○	○	–
04	R4 input port (Analog input)	R4 output port	○	○	○	–	○	○	○
05	R5 input port (Analog input)	R5 output port	○	○	○	–	○	○	○
06	R6 input port (PPG input)	R6 output port (PPG output)	○	○	○	–	○	○	○
07	R7 input port	R7 output port	○	○	○	–	○	○	○
08	R8 input port	R8 output port	○	○	○	–	○	○	–
09	R9 input port	R9 output port	○	○	○	–	○	○	–
0A	RA input port	RA output port	○	○	○	–	○	○	–
0B	RB input port	RB output port	○	○	○	–	○	○	–
0C	RC input port	RC output port	○	○	○	–	○	○	–
0D	REMO-CON count value	REMO-CON offset value	○	○	○	–	–	–	–
0E	Status input (Note 4)	REMO-CON control	○	○	○	–	–	○	–
0F	Serial receive buffer	Serial transmit buffer	○	○	○	–	–	–	–
10_H	——	Hold operating mode control	–	○	–	–	–	–	–
11	——	——	–	–	–	–	–	–	–
12	A / D coverted value	A / D analog input selector	○	○	–	–	–	–	–
13	A / D status input	A / D start register	○	○	–	–	–	–	–
14	——	——	–	–	–	–	–	–	–
15	——	Watchdog timer control	–	○	–	–	–	–	–
16	——	System clock control	–	○	–	–	–	–	–
17	——	PPG pulse data register	–	○	–	–	–	–	–
18	PPG Status input	PPG control	○	○	–	–	–	–	–
19	——	Interval Timer interrupt control	–	○	–	–	–	–	–
1A	——	PPG1 mode control	–	○	–	–	–	–	–
1B	——	PPG2 mode control	–	○	–	–	–	–	–
1C	——	Timer/Counter 1 control	–	○	–	–	–	–	–
1D	——	Timer/Counter 2 control	–	○	–	–	–	–	–
1E	——	Serial interface control 1	–	○	–	–	–	–	–
1F	——	Serial interface control 2	–	○	–	–	–	–	–

Note 1 : "——" means the reserved state. Unavailable for the user programs.

Note 2 : The 5-bit to 8-bit data conversion instruction [OUTB @HL], automatic access to ports P1 and P2.

Note 3 : As concerns the port address "00", IN and TEST instructions operate port K0, and OUT instruction operates port P0.

Note 4 : The status input of serial interface, clock generator, and $\overline{HOLD}$ ($\overline{KE0}$) pin.

Table 2-1. Port Address Assignments and Available I/O Instructions

2.2 Programmable Pulse Generator (PPG)

The 47C662/862 contains 2 channel pulse generators (PPG) available to set the output pulse delay and width independently with 12-bit resolution for each channel. One-shot or continuous pulse output can be selected and output pulse can be synchronized by external trigger input. PPG1 outputs to the $\overline{PG01}$ pin and PPG2 outputs to the $\overline{PG02}$ pin. External triggers are input to pins PGI1 and PGI2. Pins PGI1 and PGI2 can also be used as normal input/output ports in the internal clock mode.

2.2.1 Circuit configuration

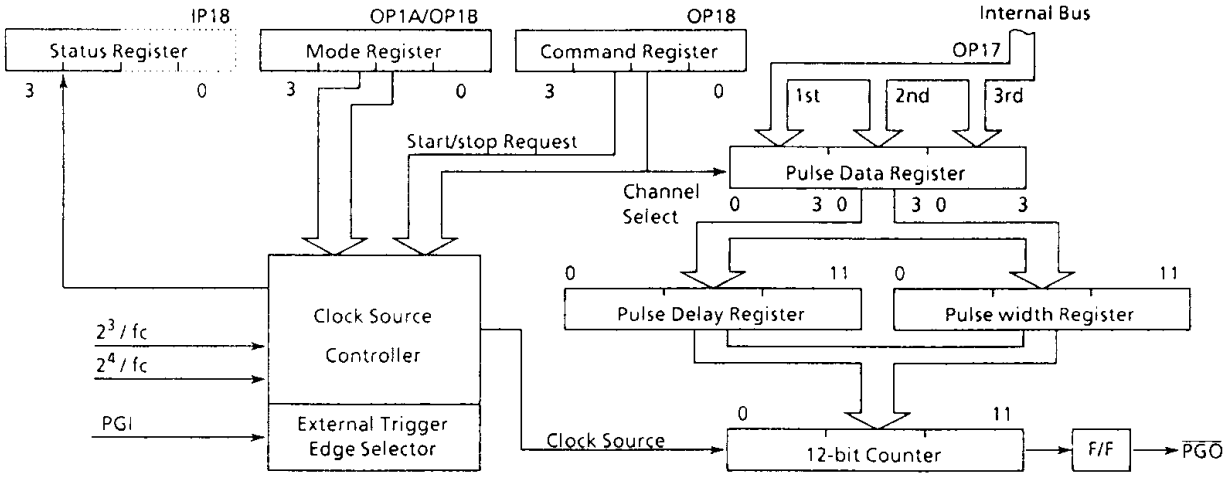


Figure 2-5. Programmable Pulse Generator (2 channels)

2.2.2 PPG Control

PPG is controlled by the data register (OP17), command register (OP18), mode registers (OP1A, OP1B) and status register (IP18).

(1) Pulse data register

Both PPG1 and PPG2 have a pulse delay register (PDR) and pulse width register (PWR) to which values set to the pulse data register (OP17) are transferred. The pulse data register is set by accessing OP17 three times: the lower 4 bits the first time, the middle 4 bits the second time and the higher 4 bits the last time. Any attempt to access OP17 four or more times is ignored.These pulse data are transferred to PDR and PWR by accessing the command register (OP18). The data transferred to PDR and PWR are alternately preset as 12-bit count preset data by 12-bit counter overflows; therefore, any output pulse width can be set at either "H" level or "L" level.

Example : Set PPG1 and PPG2 to the operating mode and set the value read from the RAM in the pulse data register and start both operating at the same time.

Main routine

```
LD      A, #1111B
OUT     A, %OP1A
LD      A, #0000B
OUT     A, %OP1B
CALL    PDW
LD      A, #1100B
OUT     A, %OP18
CALL    PWW
LD      A, #1101B
OUT     A, %OP18
LD      A, #1111B
OUT     A, %OP18
:
```

Subroutine (writting pulse data)

```
PDW :   :
        :
        ; DELAY DATA SET
        LD      HL, #20H
        OUT     @HL, %OP17
        INC     L
        OUT     @HL, %OP17
        INC     L
        OUT     @HL, %OP17
        :
        :
        RET

PWW :   :
        :
        ; WIDTH DATA SET
        LD      HL, #23H
        OUT     @HL, %OP17
        INC     L
        OUT     @HL, %OP17
        INC     L
        OUT     @HL, %OP17
        :
        :
        RET
```

(2) PPG Command Register

The higher 2 bits of the command register (OP18) are used as the PPG1 and PPG2 selectors. The two channels of PPG can be controlled either simultaneously or independently by setting/clearing SPG1 and SPG2. Pulse data transfer requests and operating start/stop requests are accepted by setting "1" to SPG1 and SPG2. For example, PPG2 can be controlled without influencing PPG1 output by operating PPG1 and then clearing SPG1 to "0". Table 2-2 shows several examples of OP18 settings.

Note : pulse data transfer requests are disabled each time pulse data are transferred to PDR or PWR, so OP17 must be accessed each time. Transfer requests are accepted only after accessing OP17 three times, even when it is not necessary to change the middle and higher 4 bits.

OP18 MSB			LSB	Operation
0	1	0	0	Data transfer to PDR of PPG1
1	1	0	1	Data transfer to PDR of PPG1 and 2 at the same time
1	0	1	1	Instruct output start PPG2 only
1	1	1	1	Instruct output start PPG1 and 2
0	1	1	0	Instruct output end PPG1 only

Table 2-2. Examples of OP18 settings

(3) PPG Mode Register

PPG1 is controlled by the OP1A mode register, PPG2 is controlled by the OP1B mode register, and each can be set independently.

A variety of pulses can be output by using different combinations of internal/external trigger and one-shot/continuous output.

a. Internal clock mode

Using the timing generator output as the count pulse, pulse output starts at the first rise after issueing a operation start request with command register (OP18). Only one cycle is output in the one-shot output mode and pulses are output until an operation stop request is accepted in the continuous output mode. Pulse output is started anew whenever an operation start request is accepted , even during pulse output.

PPG command register
(Port address : OP18 Initial value : 0000)

3	2	1	0
SPG2	SPG1	DEC	

SPG2 | Selects PPG2
0 : Not selected
1 : Selected

SPG1 | Selects PPG1
0 : Not selected
1 : Selected

DEC | PPG control
00 : Data transfer to PDR
01 : Data transfer to PWR
10 : Instruct pulse output end
11 : Instruct pulse output start

Figure 2-6. Command register

PPG1 mode register
(Port address : OP1A Initial value : 0000)

3	2	1	0
EPG1	EDG1	CTN1	CKR1

PPG2 mode register
(port address : OP1B Initial value : 0000)

3	2	1	0
EPG2	EDG2	CTN2	CKR2

EPG1 / 2 | Selects trigger mode
0 : Internal clock mode
1 : External trigger mode (input from PGI)

EDG1 / 2 | Selects External trigger edge | Note 1
0 : Trigger at the falling edge
1 : Trigger at the rising edge

Note 1. Only external trigger mode

CTN1 / 2 | Selects output mode
0 : One-shot pulse output
1 : Continuous pulse output

CKR1 / 2 | Count pulse rate
0 : 2^3 / fc [sec]
1 : 2^4 / fc

Figure 2-7. PPG mode register

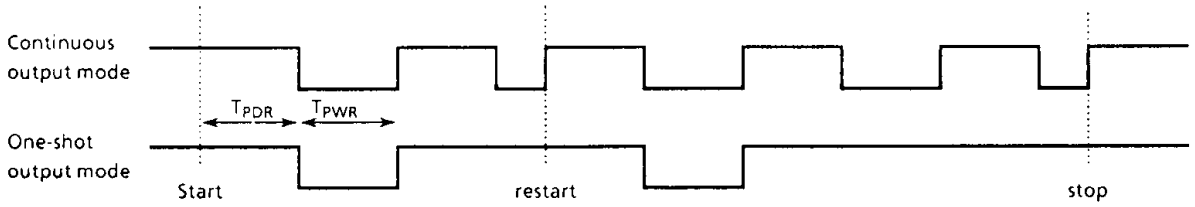


Figure 2-8. Internal clock mode

b. External trigger mode

The timing generator output is used as the count pulse and pulse output is synchronized with the external input (PGI). In the continuous mode, a pulse is output each time an external trigger edge is sensed. Trigger edges (rise or fall) can be selected with EDG of OP1A and OP1B.

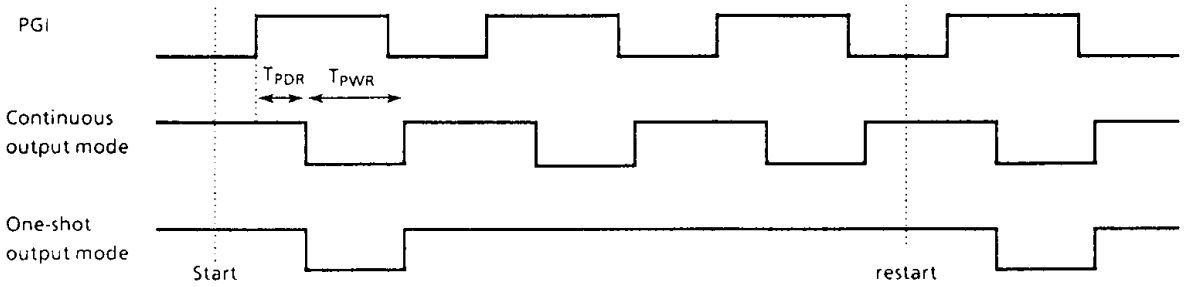


Figure 2-9. External trigger mode (at the rising edge)

c. Period of PPG output

The pulse width during "H" level output is determined by the PDR setting value and the pulse width during "L" level output is determined by the PWR setting value, as shown in Table 2-3; therefore, the basic period is T_{PDR} + T_{PWR} when T_{PDR} is "H" level width and T_{PWR} is "L" level width.

Count pulse rate	PDR, PWR setting value (HEX)	T_{PDR}, T_{PWR} (n = 0~4095)
2^3 / fc [sec]	0~FFF	(4096-n) × (2^3 / fc) [sec]
2^4 / fc	0~FFF	(4096-n) × (2^4 / fc)

Table 2-3. Output Pulse Width

(4) Operating status input

The PPG operating status can be monitored. "1" is read during pulse output by accessing IP18.

PPG status register
(Port address : IP18)

3	2	1	0
PGM2	PGM1		

PGM2	Monitors PPG2 output
0 :	Pulse output is terminated
1 :	Pulse output is in progress

PGM1	Monitors PPG1 output
0 :	Pulse output is terminated
1 :	Pulse output is in progress

Figure 2-10. PPG status register

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

PARAMETER	SYMBOL	PINS	RATING	UNIT
Supply Voltage	V_{DD}		− 0.5~7	V
Input Voltage	V_{IN}		− 0.3~V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	R7, XOUT	− 0.3~V_{DD} + 0.3	V
	V_{OUT2}	P0~P2, R6, R8, R9	− 0.3~10	
	V_{OUT3}	Source open drain pin	− 35~V_{DD} + 0.3	
Output Current (per 1 pin)	I_{OUT1}	R6	30	mA
	I_{OUT2}	R4, R5, R7-R9	3.2	
	I_{OUT3}	P0, R1, R2	− 12	
	I_{OUT4}	R3, RA, RB, RC	− 25	
Output Currnent (Total)	ΣI_{OUT1}	R6	120	mA
	ΣI_{OUT4}	R3, RA, RB, RC	− 100	
Power Dissipation [T_{opr} = 70°C]	PD		600	mW
Soldering Temperature (time)	T_{sld}		260 (10sec)	°C
Storage Temperature	T_{stg}		− 55~125	°C
Operating Temperature	T_{opr}		− 40~70	°C

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, T_{opr} = − 40~70°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}		In the Normal mode	4.5	6.0	V
			In the SLOW mode	2.7		
			In the HOLD mode	2.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input	$V_{DD} \geqq 4.5V$	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis Input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5V$	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Except Hysteresis Input	$V_{DD} \geqq 4.5V$	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis Input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5V$		$V_{DD} \times 0.1$	
Clock Frequency	fc	XIN, XOUT		0.4	6.0	MHz
	fs	XTIN, XTOUT		30.0	34.0	KHz

Note. : Input voltage V_{IH3}, V_{IL3} : in the SLOW or HOLD mode

D.C. CHARACTERISTICS

(V_{SS} = 0V, T_{opr} = −40~70°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		−	0.7	−	V
Input Current	I_{IN1}	K0, TEST, $\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5V, V_{IN} = 5.5V / 0V	−	−	±2	μA
	I_{IN2}	R ports (open drain)					
Input Resistance	R_{IN1}	K0 port with pull-up/pull-down		30	70	150	KΩ
	R_{IN2}	$\overline{RESET}$		100	220	450	
Pull-down resistance	R_K	source open drain	V_{DD} = 5.5V, V_{KK} = -30V	−	80	−	
Output Leakage Current	I_{LO1}	sink open drain	V_{DD} = 5.5V, V_{IN} = 5.5V	−	−	2	μA
	I_{LO2}	source open drain	V_{DD} = 5.5V, V_{OUT} = −32V	−	−	−2	
Output Level High Voltage	V_{OH}	P0, R1, R2	V_{DD} = 4.5V, I_{OH} = −5mA	2.4	−	−	V
Output Level Low Voltage	V_{OL}	R4, R5, R7-R9	V_{DD} = 4.5V, I_{OL} = 1.6mA	−	−	0.4	V
Output Level High Voltage	I_{OH}	R3, RA, RB, RC	V_{DD} = 4.5V, V_{OL} = 2.4V	−	-15	−	mA
Output Level Low Voltage	I_{OL}	R6	V_{DD} = 4.5V, V_{OL} = 1.0V	−	20	−	mA
Supply Current (in the Normal mode)	I_{DD}		V_{DD} = 5.5V, fc = 4MHz	−	3	6	mA
Supply Current (in the SLOW mode)	I_{DDS}		V_{DD} = 3.0V, fs = 32.768KHz	−	30	60	μA
Supply Current (in the HOLD mode)	I_{DDH}		V_{DD} = 5.5V	−	0.5	10	μA

Note 1. Typ. values show those at T_{opr} = 25°C, V_{DD} = 5V.

Note 2. Input Current I_{IN1} ;The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.

Note 3. Supply Current I_{DD}, I_{DDH} ; V_{IN} = 5.3V/0.2V
The K0 port is open when the input resistor is contained. The voltage applied to the R port is within the valid range.

Note 4. Supply Current I_{DDS} ; V_{IN} = 2.8V/0.2V
Low frequency clock is only osillated (connecting XTIN, XTOUT).

A / D CONVERSION CHARACTERISTICS

(T_{opr} = −40 to 70°C)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Analog Reference Voltage	V_{AREF}		V_{DD} − 1.5	−	V_{DD}	V
	V_{ASS}		V_{SS}	−	1.5	
Analog Reference Voltage Range	ΔV_{AREF}	V_{AREF} − V_{ASS}	2.5	−	−	V
Analog Input Voltage	V_{AIN}		V_{ASS}	−	V_{AREF}	V
Analog Supply Current	I_{REF}		−	0.5	1.0	mA
Nonlinearity Error		V_{DD} = 5.0V, V_{SS} = 0.0V V_{AREF} = 5.000V V_{ASS} = 0.000V	−	−	±1	LSB
Zero Point Error			−	−	±1	
Full Scale Error			−	−	±1	
Total Error			−	−	±2	

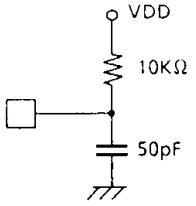
A. C. CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, T_{opr} = – 40 to 70°C)

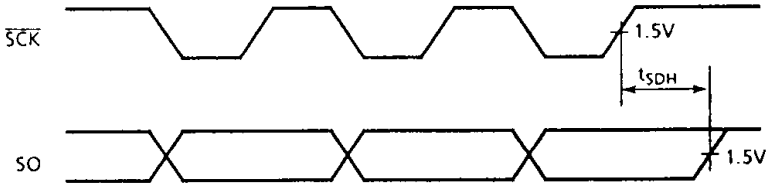
PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}	In the Normal mode	1.9	–	20	ns
		In the SLOW mode	235	–	267	
High level Clock pulse Width	t_{WCH}	External clock mode	80	–	–	ns
Low level Clock pulse Width	t_{WCL}					
A / D Sampling Time	t_{AIN}	fc = 4MHz	–	4	–	μs
Shift Data Hold Time	t_{SDH}		$0.5t_{cy}$ – 300	–	–	ns

Note. Shift Data Hold Time

External circuit for $\overline{SCK}$ pin and SO pin



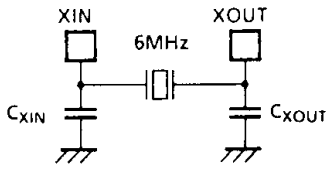
Serial port (completion of transmission)



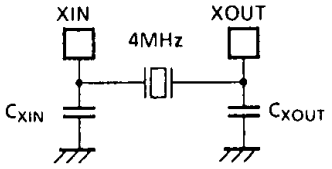
RECOMMENDED OSCILLATING CONDITIONS

(V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, T_{opr} = – 40 to 70°C)

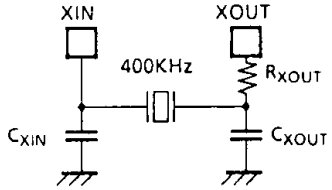
(1) 6MHz
Ceramic Resonator
CSA6.00MGU (MURATA) $C_{XIN} = C_{XOUT}$ = 30pF
KBR-6.00MS (KYOCERA) $C_{XIN} = C_{XOUT}$ = 30pF



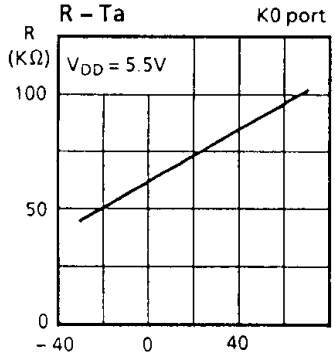
(2) 4MHz
Ceramic Resonator
CSA4.00MG (MURATA) $C_{XIN} = C_{XOUT}$ = 30pF
KBR-4.00MS (KYOCERA) $C_{XIN} = C_{XOUT}$ = 30pF
Crystal Oscillator
204B-6F 4.0000 (TOYOCOM) $C_{XIN} = C_{XOUT}$ = 20pF

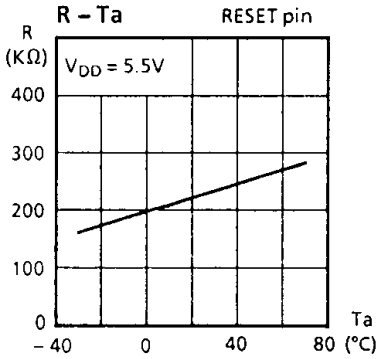


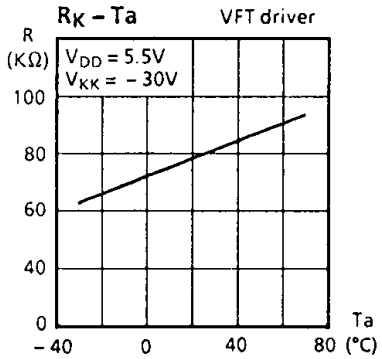
(3) 400KHz
Ceramic Resonator
CSB400B (MURATA) $C_{XIN} = C_{XOUT}$ = 220pF, R_{XOUT} = 6.8KΩ
KBR-400B (KYOCERA) $C_{XIN} = C_{XOUT}$ = 100pF, R_{XOUT} = 10KΩ

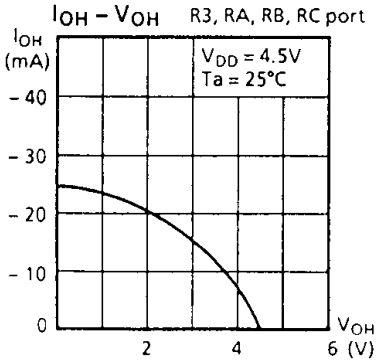


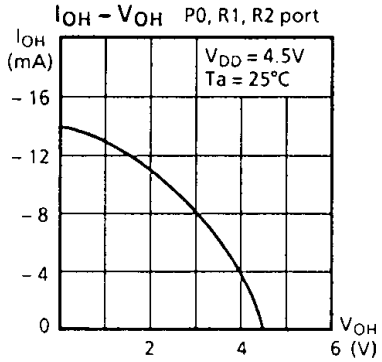
TYPICAL CHARACTERISTICS

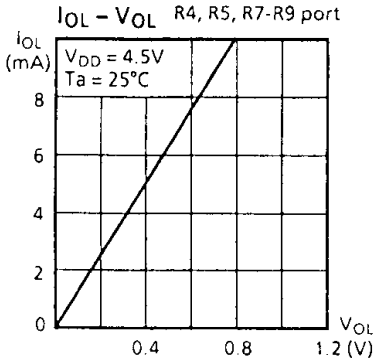


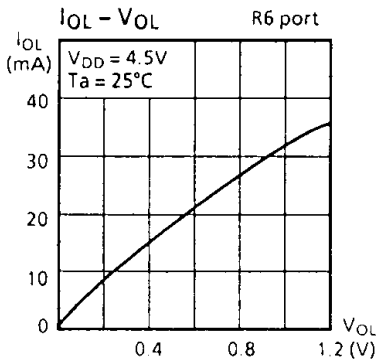


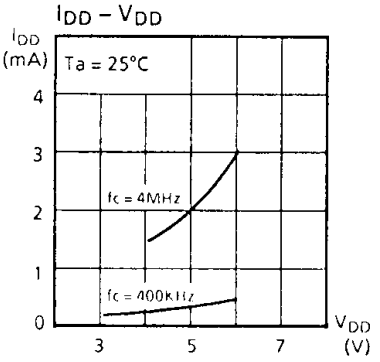


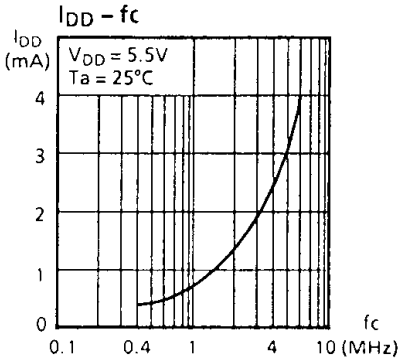












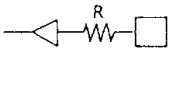
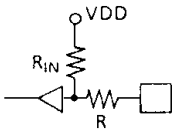
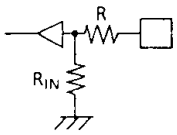
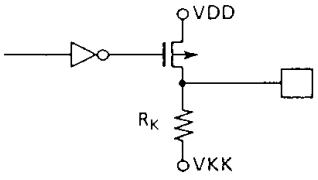
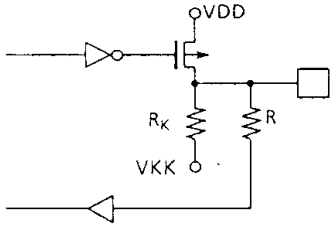
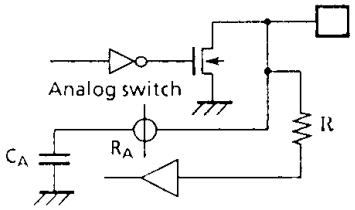
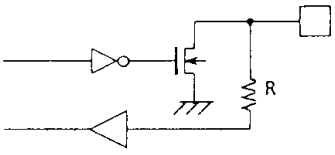
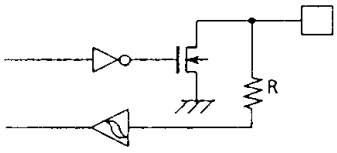
INPUT/OUTPUT CIRCUITRY

(1) Control pins

Input/Output circuitries of the 47C662/862 control pins are similar to the 47C660/860.

(2) I/O Ports

The input/output circuitries of the 47C662/862 I/O ports are shown as belows any one of the circuitries can be chosen by a code (IA~IC) by a code as a mast option.

PORT	I/O	INPUT/OUTPUT CIRCUT (CODE)			REMARKS
		IA	IB	IC	
K0	Input				Contained pull-up/pull-down resistor R_{IN} = 70KΩ (typ.) R = 1KΩ (typ.)
P0	Output				Source open drain output Initial "Hi-Z" High voltage break down R_K = 80KΩ (typ.)
R1 R2 R3 RA RB RC	I/O				Source open drain output Initial "Hi-Z" High voltage break down R_K = 80KΩ (typ.) R = 1KΩ (typ.)
R4 R5	Output				Sink open drain output Initial "Hi-Z" R = 1KΩ (typ.) Analog input R_A = 5KΩ (typ.) C_A = 12pF (typ.)
R7	I/O				Sink open drain output Initial "Hi-Z" R = 1KΩ (typ.)
R6 R8 R9	I/O				Sink open drain output Initial "Hi-Z" High current (R6) I_{OL} = 20mA (typ.) Hysteresis input R = 1KΩ (typ.)