CMOS 4-BIT MICROCONTOROLLER

TMP47C221ADF, TMP47C421ADF

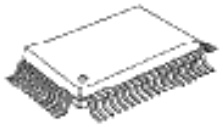
The 47C221A/421A is a high speed and high performance 4-bit single chip microcomputer with LCD drive based on the TLCS-47 CMOS series with LCD driver.

PART No.	ROM	RAM	PACKAGE	OTP
TMP47C221ADF	2048 × 8-bit	192 × 4-bit	QFP64-P-1420-1.00A	TMP47P421ADF
TMP47C421ADF	4096 × 8-bit	256 × 4-bit		

FEATURES

- ◆4-bit single chip microcomputer
- ◆Instruction execution time : 1.9 μs (at 4.2 MHz)
- ◆89 basic instructions
  - Table look-up instructions
- ◆Subroutine nesting : 15 levels max.
- ◆6 interrupt sources (External : 2, Internal : 4)
  All sources have independent latches each, and multiple interrupt control is available.
- ◆I/O port (28 pins)
  - Input 2 ports 5 pins
  - I/O 6 ports 23 pins
- ◆Interval Timer
- ◆Two 12-bit Timer / Counters
  Timer, event counter, and pulse width measurement mode
- ◆Serial Interface with 4-bit buffer
  External / internal clock, and leading / trailing edge shift mode
- ◆LCD driver
  - LCD direct drive is abailable (Max. 12-digit display at 1/4 duty LCD)
  - 1/4, 1/3, 1/2 duties or static drive are programmably selectable.
- ◆Hold function
  Battery / Capacitor back-up
- ◆Real Time Emulator : BM4721A + BM4723A

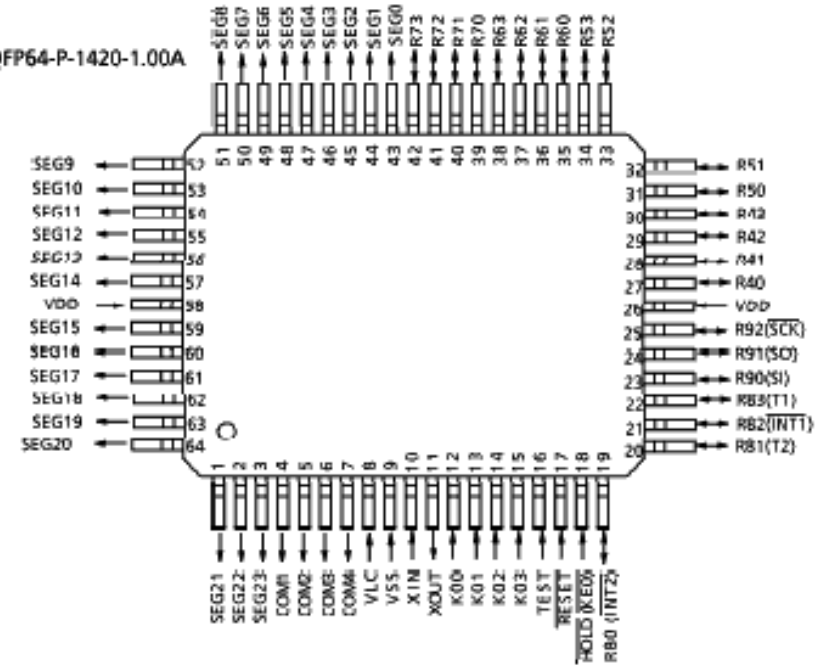
QFP64-P1420-1.00A



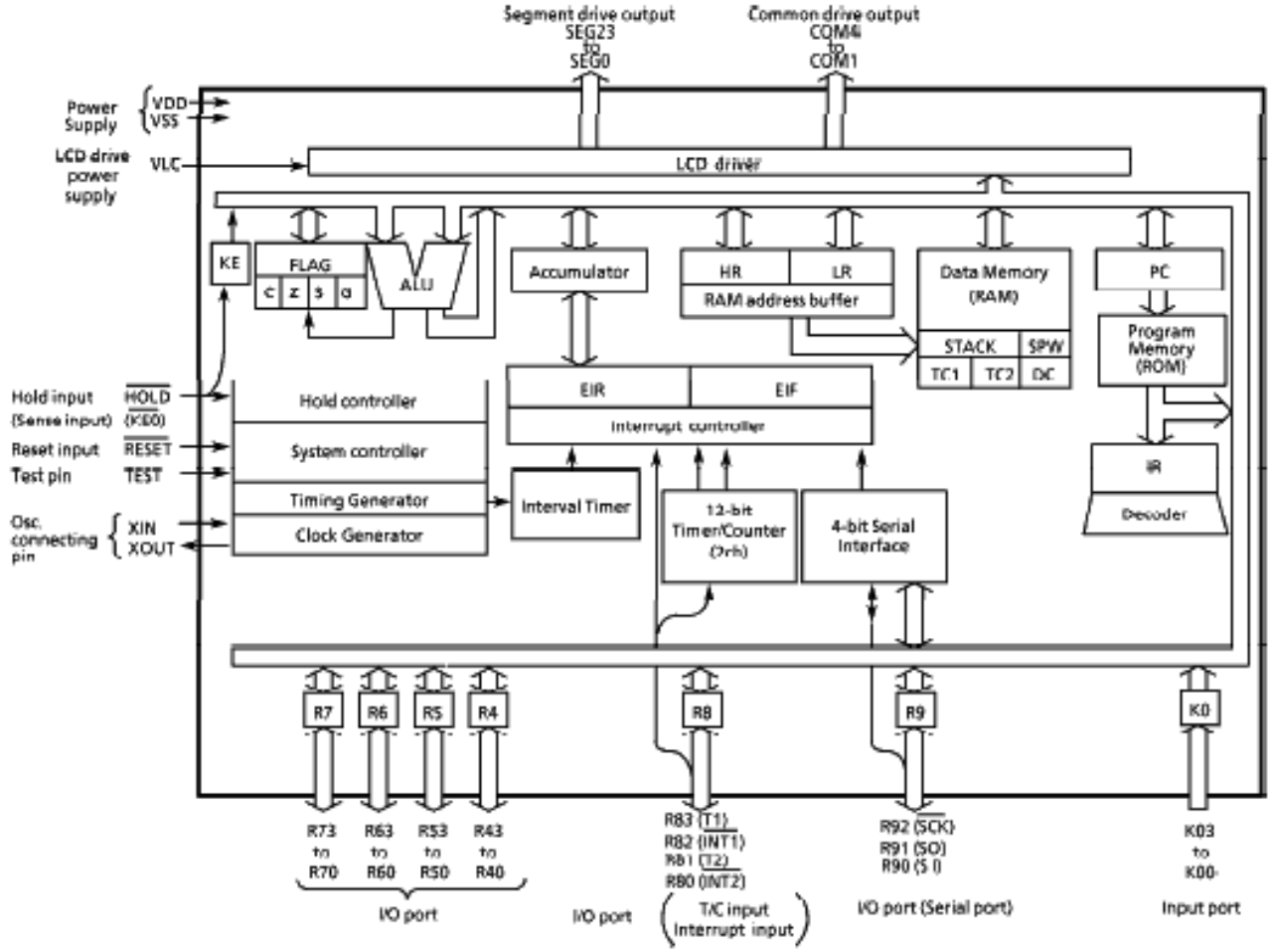
TMP47C221ADF
TMP47C421ADF
TMP47P421ADF

PIN ASSIGNMENT (TOP VIEW)

QFP64-P-1420-1.00A



BLOCK DIAGRAM



PIN FUNCTION

PIN NAME	Input/Output	FUNCTIONS	
K03 to K00	Input	4-bit input port	
R43 to R40	I/O	4-bit I/O port with latch. When using as input port, the latch must be set to "1" . Every bit data is possible to be set, cleared and tested by the manipulation of the L-register indirect addressing.	
R53 to R50			
R63 to R60			
R73 to R70			
R83 (T1)	I/O (Input)	4-bit I/O port with latch. When used as input port, external interrupt input pin, or Timer/Counter external input pin, the latch must be set to "1".	Timer / Counter 1 external input
R82 ($\overline{INT1}$)			External interrupt 1 input
R81 (T2)			Timer / Counter 2 external input
R80 ($\overline{INT2}$)			External interrupt 2 input
R92 ($\overline{SCK}$)	I/O (I/O)	3-bit I/O port with latch. When used as input port or serial port, the latch must be set to "1".	Serial clock I/O
R91 (SO)	I/O (Output)		Serial data output
R90 (S I)	I/O (Input)		Serial data input
SEG23 to SEG0	Output	LCD Segment drive output	
COM4 to COM1		LCD Common drive output	
XIN	Input	Resonator connecting pin. For inputting external clock, XIN is used and XOUT is opened.	
XOUT	Output		
$\overline{RESET}$	Input	Reset signal input	
$\overline{HOLD}$ ($\overline{KE0}$)	Input (Input)	Hold request / release signal input	Sense input
TEST	Input	Test pin for out-going test. Be opened or fixed to low level.	
VDD	Power supply	+ 5 V	
VSS		0 V (GND)	
VLC		LCD drive power supply	

OPERATIONAL DESCRIPTION

Concerning the 47C221A/421A, the configuration and functions of hardwares are described. As the description has been provided with priority on those parts differing from the 47C200B/400B, the technical data sheets for the 47C200B/400B shall also be referred to.

1. SYSTEM CONFIGURATION

◆ INTERNAL CPU FUNCTION

2.1 Program Memory (ROM)

2.2 Data Memory (ROM)

The others are the same as those of the 47C200B/400B.

◆ PERIPHERAL HARDWARE FUNCTION

① I/O Ports
② Interval Timer
③ Timer / Counters (TC1, TC2)
④ LCD Driver
⑤ Serial Interface

The description has been provided with priority on functions (①, ③ and ④) added to and changed from the 47C200B/400B and ROM / RAM configurations.

2. INTERNAL CPU FUNCTION

2.1 Program Memory (ROM)

Program memory of the 47C221A/421A are similar to the 47C200B/400B except that data conversion table cannot be used.

2.2 Data Memory (RAM)

Data memory contained in the 47C221A has a 192 × 4-bit (addresses 00 to $7F_H$, C0 to FF_H) capacity, and that contained in the 47C421A has a 256 × 4-bit (adddresses 00-FF_H) capacity.

There is no physical RAM in address 80-BF_H in the 47C221A.

Therefore, when addresses 80-BF_H are accessed on a program, RAM equivalent to address C0-FF_H is accessed.

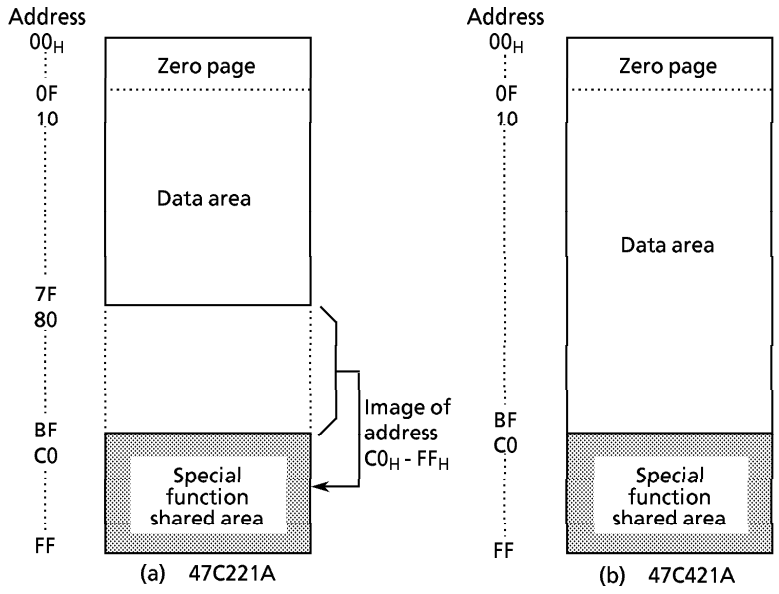


Figure 2-1. Data Memory Capacity and Address Assignment

3. PERIPHERAL HARDWARE FUNCTION

3.1 I/O port

The 47C221A/421A have 8 I/O ports (28 pins) each as follows.

① K0 ; 4-bit input
② R4, R5, R6, R7 ; 4-bit input/output
③ R8 ; 4-bit input/output (shared by external interrupt input and Timer / Counter input)
④ R9 ; 3-bit input / output (shared by serial port)
⑤ KE ; 1-bit sense input (shared by hold request/release signal input)

For the 47C221A/421A, P1 and P2 ports are eliminated.
The operations and functions of other ports are similar to that of the 47C200B/400B.
Table 3-1 lists the port address assignments and the I/O instruction that can access the port. Further, the [OUTB @ HL] instruction and 5-bit to 8-bit data conversion table cannot be used.

Table 3-1. Port Address Assignments and Available I/O Instructions.

Port address (**)	Port		Input/Output instruction						
	Input (IP**)	Output (OP**)	IN %p, A IN %p, @HL	OUT A, %p OUT@HL,%p	OUT #k, %p	OUTB @HL	SET %p, b CLR %p, b	TEST %p, b TESTP %p, b	SET @L CLR @L TEST @L
00_H	K0 input port	——	○	–	–	–	–	○	–
01	——	——	–	–	–	–	–	–	–
02	——	——	–	–	–	–	–	–	–
03	——	——	–	–	–	–	–	–	–
04	R4 input port	R4 output port	○	○	○	–	○	○	○
05	R5 input port	R5 output port	○	○	○	–	○	○	○
06	R6 input port	R6 output port	○	○	○	–	○	○	○
07	R7 input port	R7 output port	○	○	○	–	○	○	○
08	R8 input port	R8 output port	○	○	○	–	○	○	–
09	R9 input port	R9 output port	○	○	○	–	○	○	–
0A	——	——	–	–	–	–	–	–	–
0B	——	——	–	–	–	–	–	–	–
0C	——	——	–	–	–	–	–	–	–
0D	——	——	–	–	–	–	–	–	–
0E	SIO, HOLD status	——	○	–	–	–	–	○	–
0F	Serial receive buffer	Serial transmit buffer	○	○	○	–	–	–	–
10_H	Undefined	Hold operating mode control	–	○	–	–	–	–	–
11	Undefined	——	–	–	–	–	–	–	–
12	Undefined	——	–	–	–	–	–	–	–
13	Undefined	——	–	–	–	–	–	–	–
14	Undefined	——	–	–	–	–	–	–	–
15	Undefined	——	–	–	–	–	–	–	–
16	Undefined	——	–	–	–	–	–	–	–
17	Undefined	——	–	–	–	–	–	–	–
18	Undefined	——	–	–	–	–	–	–	–
19	Undefined	Interval timer control	–	○	–	–	–	–	–
1A	Undefined	LCD driver control 1	–	○	–	–	–	–	–
1B	Undefined	LCD driver control 2	–	○	–	–	–	–	–
1C	Undefined	Timer/Counter 1 control	–	○	–	–	–	–	–
1D	Undefined	Timer/Counter 2 control	–	○	–	–	–	–	–
1E	Undefined	——	–	–	–	–	–	–	–
1F	Undefined	Serial interface control	–	○	–	–	–	–	–

Note. "——" means the reserved state. Unavailable for the user programs.

3.2 Timer/Counter (TC1, TC2)

The timer/counter of 47C221A/421A are similer to that of the 47C200B/400B except for the following point. The maximum frequency applied to the external input pin under the event counter mode is dependent upon the operating state of the LCD drive circuit.

Table 3-2. The maximum frequency applied to the external input pin under the event counter mode.

Operating state of the LCD driver	Maximum frequency applied [Hz]			
	1-channel operation		2-channel operation	
	TC1	TC2	TC1	TC2
At time of blanking operation	fc/32		fc/32	fc/40
When LCD display is enabled	fc/64		fc/72	

Note. fc ; Basic clolck frequency

3.3 LCD Driver

The 47C221A/421A have the circuit that directry drivers the liquid crystal display (LCD) and its control circuit.

The 42C221/421A have the following connecting pins with LCD.

① Segment output pins 24 pins (SEG23-SEG0)
② Common output pins 4 pins (COM4-COM1)

In addition, VLC pin is provided as the driver power.

The devices that can be directly driven is selectable from LCD of following drive methods.

① 1/4 duty (1/3 bias) LCD ..... Max. 96 segments (8 segments × 12 digits)
② 1/3 duty (1/3 bias) LCD ..... Max. 72 segments (8 segments × 9 digits)
③ 1/2 duty (1/2 bias) LCD ..... Max. 48 segments (8 segments × 6 digits)
④ Static LCD ..... Max. 24 segments (8 segments × 3 digits)

3.3.1 Configuration of LCD driver

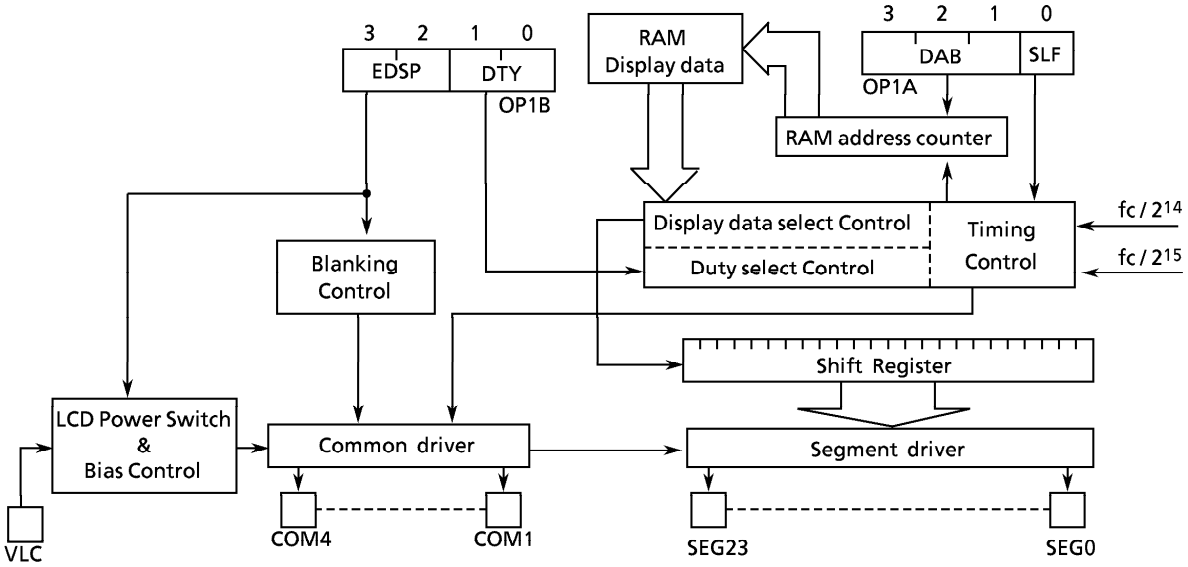


Figure 3-1. Configuration of LCD driver

3.3.2 Control of LCD driver

The LCD driver is controlled by the command register 1, 2 (OP1A, OP1B).
Note that, the MSB of the command register 2 must be cleared to "0" (set to blanking or designation of driving method) during accessing the command register 1.

LCD driver control command register 1
(port address OP1A) (Initial value 1000)

3	2	1	0
DAB			SLF

DAB	Designation of display data area	
	47C221A	47C421A
000:	Reserved	Reserved
001:	20-37$_H$	20-37$_H$
010:	40-57$_H$	40-57$_H$
011:	60-77$_H$	60-77$_H$
100:	C0-D7$_H$	80-97$_H$
101:	E0-F7$_H$	A0-B7$_H$
110:	Reserved	C0-D7$_H$
111:	Reserved	E0-F7$_H$

SLF	Selection of LCD drive Base frequency

Example : At fc = 4.19 MHz

0 : $fc / 2^{15}$ [Hz] ... 128 [Hz]
1 : $fc / 2^{14}$ 256

LCD driver control command register 2
(port address OP1B) (Initial value 0000)

3	2	1	0
EDSP		DTY	

EDSP	LCD Display Control
00:	Designation of driving methods
01:	Blanking
10:	Reserved
11:	LCD display enable

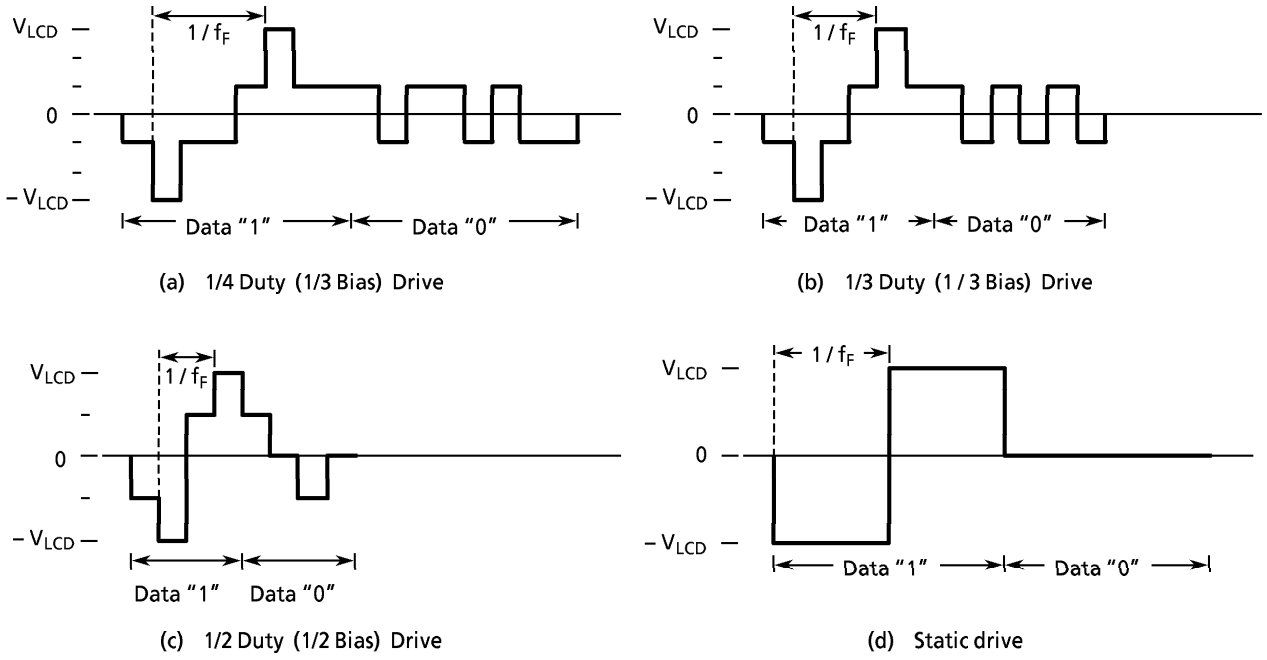
DTY	Selection of driving methods
00:	1/4 Duty (1/3 Bias)
00:	1/3 Duty (1/3 Bias)
10:	1/2 Duty (1/2 Bias)
11:	Static

Note. fc ; Basic clock frequency [Hz]

Figure 3-2. LCD driver control command register

(1) Driving methods of LCD driver

4 kinds of driving methods can be selected by DTY (bits 1 and 0 of command register). Figure 3-3 shows driving waveforms for LCD.



Note. f_F *; LCD Frame frequency* V_{LCD} *; LCD drive voltage (* $= V_{DD}–V_{LC}$*)*

Figure 3-3. LCD drive wareform (Voltage COM-SEG Pins)

(2) Frame frequency

Frame frequency is set according to the drive method and base frequency as shown in the following table 3-3.

It is possible to select base frequency (either one of 2 kind frequencies obtained from the driver) by SLF (bit 0 of command register 1) .

Table 3-3. Setting of LCD frame frequency

Driving methods / Base frequency	Frame Frequency [Hz]			
	1 / 4 Duty	1 / 3 Duty	1 / 2 Duty	Static
$\frac{fc}{2^{15}}$	$\frac{fc}{2^{15}}$	$\frac{4}{3} \cdot \frac{fc}{2^{15}}$	$\frac{4}{2} \cdot \frac{fc}{2^{15}}$	$\frac{fc}{2^{15}}$
Ex. at fc = 4.19 MHz	128	171	256	128
$\frac{fc}{2^{14}}$	$\frac{fc}{2^{14}}$	$\frac{4}{3} \cdot \frac{fc}{2^{14}}$	$\frac{4}{2} \cdot \frac{fc}{2^{14}}$	$\frac{fc}{2^{14}}$
Ex. at fc = 2.10 MHz	128	171	256	128

Note. fc ; Basic clock frequency [Hz]

(3) LCD drive voltage

The LCD drive voltage (V_{LCD}) is given by the difference in potential (VDD – VLC) between pins VDD and VLC. Therefore, when the CPU operating voltage and LCD drive voltage are the same, the VLC pin is connected to the VSS pin.

The LCD light only when the difference in potential between the segment output and common output is $\pm V_{LCD}$, and turn off at all other times.

During reset, the power switch of the LCD driver is turned off automatically, shutting off the VLC voltage.

Both the segment output and common output become V_{DD} level at this time and the LCD turn off.

The power switch is turned on to supply VLC voltage to the LCD driver by setting EDSP (bits 2 and 3 of the command register 2) to "11_B". After that, the power switch will not turn off even during blanking (setting EDSP to "01_B") and the VLC voltage continues to flow.

The power switch is turned off during hold operation low power consumption by turning off the LCD. When hold operation is released the status in effect immediately before the hold operation is reinstated.

3.3.3LCD display operation

(1) Display data setting

Display data are stored to the display data area (Max.24 words) in the data memory.

The display data area is set using DAB (bits 1 to 3 of command register 1). During reset, the display data area is set to addresses C0-$D7_H$ (47C221A) and 80-97_H (47C421A).

The display data stored to the display data area are read automatically and sent to the LCD driver by the hardware.

The LCD driver generates the segment signals and common signals in accordance with the display data and drive methods. Therefore, display patterns can be changed by only overwritting the contents of the display data area with a program. The table look- up instruction is mainly used for this overwriting. Figure 3-4 shows the correspondence between the display data area and the SEG/COM pins. The LCD light when the display data is "1" and turn off when "0".

The number of segment which canbe driven differs depending on the LCD drive method, therefore, the number of display data area bits used to store the data also differs (Refer to Table 3-4). Consequently, data memory not used to store display data and data memory for which the addresses are not connected to LCD can be used to store ordinary user's processing data.

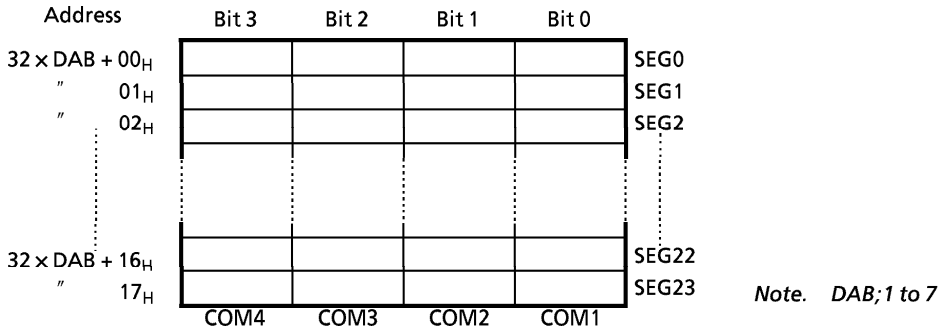


Figure 3-4. The correspondence between the display data area and the SEG/COM pins

Table 3-4. The data memory bits that are used for driving method and storing display data.

drive methods	Bit 3	Bit 2	Bit 1	Bit 0
1/4 Duty	COM4	COM3	COM2	COM1
1/3 Duty	–	COM3	COM2	COM1
1/2 Duty	–	–	COM2	COM1
Static	–	–	–	COM1

Note. – ; The data memory bits that are not used for storing display data

(2) Transfer of display data

The display data stored to the display data area are automatically transferred to the LCD driver. The processing is performed in the following sequence.

① The LCD driver issues a display data send request to the CPU

② When the instruction (or Timer / Counter processing, interrupt receive processing) currently being executed is completed, the CPU reads out the data for one cycle and sends it to the LCD driver.

The data sending cycle is generated when the VLC voltage is being applied to the LCD driver. That is, after reset is canceled, it is not generated until EDSP is set to "11_B". Table 3-5 shows the data sending cycle generation frequency.

When LCD display is enabled, the virtual instruction execution speed drops. For example, when SLF = 0 and using 1/4 duty drive, this would be 2.05 μs, for an instruction execution speed of 2 μs.

Table 3-5. Frequency of data sending cycle insertion

SLF	Driving method	Frequency of data sending cycle insertion
0	Static drive	24 times in 4,096 instruction cycles
	Except Static drive	24 times in 1,024 instruction cycles
1	Static drive	24 times in 2,048 instruction cycles
	Except Static drive	24 times in 512 instruction cycles

(3) Blanking

Blanking is applied by setting EDSP to "01_B" and turns off the LCD by outputting non light operation level to the COM pin.

The SEG pin continuously outputs the signal level in accordance with the display data and drive method. With static drive, no voltage is applied between the COM and SEG pins when the LCD is turned off by data (display data cleared to "0"), but the COM pin output becomes constant at the $V_{LCD}/2$ level when turning off the LCD by blanking, so the COM and SEG pins are then driven by $V_{LCD}/2$.

3.3.4 Control method of LCD driver

(1) Initial setting

Flow chart of initial setting is shown Figure 3-5.

Example: When operating the 47C421A with 1/4 duty LCD using a frame frequency of fc/2^{15}[Hz] (display data area at addresses 80-97_H).

```
LD      A, #0000B; Sets the 1/4 duty drive.
OUT     A, %OP1B
LD      A, #1000B; Setting of base frequency.
OUT     A, %OP1A ; Setting of display area in the
                   memory.
 :                 Setting of clear or initial value of
                   display area in the memory.
 :
LD      A, #1100B; Display enable (Release of
                   blanking)
OUT     A, %OP1B
 :
```

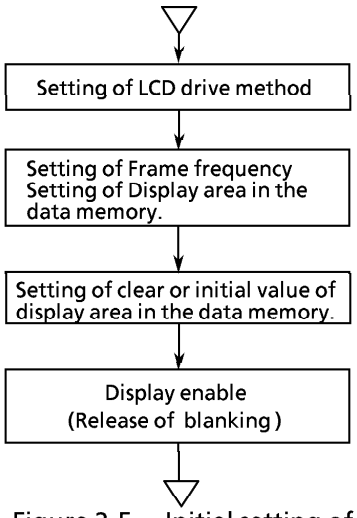


Figure 3-5. Initial setting of LCD driver

(2) Display data setting

Normally, display data are kept permanently in the program memory and are then stored to the display data area by the table look up instruction.

This can be explained using numberical display with 1/4 duty LCD as an example. The COM and SEG connections to the LCD are the same as those shown in Figure 3-6, and the display data are as shown in Table 3-6. Programming example for displaying numerals corresponding to BCD data stored at address 10_H in the data memory is shown below. The display data area is at addresses 20_H and 21_H.

```
        LD      HL, #0FCH          ;To set the DC
        LD      A,    10H
        ST      A,    @HL+
        ST      #DTBL/16, @HL+
        ST      #DTBL/256,@HL+
        LD      HL, #20H           ;Display of data corresponding
        LDL     A, @DC
        ST      A, @HL+
        LDH     A, @DC+
        ST      A, @HL+
        :
DTBL:   DATA    11011111B, 00000110B,
                11100011B, 10100111B,
                00110110B, 10110101B,
                11110101B, 00010111B,
                11110111B, 10110111B
```

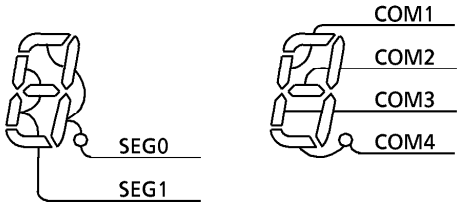


Figure 3-6. Example of COM and SEG connections

Table 3-6. Examples of Display Data (1/4 Duty LCD)

Numeral	Display	Display data memory		Numeral	Display	Display data memory	
		Upper	Lower			Upper	Lower
0	0.	1101	1111	5	5	1011	0101
1	1	0000	0110	6	6	1111	0101
2	2	1110	0011	7	7	0001	0111
3	3	1010	0111	8	8	1111	0111
4	4	0011	0110	9	9	1011	0111

Table 3-7 shows the same numerical display used in Table 3-6, but using 1/2 duty LCD. The connections of the COM and SEG pins to the LCD are the same as those shown in Figure 3-7. The display data area is at addresses 20-23$_H$.

```
        LD      HL, #0FCH       ;  To set the DC
        LD      A, 10H
        ST      A, @HL+
        ST      #DTBL/16, @HL+
        ST      #DTBL/256,@HL+
        LD      HL, #20H        ;  Display of data corresponding
        LDL     A, @DC
        ST      A, @HL+
        RORC    A
        RORC    A
        ST      A, @HL+
        LDH     A, @DC+
        ST      A, @HL+
        RORC    A
        RORC    A
        ST      A, @HL+
        ⋮
DTBL:   DATA    01110111B, 00100010B,
                10010111B, 10100111B,
                11100010B, 11100101B,
                11110101B, 01100011B,
                11110111B, 11100111B
```

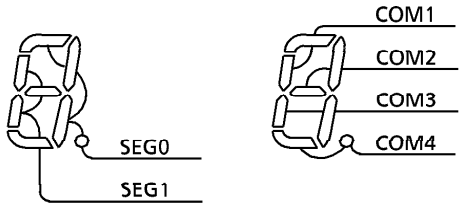


Figure 3-7. Example of COM and SEG connections

Table 3-7. Example of Display Data (1/2 duty LCD)

Numeral	Display data memory				Numeral	Display data memory			
	Upper			Lower		Upper			Lower
0	**01	**11	**01	**11	5	**11	**10	**01	**01
1	**00	**10	**00	**10	6	**11	**11	**01	**01
2	**10	**01	**01	**11	7	**01	**10	**00	**11
3	**10	**10	**01	**11	8	**11	**11	**01	**11
4	**11	**10	**00	**10	9	**11	**10	**01	**11

*Note. * ; don't care*

(3) Example of drive output

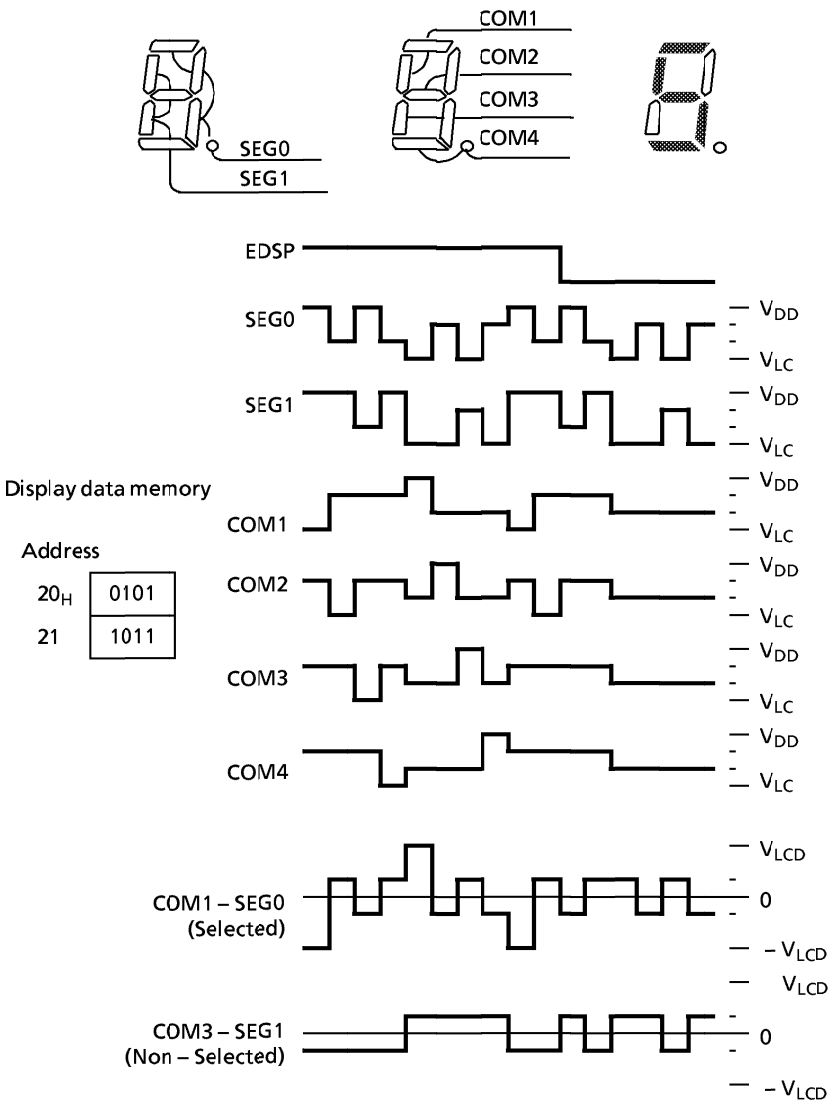


Figure 3-8. 1 / 4Duty (1 / 3Bias) Drive

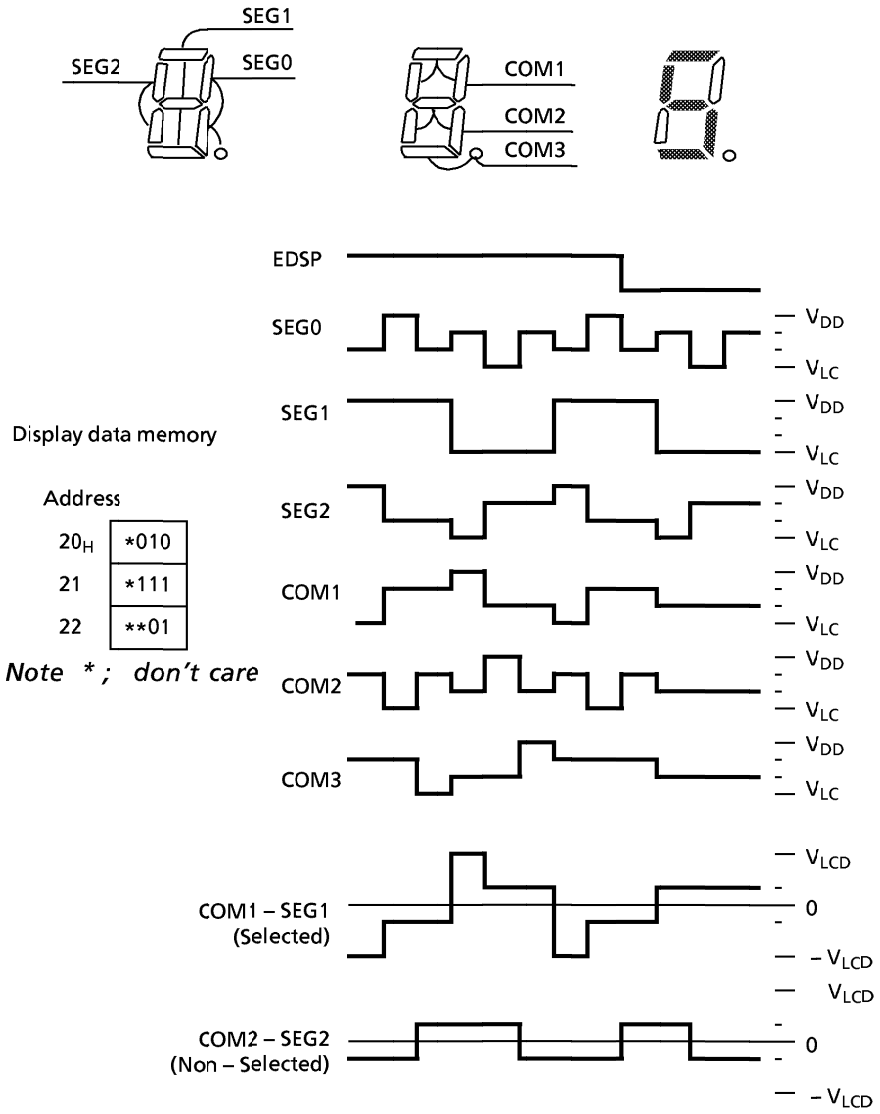


Figure 3-9. 1 / 3Duty (1 / 3Bias) Drive

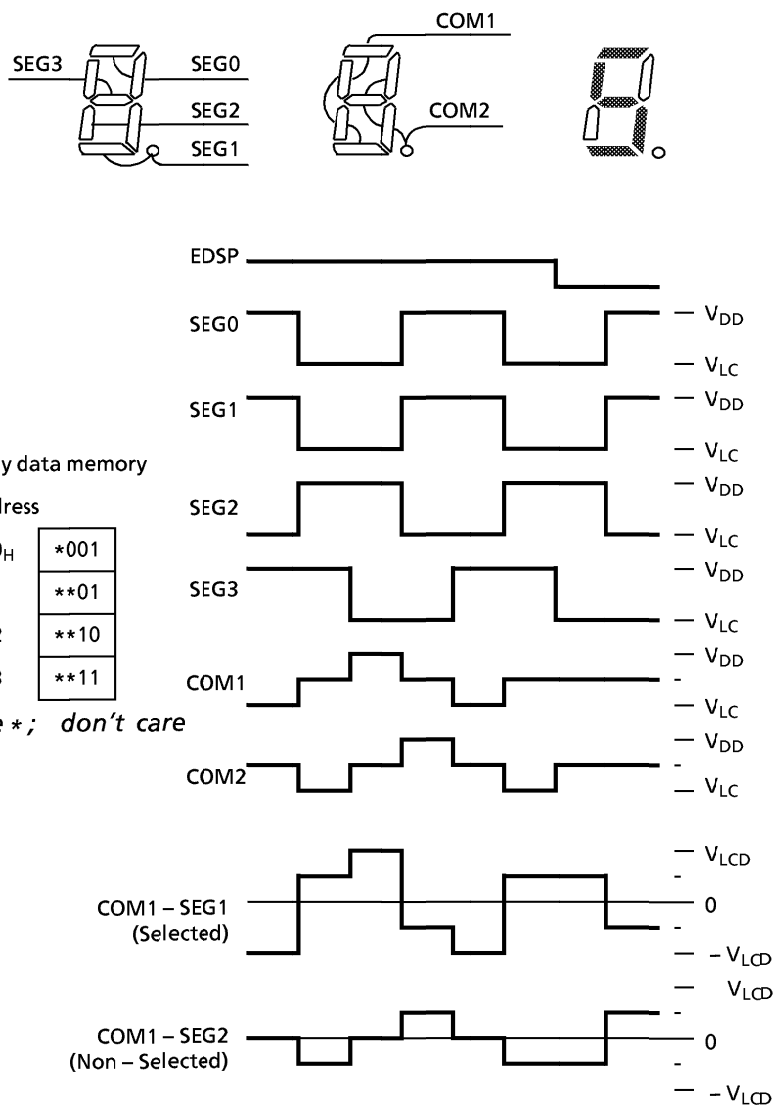


Figure 3-10. 1 / 2 Duty (1 / 2Bias) Drive

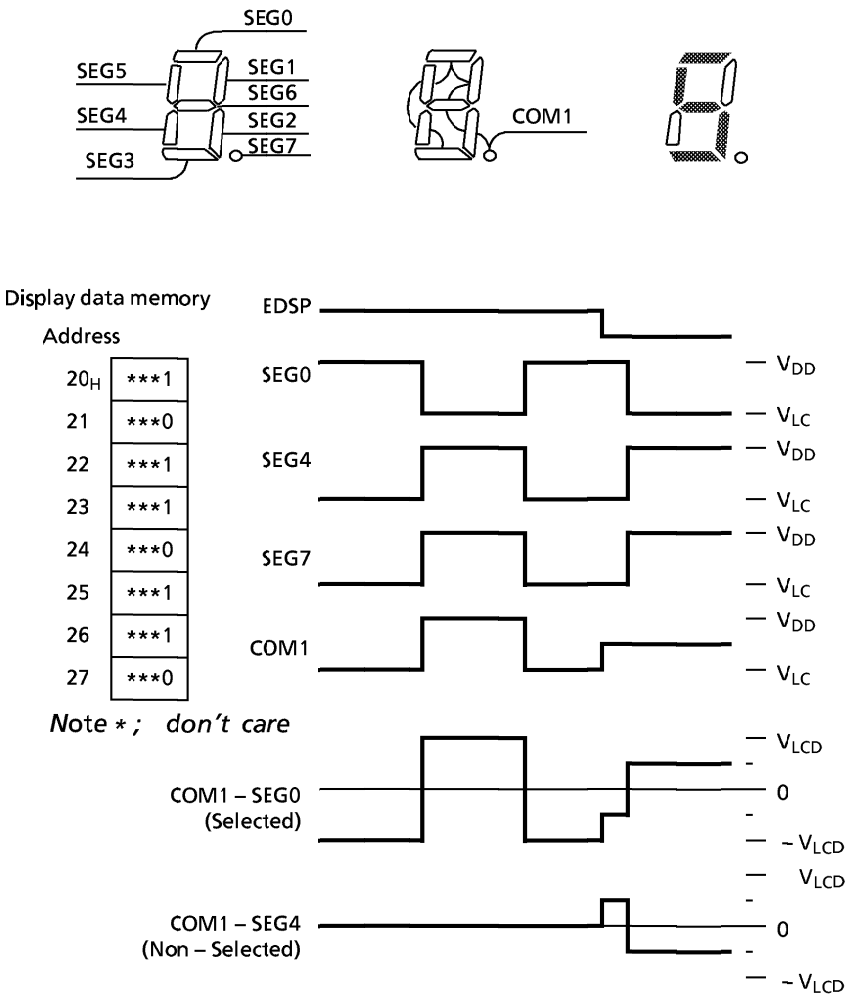


Figure 3-11. Static Drive

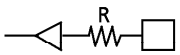
INPUT / OUTPUT CURCUITRY

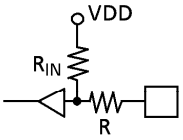
(1) Control pins

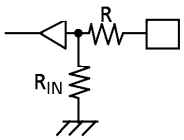
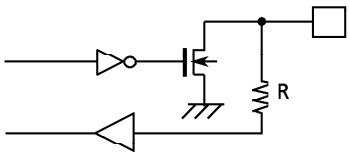
Input / Output circuitries of the 47C221A/421A control pins are similar to that of the 47C200B/400B.

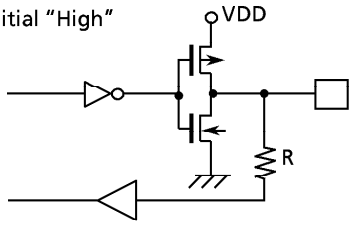
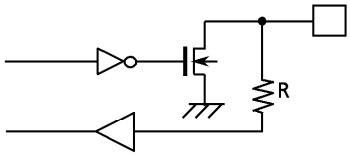
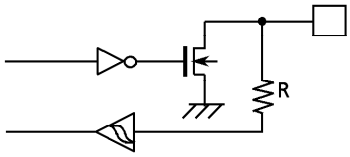
(2) I/O Ports

The input/output circuitries of the 47C221A/421A I/O ports are shown below, any one of the circuitries can be chosen by a code (GA-GF) as a mask option.

<table>
<tr><th>PORT</th><th>I/O</th><th>INPUT/OUTPUT CIRCUITRY and CODE</th><th>REMARKS</th></tr>
<tr><td>K0</td><td>Input</td><td>GA, GD
 

GB, GE
 

GC, GF
 
</td><td>pull-up/pull-down resistor
RIN = 70 kΩ (typ.)
R = 1 kΩ (typ.)</td></tr>
<tr><td>R4
R5
R6</td><td>I/O</td><td>GA, GB, GC
Initial “Hi-Z”
 

GD, GE, GF
Initial “High”
 
</td><td>Sink open drain or push-pull output
R = 1 kΩ (typ.)</td></tr>
<tr><td>R7</td><td>I/O</td><td> 
</td><td>Sink open drain output
Initial “Hi-Z”
R = 1 kΩ (typ.)</td></tr>
<tr><td>R8
R9</td><td>I/O</td><td> 
</td><td>Sink open drain output
Initial “Hi-Z”
Hysteresis input
R = 1 kΩ (typ.)</td></tr>
</table>

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0 V)

PARAMETER	SYMBOL	PINS	RATING	UNIT
Supply Voltage	V_{DD}		– 0.5 to 7	V
Supply Voltage (LCD drive)	V_{LC}		– 0.5 to V_{DD} + 0.5	V
Input Voltage	V_{IN}		– 0.5 to V_{DD} + 0.5	V
Output Voltage	V_{OUT1}	Except sink open drain pin	– 0.5 to V_{DD} + 0.5	V
	V_{OUT2}	Sink open drain pin	– 0.5 to 10	
Output Current (per 1 pin)	I_{OUT}		3.2	mA
Power Dissipation [T_{opr} = 70℃]	PD		400	mW
Soldering Temperature (time)	T_{sld}		260 (10 s)	℃
Storage Temperature	T_{stg}		– 55 to 125	℃
Operating Temperature	T_{opr}		– 30 to 70	℃

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0 V, T_{opr} = – 30 to 70 °C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}		In the Normal operating mode	4.5	6.0	V
			In the Hold operating mode	2.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input	VDD ≧ 4.5 V	VDD × 0.7	V_{DD}	V
	V_{IH2}	Hysteresis Input		VDD × 0.75		
	V_{IH3}		VDD < 4.5 V	VDD × 0.9		
Input Low Voltage	V_{IL1}	Except Hysteresis Input	VDD ≧ 4.5 V	0	V_{DD} × 0.3	V
	V_{IL2}	Hysteresis Input			V_{DD} × 0.25	
	V_{IL3}		VDD < 4.5 V		V_{DD} × 0.1	
Clock Frequency	fc			0.4	4.2	MHz

Note 1. Input Voltage V_{IH3}, V_{IL3} : in the HOLD operating mode.
Note 2. 1MHz is recommended as minimum freqency when SLF = 1. And 2MHz is when SLF = 0.

D.C. CHARACTERISTICS (V_{SS} = 0 V, V_{DD} = 4.5 to 6.0 V, T_{opr} = – 30 to 70 °C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		—	0.7	—	V
Input Current	I_{IN1}	Port K0, TEST, $\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5 V, V_{IN} = 5.5 V / 0 V	—	—	± 2	μA
	I_{IN2}	Ports R (open drain)					
Low Input Current	I_{IL}	Ports R (push-pull)	V_{DD} = 5.5 V, V_{IN} = 0.4 V	—	—	– 2	mA
Input Resistance	R_{IN1}	Port K0 with pull-up/pull-down resistor		30	70	150	kΩ
	R_{IN2}	$\overline{RESET}$		100	220	450	
Output Leakage Current	I_{LO}	Ports R (open drain)	V_{DD} = 5.5 V, V_{OUT} = 5.5 V	—	—	2	μA
Output High Voltage	V_{OH}	Ports R (push-pull)	V_{DD} = 4.5 V, I_{OH} = – 200 μA	2.4	—	—	V
Output Low Voltage	V_{OL2}	Except XOUT	V_{DD} = 4.5 V, I_{OL} = 1.6 mA	—	—	0.4	V
Segment Output Low Resistance	R_{OS1}	SEG pin	V_{DD} = 5 V, V_{DD} – V_{LC} = 3 V	—	10	—	kΩ
Common Output Low Resistance	R_{OC1}	COM pin					
Segment Output High Resistance	R_{OS2}	SEG pin		—	70	—	
Common Output High Resistance	R_{OC2}	COM pin					
Segment / Common Output Voltage	$V_{O2/3}$	SEG / COM pin		3.8	4.0	4.2	V
	$V_{O1/2}$			3.3	3.5	3.7	
	$V_{O1/3}$			2.8	3.0	3.2	
Supply Current (in the Normal mode)	I_{DD}		V_{DD} = 5.5 V, V_{LC} = V_{SS} fc = 4 MHz	—	3	6	mA
Supply Current (in the HOLD mode)	I_{DDH}		V_{DD} = 5.5 V	—	0.5	10	μA

Note1. Typ. values show those at T_{opr} = 25 °C, V_{DD} = 5 V.

Note2. Input Current IIN1 : The current through resistor is not included, when the input resistor (pull-up / pull-down) is contained.

Note3. Output resistance R_{OS}, R_{OC} : indicates the on resistance during level switching.

Note4. $V_{O2/3}$: indicates 2/3 level output voltage when driving at 1/4 or 1/3 duty.

Note5. $V_{O1/2}$: indicates 1/2 level output voltage for 1/2 duty or static drive.

Note6. $V_{O1/3}$: indicates 1/3 level output voltage when driving at 1/4 or 1/3 duty.

Note7. Supply Current : V_{IN} = 5.3 V / 0.2 V.
The voltage applied to the port R is within the valid range V_{IL} or V_{IH}.

Note 8. When using LCD, it is necessary to consider values of $R_{OS1/2}$ and $R_{OC1/2}$.

Note 9. Times for SEG / COM output resistance switching on :
R_{OS1}, R_{OC1} : 2/fs (s)
R_{OS2}, R_{OC2} : 1/(n·f_F) (1/n : duty, f_F : frame frequency)

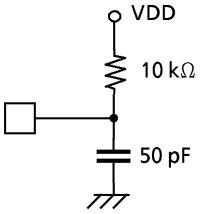
A.C. CHARACTERISTICS

(V_{SS} = 0 V, V_{DD} = 4.5 to 6.0 V, T_{opr} = – 30 to 70 °C)

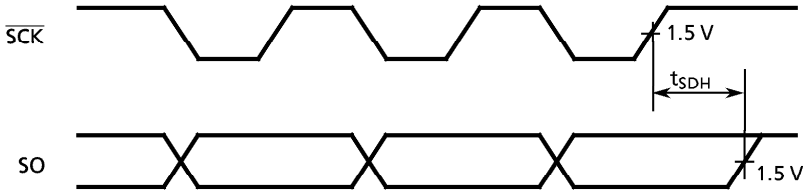
PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}		1.9	—	20	μs
High level Clock pulse Width	t_{WCH}	External clock mode	80	—	—	ns
Low level Clock pulse Width	t_{WCL}					
Shift data Hold Time	t_{SDH}		0.5 t_{cy} – 300	—	—	ns

Note. Shift data Hold Time:

External circuit for $\overline{SCK}$ pin and SO pin



Serial port (completion of transmission)



RECOMMENDED OSCILLATING CONDITIONS

(V_{SS} = 0 V, V_{DD} = 4.5 to 6.0 V, T_{opr} = – 30 to 70 °C)

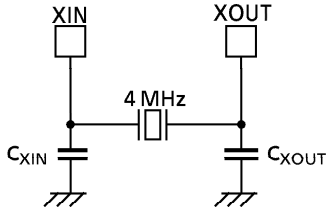
(1) 4 MHz

Ceramic Resonator

CSA4.00MG	(MURATA)	$C_{XIN} = C_{XOUT}$ = 30 pF
KBR-4.00MS	(KYOCERA)	$C_{XIN} = C_{XOUT}$ = 30 pF

Crystal Oscillator

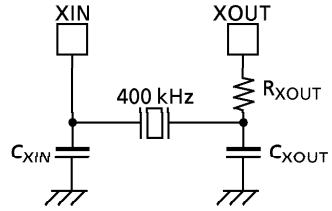
204B-6F 4.0000	(TOYOCOM)	$C_{XIN} = C_{XOUT}$ = 20 pF



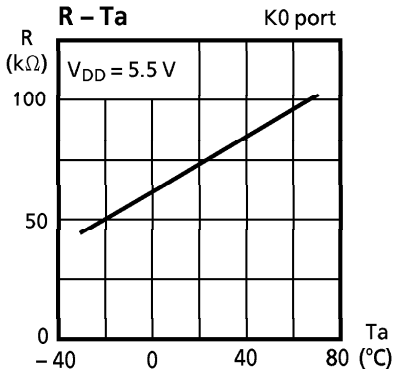
(2) 400 kHz

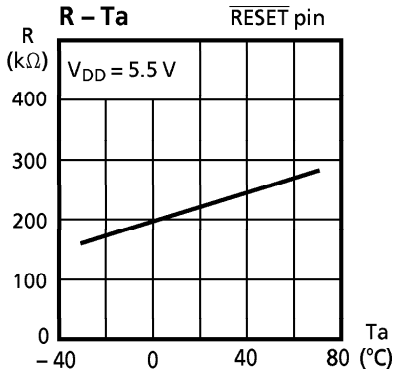
Ceramic Resonator

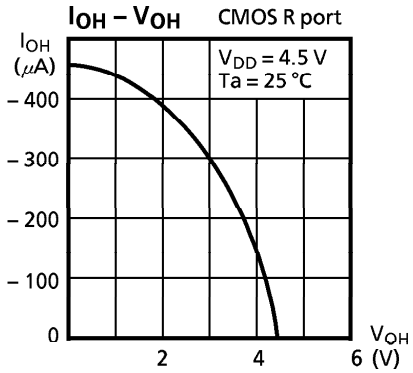
CSB400B	(MURATA)	$C_{XIN} = C_{XOUT}$ = 220 pF, R_{XOUT} = 6.8 kΩ
KBR-400B	(KYOCERA)	$C_{XIN} = C_{XOUT}$ = 100 pF, R_{XOUT} = 10 kΩ

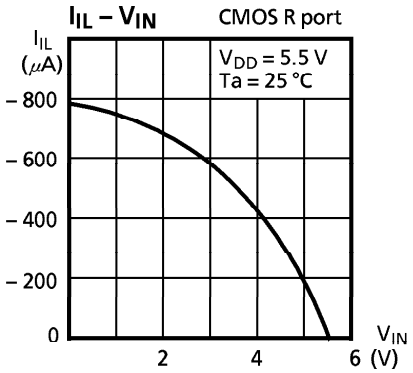


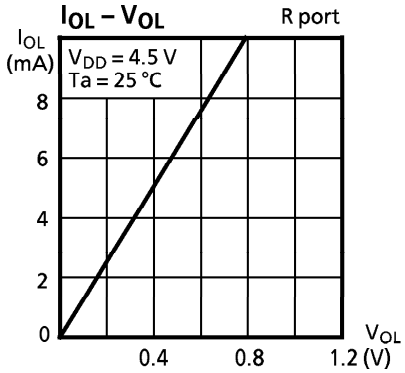
TYPICAL CHARACTERISTICS

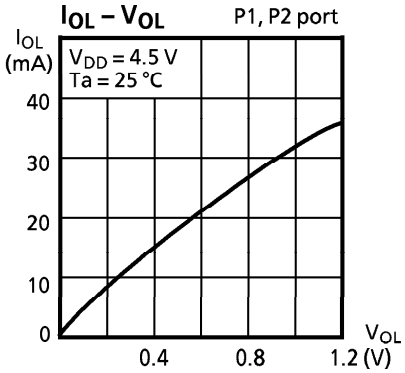


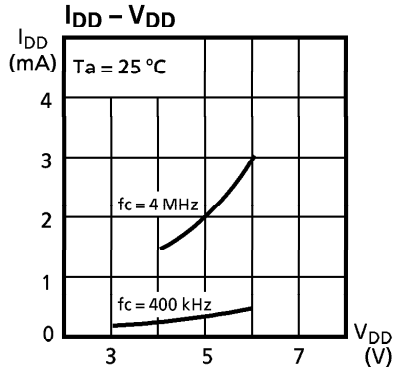


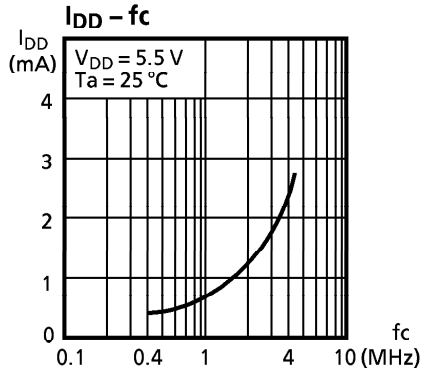


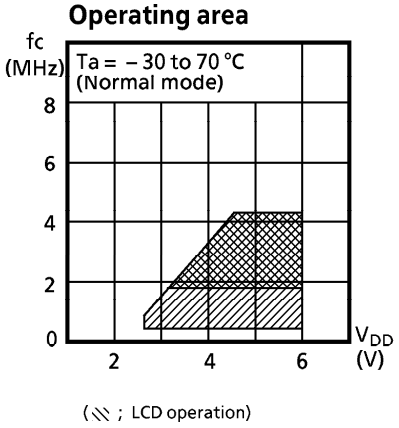












Note . 1 MHz is recommended as minimum freqency when SLF = 1. And 2 MHz is when SLF = 0.