TOSHIBA

TOSHIBA Original CMOS 4-Bit Microcontroller

TLCS-47 Series

TMP47C102PG
TMP47C202PG
TMP47C102MG
TMP47C202MG

TOSHIBA CORPORATION

Semiconductor Company

Document Change Notification

The purpose of this notification is to inform customers about the launch of the Pb-free version of the device. The introduction of a Pb-free replacement affects the datasheet. Please understand that this notification is intended as a temporary substitute for a revision of the datasheet.

Changes to the datasheet may include the following, though not all of them may apply to this particular device.

1. Part number

   Example: TMPxxxxxxF → TMPxxxxxxFG

   All references to the previous part number were left unchanged in body text. The new part number is indicated on the prelims pages (cover page and this notification).

2. Package code and package dimensions

   Example: LQFP100-P-1414-0.50C → LQFP100-P-1414-0.50F

   All references to the previous package code and package dimensions were left unchanged in body text. The new ones are indicated on the prelims pages.

3. Addition of notes on lead solderability

   Now that the device is Pb-free, notes on lead solderability have been added.

4. RESTRICTIONS ON PRODUCT USE

   The previous (obsolete) provision might be left unchanged on page 1 of body text. A new replacement is included on the next page.

5. Publication date of the datasheet

   The publication date at the lower right corner of the prelims pages applies to the new device.

1. Part number

2. Package code and dimensions

Previous Part Number (in Body Text)	Previous Package Code (in Body Text)	New Part Number	New Package Code	OTP
TMP47C102P	P-DIP20-300-2.54A	TMP47C102PG	DIP20-P-300-2.54A	TMP47P202VPG
TMP47C102M	P-SOP20-300-1.27	TMP47C102MG	SOP20-P-300-1.27	TMP47P202VMG
TMP47C202P	P-DIP20-300-2.54A	TMP47C202PG	DIP20-P-300-2.54A	TMP47P202VPG
TMP47C202M	P-SOP20-300-1.27	TMP47C202MG	SOP20-P-300-1.27	TMP47P202VMG

*: For the dimensions of the new package, see the attached Package Dimensions diagram.

3. Addition of notes on lead solderability

The following solderability test is conducted on the new device.

Lead solderability of Pb-free devices (with the G suffix)

Test	Test Conditions	Remark
Solderability	(1) Use of Lead (Pb) ·solder bath temperature = 230°C ·dipping time = 5 seconds ·the number of times = once ·use of R-type flux (2) Use of Lead (Pb)-Free ·solder bath temperature = 245°C ·dipping time = 5 seconds ·the number of times = once ·use of R-type flux	Leads with over 95% solder coverage till lead forming are acceptable.

4. RESTRICTIONS ON PRODUCT USE

The following replaces the "RESTRICTIONS ON PRODUCT USE" on page 1 of body text.

RESTRICTIONS ON PRODUCT USE 20070701-EN

- The information contained herein is subject to change without notice.
- TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.
  In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the "Handling Guide for Semiconductor Devices," or "TOSHIBA Semiconductor Reliability Handbook" etc.
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- For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance/Handling Precautions.

5. Publication date of the datasheet

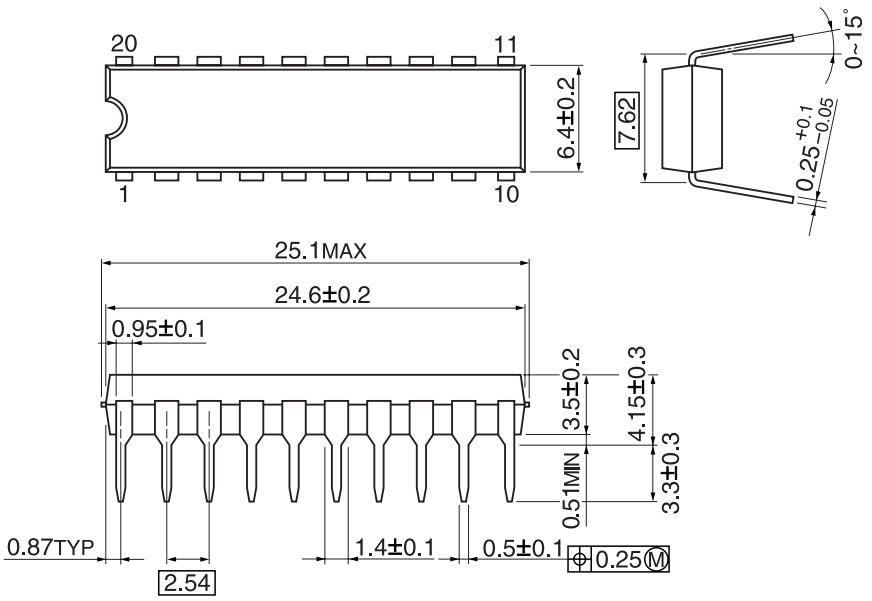
The publication date of this datasheet is printed at the lower right corner of this notification.

(Annex)

Package Dimensions

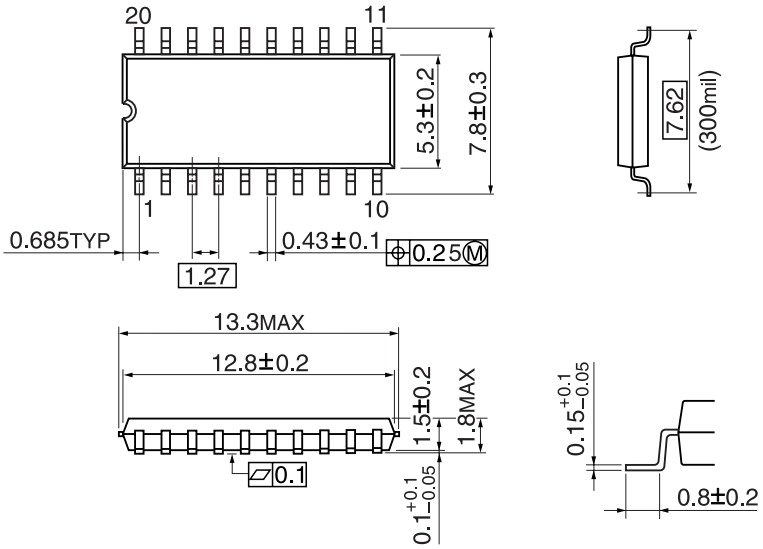
DIP20-P-300-2.54A

Unit: mm



SOP20-P-300-1.27

Unit: mm



CMOS 4-Bit Microcontroller

TMP47C102P, TMP47C202P
TMP47C102M, TMP47C202M

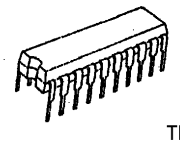
The TMP47C102/202 are high speed and high performance 4-bit single chip microcomputers, integrating ROM, RAM, input / output ports and timer / counters on a chip. The TMP47C102/202 are the standard LSI in the TLCS-47E series.
In addition, they have the output port with LED direct drive capability.

Part No.	ROM	RAM	Package	OTP
TMP47C102P	1024 × 8-bit	64 × 4-bit	P-DIP20-300-2.54A	TMP47P202VP
TMP47C102M			P-SOP20-300-1.27	TMP47P202VM
TMP47C202P	2048 × 8-bit	128 × 4-bit	P-DIP20-300-2.54A	TMP47P202VP
TMP47C202M			P-SOP20-300-1.27	TMP47P202VM

Features

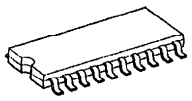
- ◆4-bit single chip microcomputer
- ◆Instruction execution time: 1.3 μs (at 6 MHz)
- ◆Low voltage operation: 2.2 V (at 2 MHz RC)
- ◆89 basic instructions
  ROM table look-up instructions
- ◆Subroutine nesting: 15 levels max
- ◆5 interrupt sources (External: 2, Internal: 3)
  All sources have independent latches each, and multiple interrupt control is available.
- ◆I/O port (15 pins)
- ◆Two 12-bit Timer / Counters
  Timer, event counter, and pulse width mea-surement mode
- ◆Interval Timer
- ◆Watchdog timer
- ◆High current outputs
  LED direct drive capability: typ. 20 mA × 4 bits (port R4)
  typ. 7 mA × 4 bits (port R5)
- ◆Hold function
  Battery / Capacitor back-up
- ◆Real Time Emulator: BM47C203

P-DIP20-300-2.54A



TMP47C102P
TMP47C202P
TMP47P202VP

P-SOP20-300-1.27

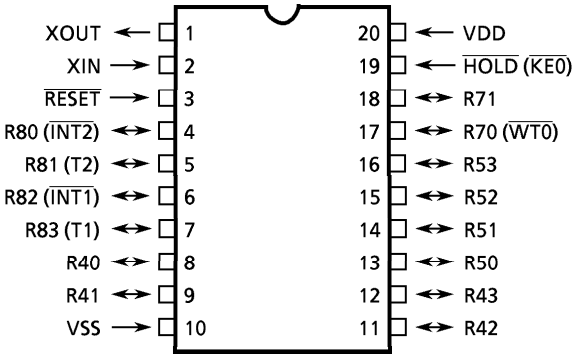


TMP47C102M
TMP47C202M
TMP47C202VM

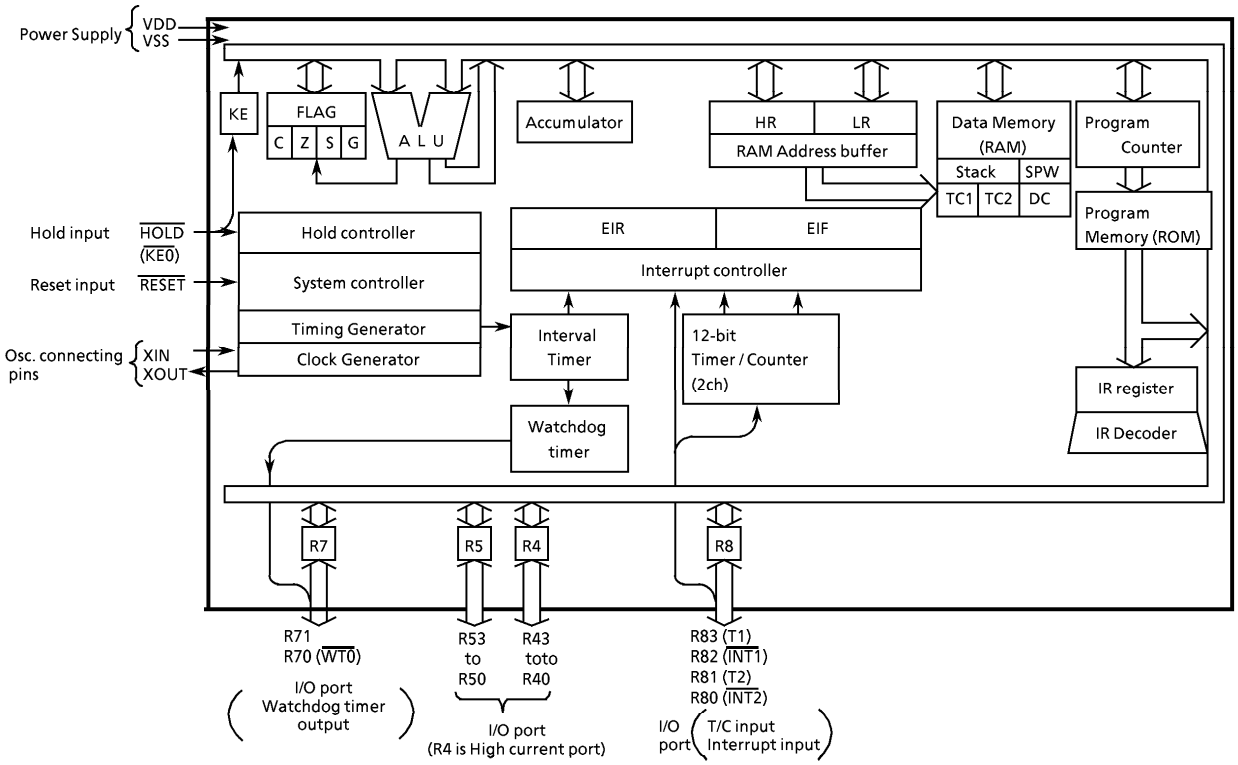
000707EBA1

Pin Assignment (Top View)

P-DIP20-300-2.54A / P-SOP20-300-1.27



Block Diagram



Pin Function

Pin Name	Input / Output	Functions	
R43 to R40	I/O	4-bit I/O port with latch (R7 port has only 2-bit).	
R53 to R50		When used as input port, the latch must be set to "1".	
R71		Every bit data is possible to be set, cleared and tested by the bit manipulation instruction of the L-register indirect addressing.	
R70 ($\overline{WTO}$)	I/O (Output)		Watchdog timer output
R83 (T1)	I/O (Input)	4-bit I/O port with latch. When used as input port, external interrupt input pin, or timer / counter external input pin, the latch must be set to "1".	Timer / Counter 1 external input
R82 ($\overline{INT1}$)			External interrupt 1 input
R81 (T2)			Timer / Counter 2 external input
R80 ($\overline{INT2}$)			External interrupt 2 input
XIN	Input	Resonator connecting pins. For inputting external clock, XIN is used and XOUT is opened.	
XOUT	Output		
$\overline{RESET}$	Input	Reset signal input	
$\overline{HOLD}$ ($\overline{KE0}$)	Input (Input)	Hold request / release signal input	Sense input
VDD	Power Supply	+ 5 V	
VSS		0 V (GND)	

Operational Description

Concerning the above component parts, the configuration and functions of hardware are described. The basic instruction of configuration in the TMP47C102/202 is the same as those of TLCS-470 series.

1. System Configuration

◆ Internal CPU Function
- 2.1 Program Counter (PC)
- 2.2 Program Memory (ROM)
- 2.3 H Register, L Register
- 2.4 Data Memory (RAM)
  - Stack
  - Stack Pointer Word (SPW)
  - Data Counter (DC)
- 2.5 ALU, Accumulator
- 2.6 Flags
- 2.7 System Controller
- 2.8 Interrupt Controller
- 2.9 Reset Circuit

◆ Peripheral Hardware Function
- 3.1 I/O Ports
- 3.2 Interval Timer
- 3.3 Timer / Counters (TC1, TC2)
- 3.4 Watchdog Timer

2. Internal CPU Function

2.1 Program Counter (PC)

The program counter is a 11-bit binary counter which indicates the address of the program memory storing the next instruction to be executed. Normally, the PC is incremented by the number of bytes of the instruction every time it is fetched. When a branch instruction or a subroutine instruction has been executed or an interrupt has been accepted, the specified values listed in Table 2-1 are set to the PC. The PC is initialized to "0" during reset.

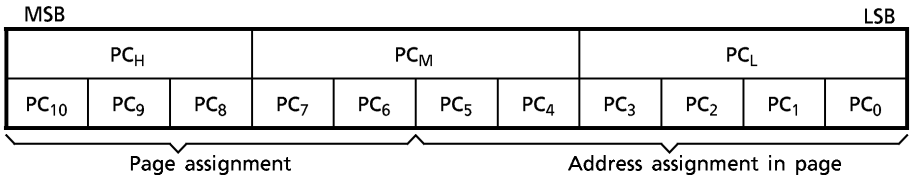


Figure 2-1. Configuration of Program Counter

The PC can directly address a 2048-byte address space. However, with the short branch, the following points must be considered:

- Short branch instruction [BSS a]
  In [BSS a] instruction execution, when the branch condition is satisfied, the value specified in the instruction is set to the lower 6 bits of the PC. That is, [BSS a] becomes the in-page branch instruction. When [BSS a] is stored at the last address of the page, the upper 5 bits of the PC point the next page, so that branch is made to the next page.

Table 2-1. Status Change of Program Counter

Instruction or Operation		Condition		Program Counter (PC)										
				PC_{10}	PC_9	PC_8	PC_7	PC_6	PC_5	PC_4	PC3	PC_2	PC_1	PC_0
Execution of Instruction	BS a	SF = 1 (Branch condition is satisfied)		Immediate data specified by the instruction										
		SF = 0 (Branch condition is not satisfied)		+ 2										
	BSS a	SF = 1	Lower 6-bit address ≠ 111111	Hold							Immediate data specified by the instruction			
			Lower 6-bit address = 111111 (last address in page)	+ 1							Immediate data specified by the instruction			
		SF = 0		+ 1										
	CALL a			Immediate data specified by the instruction										
	CALLS a			0	0	0	The data generated by the immediate data specified by the instruction					1	1	0
	RET			The return address restored from stack										
	RETI			The return address restored from stack										
	Others			Incremented by the number of bytes in the instruction										
Interrupt acceptance				0	0	0	0	0	0	0	Interrupt vector			0
Reset				0	0	0	0	0	0	0	0	0	0	0

2.2 Program Memory (ROM)

Programs and fixed data are stored in the program memory. The instruction to be executed next is read from the address indicated by the contents of the PC.

The fixed data can be read by using the table look-up instructions.

- Table look-up instructions

  [LDL A, @DC], [LDH A, @DC+]

  The table look-up instructions read the lower and upper 4 bits of the fixed data stored at the address specified in the data counter (DC) to place them into the accumulator. [LDL A, @DC] instruction reads the lower 4 bits of fixed data, and [LDH A, @DC+] instruction reads the upper 4 bits.

  The DC is a 12-bit register, allowing it to address the entire program memory space.

  In this case, the uppers bit of the DC (MSB) is ignored.

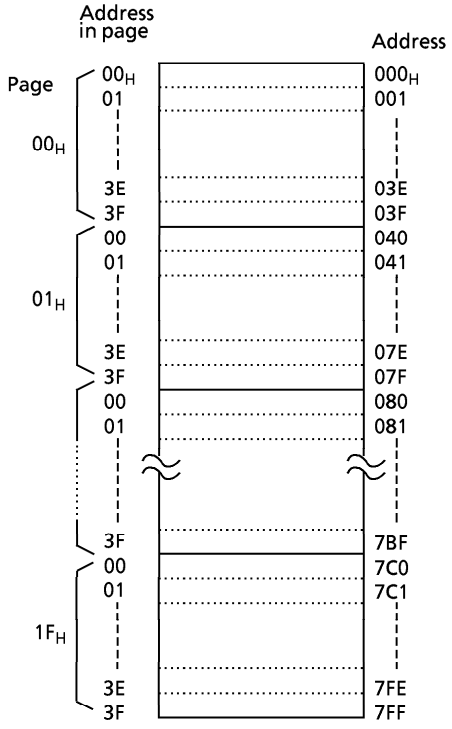


Figure 2-2. Configuration of Program Memory

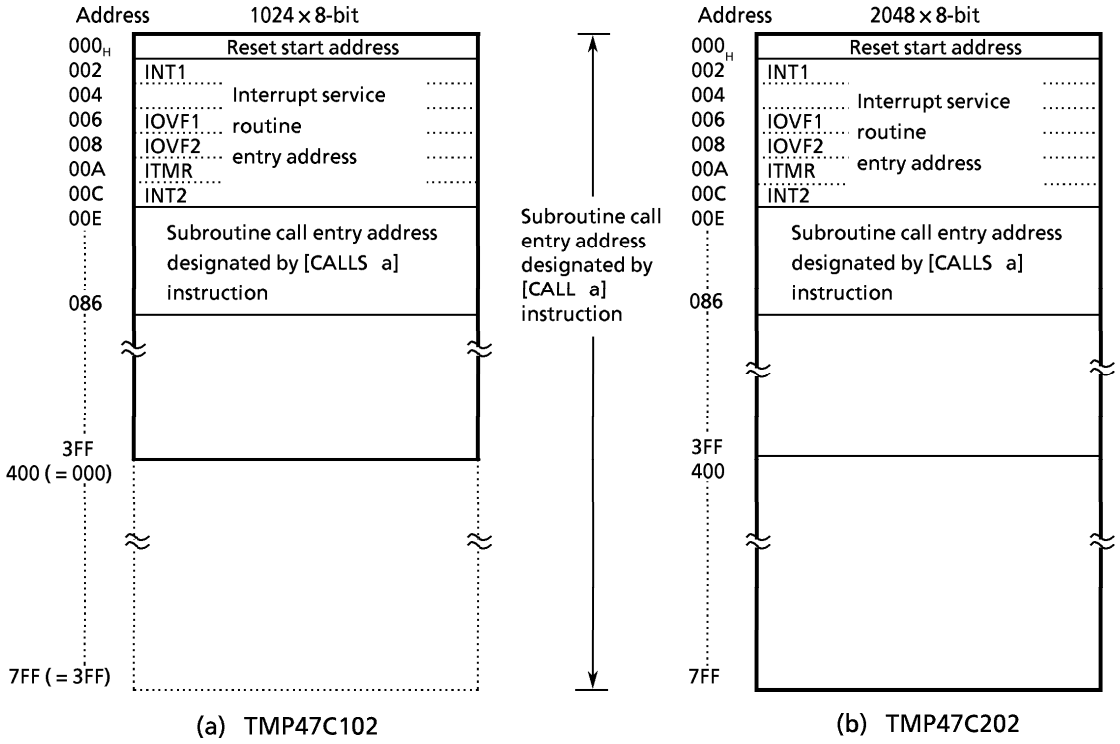
2.2.1 Program Memory Capacity

The TMP47C102 has 1024 × 8 bits (addresses 000_H through $3FF_H$) of program memory (mask ROM), the TMP47C202 has 2048 × 8 bits (addresses 000_H through $7FF_H$).

Figure 2-3 shows the program memory map. Address 000_H to 086_H of the program memory are also used for special purposes.

2.2.2 Program Memory Map

On the TMP47C102, no physical program memory exists in the address range 400_H through $7FF_H$. However, if this space is accessed by program, the most significant bit of each address is always regarded as "0" and the contents of the program memory corresponding to the address 000_H through $3FF_H$ are read.



(a) TMP47C102 (b) TMP47C202

Note: Address 004_H and 005_H can be used to store ordinary user's processing data.

Figure 2-3. Program Memory Map

2.3 H Register and L Register

The H register and the L register are 4-bit general registers. They are also used as a register pair (HL) for the data memory (RAM) addressing pointer. The RAM consists of pages, each page being 16 words long (1 word = 4 bits). The H register specifies a page and the L register specifies an address in the page.

The L register has the auto-post-increment/decrement capability, implementing the execution of composite instructions. For example, [ST A, @HL+] instruction automatically increments the contents of the L register after data transfer.

During the execution of [SET @L], [CLR @L], or [TEST @L] instructions, the L register is also used to specify the bits corresponding to I/O port pins R53 through R40 (the indirect addressing of port bits by the L register).

Example 1: To write immediate values "5" and "F_H" to data memory addresses 10_H and 11_H.

```
LD      HL,#10H          ;  HL←10H
ST      #5,@HL+          ;  RAM [10H] ←5H, LR←LR + 1
ST      #0FH,@HL+        ;  RAM [11H] ←FH, LR←LR + 1
```

Example 2: The output latch of R51 pin set "1" by the L register indirect addressing bit manipulation instruction.

```
LD      L,#0101B         ;  Sets R51 pin address to L register
SET     @L               ;  R51←1
```

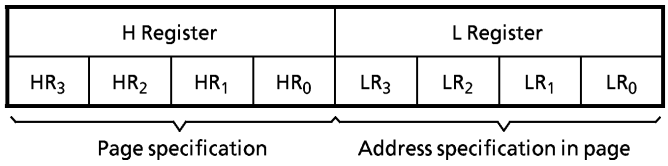


Figure 2-4. Configuration of H and L Registers

2.4 Data Memory (RAM)

The data memory stores user-processed data. One-page of this memory is 16 words long (1 word = 4 bits). It has 8 page.

The RAM is addressed in one of the three ways (addressing modes):

(1) Register-indirect addressing mode

In this mode, a page is specified by the H register and an address in the page by the L register.

Example: LD A, @HL ; Acc←RAM [HL]

(2) Direct addressing mode

In this mode, an address is directly specified by the 8 bits of the second byte (operand) in the instruction field.

Example: LD A, 2CH ; Acc←RAM [$2C_H$]

(3) Zero-page addressing mode

In this mode, an address in zero-page (addresses 00_H through $0F_H$) is specified by the lower 4 bits of the second byte (operand) in the instruction field.

Example: ST #3, 05H ; RAM [05_H] ←3

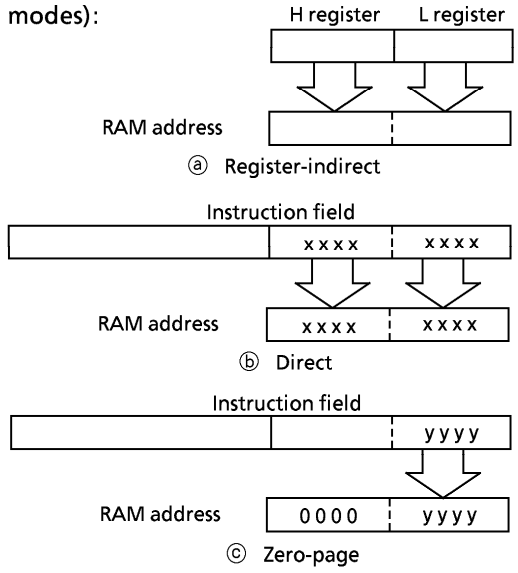
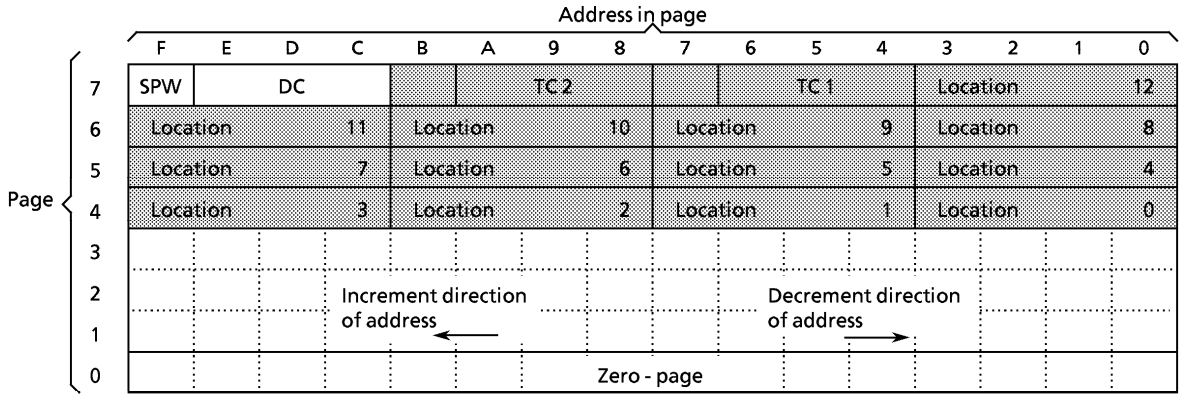


Figure 2-5. Addressing mode

2.4.1 Data Memory Map

Figure 2-6 shows the data memory map. The data memory is also used for the following special purpose.

① Stack and Stack Pointer Word (SPW)
② Data Counter (DC)
③ Count registers of the timer / counters (TC1, TC2)
④ Zero-page



Note1: ▨ *denotes the stack area.*
Note2: *The TC1 and TC2 areas are shared by the locations 13 and 14.*

Figure 2-6. Data Memory Map (TMP47C202)

(1) Stack

The stack provides the area in which the return address is saved before a jump is performed to the processing routine at the execution of a subroutine call instruction or the acceptance of an interrupt. When a subroutine call instruction is executed, the contents (the return address) of the program counter are saved; when an interrupt is accepted, the contents of the program counter and flags are saved.

When returning from the processing routine, executing the subroutine return instruction [RET] restores the contents of the program counter from the stack; executing the interrupt return instruction [RETI] restores the contents of the program counter and flags.

The stack consists of up to 15 levels (locations 0 through 14) which are provided in the data memory (addresses 40_H through $7B_H$). Each location consists of 4-word data memory. Locations 13 and 14 are shared with the count registers of the timer / counters (TC1, TC2) to be described later.

The save / restore locations in the stack are determined by the stack pointer word (SPW). The SPW is automatically decremented after save, and incremented before restore. That is, the value of the SPW indicates the stack location number for the next save.

(2) Stack Pointer Word (SPW)

Address $7F_H$ ($3F_H$ for the TMP47C102) in the data memory is called the stack pointer word, which identifies the location in the stack to be accessed (save or restore).

Generally, location number 0 to 12 can be set to the SPW, providing up to 13 levels of stack nesting. Locations 13 and 14 are shared with the timer / counters to be described later; therefore, when the timer / counters are not used, the stack area of up to 15 levels is available. Address $7F_H$ is assigned to the SPW, so that the contents of the SPW cannot be set "15" in any case.

The SPW is automatically updated when a subroutine call is executed or an interrupt is accepted. However, if it is used in excess of the stack area permitted by the data memory allocating configuration, the user-processed data may be lost. (For example, when the user-processed data area is in an address range 00_H through $4F_H$, up to location 4 of the stacks are usable. If an interrupt is accepted with location 4 already used, the user-processed data stored in addresses $4C_H$ through $4F_H$ corresponding to the location 3 area is lost.)

The SPW is not initialized by hardware, requiring to write the initial value (the location with which the use of the stack starts) by using the initialization routine. Normally, the initial value of "12" is used.

Example: To initialize the SPW (when the stack is used from location 12)

```
LD      A,#12     ;  SPW←12
ST      A,0FFH
```

(3) Data Counter (DC)

The data counter is a 12-bit register to specify the address of the data table to be referenced in the program memory (ROM). Data table reference is performed by the table look-up instructions [LDL A, @DC] and [LDH A, @DC+]. The data table may be located anywhere within the program memory address space.

The DC is assigned with a RAM address in unit of 4 bits. Therefore, the RAM manipulation instruction is used to set the initial value or read the contents of the DC.

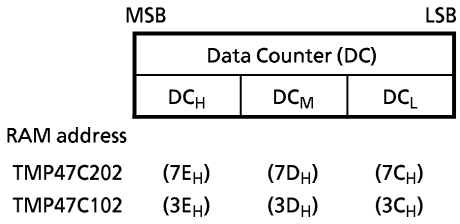
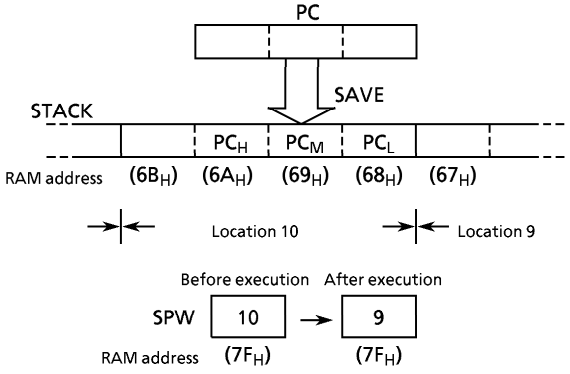


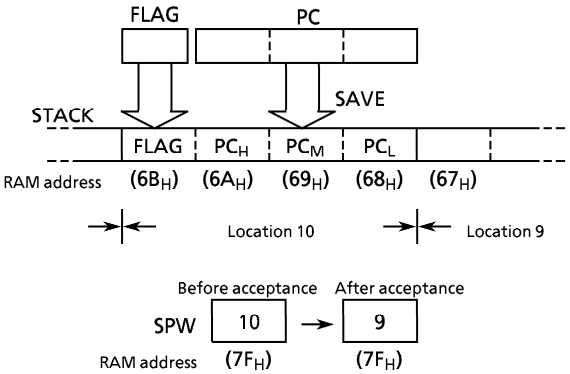
Figure 2-7. Data Counter

Example: To set the DC to 380_H.

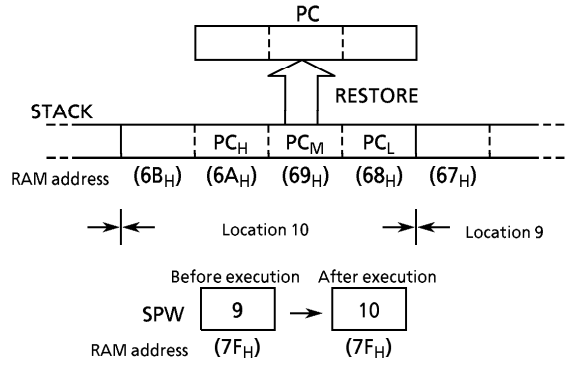
```
LD      HL,#07CH    ;  Sets RAM address of DCL to HL register pair.
ST      #0H,@HL+    ;  DC ← 380H
ST      #8H,@HL+
ST      #3H,@HL+
```



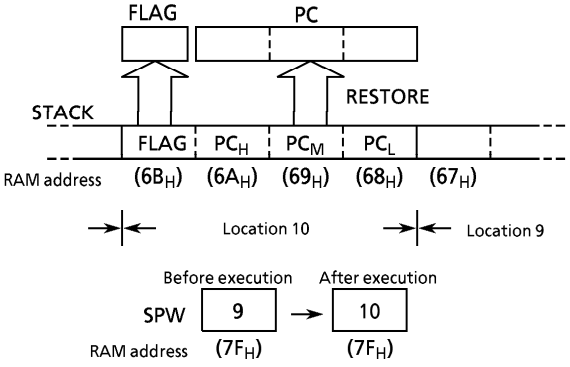
(a) At execution of the subroutine call instruction



(b) At acceptance of an interrupt



(c) At execution of the subroutine return instruction



(d) At execution of the interrupt return instruction

Figure 2-8. Accessing Stack (Save / Restore at the TMP47C202)

(4) Count registers of the timer / counters (TC1, TC2)

The TMP47C102/202 has two channels of 12-bit timer / counters. The count register of the timer / counter is assigned with a RAM addresses in unit of 4 bits, so that the initial value is set and the contents are read by using the RAM manipulation instruction.

The count registers are shared with the stack area (locations 13 and 14) described earlier, so that the stack is usable from location 13 when the timer / counter 1 is not used. When none of timer / counter 1 and timer / counter 2 are used, the stack is usable from location 14.

When both timer / counter 1 and timer/counter 2 are used, the data memory locations at addresses 77_H and $7B_H$ (37_H and $3B_H$ for the TMP47C102) can be used to store the user-processed data.

	MSB		LSB
	Timer / Counter 1 (TC1)		
	$TC1_H$	$TC1_M$	$TC1_L$
RAM address			
TMP47C202	(76_H)	(75_H)	(74_H)
TMP47C102	(36_H)	(35_H)	(34_H)

	MSB		LSB
	Timer / Counter 2 (TC2)		
	$TC2_H$	$TC2_M$	$TC2_L$
RAM address			
TMP47C202	($7A_H$)	(79_H)	(78_H)
TMP47C102	($3A_H$)	(39_H)	(38_H)

Figure 2-9. Count Registers of the Timer / Counters (TC1, TC2)

(5) Zero-page

The 16 words (at addresses 00_H through $0F_H$) of the zero page of the data memory can be used as the user flags or pointers by using zero-page addressing mode instructions (comparison, addition, transfer, and bit manipulation), providing enhanced efficiency in programming.

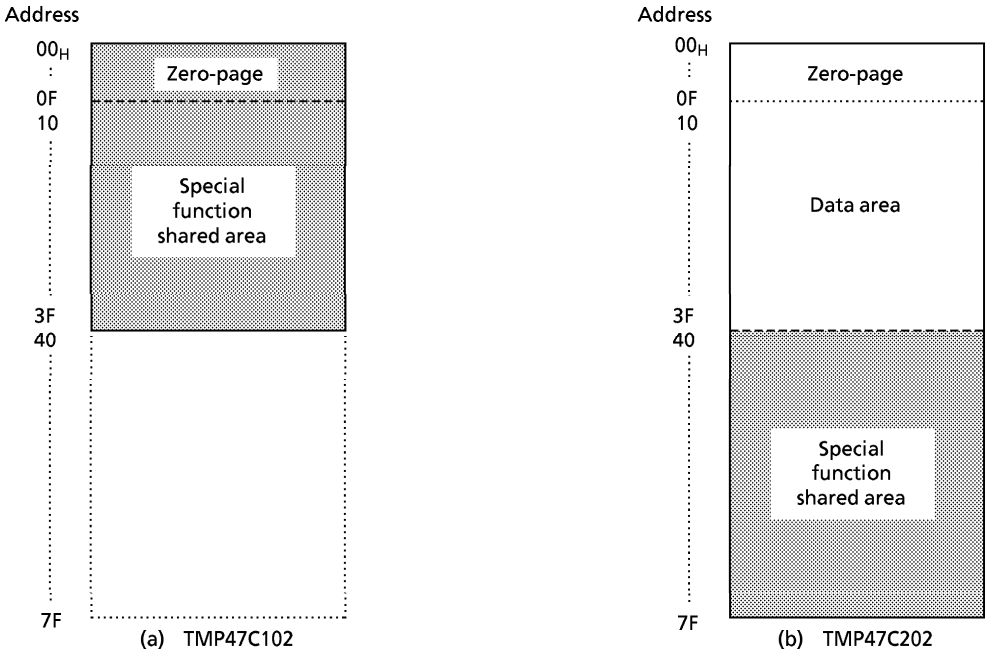
Example: To write immediate data "8" to address 09_H if bit 2 at address 04_H in the RAM is "1".

```
        TEST    04H,2       ;  Skips if bit 2 at address 04H in the RAM is "0".
        B       SKIP
        ST      #8,09H      ;  Writes "8" to address 09H in the RAM
SKIP:
```

2.4.2 Data Memory Capacity

The TMP47C102 has 64 × 4 bits (addresses 00 to $3F_H$) of the data memory (RAM), and the TMP47C202 has 128 × 4 bit (addresses 00 to $7F_H$).

When power-on is performed, the contents of the RAM become unpredictable, so that they must be initialized by the initialization routine.



Note: In the TMP47C102, the zero-page and special function shared area (stack location 3 to 0) are overlapped.
At programming, note that addresses 10 to $3F_H$ are assigned to addresses 50 to $1F_H$ in the TMP47C102. The technical data sheets for the TMP47P202V shall also be referred to.

Figure 2-10. Data Memory Capacity and Address Assignment

Example: To clear RAM (use common to the TMP47C102 and TMP47C202)

```
            LD      HL, #00H        ; HL←00H
SCLRRAM:    ST      #0, @HL+        ; RAM [HL] ←0, LR←LR + 1
            B       SCLRRAM
            ADD     H, #1           ; HR←HR + 1
            B       SCLRRAM
```

2.5 ALU and Accumulator

2.5.1 Arithmetic / Logic Unit (ALU)

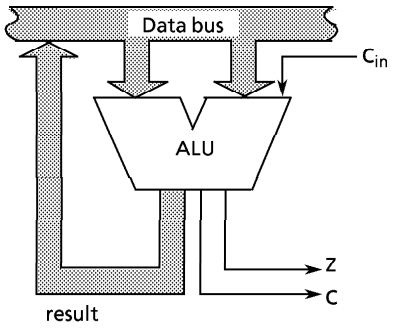
The ALU performs the arithmetic and logic operations specified by instructions on 4-bit binary data and outputs the result of the operation, the carry information (C), and the zero detect information (Z).

(1) Carry information (C)

The carry information indicates a carry-out from the most significant bit in an addition. A subtraction is performed as addition of two's complement, so that, with a subtraction, the carry information indicates that there is no borrow to the most significant bit. With a rotate instruction, the information indicates the data to be shifted out from the accumulator.

(2) Zero detect information (Z)

This information is "1" when the operation result or the data to be transferred to the accumulator/data memory is "0000_B".



Note: C_{in} indicates the carry input specified by instruction

Figure 2-11. ALU

Example: The carry information and zero detect information for 4-bit additions and subtractions.

Operation	Result	C	Z	Operation	Result	C	Z
4 + 2 =	6	0	0	8 − 1 =	7	1	0
7 + 9 =	0	1	1	2 − 2 =	0	1	1
				5 − 8 =	−3 (1101_B)	0	0

2.5.2 Accumulator (Acc)

The accumulator is a 4-bit register used to hold source data or results of the operations and data manipulations.

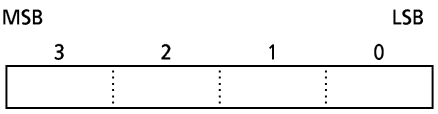


Figure 2-12. Accumulator

2.6 Flags

There are a carry flag (CF), a zero flag (ZF), a status flag (SF), and a general flag (GF), each consisting of 1 bit. These flags are set or cleared according to the condition specified by an instruction. When an interrupt is accepted, the flags are saved on the stack along with the program counter. When the [RETI] instruction is executed, the flags are restored from the stack to the states set before interrupt acceptance.

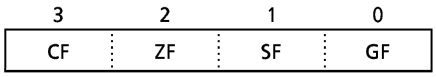


Figure 2-13. Flags

(1) Carry flag (CF)

The carry flag holds the carry information received from the ALU at the execution of an addition / subtraction with carry instruction, a compare instruction, or a rotate instruction. With a carry flag test instruction, the CF holds the value specified by it.

① Addition / subtraction with carry instructions [ADDC A, @HL], [SUBRC A, @HL]
The CF becomes the input (C_{in}) to the ALU to hold the carry information.

② Compare instructions [CMPR A, @HL], [CMPR A, #k]
The CF holds the carry information (non-borrow).

③ Rotate instructions [ROLC A], [RORC A]
The CF is shifted into the accumulator to hold the carry information (the data shifted out from the accumulator).

④ Carry flag test instructions [TESTP CF], [TEST CF]
With [TESTP CF] instruction, the content of the CF is transferred to the SF then the CF is set to "1".
With [TEST CF] instruction, the value obtained by inverting the content of the CF is transferred to the SF then the CF is cleared to "0".

(2) Zero flag (ZF)

The zero flag holds the zero detect information (Z) received from the ALU at the execution of an operational instruction, a rotate instruction, an input instrcution, or a transfer-to-accumulator instruction.

(3) Status flag (SF)

The status flag provides the branch condition for a branch instruction. Branch is performed when this flag is set to "1". Normally the SF is set to "1", so that any branch instruction can be regarded as an unconditional branch instruction. When a branch instruction is executed upon set or clear of the SF according to the condition specified by an instruction, this instruction becomes a conditional branch instruction. During reset, the SF is initialized to "1", other flags are not affected.

(4) General flag (GF)

This is a 1-bit general-purpose flag which can be set, cleared, or tested by program.

Example: When the following instructions are executed with the accumulator, H register, L register, data memory (address 07_H), and carry flag being set to "C_H", "0", "7", "5", and "1" respectively, the contents of the accumulator and flags become as follows:

Instruction	Acc after execution	Flag after execution		
		CF	ZF	SF
ADDC A, @HL	2_H	1	0	0
SUBRC A, @HL	9_H	0	0	0
CMPR A, @HL	C_H	0	0	1
AND A, @HL	4_H	1	0	1
LD A, @HL	5_H	1	0	1

Instruction	Acc after execution	Flag after execution		
		CF	ZF	SF
LD A, #0	0_H	1	1	1
ADD A, #4	0_H	1	1	0
DEC A	B_H	1	0	1
ROLC A	9_H	1	0	0
RORC A	E_H	0	0	1

2.7 System Controller

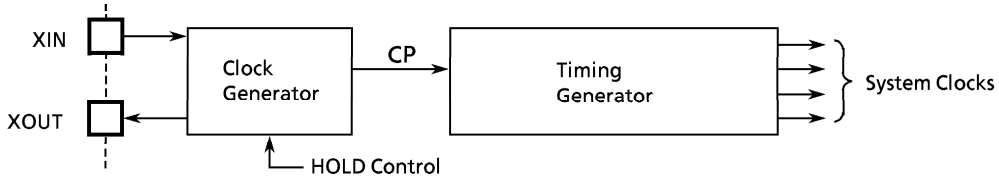
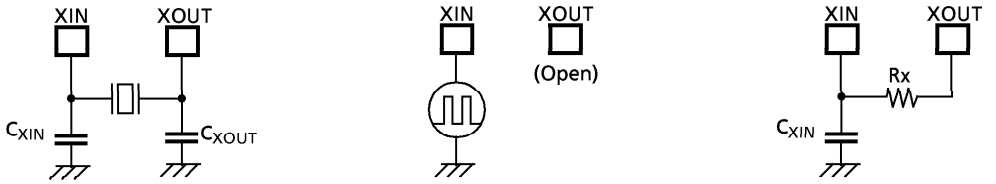


Figure 2-14. Clock Generator and Timing Generator

2.7.1 Clock Generator

The clock generator provides the basic clock pulse (CP) by which the system clock to be supplied to the CPU and the peripheral hardware is produced. The CP can be easily obtained by connecting the resonator to the XIN and XOUT pins. (RC oscillation is also possible, depending on the mask option) The clock from the external oscillator is also available. In the hold operating mode, the clock generator stops oscillating.



(a) Crystal or ceramic resonator (b) External oscillator (c) RC oscillation (mask option)

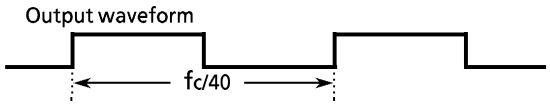
Figure 2-15. Examples of Oscillator Connection

Note: Accurate adjustment of the oscillation frequency

Although the hardware to externally and directly monitor the CP is not provided, the oscillation frequency can be adjusted by making the program to output the pulse with a fixed frequency to the port with the all interrupts disabled and timer/counters stopped and monitoring this pulse. With a system requiring the oscillation frequency adjustment, the adjusting program must be created beforehand.

Example: To output the oscillation frequency adjusting monitor pulse to port R40.

```
SFCCHK:  SET   %OP04,0
         CLR   %OP04,0
         BSS   SFCCHK
```



2.7.2 Timing Generator

The timing generator produces the system clocks from basic clock pulse (CP) which are supplied to the CPU and the peripheral hardware.

The timing generator consists of a 18-stage binary counter with a divided-by-16 prescaler. The basic clock (frequency: fc) provides the timing generator. Therefore, the output frequency at the last stage is $fc/2^{22}$[Hz]. During reset, the binary counter is cleared to "0", however, the prescaler is not cleared.

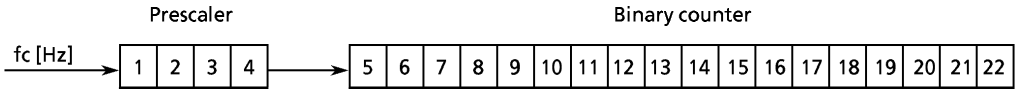


Figure 2-16. Configuration of Interval Timer

The timing generator provides the following functions:

① Generation of an internal source clock for interval timer
② Generation of an internal source clock for timer / counters
③ Generation of a warm-up time for releasing of the hold operating mode

2.7.3 Instruction Cycle

The instruction execution and the on-chip peripheral hardware operations are performed in synchronization with the basic clock pulse (CP: fc [Hz]). The smallest unit of instruction execution is called an instruction cycle. The instruction set of the TLCS-47 series consists of 1-cycle instructions and 2-cycle instructions. The former requires 1 cycle for their execution; the latter, 2 cycles. Each instruction cycle consists of 4 states (S1 through S4). Each state consists of 2 basic clock pulses.

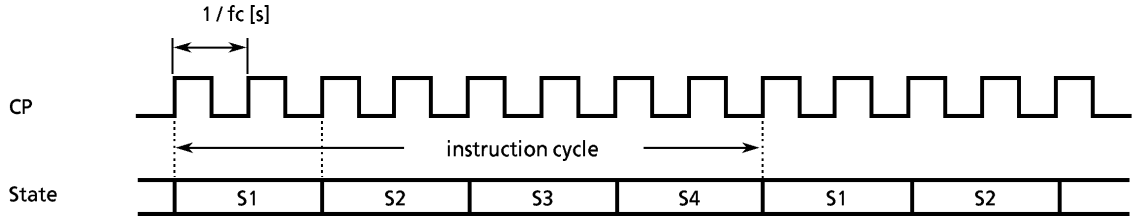


Figure 2-17. Instruction Cycle

2.7.4 Hold Operating Mode

The hold feature stops the system and holds the system's internal states active before stop with a low power. The hold operation is controlled by the command register (OP10) and the $\overline{\text{HOLD}}$ pin input. The $\overline{\text{HOLD}}$ pin input state can be known by the status register (IP0E). The $\overline{\text{HOLD}}$ pin is wired with the R82 output latch. To use this port for hold operating mode, the R82 output latch should be set to "1".

(1) Starts Hold Operating Mode

The hold operation is started when the command is set to the command register and holds the following states during the hold operation:

① The oscillator stops and the system's internal operations are all held up.
② The timing generator is cleared to "0".
③ The states of the data memory, registers, and latches valid immediately before the system is put in the hold state are all held.
④ The program counter holds the address of the instruction to be executed after the instruction ([OUT A, %OP10] or [OUT @HL, %OP10]) which starts the hold operating mode.

Hold operating mode command register
(Port address: OP10) (Initial value: *0**)

3	2	1	0
HLDMS		HWUT	

HLDMS	Starts hold operation

01: Starts hold operation in edge-release mode
11: Starts hold operation in level-release mode
*0: (Unused)

HWUT	Warm-up time at release of the hold

Example: At fc = 4 MHz

00: 2^{18}/fc [s] ..... 65.5 [ms]
01: 2^{14}/fc 4.1
10: (Unused)
11: 2^{6}/fc 0.016

Hold operating mode status register
(Port address: IP0E)

3	2	1	0
(undefined)			HOLD ($\overline{\text{INT1}}$)

HOLD	$\overline{\text{HOLD}}$ pin input state

0: $\overline{\text{HOLD}}$ pin is high
1: $\overline{\text{HOLD}}$ pin is low

*Note 1: *; Don't care*
Note 2: Do not access the OP10 when HOLD mode is not used.
Note 3: An undefined value is read from bit1 to bit3 of the IP0E with an input instruction.

Figure 2-18. Hold Operating Mode Command Register / Status Register

The hold operating mode consists of the level-sensitive release mode and the edge-sensitive release mode.

a. Level-sensitive release (back-up) mode

In this mode, the hold operation is released by setting the $\overline{\text{HOLD}}$ pin to the high level. This mode is used for the capacitor backup with power off or for the battery backup for long hours.

If the instruction to start the hold operation is executed with the $\overline{\text{HOLD}}$ pin input being high, the hold operation does not start but the release sequence (warm-up) starts immediately. Therefore, to start the hold operation in the level-sensitive release mode, that the $\overline{\text{HOLD}}$ pin input being low (the hold operation request) must be recognized in program. This recognition is performed in one of the two ways below:

① Testing HOLD (bit 0 of the status register)
② Applying the $\overline{\text{HOLD}}$ pin input also to $\overline{\text{INT1}}$ pin to generating the external interrupt 1 request.

Example: To test HOLD to start the hold operation in the level-sensitive release mode (the warm-up time = 2^{14}/fc).

```
SHOLDH: TEST    %IP0E, 0    ;  Waits until HOLD pin input goes low.
        B       SHOLDH
        LD      A, #1101B   ;  OP10←1101B
        OUT     A, %OP10
```

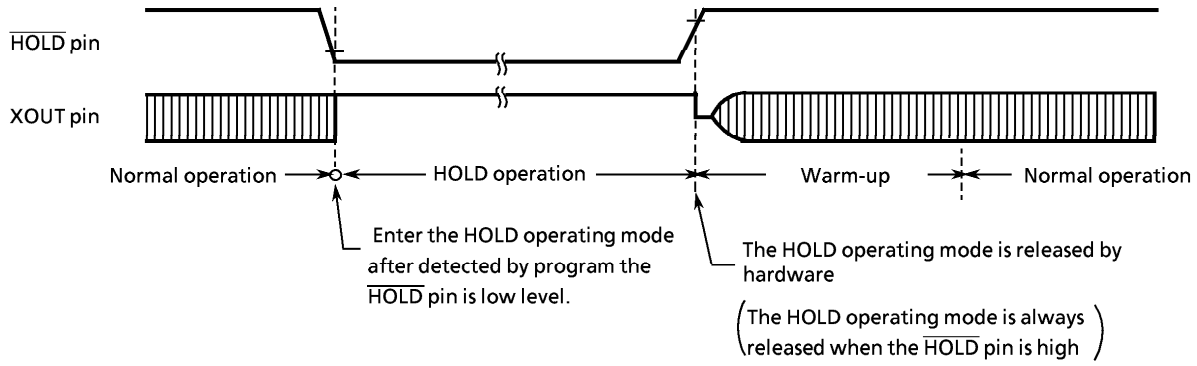


Figure 2-19. Level-sensitive release mode

b. Edge-sensitive release (clock) mode

In this mode, the hold operation is released at the rising edge of the HOLD pin input. This mode is used for applications in which a relatively short-time program processing is repeated at a certain cycle. This cyclic signal (for example, the clock supplied from the low power dissipation oscillator). In the edge-sensitive mode, even if the HOLD pin input is high, the hold operation is performed.

Example: To start the hold operation in the edge-sensitive release mode (the warm-up time = 2^{14}/fc).

```
        LD      A, #0101B   ;  OP10←0101B
        OUT     A, %OP10
```

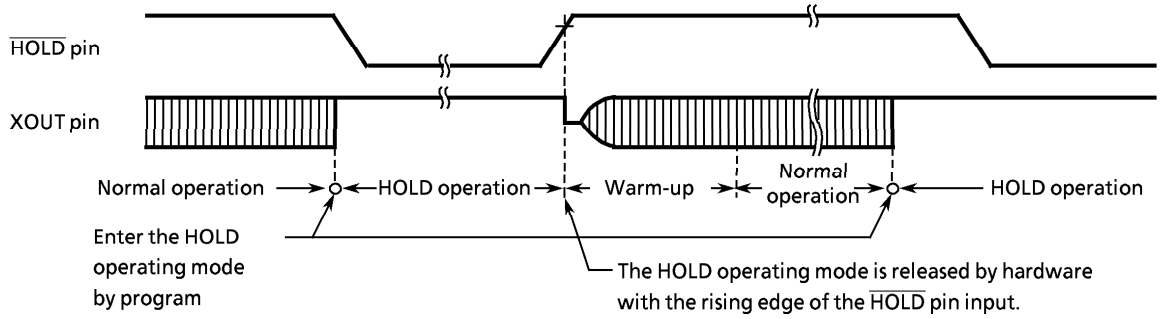


Figure 2-20. Edge-sensitive release mode

Note: In the hold operation, the dissipation of the power associated with the oscillator and the internal hardware is lowered; however, the power dissipation associated with the pin interface (depending on the external circuitry and program) is not directly determined by the hardware operation of the hold feature. This point should be considered in the system design and the interface circuit design.
In the CMOS circuitry, a current does not flow when the input level is stable at the power voltage level (V_{DD} / V_{SS}); however, when the input level gets higher than the power voltage level (by approximately 0.3 to 0.5 V), a current begins to flow. Therefore, if cutting off the output transistor at an I/O port (the open drain output pin with an input transistor connected) puts the pin signal into the high-impedance state, a current flows across the ports input transistor, requiring to fix the level by pull-up or other means.

(2) Releases Hold Operating Mode

The hold operating mode is released in the following sequence:

① The oscillator starts

② Warm-up is performed to acquire the time for stabilizing oscillation. During the warm-up , the internal operations are all stopped. One of three warm-up times can be selected by program depending on the characteristics of the oscillator used.

③ When the warm-up time has passed, an ordinary operation restarts from the instruction next to the instruction which starts the hold operation.

* The warm-up time is obtained by dividing the basic clock by the interval timer, so that, if the frequency at releasing the hold operation is unstable, the warm-up time shown in Figure 2-18. includes an error. Therefore, the warm-up time must be handled as an approximate value. The hold operation is also released by setting the $\overline{\text{RESET}}$ pin to the low level. In this case, the normal reset operation follows immediately.

2.8 Interrupt Function

2.8.1 Interrupt Controller

There are 5 interrupt sources (2 external and 3 internal). The prioritized multiple interrupt capability is supported. The interrupt latches (IL_5 through IL_0) to hold interrupt requests are provided for the interrupt sources. Each interrupt latch is set to "1" when an interrupt request is made, asking the CPU to accept the interrupt. The acceptance of interrupt can be permitted or prohibited by program through the interrupt enable master flip-flop (EIF) and interrupt enable register (EIR). When two or more interrupts occur simultaneously, the one with the highest priority determined by hardware is serviced first.

Table 2-2. Interrupt Sources

Interrupt Source			Priority	Interrupt Latch	Enable conditions	Entry address
External	Extenal Interrupt 1	(INT1)	(highest) 1	IL_5	EIF = 1	002_H
Internal	TC1 overflow Interrupt	(IOVF1)	2	IL_3	EIF = 1, EIR_2 = 1	006_H
	TC2 overflow Interrupt	(IOVF2)	3	IL_2	EIF = 1, EIR_1 = 1	008_H
	Interval Timer Interrupt	(ITMR)	4	IL_1		$00A_H$
External	External Interrupt 2	(INT2)	(lowest) 5	IL_0	EIF = 1, EIR_0 = 1	$00C_H$

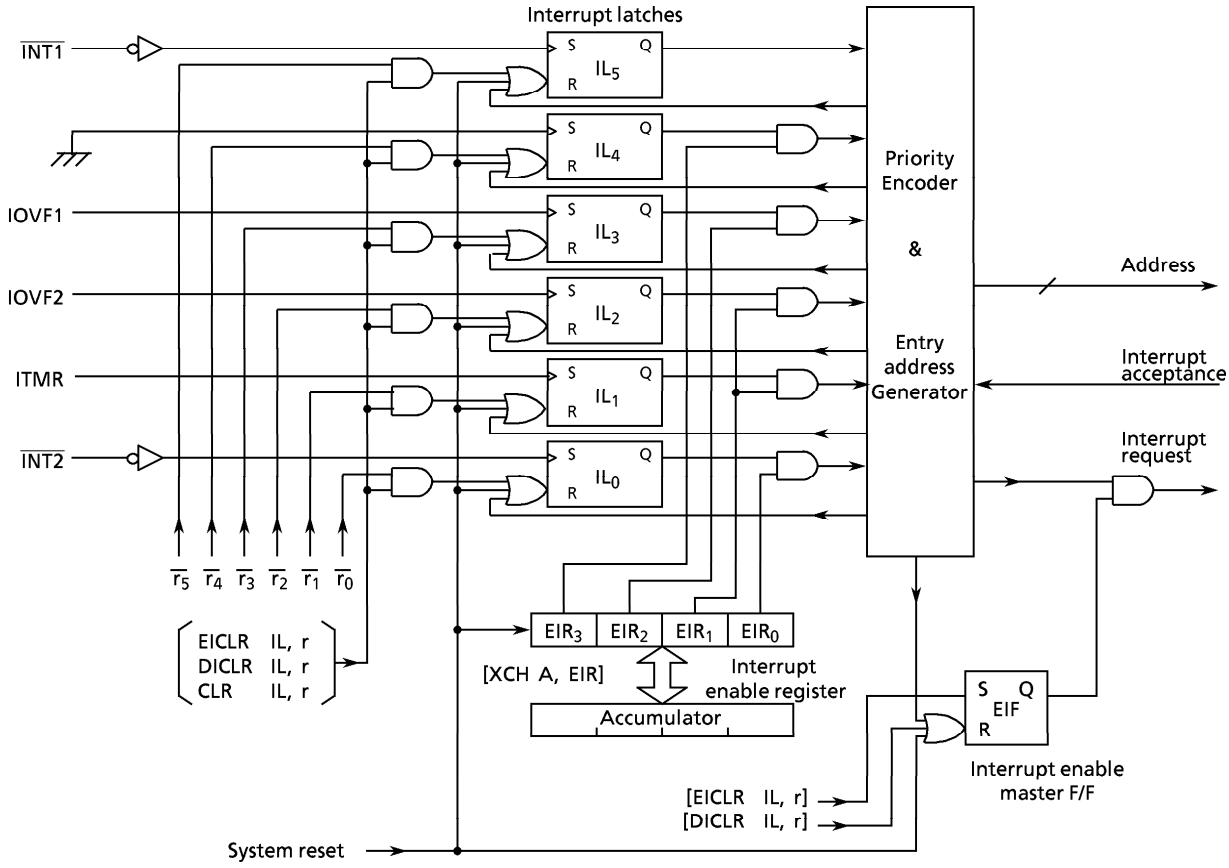


Figure 2-21. Interrupt Controller Block Diagram

(1) Interrupt enable master flip-flop (EIF)

The EIF controls the enable / disable of all interrupts. When this flip-flop is cleared to "0", all interrupts are disabled; when it is set to "1", the interrupts are enabled.

When an interrupt is accepted, the EIF is cleared to "0", temporarily disabling the acceptance of subsequent interrupts. When the interrupt service program has been executed, the EIF is set to "1" by the execution of the interrupt return instruction [RETI], being put in the enabled state again.

Set or clear of the EIF in program is performed by instructions [EICLR IL, r] and [DICLR IL, r], respectively. The EIF is initialized to "0" during reset.

(2) Interrupt enable register (EIR)

The EIR is a 4-bit register specifies the enable or disable of each interrupt except INT1. An interrupt is enabled when the corresponding bit of the EIR is "1", and an interrupt is disabled when the corresponding bit of the EIR is "0". Bit 1 of the EIR (EIR_1) is shared by both IOVF2 and ITMR interrupts.

Read/write on the EIR is performed by executing [XCH A, EIR] instruction. The EIR is initialized to "0" during reset.

(3) Interrupt latch (IL)

An interrupt latch is provided for each interrupt source. The IL is set to "1" when an interrupt request is made to ask the CPU for accepting the interrupt. Each IL is cleared to "0" upon acceptance of the interrupt. It is initialized to "0" during reset.

The ILs can be cleared independently by interrupt latch operation instructions ([EICLR IL, r], [DICLR IL, r], and [CLR IL, r]) to make them cancel interrupt requests or initialize by program. When the value of instruction field (r) is "0", the interrupt latch is cleared; when the value is "1", the IL is held. Note that the ILs cannot be set by instruction.

Example 1: To enable IOVF1, INT1, and INT2 interrupts.

```
LD      A,#0101B    ;  EIR←0101B
XCH     A,EIR
EICLR   IL,111111B  ;  EIF←1
```

Example 2: To set the EIF to "1", and to clear the interrupt latches except ITMR to "0".

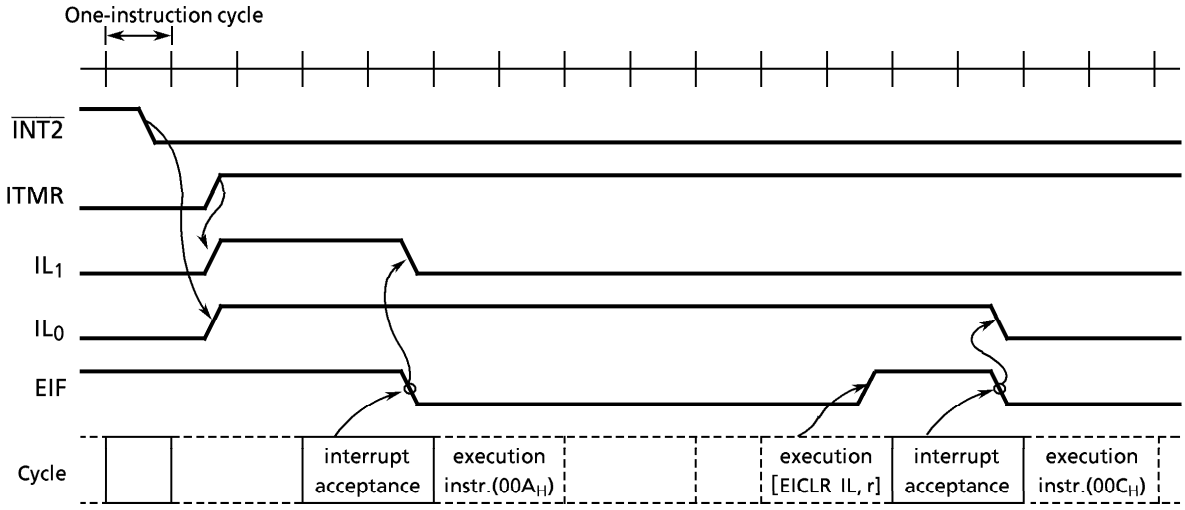
```
EICLR   IL,000010B  ;  EIF←1, IL0←0, IL2 – IL5←0
```

2.8.2 Interrupt Processing

An interrupt request is held until the interrupt is accepted or the IL is cleared by the reset or the interrupt latch operation instruction. The interrupt acknowledge processing is performed in 2 instruction cycles after the end of the current instruction execution (or after the timer/counter processing if any). The interrupt service program terminates upon execution of the interrupt return instruction [RETI].

The interrupt acknowledge processing consists of the following sequence:

① The contents of the program counter and the flags are saved on the stack.
② The interrupt entry address corresponding to the interrupt source is set to the program counter.
③ The status flag is set to "1".
④ The EIF is cleared to "0", temporarily disabling the acceptance of subsequent interrupts.
⑤ The interrupt latch for the accepted interrupt source is cleared to "0".
⑥ The instruction stored at the interrupt entry address is executed. (Generally, in the program memory space at the interrupt entry address, the branch instruction to each interrupt processing program is stored.)



Note 1: It is assumed that there is no other interrupt request and EIR = 0011B.
Note 2: The value r in the [EICLR IL, r] instruction is assumed as 111111B.
Note 3: [ ] denotes the execution of an instruction.

Figure 2-22. Interrupt Timing chart (Example)

To perform the multi-interrupt, the EIF is set to "1" in the interrupt service program, and the acceptable interrupt source is selected by the EIR. However, for the INT1 interrupt, the interrupt service is disabled under software control because it is not disabled by the EIR.

Example: The INT1 interrupt service is disabled under software control (Bit 0 of RAM [05_H] are assigned to the disabling switch of interrupt service).

```
PINT1:  TEST    05H,0    ;  Skips if RAM [05H] 0 is "1"
        B       SINT1
        RETI
SINT1:   ⋮
```

The interrupt return instruction [RETI] performs the following operations:

① Restores the contents of the program counter and the flags from the stack.
② Sets the EIF to "1" to provide the interrupt enable state again.

Note: When the time required for interrupt series is longer than that for service program is executed without executing the main program.

In the interrupt processing, the program counter and flags are automatically saved or restored but the accumulator and other registers are not. If it is necessary to save or restore them, it must be performed by program as shown in the following example. To perform the multi-interrupt, the saving RAM area never be overlapped.

Example: To save and restore the accumulator and HL register pair.

```
        XCH     HL, GSAV1      ;  RAM [GSAV1] ↔ HL
        XCH     A, GSAV1 + 2   ;  RAM [GSAV1 + 2] ↔ Acc
```

Note: The lower 2 bits of GSAV1 should be "0's".

2.8.3 External Interrupt

When an external interrupt (INT1 or INT2) occurs, the interrupt latch is set at the falling edge of the corresponding pin input ($\overline{INT1}$ or $\overline{INT2}$). The external interrupt input is the hysteresis type, each of high and low level time requires 2 or more instruction cycles for a correct interrupt operation.
The INT1 interrupt cannot be disabled by the EIR, so that it is always accepted in the interrupt enable state (EIF = "1"). Therefore, INT1 is used for an interrupt with high priority such as an emergency interrupt. When $\overline{HOLD}$ ($\overline{INT1}$) pin is used for the I/O port, the INT1 interrupt occurs at the falling edge of the pin input, so that the interrupt return [RETI] instruction must be stored at the interrupt entry address to perform dummy interrupt processing.
The INT2 interrupt can be enabled / disable by the EIR.
When R80 ($\overline{INT2}$) pin is used as the I/O port, the INT2 interrupt occurs at the falling edge of the pin input.
However the interrupt request is not accepted by clearing bit 0 of the EIR to "0".

2.9 Reset Function

When the $\overline{\text{RESET}}$ pin is held to the low level for three or more instruction cycles when the power voltage is within the operating voltage range and the oscillation is stable, reset is performed to initialize the internal states.

When the $\overline{\text{RESET}}$ pin input goes high, the reset is cleared and program execution starts from address 000_H. The $\overline{\text{RESET}}$ pin is a hysteresis input with a pull-up resistor (220 kΩ typ.). Externally attaching a capacitor and a diode implement a simplified power-on-reset operation.

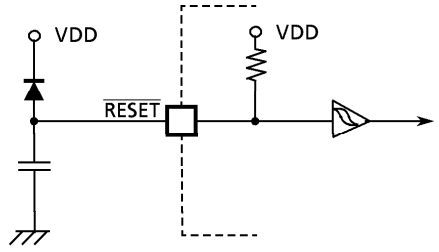


Figure 2-23. Simplified Power-On-Reset

Table 2-3. Initialization of Internal States by Reset Operation

On-chip hardware	Initial value	On-chip hardware	Initial value
Program counter (PC)	000_H	Output latch (I/O ports or Output ports)	Refer to "INPUT / OUTPUT Circuitry".
Status flag (SF)	1		
Interrupt enable master flip-flop (EIF)	0		
Interrupt enable register (EIR)	0_H	Command register	Refer to the description of each relative command register.
Interrupt latch (IL)	"0"		
Interval timer	"0"		

3. Peripheral Hardware Function

3.1 Ports

The data transfer with the external circuit and the command / status / data transfer with the internal circuit are performed by using the I/O instructions (13 kinds). There are 4 types of ports:

① I/O port ; Data transfer with external circuit
② Command register ; Control of internal circuit
③ Status register ; Reading the status signal from internal circuit
④ Data register ; Data transfer with internal circuit

These ports are assigned with port addresses (00_H through $1F_H$). Each port is selected by specifying its port address in an I/O instruction. Table 3-1 lists the port address assignments and the I/O instructions that can access the ports.

3.1.1 I/O Timing

(1) Input timing

External data is read from an input port or an I/O port in the S3 state of the second instruction cycle during the input instruction (2-cycle instruction) execution. This timing cannot be recognized from the outside, so that the transient input such as chattering must be processed by program.

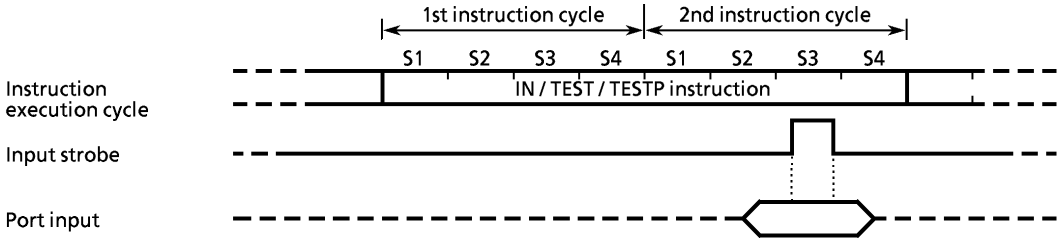


Figure 3-1. Input Timing

(2) Output timing

Data is output to an output port or an I/O port in the S4 state of the second instruction cycle during the output instruction (2-cycle instruction) execution.

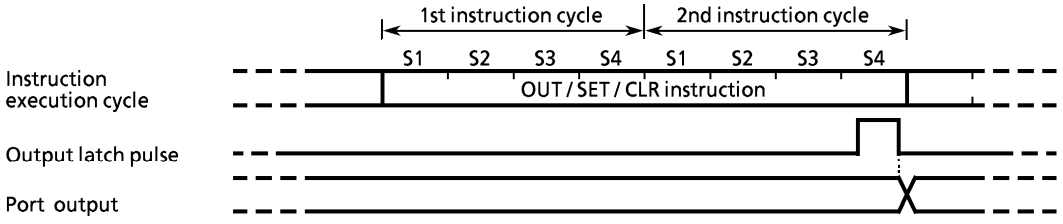


Figure 3-2. Output Timing

3.1.2 I/O Ports

The TMP47C102/202 have 5 I/O ports (15 pins) each as follows:

① R4, R5 ; 4-bit input / output
② R7 ; 2bit input / output (shared with watchdog timer output)
③ R8 ; 4-bit input / output (shared with external interrupt input and timer / counter input)
④ KE ; 1-bit sense input (shared with hold request / release signal input)

Each output port contains a latch, which holds the output data. The input ports have no latch; therefore, it is desired to hold data externally until it is read or read twice or more before processing it.

Table 3-1. Port Address Assignments and Available I/O Instructions

Port address (**)	Port		Input / Output instructions						
	Input (IP**)	Output (OP**)	IN %p, A IN %p, @HL	OUT A, %p OUT @HL, %p	OUT #k, %p	OUTB @HL	SET %p, b CLR %p, b	TEST %p, b TESTP %p, b	SET @L CLR @L TEST @L
00_H	—	—	—	—	—	—	—	—	—
01	—	—	—	—	—	—	—	—	—
02	—	—	—	—	—	—	—	—	—
03	—	—	—	—	—	—	—	—	—
04	R4 input port	R4 output port	○	○	○	—	○	○	○
05	R5 input port	R5 output port	○	○	○	—	○	○	○
06	—	—	—	—	—	—	—	—	—
07	R7 input port	R7 output port	○	○	○	—	○	○	○
08	R8 input port	R8 output port	○	○	○	—	○	○	—
09	—	—	—	—	—	—	—	—	—
0A	—	—	—	—	—	—	—	—	—
0B	—	—	—	—	—	—	—	—	—
0C	—	—	—	—	—	—	—	—	—
0D	—	—	—	—	—	—	—	—	—
0E	HOLD status	—	○	—	—	—	—	○	—
0F	—	—	—	—	—	—	—	—	—
10_H	Undefined	Hold operating mode control	—	○	—	—	—	—	—
11	Undefined	—	—	—	—	—	—	—	—
12	Undefined	—	—	—	—	—	—	—	—
13	Undefined	—	—	—	—	—	—	—	—
14	Undefined	—	—	—	—	—	—	—	—
15	Undefined	Watchdog timer control	—	○	—	—	—	—	—
16	Undefined	—	—	—	—	—	—	—	—
17	Undefined	—	—	—	—	—	—	—	—
18	Undefined	—	—	—	—	—	—	—	—
19	Undefined	Interval Timer interrupt control	—	○	—	—	—	—	—
1A	Undefined	—	—	—	—	—	—	—	—
1B	Undefined	—	—	—	—	—	—	—	—
1C	Undefined	Timer / Counter 1 control	—	○	—	—	—	—	—
1D	Undefined	Timer / Counter 2 control	—	○	—	—	—	—	—
1E	Undefined	—	—	—	—	—	—	—	—
1F	Undefined	—	—	—	—	—	—	—	—

Note: "—— "means the reserved state. Unavailable for the user programs.

(1) Port R4 (R43 to R40), R5 (R53 to R50), R7 (R71 to R70)

Ports R4 and R5 are 4-bit I/O port with a latch. When used as an input port, the latch must be set to "1". The latch is initialized to "1" during reset.

These 3 ports (10 pins) can be set, cleared, and tested for each bit as specified by L register indirect addressing bit manipulation instructions ([SET @L], [CLR @L], and [TEST @L]). Table 3-2 lists the pins (I/O ports) that correspond to the contents of L register.

Example: To clear R43 output as specified by the L register indirect addrressing bit manipulation instruction.

```
LD      L, #0011B       ;  Sets R43 pin address to L register
CLR     @L              ;  R43←0
```

Table 3-2. Relationship between L register contents and I/O port bits

L register 3 2 1 0	PIN
0 0 0 0	R40
0 0 0 1	R41
0 0 1 0	R42
0 0 1 1	R43

L register 3 2 1 0	PIN
0 1 0 0	R50
0 1 0 1	R51
0 1 1 0	R52
0 1 1 1	R53

L register 3 2 1 0	PIN
1 1 0 0	R70
1 1 0 1	R71

(a) R4 (R43 to R40), R5 (R53 to R50)

Port R4 (Port address: OP04 / IP04)

3	2	1	0
R43	R42	R41	R40

Port R4 is high current output. Port R5 is middle current output. These ports can directly drive LEDs.

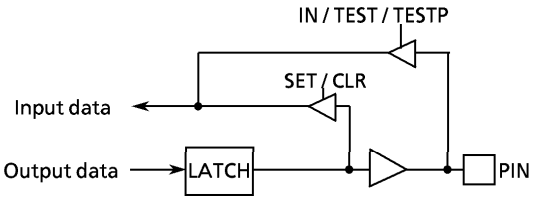


Figure 3-3. Ports R4, R5

Port R5 (Port address: OP05 / IP05)

3	2	1	0
R53	R52	R51	R50

(b) Port R7 (R71 to R70)

Port R7 is 2-bits I/O port with latch. R70 pin is shared by the watchdog timer output. To use R70 pin for the watchdog timer output, the latch should be set to "1". The latch is initialized to "1" during reset. R71 pin is normal I/O pin. R72 and R73 pins do not exist actually but "1" is read when an input instruction is executed.

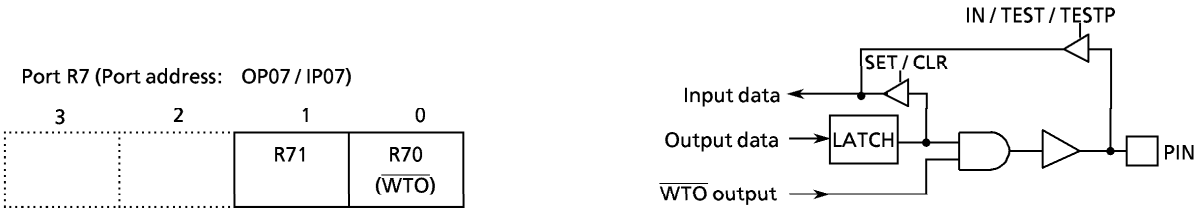


Figure 3-4. Ports R7

(2) Port R8 (R83 to R80)

Port R8 is a 4-bit I/O port with a latch. When used as an input port, the latch must be set to "1". The latch is initialized to "1" during reset.

Port R8 is shared with the external interrupt input pin and the timer/counter input pin. To use this port for one of these functional pins, the latch should be set to "1". To use it for an ordinary I/O port, the acceptance of external interrupt should be disabled or the event counter/pulse width measurement modes of the timer/counter should be disabled.

Note: When R82 (INT1) pin is used for an I/O port, external interrupt 1 occurs upon detection of the falling edge of pin input, and if the interrupt enable master flip-flop is enabled, the interrupt request is always accepted. So that a dummy interrupt processing must be performed (only the interrupt return instruction [RETI] is executed).

With R80 (INT2) pin, external interrupt 2 occurs like R82 in but bit 0 of the interrupt enable register (EIR_0) is only kept at "0", not accepting the interrupt request.

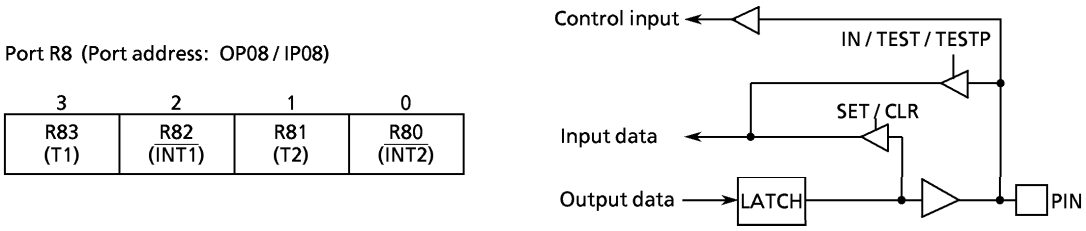


Figure 3-5. Port R8

(3) Port KE (KE0)

Port KE is a 1-bit sense input port shared with the hold request / release signal input in (HOLD). This input port is assigned to the least significant bit of Port address IP0E and is processed as the data with inverted polarity. For example, if an input instruction is executed with the pin on the high level, "0" is read. The bit1 through bit3 of port KE, an undefined value is read when an input instruction is executed.

Example: To wait until KE0 pin goes low.

```
SWAIT   :   TEST    %IP0E,0         ; Waits if KE0 pin = "H".
            B       SWAIT
```

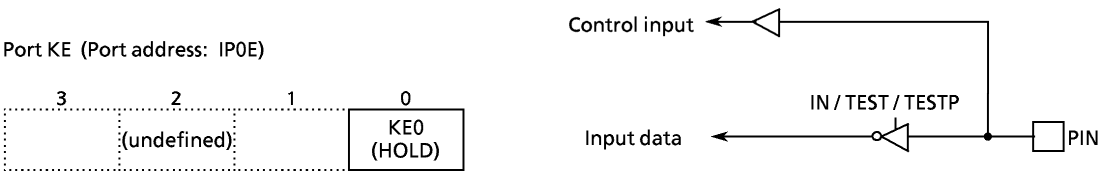


Figure 3-6. Port KE

3.2 Interval Timer Interrupt (ITMR)

The interval timer can be used to generate an interrupt with a fixed frequency. Internal timer interrrupt is control by the command register (OP19). An interval timer interrupt is generated at the first rising edge of the binary counters output after the command has been set. The interval timer is not cleared by command, so that the first interrupt may occur earlier than the preset interrupt period.

Example: To set the interval timer interrupt frequency to fc/2^{12} [Hz].

```
LD      A,  #0110B
OUT     A,  %OP19
```

Interval Timer interrupt command register
(Port address: OP19) (Initial value: 0000)

3	2	1	0
TMRE		TMRF	

TMRE	Interrupt Enable / Disable

00: Stopped
01: Enable
1*: (Unused)

*Note: *; Don't care*

TMRE	Interrupt frequency

Example: At fc = 4.19 MHz

00: fc/2^{10} [Hz] ..... 4096 [Hz]
01: fc/2^{11} 2048
10: fc/2^{12} 1024
11: fc/2^{13} 512

Figure 3-7. Command Register

3.3 Timer / Counters (TC1, TC2)

The TMP47C102/202 contain two 12-bit timer / counters (TC1, TC2). RAM addresses are assigned to the count register in unit of 4 bits, permitting the initial value setting and counter reading through the RAM manipulation instruction. When the timer / counter is not used, the mode selection may be set to "stopped" to use the RAM at the address corresponding to the timer / counter for storing the ordinary user-processed data.

	MSB		LSB
	Timer / Counter 1 (TC1)		
	$TC1_H$	$TC1_M$	$TC1_L$
RAM address			
TMP47C202	(76_H)	(75_H)	(74_H)
TMP47C102	(36_H)	(35_H)	(34_H)

	MSB		LSB
	Timer / Counter 2 (TC2)		
	$TC2_H$	$TC2_M$	$TC2_L$
RAM address			
TMP47C202	($7A_H$)	(79_H)	(78_H)
TMP47C102	($3A_H$)	(39_H)	(38_H)

Figure 3-8. The Count registers of the Timer / Counters (TC1, TC2)

3.3.1 Functions of Timer / Counters

The timer / counters provide the following functions:

① Event counter
② Programmable timer
③ Pulse width measurement

Timer / Counter 1 control command register
(Port address: OP1C) (Initial value: 0000)

3	2	1	0
TC1MS		IPR1	

TC1MS	Mode selection

00: Stopped
01: Event counter mode
10: Timer mode
11: Pulse width measurement mode

IPR1	Internal pulse rate selection

Example: At fc = 4.19 MHz

00: $fc/2^{10}$[Hz] ..... 4096 [Hz]
01: $fc/2^{14}$ 256
10: $fc/2^{18}$ 16
11: $fc/2^{22}$ 1

Timer / Counter 2 control command register
(Port address: OP1D) (Initial value: 0000)

3	2	1	0
TC2MS		IPR2	

TC2MS	Mode selection

00: Stopped
01: Event counter mode
10: Timer mode
11: Pulse width measurement mode

IPR2	Internal pulse rate selection

Example: At fc = 4.19 MHz

00: $fc/2^{10}$[Hz] ..... 4096 [Hz]
01: $fc/2^{14}$ 256
10: $fc/2^{18}$ 16
11: $fc/2^{22}$ 1

Note: fc; Basic clock frequency [Hz]

Figure 3-9. Timer / Counter Control Command Registers

3.3.2 Control of Timer / Counters

The timer / counters are controlled by the command registers. The command register is accessed as port address OP1C for TC1 and port address OP1D for TC2. These registers are initialized to "0" during reset.
The timer / counter increments at the rising edge of each count pulse. Counting starts with the first rising edge of the count pulse generated after the command has been set. Count operation is performed in one instruction cycle after the current instruction execution, during which the execution of a next instruction and the acceptance of an interrupt are delayed. If counting is requested by both TC1 and TC2 simultaneously, the request by TC1 is preferred. The request by TC2 is accepted in the next instruction cycle. Therefore, during count operation, the apparent instruction execution speed drops as counting occurs more frequently.
The timer / counter causes an interrupt upon occurrence of an overflow (a transition of the count value from FFF_H to 000_H). If the timer / counter is in the interrupt enabled state and the overflow interrupt is accepted immediately after its occurrence, the interrupt is processed in the sequence shown in Figure 3-9. Note that counting continues if there is a count request after overflow occurrence.

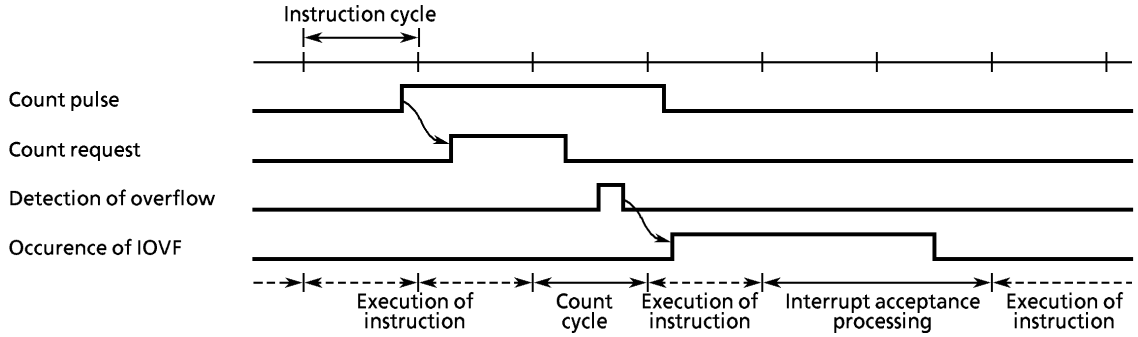


Figure 3-10. Timer/Counter Overflow Interrupt Timing

(1) Event counter mode

In the event counter mode, the timer/counter increments at each rising edge of the external pin (T1, T2) input. T1 and T2 pins are also used as the R83 and R81 pins. To use these pins as the T/C input, set the output latch of R83 and R81 to "1". At reset, output latch is initialized to "1". The maximum applied frequency of the external pin input is fc/32 for the 1-channel operation; for the 2-channel operation, the frequency is fc/32 for TC1 and fc/40 for TC2. The apparent instruction execution speed drops most to (9/11) × 100 = 82% when TC1 and TC2 are operated at the maximum applied frequency because the count operation is inserted once every 4 instruction cycles for TC1 and every 5 cycles for TC2. For example, the instruction execution speed of 2 μs drops to 3.64 μs.

Example: To operate TC2 in the event counter mode

```
LD      A, #0100B    ;  OP1D←01**B
OUT     A, %OP1D
```

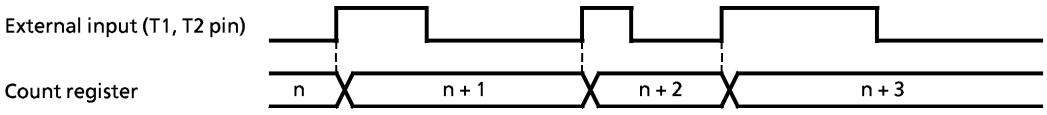


Figure 3-11. Event Counter Mode Timing chart

(2) Timer mode

In the timer mode, the timer / counter increments at the rising edge of the internal pulse generated from the interval timer. One of 4 internal pulse rates can be selected by the command register. The selected rate can be initially set to the timer / counter to generate an overflow interrupt in order to create a desired time interval.

When an internal pulse rate of $fc/2^{10}$ is used, a count operation is inserted once every 128 instruction cycles, so that the apparent instruction execution speed drops by (1/127) × 100 = 0.8%. For example, the instruction execution speed of 2 μs drops to 2.016 μs.

In the timer mode, R83 (T1) and R81 (T2) pins provide the ordinary I/O ports.

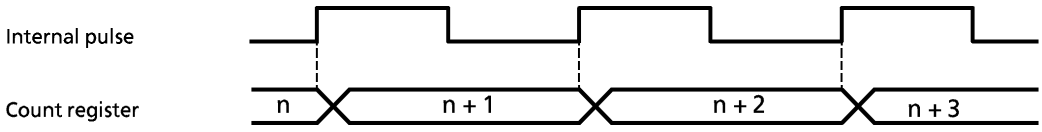


Figure 3-12. Timer Mode Timing chart

Example: To generate an overflow interrupt (at fc = 4 MHz) by the TC1 after 100 ms.

```
LD      HL,  #0F4H    ;  TC1←E79H (setting of the count register)
ST      #9,  @HL+
ST      #7,  @HL+
ST      #0EH,  @HL+
LD      A,  #1000B    ;  OP1C←1000B
OUT     A,  %OP1C
LD      A,  #0100B    ;  EIR←0100B (enables interrupt)
XCH     A,  EIR
EICLR   IL,  110111B  ;  EIF←1, IL3←0
```

**** Calculating the preset value of the count register***

The preset value of the count register is obtained from the following relation:

2^{12} – (interrupt setting time) × (internal pulse rate)

For example, to generate an overflow interrupt after 100 ms at fc = 4 MHz with the internal pulse rate of fc/2^{10}, set the following value to the count register as the preset value:

$2^{12} - (100 \times 10^{-3}) \times (4 \times 10^{6}/2^{10}) = 3705 = E79_H$

**** The apparent execution rate is calculated as following.***

$$1 \div \left\{ \frac{\text{(Fundamental clock frequency)} / 8}{\text{(Internal pulse rate)}} - 1 \right\} \times 100\ [\%]$$

Table 3-3. Internal Pulse Rate Selection

Internal pulse rate	Max. setting time	Example: At fc = 4.194304 MHz	
		Internal pulse rate	Max. setting time
fc/2^{10} [Hz]	2^{22}/fc [s]	4096 [Hz]	1 [s]
fc/2^{14}	2^{26}/fc	256	16
fc/2^{18}	2^{30}/fc	16	256
fc/2^{22}	2^{34}/fc	1	4096

(3) Pulse width measurement mode

In the pulse width measurement mode, the timer/counter increments with the pulse obtained by sampling the external pin (T2) by the internal pulse. As shown in Figure 3-13, the timer/counter increments only while the external pin input is high. The maximum applied frequency to the external pin input must be one that is enough for analyzing the count value. Normally, a frequency sufficient slower than the internal pulse rate setting is applied to the external pin.

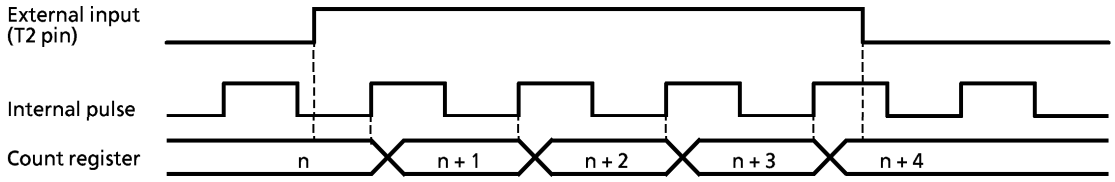


Figure 3-13. Pulse Width Measurement Mode Timing chart

3.4 Watchdog Timer (WDT)

The purpose of the watchdog timer is to detect the malfunction (ranaway) of program due to external noise or other causes and return the operation to the normal condition.

The watchdog timer output is output to R70 must be set to "1". Further, during reset, the output latch of R70 is set to "1", and the watchdog timer becomes disable state.

The initialization at time of runaway will become possible when the $\overline{\text{WTO}}$ pin and $\overline{\text{RESET}}$ pin are connected each other.

3.4.1 Configuration of Watchdog Timer

The watchdog timer consists of 3-stage binary counter, flip-flop (F/F), and its control circuit. The F/F is set to "1" during reset, and cleared to "0" at the rising edge of the binary counter output.

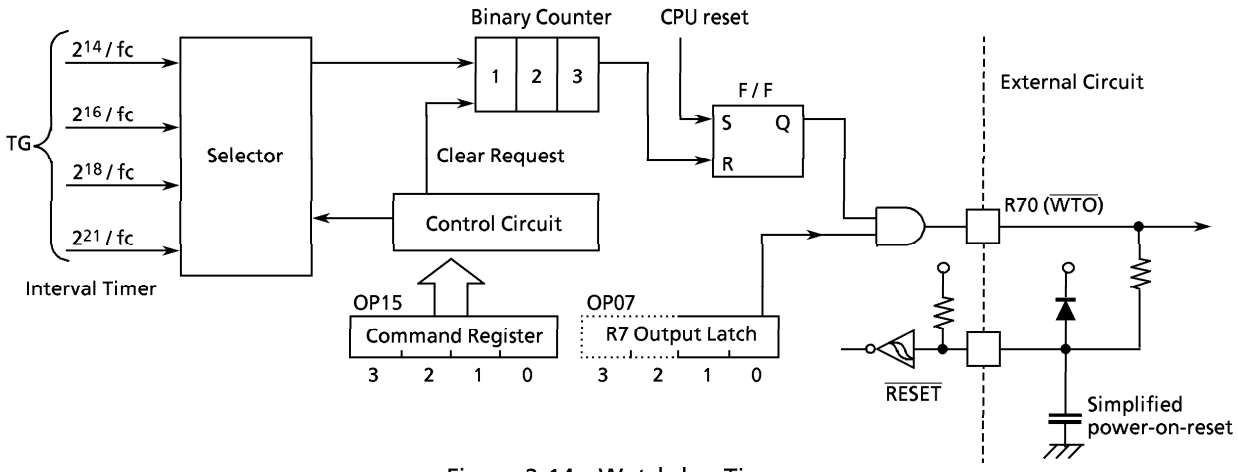


Figure 3-14. Watchdog Timer

3.4.2 Control of watchdog timer

The watchdog timer is controlled by the command register (OP15). This command register is initialized to "1000_B" during reset. The following are procedure to detect the malfunction (runaway) of CPU by the watchdog timer.

① At first, detection time of the watchdog timer should be set and binary counter should be cleared.
② The watchdog timer should be become enable.
③ Binary counter must be cleared before the detection time of the watchdog timer. When the runaway of CPU is taken place for some reason and binary counter is not cleared, the F/F is cleared to "0"at the rising edge of the binary counter and signal of runaway detection is become active ($\overline{WTO}$ output is "L").

Example: To set the watchdog detection time (2^{21}/fc [s]). And to enable the watchdog timer.

```
        LD      A, #0010B
        OUT     A, %OP15
        LD      A, #0110B
        OUT     A, %OP15
Within  :
WDT     :
detect  :
time    LD      A, #0110B
        OUT     A, %OP15
        :
        :
```

Note: It is not necessary to set RWT to "1" by program. Note that both EWT (Enable Watchdog Timer) and RWT should not be set to "1" at the same time.

Watchdog Timer control command register
(Port address: OP15) (Initial value: 1000)

3	2	1	0
RWT	EWT	TWT	

RWT	Clears binary counter

0: Clears binary counter
(After clear, automatically "1" is set)

EWT	Enable / Disable

0: Disable
1: Enable

TWT	Setting of watchdog timer detection time

Example: At fc = 4.19 MHz

00: 2^{17}/fc [s] ..... 31.25 [ms]
01: 2^{19}/fc 125
10: 2^{21}/fc 500
11: 2^{24}/fc 4000

Figure 3-15. Command Register

Port Condition by RESET Operation

The transition of Port condition by RESET operation is shown as below.

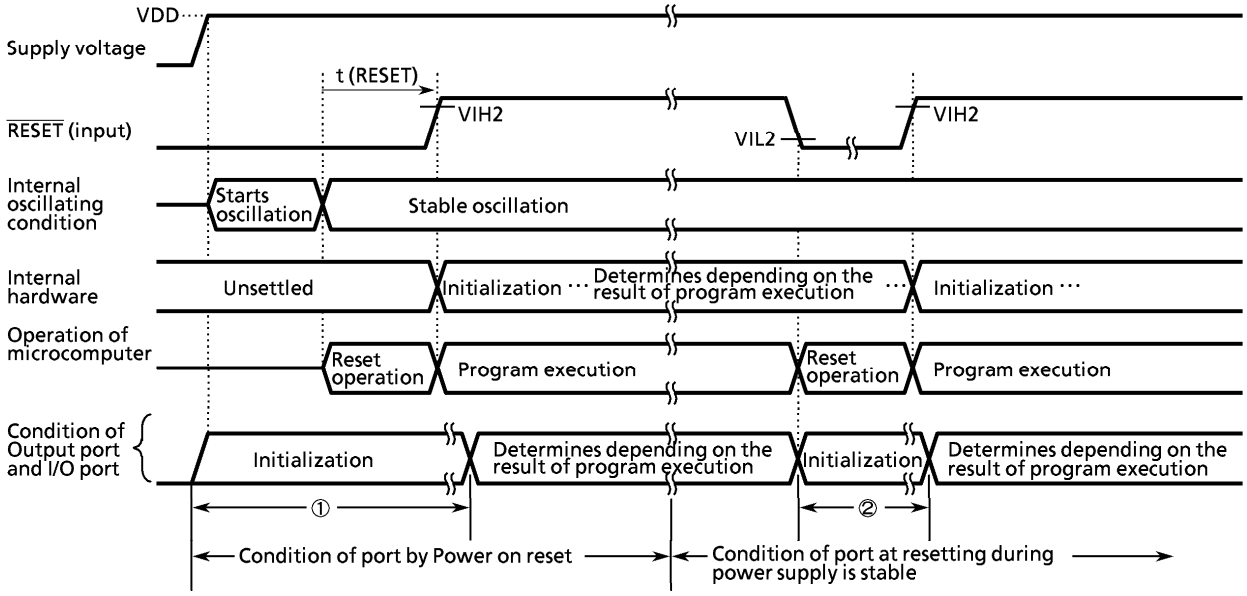


Figure 3-16. Port condition by Reset operation

Note 1: t (RESET) > 24/fc

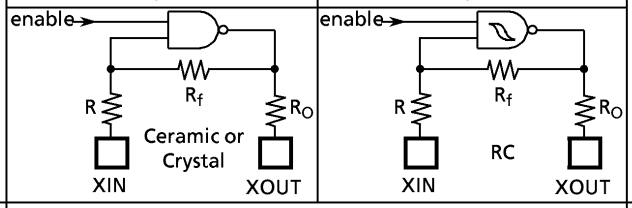
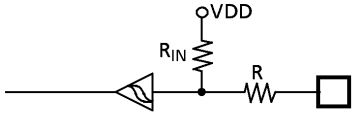
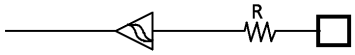
Note 2: VIL2: Stands for low level input voltage of $\overline{\text{RESET}}$ *pin.*
VIH2: Stands for high level input voltage of $\overline{\text{RESET}}$ *pin.*

Note 3: The term from power on reset to the time program is executed (above ①) and also the term starting from reset operation during power supply is stable to the program is executed (above ②), the port is on the initial condition. The initial condition of Port differs from I/O circuit by each port, refer to the section of "INPUT/OUTPUT CIRCUITRY". Thus, when using Port as an output pin, in the term of the above ① and ②, the voltage level on the signal that connects with the output pin of Port to the input pin of external application circuit should be determined by the external circuitry such as pull-up resistor and / or pull-down resistor.

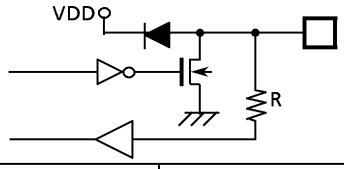
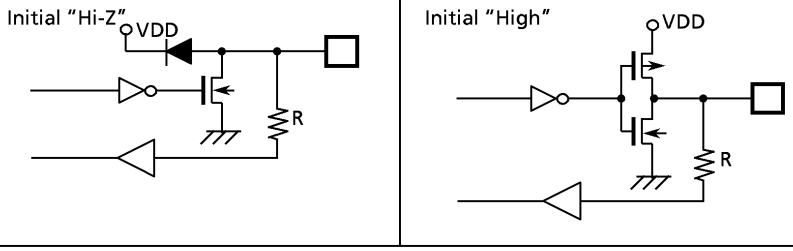
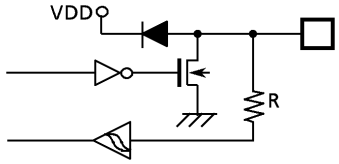
Input / Output Circuitry

The input / output circuitries of the TMP47C102/202 are shown as below, any one of the circuitries can be chosen by a code (FA, FB, FD or FE) as a mask option.

(1) Control pins

Control Pin	I/O	Circuitry and Code	Remarks
XIN XOUT	Input Output	FA, FB / FD, FE 	Resonator connecting pins R = 1 kΩ (typ.) R_f = 1.5 MΩ (typ.) R_O = 2 kΩ (typ.)
$\overline{RESET}$	Input		Hysteresis input Pull-up resistor R_{IN} = 220 kΩ (typ.) R = 1 kΩ (typ.)
$\overline{HOLD}$ ($\overline{KE0}$)	Input (Input)		Hysteresis input R = 1 kΩ (typ.)

(2) I/O ports

Port	I/O	Input / Output Circuitry and Code	Remarks
R4 R7	I/O		Sink open drain output Initial "Hi-Z" R = 1 kΩ (typ.)
R5	I/O	FA, FD / FB, FE 	Sink open drain or push-pull output R = 1 kΩ (typ.)
R8	I/O		Sink open drain output Initial "Hi-Z" Hysteresis input R = 1 kΩ (typ.)

Electrical Characteristics

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter	Symbol	Pins		Ratings	Unit
Supply Voltage	V_{DD}			– 0.3 to 6.5	V
Input Voltage	V_{IN}			– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT}			– 0.3 to V_{DD} + 0.3	V
Output Current (Per 1 pin)	I_{OUT1}	Port R4		30	mA
	I_{OUT2}	Port R5		15	
	I_{OUT3}	Ports R7, R8		3.2	
Output Current (Total)	ΣI_{OUT1}	Port R4, R5		60	mA
Power Dissipation [Topr = 70°C]	PD		DIP	300	mW
			SOP	180	
Soldering Temperature (time)	Tsld			260 (10 s)	°C
Storage Temperature	Tstg			– 55 to 125	°C
Operating Temperature	Topr			– 30 to 70	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Conditions (V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Symbol	Pins		Conditions		Min	Max	Unit
Supply Voltage	V_{DD}		Normal mode	Crystar or ceramic	fc = 6.0 MHz	4.5	5.5	V
					fc = 4.2 MHz	2.7		
				RC	fc = 2.5 MHz	2.2		
			HOLD mode	–	–	2.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input		In the normal operating area		V_{DD} × 0.7	V_{DD}	V
	V_{IH2}	Hysteresis Input				V_{DD} × 0.75		
	V_{IH3}			In the HOLD mode		V_{DD} × 0.9		
Input Low Voltage	V_{IL1}	Except Hysteresis Input		In the normal operating area		0	V_{DD} × 0.3	V
	V_{IL2}	Hysteresis Input					V_{DD} × 0.25	
	V_{IL3}			In the HOLD mode			V_{DD} × 0.1	
Clock Frequency	fc	XIN, XOUT		V_{DD} = 4.5 to 5.5 V		0.4	6.0	MHz
				V_{DD} = 2.7 to 5.5 V			4.2	
				V_{DD} = 2.2 to 5.5 V (RC)			2.5	

Note: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

DC Characteristics

(V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Symbol	Pins	Conditions	Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis Input		–	0.7	–	V
Input Current	I_{IN1}	$\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5 V, V_{IN} = 5.5 V / 0 V	–	–	± 2	μA
	I_{IN2}	Open drain output ports					
Input Resistance	R_{IN}	$\overline{RESET}$		100	220	450	kΩ
Input Low Current	I_{IL}	Push-pull output ports	V_{DD} = 5.5 V, V_{IN} = 0.4 V	–	–	– 2	mA
Output Leakage Current	I_{LO}	Open drain output ports	V_{DD} = 5.5 V, V_{OUT} = 5.5 V	–	–	2	μA
Output High Voltage	VOH	Push-pull output ports	V_{DD} = 4.5 V, I_{OH} = – 200 μA	2.4	–	–	V
			V_{DD} = 2.2 V, I_{OH} = – 5 μA	2.0	–	–	
Output Low Voltage	V_{OL}	Port R7, R8	V_{DD} = 4.5 V, I_{OL} = 1.6 mA	–	–	0.4	V
			V_{DD} = 2.2 V, I_{OL} = 20 μA	–	–	0.1	
Output Low Current	I_{OL1}	Port R4	V_{DD} = 4.5 V, V_{OL} = 1.0 V	–	20	–	mA
	I_{OL2}	Port R5		–	7	–	
Supply Current (in the Normal operating mode)	I_{DD}		V_{DD} = 5.5 V, fc = 4 MHz	–	2	4	mA
			V_{DD} = 5.5 V, fc = 4 MHz	–	1	2	
			V_{DD} = 3.0 V, fc = 400 kHz	–	0.5	1	
Supply Current (in the HOLD operating mode)	I_{DDH}		V_{DD} = 5.5 V	–	0.5	10	μA

Note 1: Typ. values show those at Topr = 25°C, V_{DD} = 5 V.

Note 2: Input Current I_{IN1}: The current through resistor is not included.

Note 3: Supply Current: V_{IN} = 5.3 V / 0.2 V (V_{DD} = 5.5 V) or 2.8 V / 0.2 V (V_{DD} = 3.0 V)

AC Characteristics

(V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Symbol	Conditions		Min	Typ.	Max	Unit
Instruction Cycle Time	tcy		V_{DD} = 4.5 to 5.5 V	1.3	–	20	μs
			V_{DD} = 2.7 to 5.5 V	1.9			
			V_{DD} = 2.2 to 5.5 V	3.2			
High level Clock pulse Width	t_{WCH}	For external clock operation	$V_{DD} \geqq 2.7$ V	80	–	–	ns
			$V_{DD} < 2.7$ V	160			
Low level Clock pulse Width	t_{WCL}		$V_{DD} \geqq 2.7$ V	80			
			$V_{DD} < 2.7$ V	160			

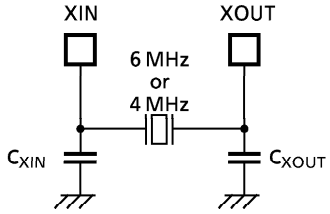
Recommended Oscillating Conditions

(V_{SS} = 0 V, V_{DD} = 2.7 to 5.5 V, Topr = – 30 to 70°C)

(1) 6 MHz

Ceramic Resonator

CSA6.00MGU (MURATA)	$C_{XIN} = C_{XOUT}$ = 30 pF
KBR-6.00MS (KYOCERA)	$C_{XIN} = C_{XOUT}$ = 30 pF
EFOEC6004A4 (NATIONAL)	$C_{XIN} = C_{XOUT}$ = 30 pF



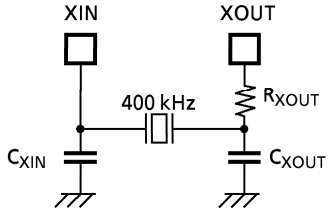
(2) 4 MHz

Ceramic Resonator

CSA4.00MG (MURATA)	$C_{XIN} = C_{XOUT}$ = 30 pF
KBR-4.00MS (KYOCERA)	$C_{XIN} = C_{XOUT}$ = 30 pF
EFOEC4004A4 (NATIONAL)	$C_{XIN} = C_{XOUT}$ = 30 pF

Crystal Oscillator

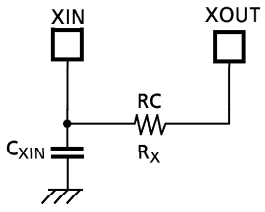
204B-6F 4.0000 (TOYOCOM)	$C_{XIN} = C_{XOUT}$ = 20 pF



(3) 400 kHz

Ceramic Resonator

CSB400B (MURATA)	$C_{XIN} = C_{XOUT}$ = 220 pF, R_{XOUT} = 6.8 kΩ
KBR-400B (KYOCERA)	$C_{XIN} = C_{XOUT}$ = 100 pF, R_{XOUT} = 10 kΩ
EFOA400K04B (NATIONAL)	$C_{XIN} = C_{XOUT}$ = 470 pF, R_{XOUT} = 0 Ω



(4) RC Oscillation (V_{SS} = 0V, V_{DD} = 5.0 V, Topr = 25°C)

2 MHz (Typ.)	C_{XIN} = 33 pF, R_X = 10 kΩ
400 kHz (Typ.)	C_{XIN} = 100 pF, R_X = 30 kΩ

Typical Characteristics