CMOS 4-BIT MICROCONTROLLER

TMP47C453AN
TMP47C453AF

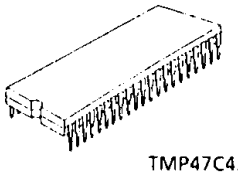
The 47C453A is a high performance 4-bit single chip microcomputer based on the TLCS-47 CMOS series. And the 47C453A has a built-in large capacity RAM for repertory dial and DTMF generator, which is suitable for application in telephones. The 47C453A is also capable of operation with low voltage such as those supplied by telephone line.

PART No.	ROM	RAM	PACKAGE	PIGGYBACK
TMP47C453AN	4096 x 8-bit	768 x 4-bit	SDIP42	TMP47C953AE
TMP47C453AF			QFP44	TMP47C953AG

FEATURES

- ◆4-bit single chip microcomputer
- ◆Instruction execution time : 8.3μs (at 960KHz)
- ◆Low voltage operation : 2.2V min.
- ◆90 basic instructions
- ◆Table look-up instructions
- ◆Subroutine nesting : 15 levels max.
- ◆6 interrupt sources (External : 2, Internal : 4)
  All sources have independent latches each, and multiple interrupt control is available
- ◆I/O port (35 pins)
  - Input 2ports 5pins
  - I/O 7ports 27pins
  - Output 1port 3pins
- ◆Interval Timer
- ◆Two 12-bit Timer/Counters
  Timer, event counter, and pulse width measurement mode
- ◆Serial Interface with 4-bit buffer
  External/internal clock, leading/trailing edge shift mode
- ◆DTMF (Dual Tone Multi Frequency) output
  - DTMF output with one instruction
  - Single tone output function
- ◆RAM for repertory dial : 768 x 4-bit max.
- ◆BEEP output function
- ◆Warm-Start function
- ◆Hold function
  - Battery/Capacitor back-up
  - Hold function controlled by port K0
- ◆Real Time Emulator : BM47C453A

SDIP42

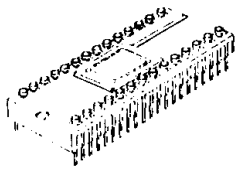


TMP47C453AN

QFP44

TMP47C453AF

SDIC42



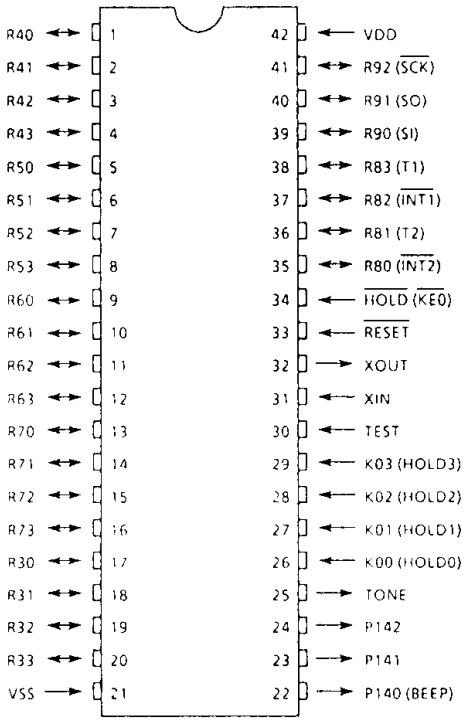
TMP47C953AE

QFC44

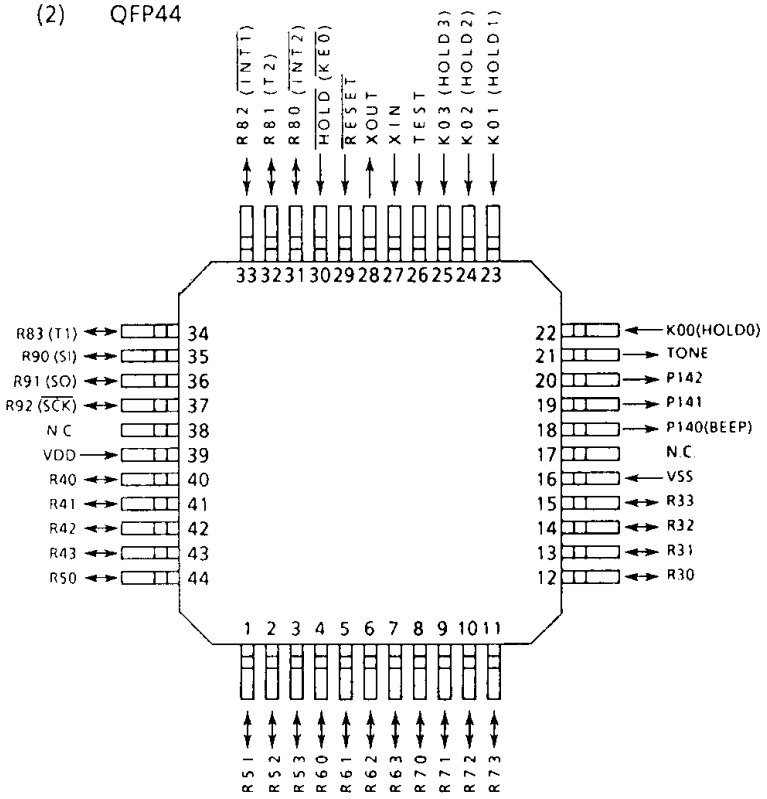
TMP47C953AG

PIN ASSIGNMENTS (TOP VIEW)

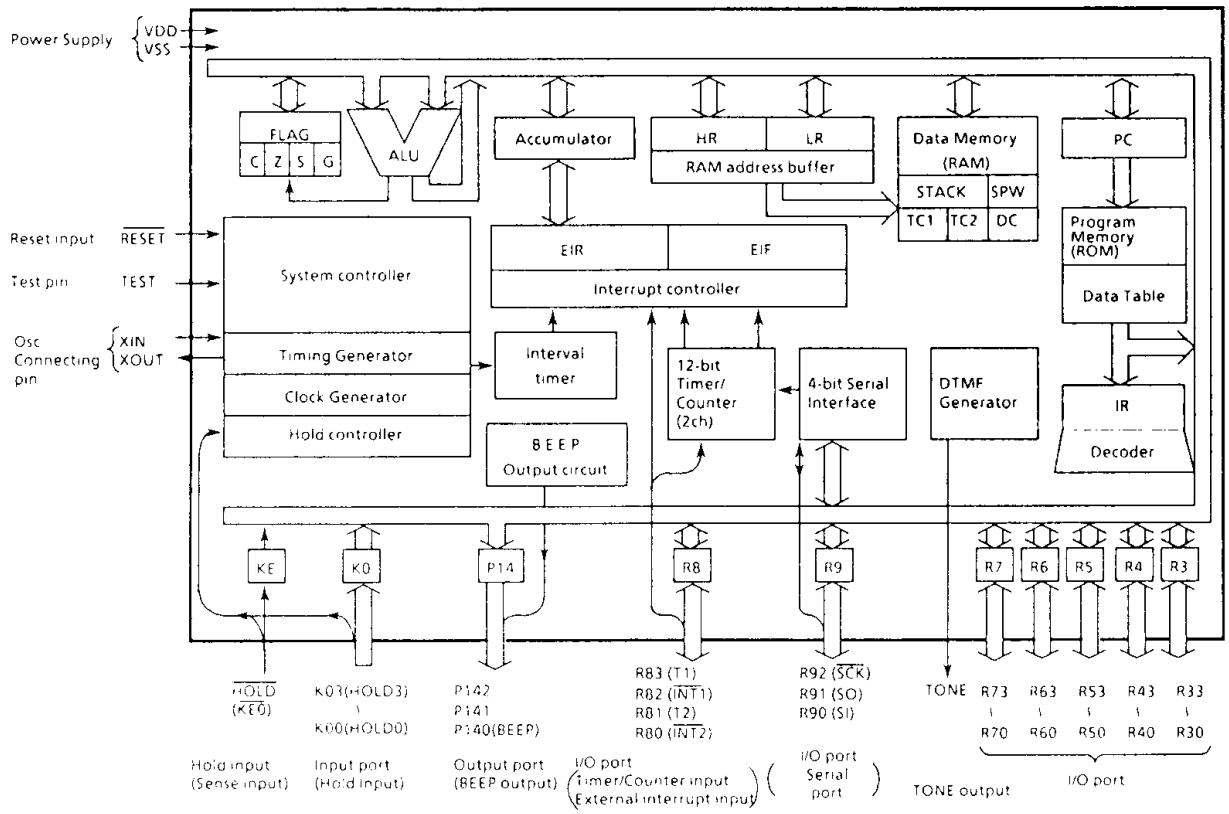
(1) SDIP42



(2) QFP44



BLOCK DIAGRAM



PIN FUNCTION

PIN NAME	Input/Output	FUNCTIONS	
K03 (HOLD3) - K00 (HOLD0)	Input (Input)	4-bit input port	Hold request/release signal input (Active "H")
R33 - R30	I/O	4-bit I/O port with latch. When used as input port, the latch must be set to "1".	
R43 - R40			
R53 - R50			
R63 - R60			
R73 - R70			
R83 (T1)	I/O (Input)	4-bit I/O port with latch. When used as input port, external interrupt input pin, or timer/counter external input pin, the latch must be set to "1".	Timer/Counter 1 external input
R82 ($\overline{INT1}$)			External interrupt 1 input
R81 (T2)			Timer/Counter 2 external input
R80 ($\overline{INT2}$)			External interrupt 2 input
R92 ($\overline{SCK}$)	I/O (I/O)	3-bit I/O port with latch. When used as input port or serial port, the latch must be set to "1".	Serial clock I/O
R91 (SO)	I/O (Output)		Serial data output
R90 (SI)	I/O (Input)		Serial data input
P142 - P141	Output	3-bit output port with latch	
P140(BEEP)	Output (Output)		BEEP Output
TONE	Output	Tone output	
XIN	Input	Resonator connecting pins.	
XOUT	Output		
$\overline{RESET}$	Input	Reset signal input	
$\overline{HOLD}$ ($\overline{KE0}$)	Input	Hold request/release signal input	Sense input
TEST	Input	Test pin for out-going test. Be opened or fixed to low level.	
VDD	Power supply	+ 2.2V to 6.0V	
VSS		0V(GND)	

OPERATIONAL DESCRIPTION

Concerning the 47C453A, the configuration and functions of hardwares are described. As the description has been provided with priority on those parts differing from the 47C400A, the technical data sheets for the 47C400A shall also be reffered to.

1. SYSTEM CONFIGURATION

(1) Data Memory
(2) I/O port
(3) DTMF Generator
(4) BEEP Output Circuit
(5) Hold Operating Mode Controller

2. INTERNAL CPU FUNCTION

2.1 Data Memory

The 47C453A data memory consists of a 768 x 4-bit RAM. First 256 x 4-bit RAM is the same as the data memory built into the 47C400A, so refer to the technical data sheets for the 47C400A for an explanation of the operation. Extended 512 x 4-bit RAM is mainly used for storing repertory dialing data and is controlled by the RAM address register, RAM data buffer register and TONE/RAM command register.

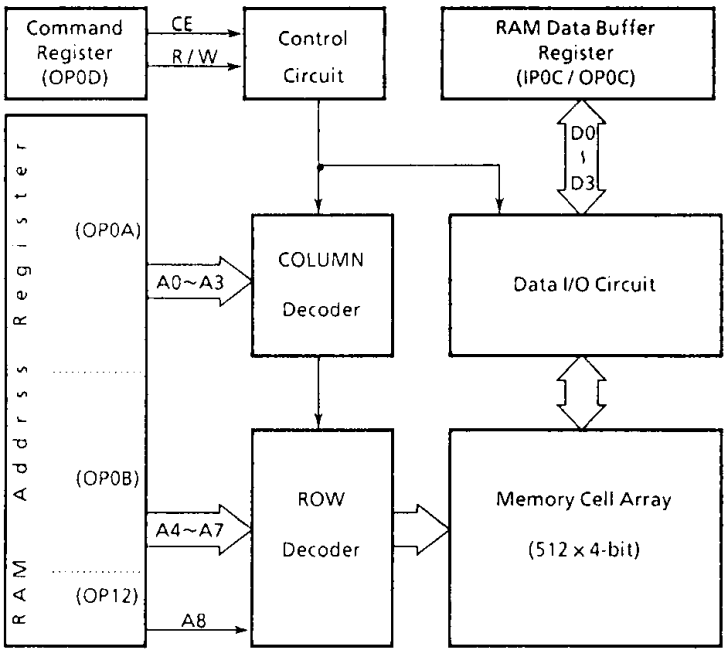


Figure 2-1. Block Diagram

(1) RAM (512 x 4-bit) Address Register

The RAM address register is a 9-bit register to specify addresses for the RAM data memory. The upper 1 bit is accessed with port address OP12, the next 4 bits are accessed with the port address OP0B/IP0B and the lower 4 bits are accessed with port address OP0A/IP0A.

These registers are initialized to "0" during reset.

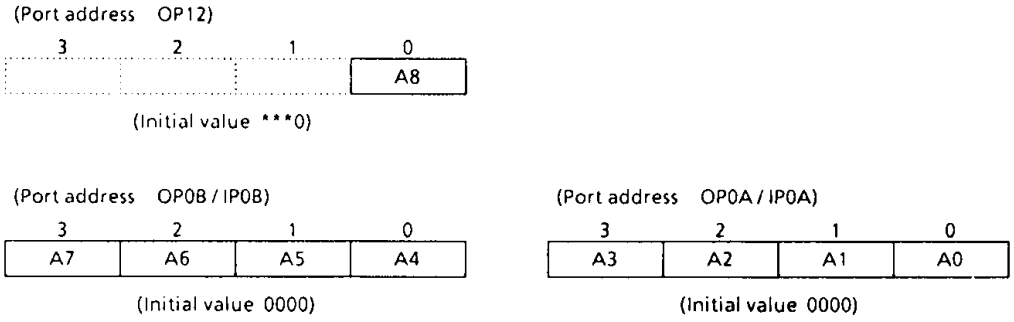


Figure 2-2. RAM Address Register

(2) RAM (512 x 4-bit) Data Buffer Register

The RAM data buffer register is a 4-bit buffer register to read or write RAM data. When writing data to RAM, it is accessed as port address OP0C. Port address IP0C is used for access when reading data from RAM.

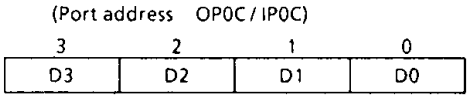


Figure 2-3. RAM Data Buffer Register

(3) RAM (512 x 4-bit) Command Register

The RAM command register (OP0D/IP0D) controls the reading or writing data, and whether RAM. is to be accessed or put in stand-by mode. This register is accessed as the port address OP0D/IP0D. The RAM command register is also used as the TONE command register.

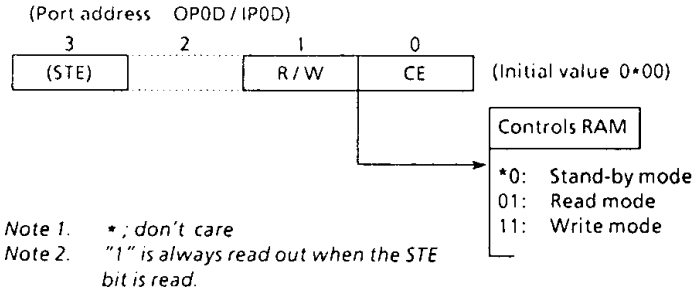


Figure 2-4. RAM Command Register

2.1.1 Access for RAM (512 × 4-bit)

To write data to RAM, load the address into the RAM address register and the data into the RAM data buffer register (OP0C) , then put the RAM command register in the write mode. The data will be written to the specified RAM address by this operation.

The data are latched in the RAM data buffer register, therefore, RAM data buffer register operation is not necessary when the same data are written continuously.

To read data from RAM, set the RAM command register to the read mode and load the address into the RAM address register, then read the data via RAM data buffer register (IP0C) . Data are not latched in the RAM data buffer register.

Example 1 : To write data "9" to address 182_H and data "7" to address $15A_H$ in RAM.

```
        LD      A,#1            ; Sets data "182H" to RAM address register.
        OUT     A,%OP12
        OUT     #8,%OP0B
        OUT     #2,%OP0A
        OUT     #9,%OP0C        ; Writes data "9" to RAM data buffer register.
        OUT     #0011B,%OP0D    ; Sets RAM to write mode.
        OUT     #0010B,%OP0D    ; Sets RAM to stand-by mode.
        OUT     #5,%OP0B        ; Sets data "15AH" to RAM address register.
        OUT     #0AH,%OP0A
        OUT     #7,%OP0C        ; Writes data "7" to RAM data buffer register.
        OUT     #0011B,%OP0D    ; Sets RAM to write mode.
        OUT     #0010B,%OP0D    ; Sets RAM to stand-by mode.
```

Example 2 : To write data "0" to address 120_H through 127_H in RAM.

```
        OUT     #0,%OP0C        ; Writes data "0" to RAM data buffer register.
        LD      A,#0            ; Sets data "120H" to RAM address register.
        OUT     #1,%OP12
        OUT     #2,%OP0B
        OUT     A,%OP0A
        OUT     #0011B,%OP0D    ; Sets RAM to write mode.
SLOOP : CMPR    A,#7            ; Increases address register.
        TESTP   ZF
        B       SWEND
        INC     A
        OUT     A,%OP0A
        BR      SLOOP
SWEND : OUT     #0010B,%OP0D    ; Sets RAM to stand-by mode.
```

Example 3 : To read data from address $0B1_H$ in RAM and store to Accumulator.

```
        OUT     #0001B,%OP0D    ; Sets RAM to read mode.
        LD      A,#0            ; Sets data "0B1H"to RAM address register
        OUT     A,%OP12
        OUT     #0BH,%OP0B
        OUT     #1,%OP0A
        IN      %IP0C,A         ; Reads data from RAM and stores to
                                  Accumulator.
```

3. PERIPHERAL HARDWARE FUNCTION

3.1 I/O Ports

The 47C453A has 10 ports (35 pins) each as follows :

①	K0	;	4-bit input (shared by hold request/release signal input)
②	R3	;	4-bit input/output
③	R4, R5, R6, R7	;	4-bit input/output
④	R8	;	4-bit input/output (shared by external interrupt input and timer/counter input)
⑤	R9	;	3-bit input/output (shared by serial port)
⑥	P14	;	3-bit output (P140 is shared by BEEP output)
⑦	KE	;	1-bit sense input (shared by hold request/release signal input)

The port K0, K3 and P14 of the 47C453A differ from those of the 47C400A. The 47C453A does not have the port P1 and P2.

Table 3-1 lists the port address assignments and the I/O instructions that can access the ports.

(1) Port K0 (K03-K00)

The 4-bit input port with pull-up resistors, shared by hold request/release signal input.

Port K0 (Port address IP00)

3	2	1	0
K03 (HOLD3)	K02 (HOLD2)	K01 (HOLD1)	K00 (HOLD0)

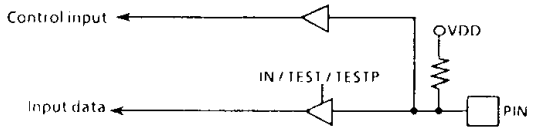


Figure 3-1. Port K0

(2) Port R3 (R33-R30)

The 4-bit I/O port with latch. When used as an input port, the latch must be set to "1". The latch is initialized to "1" during reset.

Port R3 (Port address OP03 / IP03)

3	2	1	0
R33	R32	R31	R30

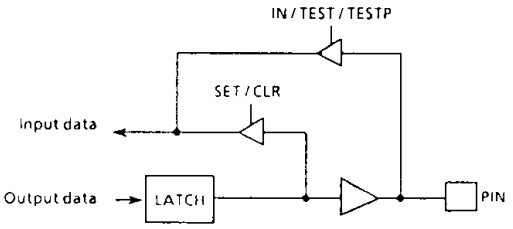


Figure 3-2. Port R3

(3) Port P14 (P142-P140)

The 3-bit output port with latch. The latch is initialized to "1" during reset. The pin P140 is shared by the BEEP output. When used as the BEEP output, the latch must be set to "1".

Port P14 (Port address OP14)

3	2	1	0
	P142	P141	P140 (BEEP)

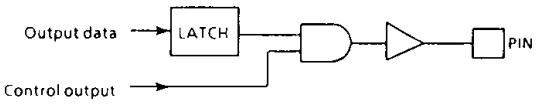


Figure 3-3. Port P14

Port address (**)	Port		Input/Output instruction						
	Input (IP**)	Output (OP**)	IN %p, A IN %p, @HL	OUT A, %p OUT@HL,%p	OUT #k, %p	OUTB @HL	SET %p, b CLR %p, b	TEST %p, b TESTP %p, b	SET @L CLR @L TEST @L
00_H	K0 Input port	——	○	-	-	-	-	○	-
01	ROW register	ROW register	○	○	○	○ (Note2)	○	○	-
02	COLUMN register	COLUMN register	○	○	○	○	○	○	-
03	R3 Input port	R3 Output port	○	○	○	-	○	○	-
04	R4 Input port	R4 Output port	○	○	○	-	○	○	○
05	R5 Input port	R5 Output port	○	○	○	-	○	○	○
06	R6 Input port	R6 Output port	○	○	○	-	○	○	○
07	R7 Input port	R7 Output port	○	○	○	-	○	○	○
08	R8 Input port	R8 Output port	○	○	○	-	○	○	-
09	R9 Input port	R9 Output port	○	○	○	-	○	○	-
0A	RAM address register	RAM address register	○	○	○	-	○	○	-
0B	RAM address register	RAM address register	○	○	○	-	○	○	-
0C	RAM data buffer register	RAM data buffer register	○	○	○	-	○	○	-
0D	RAM command register	RAM command register	○	○	○	-	-	○	-
0E	SIO, Hold status	——	○	-	-	-	-	○	-
0F	Serial receive buffer	Serial transfer buffer	○	-	○	-	-	-	-
10_H	Undefined	Hold operating mode control	-	○	-	-	-	-	-
11	Undefined	——	-	-	-	-	-	-	-
12	Undefined	RAM address register	-	○	-	-	-	-	-
13	Undefined	BEEP output control	-	○	-	-	-	-	-
14	Undefined	P14 Output port	-	○	-	-	-	-	-
15	Undefined	——	-	-	-	-	-	-	-
16	Undefined	——	-	-	-	-	-	-	-
17	Undefined	——	-	-	-	-	-	-	-
18	Undefined	——	-	-	-	-	-	-	-
19	Undefined	Interval Timer interrupt control	-	○	-	-	-	-	-
1A	Undefined	——	-	-	-	-	-	-	-
1B	Undefined	——	-	-	-	-	-	-	-
1C	Undefined	Timer/Counter 1 control	-	○	-	-	-	-	-
1D	Undefined	Timer/Counter 2 control	-	○	-	-	-	-	-
1E	Undefined	——	-	-	-	-	-	-	-
1F	Undefined	Serial interface control	-	○	-	-	-	-	-

Note 1. "——" means the reserved state. Unavailable for the user program.

Note 2. The 5-bit to 8-bit data conversion instruction [OUT @ HL], automatic access to ROW register and COLUMN register.

Table 3-1. Port Address Assignments and Available I/O Instructions

3.2 DTMF Generator

The 47C453A has a built-in DTMF generator which generates dialing signals for tone dialing type telephones. There are two groups of tone dial signals, one group of 4 sine wave low frequencies and another group of 4 sine wave high frequencies. All of these frequencies can be selected individually and combined with a frequency from the other group for a total of 16 different DTMF composite waves.

(DTMF ; Dual Tone Multi Frequency)

3.2.1 Configuration of DTMF Generator

Figure 3-4 shows configuration of the DTMF generator. The 47C453A generates two stepped, quasi sine waves for tone dial signals which can be combined and output. The high or low group of frequencies is selected by setting frequency selection codes into the ROW and COLUMN registers.

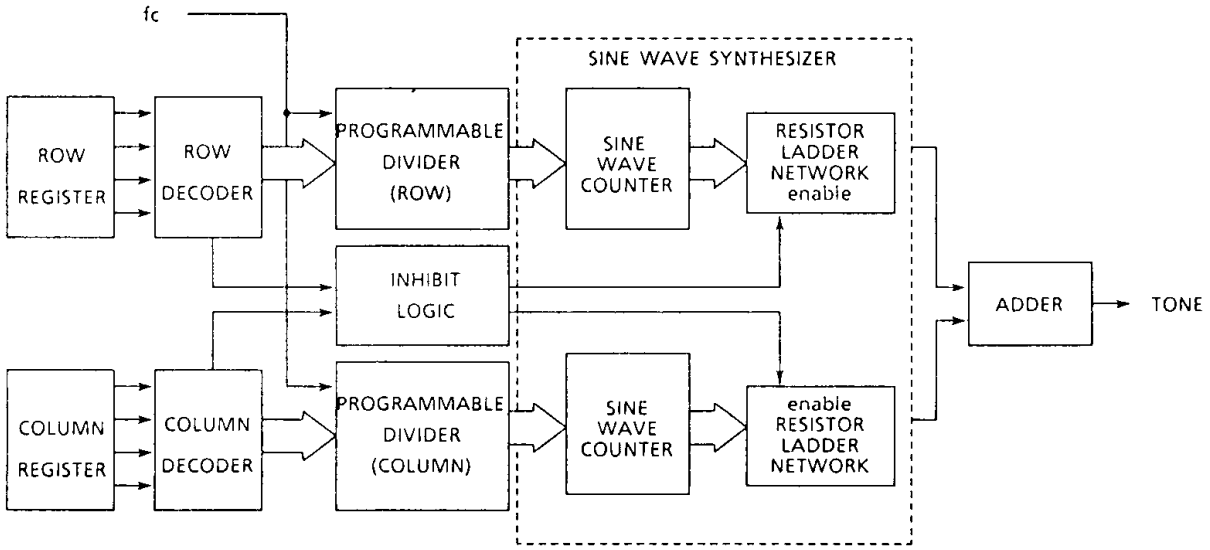


Figure 3-4. Configuration of DTMF Generator

3.2.2 Control of DTMF Generator

Tone output is controlled by ROW register (OP01/IP01) and COLUMN register (OP02/IP02). And single tone is controlled by TONE command register (OP0D/IP0D). ROW register and COLUMN register are initialized to "0" during reset.

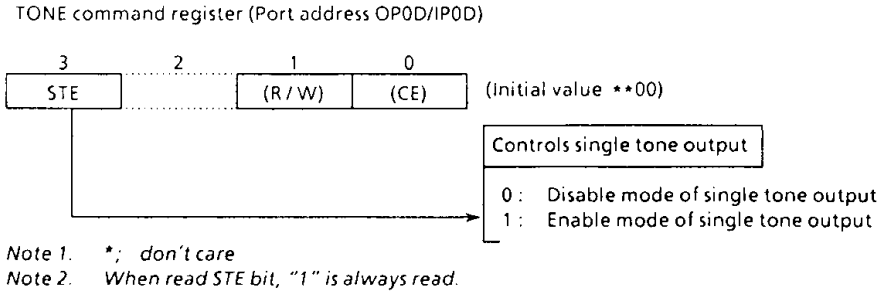


Figure 3-5. TONE command register

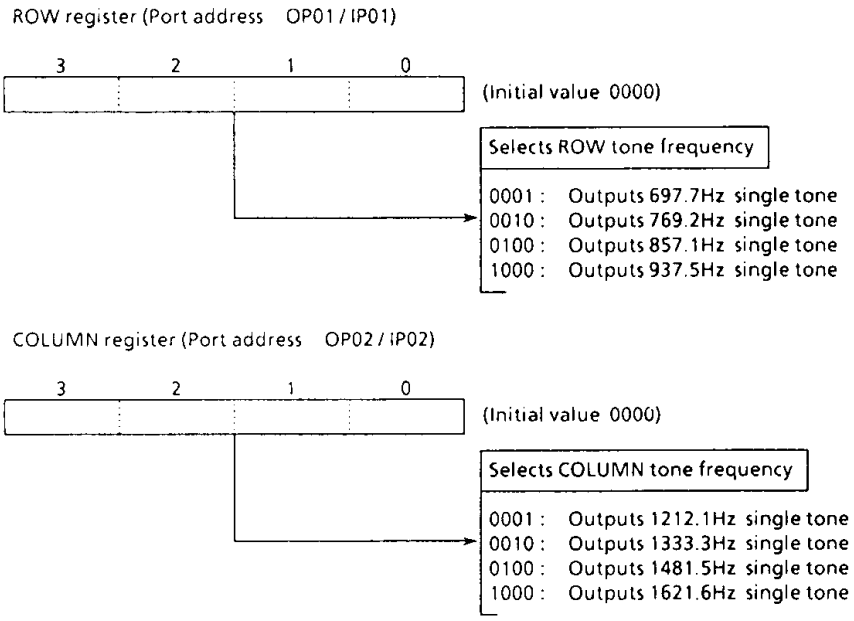


Figure 3-6. ROW, COLUMN Register

Tones are outputted by loading the frequency selection codes shown in Figure 3-6 into the ROW and COLUMN registers. In the enable mode of single tone output and either ROW or COLUMN register is disabled, another register remains to be enabled, and so single tone can be outputted, by loading an ineffective code into the register. When both the registers are enabled, dual tone can be outputted. In the disable mode of single tone output, effective codes are loaded into both ROW and COLUMN registers and then dual tone can be outputted. At this time, an ineffective code is loaded into ROW or COLUMN register and then the 47C453A has no tone output signal.
The [OUTB @HL] instruction can set 8-bit data into both registers (the upper 4 bits of the ROM data go to the COLUMN register and the lower 4 bits go to the ROW register) at the same time, and DTMF signal is outputted without single tone output.

Example 1 : To output 1481.5Hz single tone

```
OUT     #8,%OP0D ;  Sets the enable mode of single tone output.
OUT     #0,%OP01 ;  Sets an ineffective code into ROW register.
OUT     #4,%OP02 ;  Sets data "4" into COLUMN register
```

Example 2 : 8 bits data corresponding to the 5 bits of data linking the content of carry flag and the contents of data memory RAM address 90_H are read from the ROM, frequency selection codes are loaded into ROW and COLUMN registers, and dual tone is outputted.

```
LD      HL,#90H ;  HL←90H (Sets the address of the data memory)
OUTB    @HL     ;  Sets the ROM data into the ROW and COLUMN register.
```

Table 3-2 shows the corresponding frequency selection codes of the ROW and COLUMN registers for the telephone dial keys. Table 3-3 shows the deviation between the 47C453A tone output frequency and standard frequency.

		COLUMN register (OP02 / IP02)		
	Frequency selection code	0001 (1209)	0010 (1336)	0100 (1477)
ROW register (OP01/IP01)	0001 (697)	1	2	3
	0010 (770)	4	5	6
	0100 (852)	7	8	9
	1000 (941)	*	0	#
		Standard telephone dial key		

Contents of ( ) are standard frequencies, unit : Hz

Table 3-2. Corresponding frequency selection codes of the ROW and COLUMN registers for the telephone dial keys

ROW Tone						
Frequency selection code				Tone output frequency [Hz]	Standard frequency [Hz]	Deviation [%]
3	2	1	0			
0	0	0	1	697.7	697	+ 0.10
0	0	1	0	769.2	770	- 0.10
0	1	0	0	857.1	852	+ 0.60
1	0	0	0	937.5	941	- 0.37

COLUMN Tone						
Frequency selection code				Tone output frequency [Hz]	Standard frequency [Hz]	Deviation [%]
3	2	1	0			
0	0	0	1	1212.1	1209	+ 0.26
0	0	1	0	1333.3	1336	- 0.20
0	1	0	0	1481.5	1477	+ 0.30
1	0	0	0	1621.6	1633	- 0.70

Table 3-3. Tone output frequencies and Deviation from standard

3.2.3 Test mode for tone output

The 47C453A includes a test mode for checking tone output waveforms. Tones can be outputted by the curcuit shown in Figure 3-7. ROW data are inputted from the R6 port and COLUMN data are inputted from the R3 port, and any desired single or dual tones can be outputted by setting the frequency selection codes shown in Figure 3-6. Figure 3-8 shows a single tone waveform and Figure 3-9 shows a dual tone waveform.

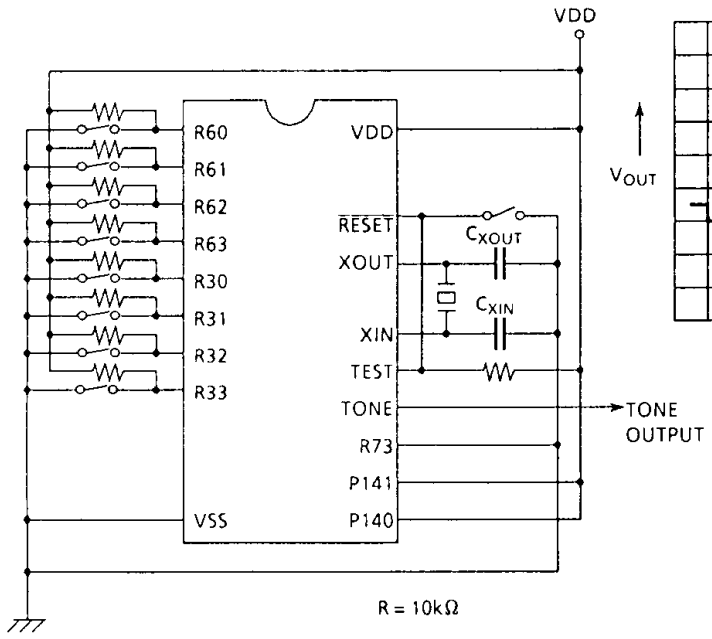


Figure 3-7. Tone test circuit

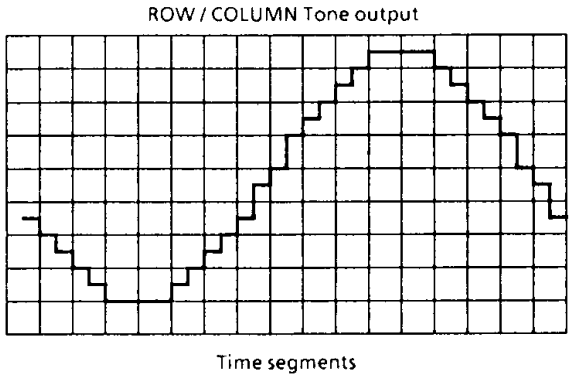


Figure 3-8. Single tone waveform

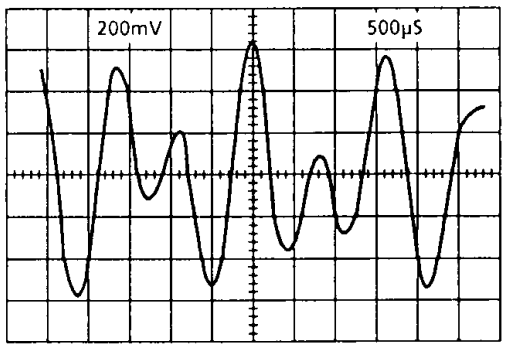


Figure 3-9. Dual tone waveform

3.3 BEEP Output Circuit

BEEP output circuit generates square wave in the audible frequency range. This circuit can drive the key input confirmation tone generator circuit for telephone applications.

BEEP output is from the P140 (BEEP) pin. This pin is for both P140 output and BEEP output. Set the P140 output latch to "1" for BEEP output.

3.3.1 Configuration of BEEP Output Circuit

Figure 3-10 shows configuration of the BEEP output circuit. The clock pulse of BEEP output circuit is supplied by an interval timer. BEEP output is controlled by frequency selection and output enable/disable setting.

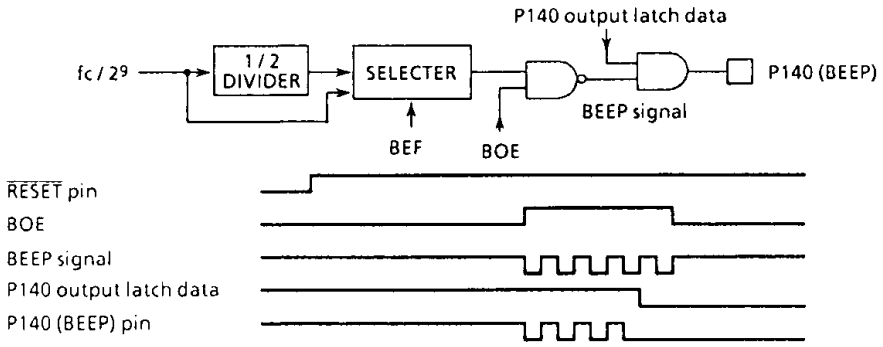


Figure 3-10. BEEP Output Circuit Configuration and Timing Chart

3.3.2 Control of BEEP Output

BEEP output is controlled with the BEEP output control command register (OP13).

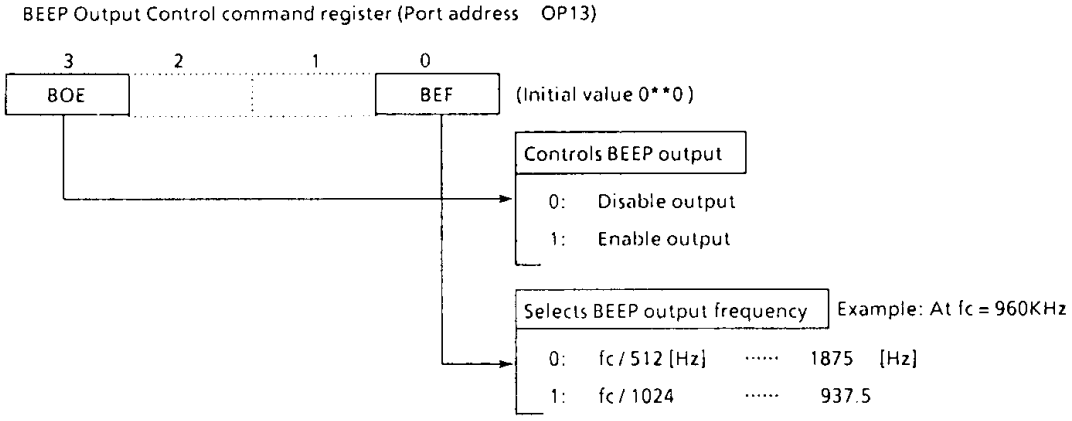
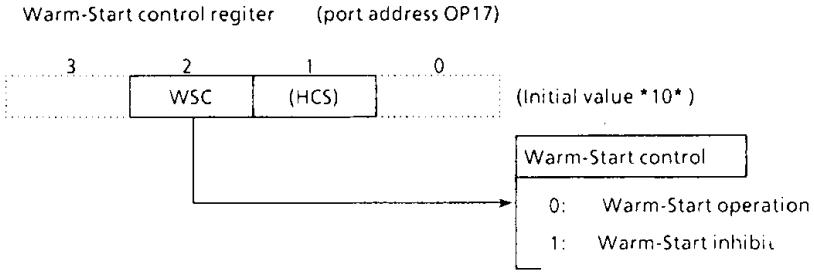


Figure 3-11. BEEP Output Control Command Register

3.4 Warm-Start Function

The 47C453A has Warm-start function which is performed reset-operation by setting a command register (OP17).



3.4 Interval Timer Interrupt (ITMR)

The interval timer can be used to generate an interrupt with a fixed frequency. For an interval timer interrupt, one of 4 frequencies can be selected by command. The command register (OP19) is initialized to "0" during reset. An interval timer interrupt is generated at the first rising edge of the binary counters output after the command has been set. The interval timer is not cleared by command, so that the first interrupt may occur earlier than the preset interrupt period.

Example: To set the interval timer interrupt frequency to $fc/2^{11}$ [Hz].

```
LD      A,  #0110B    ;  OP19←0110B
OUT     A,  %OP19
```

Interval Timer interrupt command register (Port address OP19)

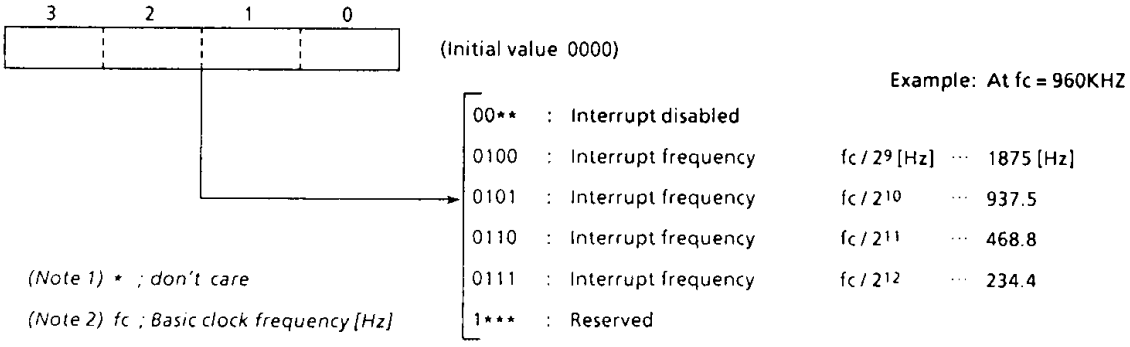


Figure 3-12. Interval Timer Interrupt Command Register

3.5 Timer/Counter

The following operating frequencies differ from those of the 47C400A.

(1) Internal pulse rate

The intrnal pulse rates shown in Table 3-4 can be selected by setting the values of the lower 2 bits of the TC1 and TC2 control command registers (OP1C, OP1D).

The values of lower 2 bits (bit1, 0)	Internal pulse rate	Max. setting time	At fc = 960KHz	
			Internal pulse rate	Max. setting time
00	$fc / 2^9$ [Hz]	$2^{21} / fc$ [sec]	1875 [Hz]	2.2 [sec]
01	$fc / 2^{13}$	$2^{25} / fc$	117.2	35
10	$fc / 2^{17}$	$2^{29} / fc$	7.3	559.2
11	$fc / 2^{21}$	$2^{33} / fc$	0.46	8947.8

Table 3-4. Internal Pulse Rate

4. POWER SAVING FUNCTION

The 47C453A provides the HOLD operating mode to implement the low-power-consumpting operations.

4.1 HOLD Operating Mode

The HOLD feature stops the system and holds the system's internal states active before stop with a low power. The HOLD operation is controlled by the $\overline{HOLD}$ pin and K0 port inputs. The $\overline{HOLD}$ pin and K0 port input state can be known by the status registers (IP0E). The $\overline{HOLD}$ pin is shared with the $\overline{KE0}$ pin.

4.1.1 HOLD Operation control circuit

Configuration of HOLD operation circuit is shown in Figure 4-1.

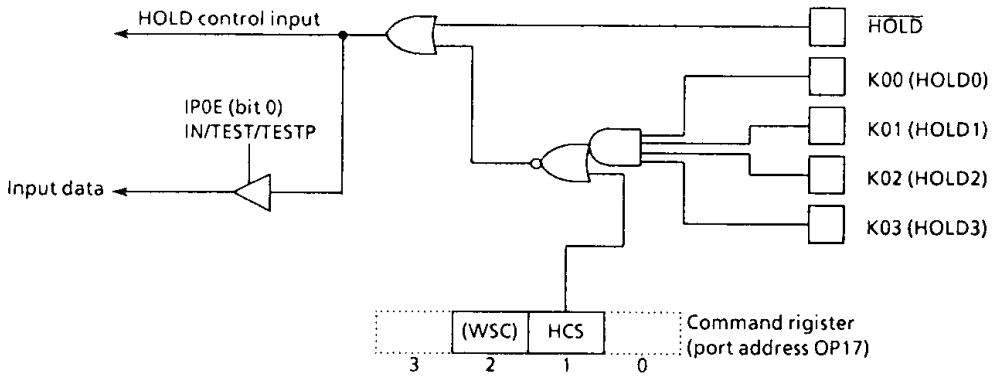


Figure 4-1. Hold control circuit

The 47C453A has a $\overline{HOLD}$ pin and K0 port as HOLD control input. Therefore, in the case of using K0 port for key inputs, the HOLD operation can be released by key inputs. HOLD control by K0 port input can be inhibited by HOLD control input select command register. (bit 1 of OP17)

HOLD control input select command register (port address OP17)

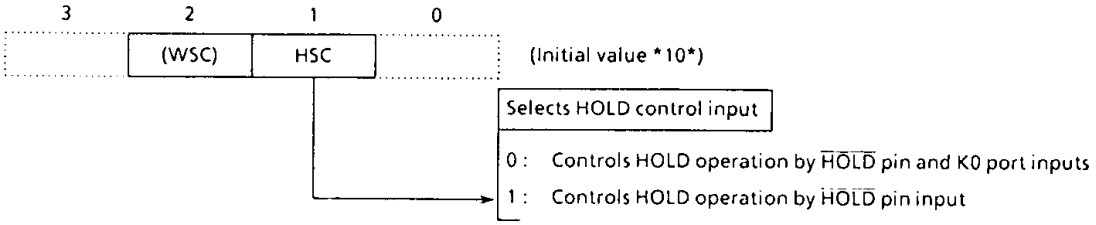


Figure 4-2. Hold control input select command register

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

PARAMETER	SYMBOL	PINS	RATINGS	UNIIT
Supply Voltage	V_{DD}		− 0.3 to 7	V
Input Voltage	V_{IN}		− 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	Except sink open drain pin	− 0.3 to V_{DD} + 0.3	V
	VOUT2	Sink open drain pin	− 0.3 to 10	
Output Current (per 1 pin)	I_{OUT}		3.2	mA
Power Dissipation [T_{opr} = 60°C]	PD		600	mW
Soldering Temperature (time)	T_{sld}		260 (10sec)	°C
Storage Temperature	T_{stg}		− 55 to 125	°C
Operating Temperature	T_{opr}		− 30 to 60	°C

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, T_{opr} = − 30 to 60°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}		In the Normal mode	2.2	6.0	V
			In the HOLD mode	2.0		
Input High Voltage	V_{IH1}	Except hysteresis input	$V_{DD} \geq 4.5V$	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5V$	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Except hysteresis input	$V_{DD} \geq 4.5V$	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5V$		$V_{DD} \times 0.1$	
Clock Frequency	fc			960		KHz

Note. Input voltage V_{IH3}, V_{IL3} : in the HOLD mode.

D.C. CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 2.2 to 6.0V, T_{opr} = − 30 to 60°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		−	0.7	−	V
Input Current	I_{IN1}	Port K0, TEST, $\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5V, V_{IN} = 5.5V / 0V	−	−	± 2	μA
	I_{IN2}	Port R (open drain)					
Input Low Current	I_{IL}	Port R (push-pull)	V_{DD} = 5.5V, V_{IN} = 0.4V	−	−	− 2	mA
Input Resistance	R_{IN1}	Port K0		30	70	150	KΩ
	R_{IN2}	$\overline{RESET}$		100	220	450	
Output Leakage Current	I_{LO}	Ports P, R (open drain)	V_{DD} = 5.5V, V_{OUT} = 5.5V	−	−	2	μA
Output High Voltage	V_{OH}	Port R (push-pull)	V_{DD} = 4.5V, I_{OH} = − 200μA	2.4	−	−	V
Output Low Voltage	V_{OL2}	Except XOUT	V_{DD} = 4.5V, I_{OL} = 1.6mA	−	−	0.4	V
Supply Current (in the Normal mode)	I_{DD}		Except TONE generating V_{DD} = 2.2V fc = 480KHz	−	0.3	0.5	mA
	I_{DDT}		TONE generating V_{DD} = 2.2 V fc = 480KHz	−	0.6	1.2	
Supply Current (in the HOLD mode)	I_{DDT}		V_{DD} = 5.5V	−	0.5	10	μA
			V_{DD} = 2.2V, Topr = 25°C	−	−	0.5	

Note 1. Typ. values show those at T_{opr} = 25°C, V_{DD} = 5V.

Note 2. Input Current I_{IN1} : The current through resistor is not included, when the pull-up/pull-down resistor is contained.

Note 3. Supply Current : V_{IN} = 2.0V / 0.2V

The K0 port is opened when the pull-up/pull-down resistor is contained.

The Voltage applied to the R port is within the valid range V_{IL} or V_{IH}.

TONE OUTPUT CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 2.2 to 6.0V, T_{opr} = − 30 to 60°C)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Tone Output Voltage (ROW)	V_{TONE}	RL ≧ 10KΩ, V_{DD} = 2.2V	125	185	250	mVrms
Pre-Emphasis High Band (COL / ROW)	PEHB	PEHB = 20log (COL/ROW)	1	2	3	dB
Output Distortion	DIS		−	−	10	%
Frequency Stability	△f	Except error of osc. frequency	−	−	0.7	%

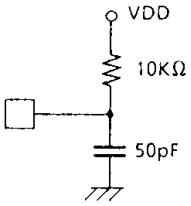
A.C. CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 2.2 to 6.0V, T_{opr} = – 30 to 60°C)

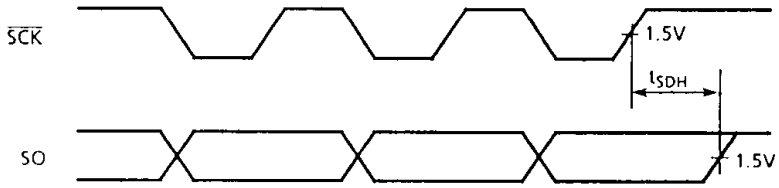
PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}		16.7			μs
Shift Data Hold Time	t_{SDH}		$0.5t_{cy}$-300	–	–	ns

Note. Shift Data Hold Time :

External circuit for $\overline{SCK}$ pin and SO pin



Serial port (completion of transmisson)

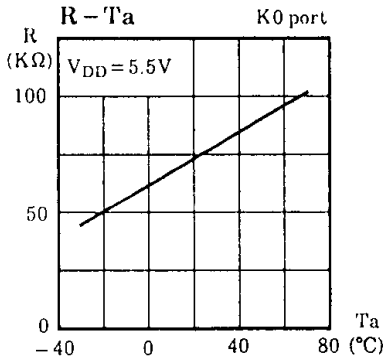


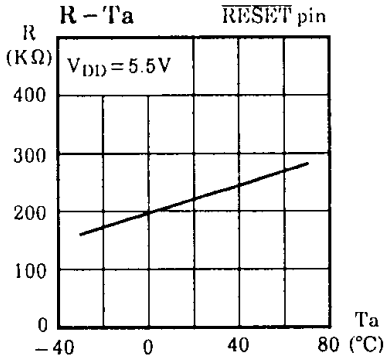
RECOMMENDED OSCILLATING CONDITION

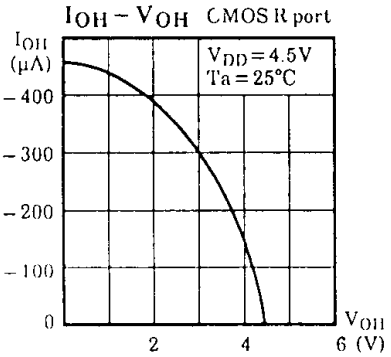
(V_{SS} = 0V, V_{DD} = 2.2 to 6.0V, T_{opr} = – 30 to 60°C)

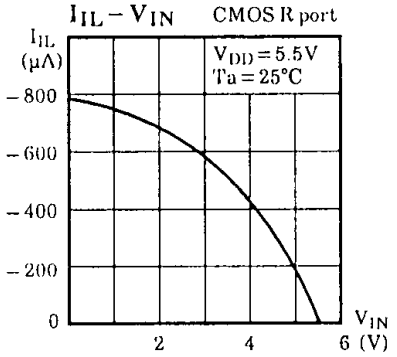
960KHz

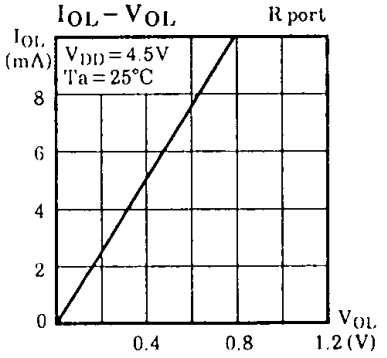
TYPICAL CHARACTERISTICS

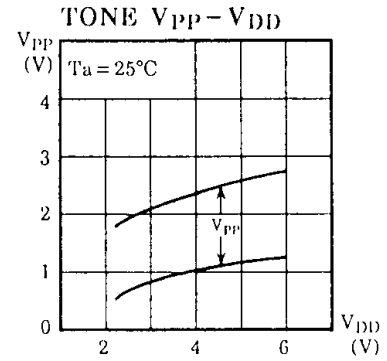


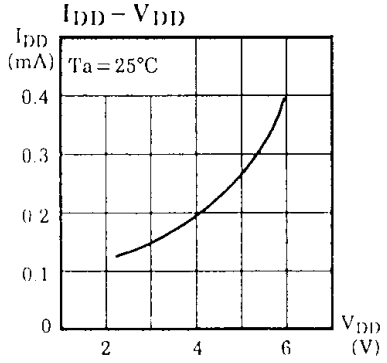


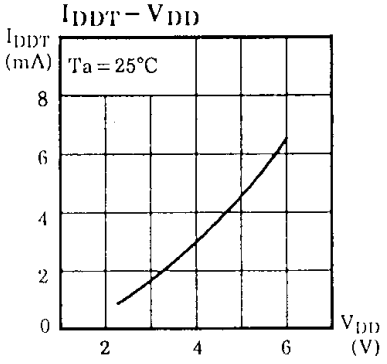












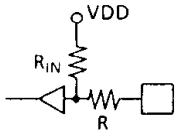
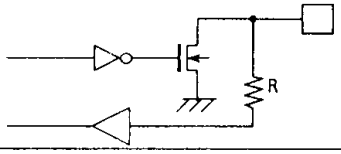
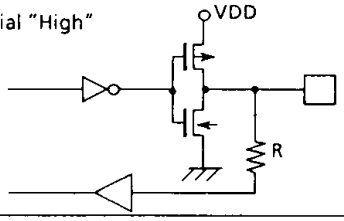
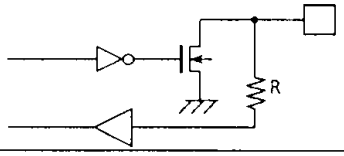
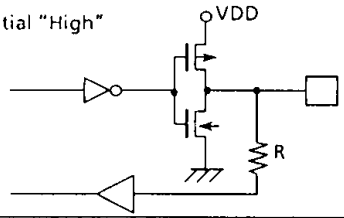
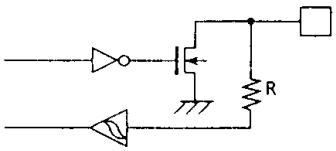
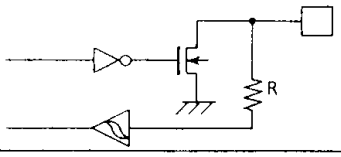
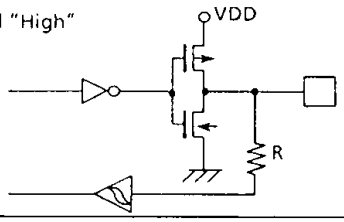
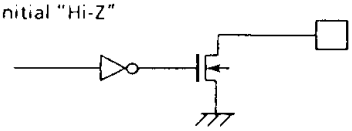
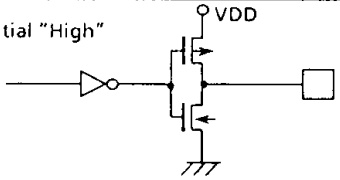
INPUT/OUTPUT Circuitry

(1) Control pins

Input/Output circuitries of the 47C453A control pins are similar to that of the 47C400A.

(2) I/O Ports

The input/output circuitries of the 47C453A I/O ports are shown as below, any one of the circuitries can be chosen by a code (WB, WE, WH) as a mask option.

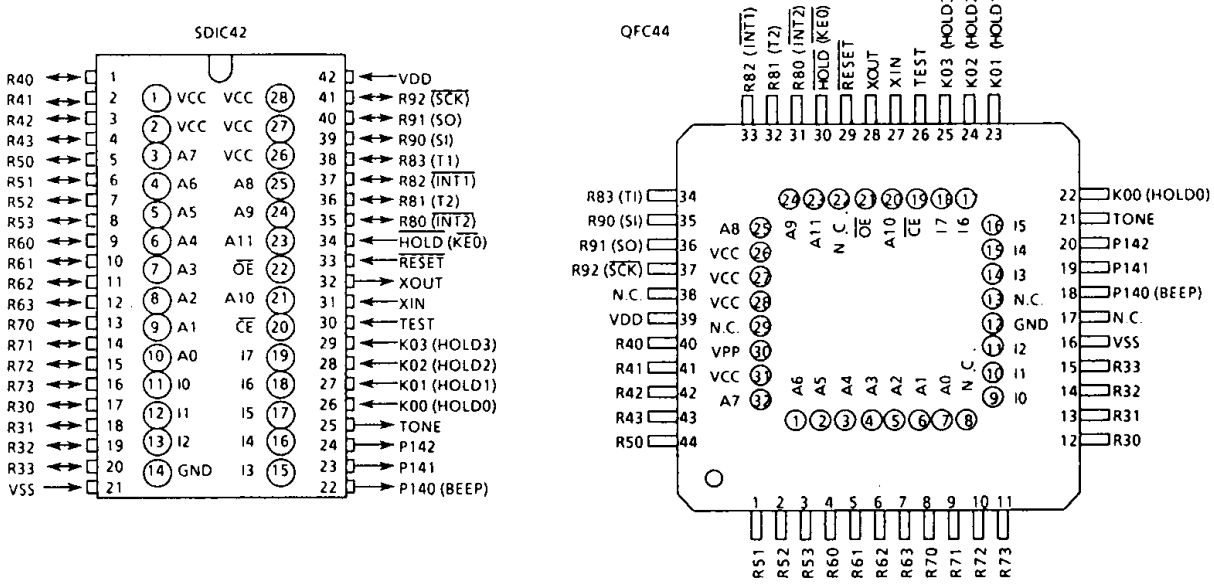
PORT	I/O	INPUT/OUTPUT CIRCUITRY (CODE)	REMARKS
K0	Input		Pull-up resistor R_{IN} = 70KΩ (typ.) R = 1KΩ (typ.)
R3 R4 R5 R6	I/O	WB: Initial "Hi-Z"  WE, WH: Initial "High" 	Sink open drain or push-pull output R = 1KΩ (typ.)
R7	I/O	WB, WE: Initial "Hi-Z"  WH: Initial "High" 	Sink open drain or push-pull output R = 1KΩ (typ.)
R8	I/O		Sink open drain Initial "Hi-Z" Hysteresis input R = 1KΩ (typ.)
R9	I/O	WB, WE: Initial "Hi-Z"  WH: Initial "High" 	Sink open drain or push-pull output Hysteresis input R = 1KΩ (typ.)
P14	Output	WB: Initial "Hi-Z"  WE, WH: Initial "High" 	Sink open drain or push-pull output

CMOS 4-BIT MICROCONTROLLER

TMP47C953AE
TMP47C953AG

The 47C953A, which is equipped with an EPROM as program memory, is a piggyback type evaluator chip used for development and operational confirmation of the 47C453A application systems (programs).
The 47C953A is pin compatible with the 47C453A which are mask-programed ROM devices.

PIN ASSIGNMENT (TOP VIEW)



PIN FUNCTION (Top of the package)

PIN NAME	Input / Output	FUNCTIONS
A11 - A0	Output	Program memory address output
I7 - I0	Input	Program memory data input
$\overline{CE}$	Output	Chip enable signal output
$\overline{OE}$		Output enable signal output
VCC	Power supply	+ 5V (connected with VDD)
GND		0V (connected with VSS)

A.C. CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Address Delay Time	t_{AD}	V_{SS} = 0V, V_{DD} = 2.2~6.0V	—	—	150	ns
Data Setup Time	t_{IS}	C_L = 100pF	150	—	—	ns
Data Hold Time	t_{IH}	Topr = -30~60°C	50	—	—	ns

NOTES FOR USE

(1) Program memory

The program areas are as shown in Figure 1.

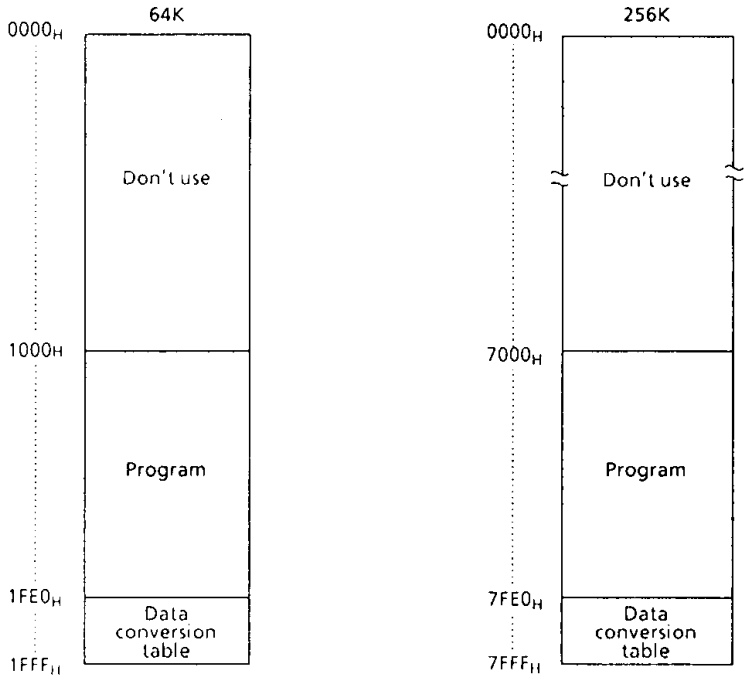


Figure 1. Program area

(2) I/O ports

Input/Output circuitries of I/O ports in the 47C953A are similar to the code WB of the 47C453A. When this chip is used as evaluator with other I/O code, it is necessary to provide the external resistors.

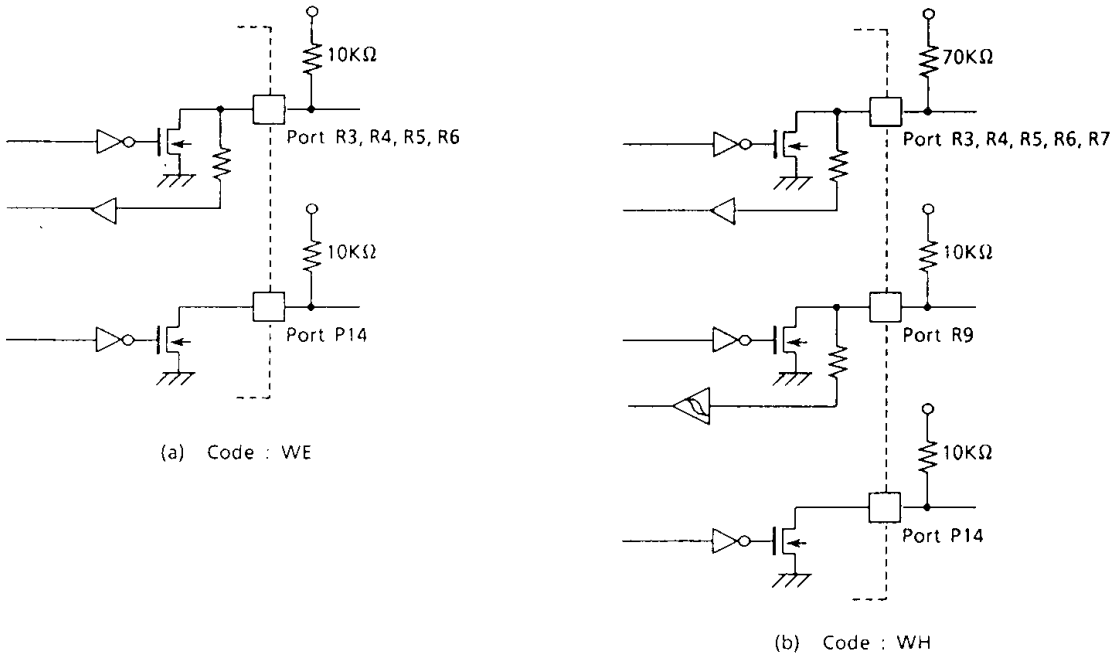


Figure 2. I/O code and external circuitry