Winbond

W83757

SUPER I/O CHIP

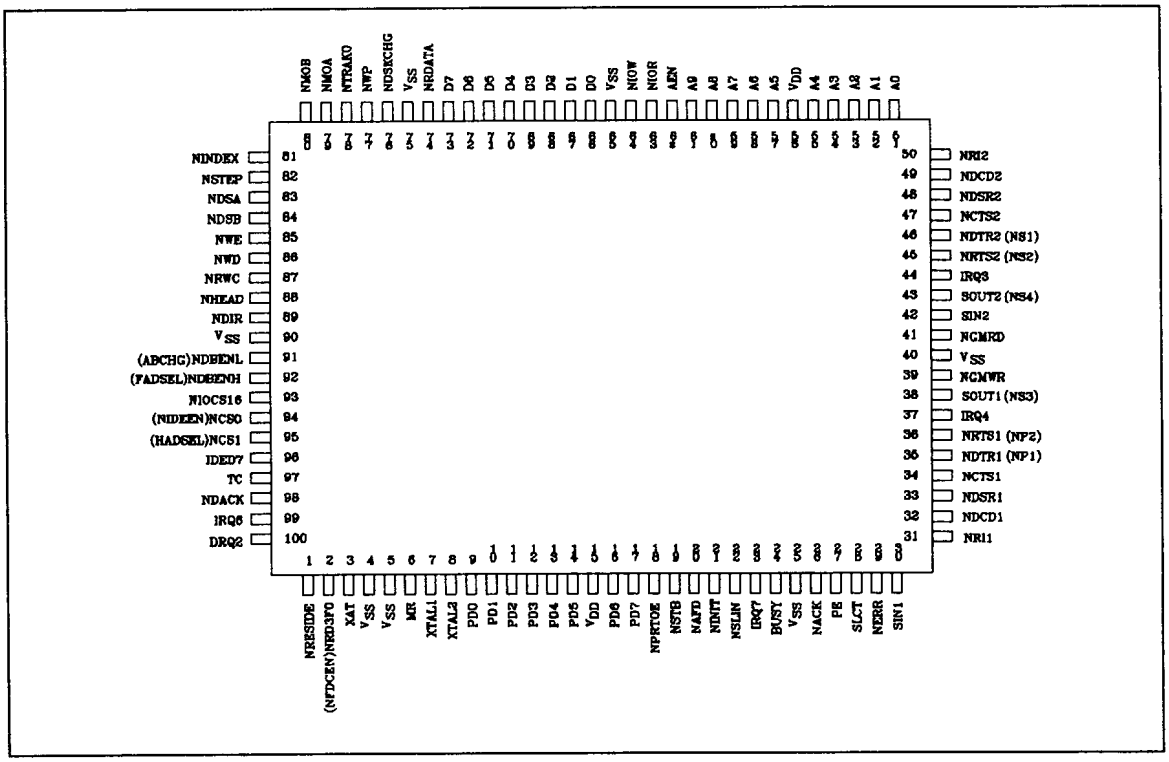
GENERAL DESCRIPTION

The W83757 is a super multi I/O chip that combines the functions of a Floppy Disk Drive adapter, serial (UART)/parallel adapter, IDE bus and game port. The W83757's disk drive adapter functions include a standard Floppy Disk Drive controller, data separator, write precompensation circuit, decode logic, data rate selection, clock generator, drive interface control logic, interrupt and DMA logic, thus greatly reducing the number of components required to interface floppy disk drives. As a UART, the chip supports serial to parallel conversion on data characters received from a peripheral device or a MODEM, and parallel to serial conversion on data characters received from the CPU. The CPU can read the complete status of the UART at any time during operation. The UART includes a programmable baud rate generator, complete MODEM control capability and a processor-interrupt system. As a parallel port, the W83757 provides the user with a fully bidirectional parallel centronics-type printer interface. Besides the above functions, this chip also supports two Embedded Hard Disk Drives (AT bus interface) and a game port decoder.

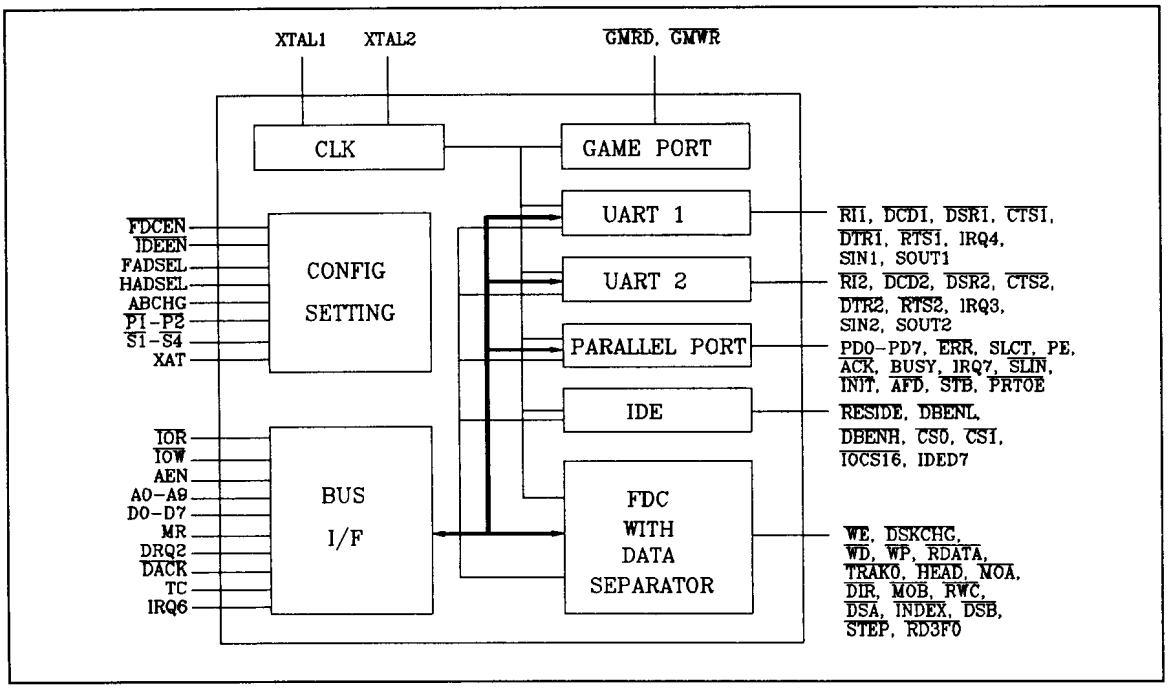
FEATURES

- Compatible with IBM PC AT/XT Disk Drive systems.
- Supports up to two 3.5", or 5.25" 360K/720K/1.2M or 1.44M Floppy Disk Drives.
- Emulates NEC765A in IBM environment.
- Supports variable write precompensation with track selectable capability.
- Built-in address mark detection circuit to simplify the read electronics.
- IBM PC system address decoder.
- Supports up to two Embedded Hard Disk Drives (IDE AT bus).
- Single 24 MHz crystal input.
- Fully programmable serial-interface characteristics:
  — 5, 6, 7 or 8-bit characters.
  — even, odd or no parity bit generation and detection.
  — 1, 1.5 or 2 stop bit generation.
- Internal diagnostic capabilities:
  — loopback control for communications link fault isolation.
  — break, parity, overrun, framing error simulation.
- Programmable baud rate generator allows division of any input clock by 1 to $(2^{16}-1)$ and generates the internal 16 $\times$ clock.
- Compatible with IBM printer port.
- 2u high performance CMOS technology.
- 100-pin QFP.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN DESCRIPTION

A. Host Interface

SYMBOL	PIN	I/O	FUNCTION
D0 ~D7	66~73	I/O	System data bus.
A0 ~A9	51~55 57~61	I	System address bus.
MR	6	I	Master reset,active high.When MR is active, the $\overline{INIT}$ is active, and STB, AUTO, and SLCT are inactive; IRQ is disabled and remains in a high impedance state. MR is low during normal operations.
AEN	62	I	System address bus enable.
$\overline{IOR}$	63	I	CPU I/O read signal.
$\overline{IOW}$	64	I	CPU I/O write signal.
$\overline{DACK}$	98	I	DMA acknowledge. When this pin is active, it indicats a DMA cycle and controller is performing DMA transfer.
TC	97	I	Terminal count. When active, this pin indicates the termination of a DMA transfer.
$\overline{IOCS16}$	93	I	16-bit I/O indiction.
DRQ2	100	O	DMA Request is being made by FDC when DRQ=1.
IRQ6	99	O	Interrupt request generated by FDC.
XAT	3	I	XT/AT select. When set to high selects XT mode. When set to low selects AT mode.
XTAL1	7	I	XTAL oscillator input.
XTAL2	8	O	XTAL oscillator output.

B. Serial Port Interface

SYMBOL	PIN	I/O	FUNCTION
$\overline{CTS1}$, $\overline{CTS2}$	34 47	I	Clear To Send is MODEM control function input. The function of these pins can be tested by the CPU by reading Bit 4 of the MODEM status register.
$\overline{DSR1}$, $\overline{DSR2}$	33 48	I	Data Set Ready. An active low indicates the MODEM or data set is ready to establish a communication link and transfer data to the UART.
$\overline{DCD1}$, $\overline{DCD2}$	32 49	I	Data Carrier Detect. An active low indicates the MODEM or data set has detected a data carrier.
$\overline{RI1}$, $\overline{RI2}$	31 50	I	Ring Indicator. An active low indicates that a ringing signal is being received by the MODEM or data set.
SIN1, SIN2	30 42	I	Serial Input. Used to receive serial data from the communication link.

	SYMBOL	PIN	I/O	FUNCTION
	$\overline{GMRD}$, $\overline{GMRW}$	41 39	O	Game port read/write control signal.
	IRQ3, IRQ4	44 37	O	Interrupt. The pins go high whenever any one of the following interrupt types has an active high condition and is enabled via the IER: Receiver error flag, Receiver data available, Transmitter holding register empty and MODEM status. The signal is high-impedance upon a reset operation.
*	SOUT1,SOUT2 (S3),(S4)	38 43	O	Serial Output. Used to transmit serial data out to the communication link. The output signal is set to a marking condition when reset.
*	$\overline{DTR1}$,$\overline{DTR2}$ (P1),(S1)	35 46	O	Data Terminal Ready. An active low informs the MODEM or data set that controller is ready to communicate.
*	$\overline{RTS1}$,$\overline{RTS2}$ (P2),(S2)	36 45	O	Request To Send. An active low informs the MODEM or data set that the controller is ready to send data.

C. Parallel Port Controller

SYMBOL	PIN	I/O	FUNCTION
BUSY	24	I	An active high indicates that the printer can't receive data. This pin is pulled high internally.
$\overline{ACK}$	26	I	An active low indicates that the printer has received the data and is ready to accept more data. This pin is pulled high internally.
PE	27	I	An active high indicates the printer has detected the end of the paper.This pin pulled high internally.
SLCT	28	I	An active high indicates the printer is selected. This pin is pulled high internally.
$\overline{ERR}$	29	I	An active low indicates the printer has encountered an error condition. This pin is pulled high internally.
$\overline{SLIN}$	22	O	Output line for detection of printer selection. This pin is pulled high internally.
$\overline{INIT}$	21	O	Output line for printer initialization. This pin is pulled high internally.
$\overline{AFD}$	20	O	An active low causes the printer to line-feed after a line is printed. This pin is pulled high internally.
$\overline{STB}$	19	O	A minimum 0.5 us width active low pulse into the printer. This pin is pulled high internally.
PD0 - PD7	9~14 16~17	I/O	Parallel port data bus.These eight lines provide a byte-wide input or output port to the system. These lines are held in a high-impedence state when the port is not selected.
$\overline{PRTOE}$	18	I	Line printer output enable.It is active low.
IRQ7	23	O	Interrupt Request is being made by printer when IRQ=1. This pin is pulled high internally.

D. Floppy and IDE Interface

SYMBOL	PIN	I/O	FUNCTION
IDED7	96	I/O	IDE data bus Bit 7.
$\overline{\text{RESIDE}}$	1	O	Reset signal for IDE interface; active low to initialize the IDE.
$\overline{\text{DBENL}}$~ABCHG	91	I/O	In output function, DBENL is for IDE data bus low byte buffer enable. When active, it accesses I/O address 1F0H-1F7H (170H-177H) and 3F6-3F7H (376H-377H). In input function, it is for A/B change mode setting during power on reset. When this pin is low, it is in normal operation. When this pin is high, it is in A/B change mode.
$\overline{\text{DBENH}}$ ~ FADSEL	92	I/O	In output function, DBENH is for IDE data bus high byte buffer enable. DBENH is active only when IOCS16 is active. When it is active, it selects I/O port address range 1F0-1F7H (170H-177H). In input function, FADSEL is for address select. When it is high, it selects I/O port address range 3F0H-3F7H. When it is low, it selects I/O port address range 370H-377H.
$\overline{\text{RD3F0}}$~$\overline{\text{FDCEN}}$	2	I/O	In output function, this pin is for Read port 3F0 in XT mode application. In input function, it is for FDC enable during power-on reset. When this pin is low, it enables the FDC port. When this pin is high, it disables the FDC port.
$\overline{\text{CS1}}$~HADSEL	95	I/O	In output function, this pin is for the IDE controller selection. CS1 decodes the HDC address 3F6H, 3F7H (376H, 377H) for ATs and 324H-327H for XTs. In input function, it is for HDC address select. When it is high, it selects I/O port address range 3F0H-3F7H, 1F0H-1F7H. When this pin is low, it selects I/O port address range 370H-377H and 170H-177H.
$\overline{\text{CS0}}$ ~ $\overline{\text{IDEEN}}$	94	I/O	In output function, this pin is for IDE controller selection. CS0 decodes the HDC address 1F0H-1F7H (170H-177H) for AT and 320H-323H for XT. In input function, it is for IDE enable during power-on reset. When this pin is high, it disables the IDE. When this pin is low, it enables the IDE.
$\overline{\text{WE}}$	85	O	Write enable. An open drain output.
$\overline{\text{DIR}}$	89	O	Direction of the head step motor. An open drain output. Logical 1 = outward motion. Logical 0 = inward motion.
$\overline{\text{HEAD}}$	88	O	Head select.This open drain output determines which disk drive head is active. Logical 1 = side 0. Logical 0 = side 1.
$\overline{\text{RWC}}$	87	O	Reduced write current. This signal can be used on two-speed disk drives to select the transfer rate. An open drain output. Logical 0 = 250kb/s, 300kb/s. Logical 1 = 500kb/s.
$\overline{\text{WD}}$	86	O	Write data. This logic low open drain writes precompensated serial data to the selected FDD. An open drain output.
$\overline{\text{STEP}}$	82	O	Step output pulses. This active low open drain output will produce a pulse to move the head to another track.

SYMBOL	PIN	I/O	FUNCTION
$\overline{INDEX}$	81	I	This active low schmitt input from the disk drive senses when the head is positioned over the beginning of a track marked by an index hole.
$\overline{TRAK0}$	78	I	Track 0. This active low schmitt input from the disk drive senses when the head is positioned over the outermost track.
$\overline{WP}$	77	I	Write protected. This active low schmitt input from the disk drive indicates that the diskette is write protected.
$\overline{RDATA}$	74	I	The read data input signal indicates a read from the FDD.
$\overline{DSKCHG}$	76	I	Diskette change.This signal is active low at power on and whenever the diskette is removed. It remains active until a STOP pulse is received with the diskette in pulse.
$\overline{MOA}$	79	O	Moter on A. When set to 0, this pin enables disk drive 1. This is an open drain output.
$\overline{MOB}$	80	O	Moter on B. When set to 0, this pin enables disk drive 0. This is an open drain output.
$\overline{DSA}$	83	O	Drive select A. When set to 0, this pin enables disk drive 1. This is an open drain output.
$\overline{DSB}$	84	O	Drive select B. When set to 0, this pin enables disk drive 0. This is an open drain output.

E. Power and Ground

SYMBOL	PIN	I/O	FUNCTION
V_{CC}	15 56	I	+5 power supply for digital circuitry.
V_{SS}	4 5 25 40 65 75 90	I	Ground

Note: $\overline{S1}$, $\overline{S2}$, $\overline{S3}$, $\overline{S4}$, $\overline{P1}$, and $\overline{P2}$ are power-on settings for I/O Port Select.

RS232 I (ACE1)			RS232 II (ACE2)			PRINTER		
$\overline{S1}$	$\overline{S3}$	Select port	$\overline{S2}$	$\overline{S4}$	Select port	$\overline{P1}$	$\overline{P2}$	Select port
L	L	2E8	L	L	3E8	L	L	3BC
L	H	3F8	L	H	2F8	L	H	378
H	L	3E8	H	L	2E8	H	L	278
H	H	Disable	H	H	Disable	H	H	Disable

BLOCK DIAGRAM AND FUNCTION DESCRIPTIONS

A. FDC and IDE

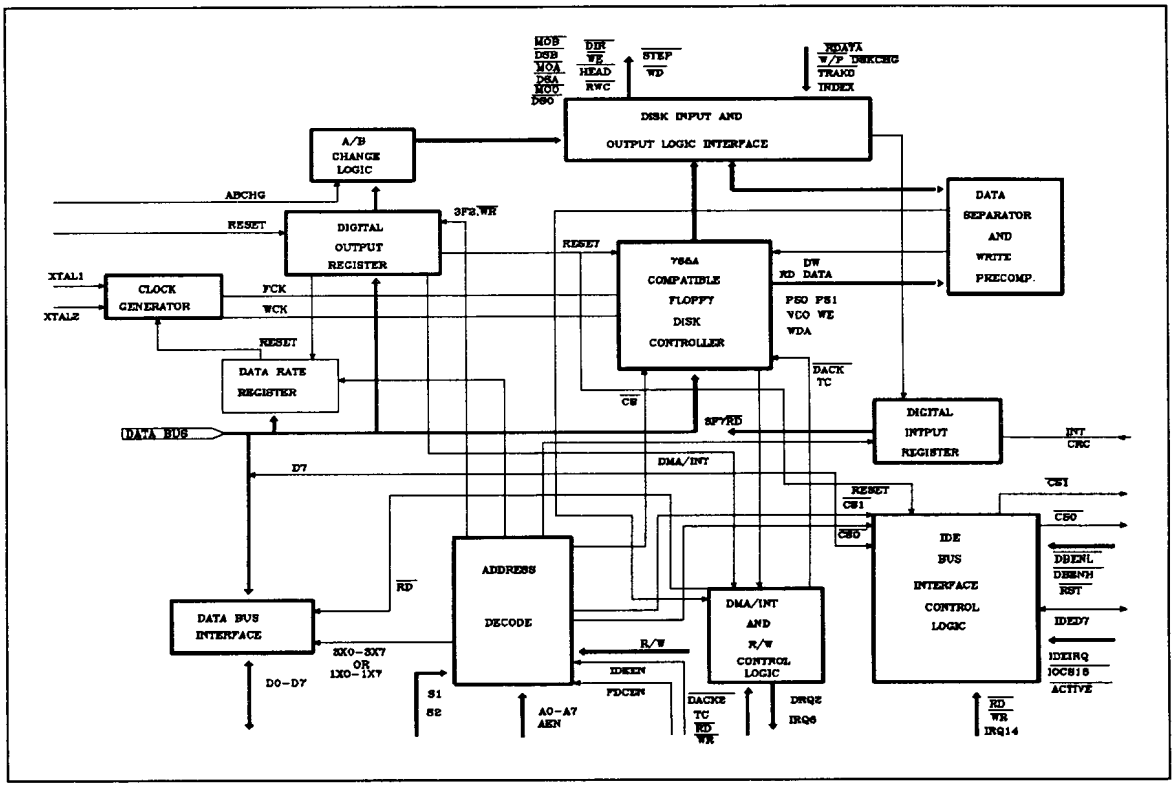


Fig. 1

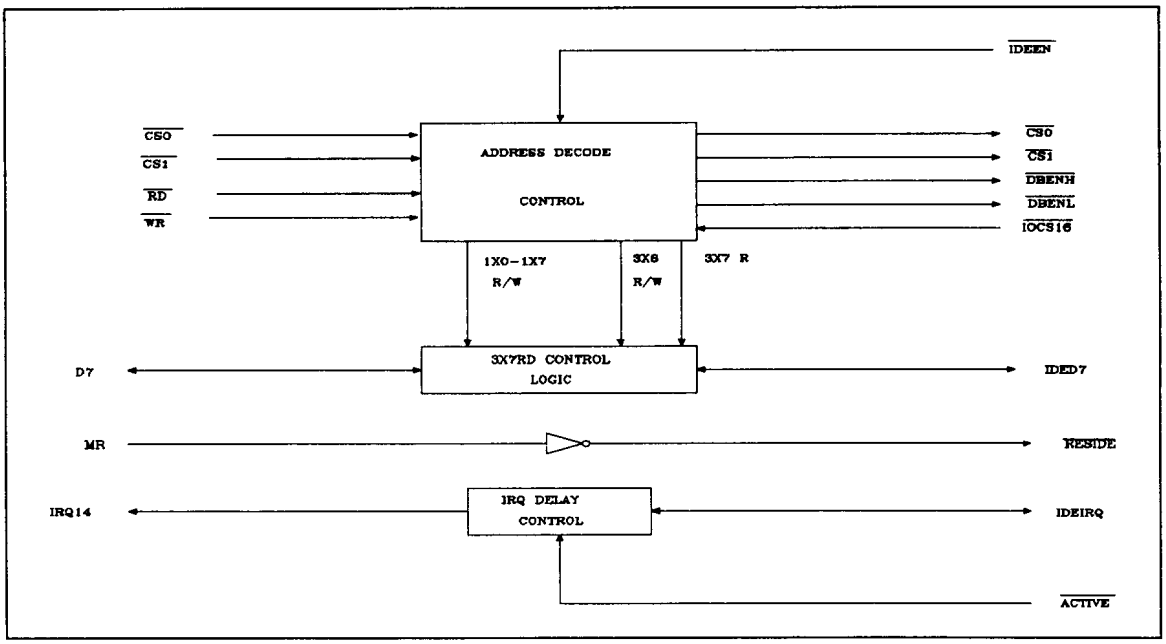


Fig. 2

(1) Clock/Timing Generation

This module is designed to generate FCK and WCK at different data transfer rates as specified by the Data Rate Register. The input XIN is divided by the divisor to generate FCK, which is fed into a synchronous down counter to issue WCK. The typical relation between these signals and the data transfer rate is summarized in the following table:

Transfer Rate	FCK	WCK
500Kb/S	8.0 MHz	1 MHz
300Kb/S	4.8 MHz	600 KHz
250Kb/S	4.0 MHz	500 KHz

(2) AB Change Mode

The AB change mode may be used to change the drive assignments of Floppy Disk Drives A and B. When the AB change jumper is set to high, and a power-on reset is performed, drive A is renamed drive B, and drive B becomes drive A without switching the drive cables. To return to the original drive assignments, simply set the AB change jumper to low and perform a second power-on reset.

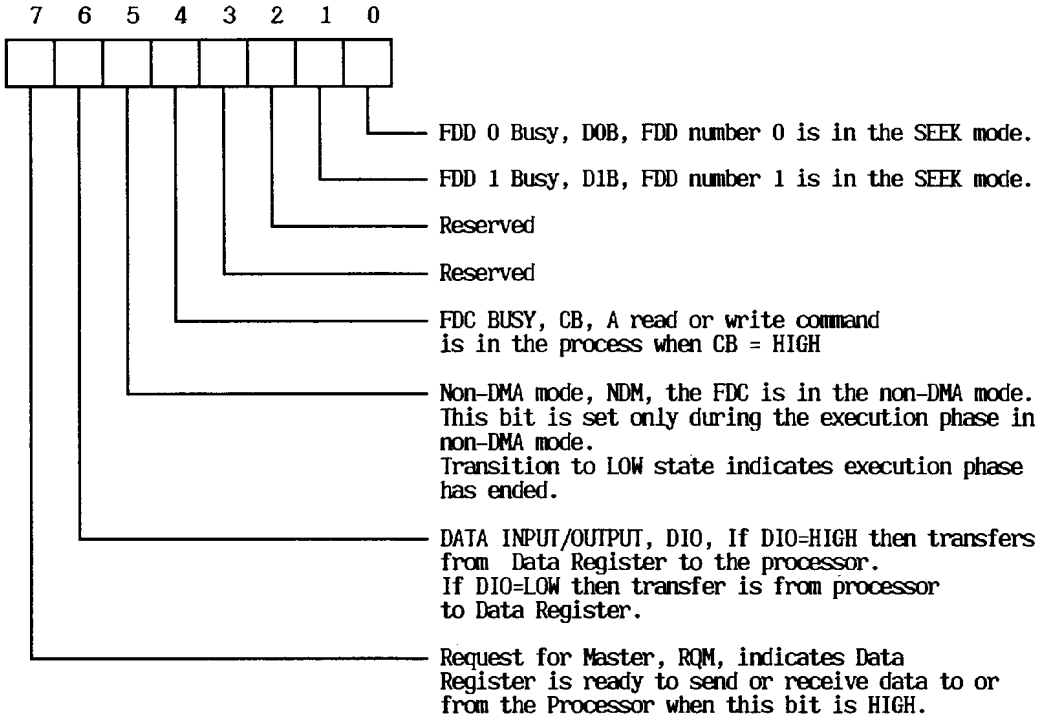
(3) Register Descriptions

There are six registers in the W83757. Four registers show the status of signals used in diskette operations, and two are controller registers. The addresses of these six registers are defined below:

ADDRESS		REGISTER	
Primary (Addsel=1)	Secondary (Addsel=0)	Read	WRITE
3F2	372		DO Register
3F4	374	MS Register	
3F5	375	DT Register	DT Register
3F7	377	DI Register	DR Register

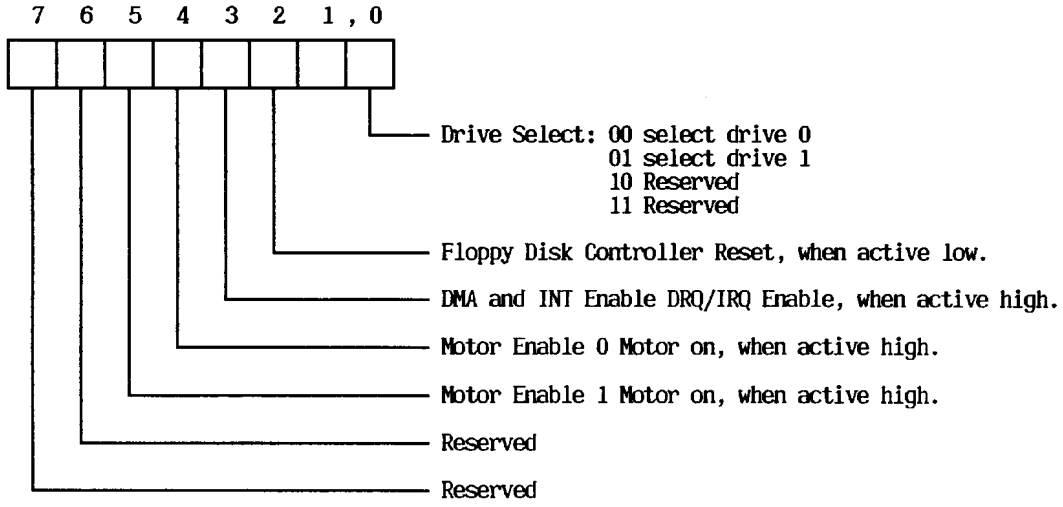
(4) Main Status Register (MS Register)

The Main Status Register is used to control the flow of data between the microprocessor and the controller. The following are the bit definitions:



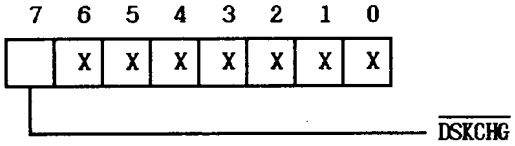
(5) Digital Output Register (DO Register)

The Digital Output Register is a write-only register controlling drive motors, drive selection, DRQ/IRQ enable, and UPD765 resetting. All the bits are cleared by the RESET pin. The bit definitions are as follows:



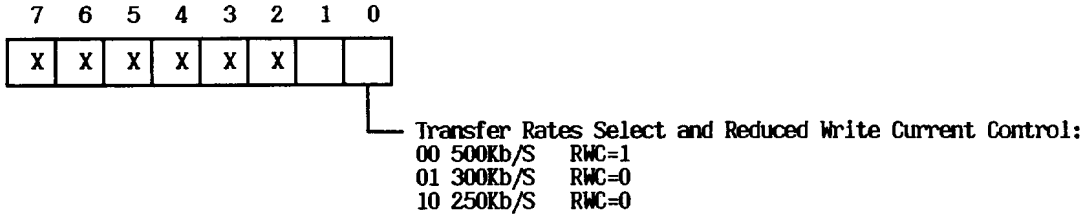
(6) Digital Input Register (DI Register)

The Digital Input Register is an 8-bit read-only register for diagnostic purposes. In PC/XT and ATs only Bit 7 is checked by the BIOS. When the register is read, Bit 7 shows the complement of $\overline{\text{DSKCHG}}$ while other bits on the data bus remain tri-stated. Bit definitions for the register are as follows:.



(7) Data Rate Register (DR Register)

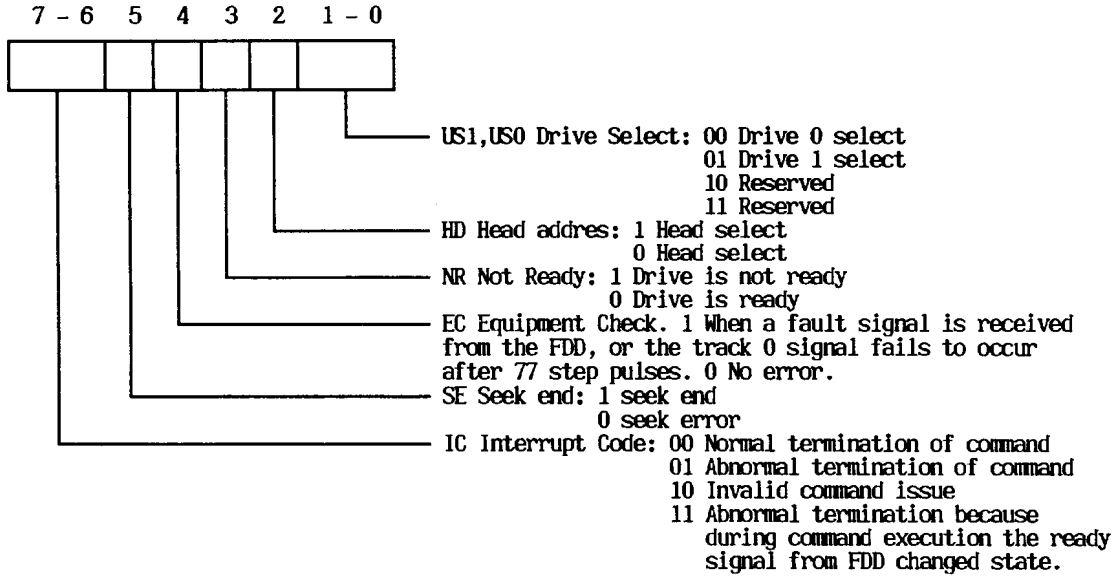
The Data Rate Register is used to set the transfer rate and select write precompensation.



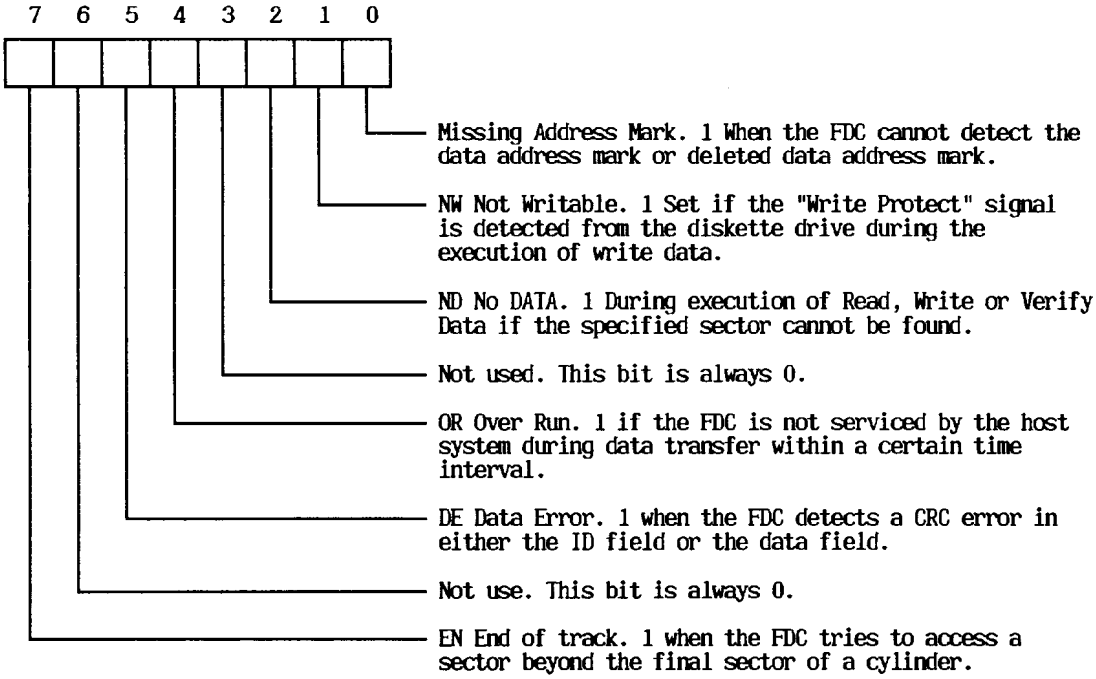
(8) Data Register (DT Register)

The Data Register consists of four status registers in a stack with only one register presented to the data bus at a time. This register stores data, commands, and parameters, and provides diskette-drive status information. Data bytes are passed through the data register to program or obtain results after a command.

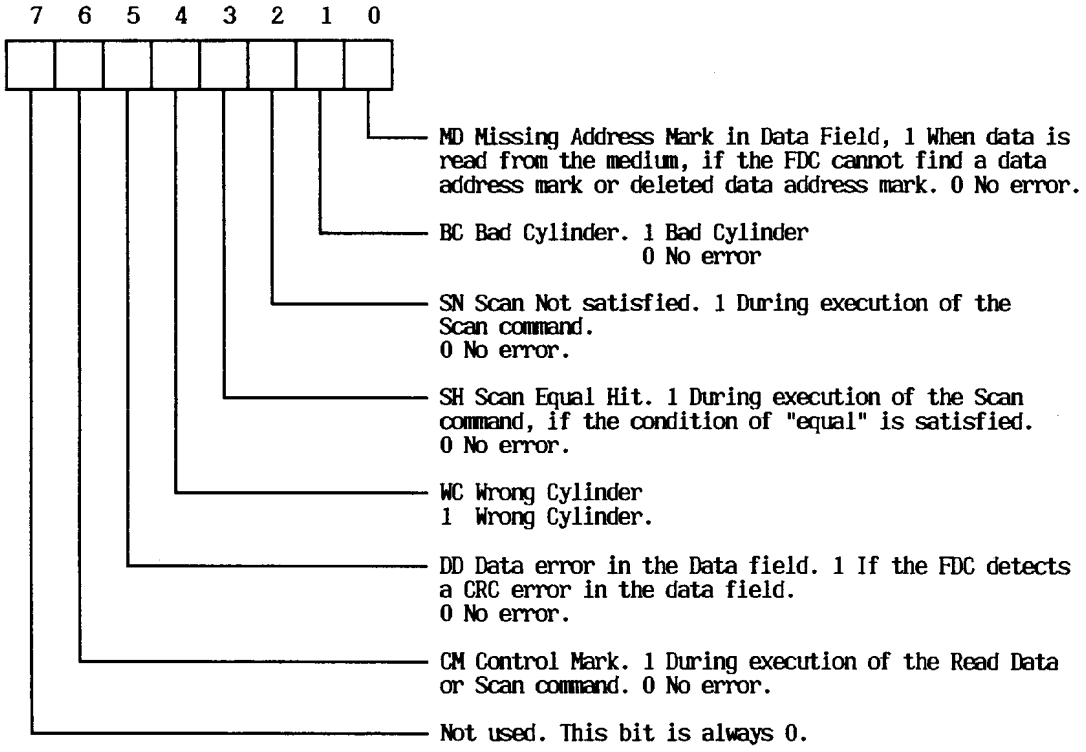
- Status Register 0 (ST0)



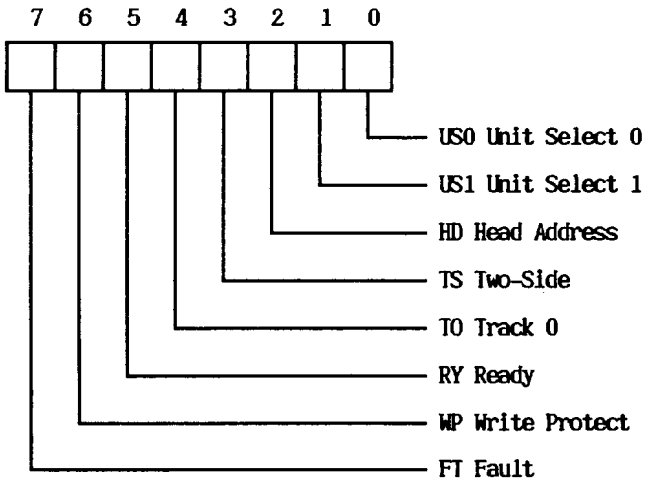
- **Status Register 1 (ST1)**



- **Status Register 2 (ST2)**



- **Status Register 3 (ST3)**



(9) IDE Decode Description

(a) When Processor selects Port 1F0-1F7 (or 170-177), chip system enables $\overline{CS0}$=LOW; otherwise, $\overline{CS0}$=HIGH. When Processor selects Port 3F6-3F7 (or 376-377) chip system enables $\overline{CS1}$=LOW; otherwise, $\overline{CS1}$=HIGH.

(b) Because the Digital Input Register reflects the current state of the floppy change flag on Bit 7 of this register, we need to disable this bit on reading this register.

(10) Hard Disk Task Files Map

I/O ADDRESS		REGISTERS	
PRIMARY (ADDSEL=1)	SECONDARY (ADDSEL=0)	READ	WRITE
1F0	170	Data Register	Data Register
1F1	171	Error Register	Write-Precomp
1F2	172	Sector Count	Sector Count
1F3	173	Sector Number	Sector Number
1F4	174	Cylinder Low	Cylinder Low
1F5	175	Cylinder High	Cylinder high
1F6	176	SDH Register	SDH Register
1F7	177	Status Register	Command Register
3F6	376	Alternate Status	Fixed Disk Control
3F7	377	Digital Input	Undefined

B. UART/PARALLEL PORT

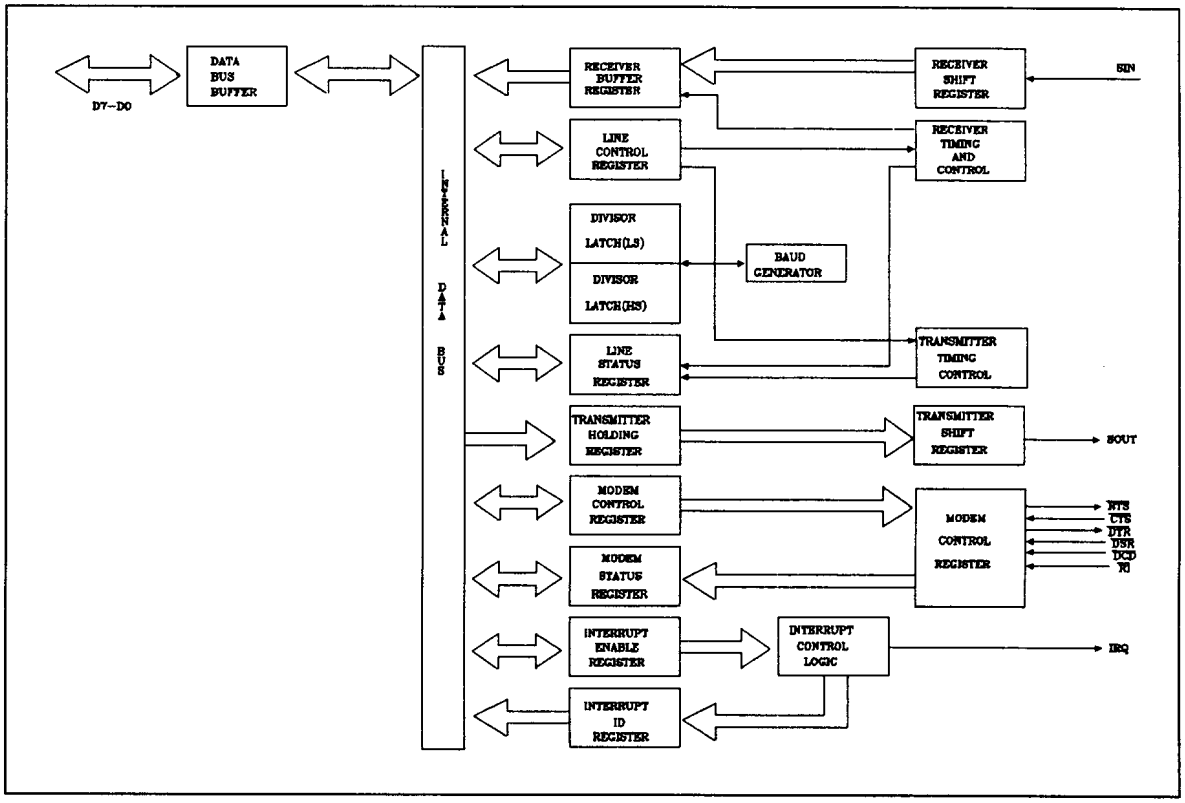


Fig. 5

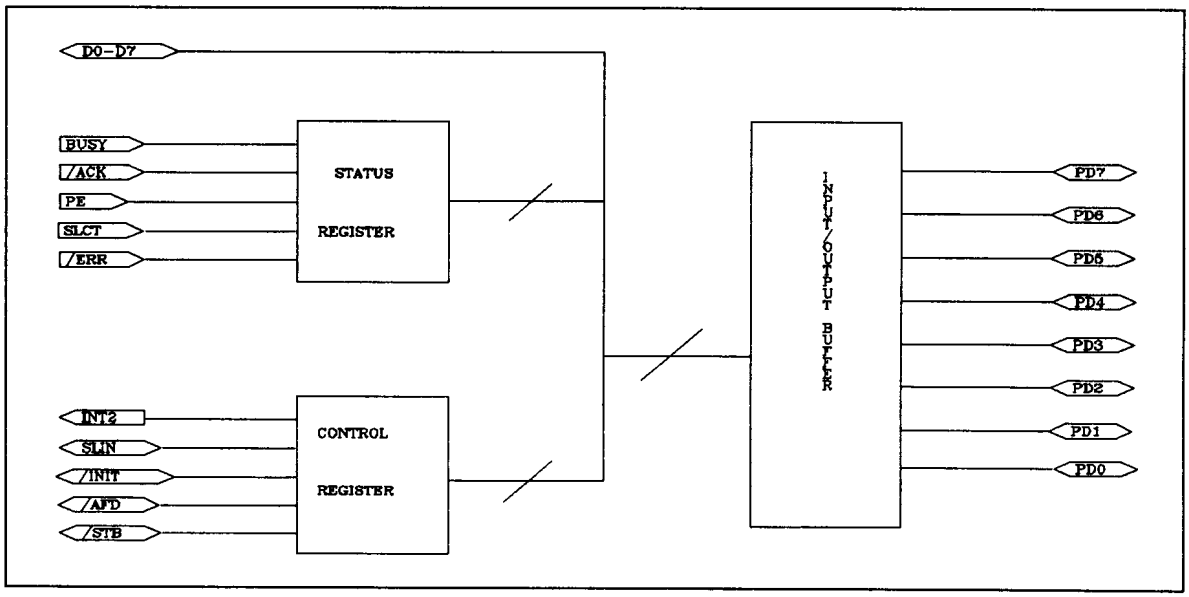


Fig. 6

(1) Register Address

DLAB	A2	A1	A0	REGISTER
0	0	0	0	Receiver Buffer (read) Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable
x	0	1	0	Interrupt Identification (read only)
x	0	1	1	Line Control
x	1	0	0	MODEM Control
x	1	0	1	Line Status
x	1	1	0	MODEM Status
x	1	1	1	Scratch
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significant byte)

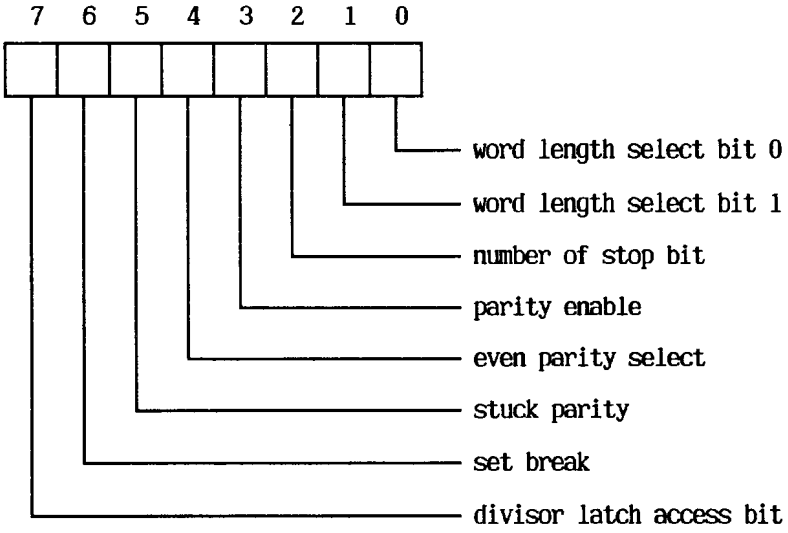
A0	A1	$\overline{IOR}$	$\overline{IOW}$	REGISTER
0	0	1	0	Write port
0	0	0	1	Read port
1	0	0	1	Printer status buffer
0	1	1	0	Printer control latch
0	1	0	1	Printer control swapper

(2) Asynchronous Communication Elements (ACE1, ACE2)

The ACEs are used to convert parallel data to a serial format on the transmit side and convert serial data to parallel on the receiver side. The serial format, in order of transmission and reception, is a start bit, followed by five to eight data bits, a parity bit (if programmed) and one, one and half (five-bit format only) or two stop bits. The ACEs are capable of handling divisors of 1 to 2^{16}, and producing a 16 $\times$ clock for driving the internal transmitter logic. Provisions are also included to use this 16 $\times$ clock to drive the receiver logic. Also included in the ACE is a complete MODEM control capability, and a processor interrupt system that may be software tailored to the computing time required to handle the communication link.

(3) Line Control Register

The system programmer specifies the format of the asynchronous data communication exchange through the Line Control Register. In addition to controlling the format, the programmer may retrieve the contents of the Line Control Register for inspection.



Notes:

Bits 0,1: Specify the number of bits in each serial character that is sent or received. The encoding of Bits 0 and 1 is as follows:

Bit 1	Bit 0	word length
0	0	5
0	1	6
1	0	7
1	1	8

Bit 2: Specifies the number of stop bits in each serial character that is sent or received. If Bit 2 is a logic 0, one stop bit is generated or checked in the data sent or received. If Bit 2 is logic 1 when a 5-bit word length is selected through Bits 0 and 1, one and half stop bits are generated or checked. If Bit 2 is a logic 1 when either a 6, 7, or 8-bit word length is selected, 2 stop bits generated or checked.

Bit 3: Specifies the parity enable. When Bit 3 is logic 1, a parity bit is generated (transmit data) or checked (receive data) between the last data word and stop bit of the serial data (the parity bit is used to produce an even or odd number of 1's when the data-word bits and parity bit are summed).

Bit 4: Specifies the even-parity select. When Bit 3 is a logic 1 and Bit 4 is a logic 0, an odd number of logic 1's is sent or checked in the data word bits and parity bit. When Bit 3 is a logic 1 and Bit 4 is a logic 1, an even number of logic 1's is sent or checked.

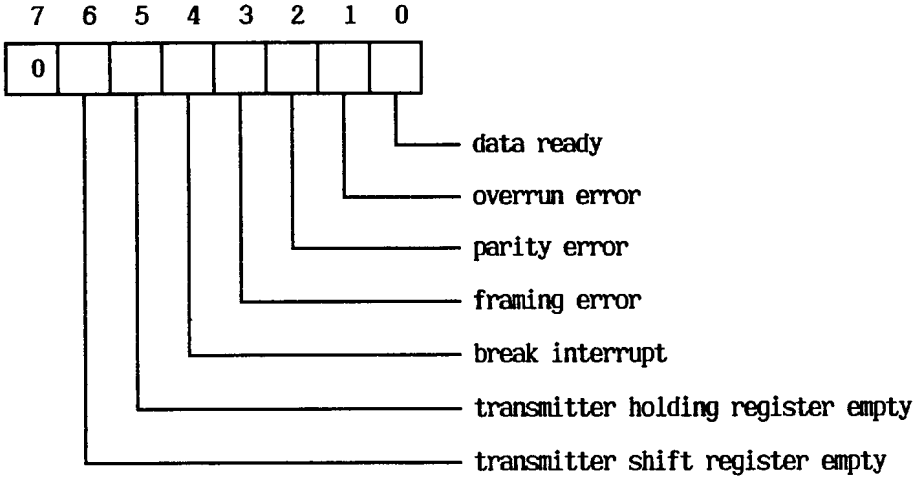
Bit 5: Specifies the stuck-parity. When Bit 3 is a logic 1 and Bit 5 is a logic 1, the parity bit is sent and then detected by the receiver as a logic 0, if Bit 4 is a logic 1 or as a logic 1, if Bit 4 is a logic 0.

Bit 6: Specifies the set-break control. When Bit 6 is set to a logic 1 the serial output (SOUT) is forced to the spacing (logic 0) state. The break is disabled by setting Bit 6 to a logic 0.

Bit 7: Specifies the divisor-latch access (DLAB). This bit must be set to high to gain access to the divisor latches of the Baud Rate Generator during a read or write operation. It must be set to low to gain access to the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

(4) Line Status Register

This 8-bit register provides status information to the CPU concerning the data transfer.



Notes:

Bit 0: This is the receiver data ready (DR) indicator. It is set to logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 may be reset to logic 0 by the processor either reading the data in the Receiver Buffer Register or writing logic 0 to it.

Bit 1: This is the overrun error (OE) indicator. It indicates that data in the Receiver Buffer Register was not read by the processor before the next character was transferred into the register, thereby destroying previous character. The OE indicator is reset whenever the processor reads the contents of the Line Status Register.

Bit 2: This is the parity error (PE) indicator and indicates the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to logic 1 upon detection of a parity error, and is reset to logic 0 whenever the processor reads the contents of the Line Status Register.

Bit 3: This is the framing error (FE) indicator. It indicates the received character does not have a valid stop bit. Bit 3 is set to logic 1 whenever the stop bit following the last data bit or parity bit is detected as a zero bit (spacing level). The FE indicator is reset whenever the CPU reads the contents of the Line Status Register.

Bit 4: This bit is the break interrupt (BI) indicator. It is set to logic 1 whenever the received data input is held in the spacing state (logic 0) for longer then a full word transmission time (e.g., total time of the start bit + data bits + parity stop bits). The BI indicator is reset whenever the CPU reads the contents of the Line Status Register.

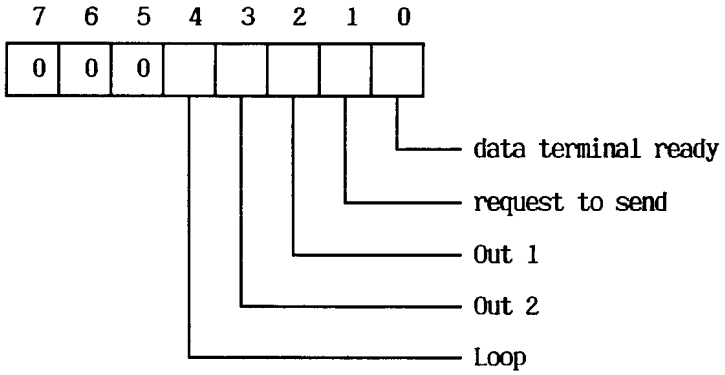
Bit 5: This bit is the Transmitter Holding Register empty (THRE) indicator. It indicates the controller is ready to accept a new character for transmission. In addition, this bit causes the controller to issue an interrupt to the processor when the THRE interrupt enable is set to active. The THRE bit is set to logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. It is reset to logic 0 when the processor loads the Transmitter Holding Register. PE bit is set to logic 1 upon detection of a parity error and is reset to logic 0 whenever the processor reads the contents of the Line Status Register.

Bit 6: This bit is the transmitter empty (TEME) indicator. It is set to logic 1 whenever the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. It is reset to logic 0 whenever THR or TSR contains a data character.

Bit 7: This bit is permanently set to logic 0.

(5) MODEM Control Register

This 8-bit register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM).



Notes:

Bit 0: This bit controls the $\overline{DTR}$ output. When Bit 0 is set to logic 1, the $\overline{DTR}$ output is forced active. When Bit 0 is reset to logic 0, the $\overline{DIR}$ output is forced inactive.

Bit 1: This bit controls the $\overline{RTS}$ output. Bit 1 forces the $\overline{RTS}$ output in a manner identical to that described above for Bit 0.

Bit 2: This bit is only used in the diagnostic mode.

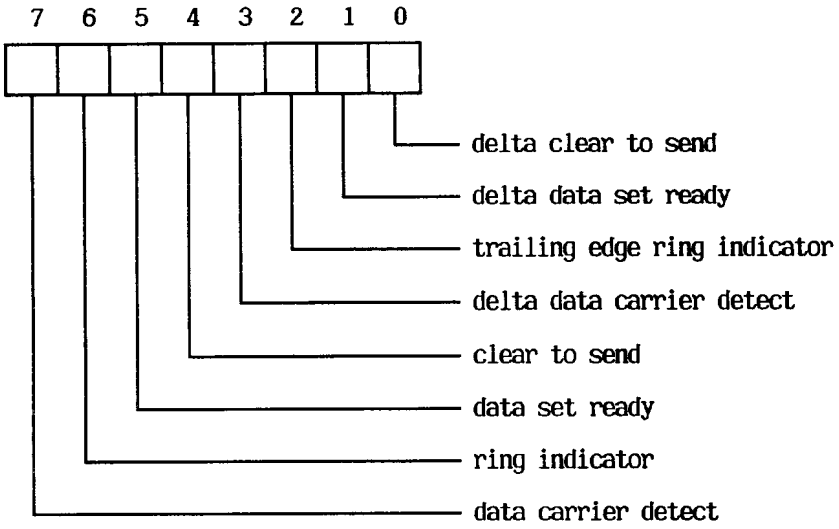
Bit 3: The enable of the interrupt output can be set to an active state by programming this bit to a high level.

Bit 4: This bit provides a loopback feature for diagnostic testing of the controller. When Bit 4 is set to logic 1, the following occur: the SOUT is set to the marking (logic 1) state; the SIN is disconnected; the output of the Transmitter Shift Register is "looped back" into the receiver shift register input; the four MODEM control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, and $\overline{RI}$) are disconnected; the four outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT1}$, and $\overline{OUT2}$) are internally connected to the four MODEM control inputs; and the MODEM output pins are forced to their inactive state (high). In the diagnostic mode, data sent is immediately received. This feature allows the processor to verify the transmit-data and receive-data path of the controller. In the diagnostic mode, the receiver and transmitter interrupt are fully operational as the MODEM control interrupts. But the interrupts' sources are now the lower four bits of the MODEM control register instead of the four control inputs. The interrupts are still controlled by the Interrupt Enable Register. The controller's interrupt sys-

tem can be tested by writting to the lower six bits of the Line Status Register and the lower four bits of the MODEM Status Register. Setting any of these bits to logic 1 generates the appropriate interrupt. When reset, these interrupts are the same as for normal operation. To return to normal operation, these registers must be reprogrammed for normal operation, and Bit 4 of the MCR must be reset to logic 0.

(6) MODEM Status Register

This 8-bit register provides the current state of the control lines from the MODEM to the processor. In addition, four bits of the MSR provide change information. These four bits are set to logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the processor reads this register.



Notes:

Bit 0: This bit is the delta clear to send indicator. It indicates the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the processor.

Bit 1: This bit is the delta data set ready indicator. It indicates the $\overline{DSR}$ input to the chip has changed state since last time it was read by the processor.

Bit 2: This bit is the trailing edge ring indicator. It indicates the $\overline{RI}$ input to the chip has changed from an active condition to an inactive condition.

Bit 3: This bit is the delta data carrier detect indicator. It indicates the $\overline{DCD}$ input to the chip has changed state.

Bit 4: This bit is the opposite of the $\overline{CTS}$ input. If Bit 4 of the MCR loop is set to a logic 1, this bit is equivalent to RTS of the MCR.

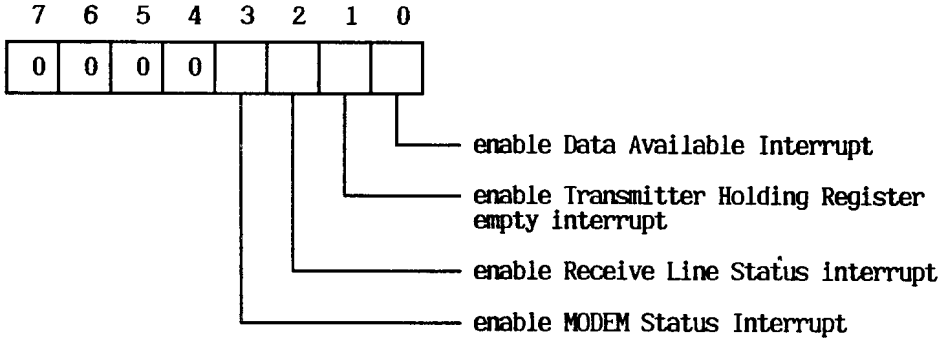
Bit 5: This bit is the opposite of the $\overline{DSR}$ input. If Bit 4 of the MCR is set to a logic 1, this bit is equivalent to DTR of the MCR.

Bit 6: This bit is the opposite of the $\overline{RI}$ input. If Bit 4 of the MCR is set to a logic 1, this bit is equivalent to OUT1 of the MCR.

Bit 7: This bit is the opposite of the $\overline{DCD}$ input. If Bit 4 of the MCR is set to a logic 1, this bit is equivalent to OUT2 of the MCR.

(8) Interrupt Enable Register

This 8-bit register allows the four types of controller interrupts to activate the interrupt output signal separately. The interrupt system can be totally disabled by resetting Bits 0 through 3 of the Interrupt Enable Register (IER). By setting the appropriate bits of this register to a logic 1, a selected interrupt can be enabled.



Notes:
Bit 0: When set to logic 1, enables the Receive Data Available Interrupt.
Bit 1: When set to logic 1, enables the Transmitter Holding Register Empty interrupt.
Bit 2: When set to logic 1, enables the Receive Line Status interrupt.
Bit 3: When set to logic 1, enables the modem status interrupt.
Bits 4-7: These four bits are always logic 0.

(9) Programmable Baud Rate Generator

The controller contains a Programmable Baud Rate Generator that is capable of taking any clock input (DC to 3.1 MHz) and dividing it by a divisor from 1 to 2^{16}-1. The output frequency of the Baud Rate Generator is the baud rate multiplied by 16. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to ensure desired operation of the Baud Rate Generator. When either of the Divisor Latches is loaded a 16-bit counter is immediately loaded.
The following table illustrates the use of a baud rate generator with crystal frequency of 1.8432 MHz. For baud rates of 38400 and below, the error obtained is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen. The W 83757 uses 24 MHz to generate the 1.8432 MHz frequency.

- Baud Rate using 24 MHz to generated 1.8432 MHz

Desired Baud Rate	Decimal Divisor Used to Generate 16×CLOCK	PerCent Error Difference between Desired and Actual
	1.8432M	1.8432M
50	2304	-
75	1536	-
110	1047	0.026
134.5	857	0.058
150	768	-
300	384	-
600	192	-
1200	96	-
1800	64	-
2000	58	0.69
2400	48	-
3600	32	-
4800	24	-
7200	16	-
9600	12	-
19200	6	-
38400	3	-
56000	2	2.86

(10) Scratchpad Register

This 8-bit Read/Write Register does not control the UART in any way. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

(11) Printer Interface Logic

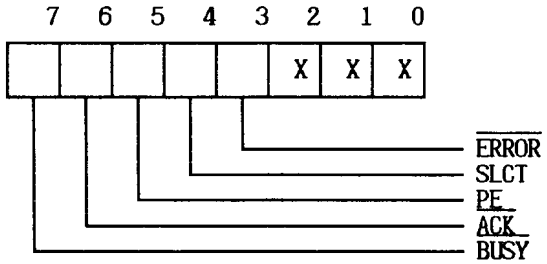
The parallel portion of the W83757 makes possible the attachment of various devices that accept eight bits of parallel data at standard TTL level.

(12) Data Swapper

The system microprocessor can read the contents of the printer's Data Latch through the Data Swapper by reading the Data Swapper address.

(13) Printer Status Buffer

The system microprocessor can read the printer status by reading the address of the Printer Status Buffer. The bit definitions are as follows:



Notes:

Bit 7: This signal may become active during data entry, when the printer is off-line during printing, or when the print head is changing position or in an error state. When Bit 7 is active, the printer is busy and can not accept data.

Bit 6: This bit represents the current state of the printer's $\overline{ACK}$ signal. A 0 means the printer has received the character and is ready to accept another. Normally, this signal will be active for approximately 5 microseconds before $\overline{BUSY}$ stops.

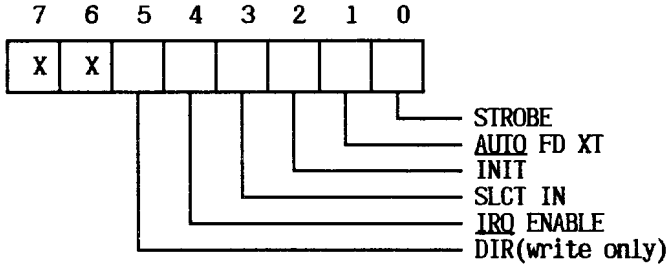
Bit 5: A 1 means the printer has detected the end of paper.

Bit 4: A 1 means the printer is selected.

Bit 3: A 0 means the printer has encountered an error condition.

(14) Printer Control Latch & Printer Control Swapper

The system microprocessor can read the contents of the printer control latch by reading the address of printer control swapper. Bit definitions are as follows:



Notes:

Bit 5: Direction control bit (only used when $\overline{PRTOE}$ is high). When logic 1, the output buffers in the parallel port are disabled allowing data driven from external sources to be read; when logic 0, they work as a printer port. This bit is write-only.

Bit 4: A 1 in this position allows an interrupt to occur when $\overline{ACK}$ changes from low state to high state.

Bit 3: A 1 in this bit position selects the printer.

Bit 2: A 0 starts the printer (50 microsecond pulse, minimum).

Bit 1: A 1 causes the printer to line-feed after a line is printed.

Bit 0: A 0.5 microsecond minimum high active pulse clocks data into the printer. Valid data must be present for a minimum of 0.5 microseconds before and after the strobe pulse.

- Parallel Port Registers

REGISTER	REGISTER BITS							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read Port	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Read Status	$\overline{BUSY}$	$\overline{ACK}$	PE	SLCT	$\overline{ERROR}$	1	1	1
Read Control	1	1	1	IRQ ENB	SLIN	$\overline{INIT}$	$\overline{AUTOFD}$	$\overline{STROBE}$
Write Port	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Write Control	1	1	1	IRQ ENB	SLIN	$\overline{INIT}$	$\overline{AUTOFD}$	$\overline{STROBE}$

MAXIMUM ABSOLUTE RATINGS

PARAMETER	RATING	UNIT
Power Supply Voltage	-0.3 to 7.0	V
Input Voltage	V_{SS}-0.3 to V_{DD}+0.3	V
Operating Temperature	0 to +70	℃
Storage Temperature	-55 to +150	℃

D.C. CHARACTERISTICS

(Ta = 0 ℃ to 70 ℃ , V_{DD} = 5V ± 10%, V_{SS} = 0V)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	CONDITION
All Inputs (except D0-D7,XTALI)					
Input Low Voltage	V_{IL}	-0.3	0.8	V	
Input High Voltage	V_{IH}	2.0	V_{DD}+0.3		
Input Leakage Current	I_{LIH}		10	μA	$V_{IN}=V_{DD}$
Input Leakage Current	I_{LIL}		-100	μA	V_{IN}=0V
Host Data Bus (D0-D7, IRQ6, DRQ2, $\overline{RD3F0}$)			0.4	V	I_{OL}=1.2mA(RD3F0)
Output Low Voltage	V_{OLB}	2.4	0.4	V	I_{OL}=12mA (D0~D7, IRQ6, DRQ2)
Output High Voltage	V_{OHB}	2.4	VDD	V	I_{OH}=-400μA
Leakage Current	I_{LOB}		10	μA	$V_{IN}=V_{DD}$
			-10	μA	V_{IN}=0V
Disk Interface Input ($\overline{WP}$, $\overline{INDEX}$, $\overline{TRAK0}$, $\overline{RDATA}$, $\overline{DSKCHG}$) and MR					
Input Hysteresis	V_H	0.25		V	
Disk Interface Output ($\overline{MOA}$-$\overline{MOB}$, $\overline{DSA}$-$\overline{DSB}$, $\overline{RWC}$, $\overline{DIR}$, $\overline{STEP}$, $\overline{WD}$, $\overline{WE}$, $\overline{HEAD}$)					
Output Low Voltage	V_{OLD}		0.4	V	I_{OL}=24mA
Leakage Current	I_{LOH}		10	μA	$V_{OUT}=V_{DD}$
VDD Supply Current	I_{DD}		200	mA	
IDE Interface Outputs ($\overline{CS0-1}$, $\overline{DBENH}$, $\overline{DBENL}$, $\overline{RESIDE}$, $\overline{IDED7}$)					
Output Low Voltage	V_{OLD}		0.4	V	I_{OL}=1.2mA($\overline{DBENH}$, $\overline{DBENL}$), I_{OL}=12mA (RESIDE, CS0-1, IDED7)
Leakage Current	I_{LOH}		10	μA	$V_{IN}=V_{DD}$

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	CONDITIONS
Leakage Current	I_{LOL}		-10	μA	V_{IN}=0V
UART. parallel interface					
Output Voltage	V_{OL}		0.4	V	I_{OL}=12mA on PD0-PD7, 2mA on all other outputs
	V_{OH}		2.4	V	I_{OH}=-0.2mA on PD0-PD7, -0.2mA on all other outputs

AC CHARACTERISTICS

A. FDC: Data rate = 500/300/250KB/sec

PARAMETER	SYMBOL	MIN.	TYP.*	MAX.	UNIT	TEST CONDITIONS
A9-A0, AEN, $\overline{DACK}$, setup time TO IOR ↓	T_{AR}	25			ns	
A9-A0, AEN, $\overline{DACK}$, hold time from IOR ↑	T_{RA}	0			ns	
$\overline{IOR}$ width	T_{RR}	80			ns	
Data access time from $\overline{IOR}$ ↓	T_{FD}			80	ns	CL = 100pf
Data hold time from $\overline{IOR}$ ↓	T_{DH}	10			ns	CL = 100pf
SD to float from $\overline{IOR}$ ↑	T_{DF}	10		50	ns	CL = 100pf
IRQ delay from $\overline{IOR}$ ↑	T_{RI}			360/570 /675	ns	
A9-A0, AEN, $\overline{DACK}$ setup time to $\overline{IOW}$ ↓	T_{AW}	25			ns	
A9-A0, AEN, $\overline{DACK}$ hold time from $\overline{IOW}$ ↑	T_{WA}	0			ns	
$\overline{IOW}$ width	T_{WW}	60			ns	
Data setup time to $\overline{IOW}$ ↑	T_{DW}	60			ns	
Data hold time from $\overline{IOW}$ ↑	T_{WD}	0			ns	
IRQ delay from $\overline{IOW}$ ↑	T_{WI}			360/570 /675	ns	
DMA cycle time	T_{MCY}	27			μs	
$\overline{DMA}$ reset delay time from DACK ↓	T_{AM}			50	ns	

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
DRQ to $\overline{DACK}$ delay	T_{MA}	0			ns	
$\overline{DACK}$ width	T_{AA}	260/430 /510			ns	
$\overline{IOR}$ delay from DRQ	T_{MR}	0			ns	
$\overline{IOW}$ delay from DRQ	T_{MW}	0			ns	
$\overline{IOW}$ or $\overline{IOR}$ response time from DRQ	T_{MRW}			12/20/24	us	
TC Width	T_{TC}	135/220 /260			ns	
RESET Width	T_{RST}	1.8/3 /3.5			μs	
$\overline{INDEX}$ Width	T_{IDX}	0.5/0.9 /1.0			μs	
$\overline{DIR}$ setup time to $\overline{STEP}$	T_{DST}	1.0/1.6 /2.0			μs	
$\overline{DIR}$ hold time from $\overline{STEP}$	T_{STD}	24/40/48			μs	
$\overline{STEP}$ pulse width	T_{STP}	6.8/11.5 /13.8	7/11.7 /14	7.2/11.9 /14.2	μs	
$\overline{STEP}$ cycle time	T_{SC}	**	**	**	μs	
$\overline{WD}$ pulse width	T_{WDD}	100/185 /225	125/210 /250	150/235 /275	ns	
Write Precompensation	T_{WPC}	100/138 /225	125/210 /250	150/235 /275	μs	

Notes:

*** Typical values for T = 25 ℃ and nominal supply voltage.**

**** Programmable from 2ms through 32ms in 2ms increments.**

B. IDE

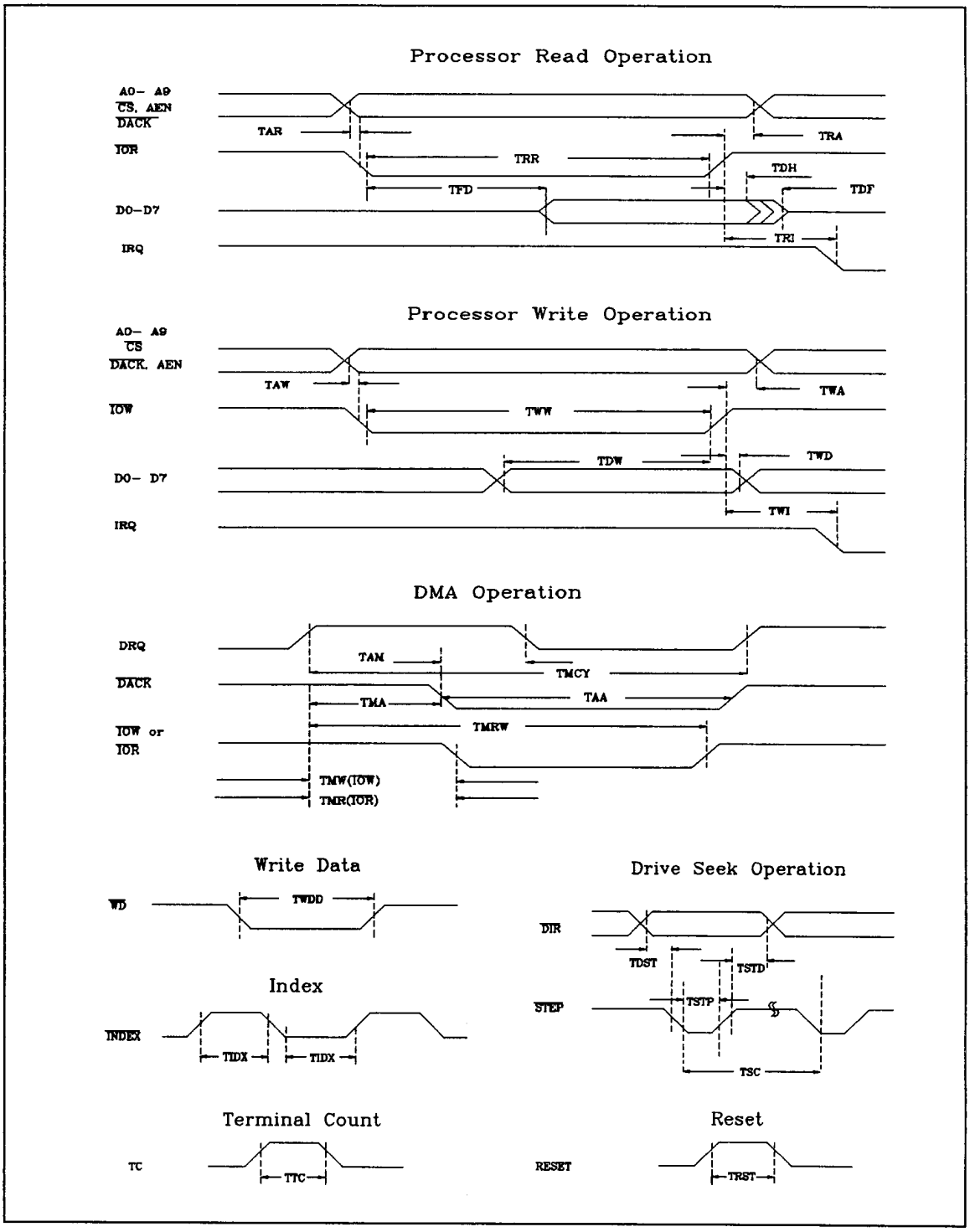
PARAMETER	SYMBOL	MIN.	MAX.	UNIT
SD hold time from $\overline{IOR}$, $\overline{IOW}$	t1	10		ns
SD hold time from $\overline{IOR}$, $\overline{IOW}$	t2	10	80	ns
$\overline{DBENL}$, $\overline{DBENH}$ delay from AEN, $\overline{IOCS16}$	t3		40	ns
$\overline{DBENL}$, $\overline{DBENH}$ delay from SA	t4		40	ns
$\overline{IDED7}$ to D7 delay (read cycle)	t5		60	ns
D7 to $\overline{IDED7}$ delay (write cycle)	t6		40	ns

D. UART/PRALLEL

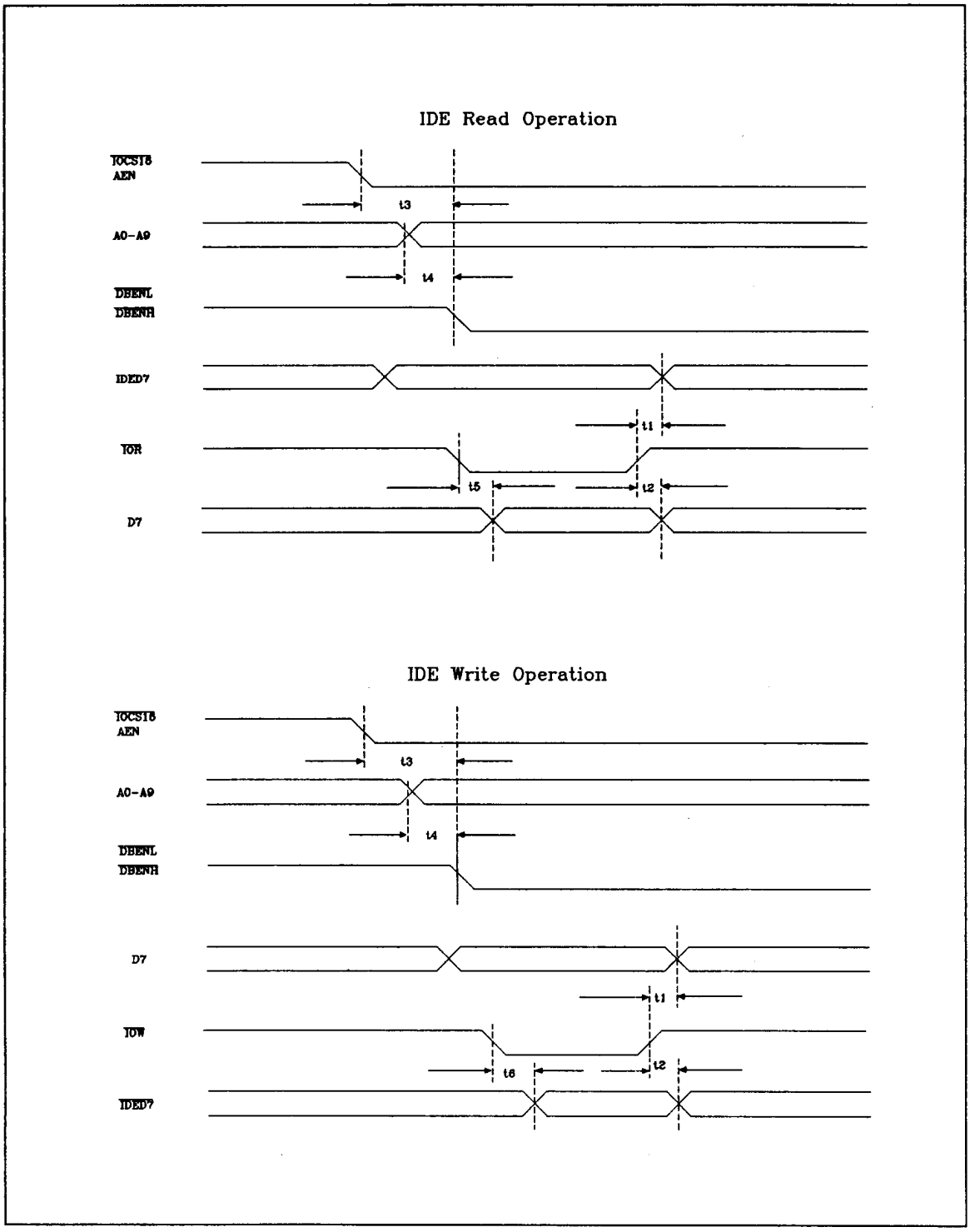
PARAMETER	SYMBOL	MIN.	MAX.	UNIT	TEST CONDITION
Delay from stop to set interrupt	T_{SINT}	9/16		Baud Rate	
Delay from $\overline{IOR}$ reset interrupt	T_{RINT}		1	μs	100pf Loading
Delay from initial IRQ reset to transmit start	T_{IRS}	1/16	8/16	Baud Rate	
Delay from $\overline{IOW}$ to reset interrupt	T_{HR}		175	ns	100pf Loading
Delay from initial $\overline{IOW}$ to interrupt	T_{SI}	9/16	16/16	Baud Rate	
Delay from Stop to Interrupt	T_{STI}		1/2	Baud Rate	
Delay from $\overline{IOR}$ to reset	T_{IR}		250	ns	100pf Loading
Delay from $\overline{IOW}$ to output	T_{MWO}		200	ns	100pf Loading
Set interrupt delay from MODEM input	T_{SIM}		250	ns	100pf Loading
Reset interrupt delay from $\overline{IOR}$	T_{RIM}		250	ns	
Interrupt active delay	T_{IAD}		30	ns	
Interrupt inactive delay	T_{IID}		30	ns	
Baud divisor	N		$2^{16}-1$		

TIMING DIAGRAMS

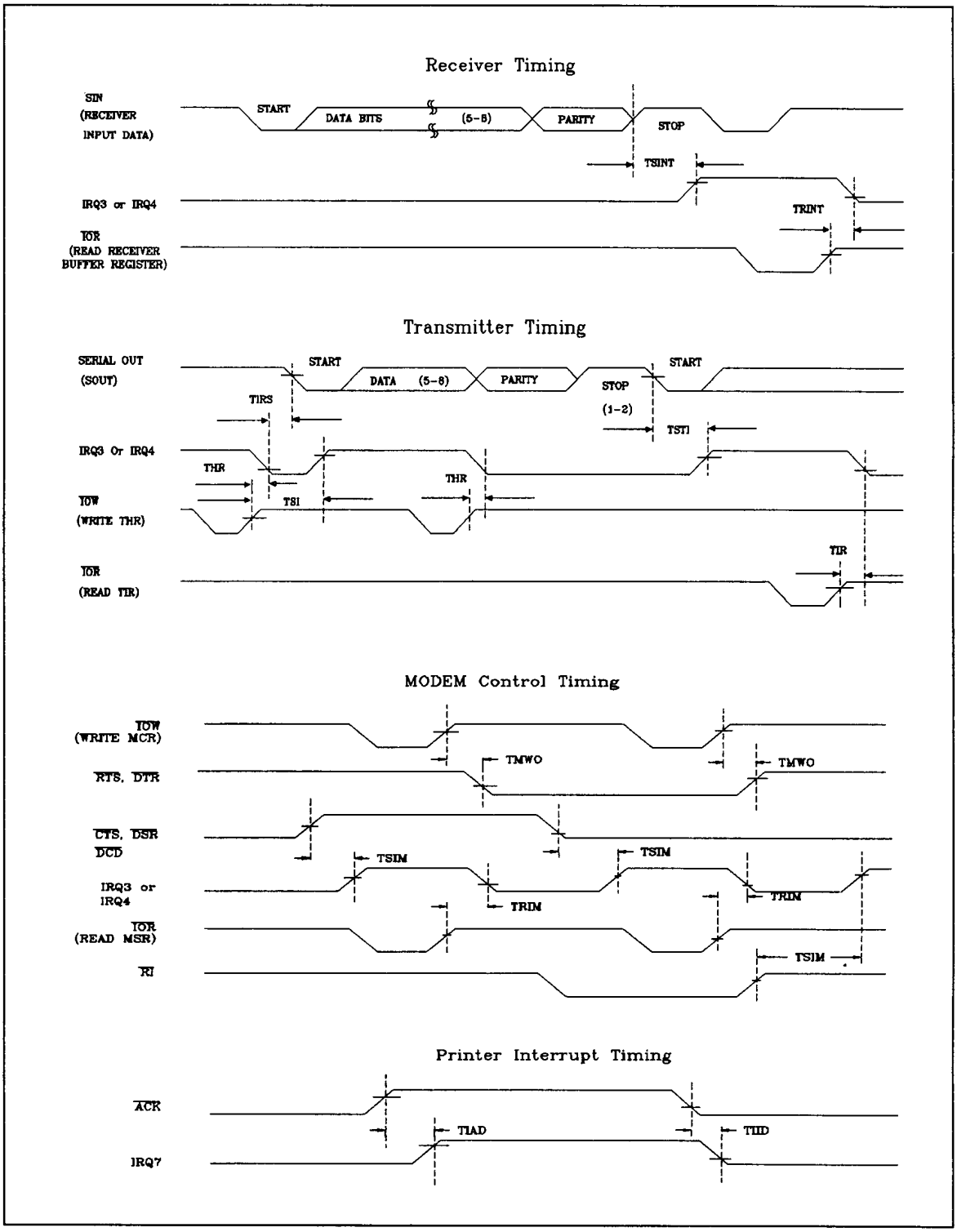
A. FDC



B. IDE Interface



C. UART/PARALLEL PORT



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