CMOS 4-BIT MICROCONTROLLER

TMP47C456AF

The 47C456A is a high speed and high performance 4-bit single chip microcomputer based on the TLCS-47 CMOS series. The 47C456A has LCD driver, DTMF generator and large-capacity RAM for repertory dial, which is suitable for application in telephones. The 47C456A has two oscillation circuits. It is possible to switch the operating mode ; high speed operation and low power consumption operation.

PART No.	ROM	RAM	PACKAGE	PIGGYBACK
TMP47C456AF	4096 x 8-bit	768 x 4-bit	QFP80	TMP47C956AG

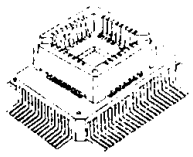
FEATURES

- ◆4-bit single chip microcomputer
- ◆Instruction execution time :
  8.3μs (at 960KHz), 244μs (at 32.8KHz)
- ◆Low voltage operation : 2.7V min.
- ◆90 basic instructions
- ◆Table look-up instructions
- ◆Subroutine nesting : 15 levels max.
- ◆6 interrupt sources (External : 2, Internal : 4)
  All sources have independent latches each, and multiple interrupt control is available.
- ◆I/O port (34 pins)
  - Input 1 port 4 pins
  - I/O 7 ports 27 pins
  - Output 1 port 3 pins
- ◆Interval Timer
- ◆Two 12-bit Timer/Counters
  Timer, event counter, and pulse width measurement mode
- ◆Watchdog Timer
- ◆Serial Interface with 4-bit buffer
  External/internal clock, and leading/trailing edge shift mode
- ◆LCD driver (automatic display)
  - LCD direct drive (Max.16-digit display at 1/4 duty LCD)
  - 1/4, 1/3, 1/2 duties or static drive are programmably selectable.
- ◆DTMF (Dual Tone Multi Frequency) output
  - DTMF output with one instruction
  - Single tone output function
- ◆RAM for repartry dial : 768 x 4-bit max.
- ◆BEEP output function
- ◆Dual-clock operation
  High-speed/Low-power-consumption operating mode
- ◆Real Time Emulator : BM47216A

QFP80

TMP47C456AF

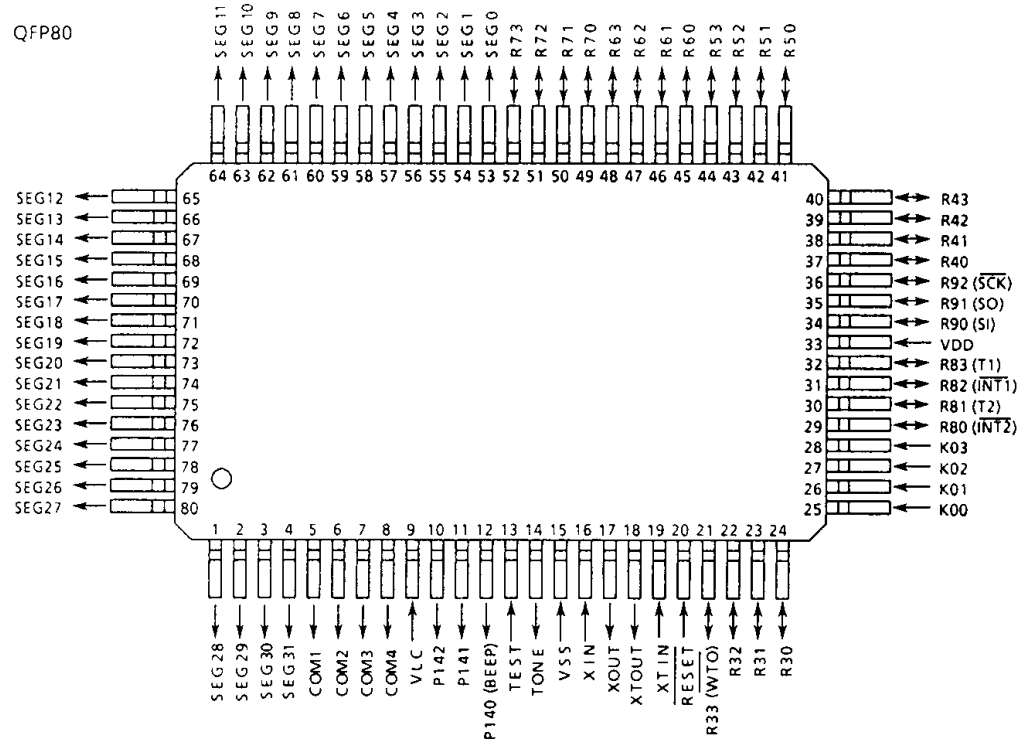
QFC80



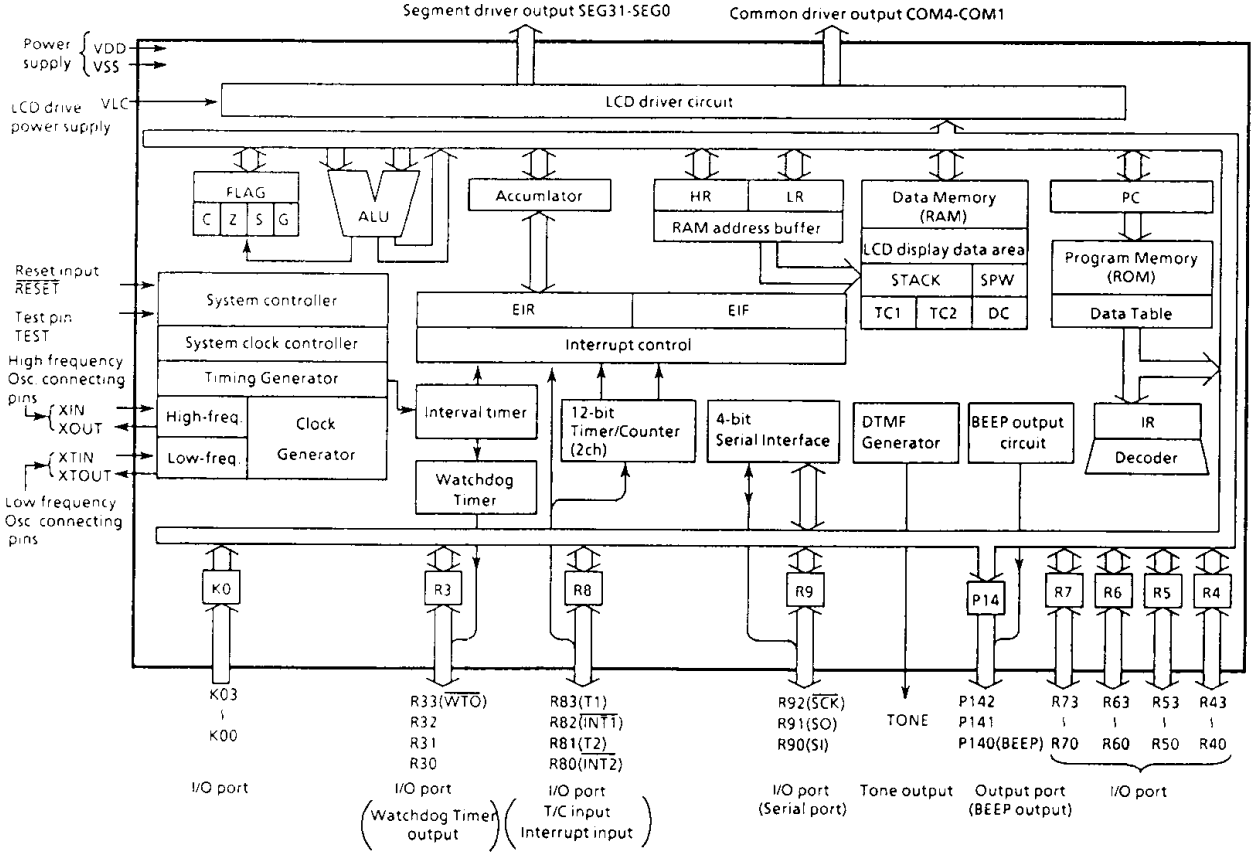
TMP47C956AG

PIN ASSIGNMENT (TOP VIEW)

QFP80



BLOCK DIAGRAM



PIN FUNCTION

PIN NAME	Input/Output	FUNCTIONS	
K03 - K00	Input	4-bit input port	
R33 ($\overline{WTO}$)	I/O (Output)	4-bit I/O port with latch. When used as the input port, the latch must be set to "1".	Watchdog timer output
R32 - R30	I/O		
R43 - R40	I/O	4-bit I/O port with latch. When used as the input port, the latch must be set to "1".	
R53 - R50			
R63 - R60			
R73 - R70			
R83 (T1)	I/O (Input)	4-bit I/O port with latch. When used as the input port, external interrupt input pin, or timer/counter input pin, the latch must be set to "1".	Timer/Counter 1 external input
R82 ($\overline{INT1}$)			External interrupt 1 input
R81 (T2)			Timer/Counter 2 external input
R80 ($\overline{INT2}$)			External interrupt 2 input
R92 (SCK)	I/O (I/O)	3-bit I/O port with latch. When used as the input port or serial port, the latch must be set to "1".	Serial clock I/O
R91 (SO)	I/O (Output)		Serial data output
R90 (SI)	I/O (Input)		Serial data input
P142 - P141	Output	3-bit I/O port with latch	
P140 (BEEP)	Output (Output)		BEEP output
SEG31 - SEG0	Output	LCD Segment driver output	
COM4 - COM1		LCD Common driver output	
TONE	Output	Tone output	
XIN	Input	Resonator connecting pins (High-frequency).	
XOUT	Output	For inputting external clock, XIN is used and XOUT is opened.	
XTIN	Input	Resonator connecting pins (Low-frequency).	
XTOUT	Output	For inputting external clock, XIN is used and XOUT is opened.	
$\overline{RESET}$	Input	Reset signal input	
TEST	Input	Test pin for shipping test. Be opened or fixed to low level.	
VDD	Power Supply	+ 2.7V to 6.0V	
VSS		0V (GND)	
VLC		LCD drive power supply	

OPERATIONAL DESCRIPTION

Concerning the 47C456A, the configuration and functions of hardwares are described. As the description has been provided with priority on those parts differing from the 47C400A, the technical data sheets for the 47C400A shall also be refered to.

1. SYSTEM CONFIGURATION

(1) Data Memory
(2) I/O port
(3) System Clock Controller
(4) Interval Timer
(5) Timer/Counter (TC1, TC2)
(6) Serial Interface
(7) LCD Driver
(8) DTMF Generator
(9) BEEP Output Circuit
(10) Watchdog Timer

2. INTERNAL CPU FUNCTION

2.1 Data Memory

The 47C456A data memory consists of a 768 x 4-bit RAM. First 256 x 4-bit RAM is the same as the data memory built into the 47C400A, so refer to the technical data sheets for the 47C400A for an explanation of the operation. Extended 512 x 4-bit RAM is mainly used for storing repertory dialing data and is controlled by the RAM address register, RAM data buffer register and TONE/RAM command register.

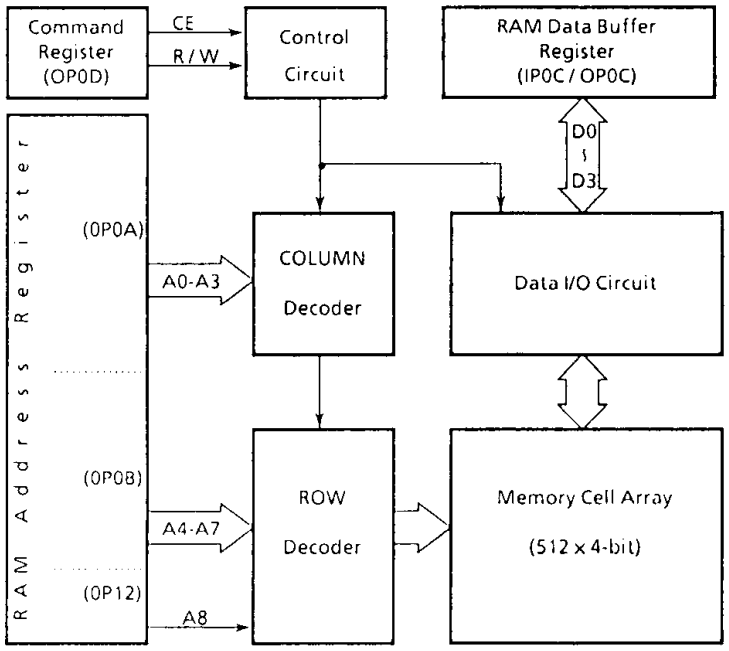


Figure 2-1. RAM Block Diagram

(1) RAM (512 x 4-bit) Address Register

The RAM address register is a 9-bit register to specify addresses for the RAM data memory. The upper 1 bit is accessed with port address OP12, the next 4 bits are accessed with the port address OP0B/IP0B and the lower 4 bits are accessed with port address OP0A/IP0A.

These registers are initialized to "0" during reset.

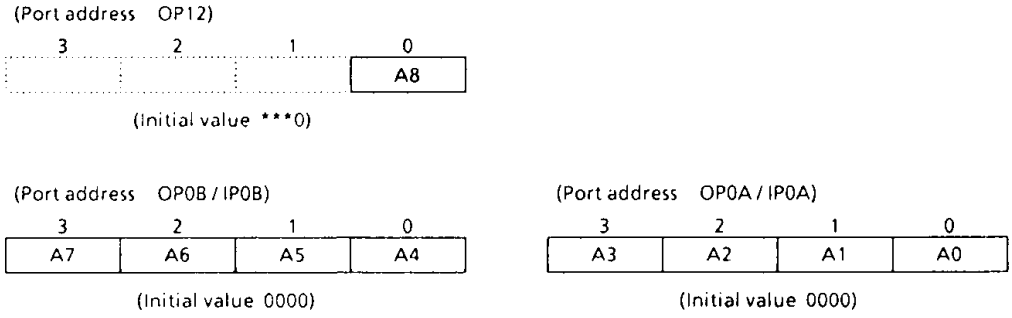


Figure 2-2. RAM Address Register

(2) RAM (512 x 4-bit) Data Buffer Register

The RAM data buffer register is a 4-bit buffer register to read or write RAM data. When writing data to RAM, it is accessed as port address OP0C. Port address IP0C is used for access when reading data from RAM.

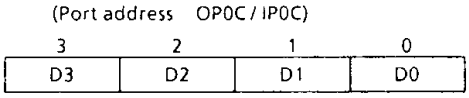
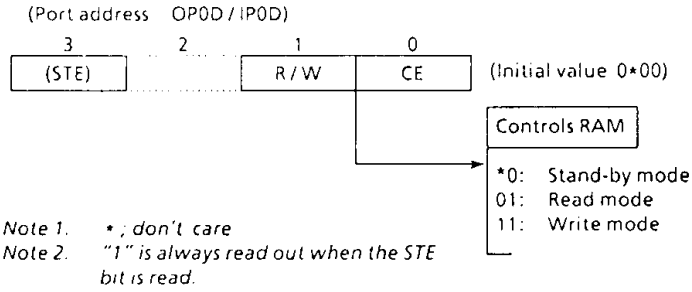


Figure 2-3. RAM Data Buffer Register

(3) RAM (512 x 4-bit) Command Register

The RAM command register (OP0D/IP0D) controls the reading or writing data, and whether RAM is to be accessed or put in stand-by mode. This register is accessed as the port address OP0D/IP0D. The RAM command register is also used as the TONE command register.



Note 1. *; don't care*

Note 2. *"1" is always read out when the STE bit is read.*

Figure 2-4. RAM Command Register

2.1.1 Access for RAM (512 × 4-bit)

To write data to RAM, load the address into the RAM address register and the data into the RAM data buffer register (OP0C) , then put the RAM command register in the write mode. The data will be written to the specified RAM address by this operation.

The data are latched in the RAM data buffer register, therefore, RAM data buffer register operation is not necessary when the same data are written continuously.

To read data from RAM, set the RAM command register to the read mode and load the address into the RAM address register, then read the data via RAM data buffer register (IP0C) . Data are not latched in the RAM data buffer register.

Example 1 : To write data "9" to address 182_H and data "7" to address $15A_H$ in RAM.

```
        LD      A,#1            ; Sets data "182H" to RAM address register.
        OUT     A,%OP12
        OUT     #8,%OP0B
        OUT     #2,%OP0A
        OUT     #9,%OP0C        ; Writes data "9" to RAM data buffer register.
        OUT     #0011B,%OP0D    ; Sets RAM to write mode.
        OUT     #0010B,%OP0D    ; Sets RAM to stand-by mode.
        OUT     #5,%OP0B        ; Sets data "15AH" to RAM address register.
        OUT     #0AH,%OP0A
        OUT     #7,%OP0C        ; Writes data "7" to RAM data buffer register.
        OUT     #0011B,%OP0D    ; Sets RAM to write mode.
        OUT     #0010B,%OP0D    ; Sets RAM to stand-by mode.
```

Example 2 : To write data "0" to address 120_H through 127_H in RAM.

```
        OUT     #0,%OP0C        ; Writes data "0" to RAM data buffer register.
        LD      A,#0            ; Sets data "120H" to RAM address register.
        OUT     #1,%OP12
        OUT     #2,%OP0B
        OUT     A,%OP0A
        OUT     #0011B,%OP0D    ; Sets RAM to write mode.
SLOOP : CMPR    A,#7            ; Increases address register.
        TESTP   ZF
        B       SWEND
        INC     A
        OUT     A,%OP0A
        BR      SLOOP
SWEND : OUT     #0010B,%OP0D    ; Sets RAM to stand-by mode.
```

Example 3 : To read data from address $0B1_H$ in RAM and store to Accumulator.

```
        OUT     #0001B,%OP0D    ; Sets RAM to read mode.
        LD      A,#0            ; Sets data "0B1H"to RAM address register
        OUT     A,%OP12
        OUT     #0BH,%OP0B
        OUT     #1,%OP0A
        IN      %IP0C,A         ; Reads data from RAM and stores to
                                  Accumulator.
```

3. PERIPHERAL HARDWARE FUNCTION

3.1 I/O Ports

The 47C456A has 9 ports (34 pins) each as follows :

①	K0	;	4-bit input
②	R3	;	4-bit input/output
③	R4, R5, R6, R7	;	4-bit input/output
④	R8	;	4-bit input/output (shared by external interrupt input and timer/counter input)
⑤	R9	;	3-bit input/output (shared by serial port)
⑥	P14	;	3-bit output (P140 is shared by BEEP output)

The port K0, R3 and P14 of the 47C456A differ from those of the 47C400A. The 47C456A does not have the port P1 and P2.

Table 3-1 lists the port address assignments and the I/O instructions that can access the ports.

(1) Port K0 (K03-K00)

The 4-bit input port with pull-up resistors.

Port K0 (Port address IP00)

3	2	1	0
K03	K02	K01	K00

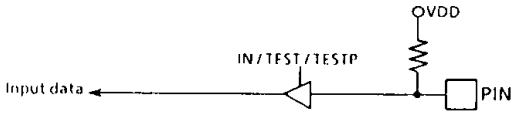


Figure 3-1. Port K0

(2) Port R3 (R33-R30)

The 4-bit I/O port with latch. When used as an input port, the latch must be set to "1". The latch is initialized to "1" during reset.

Port R3 (Port address OP03 / IP03)

3	2	1	0
R33	R32	R31	R30

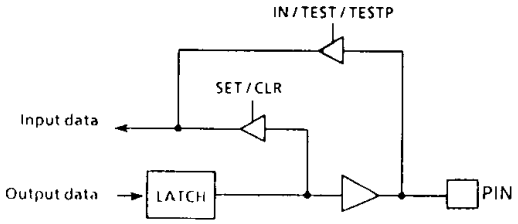


Figure 3-2. Port R3

(3) Port P14 (P142-P140)

The 3-bit output port with latch. The latch is initialized to "1" during reset. The pin P140 is shared by the BEEP output. When used as the BEEP output, the latch must be set to "1".

Port P14 (Port address OP14)

3	2	1	0
	P142	P141	P140 (BEEP)

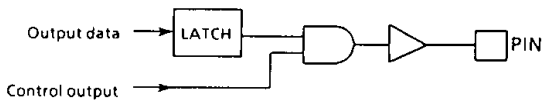


Figure 3-3. Port P14

Port address (**)	Port		Input/Output instruction						
	Input (IP**)	Output (OP**)	IN %p, A IN %p, @HL	OUT A, %p OUT@HL, %p	OUT #k, %p	OUTB @HL	SET %p, b CLR %p, b	TEST %p, b TESTP %p, b	SET @L CLR @L TEST @L
00_H	K0 input port	——	○	–	–	–	–	○	–
01	ROW register	ROW register	○	○	○	○ (Note2)	○	○	–
02	COLUMN register	COLUMN register	○	○	○		○	○	–
03	R3 input port	R3 output port	○	○	○	–	○	○	–
04	R4 input port	R4 output port	○	○	○	–	○	○	○
05	R5 input port	R5 output port	○	○	○	–	○	○	○
06	R6 input port	R6 output port	○	○	○	–	○	○	○
07	R7 input port	R7 output port	○	○	○	–	○	○	○
08	R8 input port	R8 output port	○	○	○	–	○	○	–
09	R9 input port	R9 output port	○	○	○	–	○	○	–
0A	RAM address register	RAM address register	○	○	○	–	○	○	–
0B	RAM address register	RAM address register	○	○	○	–	○	○	–
0C	RAM data buffer register	RAM data buffer register	○	○	○	–	○	○	–
0D	RAM command register	RAM command register	○	○	○	–	–	○	–
0E	SIO, SLOW operation status	——	○	–	–	–	–	○	–
0F	Serial receive buffer	Serial transfer buffer	○	○	○	–	–	–	–
10_H	Undefined	——	–	–	–	–	–	–	–
11	Undefined	——	–	–	–	–	–	–	–
12	Undefined	RAM address register	–	○	–	–	–	–	–
13	Undefined	BEEP output control	–	○	–	–	–	–	–
14	Undefined	P14 output port	–	○	–	–	–	–	–
15	Undefined	Watchdog Timer control	–	○	–	–	–	–	–
16	Undefined	System clock control	–	○	–	–	–	–	–
17	Undefined	——	–	–	–	–	–	–	–
18	Undefined	——	–	–	–	–	–	–	–
19	Undefined	Interval Timer interrupt control	–	○	–	–	–	–	–
1A	Undefined	——	–	–	–	–	–	–	–
1B	Undefined	LCD drive control	–	–	–	–	–	–	–
1C	Undefined	Timer/Counter 1 control	–	○	–	–	–	–	–
1D	Undefined	Timer/Counter 2 control	–	○	–	–	–	–	–
1E	Undefined	——	–	–	–	–	–	–	–
1F	Undefined	Serial interface control	–	○	–	–	–	–	–

Note 1. *"——" means the reserved state. Unavailable for the user program.*

Note 2. *The 5-bit to 8-bit data conversion instruction [OUTB @HL], automatic access to ROW register and COLUMN register.*

Table 3-1. Port Address Assignments and Available I/O Instructions

2.2 System Clock Controller

The 47C456A has two oscillation circuits with a high-frequency clock and a low-frequency clock. Power consumption can be decreased by switching to low-speed operation using the low-frequency clock when necessary (dual clock operation) . The high-frequency clock can be obtained by connecting an oscillator to the XIN and XOUT pins; the low-frequency clock can be obtained by connecting the oscillator to the XTIN and XOUT pins.

2.2.1 Circuit Configuration

Figure 2-4 shows the configuration of system clock controller.

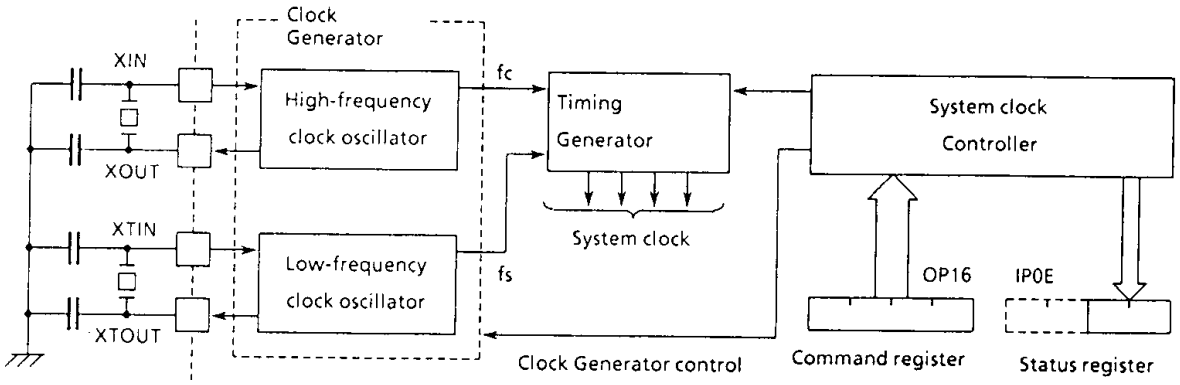


Figure 3-4. System Clock Controller

2.2.2 Dual Clock Operation Controller

Dual clock operation involves two modes : Normal operating mode using the high-frequency clock, and SLOW operating mode using the low-frequency clock. Both oscillators start operating when the power is turned on, after which the Normal operation is selected automatically. The high-frequency clock stops oscillating when a command is issued to switch to the SLOW operation. Operating mode switching is performed using the command register (OP16) . The status of the low-frequency clock and the current operating mode can be monitored using the status register (IPOE) . Figure 3-5 shows the operating mode transitions, and Figure 3-6 shows the command and status registers.

(1) Operating Mode Transmission

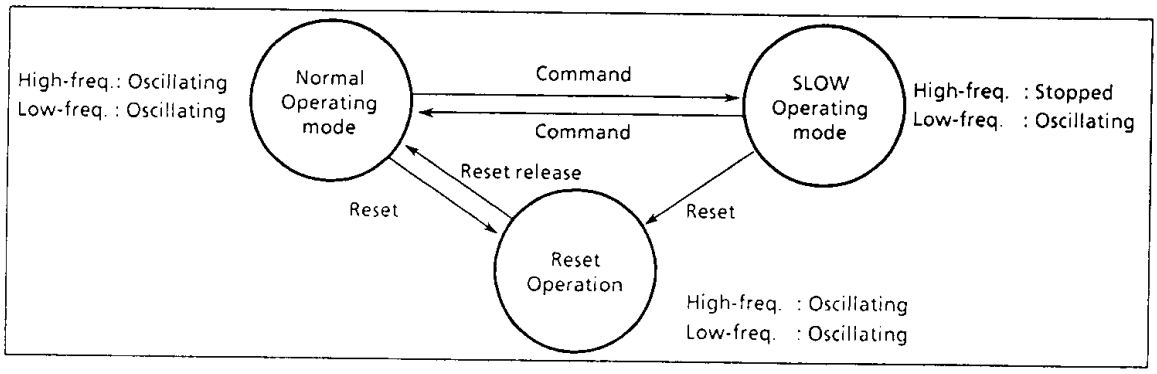


Figure 3-5. Operating Mode Transmission Diagram

(2) Operating Mode Control

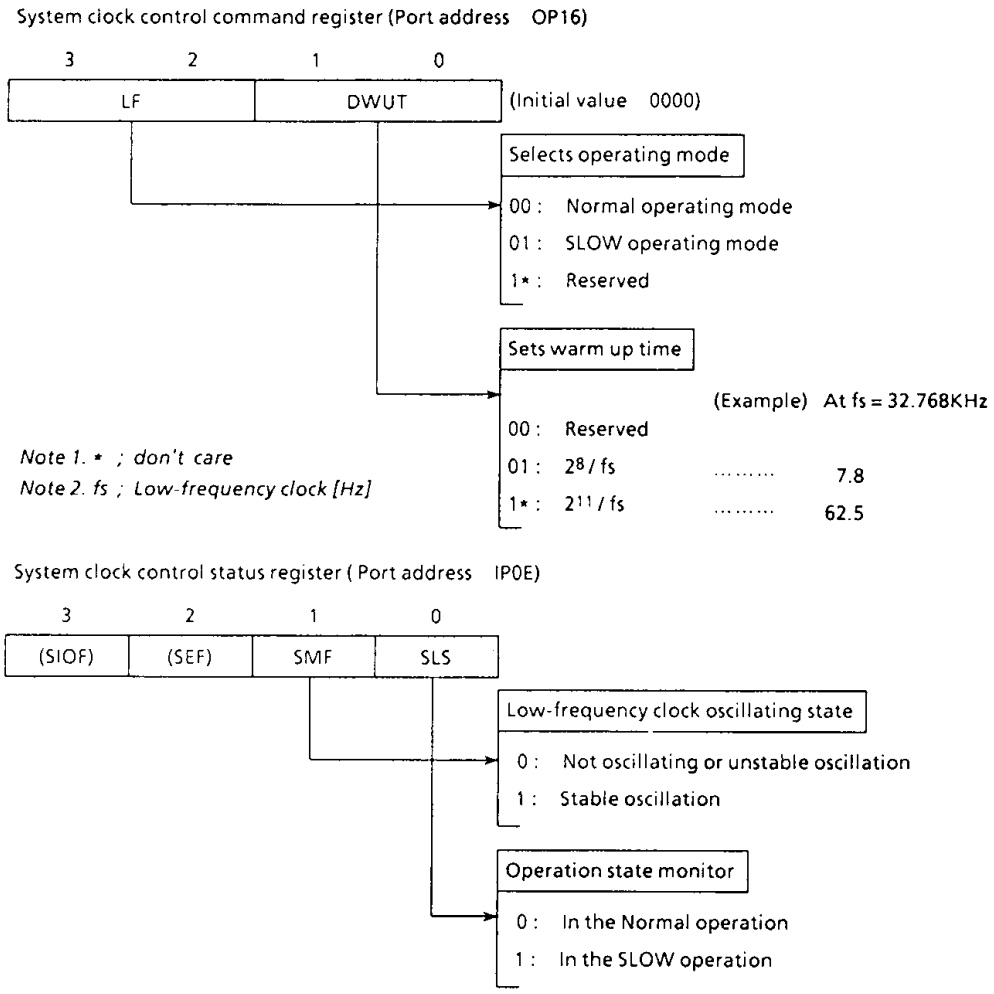


Figure 3-6. Command register and Status register

Note 1. The following operations and functions cannot be used in the SLOW operation ; therefore, this must be taken into consideration in programming.

① Timer/Counter 4096Hz (at fs = 32.8kHz) count operation (can be used with other count rates).

② Interval timer interrupt 4096Hz (at fs = 32.8kHz) operation (can be used with other timer rates).

③ Serial Interface

④ VFT drive circuit

Note 2. The power consumption of the oscillator and internal hardware is decreased in the SLOW operation, but power consumption through pin interfaces (dependent on the external circuitry and program) may prevent overall low power consumption operation ; therefore, caution is necessary during system design and interface circuit design.

(3) Operation mode switching

The following procedure is used to switch between the Normal operation and the SLOW operation. The Normal operation is selected during reset. Also, the current operating mode can be checked by monitoring SLS (status register bit 0).

a. Switching from Normal operation to SLOW operation

After monitoring SMF (status register bit 1) by program and confirming that the low-frequency clock is stable, set bit 2 of the command register to "1". The high-frequency clock will then stop. Also, after switching from Normal operation to SLOW operation (accessing the command register), execute the NOP (No Operation) instruction.

b. Returning from SLOW operation to Normal operation

When bit 2 of the command register is cleared to "0", the warm-up time must be set in DWUT. When the set warm-up time elapses, operation is switched to the Normal operation.

Example 1 : Normal operation → SLOW operation

```
SSMF:   TEST    %IP0E, 1        ; To wait until SMF goes to "1"
        B       SSMF
        LD      A, #0100B       ; Selects SLOW operating mode
        OUT     A, %OP16
        NOP                     ; No operation
        :
```

Example 2 : SLOW operation → Normal operation

```
        LD      A, #0001B       ; Selects Normal operation and sets warm-up
        OUT     A, %OP16          time (7.8ms)
        :
```

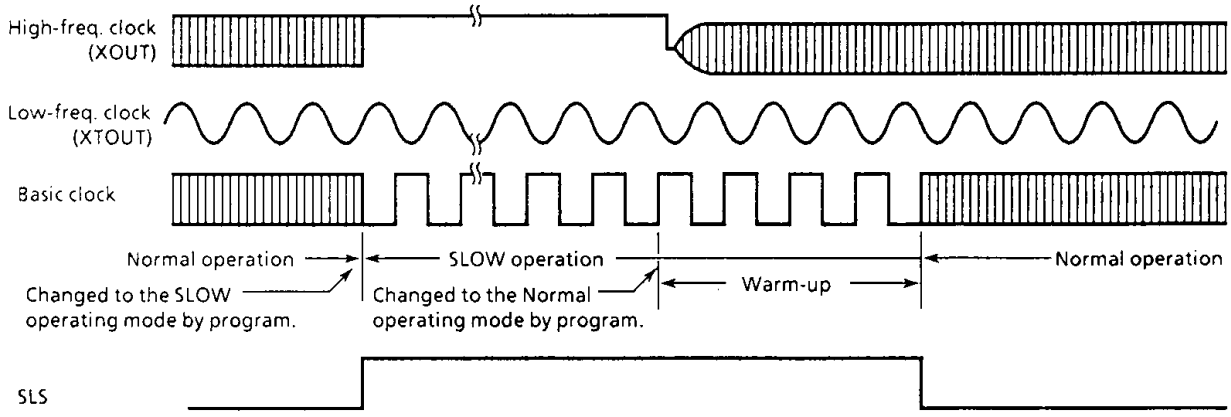


Figure 3-7. System Clock Switching Timing

3.3 Interval Timer

3.3.1 Configuration of Interval Timer

The interval timer is configured with a 15-stage binary counter and inputs the oscillation circuit output (fs) for the low-frequency clock; therefore, the final stage output is $fs/2^{15}$ [Hz]. This interval timer is cleared to "0" during reset.

Also, "fs" is input directly into the interval timer; therefore, the interval timer interrupts, timer/counter and LCD driver will not operate normally if the low-frequency oscillation is not stable.

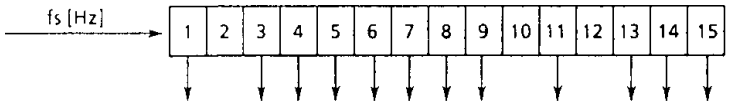


Figure 3-8. Interval Timer

3.3.2 Interval Timer Interrupt (ITMR)

Constant-frequency interrupts can be generated using the interval timer, Four different frequencies can be selected for interval timer interrupts using the command register (OP19). The command register is also initialized to "0" during reset.

An interval timer interrupt is generated at the first rising edge of the binary counters output after the command is set to the command register.

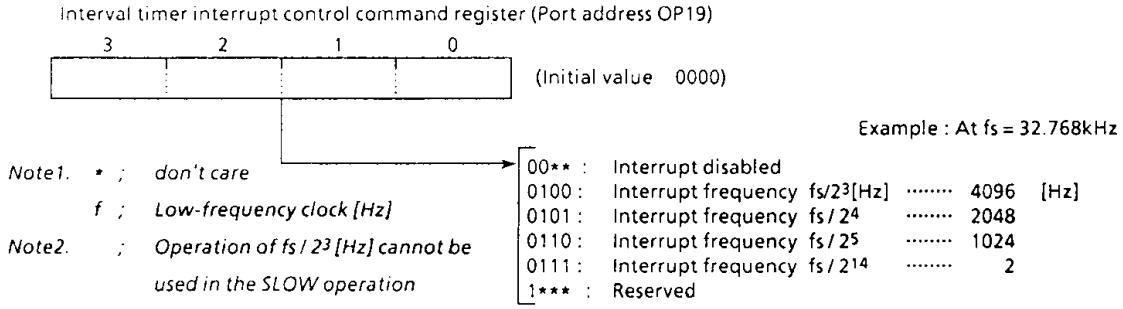


Figure 3-9. Command Register

3.4 Timer/Counter

The timer/Counter of the 47C456A is operated by a low-frequency clock (fs); therefore, the following operating frequencies differ from those of the 47C400A.

① Internal pulse rate.
② Maximum frequency applied in the event counter mode.
③ Drop ratio of instruction execution time when the timer is used.

(1) Internal pulse rate

The intrnal pulse rates shown in Table 3-2 can be selected by setting the values of the lower 2 bits of the TC1 and TC2 control command registers (OP1C, OP1D).

The values of lower 2 bits (bit1, 0)	Internal pulse rate	Max. setting time	At fs = 32.768KHz	
			Internal pulse rate	Max. setting time
00	$fs / 2^3$ [Hz]	$2^{15} / fs$ [sec]	4096 [Hz]	1 [sec]
01	$fs / 2^7$	$2^{19} / fs$	265	16
10	$fs / 2^{11}$	$2^{23} / fs$	16	256
11	$fs / 2^{15}$	$2^{27} / fs$	1	4096

Table 3-2. Internal Pulse Rate

(2) Maximum frequency applied in the event counter mode.

		Normal operating mode	SLOW operating mode
a. In 1-channel operation		fc / 32 [Hz]	fs / 32 [Hz]
b. In 2-channel operation	TC1	fc / 32	fs / 32
	TC2	fc / 40	fs / 40

(3) Drop ratio of instruction execution time when the timer is used.
With the 47C456A, count operation is inserted in the ratio of once per [(basic clock frequency) /2^3] / (internal pulse rate) instruction cycle; therefore, execution speed drops as follows:

$$100 \div \left\{ \frac{\text{(basic clock frequency)} / 2^3}{\text{(internal pulse rate)}} - 1 \right\} \%$$

Example 1: When fc = 960KHz and fs = 32.8kHz in the Normal operation and the internal pulse rate fs/2^3 is selected, count operation is inserted once per each cycle of 29 instructions; therefore, there is a drop of 100/28 = 3.57% for an instruction execution speed of 8.3μs.

Example 2: When fs = 32.8kHz in the SLOW operation, and the internal pulse rate fs/2^{11} is selected, count operation is inserted once per each cycle of 256 instructions; therefore, there is a drop of 0.39% for an instruction execution speed of 244μs. In addition, when the basic clock is obtained from "fs" (SLOW operation), count operation cannot be used with an internal pulse rate of fs/2^3.

3.5 Serial Interface

When operating using the internal clock, fs/2^2 [Hz] is used as the serial clock. Consequently, when operating at fs = 32.768kHz, the maximum transfer rate is 8192bit/sec. When the reading and writing of serial data cannot follow this clock rate, the serial clock is automatically stopped and the next shift operation stands by untill the processing is completed.
External clock can be used in the same way as for the 47C400A. The serial interface cannot be used in the SLOW operating mode.

3.6 LCD Driver

The 47C456A has circuit that directly drives the Liquid Crystal Display (LCD) and its control circuit.
The 47C456A has the following connecting pins with:

① Segment output 32 pins (SEG31 - SEG1)
② Common output 4 pins (COM4 - COM1)

In addition, VLC pin is provided as the drive power pin.

The devices that can be directly driven is selectable from LCD devices of following drive methods :

① 1 / 4 duty (1 / 3 bias) LCD ..... Max.128 segments (8 segments × 16 digits)
② 1 / 3 duty (1 / 3 bias) LCD ..... Max.96 segments (8 segments × 12 digits)
③ 1 / 2 duty(1 / 2 bias) LCD ..... Max.64 segments (8 segments × 8 digits)
④ Static LCD ..... Max.32 segments (8 segments × 4 digits)

2.6.1 Circuit Configuration

Figure 3-10 shows the configuration of the LCD driver.

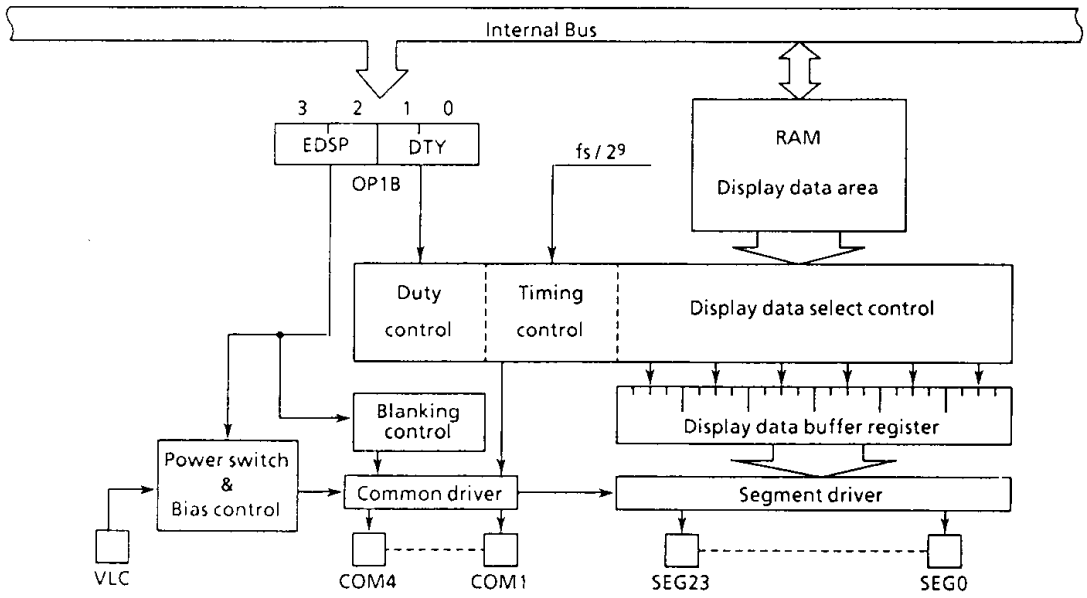


Figure 3-10. Configuration of LCD Driver

2.6.2 Control of LCD Driver

The LCD driver is controlled by the command register (OP1B).

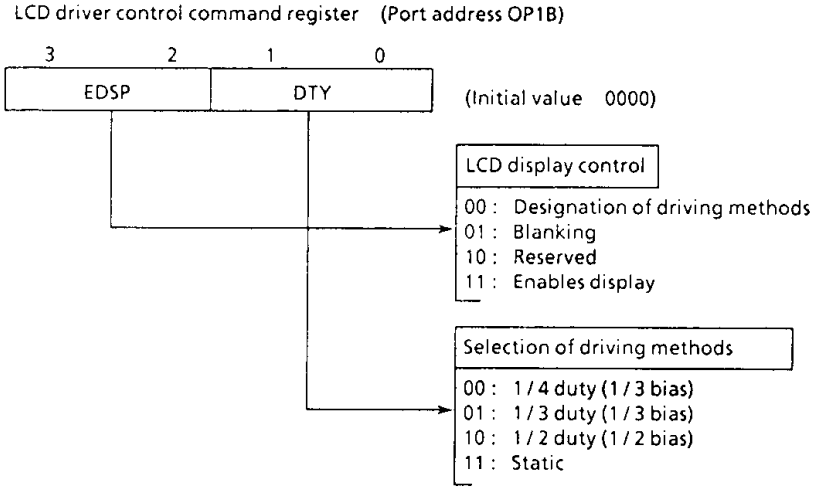
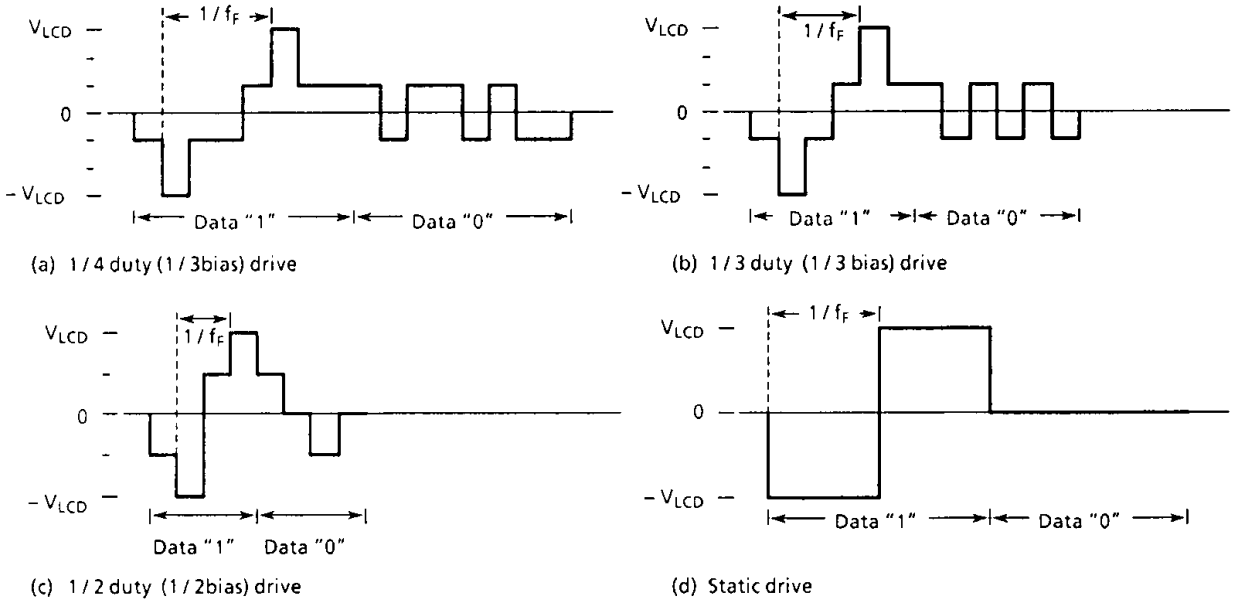


Figure 3-11. LCD Driver Control Command Register

(1) Driving methods of LCD

4 kinds of driving methods can be selected by DTY (bits 1 and 0 of command register).
Figure 3-12 shows driving waveforms for LCD.



Note. : f_F ; Frame frequency V_{LCD} ; LCD drive voltage (= V_{DD}–V_{LC})

Figure 3-12. Driving Waveform for LCD (Voltage between COM-SEG)

(2) Frame frequency

The frame frequency is set accoding to the driving method and base frequency as shown in Table 3-3.
The base frequency is given by the Interval Timer.

Base Frequency[Hz] \ Driving Method	Frame Frequency [Hz] 1/4duty	1/3duty	1/2duty	static
$\frac{fs}{2^9}$	$\frac{fs}{2^9}$	$\frac{4}{3} \cdot \frac{fs}{2^9}$	$\frac{4}{2} \cdot \frac{fs}{2^9}$	$\frac{fs}{2^9}$
At fs = 32.768KHz	64	85	128	64

fs ; Basic clock frequency [Hz]

Table 3-3. Frame Frequency Setting

(3) LCD drive voltage

The LCD drive voltage (V_{LCD}) is obtained from the difference in potential (V_{DD}-V_{LC}) between pins VDD and VLC. Thus, when the CPU operating voltage and LCD drive voltage are the same, the VLC pin is connected to the VSS pin.

The LCD light only when the difference in potential between the segment output and common output is $\pm V_{LCD}$, and turn off at all other times.

During reset, the power switch of the LCD driver is turned off automatically, shutting off the VLC voltage. Both the segment output and common output become V_{DD} level at this time and the LCD turn off.

The power switch is turned on to supply VLC voltage to the LCD driver by setting EDSP (bits 2 and 3 of the command register) to "11_B". After that, the power switch will not turn off even during blanking (setting EDSP to "01_B") and the VLC voltage continues to flow.

3.6.3 LCD Display Operation

(1) Display data setting

Display data are stored to the display data area (Max. 32 words) in the data memory.

The display data stored to the display data area are read automatically and sent to the LCD driver by the hardware.

The LCD driver generates the segment signals and common signals in accordance with the display data and drive method. Thus, display patterns can be changed by merely overwriting the contents of the display data area with a program. The table look-up instruction is mainly used for this overwriting.

Figure 3-13 shows the correspondence between the display data area and the SEG/COM pins. The LCD light when the display data is "1" and turn off when "0".

The number of segment which can be driven differs depending on the LCD drive method; therefore, the number of display data area bits used to store the data also differs (Refer to Table 3-4). Consequently, data memory not used to store display data and data memory for which the addresses are not connected to LCD can be used to store ordinary user's processing data.

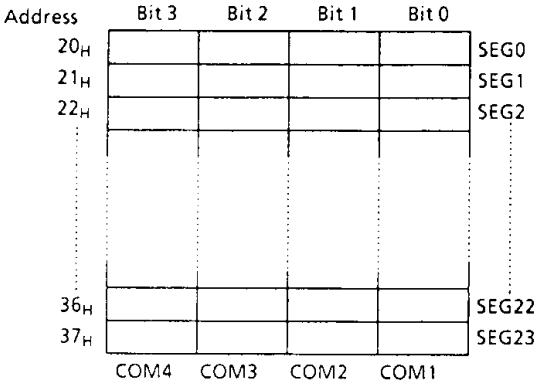


Figure 3-13. Display Data Area and SEG/COM

Driving Method	Bit 3	Bit 2	Bit 1	Bit 0
1 / 4 duty	COM4	COM3	COM2	COM1
1 / 3 duty	–	COM3	COM2	COM1
1 / 2 duty	–	–	COM2	COM1
Static	–	–	–	COM1

Note. – ; This bit is not used for display data.

Table 3-4. Driving Method and Bit for Display Data

(2) Blanking

Blanking is applied by setting EDSP to "01_B" and turns off the LCD by outputting the non light operation level to the COM pin. The SEG pin continuously outputs the signal level in accordance with the display data and drive method.

At static drive, no voltage is applied between the COM and SEG pins when the LCD is turned off by data (display data cleared to "0"), but the COM pin output becomes constant at the $V_{LCD}/2$ level when turning off the LCD by blanking, so the COM and SEG pins are then driven by $V_{LCD}/2$.

3.6.4 Control Method of LCD Driver

(1) Initial Setting

Flow chart of initial setting is shown in Figure 3-14.

Example : Driving of 1 / 4duty LCD

```
        LD      A, #0000B   ; Sets 1/4 duty drive
        OUT     A, %0P1B
        :                   ; Initializes display data area
        :
        LD      A, #1100B   ; Enable display (Relese of blanking)
        OUT     A, %0P1B
        :
```

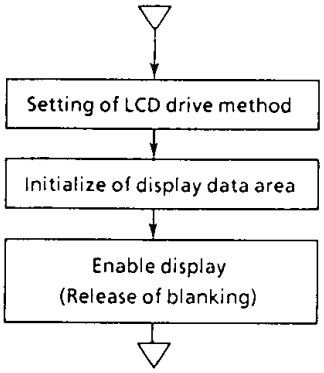


Figure 3-14. Initial Setting of LCD Driver

(2) Display Data

Normally, display data are kept permanently in the program memory and are then stored to the display data area by the table look-up instruction. This can be explained using numerical display with 1/4 duty LCD as an example. The COM and SEG connections to the LCD are the same as those shown in Figure 3-15 and the display data are as shown in Table 3-5.

Programming example for displaying numerals corresponding to BCD data stored at address 10_H in the data memory is shown below. The display data area is at addresses 20_H and 21_H.

```
        LD      HL, #0FCH              ; Sets the data counter
        LD      A, 10H
        ST      A, @HL+
        ST      #DTBL/16 ,@HL+
        ST      #DTBL/256,@HL+
        LD      HL,#20H                ; Stores display data
        LDL     A, @DC
        ST      A, @HL+
        LDH     A, @DC+
        ST      A, @HL+
         :
DTBL : DATA     11011111B, 00000110B, 11100011B, 10100111B, 00110110B,
                10110101B, 11110101B, 00010111B, 11110111B, 10110111B
```

Numeral	Display	Display data		Numeral	Display	Display data	
		Upper	Lower			Upper	Lower
0	0.	1101	1111	5	5	1011	0101
1	1	0000	0110	6	6	1111	0101
2	2	1110	0011	7	7	0001	0111
3	3	1010	0111	8	8	1111	0111
4	4	0011	0110	9	9	1011	0111

Table 3-5. Example of Display Data (1/4 Duty)

Table 3-6 shows the same numerical display used in Table 3-5, but using 1/2 duty LCD. The connections of the COM and SEG pins to the LCD are the same as those shown in Figure 3-17.
Programming example for displaying numerals corresponding to BCD data stored at address 10_H in the data memory is shown below. The display data area is at addresses 20 through 23_H.

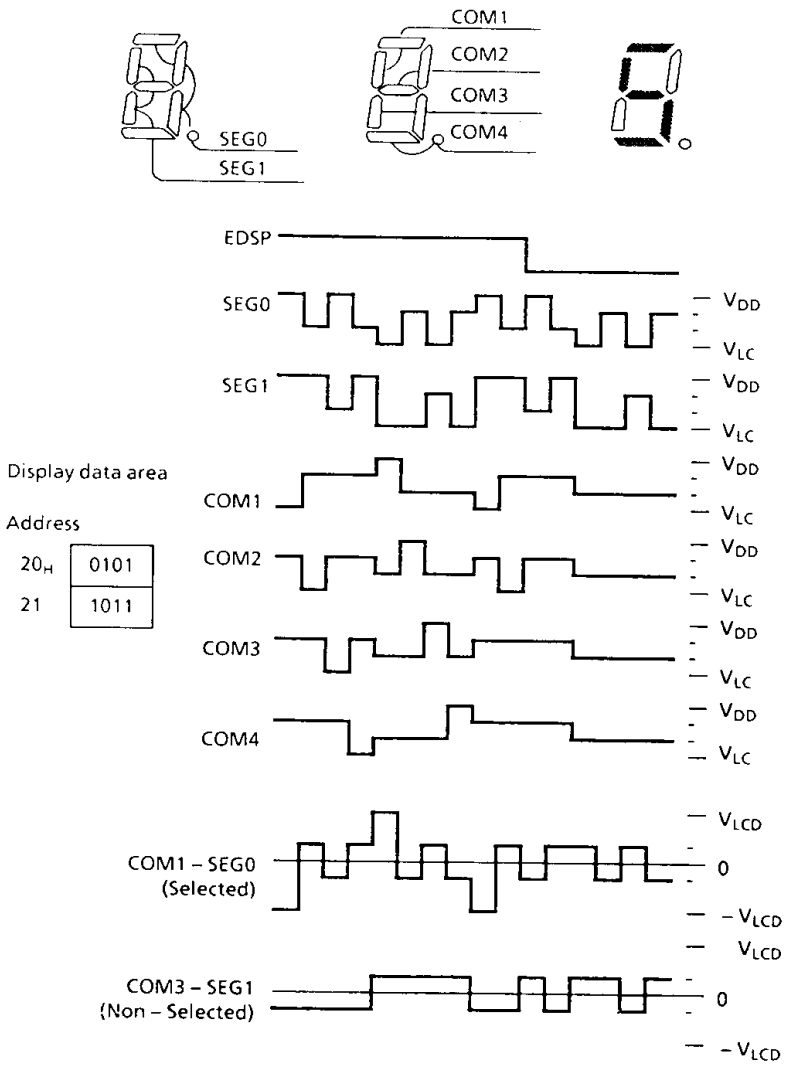
```
        LD      HL, 0FCH            ; Sets the data counter
        LD      A, 10H
        ST      A, @HL+
        ST      #DTBL/16, @HL+
        ST      #DTBL/256, @HL+
        LD      HL, #20H            ; Stores display data
        LDL     A, @DC
        ST      A, @HL+
        RORC    A
        RORC    A
        ST      A, @HL+
        LDH     A, @DC+
        ST      A, @HL+
        RORC    A
        RORC    A
        ST      A, @HL+
         :
DTBL :  DATA    01110111B, 00100010B, 10010111B, 10100111B, 11100010B,
                11100101B, 11110101B, 01100011B, 11110111B, 11100111B
```

Numeral	Display data				Numeral	Display data			
	Upper		Lower			Upper		Lower	
0	**01	**11	**01	**11	5	**11	**10	**01	**01
1	**00	**10	**00	**10	6	**11	**11	**01	**01
2	**10	**10	**01	**11	7	**01	**10	**00	**11
3	**10	**01	**01	**11	8	**11	**11	**01	**11
4	**11	**10	**00	**10	9	**11	**10	**01	**11

*Note. * ; don't care*

Table 3-6. Example of Display Data (1/2 Duty)

(3) Driving Example

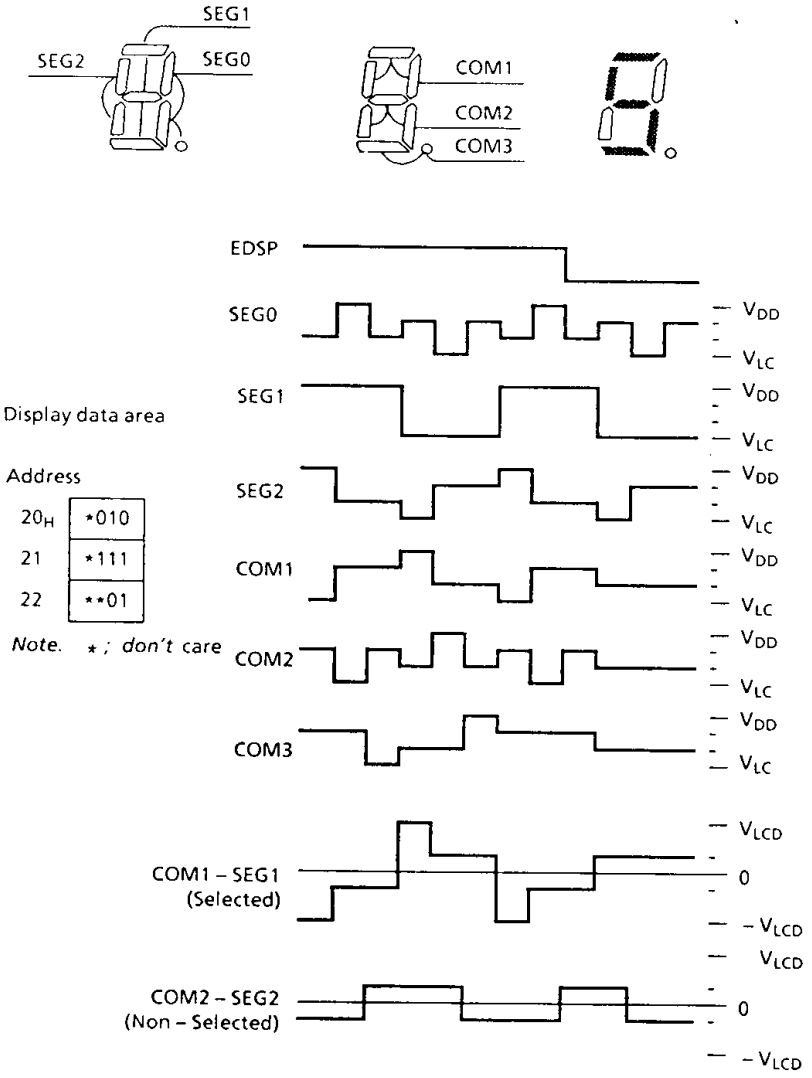


Display data area

Address

20_H	0101
21	1011

Figure 3-15. 1/4 Duty (1/3 Bias) Drive



Display data area

Address

20_H	*010
21	*111
22	**01

Note. *; *don't care*

Figure 3-16. 1/3 Duty (1/3 Bias) Drive

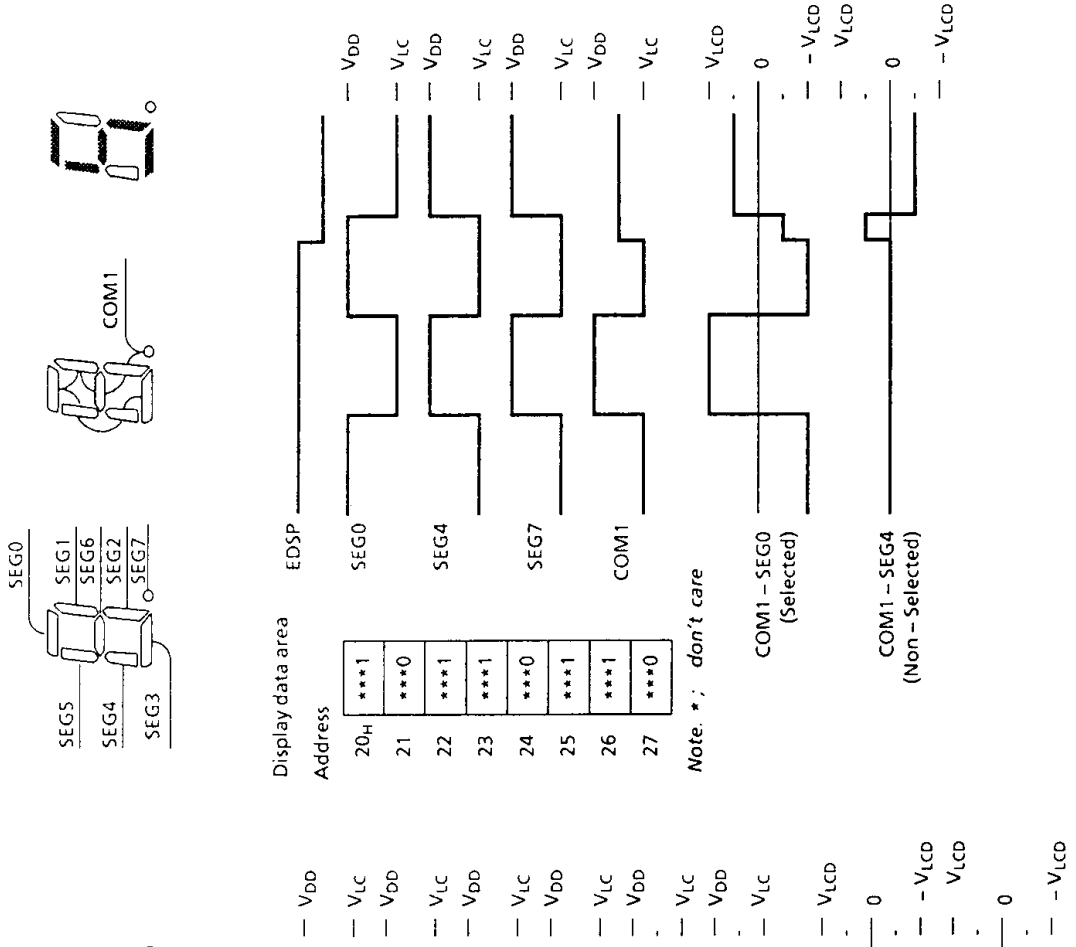


Figure 3-17. 1/2 Duty (1/2 Bias) Drive

Figure 3-18. Static Drive

3.7 DTMF Generator

The 47C456A has a DTMF (Dual Tone Multi Frequency) generator which generates dialing signals for tone dialing type telephones. There are two groups of tone dial signals, one group of 4 sine wave low frequencies and another group of 4 sine wave high frequencies. All of these frequencies can be selected individually and combined with a frequency from the other group for a total of 16 different DTMF composite waves.

3.7.1 Configuration of DTMF Generator

Figure 3-19 shows configuration of the DTMF generator . The 47C456A generates two stepped, quasi sine waves for tone dial signals which can be combined and output. The high or low group of frequencies is selected by setting frequency selection codes into the ROW and COLUMN registers.

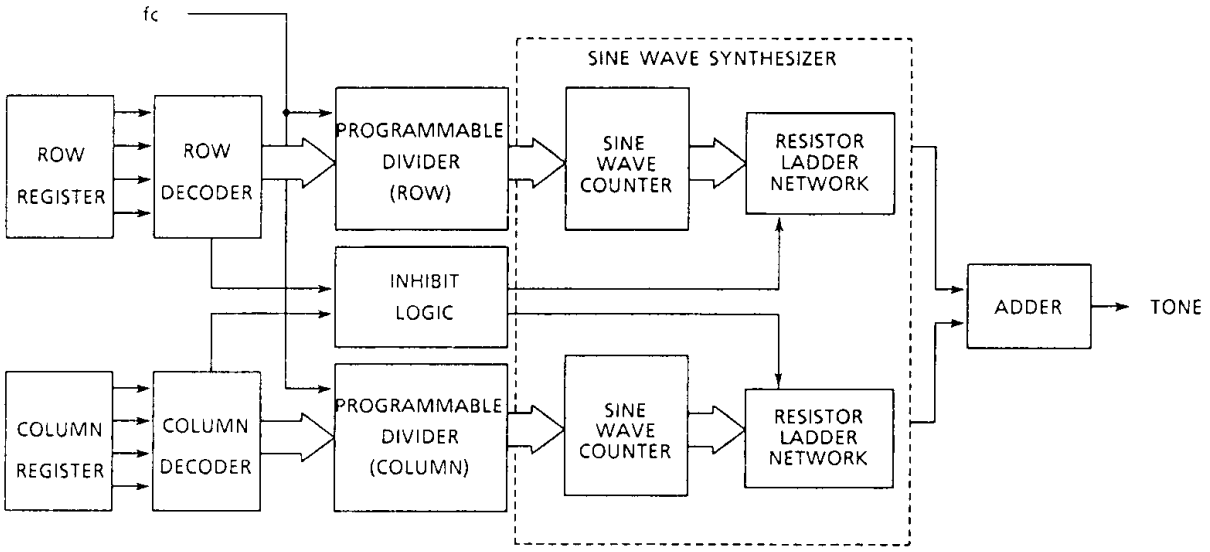


Figure 3-19. Configuration of DTMF Generator

3.7.2 Control of DTMF Generator

Tone output is controlled by ROW register (OP01/IP01) and COLUMN register (OP02/IP02) . And single tone is controlled by TONE command register (OP0D/IP0D) . ROW register, COLUMN register and TONE command register are initialized to "0" during reset.

TONE command register (Port address OP0D/IP0D)

3	2	1	0	
STE		(R/W)	(CE)	(Initial value 0*00)

Controls single tone output

0 : Disable mode of single tone output
1 : Enable mode of single tone output

Note 1. *; don't care*
Note 2. *When read STE bit, "1" is always read.*

Figure 3-20. TONE command register

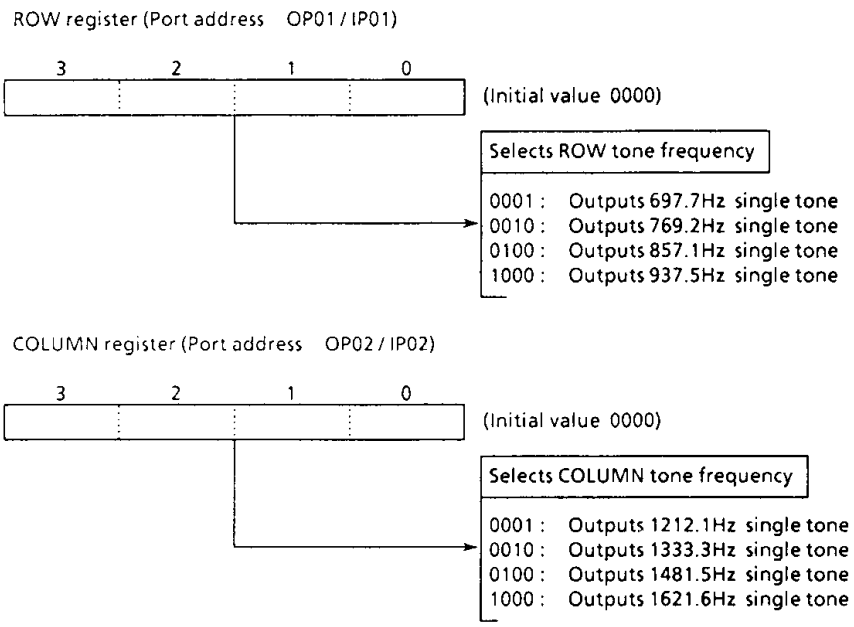


Figure 3-21. ROW, COLUMN Register

Tones are outputted by loading the frequency selection codes shown in Figure 3-21 into the ROW and COLUMN registers. In the enable mode of single tone output and either ROW or COLUMN register is disabled, another register remains to be enabled, and so single tone can be outputted, by loading an ineffective code into the register. When both the registers are enabled, dual tone can be outputted. In the disable mode of single tone output, effective codes are loaded into both ROW and COLUMN registers and then dual tone can be outputted. At this time, an ineffective code is loaded into ROW or COLUMN register and then the 47C456A has no tone output signal.
The [OUTB @HL] instruction can set 8-bit data into both registers (the upper 4 bits of the ROM data go to the COLUMN register and the lower 4 bits go to the ROW register) at the same time, and DTMF signal is outputted without single tone output.

Example 1 : To output 1481.5Hz single tone

```
OUT     #8,%OP0D ;  Sets the enable mode of single tone output.
OUT     #0,%OP01 ;  Sets an ineffective code into ROW register.
OUT     #4,%OP02 ;  Sets data "4" into COLUMN register
```

Example 2 : 8 bits data corresponding to the 5 bits of data linking the content of carry flag and the contents of data memory RAM address 90_H are read from the ROM, frequency selection codes are loaded into ROW and COLUMN registers, and dual tone is outputted.

```
LD      HL,#90H  ;  HL←90H (Sets the address of the data memory)
OUTB    @HL      ;  Sets the ROM data into the ROW and COLUMN register.
```

Table 3-7 shows the corresponding frequency selection codes of the ROW and COLUMN registers for the telephone dial keys. Table 3-8 shows the deviation between the 47C456A tone output frequency and standard frequency.

		COLUMN register (OP02 / IP02)		
	Frequency selection code	0001 (1209)	0010 (1336)	0100 (1477)
ROW register (OP01/IP01)	0001 (697)	1	2	3
	0010 (770)	4	5	6
	0100 (852)	7	8	9
	1000 (941)	*	0	#
		Standard telephone dial key		

Contents of ( ) are standard frequencies, unit : Hz

Table 3-7. Corresponding frequency selection codes of the ROW and COLUMN registers for the telephone dial keys

ROW Tone						
Frequency selection code				Tone output frequency [Hz]	Standard frequency [Hz]	Deviation [%]
3	2	1	0			
0	0	0	1	697.7	697	+ 0.10
0	0	1	0	769.2	770	- 0.10
0	1	0	0	857.1	852	+ 0.60
1	0	0	0	937.5	941	- 0.37

COLUMN Tone						
Frequency selection code				Tone output frequency [Hz]	Standard frequency [Hz]	Deviation [%]
3	2	1	0			
0	0	0	1	1212.1	1209	+ 0.26
0	0	1	0	1333.3	1336	- 0.20
0	1	0	0	1481.5	1477	+ 0.30
1	0	0	0	1621.6	1633	- 0.70

Table 3-8. Tone output frequencies and Deviation from standard of 47C456A

3.7.3 Test mode for tone output

The 47C456A includes a test mode for checking tone output waveforms. Tones can be outputted by the circuit shown in Figure 3-22. ROW data are inputted from the port R6 and COLUMN data are inputted from the port R3, and any desired single or dual tones can be outputted by setting the frequency selection codes shown in Figure 3-21. Figure 3-23 shows a single tone waveform and Figure 3-24 shows a dual tone waveform.

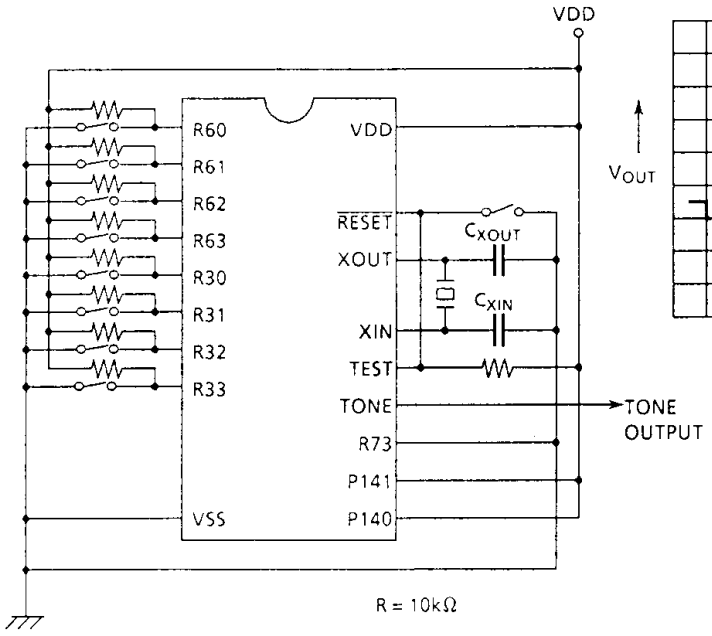


Figure 3-22. Tone test circuit

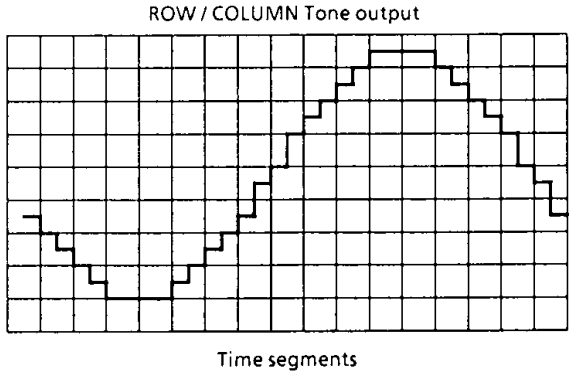


Figure 3-23. Single tone waveform

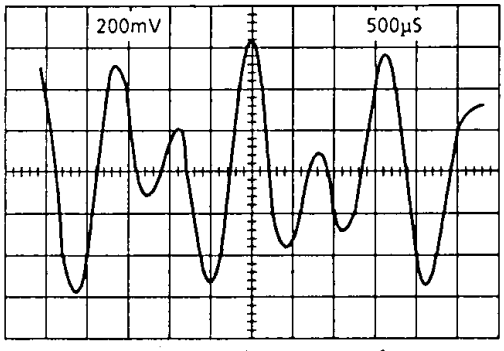


Figure 3-24. Dual tone waveform

3.8 BEEP Output Circuit

BEEP output circuit generates square wave in the audible frequency range. This circuit can drive the key input confirmation tone generator circuit for telephone applications.

BEEP output is from the P140 (BEEP) pin. This pin is for both P140 output and BEEP output. Set the P140 output latch to "1" for BEEP output.

3.8.1 BEEP Output Circuit Configuration

Figure 3-25 shows the BEEP output circuit configuration. The clock pulse of BEEP output circuit is supplied by an interval timer. BEEP output is controlled by frequency selection and output enable/disable setting.

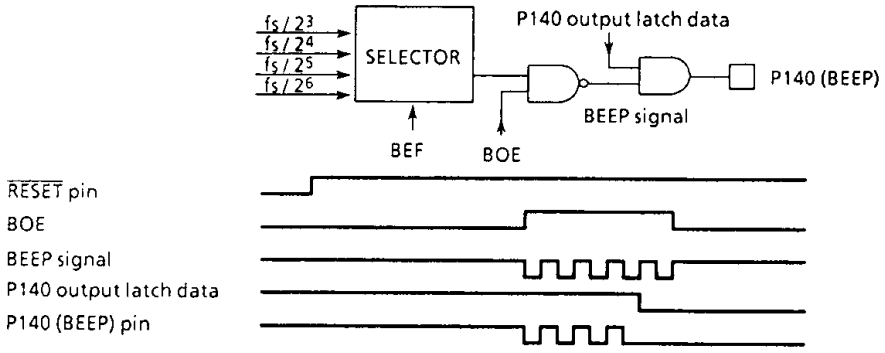


Figure 3-25. BEEP Output Circuit Configuration and Timing Chart

3.8.2 Control of BEEP Output

BEEP output is controlled by the command register (OP13).

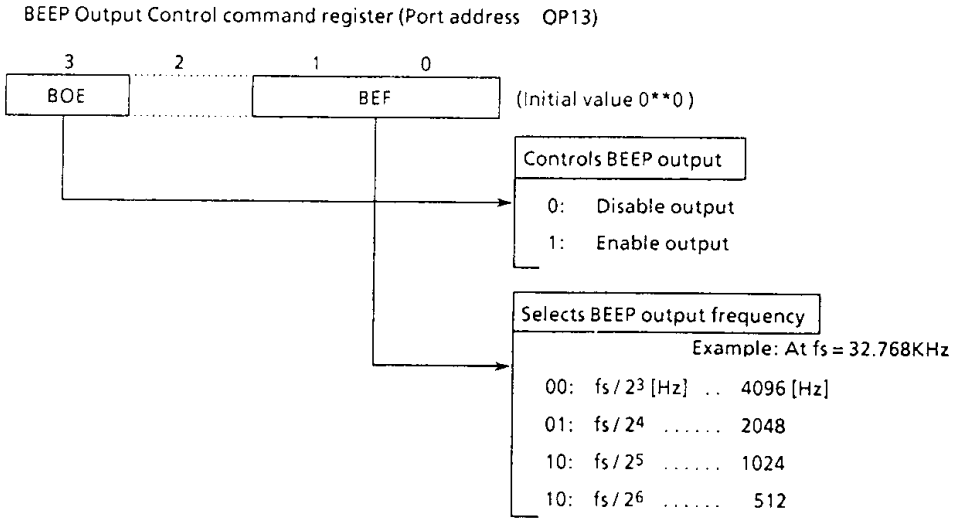


Figure 3-26. BEEP Output Control Command Register

3.9 Watchdog Timer (WDT)

The purpose of the watchdog timer is detect the malfunction (runaway) of program due to external noise or other causes and return the operation to the normal condition. The watchdog timer output is output to R33 ($\overline{WTO}$) pin.

When the watchdog timer is used, the output latch of R33 must be set to "1". Further, during reset, the output latch of R33 is set to "1", and the watchdog timer becomes disable sate. The initialization at time of runaway will become possible when the $\overline{WTO}$ pin and $\overline{RESET}$ pin are connected each other.

3.9.1 Configuration of Watchdog Timer

The watchdog timer consists of 10-stage binary counter, flip-flop (F/F), and its control circuit. The F/F is set to."1" during reset, and cleared to "0" at the rising edge of the binary counter output.

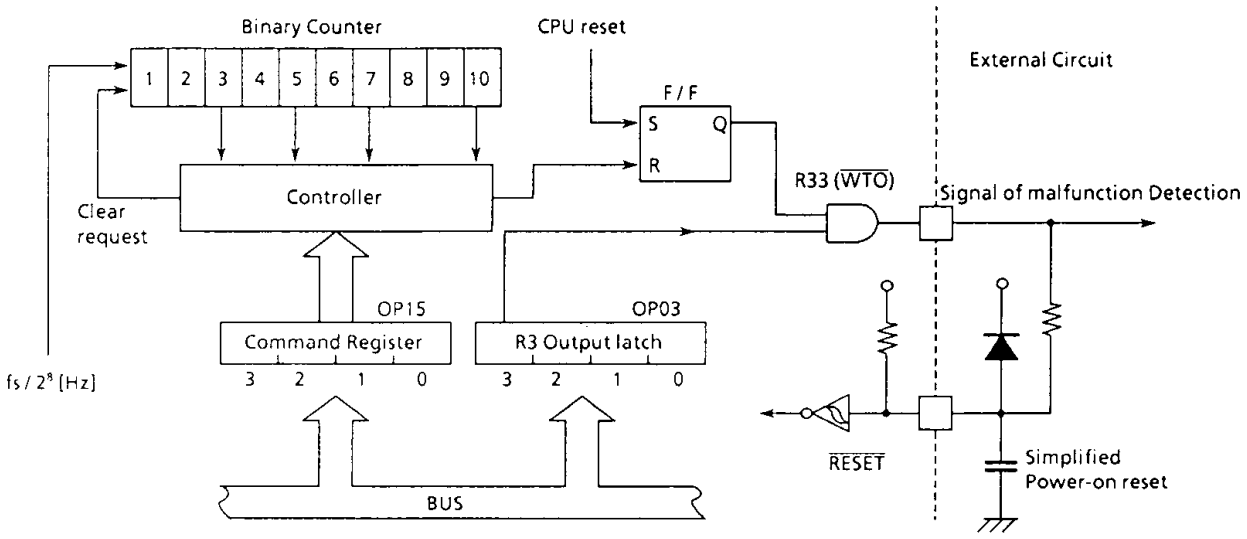


Figure 3-27. Configuration of Watchdog Timer

3.9.2 Control of Watchdog Timer

The watchdog timer is controlled by the command register (OP15). This command register is initialized to "1000_B" during reset. The following are procedure to detect the malfunction (runaway) of CPU by the watchdog timer.

① At first, detection time of the watchdog timer should be set and binary counter should be cleared.

② The watchdog timer should be become enable

③ Binary counter must be cleared before the detection time of the watchdog timer. When the malfunction of CPU is taken place for some reason and binary counter is not cleared, the F/F is cleared to '0" at the rising edge of the binary counter and signal of malfunction detection is become active ($\overline{WTO}$ output is "L").

Note. It is necessary to clear the binary counter prior to enabling watchdog timer.
Further, when switching the system clock, it is necessary to halt the watchdog timer during the warm-up time at changing from the SLOW operating mode the Normal operating mode.

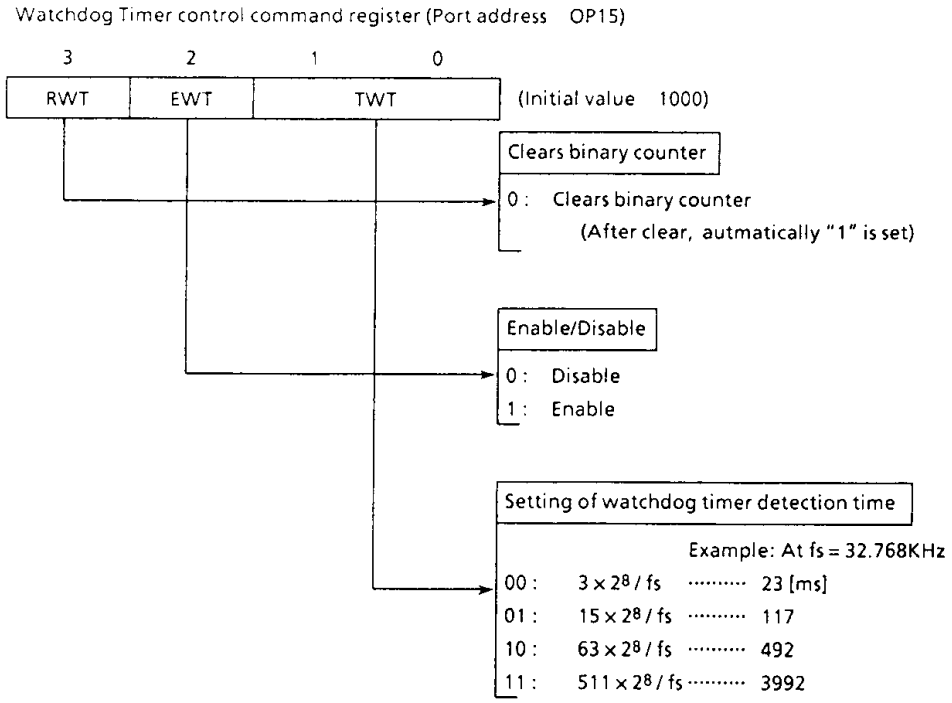


Figure 3-28. Command Register

Example : To set to the watchdog detection time ($63 \times 2^8 / fs$ [sec]). And to enable the watchdog timer.

```
        LD      A, #0010B       ; OP15 ← 0010B
                                  (Sets WDT detection time. Clears binary
                                  counter.)
        OUT     A, %OP15
        LD      A, #1110B       ; OP15 ← 1110B (Enables WDT)
        OUT     A, %OP15
        :
        :
        :
        LD      A, #0110B
        OUT     A, %OP15        ; OP15 ← 0110B (Clears binary counter)
        :
        :
```

Within WDT detection time

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

PARAMETER	SYMBOL	PINS	RATING	UNIT
Supply Voltage	V_{DD}		− 0.5 to 7	V
Supply Voltage (LCD drive)	V_{LC}		− 0.5 to V_{DD} + 0.5	V
Input Voltage	V_{IN}		− 0.5 to V_{DD} + 0.5	V
Output Voltage	V_{OUT1}	Except sink open drain pin	− 0.5 to V_{DD} + 0.5	V
	V_{OUT2}	Sink open drain pin	− 0.5 to 10	
Output Current (per 1 pin)	I_{OUT}		3.2	mA
Power Dissipation [T_{opr} = 70℃]	PD		600	mW
Soldering Temperature (time)	T_{sld}		260 (10sec)	℃
Storage Temperature	T_{stg}		− 55 to 125	℃
Operating Temperature	T_{opr}		− 30 to 60	℃

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, T_{opr} = − 30 to 60°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}		In the Normal mode	2.7	6.0	V
			In the SLOW mode	2.7		
Input High Voltage	V_{IH1}	Except Hysteresis Input	$V_{DD} \geqq 4.5V$	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis Input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5V$	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Except Hysteresis Input	$V_{DD} \geqq 4.5V$	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis Input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5V$		$V_{DD} \times 0.1$	
Clock Frequency (High freq.)	fc	XIN, XOUT		960		KHz
Clock Frequency (Low freq.)	fs	XTIN, XTOUT		30.0	34.0	KHz

Note . Input Voltage V_{IH3}, V_{IL3} : in the SLOW mode

D.C. CHARACTERISTICS (V_{SS} = 0V, T_{opr} = − 30 to 60°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		−	0.7	−	V
Input Current	I_{IN1}	Port K0, TEST, $\overline{RESET}$	V_{DD} = 5.5V, V_{IN} = 5.5V / 0V	−	−	± 2	μA
	I_{IN2}	Ports R (open drain)					
Low Level Input Current	I_{IL}	Ports R (push-pull)	V_{DD} = 5.5V, V_{IN} = 0.4V	−	−	− 2	mA
Input Resistance	R_{IN1}	Port K0 with pull-up/pull-down		30	70	150	KΩ
	R_{IN2}	$\overline{RESET}$		100	220	450	
Output Leakage Current	I_{LO}	Ports R (open drain)	V_{DD} = 5.5V, V_{OUT} = 5.5V	−	−	2	μA
Output Level High Voltage	V_{OH}	Ports R (push-pull)	V_{DD} = 4.5V, I_{OH} = − 200μA	2.4	−	−	V
Output Level Low Voltage	V_{OL2}	Except XOUT	V_{DD} = 4.5V, I_{OL} = 1.6mA	−	−	0.4	V
Segment Output Resistance	R_{OS}	SEG pin	V_{DD} = 5V, V_{DD} − V_{LC} = 3V	−	20	−	KΩ
Common Output Resistance	R_{OC}	COM pin					
Segment/Common Output Voltage	$V_{O2/3}$	SEG / COM pin		3.8	4.0	4.2	V
	$V_{O1/2}$			3.3	3.5	3.7	
	$V_{O1/3}$			2.8	3.0	3.2	
Supply Current (in the Nomal mode)	I_{DD}		V_{DD} = 5.5V, V_{LC} = V_{SS}, fc = 960KHz	−	0.6	1.2	mA
	I_{DDT}		V_{DD} = 5.5V, V_{LC} = V_{SS}, fc = 960KHz, When tone is oscillating	−	2.2	3.5	
Supply Current (in the SLOW mode)	I_{DDS}		V_{DD} = 3V, V_{LC} = V_{SS}, fs = 32.768KHz	−	15	30	μA

Note 1. Typ. values shows those at T_{opr} = 25°C, V_{DD} = 5V.

Note 2. Input Current I_{IN1} : The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.

Note 3. Output Resistance Ros, Roc : Shows on-resistance at the level switching.

Note 4. $V_{O2/3}$: Shows 2/3 level output voltage, when the 1/4 or 1/3 duty LCD is used.
$V_{O1/2}$: Shows 1/2 level output voltage, when the 1/2 duty or static LCD is used.
$V_{O1/3}$: Shows 1/3 level output voltage, when the 1/4 or 1/3 duty LCD is used.

Note 5. Supply Current I_{DD} : V_{IN} = 5.3V/0.2V
The port K0 is open when the input resistor is contained.
The voltage applied to the port R is within the valid range.

Note 6. Supply Current I_{DDS} : V_{IN} = 2.8V/0.2V. Only low frequency clock is only osillated (connecting XTIN, XTOUT).

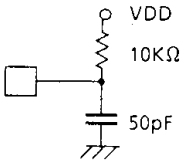
A.C. CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 2.7 to 6.0V, T_{opr} = – 30 to 60°C)

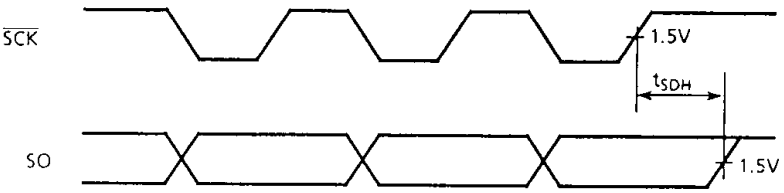
PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}	In the Normal mode	8.3			μs
		In the SLOW mode	235	—	267	μs
High level Clock pulse Width	t_{WCH}	External clock	80	—	—	ns
Low level Clock pulse Width	t_{WCL}					
Shift Data Hold Time	t_{SDH}		$0.5t_{cy}$ – 300	—	—	ns

Note. Shift Data Hold Time :

External Circuit for $\overline{SCK}$ pin and SO pin.



Serial port (completion of transmission)



TONE OUTPUT CHARACTERISTICS

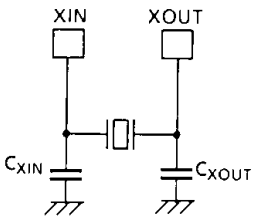
(V_{SS} = 0V, V_{DD} = 2.7 to 6.0V, T_{opr} = – 30 to 60°C)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Tone Output Voltage (ROW)	V_{TONE}	RL ≧ 10KΩ, V_{DD} = 2.7V	125	185	250	mVrms
Pre-emphasis High Band (COL / ROW)	PEHB	PEHB = 20log (COL/ROW)	1	2	3	dB
Output Distortion	DIS		—	—	10	%
Frequency Stability	△f	Except error of osc. frequency	—	—	0.7	%

RECOMMENDED OSCILLATING CONDITIONS

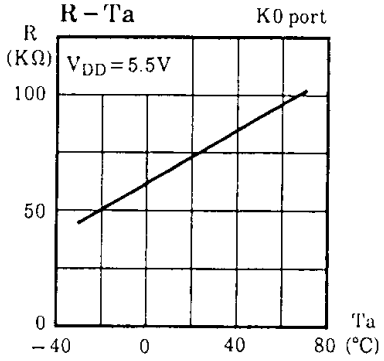
(V_{SS} = 0V, VDD = 2.7 to 6.0V, Topr = – 30 to 60°C)

960KHz
Ceramic Resonator
KBR - 960H3 (KYOCERA) $C_{XIN} = C_{XOUT}$ = 100pF
CSB960J21 (MURATA) $C_{XIN} = C_{XOUT}$ = 220pF

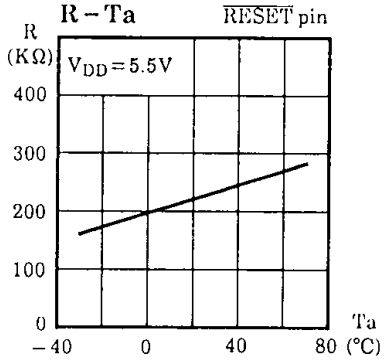


TYPICAL CHARACTERISTICS

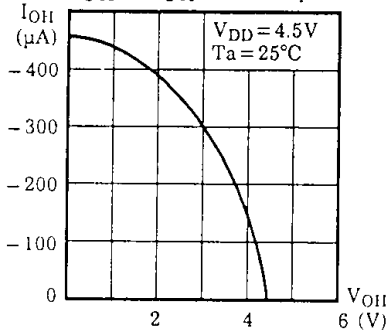
R – Ta K0 port



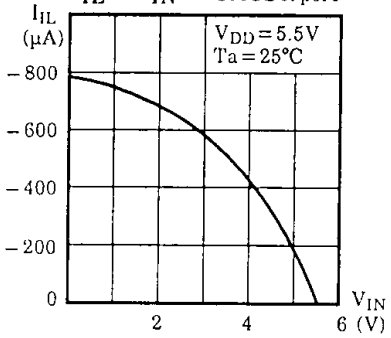
R – Ta $\overline{\text{RESET}}$ pin



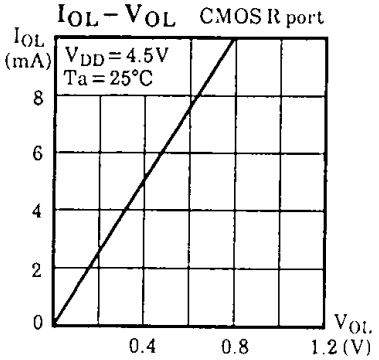
$I_{OH} - V_{OH}$ CMOS R port



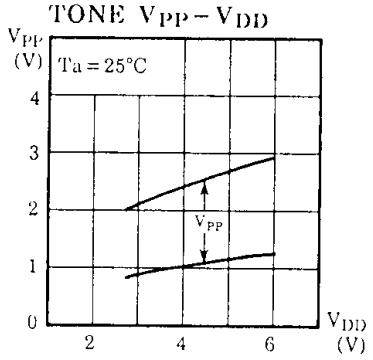
$I_{IL} - V_{IN}$ CMOS R port



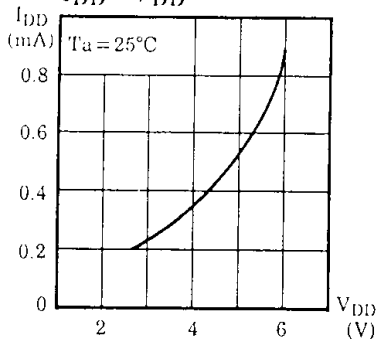
$I_{OL} - V_{OL}$ CMOS R port



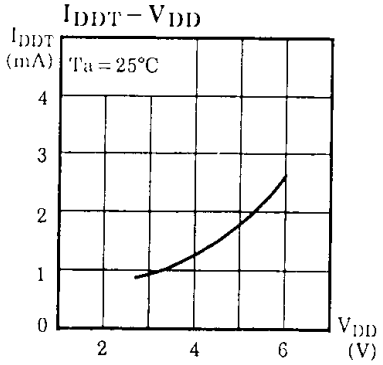
TONE $V_{PP} - V_{DD}$



$I_{DD} - V_{DD}$



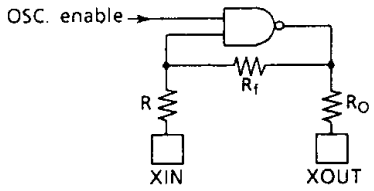
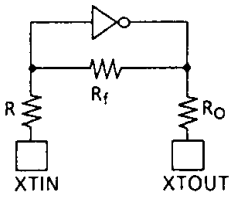
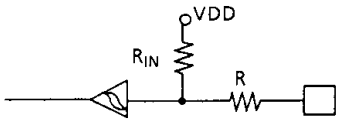
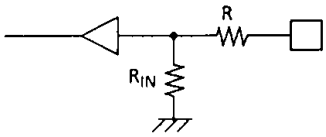
$I_{DDT} - V_{DD}$



INPUT/OUTPUT CIRCUITRY

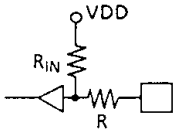
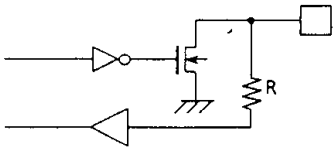
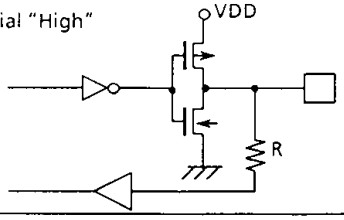
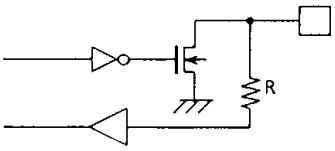
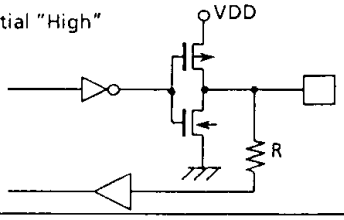
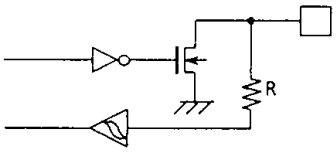
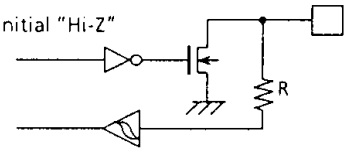
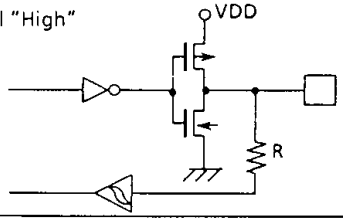
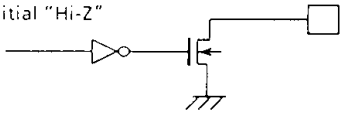
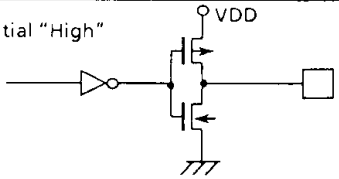
(1) Control pins

Input/Output circuitries of the 47C456A control pins are shown below.

CONTROL PIN	I/O	CIRCUITRY	REMARKS
XIN XOUT	INPUT OUTPUT		Resonator connecting pins (High frequency) R = 1KΩ (typ.) R_f = 1.5MΩ (typ.) R_O = 2KΩ (typ.)
XTIN XTOUT	INPUT OUTPUT		Resonator connecting pins (Low frequency) R = 1KΩ (typ.) R_f = 15MΩ (typ.) R_O = 200KΩ (typ.)
$\overline{RESET}$	INPUT		Hysteresis input Pull-up resistor R_{IN} = 220KΩ (typ.) R = 1KΩ (typ.)
TEST	INPUT		Pull-down resistor R_{IN} = 70KΩ (typ.) R = 1KΩ (typ.)

(2) I/O Ports

The input/output circuitries of the 47C456A I/O ports are shown below, any one of the circuitries can be chosen by a code (WB, WE, WH) as a mask option.

PORT	I/O	INPUT/OUTPUT CIRCUITRY and CODE	REMARKS
K0	Input		Pull-up resistor R_{IN} = 70KΩ (typ.) R = 1KΩ (typ.)
R3 R4 R5 R6	I/O	WB: Initial "Hi-Z"  WE, WH: Initial "High" 	Sink open drain or push-pull output R = 1KΩ (typ.)
R7	I/O	WB, WE: Initial "Hi-Z"  WH: Initial "High" 	Sink open drain or push-pull output R = 1KΩ (typ.)
R8	I/O		Sink open drain Initial "Hi-Z" Hysteresis input R = 1KΩ (typ.)
R9	I/O	WB, WE: Initial "Hi-Z"  WH: Initial "High" 	Sink open drain or push-pull output Hysteresis input R = 1KΩ (typ.)
P14	Output	WB: Initial "Hi-Z"  WE, WH: Initial "High" 	Sink open drain or push-pull output

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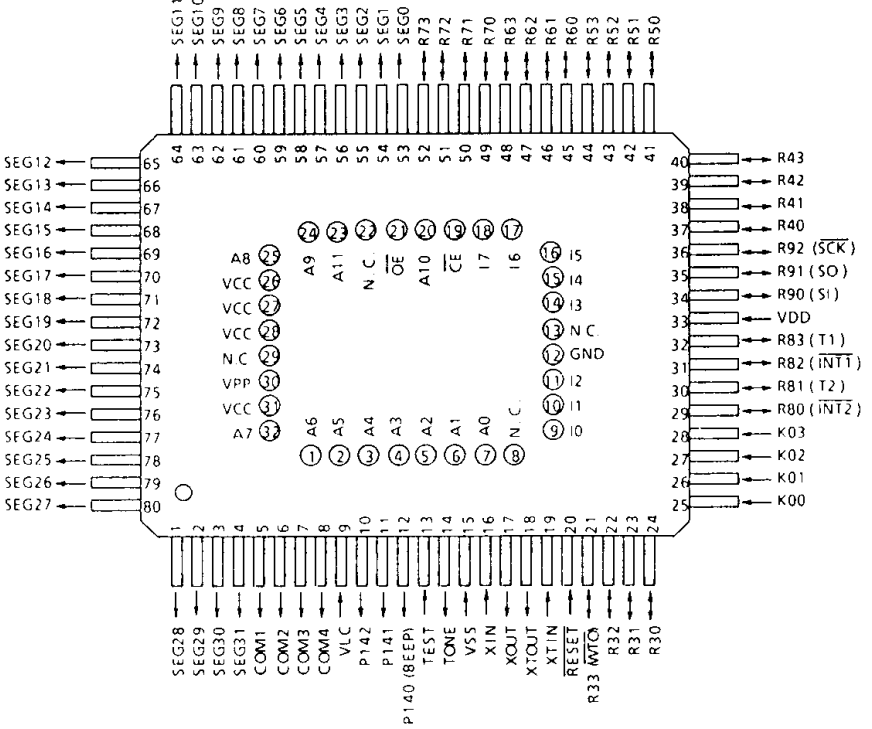
CMOS 4-BIT MICROCONTROLLER

TMP47C956AG

The 47C956A, which is equipped with an EPROM as program memory, is a piggyback type evaluator chip used for development and operational confirmation of the 47C456A application systems (programs).
The 47C956A is pin compatible with the 47C456A which is mask-programmed ROM device.

PIN ASSIGNMENT (TOP VIEW)

QFC80



PIN FUNCTION (Top of the package)

PIN NAME	Input / Output	FUNCTIONS
A11 ~ A0	Output	Program memory address output
I7 ~ I0	Input	Program memory data input
$\overline{CE}$	Output	Chip enable signal output
$\overline{OE}$		Output enable signal output
VCC	Power supply	+ 5V (connected with VDD)
GND		0V (connected with VSS)

A.C. CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Address Delay Time	t_{AD}	V_{SS} = 0V, V_{DD} = 2.7~6.0V C_L = 100pF Topr = – 30~60°C	—	—	150	ns
Data Setup Time	t_{IS}		150	—	—	ns
Data Hold Time	t_{IH}		50	—	—	ns

NOTES FOR USE

(1) Program memory

The program area is shown in Figure 1.

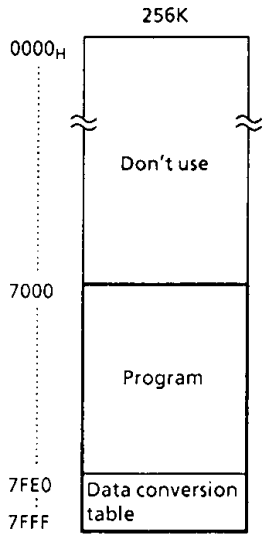


Figure 1. Program area

(2) I/O ports

Input/Output circuitries of the 47C956A I/O ports are similar to the code WB of the 47C456A.

When this chip is used as evaluator with other I/O code, it is necessary to provide the external resistors.

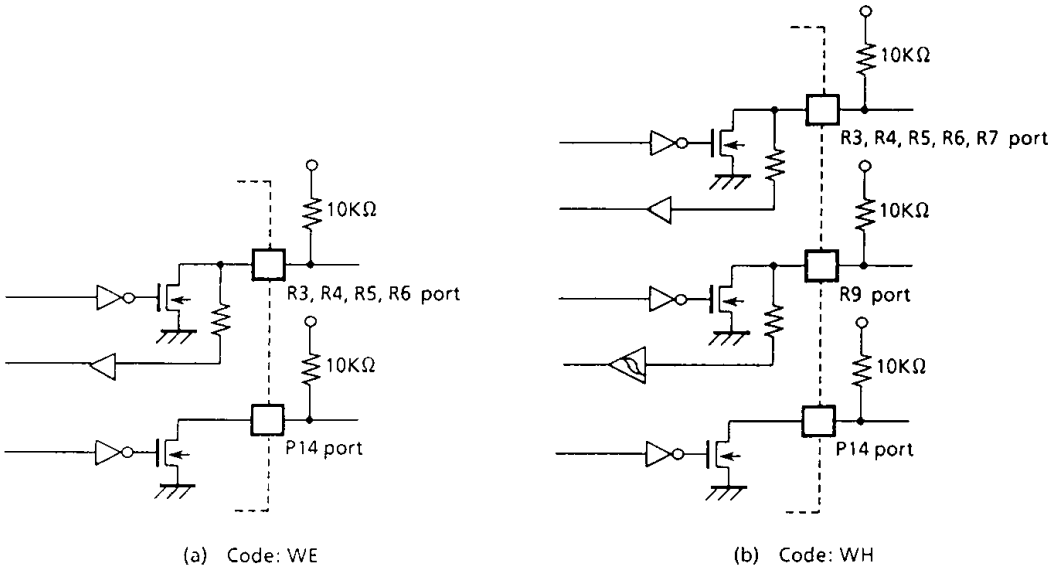


Figure 2. I/O code and external circuity