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<u>**Document Title**</u>

1Mx16 bit CellularRAM

<u>**Revision History**</u>

Revision No.	History	Draft Date	Remark
0.0	- Initial Draft	Apr. 28,2008	Preliminary
0.1	- Add PASR current table	Nov. 17,2008	
0.2	- OPTIONS in page2 updated	Mar. 11, 2009	
	- Table 10 : Electrical Characteristics and Operating Conditions updated		

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16Mb Async/Page/Burst CellularRAM

FEATURES

- Single device supports asynchrous, page and burst operation
- Vcc, VccQ voltages:
  1.7V~1.95V VCC
  1.7V~1.95V VCCQ
- Random access time: 70ns
- Burst mode READ and WRITE access:
  4, 8, 16, or 32 words, or continuous burst
  Burst wrap or sequential
  Max clock rate: 104 MHz (t_{CLK} = 9.62ns) , 133MHz(t_{CLK} = 7.5ns)
  Burst initial latency: 38.5ns (4 clocks) @ 104 MHz ,
  37.5ns(5 clocks) @ 133 MHz
  t_{ACLK}: 7ns @ 104 MHz , 5.5ns @ 133 MHz
- Page mode READ access:
  Sixteen-word page size
  Interpage READ access : 70ns
  Intrapage READ access : 20ns
- Low power consumption:
  Asynchronous READ: <25mA
  Intra page READ: <18mA
  Initial access, burst READ:
  (38.5ns [4 clocks] @ 104 MHz) <35mA
  Continuous burst READ: <30mA
  Initial access, burst READ:
  (37.5ns [5 clocks] @ 133 MHz) <40mA
  Continuous burst READ: <35mA
  Deep power down: < 10uA(max.)
- Low-power features
  On-chip temperature compensated self refresh (TCSR)
  Partial array refresh (PAR)
  Deep Power-down(DPD) mode

OPTIONS

- Configuration: 16Mb (1megabit x 16)
- Vcc core / VccQ I/O voltage supply: 1.8V
- Timing: 70ns access
- Frequency: 80 MHz, 104 MHz, 133 MHz
- Standby current at 85°C : 70μA(max)
- Operating temperature range:
  Wireless -30°C to +85°C

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General Description

CellularRAM products are high-speed, CMOS pseudo-static random access memory developed for low-power, portable applications. The 16Mb CellularRAM device has a DRAM core organized as 1 Meg x 16 bits. These devices include an industry-standard burst mode Flash interface that dramatically increase read/write bandwidth compared with other low-power SRAM or Pseudo SRAM offering.

To operate seamlessly on a burst Flash bus, CellularRAM products incorporate a transparent self refresh mechanism. The hidden refresh requires no additional support from the system memory controller and has no significant impact on device READ/WRITE performance.

Two user-accessible control registers define device operation. The bus configuration register (BCR) defines how the CellularRAM device interacts with the system memory bus and is nearly identical to its counterpart on burst mode Flash devices. The refresh configuration register (RCR) is used to control how refresh is performed on the DRAM array. These registers are automatically loaded with default settings during power-up and can be updated anytime during normal operation.

Special attention has been focused on standby current consumption during self refresh. 16Mb CellularRAM products include three mechanisms to minimize standby current. Partial array refresh (PAR) enables the system to limit refresh to only that part of the DRAM array that contains essential data. Temperature compensated refresh (TCR) uses an onchip sensor to adjust the refresh rate to match the device temperature-the refresh rate decreases at lower temperatures to minimize current consumption during standby. Deep power-down (DPD) enables the system to halt the refresh operation altogether when no vital information is stored in the device. The system configurable refresh mechanisms are accessed through the RCR.

This 16Mb CellularRAM devices is compliant with the industry-standard CellularRAM 1.5 feature set established by the CellularRAM Workgroup. It includes support for both variable and fixed latency, with three output-device drive-strength settings, additional wrap options, and a device ID register (DIDR).

Figure 1 : Functional Block Diagram -1 meg x 16
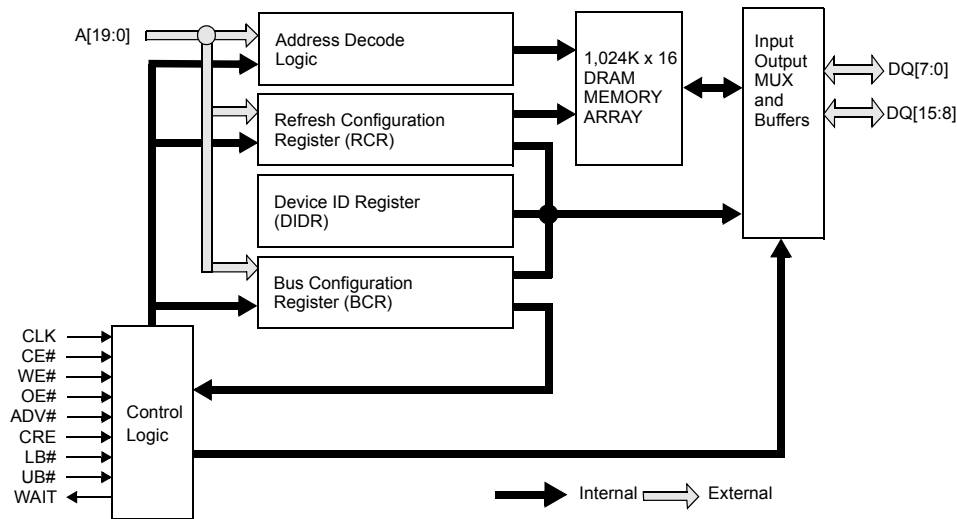
Note: Functional block diagrams illustrate simplified device operation. See pin descriptions(Table 1); Bus operations table(Table 2); and timing diagrams for detailed information.

Table 1 : PIN Descriptions

Symbol	Type	Descriptions
A[19:0]	Input	Address inputs: Inputs for addresses during READ and WRITE operations. Addresses are internally latched during READ and WRITE cycles. The address lines are also used to define the value to be loaded into the BCR or the RCR.
CLK (Note1)	Input	Clock: Synchronizes the memory to the system operating frequency during synchronous operations. When configured for synchronous operation, the address is latched on the first rising CLK edge when ADV# is active. CLK is static LOW during asynchronous access READ and WRITE operations and during PAGE READ ACCESS operations.
ADV# (Note1)	Input	Address valid: Indiates that a valid address is present on the address inputs. Addresses can be latched on the rising edge of ADV# during asynchronous READ and WRITE operations. ADV# can be held LOW during asynchronous READ and WRITE operations.
CRE	Input	Control register enable: When CRE is HIGH, WRITE operations load the RCR or BCR, and READ operations access the RCR, BCR, or DIDR.
CE#	Input	Chip enable: Activates the device when LOW. When CE# is HIGH, the device is disabled and goes into standby or deep power-down mode.
OE#	Input	Output enable: Enables the output buffers when LOW. When OE# is HIGH, the output buffers are disabled.
WE#	Input	Write enable: Determines if a given cycle is a WRITE cycle. If WE# is LOW, the cycle is a WRITE to either a configuration register or to the memory array.
LB#	Input	Lower byte enable. DQ[7:0]
UB#	Input	Upper byte enable. DQ[15:8]
DQ[15:0]	Input/Output	Data inputs/outputs.
WAIT (Note1)	Output	Wait: Provides data-valid feedback during burst READ and WRITE operations. The signal is gated by CE#. WAIT is used to arbitrate collisions between refresh and READ/WRITE operations. WAIT is also asserted at the end of a row unless wrapping within the burst length. WAIT is asserted and should be ignored during asynchronous and page mode operations. WAIT is High-Z when CE# is HIGH.
RFU	-	Reserved for future use.
Vcc	Supply	Device power supply: (1.70V~1.95V) Power supply for device core operation.
VccQ	Supply	I/O power supply: (1.70V~1.95V) Power supply for input/output buffers.
Vss	Supply	Vss must be connected to ground.
VssQ	Supply	VssQ must be connected to ground.

Note:
1. When using asynchronous mode or page mode exclusively, CLK and ADV# inputs can be tied to Vss. WAIT will be asserted but should be ignored during asynchronous and page mode operations.

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Table 2: Bus Operations

Asynchfonous Mode BCR[15]=1	Power	CLK[1]	ADV#	CE#	OE#	WE#	CRE	UB#/LB#	WAIT[2]	DQ[15:0][3]	Note
Read	Active	L	L	L	L	H	L	L	Low-z	Data out	4
Write	Active	L	L	L	X	L	L	L	Low-z	Data in	4
Standby	Standby	L	X	H	X	X	L	X	High-z	High-z	5, 6
No operation	Idle	L	X	L	X	X	L	X	Low-z	X	4, 6
Configuration register write	Active	L	L	L	H	L	H	X	Low-z	High-z	
Configuration register read	Active	L	L	L	L	H	H	L	Low-z	Config. Reg.out	
DPD	Deep Power-down	L	X	H	X	X	X	X	High-z	High-z	7
Burst Mode BCR[15]=0	**Power**	**CLK[1]**	**ADV#**	**CE#**	**OE#**	**WE#**	**CRE**	**UB#/LB#**	**WAIT[2]**	**DQ[15:0][3]**	**Note**
Async read	Active	L	L	L	L	H	L	L	Low-z	Data out	4, 8
Async write	Active	L	L	L	X	L	L	L	Low-z	Data in	4
Standby	Standby	L	X	H	X	X	L	X	High-z	High-z	5, 6
No operation	Idle	L	X	L	X	X	L	X	Low-z	X	4, 6
Initial burst read	Active	⌐⌐	L	L	X	H	L	L	Low-z	X	4, 9
Initial burst write	Active	⌐⌐	L	L	H	L	L	X	Low-z	X	4, 9
Burst continue	Active	⌐⌐	H	L	X	X	X	L	Low-z	Data out or Data in	4, 9
Burst suspend	Active	X	X	L	H	X	X	X	Low-z	High-z	4, 9
Configuration register write	Active	⌐⌐	L	L	H	L	H	X	Low-z	High-z	9, 10
Configuration register read	Active	⌐⌐	L	L	L	H	H	L	Low-z	Config. Reg.out	9, 10
DPD	Deep Power-down	L	X	H	X	X	X	X	High-z	High-z	7

Note:
1. CLK must be LOW during async read and async write modes; and to achieve standby power during standby and DPD modes. CLK must be static (HIGH or LOW) during burst suspend.
2. The WAIT polarity is configured through the bus configuration register (BCR[10]).
3. When LB# and UB# are in select mode (LOW), DQ[15:0] are affected. When only LB# is in select mode, DQ[7:0] are affected. When only UB# is in the select mode, DQ[15:8] are affected.
4. The device will consume active power in this mode whenever addresses are changed.
5. When the device is in standby mode, address inputs and data inputs/outputs are internally isolated from any external influence.
6. V_{IN} = VccQ or 0V; all device pins must be static (unswitched) in order to achieve standby current.
7. DPD is initiated when CE# transitions from LOW to HIGH after writing RCR[4] to 0. DPD is maintained until CE# transitions from HIGH to LOW.
8. When the BCR is configured for sync mode, sync READ and WRITE, and async READ and WRITE are supported by EMLSI.
9. Burst mode operation is initialized through the bus configuration register (BCR[15]).
10. Initial cycle. Following cycles are the same as BURST CONTINUE. CE# must stay LOW for the equivalent of a single-word burst (as indicated by WAIT).

Functional Description

In general, CellularRAM devices are high-density alternatives to SRAM and Pseudo SRAM products, popular in low-power, portable applications. The 16Mb device contains a 16,777,216-bit DRAM core, organized as 1,048,576 addresses by 16 bits.The device implements the same high-speed bus interface found on burst mode Flash products. The CellularRAM bus interface supports both asynchronous and burst mode transfers. Page mode accesses are also included as a bandwidth-enhancing extension to the asynchronous read protocol.

Power-Up Initialization

16Mb CellularRAM products include an on-chip voltage sensor used to launch the power-up initialization process. Initialization will configure the BCR and the RCR with their default settings. (See Figure 16 and 20) Vcc and VccQ must be applied simultaneously. When they reach a stable level at or above 1.7V, the device will require 150μs to complete its self-initialization process. During the initialization period, CE# should remain HIGH. When initialization is complete, the device is ready for normal operation.

Figure 2: Power-Up Initialization Timing

Vcc=1.7V

Vcc
VccQ

$t_{PU} \geq 150\mu s$

Device ready for normal operation

Device Initialization
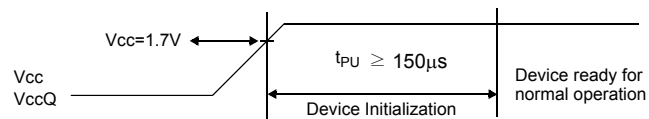
Bus Operating Modes

16Mb CellularRAM products incorporate a burst mode interface found on Flash products targeting low-power, wireless applications. This bus interface supports asynchronous, page mode, and burst mode read and write transfers. The specific interface supported is defined by the value loaded into the BCR. Page mode is controlled by the refresh configuration register (RCR[7]).

Asynchronous Mode

CellularRAM products power up in the asynchronous operating mode.This mode uses the industry- standard SRAM control bus (CE#, OE#, WE#, and LB#/UB#). READ operations (Figure 3) are initiated by bringing CE#, OE#, and LB#/UB# LOW while keeping WE# HIGH. Valid data will be driven out of the I/Os after the specified access time has elapsed. WRITE operations (Figure 4) occur when CE#, WE#, and LB#/UB# are driven LOW. During asynchronous WRITE operations, the OE# level is a "Don't care", and WE# will over-ride OE#. The data to be written is latched on the rising edge of CE#, WE#, or LB#/UB# (whichever occurs first). Asynchronous operations (page mode disabled) can either use the ADV# input to latch the address, or ADV# can be driven LOW during the entire READ/WRITE operation.

During asynchronous operation, the CLK input must be held static LOW. WAIT will be driven while the device is enabled and its state should be ignored. WE# LOW time must be limited to t_{CEM}

Figure 3: READ Operation (ADV# LOW)
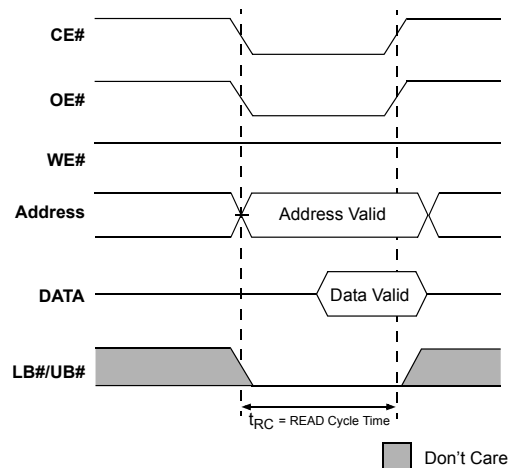
Note: ADV# must remain Low for PAGE MODE operation.

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Figure 4: WRITE Operation (ADV# LOW)
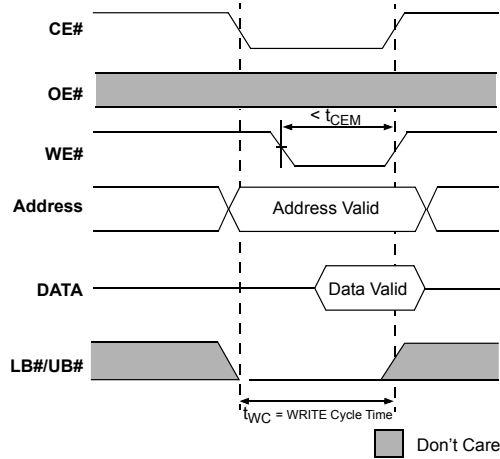
Page Mode Read Operation

Page mode is a performance-enhancing extension to the legacy asynchronous READ operation. In page-mode-capable products, an initial asynchronous read access is performed, then adjacent addresses can be read quickly by simply changing the low-order address. Addresses A[3:0] are used to determine the members of the 16-address CellularRAM page. Any change in addresses A[4] or higher will initiate a new t_{AA} access time. Figure 5 shows the timing for a page mode access. Page mode takes advantage of the fact that adjacent addresses can be read in a shorter period of time than random addresses. WRITE operations do not include comparable page mode functionality. During asynchronous page mode operation, the CLK input must be held LOW. CE# must be driven HIGH upon completion of a page mode access. WAIT will be driven while the device is enabled and its state should be ignored. Page mode is enabled by setting RCR[7] to HIGH. ADV# must be driven LOW during all page mode READ accesses. Due to refresh considerations, CE# must not be LOW longer than t_{CEM}.

Figure 5: Page Mode READ Operation (ADV# LOW)
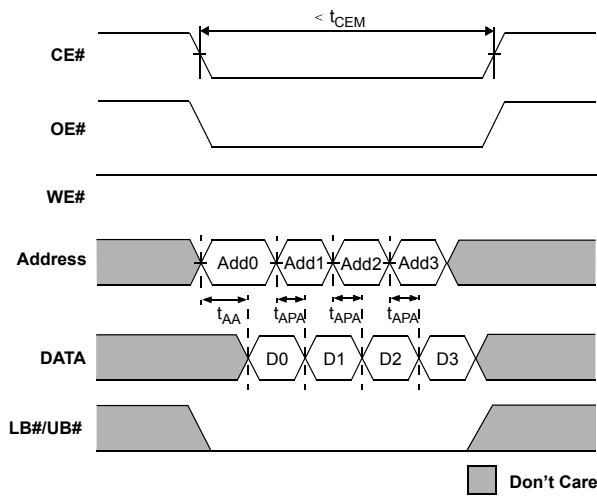
Burst Mode Operation

Burst mode operations enable high-speed synchronous READ and WRITE operations. Burst operations consist of a multi-clock sequence that must be performed in an ordered fashion. After CE# goes LOW, the address to access is latched on the rising edge of the next clock that ADV# is LOW. During this first clock rising edge, WE# indicates whether the operation is going to be a READ (WE# = HIGH, Figure 6) or a WRITE (WE# = LOW, Figure 7).

Figure 6: Burst Mode READ (4-word burst)
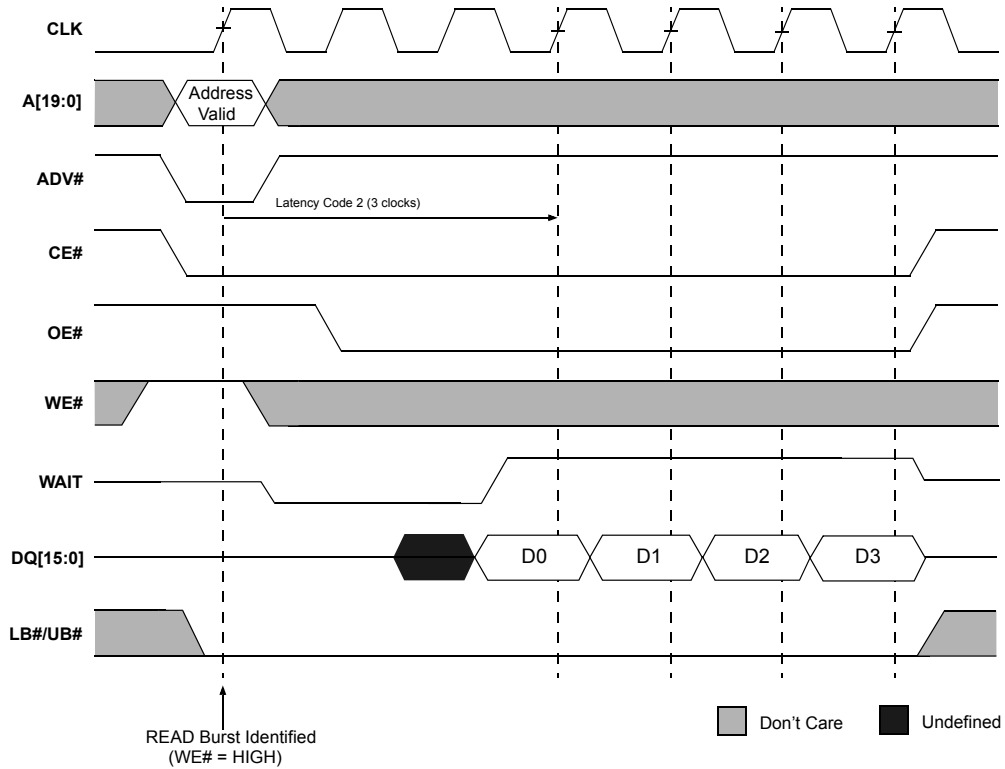
Note: Non-default BCR settings for burst mode READ (4-word burst): Fixed or variable latency; Latency code 2 (3 clocks); WAIT active LOW; WAIT asserted during delay. Diagram in the figure 6 is representative of variable latency with no refresh collision or fixed-latency access.

Figure 7: Burst Mode WRITE (4-word burst)

WRITE Burst Identified
(WE# = LOW)

Don't Care
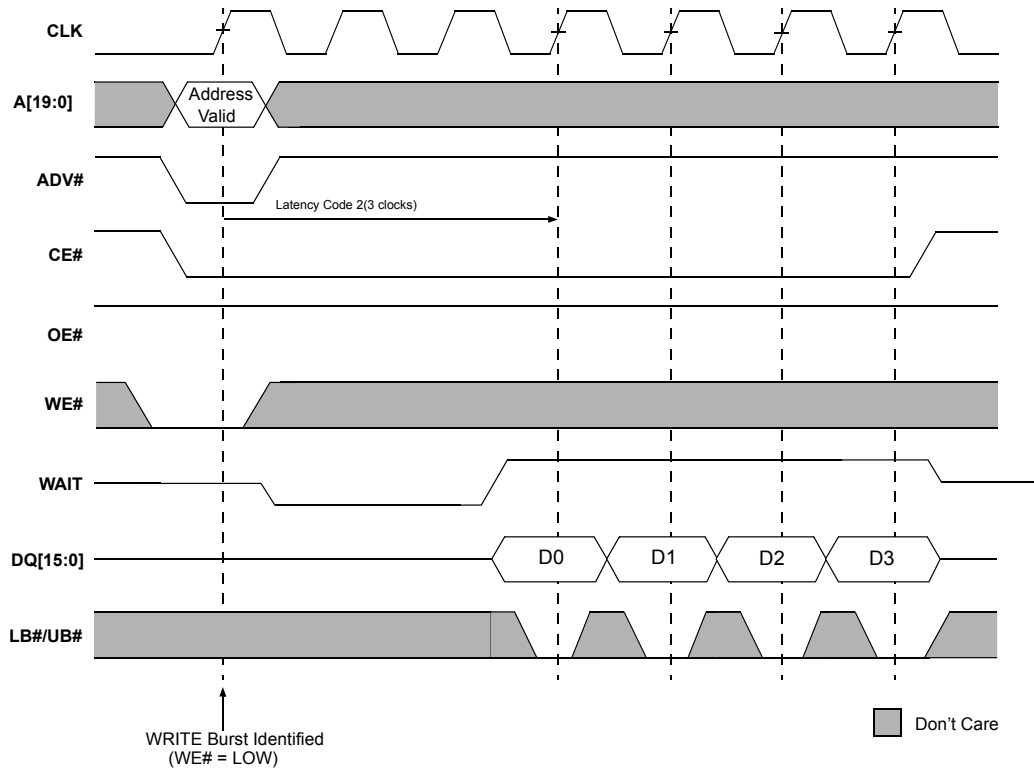
Note:
Non-default BCR settings for burst mode WRITE (4-word burst): Fixed or variable latency; latency code 2 (3 clocks); WAIT active LOW; WAIT asserted during delay.

The size of a burst can be specified in the BCR either as a fixed length or continuous. Fixed-length bursts consist of four, eight, sixteen, or thirty-two words. Continuous bursts have the ability to start at a specified address and burst to the end of the 128-word row.

The latency count stored in the BCR defines the number of clock cycles that elapse before the initial data value is transferred between the processor and CellularRAM device. The initial latency for READ operations can be configured as fixed or variable (WRITE operations always use fixed latency). Variable latency allows the CellularRAM to be configured for minimum latency at high clock frequencies, but the controller must monitor WAIT to detect any conflict with refresh cycles.

Fixed latency outputs the first data word after the worst-case access delay, including allowance for refresh collisions. The initial latency time and clock speed determine the latency count setting. Fixed latency is used when the controller cannot monitor WAIT. Fixed latency also provides improved performance at lower clock frequencies.

The WAIT output asserts when a burst is initiated, and de-asserts to indicate when data is to be transferred into (or out of) the memory. WAIT will again be asserted at the boundary of the 128-word row, unless wrapping within the burst length. With wrap off, the CellularRAM device will restore the previous row's data and access the next row, WAIT will be de-asserted, and the burst can continue across the row boundary(See Figure 34 on page 45 for a READ, Figure 42 on page 53 for a WRITE).

To access other devices on the same bus without the timing penalty of the initial latency for a new burst, burst mode can be suspended. Bursts are suspended by stopping CLK. CLK can be stopped HIGH or LOW. If another device will use the data bus while the burst is suspended, OE# should be taken HIGH to disable the CellularRAM outputs; otherwise, OE# can remain LOW. Note that the WAIT output will continue to be active, and as a result no other devices should directly share the WAIT connection to the controller. To continue the burst sequence, OE# is taken LOW, then CLK is restarted after valid data is available on the bus. The CE# LOW time

Figure 8: Refresh Collision During Variable-Latency READ Operation

Additional WAIT states inserted to allow refresh completion

Don't Care   Undefined
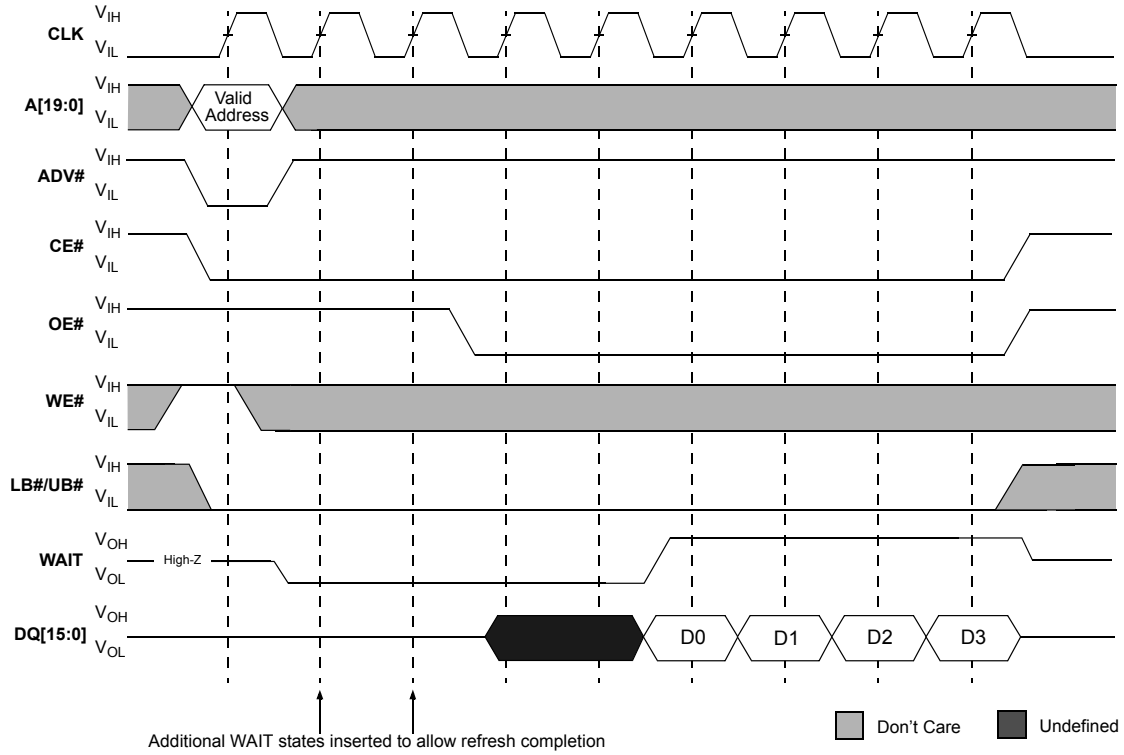
Note:
Non-default BCR settings for refresh collision during variable-latency READ operation: Latency code 2 (3 clocks); WAIT active LOW; WAIT asserted during delay.

Mixed-Mode Operation

The device supports a combination of synchronous READ and asynchronous READ and WRITE operations when the BCR is configured for synchronous operation. (Some vendors also support asychronous READ.) The asynchronous READ and WRITE operations require that the clock (CLK) remain LOW during the entire sequence. The ADV# signal can be used to latch the target address, or it can remain LOW during the entire WRITE operation. CE# can remain LOW when transitioning between mixed-mode operations with fixed latency enabled; however, the CE# LOW time must not exceed t_{CEM}. Mixed-mode operation facilitates a seamless interface to legacy burst mode Flash memory controllers. See Figure 47 for the "Asychronous WRITE Followed by Burst READ" timing diagram.

WAIT Operation

The WAIT output on a CellularRAM device is typically connected to a shared, system-level WAIT signal. (See Figure 9.) The shared WAIT signal is used by the processor to coordinate transactions with multiple memories on the synchronous bus.

Figure 9: Wired or WAIT Configuration
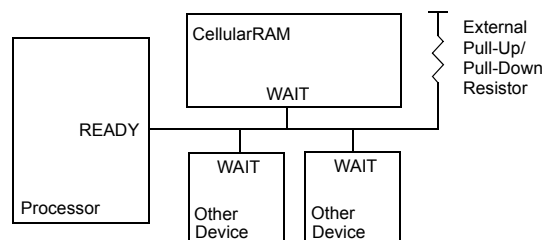
When a READ or WRITE operation has been initiated, WAIT goes active to indicate that the CellularRAM device requires additional time before data can be transferred. For READ operations, WAIT will remain active until valid data is output from the device. For WRITE operations, WAIT will indicate to the memory controller when data will be accepted into the CellularRAM device. When WAIT transitions to an inactive state, the data burst will progress on successive clock edges.

During a burst cycle, CE# must remain asserted until the first data is valid. Bringing CE# HIGH during WAIT cycles may cause data corruption. When using variable initial access latency (BCR[14] = 0), the WAIT output performs an arbitration role for READ operations launched while an on-chip refresh is in progress. If a collision occurs, WAIT is asserted for additional clock cycles until the refresh has completed. (See Figure 8) When the refresh operation has completed, the READ operation will continue normally.

WAIT will be asserted but should be ignored during asynchronous READ and WRITE, and page READ operations. By using fixed initial latency (BCR[14] = 1), this CellularRAM device can be used in burst mode without monitoring the WAIT signal. However, WAIT can still be used to determine when valid data is available at the start of the burst and at the end of row. If WAIT is not monitored, the controller must stop burst accesses at row boundaries on its own.

LB#/UB# Operation

The LB# enable and UB# enable signals support byte-wide data WRITEs. During WRITE operations, any disabled bytes will not be transferred to the RAM array and the internal value will remain unchanged. During an asynchronous WRITE cycle, the data to be written is latched on the rising edge of CE#, WE#, LB#, or UB#, whichever occurs first. LB# and UB# must be LOW during READ cycles. When both the LB# and UB# are disabled (HIGH) during an operation, the device will disable the data bus from receiving or transmitting data. Although the device will seem to be deselected, it remains in an active mode as long as CE# remains LOW.

is limited by refresh considerations. CE# must not stay LOW longer than t_{CEM}. If a burst suspension will cause CE# to remain LOW for longer than t_{CEM}, CE# should be taken HIGH and the burst restarted with a new CE# LOW / ADV# LOW cycle.

Low-Power Operation

Standby Mode Operation
During standby, the device current consumption is reduced to the level necessary to perform the DRAM refresh operation. Standby operation occurs when CE# is HIGH. The device will enter a reduced power state upon completion of a READ or WRITE operation, or when the address and control inputs remain static for an extended period of time. This mode will continue until a change occurs to the address or control inputs.

Temperature Compensated Refresh
Temperature compensated refresh (TCR) allows for adequate refresh at different temperatures. This CellularRAM device includes an on-chip temperature sensor that automatically adjusts the refresh rate according to the operating temperature. The device continually adjusts the refresh rate to match that temperature.

Partial Array Refresh
Partial array refresh (PAR) restricts refresh operation to a portion of the total memory array. This feature enables the device to reduce standby current by refreshing only that part of the memory array required by the host system. The refresh options are full array, one-half array, one-quarter array, one-eighth array, or none of the array. The mapping of these partitions can start at either the beginning or the end of the address map. (See Table 11) READ and WRITE operations to address ranges receiving refresh will not be affected. Data stored in addresses not receiving refresh will become corrupted. When re-enabling additional portions of the array, the new portions are available immediately upon writing to the RCR.

Deep Power-Down Operation
Deep power-down (DPD) operation disables all refresh-related activity. This mode is used if the system does not require the storage provided by the CellularRAM device. Any stored data will become corrupted when DPD is enabled. When refresh activity has been re-enabled, the CellularRAM device will require 150μs to perform an initialization procedure before normal operations can resume. During this 150μs period, the current consumption will be higher than the specified standby levels, but considerably lower than the active current specification. DPD can be enabled by writing to the RCR using CRE or the software access sequence; DPD starts when CE# goes HIGH. DPD is disabled the next time CE# goes LOW and stays LOW for at least 10μs.

Registers

Two user-accessible configuration registers define the device operation. The bus configuration register (BCR) defines how the CellularRAM interacts with the system memory bus and is nearly identical to its counterpart on burst mode Flash devices. The refresh configuration register (RCR) is used to control how refresh is performed on the DRAM array. These registers are automatically loaded with default settings during power-up, and can be updated any time the devices are operating in a standby state. A DIDR provides information on the device manufacturer, CellularRAM generation, and the specific device configuration. The DIDR is read-only.

Access Using CRE

The registers can be accessed using either a synchronous or an asynchronous operation when the control register enable (CRE) input is HIGH. (See Figure 10 through 13) When CRE is LOW, a READ or WRITE operation will access the memory array. The configuration register values are written via addresses A[19:0]. In an asynchronous WRITE, the values are latched into the configuration register on the rising edge of ADV#, CE#, or WE#, whichever occurs first; LB# and UB# are "Don't Care". The BCR is accessed when A[19:18] are 10b; the RCR is accessed when A[19:18] are 00b. The DIDR is read when A[19:18] are 01b. For reads, address inputs other than A[19:18] are "Don't Care", and register bits 15:0 are output on DQ[15:0]. Immediately after performing a configuration register READ or WRITE operation, reading the memory array is highly recommended.

Figure 10: Configuration Register WRITE, Asynchronous Mode, Followed by READ ARRAY Operation
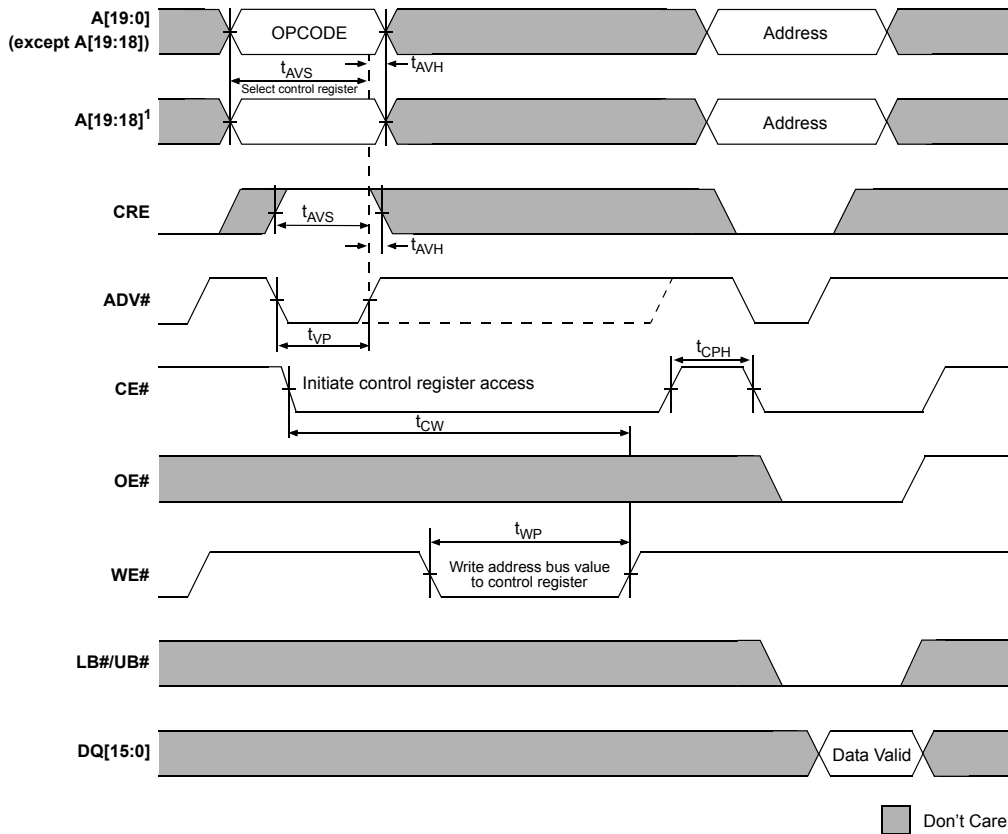
Note: 1. A[19:18] = 00b to load RCR, and 10b to load BCR.

Figure 11: Configuration Register WRITE, Synchronous Mode, Followed by READ ARRAY Operation
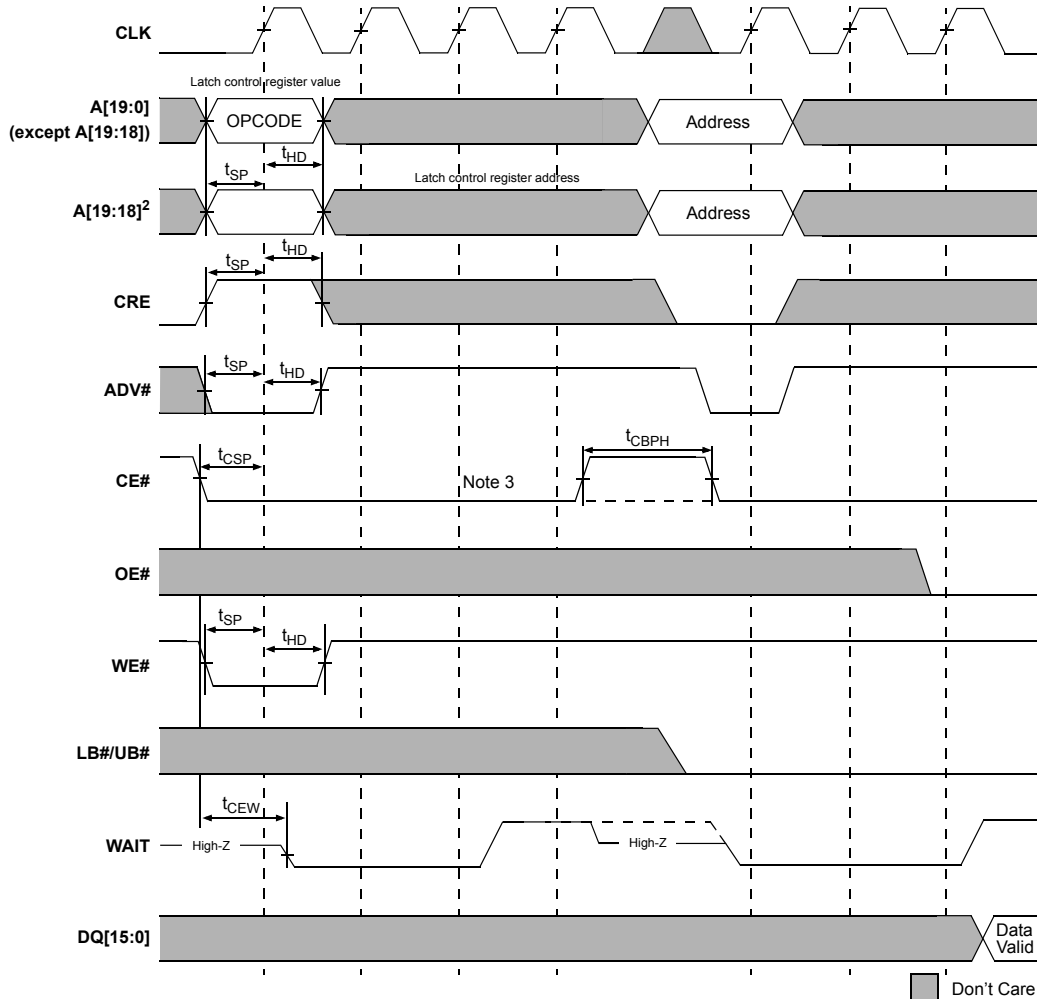
Note:
1. Non-default BCR settings for synchronous mode configuration register WRITE followed by READ ARRAY operation: Latency code 2 (3 clocks), WAIT active LOW, WAIT asserted during delay.
2. A[19:18] = 00b to load RCR, and 10b to load BCR.
3. CE# must remain LOW to complete a burst-of-one WRITE. WAIT must be monitored; additional WAIT cycles caused by refresh collisions require a corresponding number of additional CE# LOW cycles.

Figure 12: Register READ, Asynchronous Mode, Followed by READ ARRAY Operation

Note: A[19:18] = 00b to read RCR, 10b to read BCR, and 01b to read DIDR.

Figure 13: Register READ, Synchronous Mode, Followed by READ ARRAY Operation (WE# HIGH)
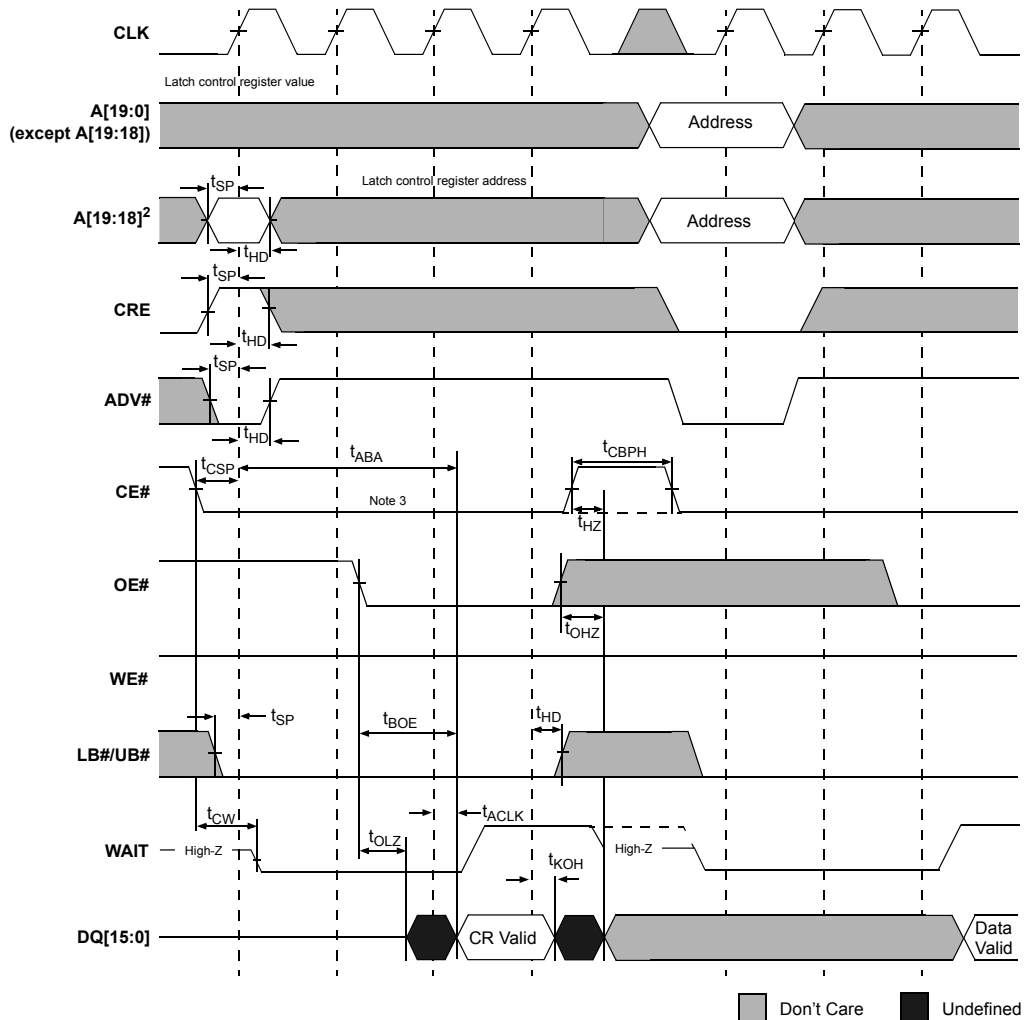
Note:
1. Non-default BCR settings for synchronous mode register READ followed by READ ARRAY operation: Latency code 2 (3 clocks); WAIT active LOW; WAIT asserted during delay.
2. A[19:18] = 00b to read RCR, 10b to read BCR, and 01b to read DIDR.
3. CE# must remain LOW to complete a burst-of-one READ. WAIT must be monitored; additional WAIT cycles caused by refresh collisions require a corresponding number of additional CE# LOW cycles.

Software Access

Software access of the registers uses a sequence of asynchronous READ and asynchronous WRITE operations. The contents of the configuration registers can be modified and all registers can be read using the software sequence. The configuration registers are loaded using a four-step sequence consisting of two asynchronous READ operations followed by two asynchronous WRITE operations.(See Figure 14.) The read sequence is virtually identical except that an asynchronous READ is performed during the fourth operation. (See Figure 15.) The address used during all READ and WRITE operations is the highest address of the CellularRAM device being accessed (FFFFFh); the contents of this address are not changed by using this sequence. The data value presented during the third operation (WRITE) in the sequence defines whether the BCR, RCR, or the DIDR is to be accessed. If the data is 0000h, the sequence will access the RCR; if the data is 0001h, the sequence will access the BCR; if the data is 0002h, the sequence will access the DIDR. During the fourth operation, DQ[15:0] transfer data in to or out of bits 15:0 of the registers. The use of the software sequence does not affect the ability to perform the standard (CRE-controlled) method of loading the configuration registers. However, the software nature of this access mechanism eliminates the need for CRE. If the software mechanism is used, CRE can simply be tied to Vss. The port line often used for CRE control purposes is no longer required.

Figure 14: Load Configuration Register
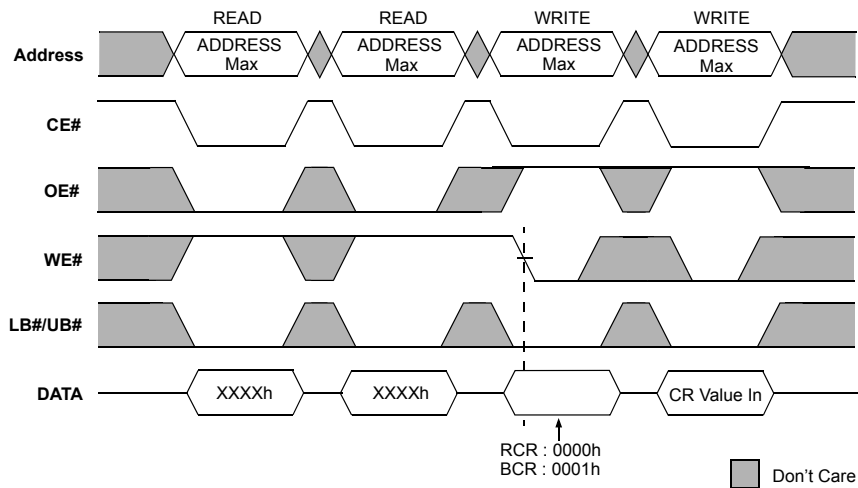
Figure 15: Read Configuration Register
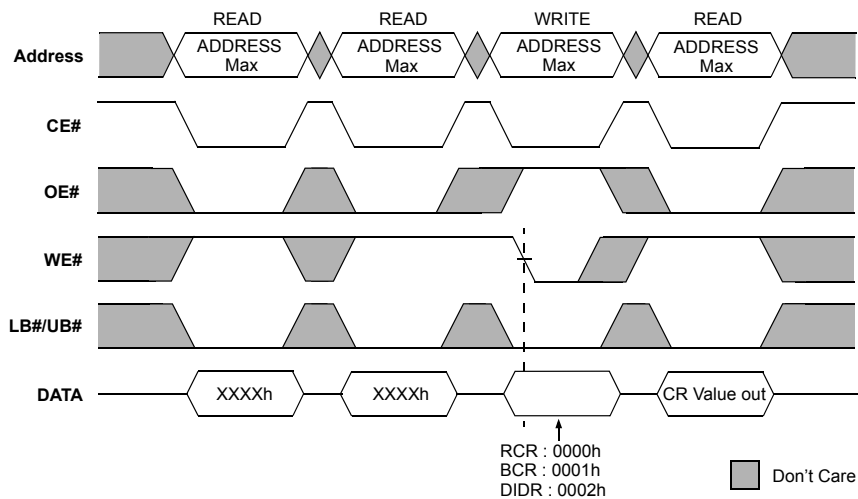
Bus Configuration Register

The BCR defines how the CellularRAM device interacts with the system memory bus. Page mode operation is enabled by a bit contained in the RCR. Figure 16 describes the control bit BCR. At power-up, the BCR is set to 9D1Fh. The BCR is accessed with CRE HIGH and A[19:18] = 10b, or through the register access software sequence with DQ = 0001h on the third cycle.

Figure 16: Bus Configuration Register Definition

A[19:18]	A[17:16]	A15	A14	A13 A12 A11	A10	A9	A8	A7	A6	A5 A4	A3	A2 A1 A0
19-18	17-16	15	14	13 12 11	10	9	8	7	6	5 4	3	2 1 0
Register Select	Reserved	Operating Mode	Initial Latency	Latency Counter	WAIT Polarity	Reserved	WAIT Configuration(WC)	Reserved	Reserved	Drive Strength	Burst Wrap(BW)*	Burst Length(BL)*

Must be set to "0"

Must be set to "0"

Must be set to "0"

Must be set to "0"

BCR[14]	Initial Access Latency
0	Variable (default)
1	Fixed

BCR[13]	BCR[12]	BCR[11]	Latency Counter
0	0	0	Code 8
0	0	1	Code 1 - Reserved
0	1	0	Code 2
0	1	1	Code 3 (default)
1	0	0	Code 4
1	0	1	Code 5
1	1	0	Code 6
1	1	1	Code 7 - Reserved

BCR[3]	Burst Wrap (Note 1)
0	Burst wraps within the burst length
1	Burst no wrap (default)

BCR[5]	BCR[4]	Drive Strength
0	0	Full
0	1	1/2 (default)
1	0	1/4
1	1	Reserved

BCR[8]	WAIT Configuration
0	Asserted during delay
1	Asserted one data before delay(default)

BCR[10]	WAIT Polarity
0	Active LOW
1	Active HIGH (default)

BCR[15]	Operating Mode
0	Synchronous burst access mode
1	Asynchronous access mode (default)

BCR[2]	BCR[1]	BCR[0]	Burst Length (Note 1)
0	0	1	4 words
0	1	0	8 words
0	1	1	16 words
1	0	0	32 words
1	1	1	Continuous burst (default)
Others			Reserved

BCR[19]	BCR[18]	Register Select
0	0	Select RCR
1	0	Select BCR
0	1	Select DIDR

Note: 1. Burst wrap and length apply to both READ and WRITE operations.

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Burst Length (BCR[2:0]) Default = Continuous Burst
Burst lengths define the number of words the device outputs during burst READ and WRITE operations. The device supports a burst length of 4, 8, 16, or 32 words. The device can also be set in continuous burst mode where data is accessed sequentially up to the end of row.

Burst Wrap (BCR[3]) Default = No Wrap
The burst-wrap option determines if a 4, 8, 16, or 32 word READ or WRITE burst wraps within the burst length, or steps through sequential addresses. If the wrap option is not enabled, the device accesses data from sequential addresses up to the end of the row.

Table 3: Sequence and Burst Length

BURST Wrap		Starting Address	4 Word Burst Length	8 Word Burst Length	16 Word Burst Length	32 Word Burst Length	Continuous Burst
BCR[3]	Wrap	Decimal	Linear	Linear	Linear	Linear	Linear
0	Yes	0	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15	0-1-2 ... 29-30-31	0-1-2-3-4-5-6-...
		1	1-2-3-0	1-2-3-4-5-6-7-0	1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-0	1-2-3 ... 30-31-0	1-2-3-4-5-6-7-...
		2	2-3-0-1	2-3-4-5-6-7-0-1	2-3-4-5-6-7-8-9-10-11-12-13-14-15-0-1	2-3-4 ... 31-0-1	2-3-4-5-6-7-8-...
		3	3-0-1-2	3-4-5-6-7-0-1-2	3-4-5-6-7-8-9-10-11-12-13-14-15-0-1-2	3-4-5 ... 0-1-2	3-4-5-6-7-8-9-...
		4		4-5-6-7-0-1-2-3	4-5-6-7-8-9-10-11-12-13-14-15-0-1-2-3	4-5-6 ... 1-2-3	4-5-6-7-8-9-10-...
		5		5-6-7-0-1-2-3-4	5-6-7-8-9-10-11-12-13-14-15-0-1-2-3-4	5-6-7 ... 2-3-4	5-6-7-8-9-10-11-...
		6		6-7-0-1-2-3-4-5	6-7-8-9-10-11-12-13-14-15-0-1-2-3-4-5	6-7-8 ... 3-4-5	6-7-8-9-10-11-12-...
		7		7-0-1-2-3-4-5-6	7-8-9-10-11-12-13-14-15-0-1-2-3-4-5-6	7-8-9 ... 4-5-6	7-8-9-10-11-12-13-...
		...			...	...	...
		14			14-15-0-1-2-3-4-5-6-7-8-9-10-11-12-13	14-15-16-...-11-12-13	14-15-16-17-18-19-20-...
		15			15-0-1-2-3-4-5-6-7-8-9-10-11-12-13-14	15-16-17...-12-13-14	15-16-17-18-19-20-21-...
		...				...	...
		30				30-31-0-...-27-28-29	30-31-32-33-34-...
		31				31-0-1-... -28-29-30	31-32-33-34-35-...
1	No	0	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15	0-1-2-...-29-30-31	0-1-2-3-4-5-6-...
		1	1-2-3-4	1-2-3-4-5-6-7-8	1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-16	1-2-3-...-30-31-32	1-2-3-4-5-6-7-...
		2	2-3-4-5	2-3-4-5-6-7-8-9	2-3-4-5-6-7-8-9-10-11-12-13-14-15-16-17	2-3-4-...-31-32-33	2-3-4-5-6-7-8-...
		3	3-4-5-6	3-4-5-6-7-8-9-10	3-4-5-6-7-8-9-10-11-12-13-14-15-16-17-18	3-4-5-...-32-33-34	3-4-5-6-7-8-9-...
		4		4-5-6-7-8-9-10-11	4-5-6-7-8-9-10-11-12-13-14-15-16-17-18-19	4-5-6-...-33-34-35	4-5-6-7-8-9-10-...
		5		5-6-7-8-9-10-11-12	5-6-7-8-9-10-11-12-13-14-15-16-17-18-19-20	5-6-7-...-34-35-36	5-6-7-8-9-10-11-...
		6		6-7-8-9-10-11-12-13	6-7-8-9-10-11-12-13-14-15-16-17-18-19-20-21	6-7-8-...-35-36-37	6-7-8-9-10-11-12-...
		7		7-8-9-10-11-12-13-14	7-8-9-10-11-12-13-14-15-16-17-18-19-20-21-22	7-8-9-...-36-37-38	7-8-9-10-11-12-13-...
		...			...	...	...
		14			14-15-16-17-18-...-23-24-25-26-27-28-29	14-15-16-...43-44-45	14-15-16-17-18-19-20-...
		15			15-16-17-18-19-...-24-25-26-27-28-29-30	15-16-17-...-44-45-46	15-16-17-18-19-20-21-...
		...				...	...
		30				30-31-32-...-59-60-61	30-31-32-33-34-35-36-...
		31				31-32-33-...-60-61-62	31-32-33-34-35-36-37-...

Drive Strength (BCR[5:4]) Default = Outputs Use Half-Drive Strength

The output driver strength can be altered to full, one-half, or one-quarter strength to adjust for different data bus loading scenarios. The reduced-strength options are intended for stacked chip (Flash + CellularRAM) environments when there is a dedicated memory bus. The reduced-drive-strength option minimizes the noise generated on the data bus during READ operations. Full output drive strength should be selected when using a discrete CellularRAM device in a more heavily loaded data bus environment. Outputs are configured at half-drive strength during testing. See Table 4 for additional information.

Table 4: Drive Strength

BCR[5]	BCR[4]	Drive Strength	Impedance Typ (Ω)	Use Recommendation
0	0	Full	25~30	CL = 30pF to 50pF
0	1	1/2 (default)	50	CL = 15pF to 30pF 104 MHz at light load
1	0	1/4	100	CL = 15pF or lower
1	1	Reserved		

WAIT Configuration (BCR[8]) Default = WAIT Transitions One Clock Before Data Valid/Invalid

The WAIT configuration bit is used to determine when WAIT transitions between the asserted and the de-asserted state with respect to valid data presented on the data bus. The memory controller will use the WAIT signal to coordinate data transfer during synchronous READ and WRITE operations. When BCR[8] = 0, data will be valid or invalid on the clock edge immediately after WAIT transitions to the de-asserted or asserted state, respectively. When A8 = 1, the WAIT signal transitions one clock period prior to the data bus going valid or invalid. (See Figure 17.)

WAIT Polarity (BCR[10]) Default = WAIT Active HIGH

The WAIT polarity bit indicates whether an asserted WAIT output should be HIGH or LOW. This bit will determine whether the WAIT signal requires a pull-up or pull-down resistor to maintain the de-asserted state.

Figure 17: WAIT Configuration During Burst Operation
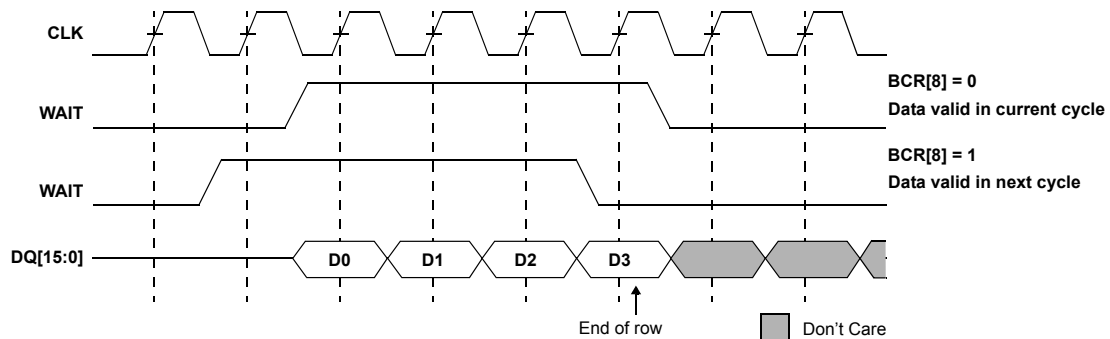
Note: Non-default BCR setting: WAIT active LOW.

Latency Counter (BCR[13:11]) Default = Three Clock Latency

The latency counter bits determine how many clocks occur between the beginning of a READ or WRITE operation and the first data value transferred. For allowable latency codes, see Tables 5 and 6, respectively, and Figures 18 and 19, respectively.

Initial Access Latency (BCR[14]) Default = Variable

Variable initial access latency outputs data after the number of clocks set by the latency counter. However, WAIT must be monitored to detect delays caused by collisions with refresh operations. Fixed initial access latency outputs the first data at a consistent time that allows for worst-case refresh collisions. The latency counter must be configured to match the initial latency and the clock frequency. It is not necessary to monitor WAIT with fixed initial latency. The burst begins after the number of clock cycles configured by the latency counter. (See Table 6 and Figure 19)

Table 5: Variable Latency Configuration Codes

BCR[13:11]	Latency Configuration Code	Latency [1]		Max Input CLK Frequency (MHz)		
		Normal	Refresh Collision	133	104	80
010	2 (3 clocks)	2	4	66(15ns)	66(15ns)	52(19.2ns)
011	3 (4 clocks)-default	3	6	104(9.62ns)	104(9.62ns)	80(12.5ns)
100	4 (5 clocks)	4	8	133(7.5ns)	-	-
Others	Reserved	-	-	-	-	-

Note: 1. Latency is the number of clock cycles from the initiation of a burst operation until data appears. Data is transferred on the next clock cycle.

Figure18: Latency Counter (Variable Initial Latency, No Refresh Collision)
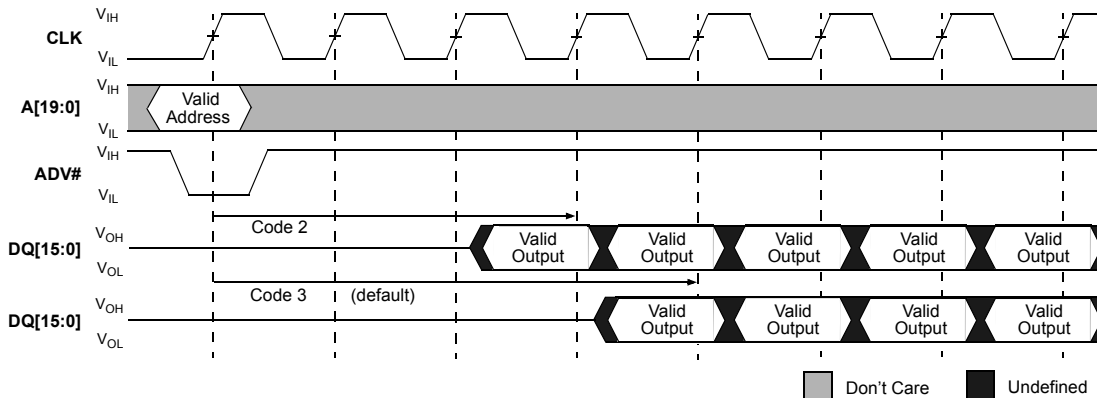
Table 6: Fixed Latency Configuration Codes

BCR[13:11]	Latency Configuration Code	Latency Count (N)	Max Input CLK Frequency (MHz)		
			133	104	80
010	2 (3 clocks)	2	33(30ns)	33(30ns)	33(30ns)
011	3 (4 clocks)-default	3	52(19.2ns)	52(19.2ns)	52(19.2ns)
100	4 (5 clocks)	4	66(15ns)	66(15ns)	66(15ns)
101	5 (6 clocks)	5	75(13.3ns)	75(13.3ns)	75(13.3ns)
110	6 (7 clocks)	6	104(9.62ns)	104(9.62ns)	80(12.5ns)
000	8 (9 clocks)	8	133(7.5ns)	-	-
others	Reserved	--	-	-	-

Figure 19: Latency Counter (Fixed Latency)
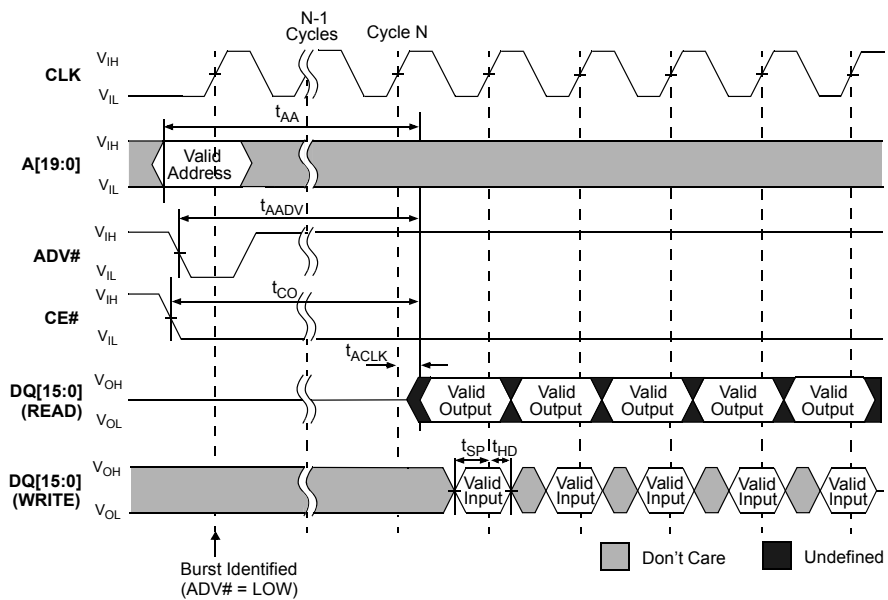
Operating Mode (BCR[15]) Default = Asynchronous Operation
The operating mode bit selects either synchronous burst operation or the default asynchronous mode of operation.

Refresh Configuration Register

The refresh configuration register (RCR) defines how the CellularRAM device performs its transparent self refresh. Altering the refresh parameters can dramatically reduce current consumption during standby mode. Page mode control is also embedded into the RCR. Figure 20 describes the control bits used in the RCR. At power-up, the RCR is set to 0010h. The RCR is accessed with CRE HIGH and A[19:18] = 00b; or through the register access software sequence with DQ = 0000h on the third cycle.

Figure 20: Refresh Configuration Register Mapping

Address Bus

A[19:18]	A[17:8]	A7	A6	A5	A4	A3	A2	A1	A0
19-18	17-8	7	6	5	4	3	2	1	0
Register Select	Reserved	Page	Reserved		DPD	Reserved	PAR		

All must be set to "0"

Setting is ignored (Default 00b)

Must be set to "0"

RCR[19]	RCR[18]	Register Select
0	0	Select RCR
1	0	Select BCR
0	1	Select DIDR

RCR[2]	RCR[1]	RCR[0]	Refresh Coverage
0	0	0	Full array (default)
0	0	1	Bottom 1/2 array
0	1	0	Bottom 1/4 array
0	1	1	Bottom 1/8 array
1	0	0	None of array
1	0	1	Top 1/2 array
1	1	0	Top 1/4 array
1	1	1	Top 1/8 array

RCR[7]	Page Mode Enable/Disable
0	Page Mode Disable (default)
1	Page Mode Enable

RCR[4]	Deep Power-Down
0	DPD Enable
1	DPD Disable (default)

Partial Array Refresh (RCR[2:0] Default = Full Array Refresh

The PAR bits restrict refresh operation to a portion of the total memory array. This feature allows the device to reduce standby current by refreshing only that part of the memory array required by the host system. The refresh options are full array, one-half array, one-quarter array, one-eighth array, or none of the array. The mapping of these partitions can start at either the beginning or the end of the address map.

Table 7: Address Patterns for PAR (RCR[4] = 1)

RCR[2]	RCR[1]	RCR[0]	Active Section	Address Space	Size	Density
0	0	0	Full Die	00000h-FFFFFh	1 Meg x 16	16Mb
0	0	1	One-half die	00000h-7FFFFh	512 K x 16	8Mb
0	1	0	One-quarter of die	00000h-3FFFFh	256 K x 16	4Mb
0	1	1	One-eighth of die	00000h-1FFFFh	128 K x 16	2Mb
1	0	0	None of die	0	0 Meg x 16	0Mb
1	0	1	One-half of die	80000h-FFFFFh	512 K x 16	8Mb
1	1	0	One-quarter of die	C0000h-FFFFFh	256 K x 16	4Mb
1	1	1	One-eighth of die	E0000h-FFFFFh	128 K x 16	2Mb

Deep Power-Down (RCR[4]) Default = DPD Disabled

The deep power-down bit enables and disables all refresh-related activity. This mode is used if the system does not require the storage provided by the CellularRAM device. Any stored data will become corrupted when DPD is enabled. When refresh activity has been re-enabled, the CellularRAM device will require 150μs to perform an initialization procedure before normal operations can resume. Deep power-down is enabled by setting RCR[4] = 0 and taking CE# HIGH. DPD can be enabled using CRE or the software sequence to access the RCR. Taking CE# LOW for at least 10μs disables DPD and sets RCR[4] = 1; it is not necessary to write to the RCR to disable DPD. BCR and RCR values (other than RCR[4]) are preserved during DPD.

Page Mode Operation (RCR[7]) Default = Disabled

The page mode operation bit determines whether page mode is enabled for asynchronous READ operations. In the power-up default state, page mode is disabled.

Device Identification Register

The DIDR provides information on the device manufacturer, CellularRAM generation, and the specific device configuration. Table 8 describes the bit fields in the DIDR. This register is read-only. The DIDR is accessed with CRE HIGH and A[19:18] = 01b, or through the register access software sequence with DQ = 0002h on the third cycle.

Table 8: Device Identification Register Mapping

Bit Field	DIDR[15]		DIDR[14:11]		DIDR[10:8]		DIDR[7:5]		DIDR[4:0]	
Field name	Row Length		Device version		Device density		CellularRAM generation		Vendor ID	
	Length	Bit Setting	Version	Bit Setting	Density	Bit Setting	Generation	Bit Setting	Vendor	Bit Setting
Options	128 words	0b	2nd	0001b	16Mb	000b	CR 1.5	010b	EMLSI	01010b

Electrical Characteristics

Table 9: Absolute Maximum Ratings

Parameter	Rating
Voltage to any pin except Vcc, VccQ relative to Vss	-0.30V to VccQ + 0.3V
Voltage on Vcc supply relative to Vss	-0.2V to +2.45V
Voltage on VccQ supply relative to Vss	-0.2V to +2.45V
Storage temperature (plastic)	-55°C to +150°C
Operating temperature (case) Wireless	-30°C to +85°C
Soldering temperature and time 10s (solder ball only)	+260°C

Stresses greater than those listed may cause permanent damage to the device.
This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 10: Electrical Characteristics and Operating Conditions

Wireless Temperature (-30°C < T_C < +85°C)

Description	Conditions	Symbol	Min	Max	Unit	Note
Supply voltage		Vcc	1.7	1.95	V	
I/O supply voltage		VccQ	1.7	1.95	V	
Input high voltage		V_{IH}	VccQ - 0.4	VccQ + 0.2	V	1
Input low voltage		V_{IL}	-0.20	0.4	V	2
Output high voltage	I_{OH} = -0.2mA	V_{OH}	0.80 VccQ		V	3
Output low voltage	I_{OL} = +0.2mA	V_{OL}		0.20 VccQ	V	3
Input leakage current	V_{IN} = 0 to VccQ	I_{LI}		1	μA	
Output leakage current	OE# = V_{IH} or chip disabled	I_{LO}		1	μA	

Operating current	Conditions	Symbol		Typ	Max	Unit	Note
Asynchronous random READ/WRITE		$I_{CC}1$	70ns		25	mA	4
Asynchronous PAGE READ		$I_{CC}1P$	70ns		18	mA	4
Initial access burst READ/WRITE		$I_{CC}2$	133MHz		40	mA	4
			104MHz		35	mA	
	V_{IN} = VccQ or 0V chip enabled, I_{OUT} = 0		80MHz		30	mA	
Continuous burst READ		$I_{CC}3R$	133MHz		35	mA	4
			104MHz		30	mA	
			80MHz		25	mA	
Continuous burst WRITE		$I_{CC}3W$	133MHz		40	mA	4
			104MHz		35	mA	
			80MHz		30	mA	
Standby current	V_{IN} = V_{CCQ} or 0V, CE# = V_{CCQ}	I_{SB}	Standard		70	μA	5, 6

Note:
1. Input signals may overshoot to VccQ + 1.0V for periods less than 2ns during transitions.
2. Input signals may undershoot to Vss - 1.0V for periods less than 2ns during transitions.
3. BCR[5:4] = 01b (default setting of one-half drive strength).
4. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add the current required to drive output capacitance expected in the actual system.
5. I_{SB} (max) values measured with PAR set to FULL ARRAY and at +85°C. In order to achieve low standby current, all inputs must be driven to either VccQ or Vss. I_{SB} might be slightly higher for up to 500ms after power-up, or when entering standby mode.
6. I_{SB} (typ) is the average I_{SB} at 25°C and Vcc = VccQ = 1.8V. This parameter is verified during characterization, and is not 100% tested.

Table 11: Deep Power-Down Specifications

Description	Conditions	Symbol	Typ	Max	Unit
Deep Power-Down	V_{IN} = VccQ or 0V; Vcc, VccQ = 1.95V; +85°C	I_{ZZ}	-	10	μA

Note: Typical (TYP) I_{ZZ} value is tested at Vcc=1.8V, T_A=25°C and not guaranteed.

Table 12: Partial-Array Refresh Specifications and Conditions

| Description	Conditions	Symbol		Array Partition	Max	Unit
Partial-array refresh standby current	V_{IN} = V_{CCQ} or 0V, CE# = V_{CCQ}	I_{PAR}	Standard power (no designation)	Full	70	uA
				1/2	65	
				1/4	60	
				1/8	60	
				0	50	

Note: IPAR (MAX) values measured at 85°C. IPAR might be slightly higher for up to 500 ms after changes to the PAR array partition or when entering standby mode.

Table 13: Capacitance

Description	Conditions	Symbol	Min	Max	Unit	Note
Input Capacitance	Tc = +25°C; f = 1 MHz; V_{IN} = 0V	C_{IN}	2.0	6	pF	1
Input/Output Capacitance(DQ)		C_{IO}	3.5	6	pF	1

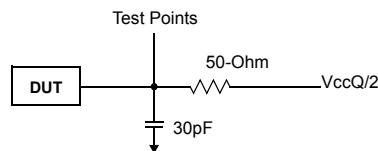Note: These parameters are verified in device characterization and are not 100% tested.

Figure 21: AC Input/Output Reference Waveform
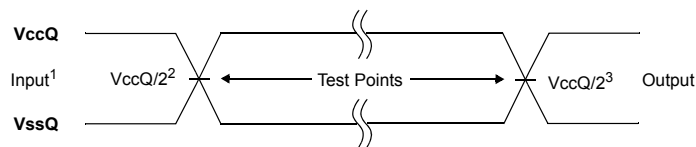
Note:
1. AC test inputs are driven at VccQ for a logic 1 and VssQ for a logic 0. Input rise and fall times (10% to 90%) <1.6ns.
2. Input timing begins at VccQ/2.
3. Output timing ends at VccQ/2.

Figure 22: AC Output Load Circuit

Note: All tests are performed with the outputs configured for default setting of half drive strength (BCR[5:4] = 01b).

TIMING REQUIREMENTS

Table 14: Asynchronous READ Cycle Timing Requirements

All tests performed with outputs configured for default setting of half drive strength, (BCR[5:4] = 01b).

Parameter	Symbol	70ns		Unit	Note
		Min	Max		
Address access time	t_{AA}	-	70	ns	
ADV# access time	t_{AADV}	-	70	ns	
Page access time	t_{APA}	-	20	ns	4
Address hold from ADV# HIGH	t_{AVH}	2	-	ns	
Address setup to ADV# HIGH	t_{AVS}	5	-	ns	
LB#/UB# access time	t_{BA}	-	70	ns	
LB#/UB# disable to DQ High-Z output	t_{BHZ}	-	7	ns	1
LB#/UB# enable to Low-Z output	t_{BLZ}	10	-	ns	2
Maximum CE# pulse width	t_{CEM}	-	4	µs	3
CE# LOW to WAIT valid	t_{CEW}	1	7.5	ns	
Chip select access time	t_{CO}	-	70	ns	
CE# LOW to ADV# HIGH	t_{CVS}	7	-	ns	
Chip disable to DQ and WAIT High-Z output	t_{HZ}	-	7	ns	1
Chip enable to Low-Z output	t_{LZ}	10	-	ns	2
Output enable to valid output	t_{OE}	-	20	ns	
Output hold from address change	t_{OH}	5	-	ns	
Output disable to DQ High-Z output	t_{OHZ}	-	7	ns	1
Output enable to Low-Z output	t_{OLZ}	3	-	ns	2
Page READ cycle time	t_{PC}	20	-	ns	4
READ cycle time	t_{RC}	70	-	ns	
ADV# pulse width LOW	t_{VP}	5	-	ns	

Note:
1. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward VccQ/2.
2. The Low-Z timings measure a 100mV transition away from the High-Z (VccQ/2) level toward either V_{OH} or V_{OL}.
3. Page mode enabled only.
4. Contact EMLSI for specific timing.

Table 15: Burst READ Cycle Timing Requirements

All tests performed with outputs configured for default setting of half drive strength, (BCR[5:4] = 01b).

Parameter	Symbol	133MHz		104MHz		80MHZ		Unit	Note
		Min	Max	Min	Max	Min	Max		
Address access time (fixed latency)	t_{AA}	-	70	-	70	-	70	ns	
ADV# access time (fixed latency)	t_{AADV}	-	70	-	70	-	70	ns	
Burst to READ access time (variable latency)	t_{ABA}	-	35.5	-	35.9	-	46	ns	
CLK to output delay	t_{ACLK}	-	5.5	-	7	-	9	ns	
Address hold from ADV# HIGH(fixed latency)	t_{AVH}	2	-	2	-	2	-	ns	
Burst OE# LOW to output delay	t_{BOE}	-	20	-	20	-	20	ns	
CE# HIGH between subsequent burst or mixed mode operations	t_{CBPH}	5	-	5	-	6	-	ns	1
Maximum CE# pulse width	t_{CEM}	-	4	-	4	-	4	µs	1
CE# or ADV# LOW to WAIT valid	t_{CEW}	1	7.5	1	7.5	1	7.5	ns	
CLK period	t_{CLK}	7.5	-	9.62	-	12.5	-	ns	
Chip select access time (fixed latency)	t_{CO}	-	70	-	70	-	70	ns	
CE# setup time to active CLK edge	t_{CSP}	2.5	-	3	-	4	-	ns	
Hold time from active CLK edge	t_{HD}	1.5	-	2	-	2	-	ns	
Chip disable to DQ and WAIT High-Z output	t_{HZ}	-	7	-	7	-	7	ns	3
CLK rise or fall time	t_{KHKL}	-	1.2	-	1.6	-	1.8	ns	
CLK to WAIT valid	t_{KHTL}	-	5.5	-	7	-	9	ns	
Output HOLD from CLK	t_{KOH}	2	-	2	-	2	-	ns	
CLK HIGH or LOW time	t_{KP}	3	-	3	-	4	-	ns	
Output disable to DQ High-Z output	t_{OHZ}	-	7	-	7	-	7	ns	2
Output enable to Low-Z output	t_{OLZ}	3	-	3	-	3	-	ns	3
Setup time to active CLK edge	t_{SP}	2	-	3	-	3	-	ns	

Note:
1. A refresh opportunity must be provided every t_{CEM}. A refresh opportunity is satisfied by either of the following two conditions: a) clocked CE# HIGH, or b) CE# HIGH for longer than 15ns.
2. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward VccQ/2.
3. The Low-Z timings measure a 100mV transition away from the High-Z (VccQ/2) level toward either V_{OH} or V_{OL}.

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Table 16: Asynchronous WRITE Cycle Timing Requirements

Parameter	Symbol	70ns		Unit	Note
		Min	Max		
Address and ADV# LOW setup time	t_{AS}	0	-	ns	
Address HOLD from ADV# going HIGH	t_{AVH}	2	-	ns	
Address setup to ADV# going HIGH	t_{AVS}	5	-	ns	
Address valid to end of WRITE	t_{AW}	70	-	ns	
LB#/UB# select to end of WRITE	t_{BW}	70	-	ns	
CE# LOW to WAIT valid	t_{CEW}	1	7.5	ns	
CE# HIGH between subsequent async operations	t_{CPH}	5	-	ns	
CE# LOW to ADV# HIGH	t_{CVS}	7	-	ns	
Chip enable to end of WRITE	t_{CW}	70	-	ns	
Data HOLD from WRITE time	t_{DH}	0	-	ns	
Data WRITE setup time	t_{DW}	20	-	ns	
Chip disable to WAIT High-Z output	t_{HZ}	-	7	ns	1
Chip enable to Low-Z output	t_{LZ}	10	-	ns	2
End WRITE to Low-Z output	t_{OW}	5	-	ns	2
ADV# pulse width	t_{VP}	5	-	ns	
ADV# setup to end of WRITE	t_{VS}	70	-	ns	
WRITE cycle time	t_{WC}	70	-	ns	
WRITE to DQ High-Z output	t_{WHZ}	-	7	ns	1
WRITE pulse width	t_{WP}	45	-	ns	3
WRITE pulse width HIGH	t_{WPH}	10	-	ns	
WRITE recovery time	t_{WR}	0	-	ns	

Note:
1. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward VccQ/2.
2. The Low-Z timings measure a 100mV transition away from the High-Z (VccQ/2) level toward either V_{OH} or V_{OL}.
3. WE# Low time must be limited to t_{CEM} (4μs).

Table 17: Burst WRITE Cycle Timing Requirements

| Parameter	Symbol	133MHz		104MHz		80MHZ		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Address and ADV# LOW setup time	t_{AS}	0	-	0	-	0	-	ns	1
Address HOLD from ADV# HIGH(fixed latency)	t_{AVH}	2	-	2	-	2	-	ns	
CE# HIGH between subsequent burst or mixed mode operations	t_{CBPH}	5	-	5	-	6	-	ns	2
Maximum CE# pulse width	t_{CEM}	-	4	-	4		4	µs	2
CE# LOW to WAIT valid	t_{CEW}	1	7.5	1	7.5	1	7.5	ns	
Clock period	t_{CLK}	7.5	-	9.62	-	12.5	-	ns	
CE# setup to CLK active edge	t_{CSP}	2.5	-	3	-	4	-	ns	
Hold time from active CLK edge	t_{HD}	1.5	-	2	-	2	-	ns	
Chip disable to WAIT High-Z output	t_{HZ}	-	7	-	7	-	7	ns	3
CLK rise or fall time	t_{KHKL}	-	1.2	-	1.6	-	1.8	ns	
Clock to WAIT valid	t_{KHTL}	-	5.5	-	7	-	9	ns	
CLK HIGH or LOW time	t_{KP}	3	-	3	-	4	-	ns	
Setup time to activate CLK edge	t_{SP}	2	-	3	-	3	-	ns	

Note:
1. t_{AS} required if t_{CSP} > 20ns.
2. A refresh opportunity must be provided every t_{CEM}. A refresh opportunity is satisfied by either of the following two conditions: a) clocked CE# HIGH, or b) CE# HIGH for longer than 15ns.
3. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward VccQ/2.

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TIMING DIAGRAMS

Figure 23: Initialization Period
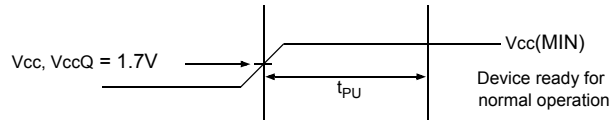
Figure 24: DPD Entry and Exit Timing Parameters
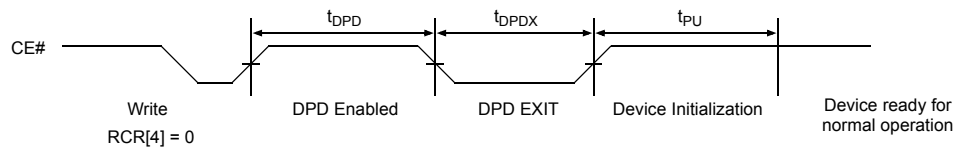
Table 18: Initialization and DPD Timing Parameters

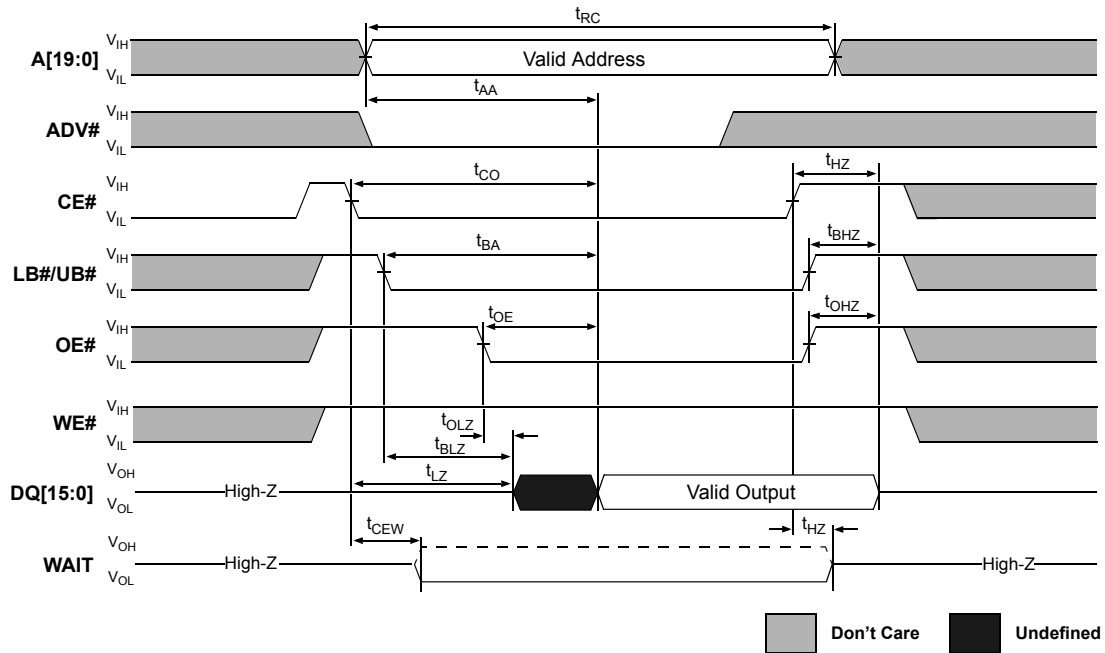| Symbol	Min	Max	Unit
t_{DPD}	150		μs
t_{DPDX}	10		μs
t_{PU}		150	μs

Figure 25: Asynchronous READ

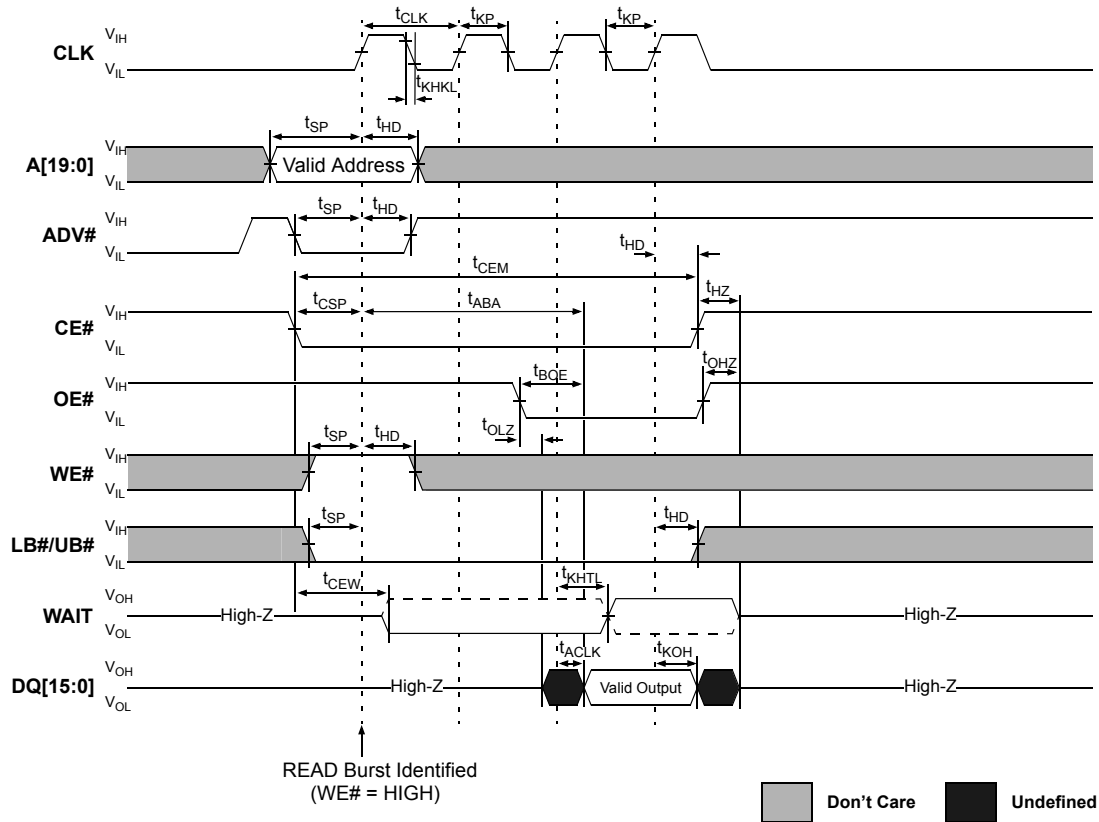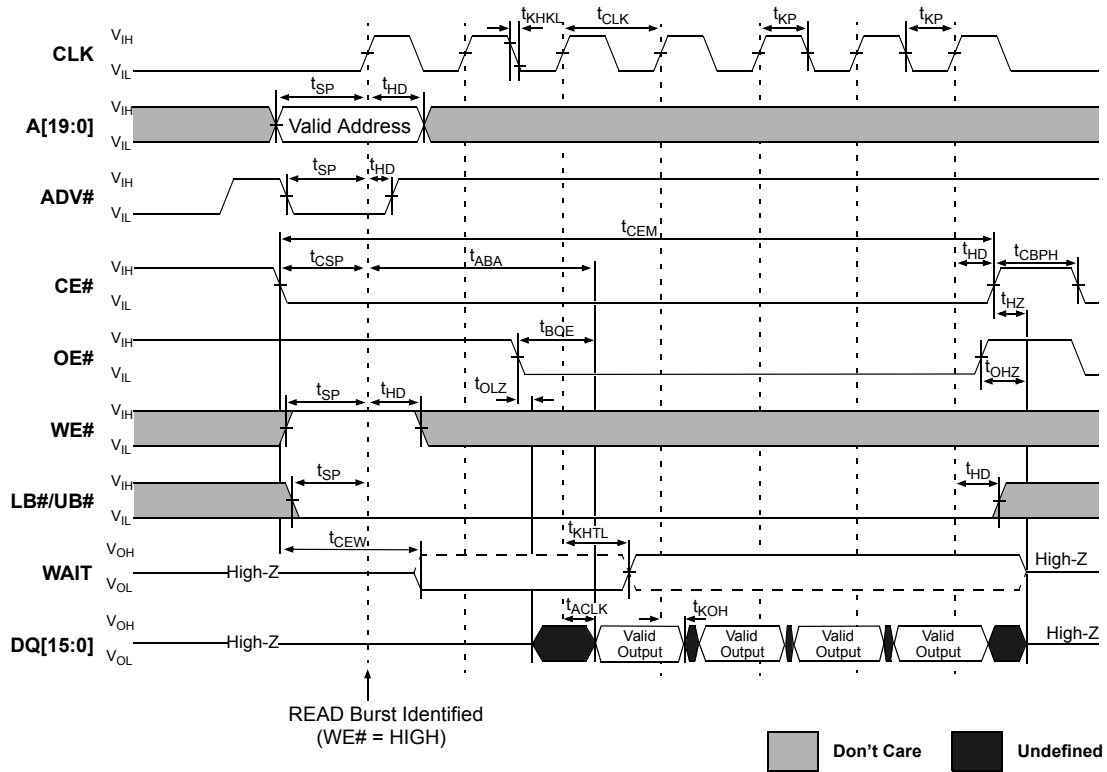**Figure 26: Asynchronous READ Using ADV#**
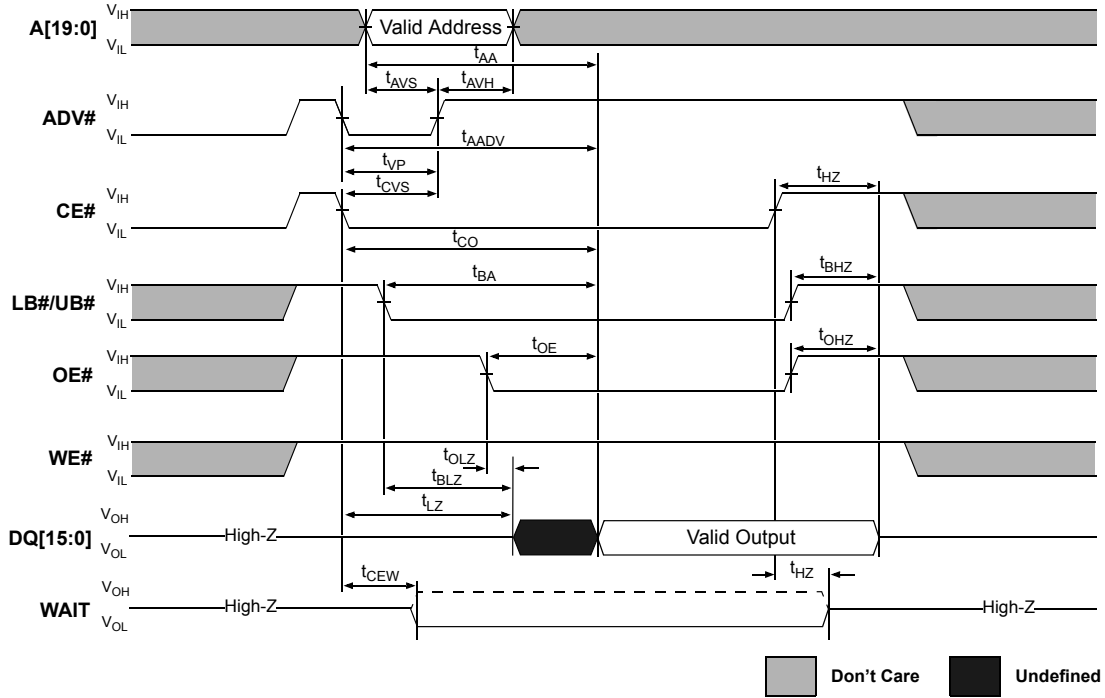
Figure 27: PAGE MODE READ
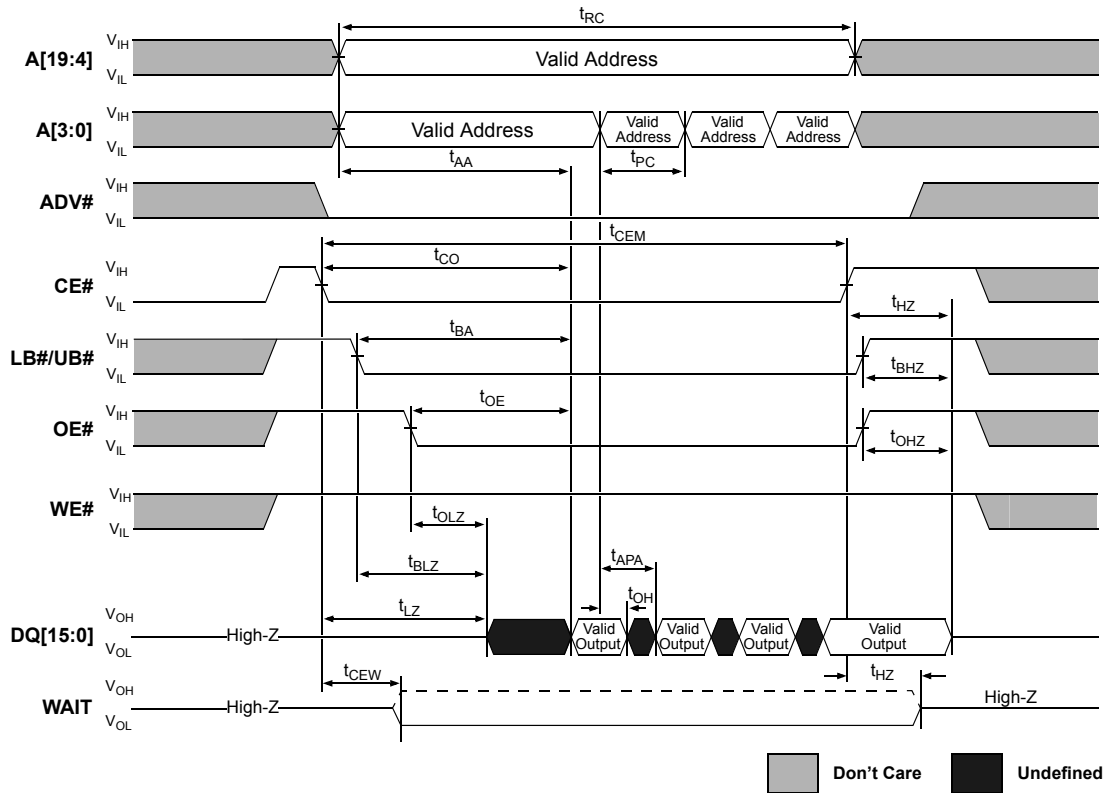
Figure 28: Single-Access Burst READ Operation - Variable Latency

READ Burst Identified
(WE# = HIGH)

Don't Care   Undefined

Note:
1. Non-default BCR settings: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.

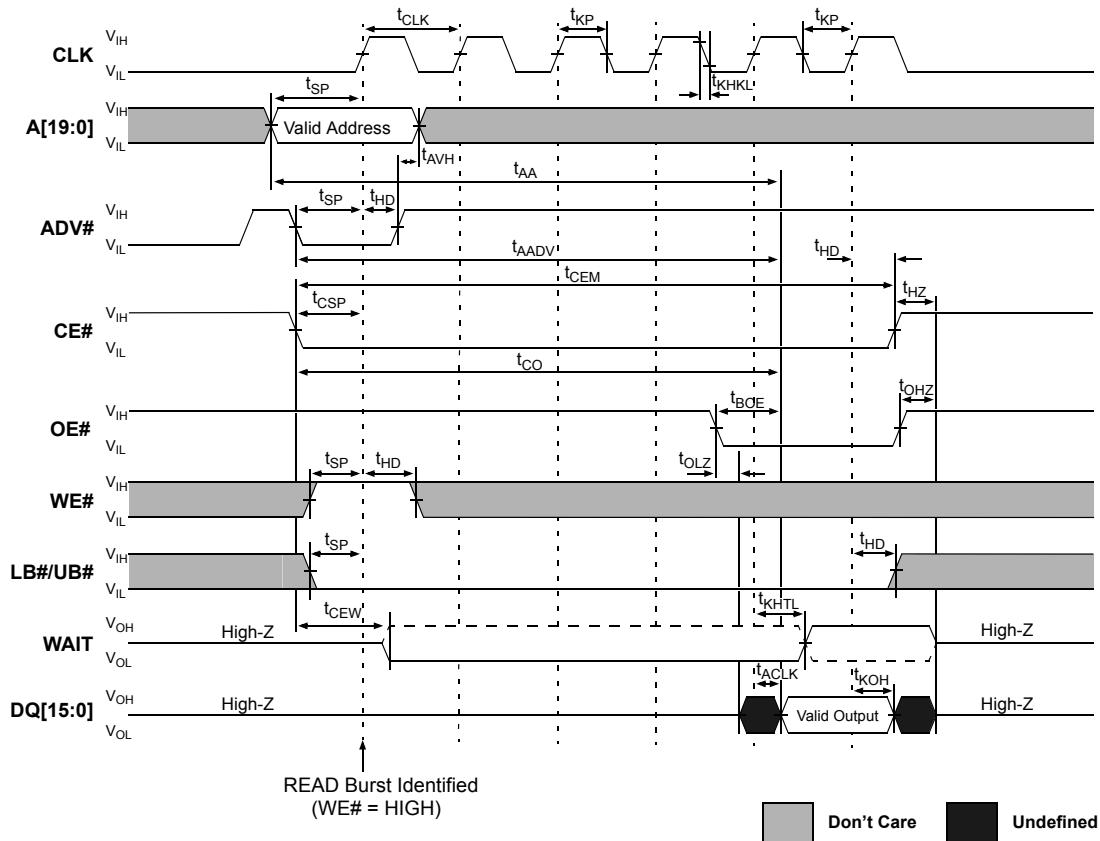**Figure 29: 4-Word Burst READ Operation - Variable Latency**

READ Burst Identified
(WE# = HIGH)

| Don't Care | Undefined |

Note:
1. Non-default BCR settings: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.

Figure 30: Single-Access Burst READ Operation - Fixed Latency

READ Burst Identified
(WE# = HIGH)

Don't Care   Undefined

Note:
1. Non-default BCR settings: Fixed latency; latency code four (five clocks); WAIT active LOW; WAIT asserted during delay.
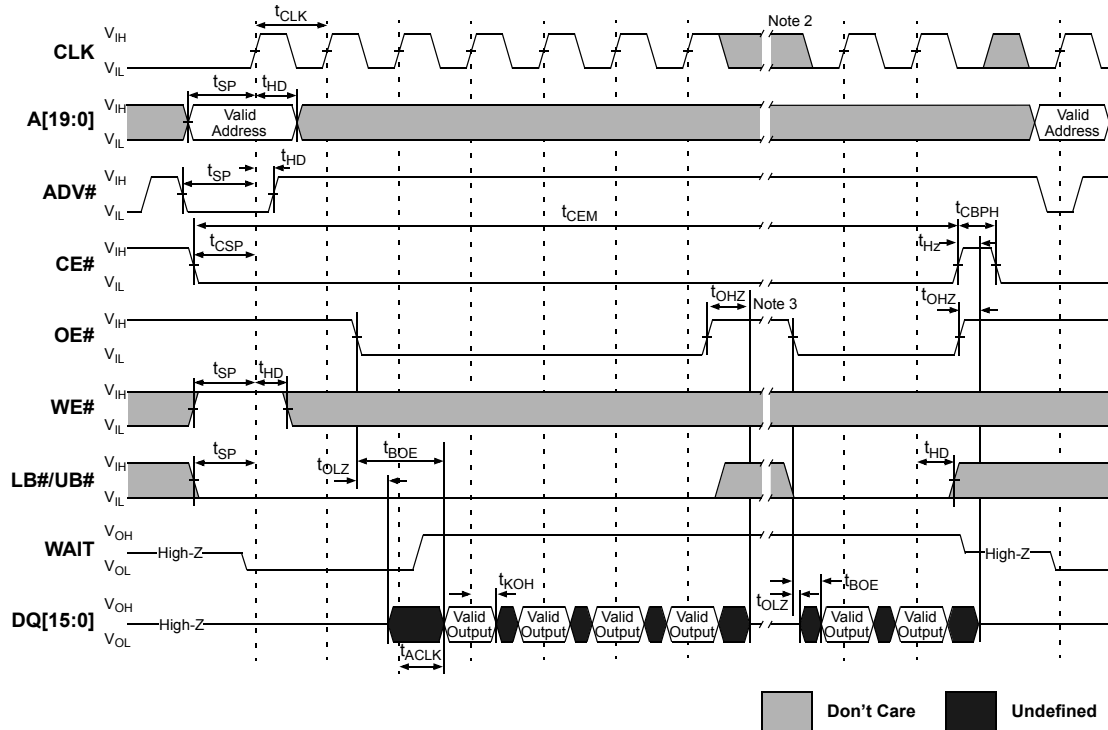
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Figure 31. 4-Word Burst READ Operation - Fixed Latency
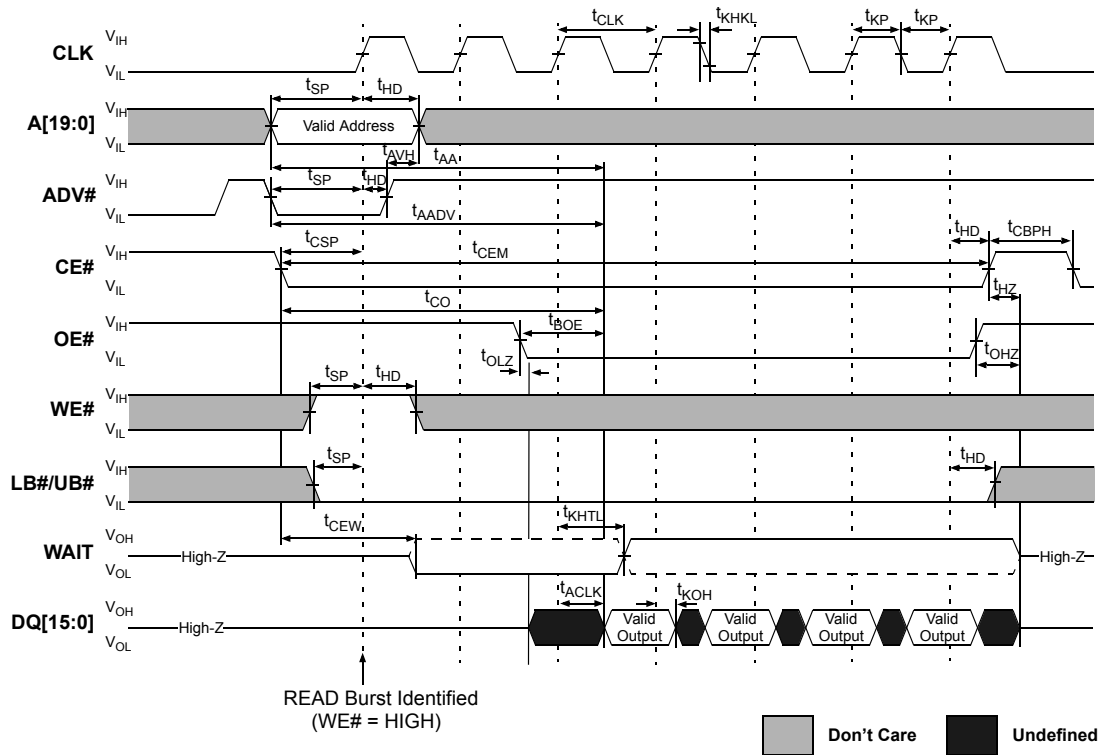
READ Burst Identified
(WE# = HIGH)

Don't Care   Undefined

Note:
1. Non-default BCR settings: Fixed latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.

Figure 32. READ Burst Suspend

Note:
1. Non-default BCR settings for READ burst suspend: Fixed or variable latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. CLK can be stopped LOW or HIGH, but must be static, with no LOW-to-HIGH transitions during burst suspend.
3. OE# can stay LOW during burst suspend. If OE# is LOW, DQ[15:0] will continue to output valid data.

Figure 33. Burst READ at End-of-Row (Wrap Off)
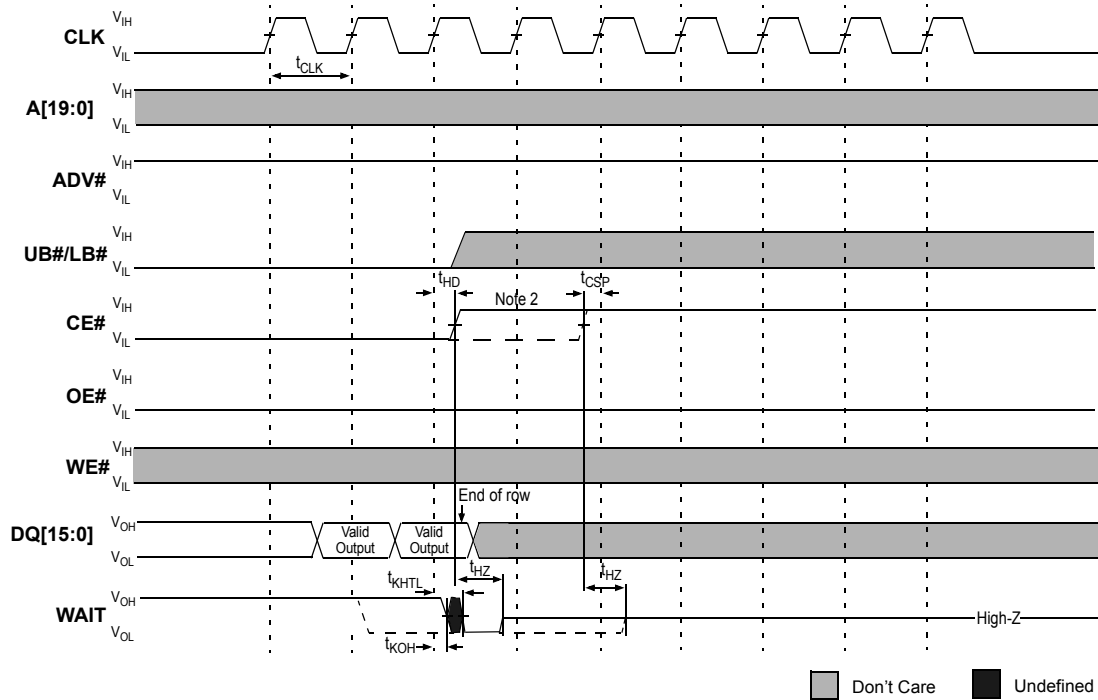
Note:
1. Non-default BCR settings for burst READ at end of row : fixed or variable latency, WAIT active LOW; WAIT asserted during delay.
2. For burst READs, CE# must go HIGH before the second CLK after the WAIT period begins (before the second CLK after WAIT asserts with BCR[8]=0, or before the third CLK after WAIT asserts with BCR[8]=1).

Figure 34. Burst READ Row boundary crossing
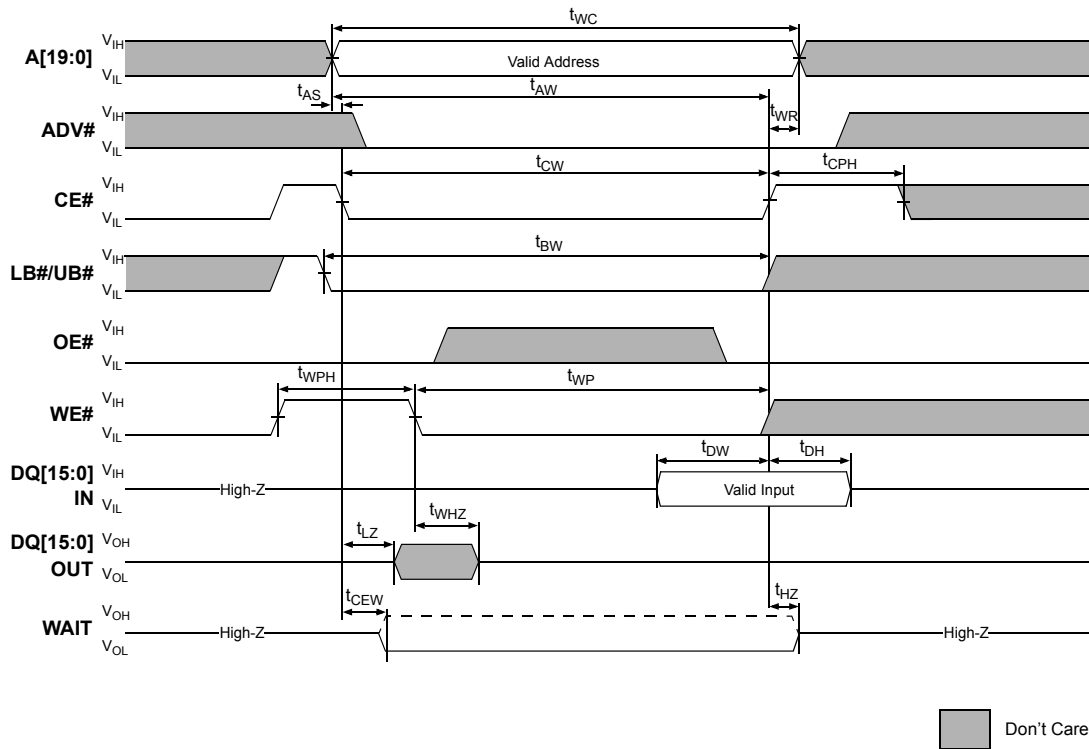

Don't Care

Note:
1. Non-default BCR settings for burst READ at end of row : fixed or variable latency, WAIT active LOW, WAIT asserted during delay. (shown as solid line)
2. WAIT will be assert for LC cycles for variables latency, or LC cycles for fixed latency.

Figure 35. CE#-Controlled Asynchronous WRITE

Figure 36. LB#/UB#-Controlled Asynchronous WRITE
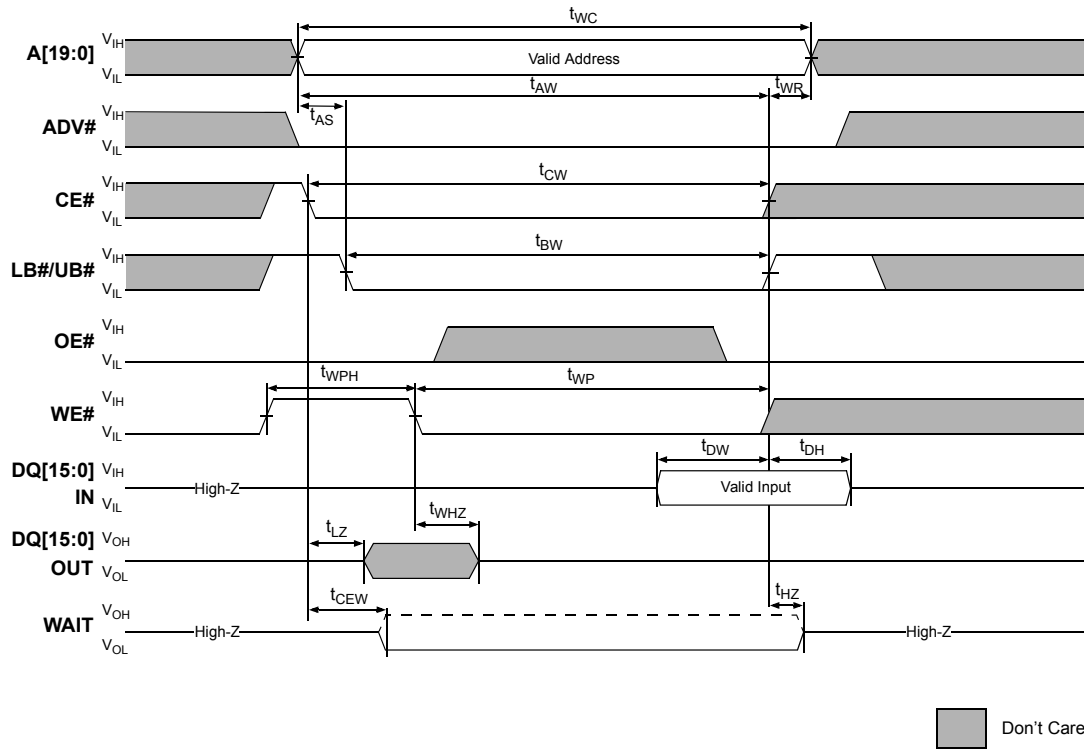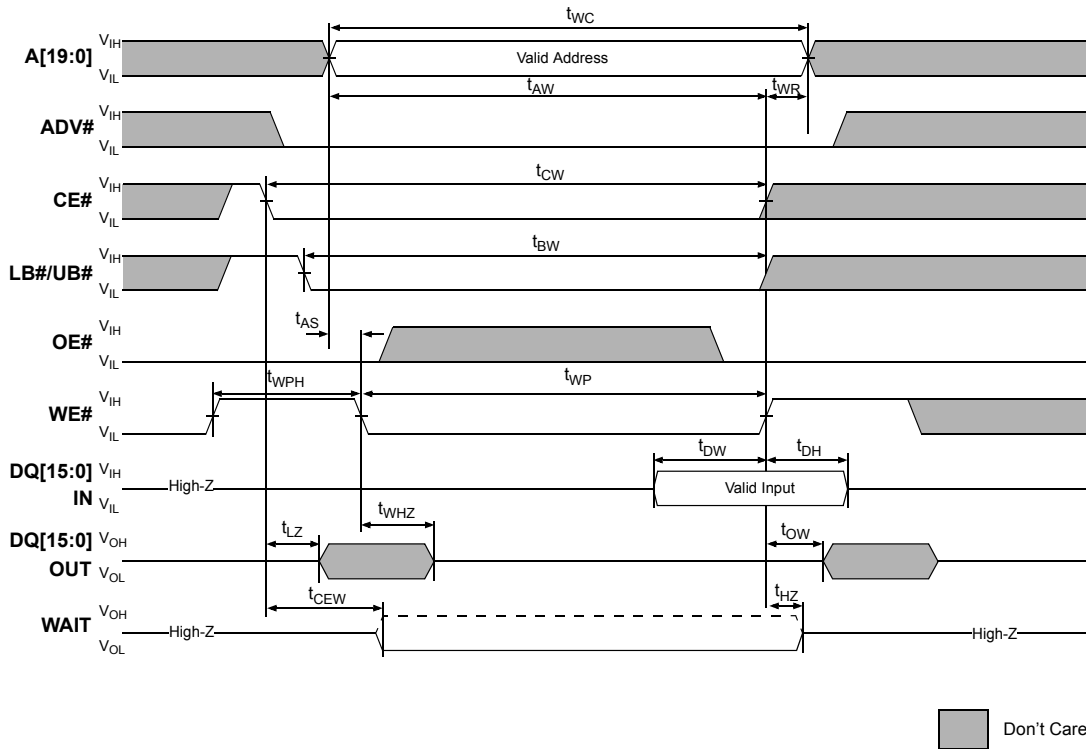
Figure 37. WE#-Controlled Asynchronous WRITE

Don't Care

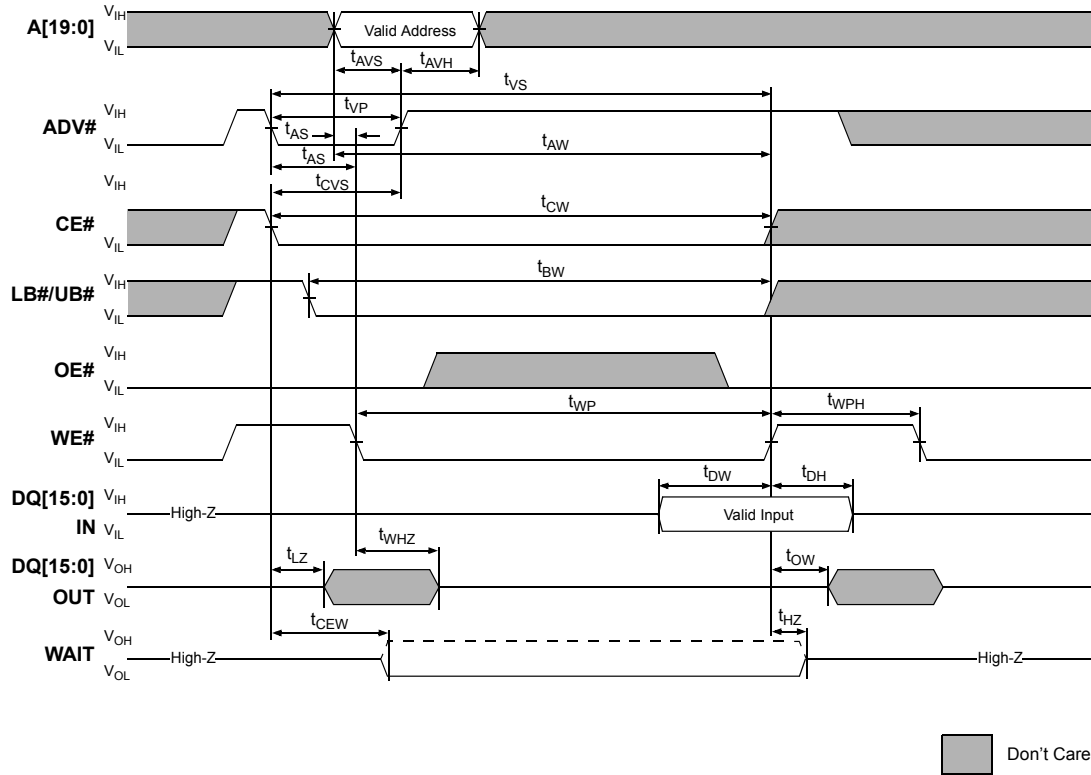**Figure 38. Asynchronous WRITE Using ADV#**

Figure 39. Burst WRITE Operation - Variable Latency Mode

WRITE Burst Identified
(WE# = Low)

Don't Care

Note:
1. Non-default BCR settings for burst WRITE operation in variable latency mode: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay; burst length four; burst wrap enabled.
2. WAIT asserts for LC cycles for both fixed and variable latency. LC = Latency Code (BCR[13:11]).
3. t_{AS} required if t_{CSP} > 20ns.

Figure 40. Burst WRITE Operation - Fixed Latency Mode

WRITE Burst Identified
(WE# = Low)

Don't Care
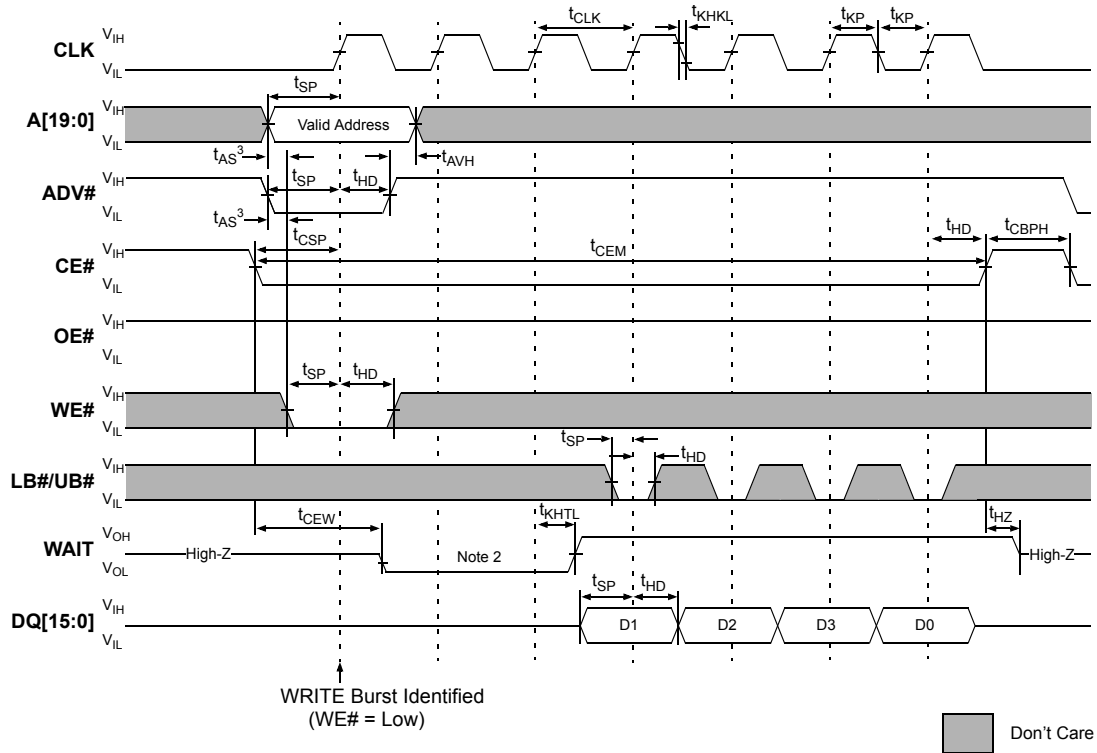
Note:
1. Non-default BCR settings for burst WRITE operation in fixed latency mode: Fixed latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay; burst length four; burst wrap enabled.
2. WAIT asserts for LC cycles for both fixed and variable latency. LC = Latency Code (BCR[13:11]).
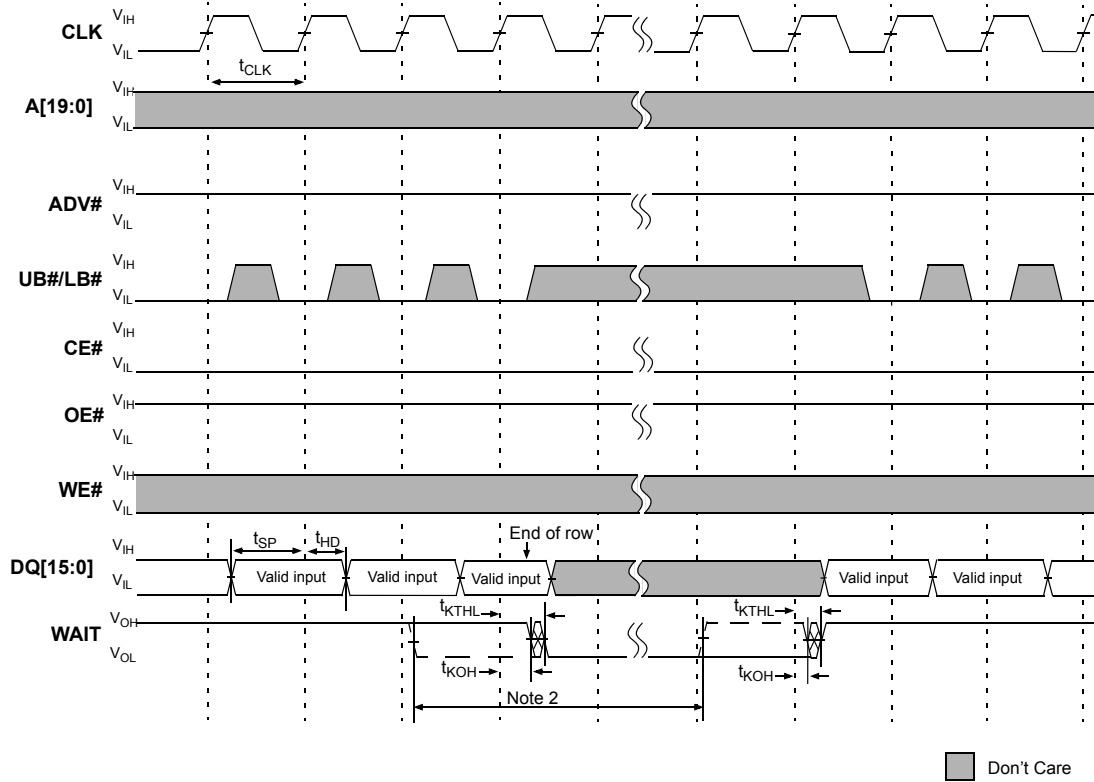3. t_{AS} required if t_{CSP} > 20ns.

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Figure 41. Burst WRITE at End-of-Row (Wrap Off)
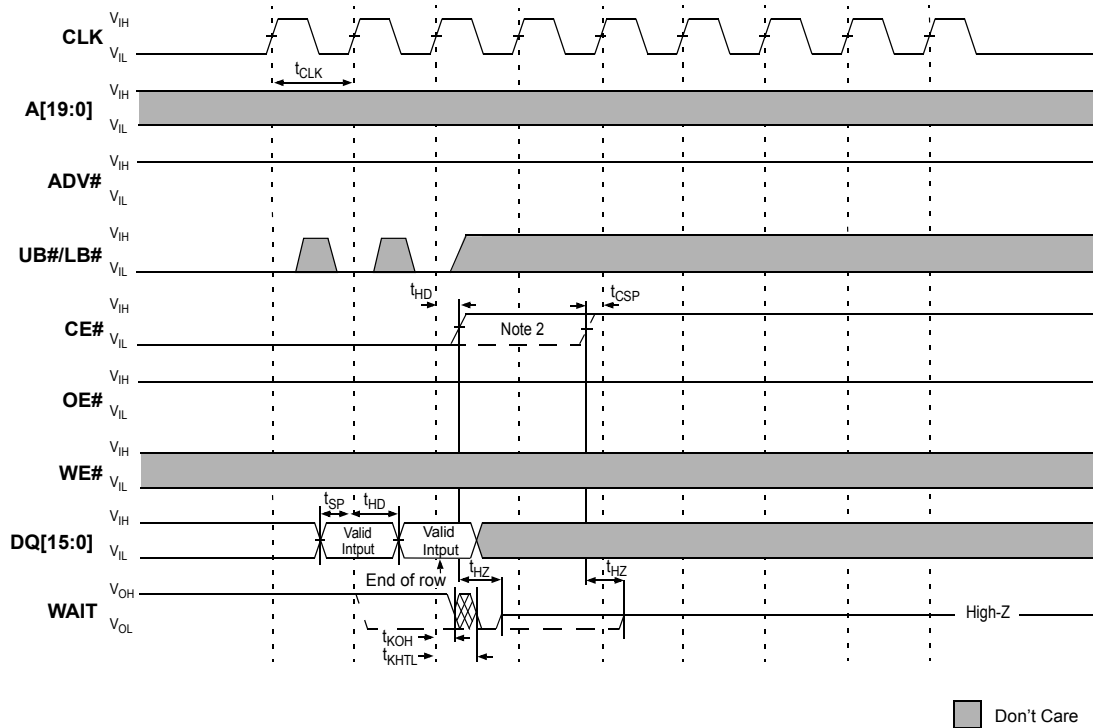
Note:
1. Non-default BCR settings for burst WRITE at end of row: fixed or variable latency, WAIT active LOW, WAIT asserted during delay. (shown as solid line)
2. For burst WRITEs, CE# must go HIGH before the second CLK after the WAIT period begins(before the second CLK after WAIT asserts with BCR[8]=0, or before the third CLK after WAIT asserts with BCR[8]=1).
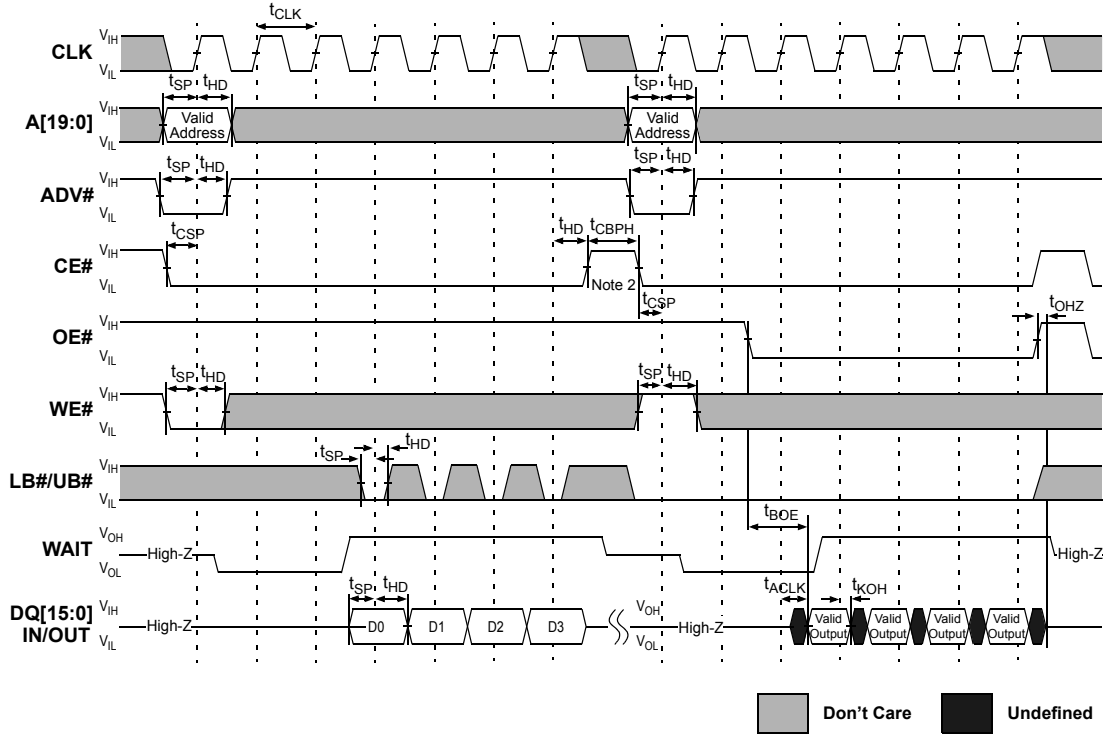
Figure 42. Burst WRITE Row boundary crossing

Don't Care

Note:
1. Non-default BCR settings for burst WRITE at end of row : Fixed or variable latency, WAIT active LOW, WAIT asserted during delay. (shown as solid line)
2. WAIT will be assert for LC cycles for variables latency, or LC cycles for fixed latency.
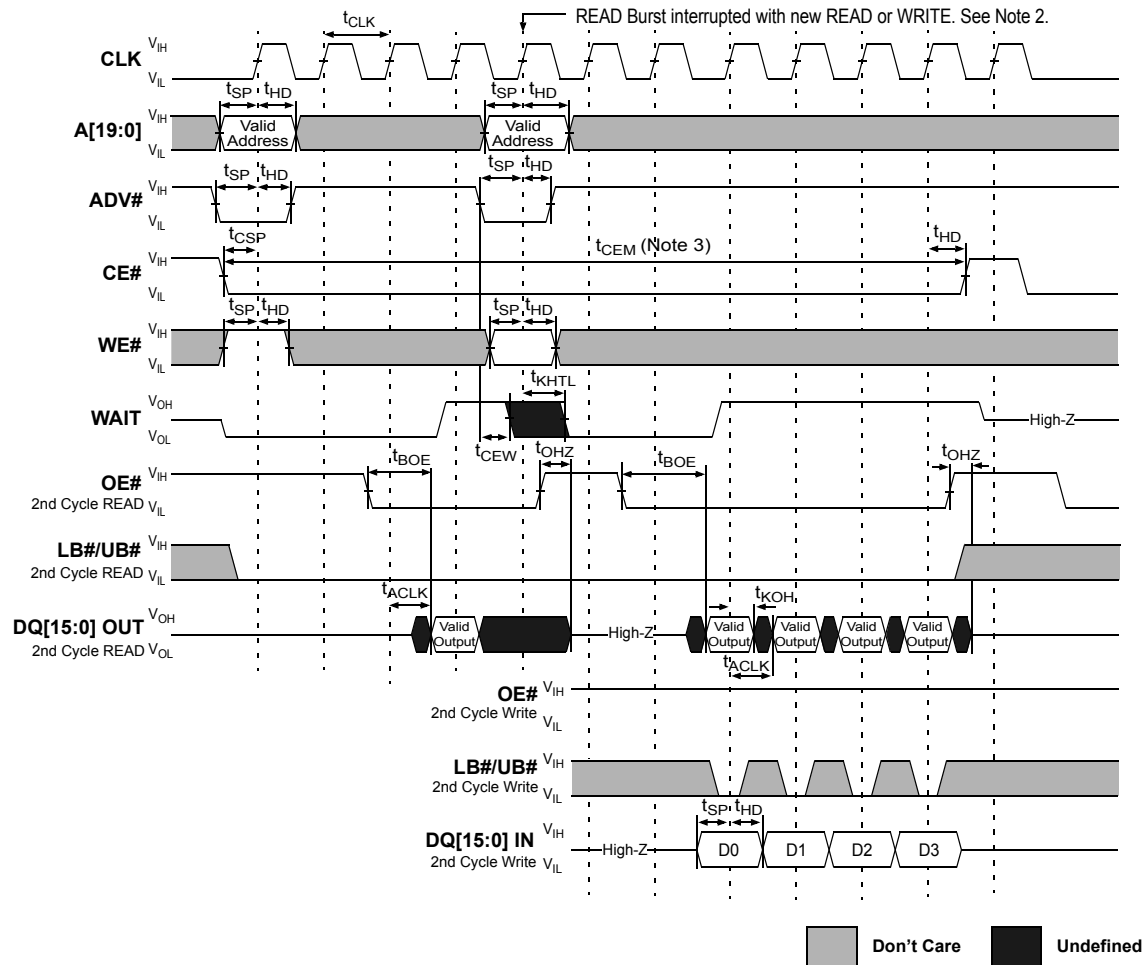
Figure 43. Burst WRITE Followed by Burst READ

Note:
1. Non-default BCR settings for burst WRITE followed by burst READ: Fixed or variable latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. A refresh opportunity must be provided every t_{CEM}. A refresh opportunity is satisfied by either of the following two conditions: a) clocked CE# HIGH, or b) CE# HIGH for longer than 15ns. CE# can stay LOW between burst READ and burst WRITE operations, but CE# must not remain LOW longer than t_{CEM}. See burst interrupt diagrams for cases where CE# stays LOW between bursts.

Figure 44. Burst READ Interrupted by Burst READ or WRITE

READ Burst interrupted with new READ or WRITE. See Note 2.

CLK

A[19:0]

ADV#

CE#

WE#

WAIT

OE#
2nd Cycle READ

LB#/UB#
2nd Cycle READ

DQ[15:0] OUT
2nd Cycle READ

OE#
2nd Cycle Write

LB#/UB#
2nd Cycle Write

DQ[15:0] IN
2nd Cycle Write

Don't Care   Undefined

Note:
1. Non-default BCR settings for burst READ interrupted by burst READ or WRITE: Fixed or variable latency code two (three clocks); WAIT active LOW; WAIT asserted during delay. All bursts shown for variable latency; no refresh collision.
2. Burst interrupt shown on first allowable clock (i.e., after the first data received by the controller).
3. CE# can stay LOW between burst operations, but CE# must not remain LOW longer than t_{CEM}.

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Figure 45. Burst WRITE Interrupted by Burst WRITE or READ - Variable Latency Mode
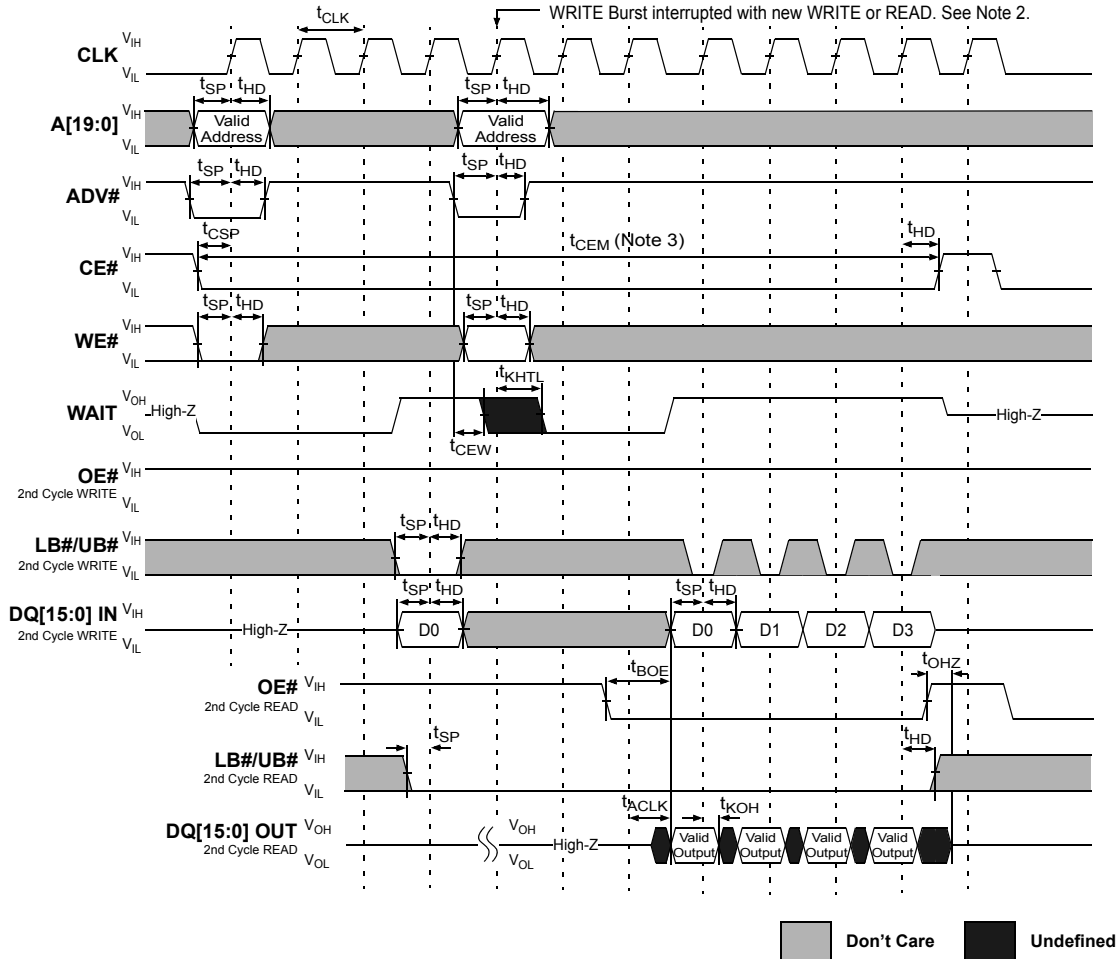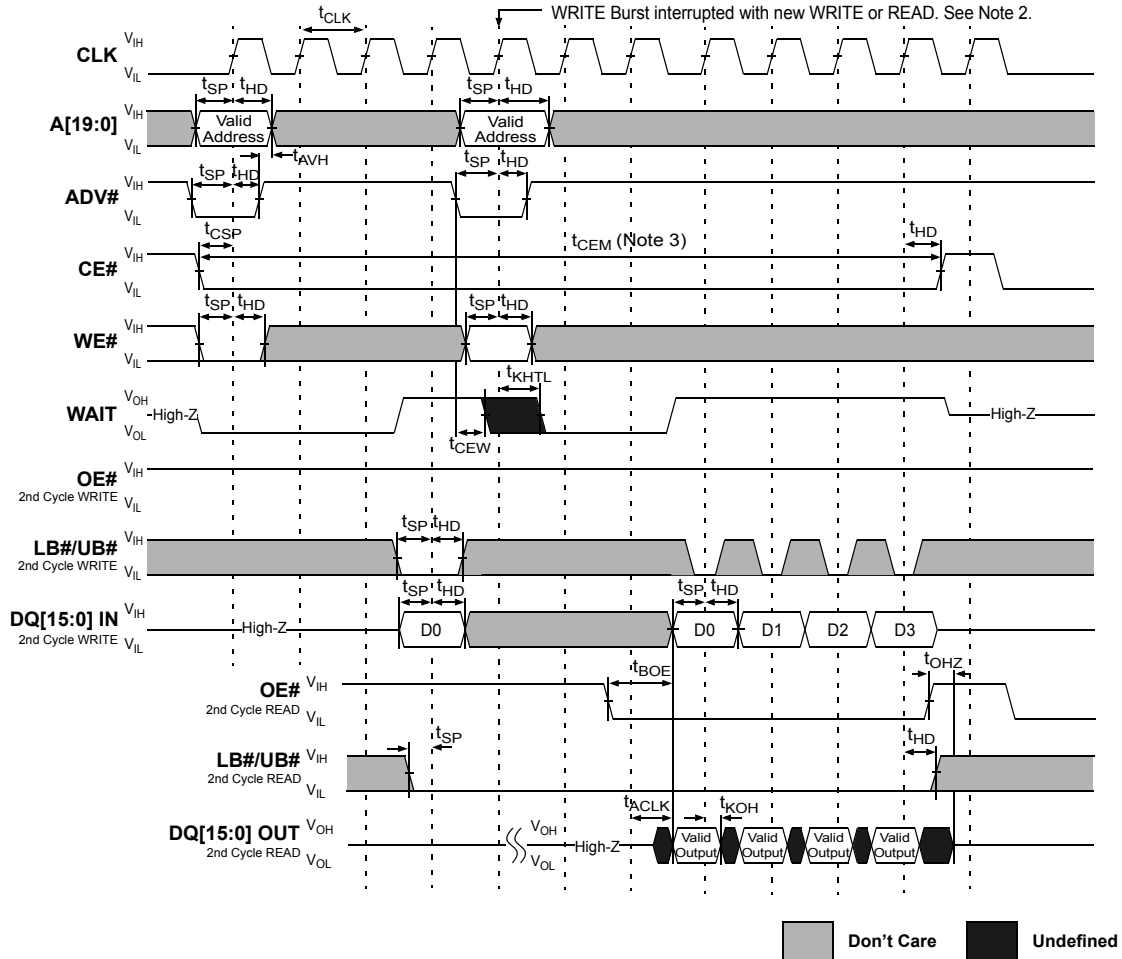

Note:
1. Non-default BCR settings for burst WRITE interrupted by burst WRITE or READ in variable latency mode: Variable latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay. All bursts shown for variable latency; no refresh collision.
2. Burst interrupt shown on first allowable clock (i.e., after first data word written).
3. CE# can stay LOW between burst operations, but CE# must not remain LOW longer than t_{CEM}.

Figure 46. Burst WRITE Interrupted by Burst WRITE or READ - Fixed Latency Mode

Note:
1. Non-default BCR settings for burst WRITE interrupted by burst WRITE or READ in fixed latency mode: Fixed latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. Burst interrupt shown on first allowable clock (i.e., after first data word written).
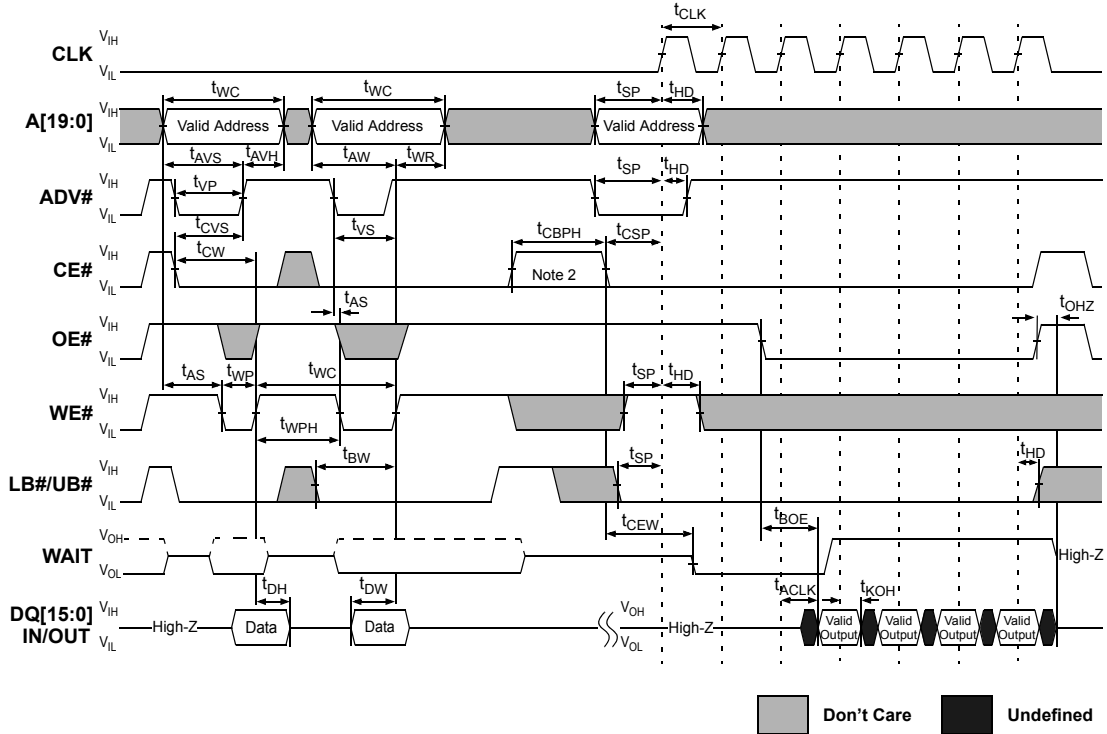3. CE# can stay LOW between burst operations, but CE# must not remain LOW longer than t_{CEM}.

Figure 47. Asynchronous WRITE Followed by Burst READ

Note:
1. Non-default BCR settings for asynchronous WRITE followed by burst READ: Fixed or variable latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. When transitioning between asynchronous and variable-latency burst operations, CE# must go HIGH. CE# can stay LOW when transitioning to fixed-latency burst READs. A refresh opportunity must be provided every t_{CEM}. A refresh opportunity is satisfied by either of the following two conditions: a) clocked CE# HIGH, or b) CE# HIGH for longer than 15ns.

Figure 48. Asynchronous WRITE (ADV# LOW) Followed By Burst READ
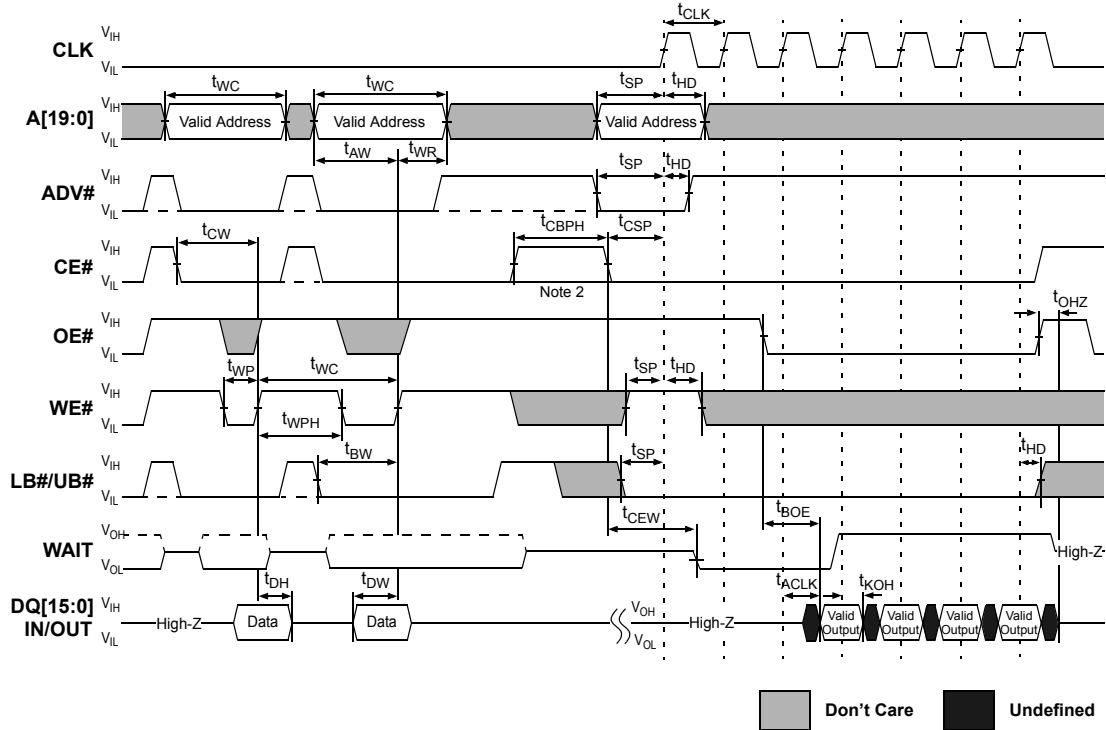
Note:
1. Non-default BCR settings for asynchronous WRITE, with ADV# LOW, followed by burst READ: Fixed or variable latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. When transitioning between asynchronous and variable-latency burst operations, CE# must go HIGH. CE# can stay LOW when transitioning to fixed-latency burst READs. A refresh opportunity must be provided every t_{CEM}. A refresh opportunity is satisfied by either of the following two conditions: a) clocked CE# HIGH, or b) CE# HIGH for longer than 15ns.
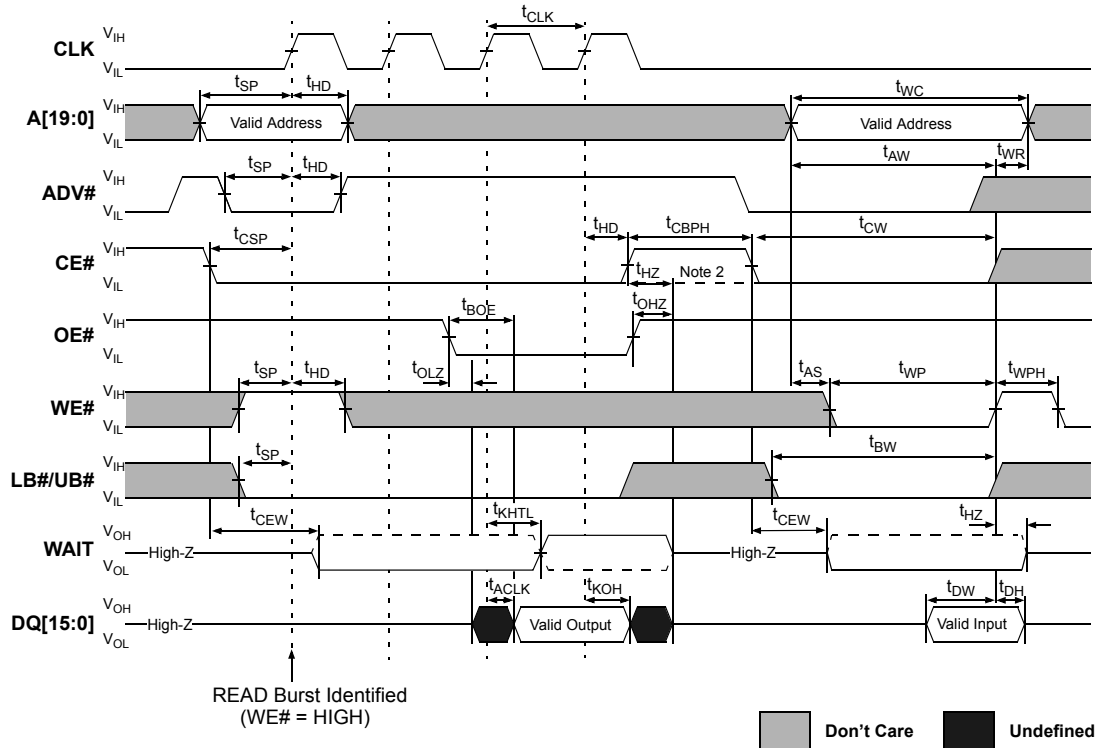
Figure 49. Burst READ Followed by Asynchronous WRITE (WE#-Controlled)

Note:
1. Non-default BCR settings for burst READ followed by asynchronous WE#-controlled WRITE: Fixed or variable latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. When transitioning between asynchronous and variable-latency burst operations, CE# must go HIGH. CE# can stay LOW when transitioning from fixed-latency burst READs; asynchronous operation begins at the falling edge of ADV#. A refresh opportunity must be provided every t_{CEM}. A refresh opportunity is satisfied by either of the following two conditions: a) clocked CE# HIGH, or b) CE# HIGH for longer than 15ns.
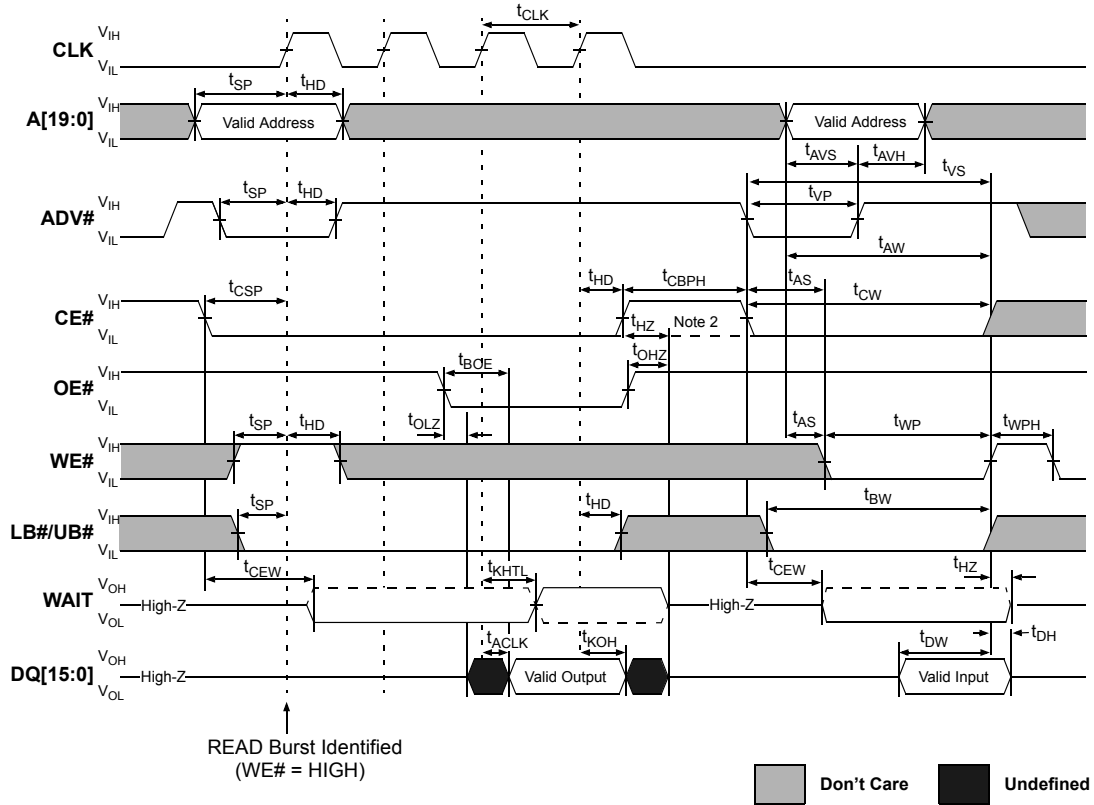
Figure 50. Burst READ Followed by Asynchronous WRITE Using ADV#

READ Burst Identified
(WE# = HIGH)

| Don't Care | | Undefined |

Note:
1. Non-default BCR settings for burst READ followed by asynchronous WRITE using ADV#: Fixed or variable latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. When transitioning between asynchronous and variable-latency burst operations, CE# must go HIGH. CE# can stay LOW when transitioning from fixed-latency burst READs; asynchronous operation begins at the falling edge of ADV#. A refresh opportunity must be provided every t_{CEM}. A refresh opportunity is satisfied by either of the following two conditions: a) clocked CE# HIGH, or b) CE# HIGH for longer than 15ns.
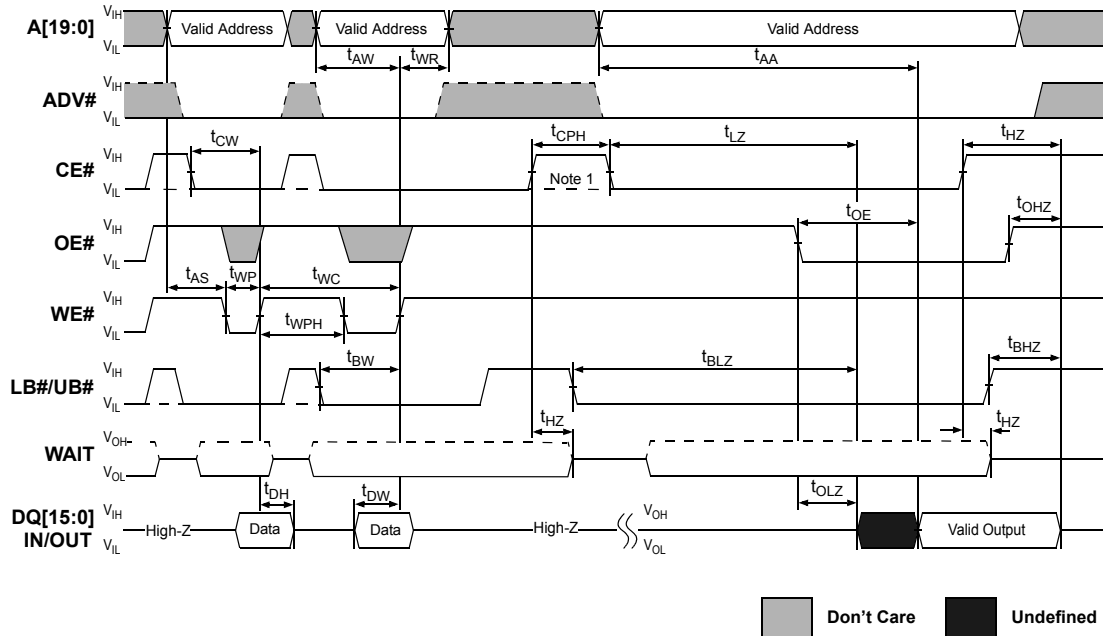
Figure 51. Asynchronous WRITE Followed by Asynchronous READ - ADV# LOW

Note:
1. When configured for synchronous mode (BCR[15] = 0), CE# must remain HIGH for at least 5ns (t_{CPH}) to schedule the appropriate refresh interval. Otherwise, t_{CPH} is only required after CE#-controlled WRITEs.

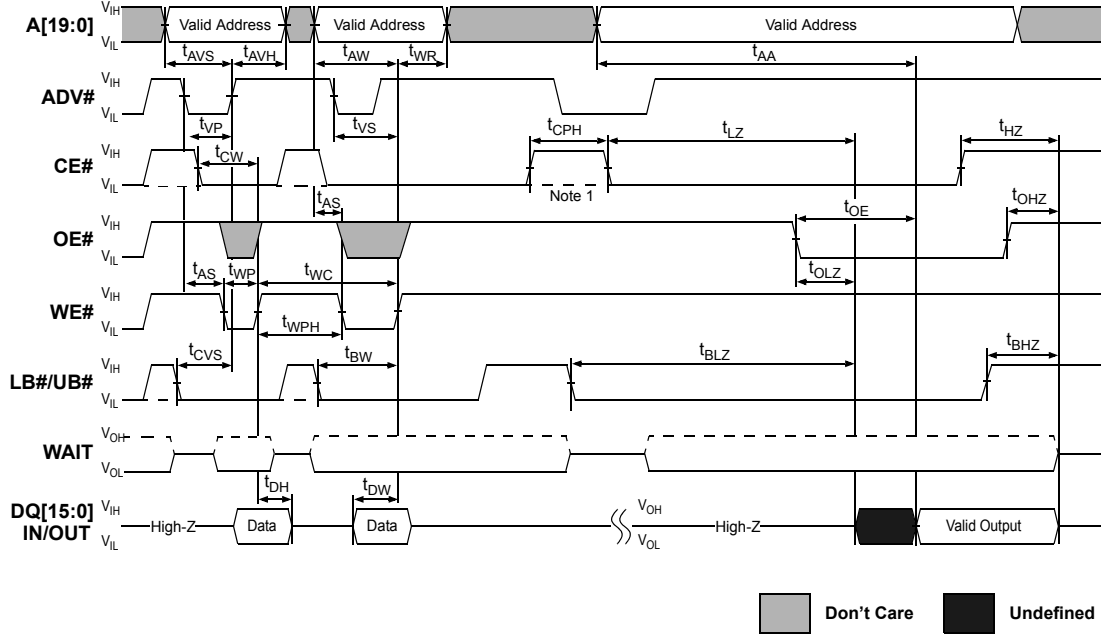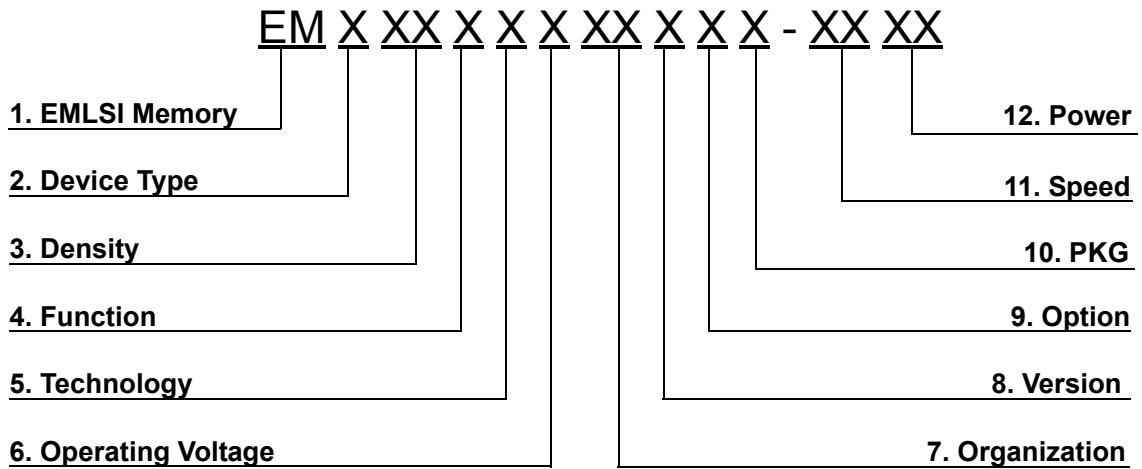**Figure 52. Asynchronous WRITE Followed by Asynchronous READ**

Note:
1. When configured for synchronous mode (BCR[15] = 0), CE# must remain HIGH for at least 5ns (t_{CPH}) to schedule the appropriate refresh
   interval. Otherwise, t_{CPH} is only required after CE#-controlled WRITEs.

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MEMORY FUNCTION GUIDE

EM X XX X X X XX X X X - XX XX

1. EMLSI Memory

2. Device Type

3. Density

4. Function

5. Technology

6. Operating Voltage

12. Power

11. Speed

10. PKG

9. Option

8. Version

7. Organization

1. Memory Component

2. Device Type
- 6 ---------------------- Low Power SRAM
- 7 ---------------------- STRAM
- C --------------------- CellularRAM

3. Density
- 4 ----------------------- 4M
- 8 ---------------------- 8M
- 16 --------------------- 16M
- 32 --------------------- 32M
- 64 --------------------- 64M
- 28 --------------------- 128M

4. Function
- 2 ----Multiplexed async.
- 3-----Multiplexed sync.
- 4-----Demultiplexed async.
- 5-----Multiplexed sync.
- 6-----Demultiplexed sync.

5. Technology
- S ----------------------- Single Transistor

6. Operating Voltage
- V ----------------------- 3.3V
- U ----------------------- 3.0V
- S ---------------------- 2.5V
- R ---------------------- 2.0V
- P ---------------------- 1.8V
- L ---------------------- 1.5V

7. Organization
- 8 ---------------------- x8 bit
- 16 ---------------------- x16 bit
- 32 ---------------------- x32 bit

8. Version
- Blank ----------------- Mother die
- A ---------------------- 2'nd generation
- B ---------------------- 3'rd generation
- C ---------------------- 4'th generation
- D ---------------------- 5'th generation

9. Option
- Blank ---- No optional mode
- J ------------ Non-RBC
- K ------------ RBC
- L ------------ 8 page mode / DPD
- M ------------8 page mode Non-DPD
- N -----------16 page mode / DPD
- P ------------ 16 page mode / Non-DPD
- R -------------DPD / Non-page mode
- S ------------ Non-DPD/ Non-page mode

10. Package
- Blank --------------------- Wafer
- S   --------------------- 32 sTSOP1
- T   --------------------- 32 TSOP1
- U   --------------------- 44 TSOP2
- P   --------------------- 48 FPBGA
- Z   --------------------- 52 FPBGA
- Y   --------------------- 54 FPBGA
- W   --------------------- 60 FPBGA
- V   --------------------- 90 FPBGA

11. Speed (@async.)
- 45 ---------------------- 45ns
- 55 ---------------------- 55ns
- 70 ---------------------- 70ns
- 85 ---------------------- 85ns
- 90 ---------------------- 90ns
- 10 -------------------- 100ns
- 12 -------------------- 120ns

12. Power
- LL --------------------- Low Low Power
- LF --------------------- Low Low Power
              (Pb-Free&Green)
- L --------------------- Low Power
- S --------------------- Standard Power