

1°C Temperature Sensor with Beta Compensation and Selectable Address

PRODUCT FEATURES

Datasheet

General Description

The EMC1413 and EMC1414 are high accuracy, low cost, System Management Bus (SMBus) temperature sensors. Advanced features such as Resistance Error Correction (REC), Beta Compensation (to support CPU diodes requiring the BJT/transistor model including 45nm, 65nm and 90nm processors) and automatic diode type detection combine to provide a robust solution for complex environmental monitoring applications.

Each device provides $\pm 1^\circ$ accuracy for external diode temperatures and $\pm 2^\circ\text{C}$ accuracy for the internal diode temperature. The EMC1413 monitors three temperature channels (two external and one internal). The EMC1414 monitors four temperature channels (three external and one internal).

Resistance Error Correction automatically eliminates the temperature error caused by series resistance allowing greater flexibility in routing thermal diodes. Beta Compensation eliminates temperature errors caused by low, variable beta transistors common in today's fine geometry processors. The automatic beta detection feature monitors each external diode/transistor and determines the optimum sensor settings for accurate temperature measurements regardless of processor technology. This frees the user from providing unique sensor configurations for each temperature monitoring application. These advanced features plus $\pm 1^\circ\text{C}$ measurement accuracy provide a low-cost, highly flexible and accurate solution for critical temperature monitoring applications.

Applications

- Notebook Computers
- Desktop Computers
- Industrial
- Embedded applications

Features

- Programmable SMBus Address
- Support for diodes requiring the BJT/transistor model
 - supports 45nm, 65nm, and 90nm CPU thermal diodes.
- Automatically determines external diode type and optimal settings
- Resistance Error Correction
- External Temperature Monitors
 - $\pm 1^\circ\text{C}$ Accuracy ($60^\circ\text{C} < T_{\text{DIODE}} < 100^\circ\text{C}$)
 - 0.125°C Resolution
 - Anti-parallel diodes for extra diode support
- Internal Temperature Monitor
 - $\pm 2^\circ\text{C}$ accuracy
- 3.3V Supply Voltage
- Programmable temperature limits for ALERT and THERM
- Available in these Lead-free RoHS Compliant Packages
 - 10-pin 3mm x 3mm DFN
 - 10-pin MSOP

ORDER NUMBER(S):

EMC1413-1-AIZL-TR FOR 10-PIN MSOP LEAD-FREE ROHS COMPLIANT PACKAGE
EMC1413-A-AIZL-TR FOR 10-PIN MSOP LEAD-FREE ROHS COMPLIANT PACKAGE
EMC1413-3-AIZL-TR FOR 10-PIN MSOP LEAD-FREE ROHS COMPLIANT PACKAGE
EMC1413-A-AIA-TR FOR 10-PIN DFN LEAD-FREE ROHS COMPLIANT PACKAGE
EMC1414-1-AIZL-TR FOR 10-PIN MSOP LEAD-FREE ROHS COMPLIANT PACKAGE
EMC1414-A-AIZL-TR FOR 10-PIN MSOP LEAD-FREE ROHS COMPLIANT PACKAGE
EMC1414-3-AIZL-TR FOR 10-PIN MSOP LEAD-FREE ROHS COMPLIANT PACKAGE
EMC1414-A-AIA-TR FOR 10-PIN DFN LEAD-FREE ROHS COMPLIANT PACKAGE

Note: See [Table 1.1](#), "Part Selection" for SMBus addressing options.

REEL SIZE IS 4,000 PIECES.

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smSC.com/rohs



80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000, FAX (631) 273-3123

Copyright © 2009 SMSC or its subsidiaries. All rights reserved.

Circuit diagrams and other information relating to SMSC products are included as a means of illustrating typical applications. Consequently, complete information sufficient for construction purposes is not necessarily given. Although the information has been checked and is believed to be accurate, no responsibility is assumed for inaccuracies. SMSC reserves the right to make changes to specifications and product descriptions at any time without notice. Contact your local SMSC sales office to obtain the latest specifications before placing your product order. The provision of this information does not convey to the purchaser of the described semiconductor devices any licenses under any patent rights or other intellectual property rights of SMSC or others. All sales are expressly conditional on your agreement to the terms and conditions of the most recently dated version of SMSC's standard Terms of Sale Agreement dated before the date of your order (the "Terms of Sale Agreement"). The product may contain design defects or errors known as anomalies which may cause the product's functions to deviate from published specifications. Anomaly sheets are available upon request. SMSC products are not designed, intended, authorized or warranted for use in any life support or other application where product failure could cause or contribute to personal injury or severe property damage. Any and all such uses without prior written approval of an Officer of SMSC and further testing and/or modification will be fully at the risk of the customer. Copies of this document or other SMSC literature, as well as the Terms of Sale Agreement, may be obtained by visiting SMSC's website at <http://www.smSC.com>. SMSC is a registered trademark of Standard Microsystems Corporation ("SMSC"). Product names and company names are the trademarks of their respective holders.

SMSC DISCLAIMS AND EXCLUDES ANY AND ALL WARRANTIES, INCLUDING WITHOUT LIMITATION ANY AND ALL IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, TITLE, AND AGAINST INFRINGEMENT AND THE LIKE, AND ANY AND ALL WARRANTIES ARISING FROM ANY COURSE OF DEALING OR USAGE OF TRADE. IN NO EVENT SHALL SMSC BE LIABLE FOR ANY DIRECT, INCIDENTAL, INDIRECT, SPECIAL, PUNITIVE, OR CONSEQUENTIAL DAMAGES; OR FOR LOST DATA, PROFITS, SAVINGS OR REVENUES OF ANY KIND; REGARDLESS OF THE FORM OF ACTION, WHETHER BASED ON CONTRACT; TORT; NEGLIGENCE OF SMSC OR OTHERS; STRICT LIABILITY; BREACH OF WARRANTY; OR OTHERWISE; WHETHER OR NOT ANY REMEDY OF BUYER IS HELD TO HAVE FAILED OF ITS ESSENTIAL PURPOSE, AND WHETHER OR NOT SMSC HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Table of Contents

Chapter 1	Block Diagram	7
1.1	Part Selection	7
Chapter 2	Pin Description	8
Chapter 3	Electrical Specifications	10
3.1	Absolute Maximum Ratings	10
3.2	Electrical Specifications	11
3.3	SMBus Electrical Characteristics	12
Chapter 4	System Management Bus Interface Protocol	13
4.1	System Management Bus Interface Protocol	13
4.2	Write Byte	13
4.3	Read Byte	14
4.4	Send Byte	14
4.5	Receive Byte	14
4.6	Alert Response Address	14
4.7	SMBus Address	15
4.8	SMBus Timeout	15
Chapter 5	Product Description	16
5.1	Modes of Operation	17
5.1.1	Conversion Rates	17
5.1.2	Dynamic Averaging	17
5.2	THERM Output	19
5.2.1	THERM Pin Considerations	19
5.3	ALERT Output	19
5.3.1	ALERT Pin Interrupt Mode	20
5.3.2	ALERT Pin Comparator Mode	20
5.4	Beta Compensation	20
5.5	Resistance Error Correction (REC)	20
5.6	Programmable External Diode Ideality Factor	20
5.7	Diode Faults	21
5.8	Consecutive Alerts	21
5.9	Digital Filter	21
5.10	Temperature Monitors	23
5.11	Temperature Measurement Results and Data	23
5.12	Anti-parallel Diode Connections	24
5.13	External Diode Connections	24
Chapter 6	Register Description	25
6.1	Data Read Interlock	28
6.2	Temperature Data Registers	28
6.3	Status Register	29
6.4	Configuration Register	29
6.5	Conversion Rate Register	30
6.6	Limit Registers	31
6.7	Scratchpad Registers	33
6.8	One Shot Register	33
6.9	Therm Limit Registers	33
6.10	External Diode Fault Register	34

6.11	Channel Mask Register	34
6.12	Consecutive ALERT Register	35
6.13	Beta Configuration Registers	36
6.14	External Diode Ideality Factor Registers	37
6.15	High Limit Status Register	39
6.16	Low Limit Status Register	39
6.17	THERM Limit Status Register	40
6.18	Filter Control Register	40
6.19	Product ID Register	41
6.20	SMSC ID Register (FEh)	41
6.21	Revision Register (FFh)	41

Chapter 7 Typical Operating Curves..... **42**

Chapter 8 Package Information..... **44**

8.1	Package Markings	47
-----	------------------	----

Chapter 9 Revision History..... **50**

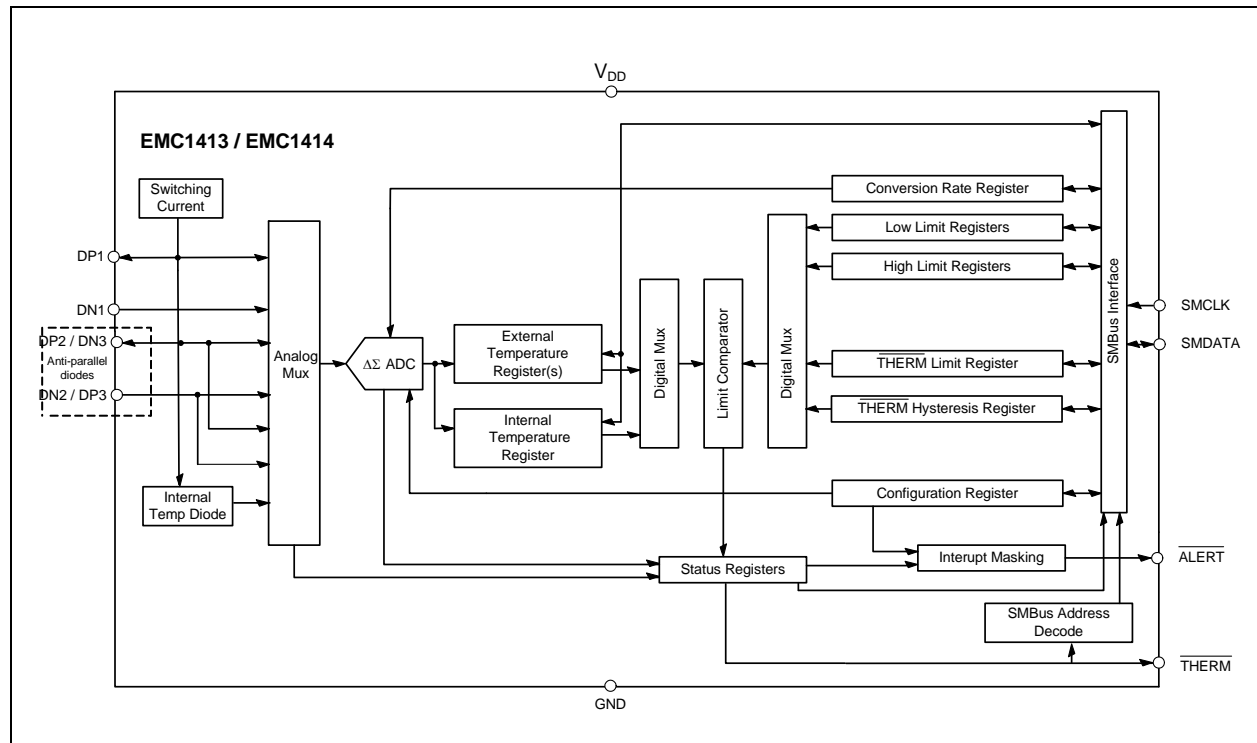
List of Figures

Figure 2.1	EMC1413/EMC1414 Pin Diagram, MSOP-10	8
Figure 2.2	EMC1413/EMC1414 Pin Diagram, DFN-10	8
Figure 4.1	SMBus Timing Diagram	13
Figure 5.1	System Diagram for EMC1413	16
Figure 5.2	System Diagram for EMC1414	17
Figure 5.3	Isolating THERM Pin	19
Figure 5.4	Temperature Filter Step Response	22
Figure 5.5	Temperature Filter Impulse Response	22
Figure 5.6	Diode Configurations	24
Figure 8.1	10 Pin MSOP / TSSOP Package	44
Figure 8.2	10 Pin DFN Package Drawing	45
Figure 8.3	10 Pin DFN Package Dimensions	46
Figure 8.4	10 Pin DFN PCB Footprint	46
Figure 8.5	EMC1413-AIZL Package Marking for 10 Pin MSOP	47
Figure 8.6	EMC1413-A-AIA Package Marking for 10 Pin DFN	48
Figure 8.7	EMC1414 Package Marking	48
Figure 8.8	EMC1414-A-AIA Package Marking for 10 Pin DFN	49

List of Tables

Table 1.1	Part Selection	7
Table 2.1	EMC1413 and EMC1414 Pin Description	8
Table 3.1	Absolute Maximum Ratings	10
Table 3.2	Electrical Specifications	11
Table 3.3	SMBus Electrical Specifications	12
Table 4.1	Protocol Format	13
Table 4.2	Write Byte Protocol	13
Table 4.3	Read Byte Protocol	14
Table 4.4	Send Byte Protocol	14
Table 4.5	Receive Byte Protocol	14
Table 4.6	Alert Response Address Protocol	14
Table 4.7	SMBus Address Decode	15
Table 5.1	Supply Current vs. Conversion Rate for EMC1413	18
Table 5.2	Supply Current vs. Conversion Rate for EMC1414	18
Table 5.3	EMC1413 and EMC1414 Temperature Data Format	23
Table 6.1	Register Set in Hexadecimal Order	25
Table 6.2	Temperature Data Registers	28
Table 6.3	Status Register	29
Table 6.4	Configuration Register	29
Table 6.5	Conversion Rate Register	30
Table 6.6	Conversion Rate	31
Table 6.7	Temperature Limit Registers	31
Table 6.8	Scratchpad Register	33
Table 6.9	One Shot Register	33
Table 6.10	Therm Limit Registers	33
Table 6.11	External Diode Fault Register	34
Table 6.12	Channel Mask Register	34
Table 6.13	Consecutive ALERT Register	35
Table 6.14	Consecutive Alert / THERM Settings	36
Table 6.15	Beta Configuration Registers	36
Table 6.16	CPU Beta Values	37
Table 6.17	Ideality Configuration Registers	37
Table 6.18	Ideality Factor Look-Up Table (Diode Model)	38
Table 6.19	Substrate Diode Ideality Factor Look-Up Table (BJT Model)	38
Table 6.20	High Limit Status Register	39
Table 6.21	Low Limit Status Register	39
Table 6.22	THERM Limit Status Register	40
Table 6.23	Filter Configuration Register	40
Table 6.24	Filter Settings	41
Table 6.25	Product ID Register	41
Table 6.26	Manufacturer ID Register	41
Table 6.27	Revision Register	41
Table 9.1	Customer Revision History	50

Chapter 1 Block Diagram



1.1 Part Selection

The EMC1413 and EMC1414 device configuration is highlighted below.

Table 1.1 Part Selection

PART NUMBER	SMBUS ADDRESS	PACKAGE	FUNCTIONALITY				PRODUCT ID
			EXT DIODES	DIODE 1 CONFIG	DIODE 2 CONFIG	OTHER	
EMC1413 - 1 - AIZL	1001_100xb	10-pin MSOP	2	Detect Diode w/ REC enabled	Detect Diode w/ REC enabled	Software program- mable and mask- able High Limits	21h
EMC1413 - A - AIZL	See Table 4.7					Software program- mable THERM Limits	
EMC1413 - 3 - AIZL	0011_000xb						
EMC1413 - A - AIA	See Table 4.7	10-pin DFN 3mm x 3mm	3	Detect Diode w/ REC enabled	Fixed 2N3904 in anti-parallel diode configuration Note 1.1	Software program- mable and mask- able High Limits	25h
EMC1414 - 1 - AIZL	1001_100xb	Software program- mable THERM Limits					
EMC1414 - A - AIZL	See Table 4.7						
EMC1414 - 3 - AIZL	0011_000xb						
EMC1414 - A - AIA	See Table 4.7	10-pin DFN 3mm x 3mm					

Note 1.1 External 2 and external 3 channels have beta configuration hard wired to '0111b' and REC enabled.

Chapter 2 Pin Description

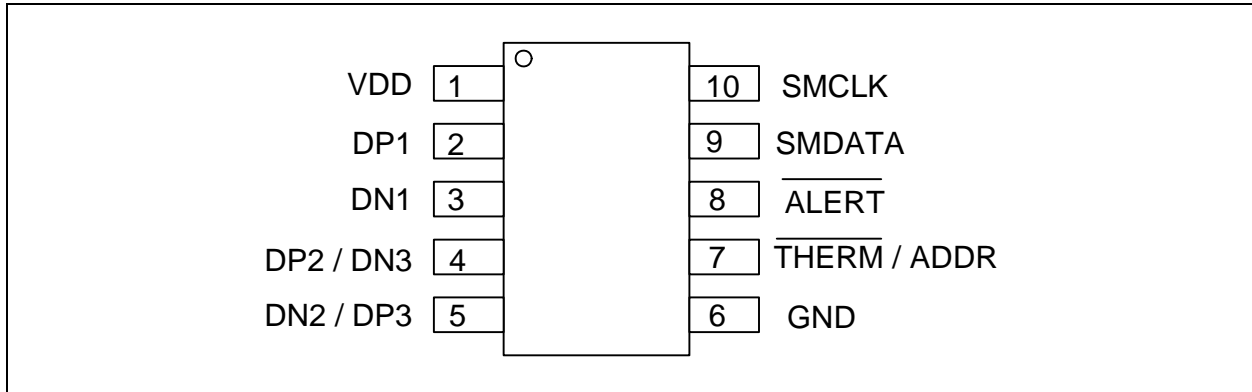


Figure 2.1 EMC1413/EMC1414 Pin Diagram, MSOP-10

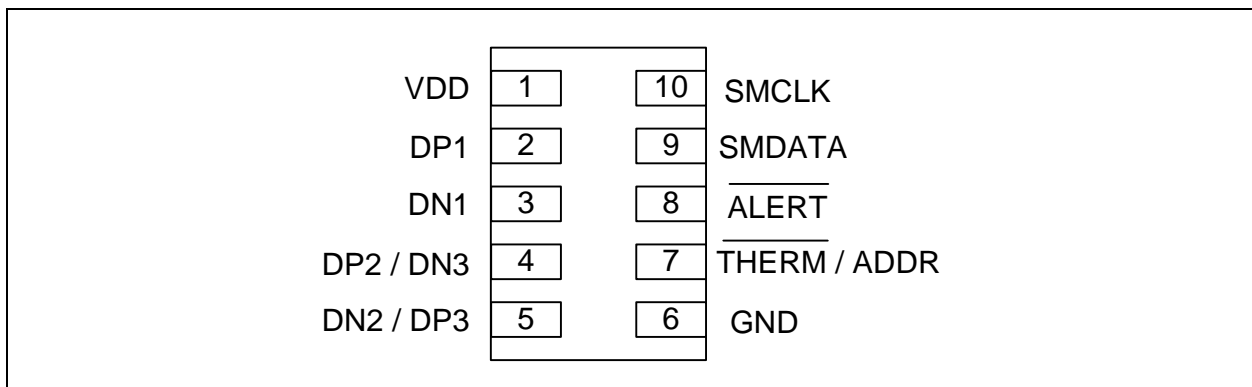


Figure 2.2 EMC1413/EMC1414 Pin Diagram, DFN-10

Table 2.1 EMC1413 and EMC1414 Pin Description

PIN NUMBER	NAME	FUNCTION	TYPE
1	VDD	Power supply	Power
2	DP1	External diode 1 positive (anode) connection	AIO
3	DN1	External diode 1 negative (cathode) connection	AIO
4	DP2 / DN3	External diode 2 positive (anode) connection / External Diode 3 negative (cathode) connection for anti-parallel diodes	AIO
5	DN2 / DP3	External diode 2 negative (cathode) connection / External Diode 3 positive (anode) connection for anti-parallel diodes	AIO

Table 2.1 EMC1413 and EMC1414 Pin Description (continued)

PIN NUMBER	NAME	FUNCTION	TYPE
6	GND	Ground	Power
7	$\overline{\text{THERM}}$ / ADDR	Critical $\overline{\text{THERM}}$ output signal - requires pull-up resistor to determine SMBus address	OD (5V)
8	$\overline{\text{ALERT}}$	Active low digital $\overline{\text{ALERT}}$ output signal - requires pull-up resistor	OD (5V)
9	SMDATA	SMBus Data input/output	DIOD (5V)
10	SMCLK	SMBus Clock input	DI (5V)

APPLICATION NOTE: For the 5V tolerant pins that have a pull-up resistor (SMCLK, SMDATA, $\overline{\text{THERM}}$, $\overline{\text{ALERT}}$), the voltage difference between VDD and the pull-up voltage must never exceed 3.6V.

The pin types are described below:

Power - these pins are used to supply either VDD or GND to the device.

AIO - Analog Input / Output.

DI - Digital Input.

OD - Open Drain Digital Output.

DIOD - Digital Input / Open Drain Output.

Chapter 3 Electrical Specifications

3.1 Absolute Maximum Ratings

Table 3.1 Absolute Maximum Ratings

DESCRIPTION	RATING	UNIT
Supply Voltage (V_{DD})	-0.3 to 4.0	V
Voltage on 5V tolerant pins (V_{5VT_pin})	-0.3 to 5.5	V
Voltage on 5V tolerant pins ($ V_{5VT_pin} - V_{DD} $) (see Note 3.1)	-0.3 to 3.6	V
Voltage on any other pin to Ground	-0.3 to $V_{DD} + 0.3$	V
Operating Temperature Range	-40 to +125	°C
Storage Temperature Range	-55 to +150	°C
Lead Temperature Range	Refer to JEDEC Spec. J-STD-020	
Package Thermal Characteristics for MSOP-10		
Thermal Resistance (θ_{j-a})	132.2	°C/W
Package Thermal Characteristics for DFN-10		
Thermal Resistance (θ_{j-a})	77.7	°C/W
ESD Rating, All pins HBM	2000	V

Note: Stresses at or above those listed could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied. When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

Note 3.1 For the 5V tolerant pins that have a pull-up resistor (\overline{SMCLK} , \overline{SMDATA} , \overline{THERM} , \overline{ALERT}), the pull-up voltage must not exceed 3.6V when the device is unpowered.

3.2 Electrical Specifications

Table 3.2 Electrical Specifications

V _{DD} = 3.0V to 3.6V, T _A = -40°C to 125°C, all typical values at T _A = 27°C unless otherwise noted.						
CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNITS	CONDITIONS
DC Power						
Supply Voltage	V _{DD}	3.0	3.3	3.6	V	
Supply Current	I _{DD}		430	850	µA	1 conversion / sec, dynamic averaging disabled
			930	1200	µA	4 conversions / sec, dynamic averaging enabled
			1120		µA	≥ 16 conversions / sec, dynamic averaging enabled
Standby Supply Current	I _{DD}		170	230	µA	Device in Standby mode, no SMBus communications, ALERT and THERM pins not asserted.
Power Up Time	t _{PUP}		10		ms	
Time to first data available	t _{CONV_1ST}			300	ms	
Internal Temperature Monitor						
Temperature Accuracy			±0.25	±1	°C	-5°C < T _A < 100°C
				±2	°C	-40°C < T _A < 125°C
Temperature Resolution			0.125		°C	
External Temperature Monitor						
Temperature Accuracy			±0.25	±1	°C	+20°C < T _{DIODE} < +110°C 0°C < T _A < 100°C
			±0.5	±2	°C	-40°C < T _{DIODE} < 127°C
Temperature Resolution			0.125		°C	
	t _{CONV}		190		ms	EMC1413, default settings
	t _{CONV}		150		ms	EMC1414, default settings
Capacitive Filter	C _{FILTER}		2.2	2.5	nF	Connected across external diode
ALERT and THERM pins						
Output Low Voltage	V _{OL}	0.4			V	I _{SINK} = 8mA
Leakage Current	I _{LEAK}			±5	µA	ALERT and THERM pins Device powered or unpowered T _A < 85°C pull-up voltage ≤ 3.6V

3.3 SMBus Electrical Characteristics

Table 3.3 SMBus Electrical Specifications

V _{DD} = 3.0V to 3.6V, T _A = -40°C to 125°C, all typical values are at T _A = 27°C unless otherwise noted.						
CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNITS	CONDITIONS
SMBus Interface						
Input High Voltage	V _{IH}	2.0		V _{DD}	V	5V Tolerant
Input Low Voltage	V _{IL}	-0.3		0.8	V	5V Tolerant
Input High/Low Current	I _{IH} / I _{IL}			±5	uA	Powered or unpowered TA < 85°C
Hysteresis			420		mV	
Input Capacitance	C _{IN}		5		pF	
Output Low Sink Current	I _{OL}	8.2		15	mA	SMDATA = 0.4V
SMBus Timing						
Clock Frequency	f _{SMB}	10		400	kHz	
Spike Suppression	t _{SP}			50	ns	
Bus free time Start to Stop	t _{BUF}	1.3			us	
Hold Time: Start	t _{HD:STA}	0.6			us	
Setup Time: Start	t _{SU:STA}	0.6			us	
Setup Time: Stop	t _{SU:STP}	0.6			us	
Data Hold Time	t _{HD:DAT}	0.3			us	
Data Setup Time	t _{SU:DAT}	100			ns	
Clock Low Period	t _{LOW}	1.3			us	
Clock High Period	t _{HIGH}	0.6			us	
Clock/Data Fall time	t _{FALL}			300	ns	Min = 20+0.1C _{LOAD} ns
Clock/Data Rise time	t _{RISE}			300	ns	Min = 20+0.1C _{LOAD} ns
Capacitive Load	C _{LOAD}			400	pF	per bus line

Chapter 4 System Management Bus Interface Protocol

4.1 System Management Bus Interface Protocol

The EMC1413 and EMC1414 communicate with a host controller, such as an SMSC SIO, through the SMBus. The SMBus is a two-wire serial communication protocol between a computer host and its peripheral devices. A detailed timing diagram is shown in Figure 4.1, "SMBus Timing Diagram"

For the first 15ms after power-up the device may not respond to SMBus communications.

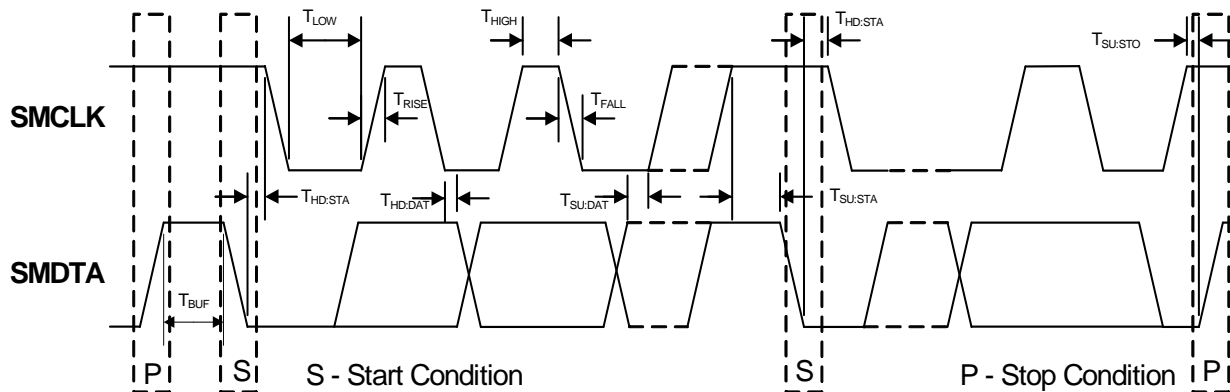


Figure 4.1 SMBus Timing Diagram

The EMC1413 and EMC1414 are SMBus 2.0 compatible and support Send Byte, Read Byte, Write Byte, Receive Byte, and the Alert Response Address as valid protocols as shown below.

All of the below protocols use the convention in Table 4.1, "Protocol Format".

Table 4.1 Protocol Format

DATA SENT TO DEVICE	DATA SENT TO THE HOST
# of bits sent	# of bits sent

Attempting to communicate with the EMC1413 and EMC1414 SMBus interface with an invalid slave address or invalid protocol will result in no response from the device and will not affect its register contents. Stretching of the SMCLK signal is supported, provided other devices on the SMBus control the timing.

4.2 Write Byte

The Write Byte is used to write one byte of data to the registers as shown below Table 4.2:

Table 4.2 Write Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	REGISTER DATA	ACK	STOP
1 -> 0	1001_100	0	0	XXh	0	XXh	0	0 -> 1

4.3 Read Byte

The Read Byte protocol is used to read one byte of data from the registers as shown in [Table 4.3](#).

Table 4.3 Read Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	START	SLAVE ADDRESS	RD	ACK	REGISTER DATA	NACK	STOP
1 -> 0	1001_100	0	1	XXh	0	1 -> 0	1001_100	1	1	XX	1	0 -> 1

4.4 Send Byte

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data is transferred during the Send Byte protocol as shown in [Table 4.4](#).

Table 4.4 Send Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	STOP
1 -> 0	1001_100	0	0	XXh	0	0 -> 1

4.5 Receive Byte

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g. set via Send Byte). This is used for consecutive reads of the same register as shown in [Table 4.5](#).

Table 4.5 Receive Byte Protocol

START	SLAVE ADDRESS	RD	ACK	REGISTER DATA	NACK	STOP
1 -> 0	1001_100	1	0	XXh	1	0 -> 1

4.6 Alert Response Address

The $\overline{\text{ALERT}}$ output can be used as a processor interrupt or as an SMBus Alert.

When it detects that the $\overline{\text{ALERT}}$ pin is asserted, the host will send the Alert Response Address (ARA) to the general address of 0001_100xb. All devices with active interrupts will respond with their client address as shown in [Table 4.6](#).

Table 4.6 Alert Response Address Protocol

START	ALERT RESPONSE ADDRESS	RD	ACK	DEVICE ADDRESS	NACK	STOP
1 -> 0	0001_100	1	0	1001_1000	1	0 -> 1

Datasheet

The EMC1413 and EMC1414 will respond to the ARA in the following way:

1. Send Slave Address and verify that full slave address was sent (i.e. the SMBus communication from the device was not prematurely stopped due to a bus contention event).
2. Set the MASK bit to clear the $\overline{\text{ALERT}}$ pin.

APPLICATION NOTE: The ARA does not clear the Status Register and if the MASK bit is cleared prior to the Status Register being cleared, the ALERT pin will be reasserted.

4.7 SMBus Address

The EMC1413-A and EMC1414-A SMBus slave address is determined by the pull-up resistor on the THERM pin as shown in [Table 4.7, "SMBus Address Decode"](#).

The Address decode is performed by pulling known currents from VDD through the external resistor causing the pin voltage to drop based on the respective current / resistor relationship. This pin voltage is compared against a threshold that determines the value of the pull-up resistor.

Table 4.7 SMBus Address Decode

PULL UP RESISTOR ON THERM PIN	SMBUS ADDRESS
4.7k	1111_100xb
6.8k	1011_100xb
10k	1001_100xb
15k	1101_100xb
22k	0011_100xb
33k	0111_100xb

The EMC1413 and EMC1414 -1 and -3 SMBus address is hard wired as given in [Table 1.1, "Part Selection"](#).

APPLICATION NOTE: The pull-up resistor on the THERM pin must be connected to the same 3.3V supply that drives the VDD pin. Additionally, for ~10ms after power up, the THERM pin must not be pulled low SMBus slave address will not be decoded properly. If the system requirements do not permit these conditions, then the THERM pin must be isolated from their respective busses during this time.

4.8 SMBus Timeout

The EMC1413 and EMC1414 support SMBus Timeout. If the clock line is held low for longer than 30ms, the device will reset its SMBus protocol. This function can be enabled by setting the TIMEOUT bit in the Consecutive Alert Register (see [Section 6.12, "Consecutive ALERT Register"](#)).

Chapter 5 Product Description

The EMC1413 and EMC1414 are SMBus temperature sensors. The EMC1413 monitors one internal diode and two externally connected temperature diodes. The EMC1414 monitors one internal diode and three externally connected temperature diodes.

Thermal management is performed in cooperation with a host device. This consists of the host reading the temperature data of both the external and internal temperature diodes of the EMC1413 and EMC1414 and using that data to control the speed of one or more fans.

The EMC1413 and EMC1414 have two levels of monitoring. The first provides a maskable $\overline{\text{ALERT}}$ signal to the host when the measured temperatures exceeds user programmable limits. This allows the EMC1413 or EMC1414 to be used as an independent thermal watchdog to warn the host of temperature hot spots without direct control by the host. The second level of monitoring provides a non maskable interrupt on the $\overline{\text{THERM}}$ pin if the measured temperatures meet or exceed a second programmable limit.

Since the EMC1413 and EMC1414 automatically correct for temperature errors due to series resistance in temperature diode lines, there is greater flexibility in where external diodes are positioned and better measurement accuracy than previously available with non-resistance error correcting devices. The automatic beta detection feature means that there is no need to program the device according to which type of diode is present on the External Diode 1 channel. This also includes CPU diodes that require the transistor or BJT model for monitoring their temperature. Therefore, the EMC1413/EMC1414 can power up ready to operate for any system configuration.

For the EMC1414, External Diode channels 2 and 3 are only compatible with general purpose diodes (such as a 2N3904).

Figure 5.1 shows a system level block diagram of the EMC1413. Figure 5.2 shows a system level block diagram of the EMC1414.

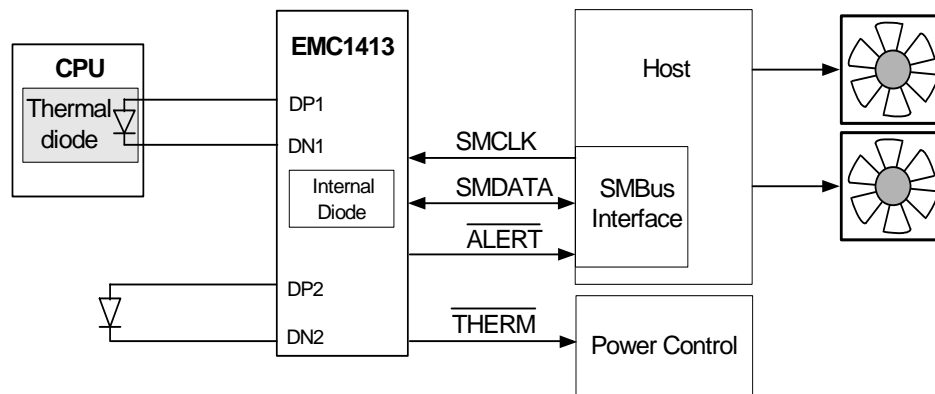


Figure 5.1 System Diagram for EMC1413

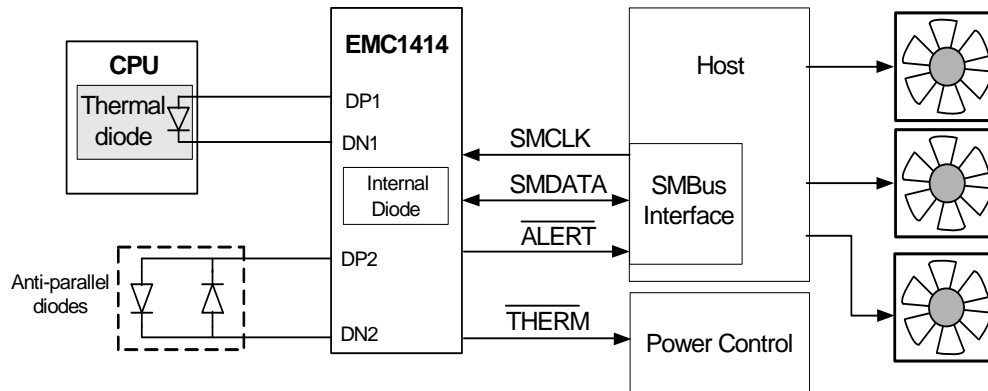


Figure 5.2 System Diagram for EMC1414

5.1 Modes of Operation

The EMC1413 and EMC1414 have two modes of operation:

- Active (Run) - In this mode of operation, the ADC is converting on all temperature channels at the programmed conversion rate. The temperature data is updated at the end of every conversion and the limits are checked. In Active mode, writing to the one-shot register will do nothing.
- Standby (Stop) - In this mode of operation, the majority of circuitry is powered down to reduce supply current. The temperature data is not updated and the limits are not checked. In this mode of operation, the SMBus is fully active and the part will return requested data. Writing to the one-shot register will enable the device to update all temperature channels. Once all the channels are updated, the device will return to the Standby mode.

5.1.1 Conversion Rates

The EMC1413 and EMC1414 may be configured for different conversion rates based on the system requirements. The conversion rate is configured as described in [Section 6.5, "Conversion Rate Register"](#). The default conversion rate is 4 conversions per second. Other available conversion rates are shown in [Table 6.6, "Conversion Rate"](#).

5.1.2 Dynamic Averaging

Dynamic averaging causes the EMC1413 and EMC1414 to measure the external diode channels for an extended time based on the selected conversion rate. This functionality can be disabled for increased power savings at the lower conversion rates (see [Section 6.4, "Configuration Register"](#)). When dynamic averaging is enabled, the device will automatically adjust the sampling and measurement time for the external diode channels. This allows the device to average 2x or 16x longer than the normal 11 bit operation (nominally 21ms per channel) while still maintaining the selected conversion rate. The benefits of dynamic averaging are improved noise rejection due to the longer integration time as well as less random variation of the temperature measurement.

When enabled, the dynamic averaging applies when a one-shot command is issued. The device will perform the desired averaging during the one-shot operation according to the selected conversion rate.

When enabled, the dynamic averaging will affect the average supply current based on the chosen conversion rate as shown in [Table 5.1, "Supply Current vs. Conversion Rate for EMC1413"](#) for EMC1413.

Table 5.1 Supply Current vs. Conversion Rate for EMC1413

CONVERSION RATE	AVERAGE SUPPLY CURRENT		AVERAGING FACTOR (BASED ON 11-BIT OPERATION)	
	ENABLED (DEFAULT)	DISABLED	ENABLED (DEFAULT)	DISABLED
1 / 16 sec	660uA	430uA	16x	1x
1 / 8 sec	660uA	430uA	16x	1x
1 / 4 sec	660uA	430uA	16x	1x
1 / 2 sec	660uA	430uA	16x	1x
1 / sec	660uA	430uA	16x	1x
2 / sec	930uA	475uA	8x	1x
4 / sec (default)	950uA	510uA	4x	1x
8 / sec	1010uA	630uA	2x	1x
16 / sec	1020uA	775uA	1x	1x
32 / sec	1050uA	1050uA	0.5x	0.5x
64 / sec	1100uA	1100uA	0.25x	0.25x

When enabled, the dynamic averaging will affect the average supply current based on the chosen conversion rate as shown in [Table 5.2](#) for EMC1414.

Table 5.2 Supply Current vs. Conversion Rate for EMC1414

CONVERSION RATE	AVERAGE SUPPLY CURRENT		AVERAGING FACTOR (BASED ON 11-BIT OPERATION)	
	ENABLED (DEFAULT)	DISABLED	ENABLED (DEFAULT)	DISABLED
1 / 16 sec	660uA	430uA	16x	1x
1 / 8 sec	660uA	430uA	16x	1x
1 / 4 sec	660uA	430uA	16x	1x
1 / 2 sec	660uA	430uA	16x	1x
1 / sec	660uA	430uA	8x	1x
2 / sec	930uA	475uA	4x	1x
4 / sec (default)	950uA	510uA	2x	1x
8 / sec	1010uA	630uA	1x	1x
16 / sec	1020uA	775uA	0.5x	0.5x

Table 5.2 Supply Current vs. Conversion Rate for EMC1414 (continued)

CONVERSION RATE	AVERAGE SUPPLY CURRENT		AVERAGING FACTOR (BASED ON 11-BIT OPERATION)	
	ENABLED (DEFAULT)	DISABLED	ENABLED (DEFAULT)	DISABLED
32 / sec	1050uA	1050uA	0.25x	0.25x
64 / sec	1100uA	1100uA	0.125x	0.125x

5.2 THERM Output

The $\overline{\text{THERM}}$ output is asserted independently of the $\overline{\text{ALERT}}$ output and cannot be masked. Whenever any of the measured temperatures exceed the user programmed THERM Limit values for the programmed number of consecutive measurements, the $\overline{\text{THERM}}$ output is asserted. Once it has been asserted, it will remain asserted until all measured temperatures drop below the THERM Limit minus the THERM Hysteresis (also programmable).

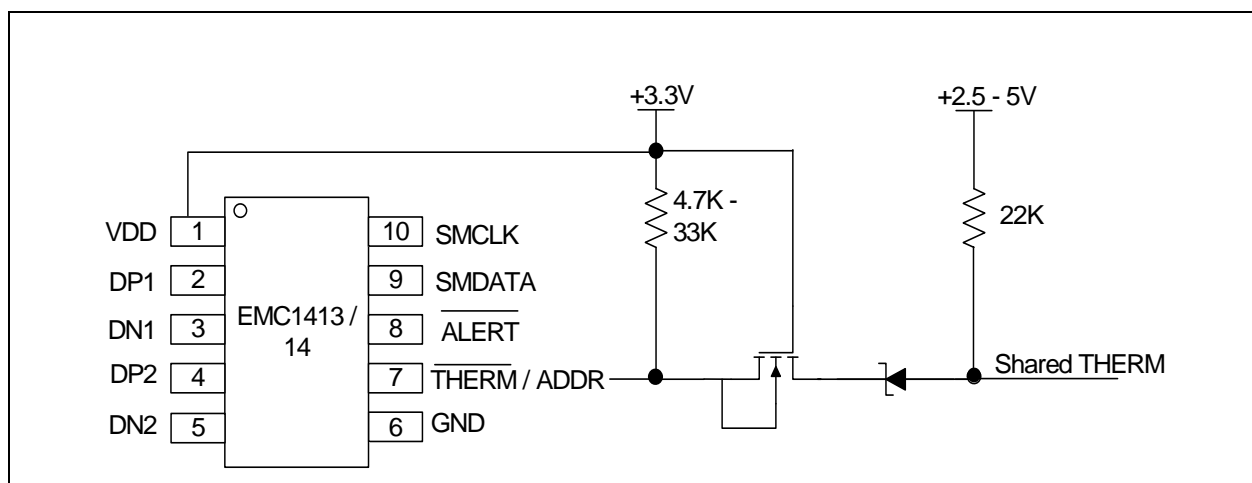
When the $\overline{\text{THERM}}$ pin is asserted, the Therm status bits will likewise be set. Reading these bits will not clear them until the $\overline{\text{THERM}}$ pin is deasserted. Once the $\overline{\text{THERM}}$ pin is deasserted, the THERM status bits will be automatically cleared.

5.2.1 THERM Pin Considerations

Because of the decode method used to determine the SMBus Address it is important that the pull-up resistance on $\overline{\text{THERM}}$ pin be within $\pm 10\%$ tolerance. Additionally, the pull-up resistor on the $\overline{\text{THERM}}$ pin must be connected to the same 3.3V supply that drives the VDD pin.

For 15ms after power up, the $\overline{\text{THERM}}$ pin must not be pulled low or the SMBus Address will not be decoded properly. If the system requirements do not permit these conditions, then the $\overline{\text{THERM}}$ pin must be isolated from their respective busses during this time.

One method of isolating this pin is shown in Figure 5.3.

Figure 5.3 Isolating $\overline{\text{THERM}}$ Pin

5.3 ALERT Output

The $\overline{\text{ALERT}}$ pin is an open drain output and requires a pull-up resistor to V_{DD} and has two modes of operation: interrupt mode and comparator Mode. The mode of the $\overline{\text{ALERT}}$ output is selected via the ALERT / COMP bit in the Configuration Register (see Section 6.4).

5.3.1 ALERT Pin Interrupt Mode

When configured to operate in interrupt mode, the $\overline{\text{ALERT}}$ pin asserts low when an out of limit measurement (\geq high limit or $<$ low limit) is detected on any diode or when a diode fault is detected. The $\overline{\text{ALERT}}$ pin will remain asserted as long as an out-of-limit condition remains. Once the out-of-limit condition has been removed, the $\overline{\text{ALERT}}$ pin will remain asserted until the appropriate status bits are cleared.

The $\overline{\text{ALERT}}$ pin can be masked by setting the MASK bit. Once the $\overline{\text{ALERT}}$ pin has been masked, it will be de-asserted and remain de-asserted until the MASK bit is cleared by the user. Any interrupt conditions that occur while the $\overline{\text{ALERT}}$ pin is masked will update the Status Register normally.

The $\overline{\text{ALERT}}$ pin is used as an interrupt signal or as an Smbus Alert signal that allows an SMBus slave to communicate an error condition to the master. One or more $\overline{\text{ALERT}}$ outputs can be hard-wired together.

5.3.2 ALERT Pin Comparator Mode

When the ALERT pin is configured to operate in comparator mode it will be asserted if any of the measured temperatures exceeds the respective high limit. The $\overline{\text{ALERT}}$ pin will remain asserted until all temperatures drop below the corresponding high limit minus the THERM Hysteresis value.

When the $\overline{\text{ALERT}}$ pin is asserted in comparator mode, the corresponding high limit status bits will be set. Reading these bits will not clear them until the $\overline{\text{ALERT}}$ pin is deasserted. Once the $\overline{\text{ALERT}}$ pin is deasserted, the status bits will be automatically cleared.

The MASK bit will not block the $\overline{\text{ALERT}}$ pin in this mode, however the individual channel masks (see [Section 6.11, "Channel Mask Register"](#)) will prevent the respective channel from asserting the ALERT pin.

5.4 Beta Compensation

The EMC1413 and EMC1414 are configured to monitor the temperature of basic diodes (e.g. 2N3904), or CPU thermal diodes. It automatically detects the type of external diode (CPU diode or diode connected transistor) and determines the optimal setting to reduce temperature errors introduced by beta variation for the External Diode 1 channel only. Compensating for this error is also known as implementing the transistor or BJT model for temperature measurement.

For discrete transistors configured with the collector and base shorted together, the beta is generally sufficiently high such that the percent change in beta variation is very small. For example, a 10% variation in beta for two forced emitter currents with a transistor whose ideal beta is 50 would contribute approximately 0.25°C error at 100°C. However for substrate transistors where the base-emitter junction is used for temperature measurement and the collector is tied to the substrate, the proportional beta variation will cause large error. For example, a 10% variation in beta for two forced emitter currents with a transistor whose ideal beta is 0.5 would contribute approximately 8.25°C error at 100°C.

The External Diode 2 and External Diode 3 channels do not support Beta Compensation.

5.5 Resistance Error Correction (REC)

Parasitic resistance in series with the external diodes will limit the accuracy obtainable from temperature measurement devices. The voltage developed across this resistance by the switching diode currents cause the temperature measurement to read higher than the true temperature. Contributors to series resistance are PCB trace resistance, on die (i.e. on the processor) metal resistance, bulk resistance in the base and emitter of the temperature transistor. Typically, the error caused by series resistance is +0.7°C per ohm. The EMC1413 and EMC1414 automatically correct up to 100 ohms of series resistance.

5.6 Programmable External Diode Ideality Factor

The EMC1413 and EMC1414 is designed for external diodes with an ideality factor of 1.008. Not all external diodes, processor or discrete, will have this exact value. This variation of the ideality factor introduces error in the temperature measurement which must be corrected for. This correction is

Datasheet

typically done using programmable offset registers. Since an ideality factor mismatch introduces an error that is a function of temperature, this correction is only accurate within a small range of temperatures. To provide maximum flexibility to the user, the EMC1413 and EMC1414 provides a 6-bit register for each external diode where the ideality factor of the diode used is programmed to eliminate errors across all temperatures.

APPLICATION NOTE: When monitoring a substrate transistor or CPU diode and beta compensation is enabled, the Ideality Factor should not be adjusted. Beta Compensation automatically corrects for most ideality errors.

5.7 Diode Faults

The EMC1413 and EMC1414 detect an open on the DP and DN pins, and a short across the DP and DN pins. For each temperature measurement made, the device checks for a diode fault on the external diode channel(s). When a diode fault is detected, the ALERT pin asserts (unless masked, see [Section 5.8, "Consecutive Alerts"](#)) and the temperature data reads 00h in the MSB and LSB registers (note: the low limit will not be checked). A diode fault is defined as one of the following: an open between DP and DN, a short from V_{DD} to DP, or a short from V_{DD} to DN.

If a short occurs across DP and DN or a short occurs from DP to GND, the low limit status bit is set and the ALERT pin asserts (unless masked). This condition is indistinguishable from a temperature measurement of 0.000degC (-64°C in extended range) resulting in temperature data of 00h in the MSB and LSB registers.

If a short from DN to GND occurs (with a diode connected), temperature measurements will continue as normal with no alerts.

5.8 Consecutive Alerts

The EMC1413 and EMC1414 contain multiple consecutive alert counters. One set of counters applies to the ALERT pin and the second set of counters applies to the THERM pin. Each temperature measurement channel has a separate consecutive alert counter for each of the ALERT and THERM pins. All counters are user programmable and determine the number of consecutive measurements that a temperature channel(s) must be out-of-limit or reporting a diode fault before the corresponding pin is asserted.

See [Section 6.12, "Consecutive ALERT Register"](#) for more details on the consecutive alert function.

5.9 Digital Filter

To reduce the effect of noise and temperature spikes on the reported temperature, the External Diode 1 channel uses a programmable digital filter. This filter can be configured as Level 1, Level 2, or Disabled. The typical filter performance is shown in Figure 5.4, "Temperature Filter Step Response" and Figure 5.5, "Temperature Filter Impulse Response".

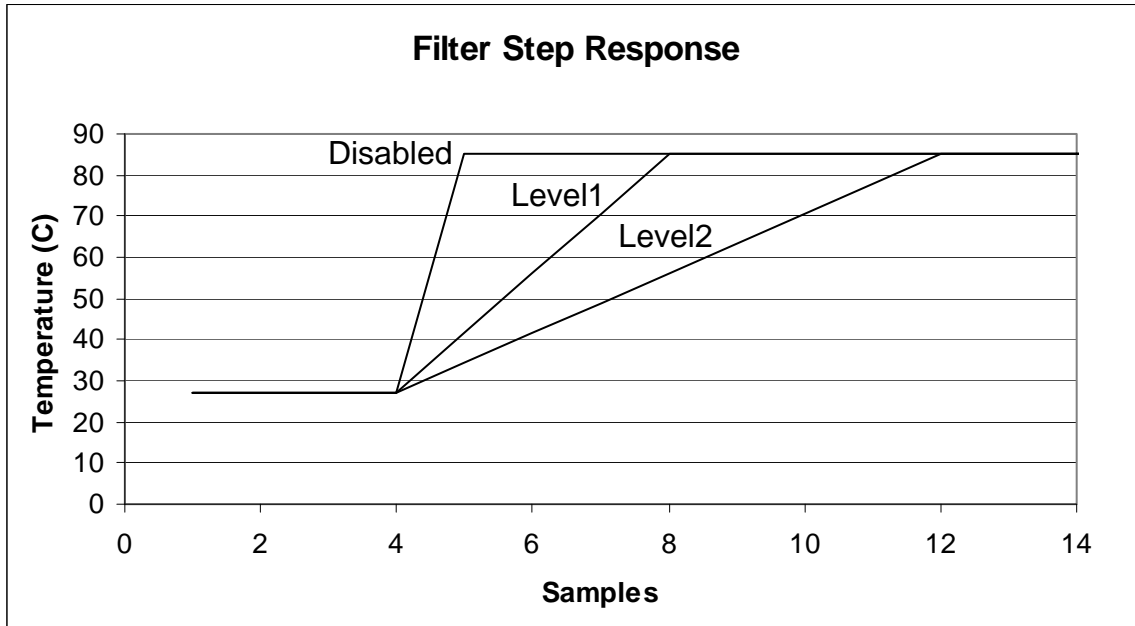


Figure 5.4 Temperature Filter Step Response

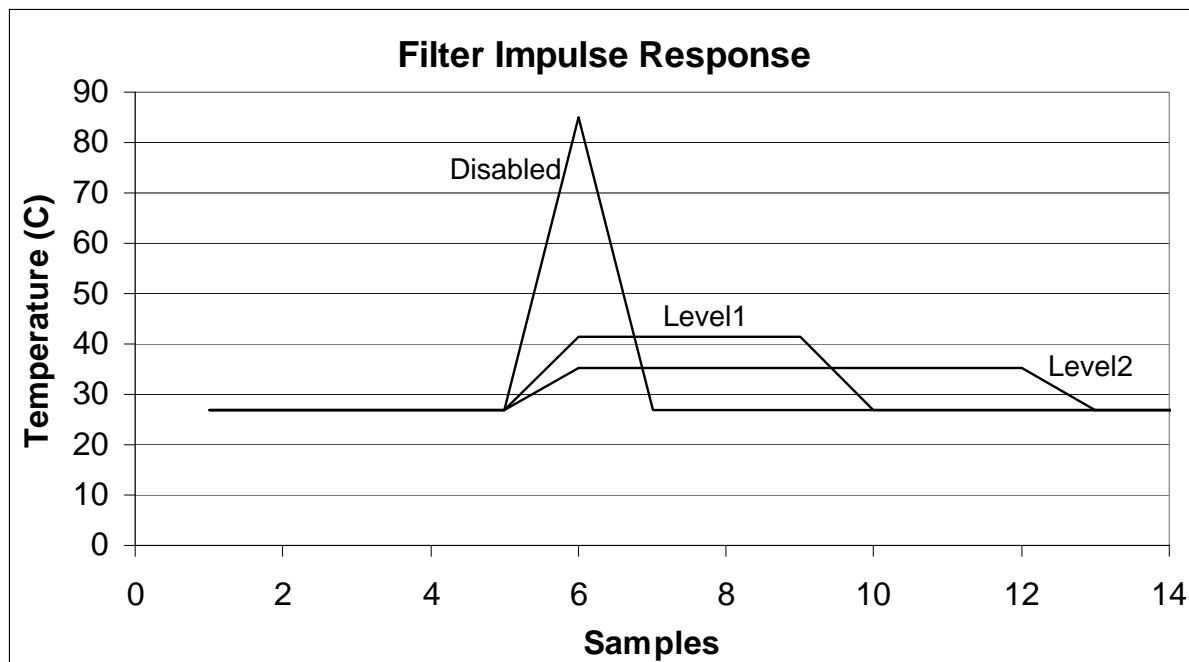


Figure 5.5 Temperature Filter Impulse Response

5.10 Temperature Monitors

In general, thermal diode temperature measurements are based on the change in forward bias voltage of a diode when operated at two different currents. This ΔV_{BE} is proportional to absolute temperature as shown in the following equation:

$$\Delta V_{BE} = \frac{\eta kT}{q} \ln \left(\frac{I_{HIGH}}{I_{LOW}} \right)$$

where:

k = Boltzmann's constant

T = absolute temperature in Kelvin [1]

q = electron charge

η = diode ideality factor

5.11 Temperature Measurement Results and Data

The temperature measurement results are stored in the internal and external temperature registers. These are then compared with the values stored in the high and low limit registers. Both external and internal temperature measurements are stored in 11-bit format with the eight (8) most significant bits stored in a high byte register and the three (3) least significant bits stored in the three (3) MSB positions of the low byte register. All other bits of the low byte register are set to zero.

The EMC1413 and EMC1414 have two selectable temperature ranges. The default range is from 0°C to +127°C and the temperature is represented as binary number able to report a temperature from 0°C to +127.875°C in 0.125°C steps.

The extended range is an extended temperature range from -64°C to +191°C. The data format is a binary number offset by 64°C. The extended range is used to measure temperature diodes with a large known offset (such as AMD processor diodes) where the diode temperature plus the offset would be equivalent to a temperature higher than +127°C.

Table 5.3, "EMC1413 and EMC1414 Temperature Data Format" shows the default and extended range formats.

Table 5.3 EMC1413 and EMC1414 Temperature Data Format

TEMPERATURE (°C)	DEFAULT RANGE 0°C TO 127°C	EXTENDED RANGE RANGE -64°C TO 191°C
Diode Fault	000 0000 0000	000 0000 0000
-64	000 0000 0000	000 0000 0000 Note 5.2
-1	000 0000 0000	001 1111 1000b
0	000 0000 0000 Note 5.1	010 0000 0000
0.125	000 0000 0001	010 0000 0001
1	000 0000 1000	010 0000 1000
64	010 0000 0000	100 0000 0000
65	010 0000 1000	100 0000 1000
127	011 1111 1000	101 1111 1000
127.875	011 1111 1111	101 1111 1111
128	011 1111 1111 Note 5.3	110 0000 0000

Table 5.3 EMC1413 and EMC1414 Temperature Data Format (continued)

TEMPERATURE (°C)	DEFAULT RANGE 0°C TO 127°C	EXTENDED RANGE RANGE -64°C TO 191°C
190	011 1111 1111	111 1111 0000
191	011 1111 1111	111 1111 1000
>= 191.875	011 1111 1111	111 1111 1111 Note 5.4

Note 5.1 In default mode, all temperatures < 0°C will be reported as 0°C.

Note 5.2 In the extended range, all temperatures < -64°C will be reported as -64°C.

Note 5.3 For the default range, all temperatures > +127.875°C will be reported as +127.875°C.

Note 5.4 For the extended range, all temperatures > +191.875°C will be reported as +191.875°C.

5.12 Anti-parallel Diode Connections

The EMC1414 supports reading two external diodes on the same set of pins (DP2, DN2). These diodes are connected as shown in Figure 5.2, "System Diagram for EMC1414". Due to the anti-parallel connection of these diodes, both diodes will be reverse biased by a V_{BE} voltage (approximately 0.7V). Because of this reverse bias, only discrete thermal diodes (such as a 2N3904) are recommended to be placed on these pins.

5.13 External Diode Connections

The EMC1413 can be configured to measure a CPU substrate transistor, a discrete 2N3904 thermal diode, or an AMD processor diode. The diodes can be connected in a variety of ways as indicated in Figure 5.6, "Diode Configurations".

The EMC1414 can be configured to measure a CPU substrate transistor, a discrete 2N3904 thermal diode, or an AMD processor diode on the External Diode 1 channel only. The External Diode 2 and External Diode 3 channels are configured to measure a pair of discrete anti-parallel diodes (shared on pins DP2 and DN2). The supported configurations for the external diode channels are shown in Figure 5.6, "Diode Configurations".

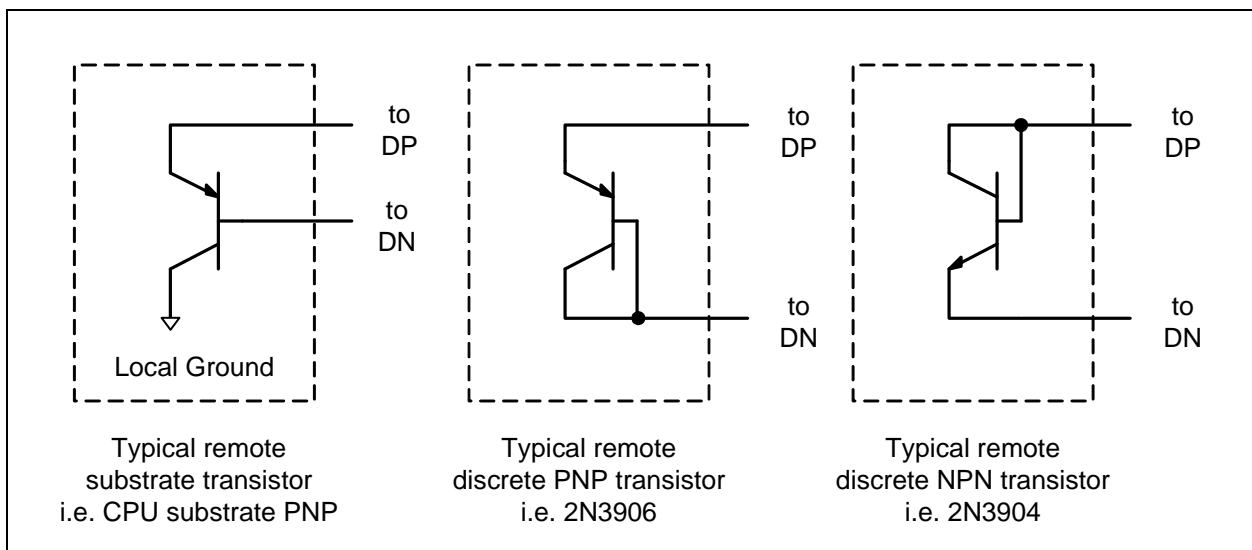


Figure 5.6 Diode Configurations

Chapter 6 Register Description

The registers shown in [Table 6.1](#) are accessible through the SMBus. An entry of '-' indicates that the bit is not used and will always read '0'.

Table 6.1 Register Set in Hexadecimal Order

REGISTER ADDRESS	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	PAGE
00h	R	Internal Diode Data High Byte	Stores the integer data for the Internal Diode	00h	Page 28
01h	R	External Diode 1 Data High Byte	Stores the integer data for External Diode 1	00h	
02h	R	Status	Stores the status bits for the Internal Diode and External Diodes	00h	Page 29
03h	R/W	Configuration	Controls the general operation of the device (mirrored at address 09h)	00h	Page 29
04h	R/W	Conversion Rate	Controls the conversion rate for updating temperature data (mirrored at address 0Ah)	06h (4/sec)	Page 30
05h	R/W	Internal Diode High Limit	Stores the 8-bit high limit for the Internal Diode (mirrored at address 0Bh)	55h (85°C)	Page 31
06h	R/W	Internal Diode Low Limit	Stores the 8-bit low limit for the Internal Diode (mirrored at address 0Ch)	00h (0°C)	
07h	R/W	External Diode 1 High Limit High Byte	Stores the integer portion of the high limit for External Diode 1 (mirrored at register 0Dh)	55h (85°C)	
08h	R/W	External Diode 1 Low Limit High Byte	Stores the integer portion of the low limit for External Diode 1 (mirrored at register 0Eh)	00h (0°C)	
09h	R/W	Configuration	Controls the general operation of the device (mirrored at address 03h)	00h	Page 29
0Ah	R/W	Conversion Rate	Controls the conversion rate for updating temperature data (mirrored at address 04h)	06h (4/sec)	Page 30

Table 6.1 Register Set in Hexadecimal Order (continued)

REGISTER ADDRESS	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	PAGE
0Bh	R/W	Internal Diode High Limit	Stores the 8-bit high limit for the Internal Diode (mirrored at address 05h)	55h (85°C)	Page 31
0Ch	R/W	Internal Diode Low Limit	Stores the 8-bit low limit for the Internal Diode (mirrored at address 06h)	00h (0°C)	
0Dh	R/W	External Diode 1 High Limit High Byte	Stores the integer portion of the high limit for External Diode 1 (mirrored at register 07h)	55h (85°C)	
0Eh	R/W	External Diode 1 Low Limit High Byte	Stores the integer portion of the low limit for External Diode 1 (mirrored at register 08h)	00h (0°C)	
0Fh	W	One shot	A write to this register initiates a one shot update.	00h	Page 33
10h	R	External Diode 1 Data Low Byte	Stores the fractional data for External Diode 1	00h	Page 28
11h	R/W	Scratchpad	Scratchpad register for software compatibility	00h	Page 33
12h	R/W	Scratchpad	Scratchpad register for software compatibility	00h	Page 33
13h	R/W	External Diode 1 High Limit Low Byte	Stores the fractional portion of the high limit for External Diode 1	00h	Page 31
14h	R/W	External Diode 1 Low Limit Low Byte	Stores the fractional portion of the low limit for External Diode 1	00h	
15h	R/W	External Diode 2 High Limit High Byte	Stores the integer portion of the high limit for External Diode 2	55h (85°C)	Page 31
16h	R/W	External Diode 2 Low Limit High Byte	Stores the integer portion of the low limit for External Diode 2	00h (0°C)	
17h	R/W	External Diode 2 High Limit Low Byte	Stores the fractional portion of the high limit External Diode 2	00h	Page 31
18h	R/W	External Diode 2 Low Limit Low Byte	Stores the fractional portion of the low limit for External Diode 2	00h	
19h	R/W	External Diode 1 THERM Limit	Stores the 8-bit critical temperature limit for External Diode 1	55h (85°C)	Page 33
1Ah	R/W	External Diode 2 THERM Limit	Stores the 8-bit critical temperature limit for External Diode 2	55h (85°C)	Page 33
1Bh	R-C	External Diode Fault	Stores status bits indicating which external diode detected a diode fault	00h	Page 34
1Fh	R/W	Channel Mask Register	Controls the masking of individual channels	00h	Page 34

Table 6.1 Register Set in Hexadecimal Order (continued)

REGISTER ADDRESS	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	PAGE
20h	R/W	Internal Diode THERM Limit	Stores the 8-bit critical temperature limit for the Internal Diode	55h (85°C)	Page 33
21h	R/W	THERM Hysteresis	Stores the 8-bit hysteresis value that applies to all THERM limits	0Ah (10°C)	
22h	R/W	Consecutive ALERT	Controls the number of out-of-limit conditions that must occur before an interrupt is asserted	70h	Page 35
23h	R	External Diode 2 Data High Byte	Stores the integer data for External Diode 2	00h	Page 28
24h	R	External Diode 2 Data Low Byte	Stores the fractional data for External Diode 2	00h	
25h	R/W	External Diode 1 Beta Configuration	Stores the Beta Compensation circuitry settings for External Diode 1	08h	Page 36
26h	R/W	External Diode 2 Beta Configuration	Stores the Beta Compensation circuitry settings for External Diode 2	08h or 07h	Page 36
27h	R/W	External Diode 1 Ideality Factor	Stores the ideality factor for External Diode 1	12h (1.008)	Page 37
28h	R/W	External Diode 2 Ideality Factor	Stores the ideality factor for External Diode 2	12h (1.008)	Page 37
29h	R	Internal Diode Data Low Byte	Stores the fractional data for the Internal Diode	00h	Page 28
2Ah	R	External Diode 3 High Byte	Stores the integer data for External Diode 3	00h	Page 28
2Bh	R	External Diode 3 Low Byte	Stores the fractional data for External Diode 3	00h	
2Ch	R/W	External Diode 3 High Limit High Byte	Stores the integer portion of the high limit for External Diode 3	55h (85°C)	Page 31
2Dh	R/W	External Diode 3 Low Limit High Byte	Stores the integer portion of the low limit for External Diode 3	00h (0°C)	
2Eh	R/W	External Diode 3 High Limit Low Byte	Stores the fractional portion of the high limit for External Diode 3	00h	
2Fh	R/W	External Diode 3 Low Limit Low Byte	Stores the fractional portion of the low limit for External Diode 3	00h	
30h	R/W	External Diode 3 THERM Limit	Stores the 8-bit critical temperature limit for External Diode 3	55h (85°C)	
31h	R/W	External Diode 3 Ideality Factor	Stores the ideality factor for External Diode 3	12h (1.008)	Page 37
35h	R-C	High Limit Status	Status bits for the High Limits	00h	Page 39
36h	R-C	Low Limit Status	Status bits for the Low Limits	00h	Page 39
37h	R	THERM Limit Status	Status bits for the THERM Limits	00h	Page 40

Table 6.1 Register Set in Hexadecimal Order (continued)

REGISTER ADDRESS	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	PAGE
40h	R/W	Filter Control	Controls the digital filter setting for the External Diode 1 channel	00h	Page 40
FDh	R	Product ID	Stores a fixed value that identifies each product	Table 6.25	Page 41
FEh	R	SMSC ID	Stores a fixed value that represents SMSC	5Dh	Page 41
FFh	R	Revision	Stores a fixed value that represents the revision number	03h	Page 41

6.1 Data Read Interlock

When any temperature channel high byte register is read, the corresponding low byte is copied into an internal 'shadow' register. The user is free to read the low byte at any time and be guaranteed that it will correspond to the previously read high byte. Regardless if the low byte is read or not, reading from the same high byte register again will automatically refresh this stored low byte data.

6.2 Temperature Data Registers

Table 6.2 Temperature Data Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
00h	R	Internal Diode High Byte	128	64	32	16	8	4	2	1	00h
29h	R	Internal Diode Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
01h	R	External Diode 1 High Byte	128	64	32	16	8	4	2	1	00h
10h	R	External Diode 1 Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
23h	R	External Diode 2 High Byte	128	64	32	16	8	4	2	1	00h
24h	R	External Diode 2 Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
2Ah	R	External Diode 3 High Byte	128	64	32	16	8	4	2	1	00h
2Bh	R	External Diode 3 Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h

As shown in [Table 6.2, "Temperature Data Registers"](#), all temperatures are stored as an 11-bit value with the high byte representing the integer value and the low byte representing the fractional value left justified to occupy the MSBits.

6.3 Status Register

Table 6.3 Status Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
02h	R	Status	BUSY	-	-	HIGH	LOW	FAULT	THERM	-	00h

The Status Register reports general error conditions. To identify specific channels, refer to [Section 6.10, "External Diode Fault Register"](#), [Section 6.15, "High Limit Status Register"](#), [Section 6.16, "Low Limit Status Register"](#), and [Section 6.17, "THERM Limit Status Register"](#). The individual Status Register bits are cleared when the appropriate High Limit, Low Limit, or THERM Limit register has been read or cleared.

Bit 7 - BUSY - This bit indicates that the ADC is currently converting. This bit does not cause either the ALERT or THERM pins to be asserted.

Bit 4 - HIGH - This bit is set when any of the temperature channels exceeds its programmed high limit. See the High Limit Status Register for specific channel information ([Section 6.15, "High Limit Status Register"](#)). When set, this bit will assert the $\overline{\text{ALERT}}$ pin.

Bit 3 - LOW - This bit is set when any of the temperature channels drops below its programmed low limit. See the Low Limit Status Register for specific channel information ([Section 6.16, "Low Limit Status Register"](#)). When set, this bit will assert the $\overline{\text{ALERT}}$ pin.

Bit 2 - FAULT - This bit is asserted when a diode fault is detected on any of the external diode channels. See the External Diode Fault Register for specific channel information ([Section 6.10, "External Diode Fault Register"](#)). When set, this bit will assert the $\overline{\text{ALERT}}$ pin.

Bit 1 - THERM - This bit is set when the any of the temperature channels exceeds its programmed THERM limit. See the THERM Limit Status Register for specific channel information ([Section 6.17, "THERM Limit Status Register"](#)). When set, this bit will assert the $\overline{\text{THERM}}$ pin.

6.4 Configuration Register

Table 6.4 Configuration Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
03h	R/W	Configuration	MASK_ ALL	RUN / STOP	ALERT/ COMP	RECD ₁	RECD ₂	RANGE	DAVG_ DIS	- APDD	00h
09h											

The Configuration Register controls the basic operation of the device. This register is fully accessible at either address.

Bit 7 - MASK_ALL - Masks the $\overline{\text{ALERT}}$ pin from asserting.

- '0' (default) - The $\overline{\text{ALERT}}$ pin is not masked. If any of the appropriate status bits are set the $\overline{\text{ALERT}}$ pin will be asserted.
- '1' - The $\overline{\text{ALERT}}$ pin is masked. It will not be asserted for any interrupt condition unless it is configured as a secondary THERM pin. The Status Registers will be updated normally.

Bit 6 - RUN / STOP - Controls Active/Standby modes.

- '0' (default) - The device is in Active mode and converting on all channels.
- '1' - The device is in Standby mode and not converting.

Bit 5 - ALERT/COMP - Controls the operation of the $\overline{\text{ALERT}}$ pin.

- '0' (default) - The $\overline{\text{ALERT}}$ pin acts as described in [Section 5.3, "ALERT Output"](#).

- '1' - The $\overline{\text{ALERT}}$ pin acts in comparator mode as described in [Section 5.3.2, "ALERT Pin Comparator Mode"](#). In this mode the MASK_ALL bit is ignored.

Bit 4 - RECD1 - Disables the Resistance Error Correction (REC) for External Diode 1.

- '0' (default)- REC is enabled for External Diode 1.
- '1' - REC is disabled for External Diode 1.

Bit 3 - RECD2 - Disables the Resistance Error Correction (REC) for External Diode 2 and External Diode 3.

- '0' (default) - REC is enabled for External Diode 2 and External Diode 3.
- '1' - REC is disabled for External Diode 2 and External Diode 3.

Bit 2 - RANGE - Configures the measurement range and data format of the temperature channels.

- '0' (default) - The temperature measurement range is 0°C to +127.875°C and the data format is binary.
- '1' -The temperature measurement range is -64°C to +191.875°C and the data format is offset binary (see [Table 5.3, "EMC1413 and EMC1414 Temperature Data Format"](#)).

Bit 1 - DAVG_DIS - Disables the dynamic averaging feature on all temperature channels.

- '0' (default) - The dynamic averaging feature is enabled. All temperature channels will be converted with an averaging factor that is based on the conversion rate as shown in [Table 5.1](#) and [Table 5.2](#).
- '1' - The dynamic averaging feature is disabled. All temperature channels will be converted with a maximum averaging factor of 1x (equivalent to 11-bit conversion). For higher conversion rates, this averaging factor will be reduced as shown in [Table 5.1](#) and [Table 5.2](#).

Bit 0 - APDD (EMC1414 only) - Disables the anti-parallel diode operation. Beta Compensation is disabled on External Diode 2 and 3 regardless of APDD setting. In addition, External Diode 2 Beta Configuration register will be ignored.

- '0' (default) - Anti-parallel diode mode is enabled. Two external diodes will be measured on the DP2 and DN2 pins.
- '1' - Anti-parallel diode mode is disabled. Only one external diode will be measured on the DP2 and DN2 pins.

6.5 Conversion Rate Register

Table 6.5 Conversion Rate Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
04h	R/W	Conversion Rate	-	-	-	-	CONV[3:0]			06h (4/sec)	
0Ah											

The Conversion Rate Register controls how often the temperature measurement channels are updated and compared against the limits. This register is fully accessible at either address.

Bits 3-0 - CONV[3:0] - Determines the conversion rate as shown in [Table 6.6](#).

Table 6.6 Conversion Rate

CONV[3:0]					CONVERSIONS / SECOND
HEX	3	2	1	0	
0h	0	0	0	0	1 / 16
1h	0	0	0	1	1 / 8
2h	0	0	1	0	1 / 4
3h	0	0	1	1	1 / 2
4h	0	1	0	0	1
5h	0	1	0	1	2
6h	0	1	1	0	4 (default)
7h	0	1	1	1	8
8h	1	0	0	0	16
9h	1	0	0	1	32
Ah	1	0	1	0	64
Bh - Fh	All others				1

6.6 Limit Registers

Table 6.7 Temperature Limit Registers

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
05h	R/W	Internal Diode High Limit	128	64	32	16	8	4	2	1	55h (85°C)
0Bh											
06h	R/W	Internal Diode Low Limit	128	64	32	16	8	4	2	1	00h (0°C)
0Ch											
07h	R/W	External Diode 1 High Limit High Byte	128	64	32	16	8	4	2	1	55h (85°C)
0Dh											
13h	R/W	External Diode 1 High Limit Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
08h	R/W	External Diode 1 Low Limit High Byte	128	64	32	16	8	4	2	1	00h (0°C)
0Eh											

Table 6.7 Temperature Limit Registers (continued)

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
14h	R/W	External Diode 1 Low Limit Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
15h	R/W	External Diode 2 High Limit High Byte	128	64	32	16	8	4	2	1	55h (85°C)
16h	R/W	External Diode 2 Low Limit High Byte	128	64	32	16	8	4	2	1	00h (0°C)
17h	R/W	External Diode 2 High Limit Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
18h	R/W	External Diode 2 Low Limit Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
2Ch	R/W	External Diode 3 High Limit High Byte	128	64	32	16	8	4	2	1	55h (85°C)
2Dh	R/W	External Diode 3 Low Limit High Byte	128	64	32	16	8	4	2	1	00h (0°C)
2Eh	R/W	External Diode 3 High Limit Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
2Fh	R/W	External Diode 3 Low Limit Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h

The device contains both high and low limits for all temperature channels. If the measured temperature exceeds the high limit, then the corresponding status bit is set and the ALERT pin is asserted. Likewise, if the measured temperature is less than or equal to the low limit, the corresponding status bit is set and the ALERT pin is asserted.

The data format for the limits must match the selected data format for the temperature so that if the extended temperature range is used, the limits must be programmed in the extended data format.

The limit registers with multiple addresses are fully accessible at either address.

When the device is in standby mode, updating the limit registers will have no effect until the next conversion cycle occurs. This can be initiated via a write to the One Shot Register or by clearing the RUN / STOP bit in the Configuration Register (see [Section 6.4](#)).

6.7 Scratchpad Registers

Table 6.8 Scratchpad Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
11h	R/W	Scratchpad	7	6	5	4	3	2	1	0	00h
12h	R/W	Scratchpad	7	6	5	4	3	2	1	0	00h

The Scratchpad Registers are Read Write registers that are used for place holders to be software compatible with legacy programs. Reading from the registers will return what is written to them.

6.8 One Shot Register

Table 6.9 One Shot Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
0Fh	W	One Shot	Writing to this register initiates a single conversion cycle. Data is not stored and always reads 00h								00h

The One Shot Register is used to initiate a one shot command. Writing to the one shot register, when the device is in standby mode and BUSY bit (in Status Register) is '0', will immediately cause the ADC to update all temperature measurements. Writing to the One Shot Register while the device is in active mode will have no affect.

6.9 Therm Limit Registers

Table 6.10 Therm Limit Registers

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
19h	R/W	External Diode 1 THERM Limit	128	64	32	16	8	4	2	1	55h (85°C)
1Ah	R/W	External Diode 2 THERM Limit	128	64	32	16	8	4	2	1	55h (85°C)
20h	R/W	Internal Diode THERM Limit	128	64	32	16	8	4	2	1	55h (85°C)
21h	R/W	THERM Hysteresis	128	64	32	16	8	4	2	1	0Ah (10°C)
30h	R/W	External Diode 3 THERM Limit	128	64	32	16	8	4	2	1	55h (85°C)

The THERM Limit Registers are used to determine whether a critical thermal event has occurred. If the measured temperature exceeds the THERM Limit, then the THERM pin is asserted. The limit setting must match the chosen data format of the temperature reading registers.

Unlike the $\overline{\text{ALERT}}$ pin, the $\overline{\text{THERM}}$ pin cannot be masked. Additionally, the $\overline{\text{THERM}}$ pin will be released once the temperature drops below the corresponding threshold minus the THERM Hysteresis.

6.10 External Diode Fault Register

Table 6.11 External Diode Fault Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
1Bh	R-C	External Diode Fault	-	-	-	-	E3FLT	E2FLT	E1FLT	-	00h

The External Diode Fault Register indicates which of the external diodes caused the FAULT bit in the Status Register to be set. This register is cleared when it is read.

Bit 3 - E3FLT - This bit is set if the External Diode 3 channel reported a diode fault.

Bit 2 - E2FLT - This bit is set if the External Diode 2 channel reported a diode fault.

Bit 1 - E1FLT - This bit is set if the External Diode 1 channel reported a diode fault.

6.11 Channel Mask Register

Table 6.12 Channel Mask Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
1Fh	R/W	Channel Mask	-	-	-	-	E3 MASK	E2 MASK	E1 MASK	INT MASK	00h

The Channel Mask Register controls individual channel masking. When a channel is masked, the $\overline{\text{ALERT}}$ pin will not be asserted when the masked channel reads a diode fault or out of limit error. The channel mask does not mask the $\overline{\text{THERM}}$ pin.

Bit 3 - E3MASK - Masks the $\overline{\text{ALERT}}$ pin from asserting when the External Diode 3 channel is out of limit or reports a diode fault.

- '0' (default) - The External Diode 3 channel will cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out of limit or reports a diode fault.

- '1' - The External Diode 3 channel will not cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out of limit or reports a diode fault.

Bit 2 - E2MASK - Masks the $\overline{\text{ALERT}}$ pin from asserting when the External Diode 2 channel is out of limit or reports a diode fault.

- '0' (default) - The External Diode 2 channel will cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out of limit or reports a diode fault.

- '1' - The External Diode 2 channel will not cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out of limit or reports a diode fault.

Bit 1 - E1MASK - Masks the $\overline{\text{ALERT}}$ pin from asserting when the External Diode 1 channel is out of limit or reports a diode fault.

- '0' (default) - The External Diode 1 channel will cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out of limit or reports a diode fault.

- '1' - The External Diode 1 channel will not cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out of limit or reports a diode fault.

Bit 0 - INTMASK - Masks the $\overline{\text{ALERT}}$ pin from asserting when the Internal Diode temperature is out of limit.

Datasheet

- '0' (default) - The Internal Diode channel will cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out of limit.
- '1' - The Internal Diode channel will not cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out of limit.

6.12 Consecutive ALERT Register

Table 6.13 Consecutive ALERT Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
22h	R/W	Consecutive ALERT	TIME OUT	CTHRM[2:0]			CALRT[2:0]			-	70h

The Consecutive ALERT Register determines how many times an out-of-limit error or diode fault must be detected in consecutive measurements before the ALERT or THERM pin is asserted. Additionally, the Consecutive ALERT Register controls the SMBus Timeout functionality.

An out-of-limit condition (i.e. HIGH, LOW, or FAULT) occurring on the same temperature channel in consecutive measurements will increment the consecutive alert counter. The counters will also be reset if no out-of-limit condition or diode fault condition occurs in a consecutive reading.

When the ALERT pin is configured as an interrupt, when the consecutive alert counter reaches its programmed value, the following will occur: the STATUS bit(s) for that channel and the last error condition(s) (i.e. E1HIGH, or E2LOW and/or E2FAULT) will be set to '1', the ALERT pin will be asserted, the consecutive alert counter will be cleared, and measurements will continue.

When the $\overline{\text{ALERT}}$ pin is configured as a comparator, the consecutive alert counter will ignore diode fault and low limit errors and only increment if the measured temperature exceeds the High Limit. Additionally, once the consecutive alert counter reaches the programmed limit, the ALERT pin will be asserted, but the counter will not be reset. It will remain set until the temperature drops below the High Limit minus the THERM Hysteresis value.

For example, if the CALRT[2:0] bits are set for 4 consecutive alerts on an EMC1413 device, the high limits are set at 70°C, and none of the channels are masked, then the $\overline{\text{ALERT}}$ pin will be asserted after the following four measurements:

1. Internal Diode reads 71°C and both external diodes read 69°C. Consecutive alert counter for INT is incremented to 1.
2. Both Internal Diode and External Diode 1 read 71°C and External Diode 2 reads 68°C. Consecutive alert counter for INT is incremented to 2 and for EXT1 is set to 1.
3. The External Diode 1 reads 71°C and both the Internal Diode and External Diode 2 read 69°C. Consecutive alert counter for INT and EXT2 are cleared and EXT1 is incremented to 2.
4. The Internal Diode reads 71°C and both external diodes read 71°C. Consecutive alert counter for INT is set to 1, EXT2 is set to 1, and EXT1 is incremented to 3.
5. The Internal Diode reads 71°C and both the external diodes read 71°C. Consecutive alert counter for INT is incremented to 2, EXT2 is set to 2, and EXT1 is incremented to 4. The appropriate status bits are set for EXT1 and the ALERT pin is asserted. EXT1 counter is reset to 0 and all other counters hold the last value until the next temperature measurement.

Bit 7 - TIMEOUT - Determines whether the SMBus Timeout function is enabled.

- '0' (default) - The SMBus Timeout feature is disabled. The SMCLK line can be held low indefinitely without the device resetting its SMBus protocol.
- '1' - The SMBus Timeout feature is enabled. If the SMCLK line is held low for more than 30ms, then the device will reset the SMBus protocol.

Bits 6-4 - CTHRM[2:0] - Determines the number of consecutive measurements that must exceed the corresponding THERM Limit before the THERM pin is asserted. All temperature channels use this value to set the respective counters. The consecutive THERM counter is incremented whenever any measurement exceed the corresponding THERM Limit.

If the temperature drops below the THERM limit, then the counter is reset. If a number of consecutive measurements above the THERM limit occurs, then the $\overline{\text{THERM}}$ pin is asserted low.

Once the $\overline{\text{THERM}}$ pin has been asserted, the consecutive therm counter will not reset until the corresponding temperature drops below the THERM Limit minus the THERM Hysteresis value.

The bits are decoded as shown in Table 6.14, "Consecutive Alert / THERM Settings". The default setting is 4 consecutive out of limit conversions.

Bits 3-1 - CALRT[2:0] - Determine the number of consecutive measurements that must have an out of limit condition or diode fault before the ALERT pin is asserted. All temperature channels use this value to set the respective counters. The bits are decoded as shown in Table 6.14. The default setting is 1 consecutive out of limit conversion.

Table 6.14 Consecutive Alert / THERM Settings

2	1	0	NUMBER OF CONSECUTIVE OUT OF LIMIT MEASUREMENTS
0	0	0	1 (default for CALRT[2:0])
0	0	1	2
0	1	1	3
1	1	1	4 (default for CTHRM[2:0])

6.13 Beta Configuration Registers

Table 6.15 Beta Configuration Registers

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
25h	R/W	External Diode 1 Beta Configuration	-	-	-	-	ENABLE1	BETA1[2:0]			08h
26h	R/W	External Diode 2 Beta Configuration	-	-	-	-	ENABLE2	BETA2[2:0]			08h for EMC1413 or 07h for EMC1414

This register is used to set the Beta Compensation factor that is used for the external diode channels.

Bit 3 - ENABLEx - Enables the Beta Compensation factor autodetection function. This function shall be disabled for External Diode 2.

- '0' - The Beta Compensation Factor autodetection circuitry is disabled. The External Diode will always use the Beta Compensation factor set by the BETAx[2:0] bits.
- '1' (default) - The Beta Compensation factor autodetection circuitry is enabled. At the beginning of every conversion, the optimal Beta Compensation factor setting will be determined and applied. The BETAx[2:0] bits will be automatically updated to indicate the current setting.

Bit 2-0 - BETAx[2:0] - These bits always reflect the current beta configuration settings. If autodetection circuitry is enabled, then these bits will be updated automatically and writing to these bits will have no effect. If the autodetection circuitry is disabled, then these bits will determine the beta configuration setting that is used for their respective channels.

Care should be taken when setting the BETAx[2:0] bits when the autodetection circuitry is disabled. If the Beta Compensation factor is set at a beta value that is higher than the transistor beta, then the

Datasheet

circuit may introduce measurement errors. When measuring a discrete thermal diode (such as 2N3904) or a CPU diode that functions like a discrete thermal diode (such as an AMD processor diode), then the BETAX[2:0] bits should be set to '111b'.

Table 6.16 CPU Beta Values

HEX	ENABLEX	BETAX[2:0]			MINIMUM BETA
		2	1	0	
0h	0	0	0	0	0.11
1h	0	0	0	1	0.18
2h	0	0	1	0	0.25
3h	0	0	1	1	0.33
4h	0	1	0	0	0.43
5h	0	1	0	1	1.00
6h	0	1	1	0	2.33
7h	0	1	1	1	Disabled
8h - Fh	1	X	X	X	Autodetection

6.14 External Diode Ideality Factor Registers

Table 6.17 Ideality Configuration Registers

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
27h	R/W	External Diode 1 Ideality Factor	-	-	IDEALITY1[5:0]					12h	
28h	R/W	External Diode 2 Ideality Factor	-	-	IDEALITY2[5:0]					12h	
31h	R/W	External Diode 3 Ideality Factor	-	-	IDEALITY3[5:0]					12h	

These registers store the ideality factors that are applied to the external diodes. [Table 6.18, "Ideality Factor Look-Up Table \(Diode Model\)"](#) defines each setting and the corresponding ideality factor. Beta Compensation and Resistance Error Correction automatically correct for most diode ideality errors, therefore it is not recommended that these settings be updated without consulting SMSC.

Table 6.18 Ideality Factor Look-Up Table (Diode Model)

SETTING	FACTOR	SETTING	FACTOR	SETTING	FACTOR
08h	0.9949	18h	1.0159	28h	1.0371
09h	0.9962	19h	1.0172	29h	1.0384
0Ah	0.9975	1Ah	1.0185	2Ah	1.0397
0Bh	0.9988	1Bh	1.0200	2Bh	1.0410
0Ch	1.0001	1Ch	1.0212	2Ch	1.0423
0Dh	1.0014	1Dh	1.0226	2Dh	1.0436
0Eh	1.0027	1Eh	1.0239	2Eh	1.0449
0Fh	1.0040	1Fh	1.0253	2Fh	1.0462
10h	1.0053	20h	1.0267	30h	1.0475
11h	1.0066	21h	1.0280	31h	1.0488
12h	1.0080	22h	1.0293	32h	1.0501
13h	1.0093	23h	1.0306	33h	1.0514
14h	1.0106	24h	1.0319	34h	1.0527
15h	1.0119	25h	1.0332	35h	1.0540
16h	1.0133	26h	1.0345	36h	1.0553
17h	1.0146	27h	1.0358	37h	1.0566

For CPU substrate transistors that require the BJT transistor model, the ideality factor behaves slightly differently than for discrete diode-connected transistors. Refer to [Table 6.19, "Substrate Diode Ideality Factor Look-Up Table \(BJT Model\)"](#) when using a CPU substrate transistor.

Table 6.19 Substrate Diode Ideality Factor Look-Up Table (BJT Model)

SETTING	FACTOR	SETTING	FACTOR	SETTING	FACTOR
08h	0.9869	18h	1.0079	28h	1.0291
09h	0.9882	19h	1.0092	29h	1.0304
0Ah	0.9895	1Ah	1.0105	2Ah	1.0317
0Bh	0.9908	1Bh	1.0120	2Bh	1.0330
0Ch	0.9921	1Ch	1.0132	2Ch	1.0343
0Dh	0.9934	1Dh	1.0146	2Dh	1.0356
0Eh	0.9947	1Eh	1.0159	2Eh	1.0369
0Fh	0.9960	1Fh	1.0173	2Fh	1.0382
10h	0.9973	20h	1.0187	30h	1.0395
11h	0.9986	21h	1.0200	31h	1.0408

Table 6.19 Substrate Diode Ideality Factor Look-Up Table (BJT Model) (continued)

SETTING	FACTOR	SETTING	FACTOR	SETTING	FACTOR
12h	1.0000	22h	1.0213	32h	1.0421
13h	1.0013	23h	1.0226	33h	1.0434
14h	1.0026	24h	1.0239	34h	1.0447
15h	1.0039	25h	1.0252	35h	1.0460
16h	1.0053	26h	1.0265	36h	1.0473
17h	1.0066	27h	1.0278	37h	1.0486

APPLICATION NOTE: When measuring a 65nm Intel CPUs, the Ideality Setting should be the default 12h. When measuring 45nm Intel CPUs, the Ideality Setting should be 15h.

6.15 High Limit Status Register

Table 6.20 High Limit Status Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
35h	R-C	High Limit Status	-	-	-	-	E3HIGH	E2HIGH	E1HIGH	IHIGH	00h

The High Limit Status Register contains the status bits that are set when a temperature channel high limit is exceeded. If any of these bits are set, then the HIGH status bit in the Status Register is set. Reading from the High Limit Status Register will clear all bits if. Reading from the register will also clear the HIGH status bit in the Status Register.

The $\overline{\text{ALERT}}$ pin will be set if the programmed number of consecutive alert counts have been met and any of these status bits are set.

The status bits will remain set until read unless the $\overline{\text{ALERT}}$ pin is configured as a comparator output (see Section 5.3.2, "ALERT Pin Comparator Mode").

Bit 3 - E3HIGH - This bit is set when the External Diode 3 channel exceeds its programmed high limit.

Bit 2 - E2HIGH - This bit is set when the External Diode 2 channel exceeds its programmed high limit.

Bit 1 - E1HIGH - This bit is set when the External Diode 1 channel exceeds its programmed high limit.

Bit 0 - IHIGH - This bit is set when the Internal Diode channel exceeds its programmed high limit.

6.16 Low Limit Status Register

Table 6.21 Low Limit Status Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
36h	R-C	Low Limit Status	-	-	-	-	E3LOW	E2LOW	E1LOW	ILOW	00h

The Low Limit Status Register contains the status bits that are set when a temperature channel drops below the low limit. If any of these bits are set, then the LOW status bit in the Status Register is set. Reading from the Low Limit Status Register will clear all bits. Reading from the register will also clear the LOW status bit in the Status Register.

The $\overline{\text{ALERT}}$ pin will be set if the programmed number of consecutive alert counts have been met and any of these status bits are set.

The status bits will remain set until read unless the $\overline{\text{ALERT}}$ pin is configured as a comparator output (see [Section 5.3.2, "ALERT Pin Comparator Mode"](#)).

Bit 3 - E3LOW - This bit is set when the External Diode 3 channel drops below its programmed low limit.

Bit 2 - E2LOW - This bit is set when the External Diode 2 channel drops below its programmed low limit.

Bit 1 - E1LOW - This bit is set when the External Diode 1 channel drops below its programmed low limit.

Bit 0 - ILOW - This bit is set when the Internal Diode channel drops below its programmed low limit.

6.17 THERM Limit Status Register

Table 6.22 THERM Limit Status Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
37h	R-C	THERM Limit Status	-	-	-	-	-E3 THERM	E2 THERM	E1 THERM	ITHERM	00h

The THERM Limit Status Register contains the status bits that are set when a temperature channel THERM Limit is exceeded. If any of these bits are set, then the THERM status bit in the Status Register is set. Reading from the THERM Limit Status Register will not clear the status bits. Once the temperature drops below the THERM Limit minus the THERM Hysteresis, the corresponding status bits will be automatically cleared. The THERM bit in the Status Register will be cleared when all individual channel THERM bits are cleared.

Bit 3 - E3THERM - This bit is set when the External Diode 3 channel exceeds its programmed THERM Limit. When set, this bit will assert the $\overline{\text{THERM}}$ pin.

Bit 2 - E2THERM - This bit is set when the External Diode 2 channel exceeds its programmed THERM Limit. When set, this bit will assert the $\overline{\text{THERM}}$ pin.

Bit 1 - E1THERM - This bit is set when the External Diode 1 channel exceeds its programmed THERM limit. When set, this bit will assert the $\overline{\text{THERM}}$ pin.

Bit 0- ITHERM - This bit is set when the Internal Diode channel exceeds its programmed THERM limit. When set, this bit will assert the $\overline{\text{THERM}}$ pin.

6.18 Filter Control Register

Table 6.23 Filter Configuration Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
40h	R/W	Filter Control	-	-	-	-	-	-	FILTER[1:0]		00h

The Filter Configuration Register controls the digital filter on the External Diode 1 channel.

Bits 1-0 - FILTER[1:0] - Control the level of digital filtering that is applied to the External Diode temperature measurements as shown in [Table 6.24, "Filter Settings"](#). See Figure 5.4, "Temperature Filter Step Response" and Figure 5.5, "Temperature Filter Impulse Response" for examples on the filter behavior.

Table 6.24 Filter Settings

FILTER[1:0]		AVERAGING
1	0	
0	0	Disabled (default)
0	1	Level 1
1	0	Level 1
1	1	Level 2

6.19 Product ID Register

Table 6.25 Product ID Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
FDh	R	Product ID	0	0	1	0	0	0	0	1	21h EMC1413
FDh	R	Product ID	0	0	1	0	0	1	0	1	25h EMC1414

The Product ID Register holds a unique value that identifies the device.

6.20 SMSC ID Register (FEh)

Table 6.26 Manufacturer ID Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
FEh	R	SMSC ID	0	1	0	1	1	1	0	1	5Dh

The Manufacturer ID register contains an 8 bit word that identifies the SMSC as the manufacturer of the EMC1413 and EMC1414.

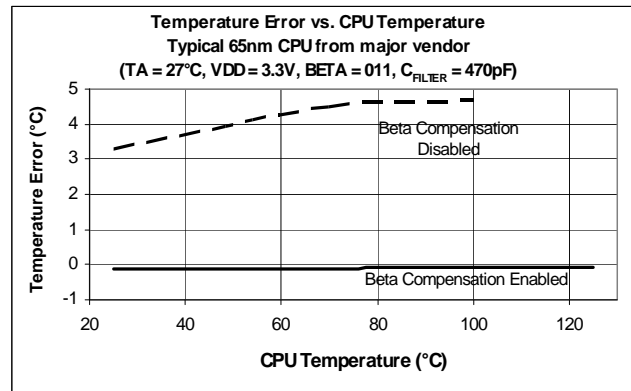
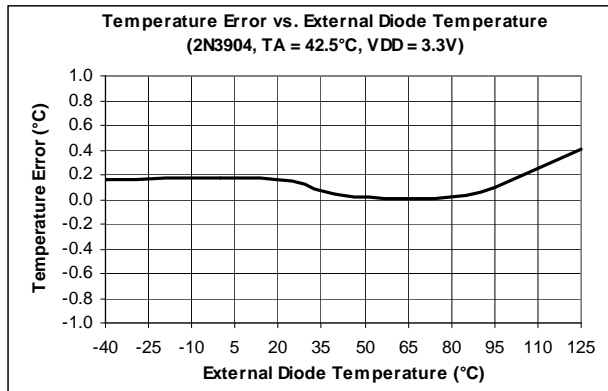
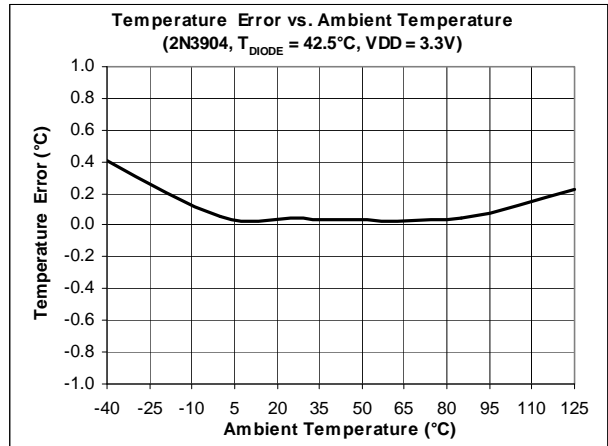
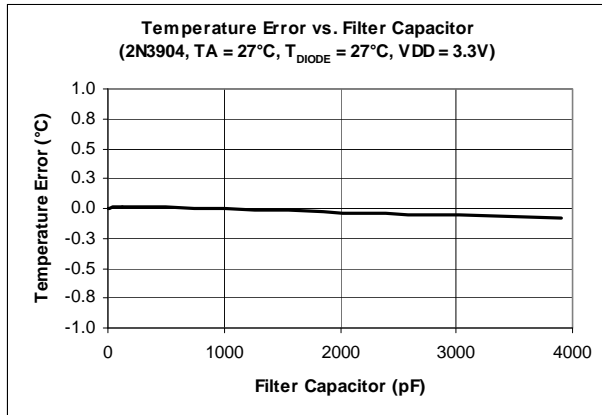
6.21 Revision Register (FFh)

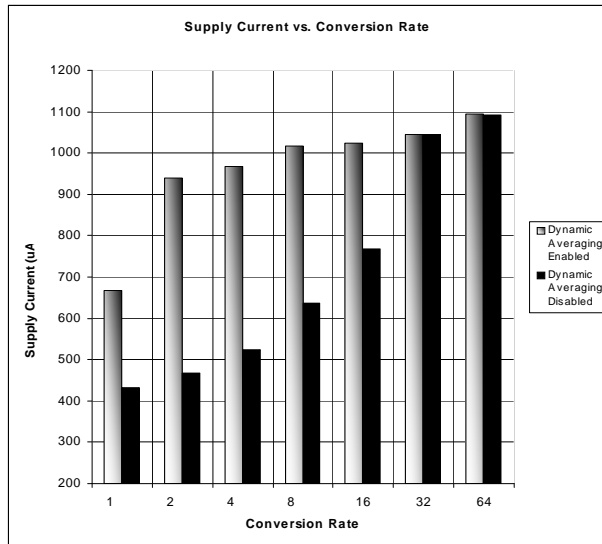
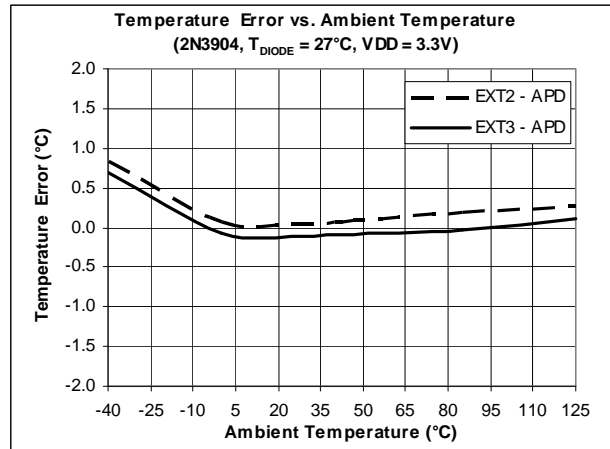
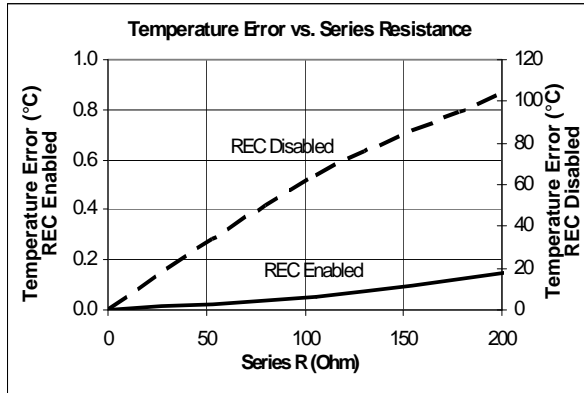
Table 6.27 Revision Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
FFh	R	Revision	0	0	0	0	0	0	1	1	03h

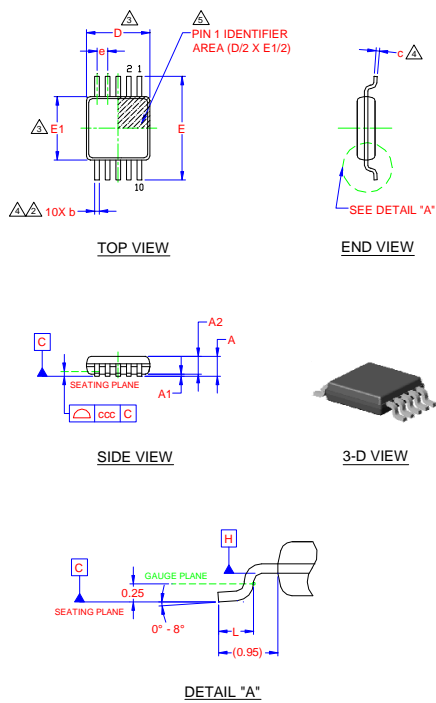
The Revision register contains an 8 bit word that identifies the die revision.

Chapter 7 Typical Operating Curves





Chapter 8 Package Information



REVISION	DESCRIPTION	DATE	RELEASED
A	INITIAL RELEASE		S.K.IJLIEV

COMMON DIMENSIONS					
SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	0.80	—	1.10	—	OVERALL PKG HEIGHT
A1	0.05	—	0.15	—	STANDOFF
A2	0.75	0.85	0.95	—	BODY THICKNESS
D	2.80	3.00	3.20	3	"X" BODY SIZE
E	4.65	4.90	5.15	—	LEAD SPAN
E1	2.80	3.00	3.20	3	"Y" BODY SIZE
L	0.40	—	0.80	—	LEAD FOOT LENGTH
b	0.17	—	0.27	2,4	LEAD WIDTH
c	0.08	—	0.23	4	LEAD FOOT THICKNESS
e	0.50 BSC		—	—	LEAD PITCH
ccc	0.00	—	0.10	—	COPLANARITY

- NOTES:
- ALL DIMENSIONS ARE IN MILLIMETER.
 - TOLERANCE ON THE TRUE POSITION OF EACH LEAD IS ± 0.04 mm AT MAXIMUM MATERIAL CONDITION.
 - PACKAGE BODY DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD/INTERLEAD PROTRUSIONS OR FLASH. MAXIMUM MOLD PROTRUSIONS OR FLASH IS 0.15 mm (0.006 INCHES) PER END AND SIDE. DIMENSIONS "D" AND "E1" ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY, INCLUDING ANY MISMATCH BETWEEN TOP AND BOTTOM PLASTIC BODY. THEY ARE DETERMINED AT DATUM PLANE "H".
 - DIMENSIONS "b" AND "c" APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 mm AND 0.15 mm FROM THE LEAD TIP.
 - DETAILS OF THE PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN MILLIMETERS AND TOLERANCES ARE:	MINOR ANGLES	DECIMAL	ANGULAR
0.05	0.05	0.05	0.05
0.10	0.10	0.10	0.10
0.25	0.25	0.25	0.25
0.50	0.50	0.50	0.50
1.00	1.00	1.00	1.00
2.00	2.00	2.00	2.00
3.00	3.00	3.00	3.00
4.00	4.00	4.00	4.00
5.00	5.00	5.00	5.00
6.00	6.00	6.00	6.00
7.00	7.00	7.00	7.00
8.00	8.00	8.00	8.00
9.00	9.00	9.00	9.00
10.00	10.00	10.00	10.00
11.00	11.00	11.00	11.00
12.00	12.00	12.00	12.00
13.00	13.00	13.00	13.00
14.00	14.00	14.00	14.00
15.00	15.00	15.00	15.00
16.00	16.00	16.00	16.00
17.00	17.00	17.00	17.00
18.00	18.00	18.00	18.00
19.00	19.00	19.00	19.00
20.00	20.00	20.00	20.00
21.00	21.00	21.00	21.00
22.00	22.00	22.00	22.00
23.00	23.00	23.00	23.00
24.00	24.00	24.00	24.00
25.00	25.00	25.00	25.00
26.00	26.00	26.00	26.00
27.00	27.00	27.00	27.00
28.00	28.00	28.00	28.00
29.00	29.00	29.00	29.00
30.00	30.00	30.00	30.00
31.00	31.00	31.00	31.00
32.00	32.00	32.00	32.00
33.00	33.00	33.00	33.00
34.00	34.00	34.00	34.00
35.00	35.00	35.00	35.00
36.00	36.00	36.00	36.00
37.00	37.00	37.00	37.00
38.00	38.00	38.00	38.00
39.00	39.00	39.00	39.00
40.00	40.00	40.00	40.00
41.00	41.00	41.00	41.00
42.00	42.00	42.00	42.00
43.00	43.00	43.00	43.00
44.00	44.00	44.00	44.00
45.00	45.00	45.00	45.00
46.00	46.00	46.00	46.00
47.00	47.00	47.00	47.00
48.00	48.00	48.00	48.00
49.00	49.00	49.00	49.00
50.00	50.00	50.00	50.00
51.00	51.00	51.00	51.00
52.00	52.00	52.00	52.00
53.00	53.00	53.00	53.00
54.00	54.00	54.00	54.00
55.00	55.00	55.00	55.00
56.00	56.00	56.00	56.00
57.00	57.00	57.00	57.00
58.00	58.00	58.00	58.00
59.00	59.00	59.00	59.00
60.00	60.00	60.00	60.00
61.00	61.00	61.00	61.00
62.00	62.00	62.00	62.00
63.00	63.00	63.00	63.00
64.00	64.00	64.00	64.00
65.00	65.00	65.00	65.00
66.00	66.00	66.00	66.00
67.00	67.00	67.00	67.00
68.00	68.00	68.00	68.00
69.00	69.00	69.00	69.00
70.00	70.00	70.00	70.00
71.00	71.00	71.00	71.00
72.00	72.00	72.00	72.00
73.00	73.00	73.00	73.00
74.00	74.00	74.00	74.00
75.00	75.00	75.00	75.00
76.00	76.00	76.00	76.00
77.00	77.00	77.00	77.00
78.00	78.00	78.00	78.00
79.00	79.00	79.00	79.00
80.00	80.00	80.00	80.00
81.00	81.00	81.00	81.00
82.00	82.00	82.00	82.00
83.00	83.00	83.00	83.00
84.00	84.00	84.00	84.00
85.00	85.00	85.00	85.00
86.00	86.00	86.00	86.00
87.00	87.00	87.00	87.00
88.00	88.00	88.00	88.00
89.00	89.00	89.00	89.00
90.00	90.00	90.00	90.00
91.00	91.00	91.00	91.00
92.00	92.00	92.00	92.00
93.00	93.00	93.00	93.00
94.00	94.00	94.00	94.00
95.00	95.00	95.00	95.00
96.00	96.00	96.00	96.00
97.00	97.00	97.00	97.00
98.00	98.00	98.00	98.00
99.00	99.00	99.00	99.00
100.00	100.00	100.00	100.00

Figure 8.1 10 Pin MSOP / TSSOP Package

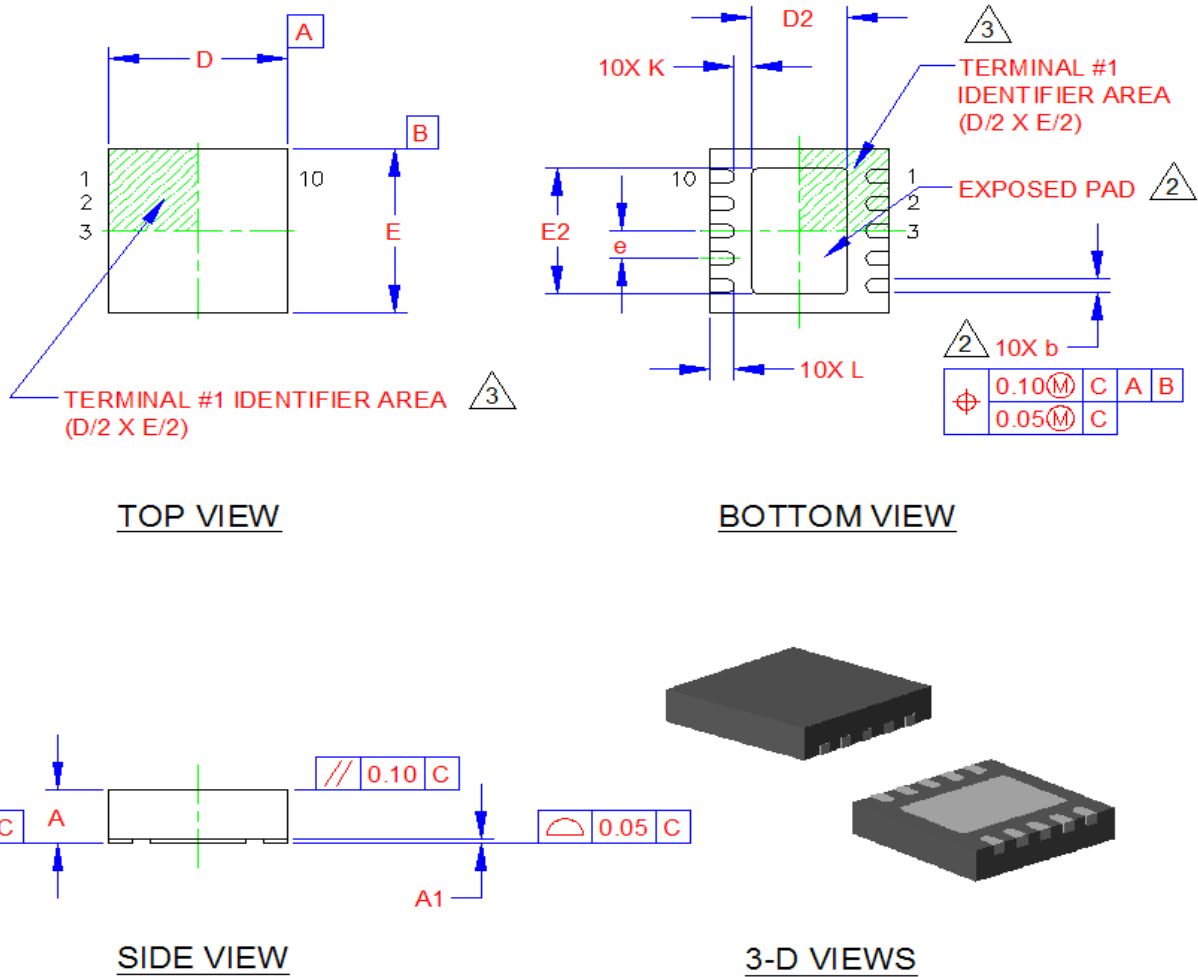
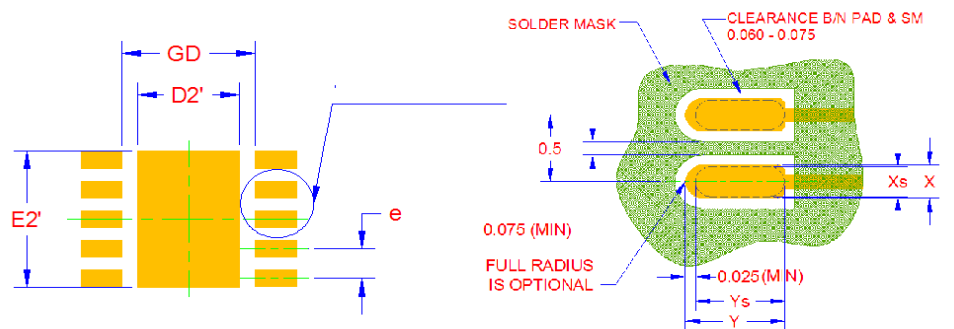


Figure 8.2 10 Pin DFN Package Drawing

COMMON DIMENSIONS					
SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	0.80	0.85	0.90	-	OVERALL PACKAGE HEIGHT
A1	0	0.02	0.05	-	STANDOFF
D/E	2.90	3.00	3.10	-	X/Y BODY SIZE
D2	1.50	1.60	1.70	2	X EXPOSED PAD SIZE
E2	2.20	2.30	2.40	2	Y EXPOSED PAD SIZE
L	0.35	0.40	0.45	-	TERMINAL LENGTH
b	0.18	0.25	0.30	2	TERMINAL WIDTH
K	0.25	0.30	-	-	TERMINAL TO PAD DISTANCE
e	0.50 BSC		-	-	TERMINAL PITCH

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. UNILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED PAD, AS WELL AS THE TERMINALS. DIMENSIONS "b" APPLIES TO PLATED TERMINALS AND IT IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
3. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE AREA INDICATED.

Figure 8.3 10 Pin DFN Package Dimensions

PCB LAND PATTERN

LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
GD	2.10	-	2.20
D2'	-	1.60	1.60
E2'	-	2.30	-
Pad: X	-	0.28	0.28
Pad: Y	-	0.69	0.69
e	0.50		

Figure 8.4 10 Pin DFN PCB Footprint

Datasheet

8.1 Package Markings

All EMC1413 devices will be marked as shown in [Figure 8.5](#) or [Figure 8.6](#).

All EMC1414 devices will be marked as shown in [Figure 8.7](#).

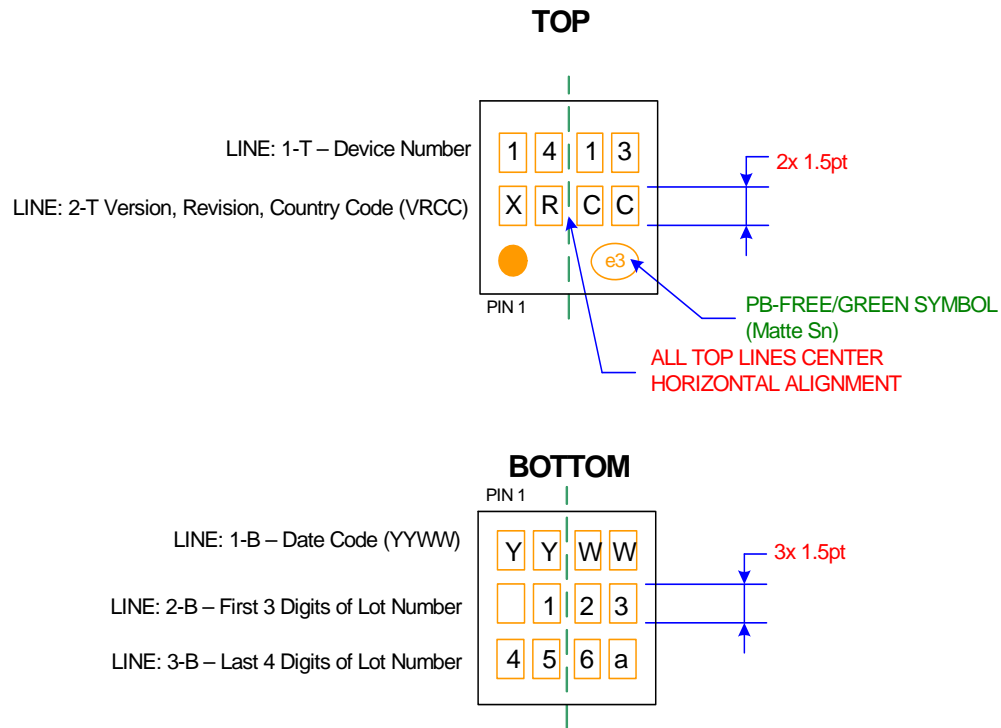
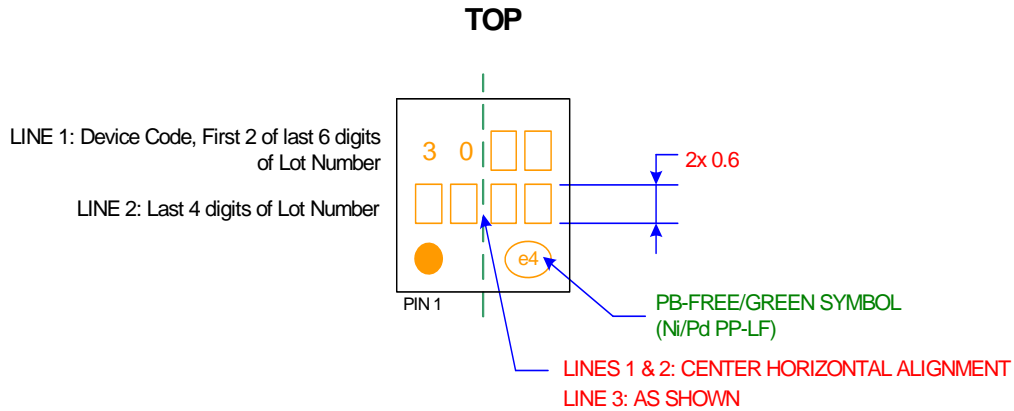


Figure 8.5 EMC1413-AIZL Package Marking for 10 Pin MSOP



BOTTOM

BOTTOM MARKING IS NOT ALLOWED

Figure 8.6 EMC1413-A-AIA Package Marking for 10 Pin DFN

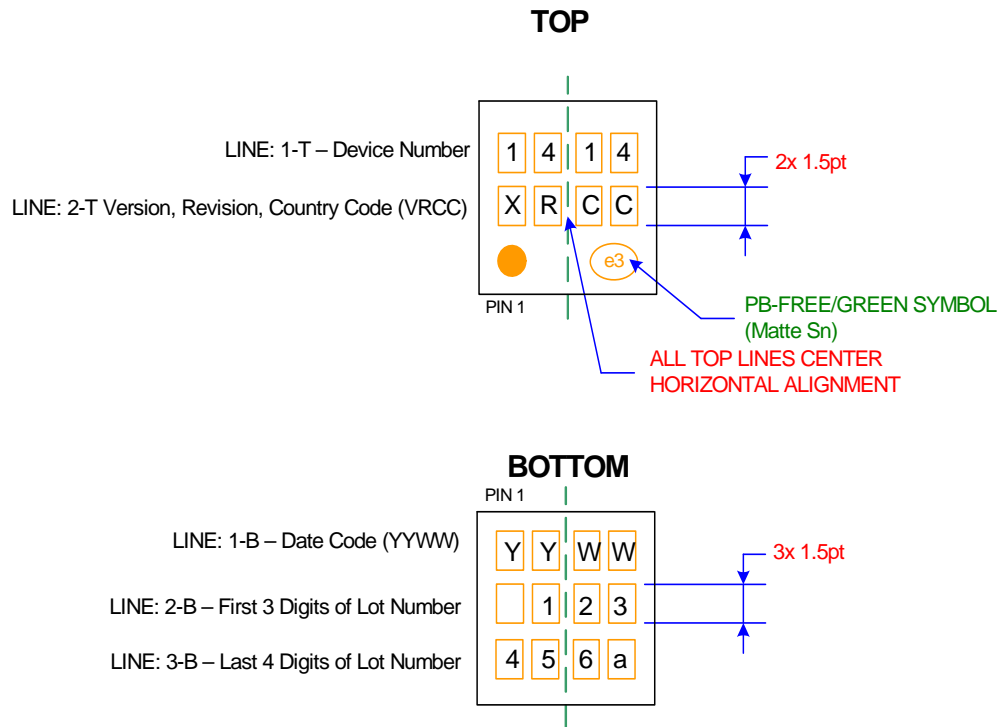
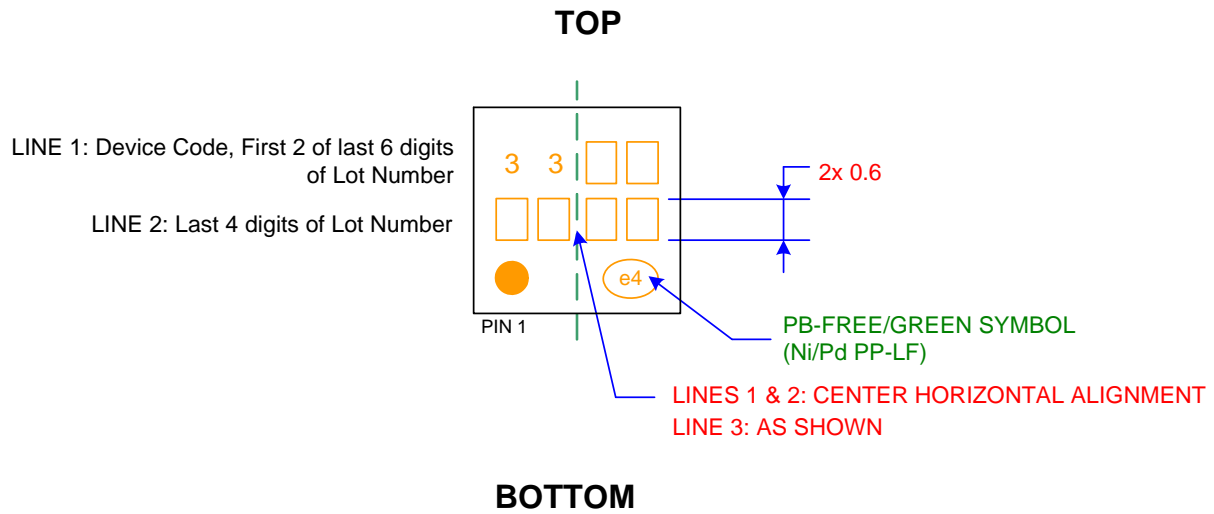


Figure 8.7 EMC1414 Package Marking



BOTTOM MARKING IS NOT ALLOWED

Figure 8.8 EMC1414-A-AIA Package Marking for 10 Pin DFN

Chapter 9 Revision History

Table 9.1 Customer Revision History

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
Rev. 1.37 (12-23-09)	Section 6.21, "Revision Register (FFh)"	Changed default from 01h to 03h to match the actual value.
	Ordering Information	Added EMC1414-A-AIA-TR in a 10-pin DFN
	Table 3.1, "Absolute Maximum Ratings"	Updated voltage on 5V tolerant pins with pull up from -0.3 to 3.6 to 0 to 3.6.
Rev. 1.35 (05-06-09)	Table 2.1, "EMC1413 and EMC1414 Pin Description"	Identified 5V tolerant pins. Added the following application note below table: "For the 5V tolerant pins that have a pull-up resistor (SMCLK, SMDATA, THERM, ALERT), the voltage difference between VDD and the pull-up voltage must never exceed 3.6V."
	Table 3.1, "Absolute Maximum Ratings"	Updated voltage limits for 5V tolerant pins with pull-up resistors. Added the following note below table: "For the 5V tolerant pins that have a pull-up resistor (SMCLK, SMDATA, THERM, ALERT), the pull-up voltage must not exceed 3.6V when the device is unpowered."
	Table 3.2, "Electrical Specifications"	Added leakage current
	Ordering Information and Table 1.1, "Part Selection"	Added EMC1414-3 and EMC1413-3
	Figure 8.2, "10 Pin DFN Package Drawing"	Updated figures for package
Rev. 1.34 (12-02-08)	Initial document creation	