National Semiconductor

LM9627 Color CMOS Image Sensor VGA 30 FPS

General Description

The LM9627 is a high performance, low power, third inch VGA CMOS Active Pixel Sensor capable of capturing color digital still or motion images and converting them to a digital data stream.

In addition to the active pixel array, an on-chip 12 bit A/D converter, fixed pattern noise elimination circuits and a video gain amplifier is provided. Furthermore, an integrated programmable smart timing and control circuit allows the user maximum flexibility in adjusting integration time, active window size, gain and frame rate. Various control, timing and power modes are also provided.

Features

- Supplied with micro lenses
- Video or snapshot operations
- Programmable pixel clock, inter-frame and inter-line delays.
- Programmable partial or full frame integration
- Programmable gain adjustment
- Horizontal & vertical sub-sampling (2:1 & 4:2)
- Windowing
- External snapshot trigger & event synchronisation signals
- Auto black level compensation
- Flexible digital video read-out supporting programmable:
  - polarity for synchronisation and pixel clock signals
  - leading edge adjustment for horizontal synchronization
- Programmable via 2 wire I^2C compatible serial interface
- Power on reset & power down mode

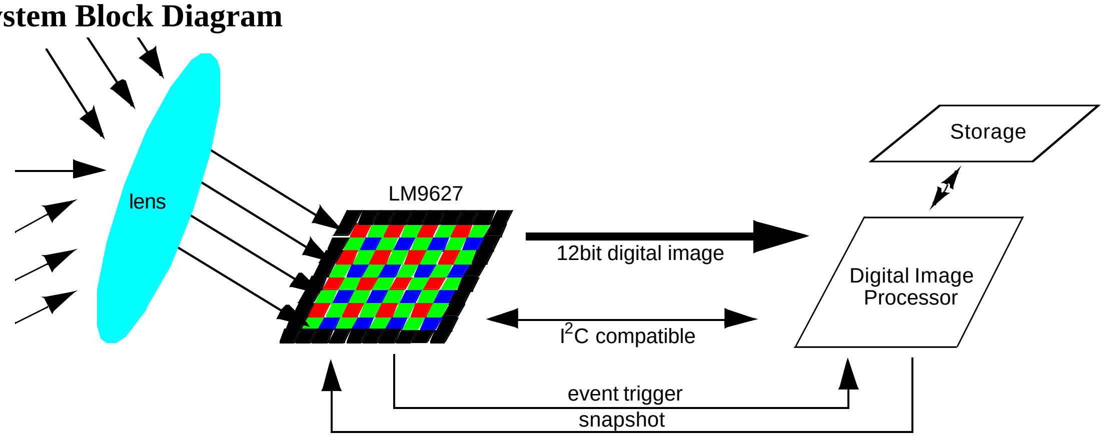
Applications

- PC Camera
- Digital Still Camera
- Video Conferencing
- Security Cameras
- Toys
- Machine Vision

Key Specifications

• Array Format	Total: 664H x 504V Active: 648H x 488V
• Effective Image Area	Total: 4.98mm x 3.78 mm Active: 4.86 mm x 3.66 mm
• Optical Format	1/3“
• Pixel Size	7.5µm x 7.5µm
• Video Outputs	8,10 & 12 Bit Digital
• Dynamic Range	57dB
• FPN	0.35%
• Sensitivity	
red	14.5 kLSBs/lux.s
green	7.5 kLSBs/lux.s
blue	5.1 kLSBs/lux.s
• Quantum Efficiency	27%
• Fill Factor	47% (no micro lens)
• Color Mosaic	Bayer pattern
• Package	48 LCC
• Single Supply	3.3 V
• Power Consumption	90 mW
• Operating Temp	0 to 50^oC

System Block Diagram



Overall Chip Block Diagram

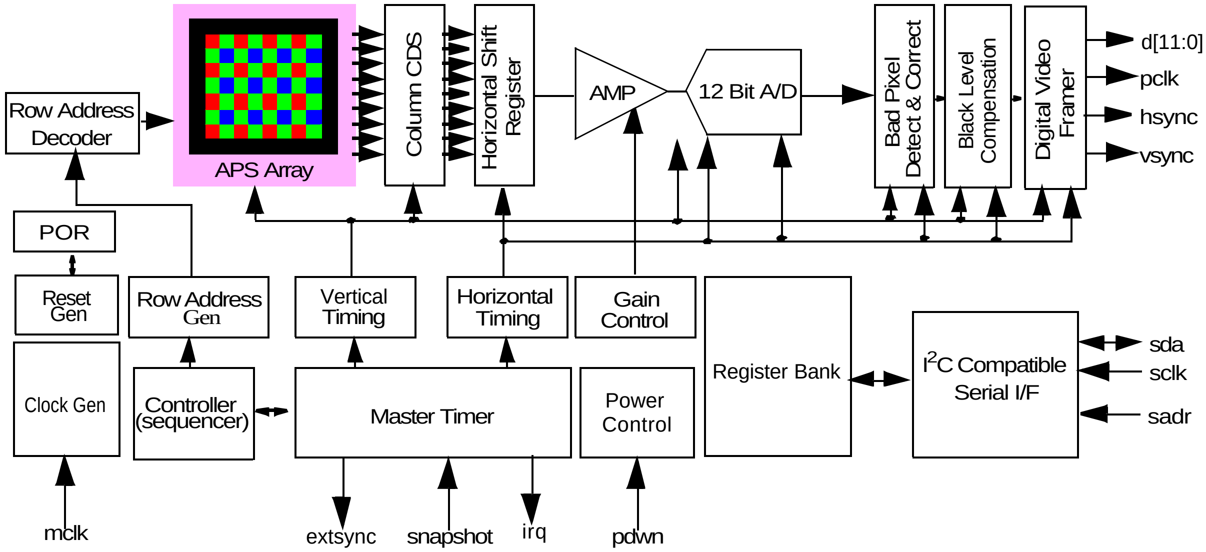
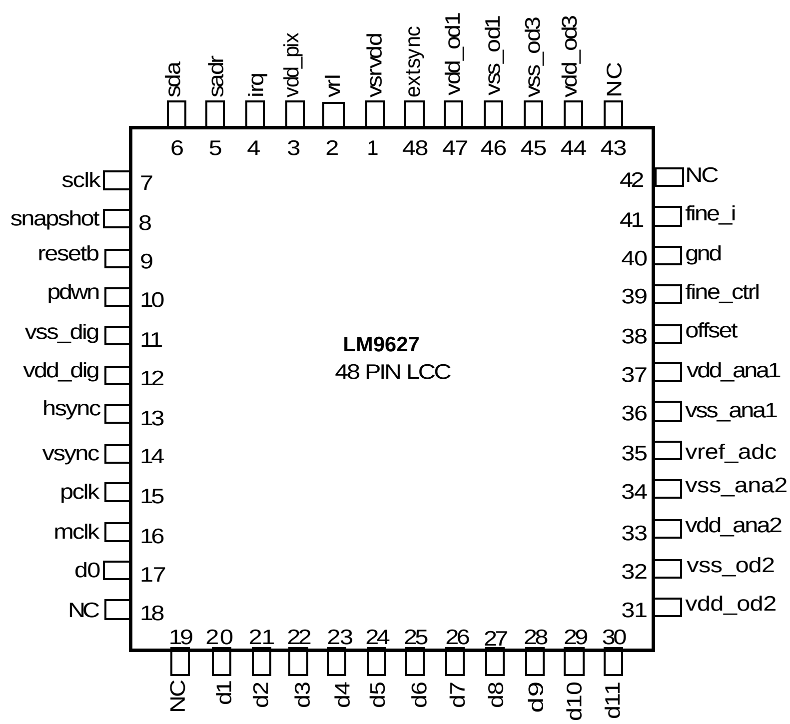


Figure 1. Chip Block Diagram

Connection Diagram



Ordering Information

Temperature ($0°C \leq T_A \leq +50°C$)	NS Package
LM9627 CCEA	LCC

Typical Application Circuit

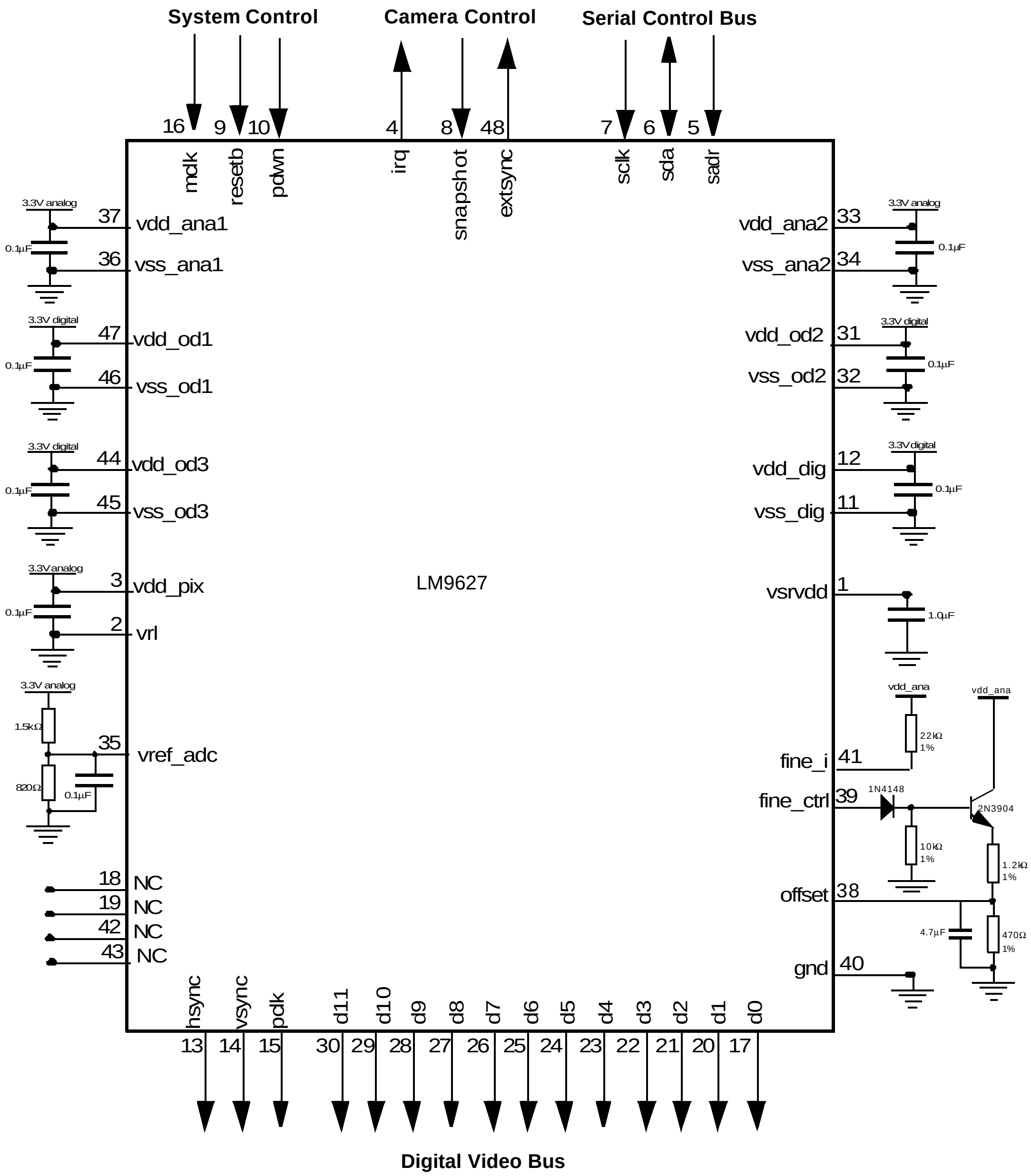


Figure 2. Typical Application Diagram

Scan Read Out Direction

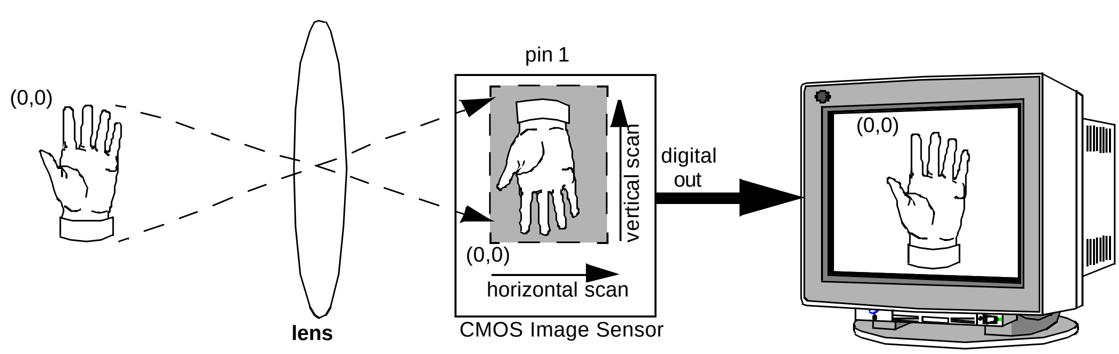


Figure 3. Scan directions and position of origin in imaging system

Pin Descriptions

Pin	Name	I/O	Typ	Description
1	vsrvdd	I0	P	Analog bidirectional, it should be connect to ground via a 1.0µf capacitor. This pin is the internal charge pump voltage source.
2	vrl	I	A	Anti blooming pin. This pin is normally tied to ground.
3	vdd_pix	I	P	3.3 volt supply for the pixel array.
4	irq	O	D	Digital output, the interrupt request pin. This pin generates interrupts during snapshot mode.
5	sadr	I	D	Digital input with pull down resistor. This pin is used to program different slave addresses for the sensor in an I^2C compatible system.
6	sda	IO	D	I^2C compatible serial interface data bus. The output stage of this pin has an open drain driver.
7	sclk	I	D	I^2C compatible serial interface clock.
8	snapshot	I	D	Digital input with pull down resistor used to activate (trigger) a snapshot sequence.
9	resetb	I	D	Digital input with pull up resistor. When forced to a logic 0 the sensor is reset to its default power up state. The *resetb* signal is internally synchronized to *mclk* which must be running for a reset to occur.
10	pdwn	I	D	Digital input with pull down resistor. When forced to a logic 1 the sensor is put into power down mode.
11	vss_dig	I	P	0 volt power supply for the digital circuits.
12	vdd_dig	I	P	3.3 volt power supply for the digital circuits.
13	hsync	IO	D	Digital Bidirectional. This is a dual mode pin. When the sensor's digital video port is configured to be a master, (the default), this pin is an output and is the horizontal synchronization pulse. When the sensor's digital video port is configured to be a slave, this pin is an input and is the row trigger.
14	vsync	IO	D	Digital Bidirectional. This is a dual mode pin. When the sensor's digital video port is configured to be a master, (the default), this pin is an output and is the vertical synchronization pulse. When the sensor's digital video port is configured to be a slave, this pin is an input and is the frame trigger.
15	pclk	O	D	Digital output. The pixel clock.
16	mclk	I	D	Digital input. The sensor's master clock input.
17	d0	O	D	Digital output. Bit 0 of the digital video output bus. This output can be put into tri-state mode.
18	NC			Pin not used, do not connect.
19	NC			Pin not used, do not connect.
20	d1	O	D	Digital output. Bit 1 of the digital video output bus. This output can be put into tri-state mode.
21	d2	O	D	Digital output. Bit 2 of the digital video output bus. This output can be put into tri-state mode.
22	d3	O	D	Digital output. Bit 3 of the digital video output bus. This output can be put into tri-state mode.
23	d4	O	D	Digital output. Bit 4 of the digital video output bus. This output can be put into tri-state mode.
24	d5	O	D	Digital output. Bit 5 of the digital video output bus. This output can be put into tri-state mode.
25	d6	O	D	Digital output. Bit 6 of the digital video output bus. This output can be put into tri-state mode.

Pin Descriptions (Continued)

Pin	Name	I/O	Typ	Description
26	d7	O	D	Digital output. Bit 7 of the digital video output bus. This output can be put into tri-state mode.
27	d8	O	D	Digital output. Bit 8 of the digital video output bus. This output can be put into tri-state mode.
28	d9	O	D	Digital output. Bit 9 of the digital video output bus. This output can be put into tri-state mode.
29	d10	O	D	Digital output. Bit 10 of the digital video output bus. This output can be put into tri-state mode.
30	d11	O	D	Digital output. Bit 11 of the digital video output bus. This output can be put into tri-state mode.
31	vdd_od2	I	P	3.3 volt supply for the digital IO buffers.
32	vss_od2	I	P	0 volt supply for the digital IO buffers
33	vdd_ana2	I	P	3.3 volt supply for analog circuits.
34	vss_ana2	I	P	0 volt supply for analog circuits.
35	vref_adc	I	A	A/D reference resistor ladder voltage. See figure 4 for equivalent circuit.
36	vss_ana1	I	P	0 volt supply for analog circuits.
37	vdd_ana1	I	P	3.3 volt supply for analog circuits.
38	offset	I	A	Analog input used to adjust the offset of the sensor. See figure 4 for equivalent circuit.
39	fine_ctrl	O	A	Analog output used to drive the *offset* pin.
40	gnd			This pin must be tied to ground.
41	fine_i	I	A	Bias current for the fine offset adjust.
42	NC			Pin not used, do not connect.
43	NC			Pin not used, do not connect.
44	vdd_od3	I	P	3.3 volt supply for the sensor.
45	vss_od3	I	P	0 volt supply for the sensor.
46	vss_od1	I	P	0 volt supply for the digital IO buffers
47	vdd_od1	I	P	3.3 volt supply for the digital IO buffers.
48	extsync	O	D	Digital output. The external event synchronization signal is used to synchronize external events in snapshot mode.

Legend: (I=Input), (O=Output), (IO=Bi-directional), (P=Power), (D=Digital), (A=Analog).

Figure 4. Equivalent Circuits For *adc_ref* and *offset* pins

Absolute Maximum Ratings (Notes 1 & 2)

Any Positive Supply Voltage	6.5V
Voltage On Any Input or Output Pin	-0.5V to 6.5V
Input Current at any pin (Note 3)	±25mA
ESD Susceptibility (Note 5)	
Human Body Model	2000V
Machine Model	200V
Package Input Current (Note 3)	±50mA
Package Power Dissipation @ T_A (Note 4)	2.5W
Soldering Temperature Infrared, 10 seconds (Note 6)	220°C
Storage Temperature	-40°C to 125°C

Operating Ratings (Notes 1 & 2)

Operating Temperature Range	0°C ≤T≤+50°C
All VDD Supply Voltages	+3.15V to +3.6V
Voltage Range on *vref_adc* pin	+0.6V to +1.0V
Voltage Range on *offset* pin	+0.04V to +0.4V

DC and logic level specifications

The following specifications apply for all VDD pins= +3.3V. **Boldface limits apply for TA = T_{MIN} to T_{MAX}:** all other limits T_A = 25°C (Note 7)

Symbol	Parameter	Conditions	Min note 9	Typical note 8	Max note 9	Units
sclk, sda, sadr, Digital Input/Output Characteristics						
VIH	Logical “1” Input Voltage		**0.7*vdd_od**		**vdd_od+0.5**	V
VIL	Logical “0” Input Voltage		**-0.5**		**0.3*vdd_od**	V
VOL	Logical “0” Output Voltage	vdd_od = +3.15V, Iout=3.0mA			**0.5**	V
V_{hys}	Hysteresis *(SCLK pin only)*	vdd_od = +3.15V	**0.05*vdd_od**			V
I_{leak}	Input Leakage Current	Vin=vss_od		-1		mA
mclk, snapshot, pdwn, resetb, hsync, vsync Digital Input Characteristics						
VIH	Logical “1” Input Voltage	vdd_dig = +3.6V	**2.0**			V
VIL	Logical “0” Input Voltage	vdd_dig = +3.15V			**0.8**	V
IIH	Logical “1” Input Current	VIH = vdd_dig		0.1		mA
IIL	Logical “0” Input Current	VIL = vss_dig		-1		mA
d0 - d11, pclk, hsync, vsync, extsync, irq, Digital Output Characteristics						
VOH	Logical “1” Output Voltage	vdd_od=3.15V, Iout=-1.6mA	**2.2**			V
VOL	Logical “0” Output Voltage	vdd_od=3.15V, Iout =-1.6mA			**0.5**	V
IOZ	TRI-STATE Output Current	VOUT = vss_od VOUT = vdd_od		-0.1 0.1		mA mA
IOS	Output Short Circuit Current			+/-17		mA
Power Supply Characteristics						
IA	Analog Supply Current	Power down mode, no clock. Operational mode in dark		700 19		mA mA
ID	Digital Supply Current	Power down mode, no clock. Operational mode in dark		300 7		mA mA

Power Dissipation Specifications

The following specifications apply for All VDD pins = +3.3V. **Boldface limits apply for TA = T_{MIN} to T_{MAX}:** all other limits T_A = 25°C.

Symbol	Parameter	Conditions	Min note 9	Typical note 8	Max note 9	Units
P_{dwn}	Power Down	no clock running		5		mW
PWR	Average Power Dissipation	mclk = 48Mhz & sensors default settings in dark.		90		mW

Video Amplifier Specifications

The following specifications apply for all VDD pins= +3.3V. **Boldface limits apply for TA = T_{MIN} to T_{MAX}**: all other limits T_A = 25°C.

Symbol	Parameter	Conditions	Min note 9	Typical note 8	Max note 9	Units
	Video Amplifier Nominal Gain	64 linear steps		0-15		dB

AC Electrical Characteristics

The following specifications apply for All VDD pins = +3.3V. **Boldface limits apply for T_A = T_{MIN} to T_{MAX}**: all other limits T_A = 25°C.

Symbol	Parameter	Conditions	Min note 9	Typical note 8	Max note 9	Units
F_{mclk}	Input Clock Frequency		**12**		**48**	MHz
T_{ch}	Clock High Time	@ CLK_{max}	**10**		**45**	ns
T_{cl}	Clock Low Time	@ CLK_{max}	**10**		**45**	ns
	Clock Duty Cycle	@ CLK_{max}	**45/55**		**55/45**	min/max
T_{rc}, T_{fc}	Clock Input Rise and Fall Time			3		ns
F_{hclk}	Internal System Clock Frequency		**1.0**		**14.0**	MHz
T_{reset}	Reset pulse width		**1.0**			µs
FRM_{rate}	Frame Rate		**1**		**30**	fps

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to VSS = vss_ana = vss_od = vss_dig = 0V, unless otherwise specified.

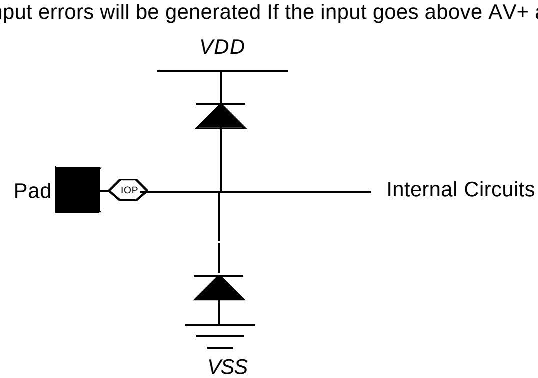
Note 3: When the voltage at any pin exceeds the power supplies (VIN < VSS or VIN > VDD), the current at that pin should be limited to 25mA. The 50mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25mA.

Note 4: The absolute maximum junction temperature (TJmax) for this device is 125°C. The maximum allowable power dissipation is dictated by TJmax, the junction-to-ambient thermal resistance (ΘJA), and the ambient temperature (T_A), and can be calculated using the formula PDMAX = (TJmax - T_A)/ΘJA. In the 48-pin LCC, ΘJA is 38.5°C/W, so PDMAX = 2.5W at 25°C and 1.94W at the maximum operating ambient temperature of 50°C. Note that the power dissipation of this device under normal operation will be well under the PDMAX of the package.

Note 5: Human body model is 100pF capacitor discharged through a 1.5kΩ resistor. Machine model is 220pF discharged through ZERO Ohms.

Note 6: See AN450, "Surface Mounting Methods and Their Effect on Product Reliability", or the section entitled "Surface Mount" found in any post 1986 National Semiconductor Linear Data Book, for other methods of soldering surface mount devices.

Note 7: The analog inputs are protected as shown below. Input voltage magnitude up to 500mV beyond the supply rails will not damage this device. However, input errors will be generated If the input goes above AV+ and below AGND.



Note 8: Typical figures are at TJ = 25°C, and represent most likely parametric norms.

Note 9: Test limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

CMOS Active Pixel Array Specifications

Parameter	Value	Units
Number of pixels (column, row) Total Active	664 x 504 648 x 488	pixels pixels
Array size (x,y Dimensions) Total Active	4.98 x 3.78 4.86 x 3.66	mm mm
Pixel Pitch	**7.5**	µ
Fill Factor (without micro-lens)	**47**	%

Image Sensor Specifications

The following specifications apply for All VDD pins = +3.3V, T_A = 25^{o}C, Illumination Color Temperature = 2850^{o}K, IR cutoff filter at 700nm, *mclk* = 48MHz, frame rate = 30Hz, *vref_adc* = 0.6 volt, video gain 0dB.

Parameter	Conditions	Min	Typical note 1	Max	Units
Optical Sensitivity @ A/D output red green blue			14.5 7.5 5.1		kLSBs/(lux.s)
Optical Sensitivity @ A/D input red green blue			2.12 1.1 0.75		volt/(lux.s)
Dynamic Range			57		dB
Read Noise			5.3		LSBs
Offset Fixed Pattern Noise	RMS value of pixel FPN in dark as a percentage of full scale.		0.35		%
Sensitivity Fixed Pattern Noise	RMS variation of pixel sensitivities as a percentage of the average sensitivity.		1		%

Note 1: Typical figures are at TJ = 25^{o}C, and represent most likely parametric norms.

Sensor Response Curves

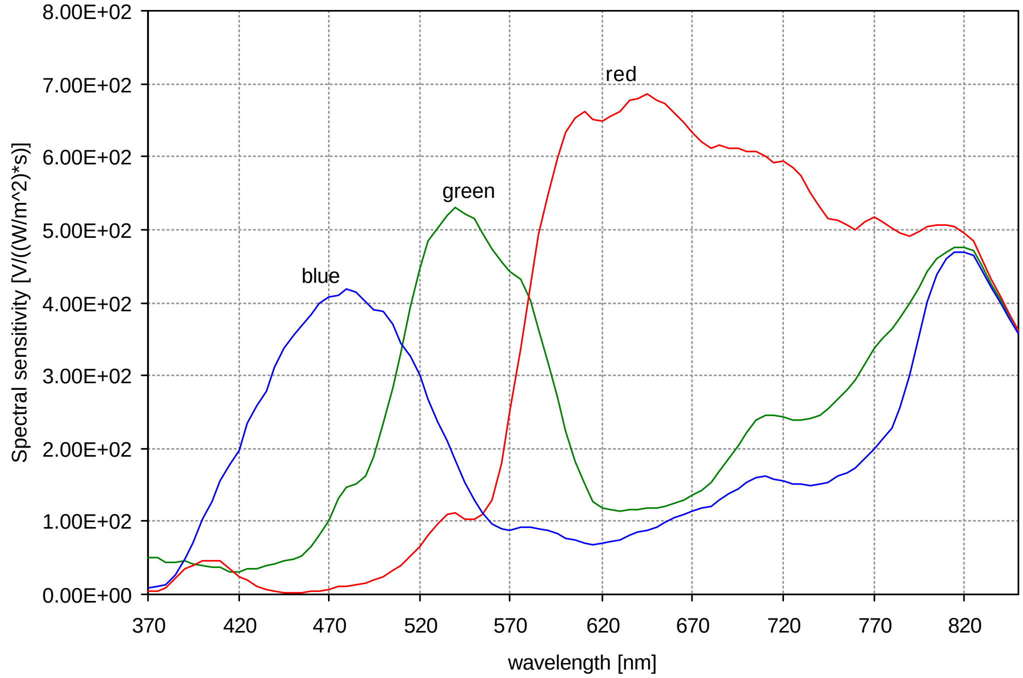


Figure 5. Spectral Response Curve

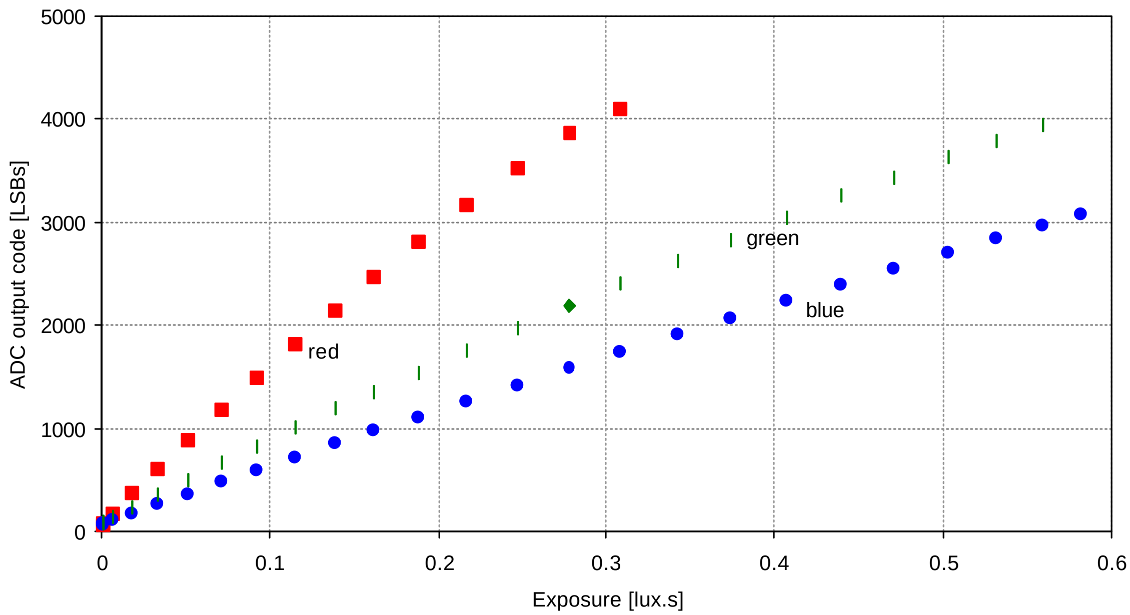


Figure 6. Linearity Response Curve

Functional Description

1.0 OVERVIEW

1.1 Light Capture and Conversion

The LM9627 contains a CMOS active pixel array consisting of 648 rows by 488 columns. This active region is surrounded by 8 columns and 8 rows of optically shielded (black) pixels as shown in Figure7.

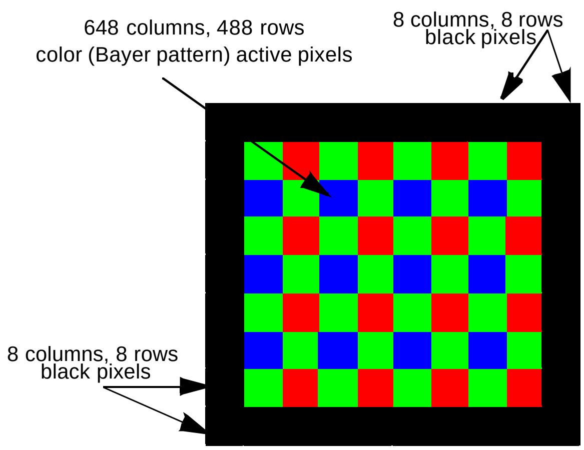


Figure 7: CMOS APS region of the LM9627

The color filters are Bayer pattern coded starting at row 8 and column 8. (rows 0 to 7 & columns 0 to 7 are black). The color coding is green, red, green, red until the end of row 8, then blue, green, blue, green until the end or row 9 and so on (see Figure 7).

At the beginning of a given integration time the on-board timing and control circuit will reset every pixel in the array one row at a time as shown in Figure 8. Note that all pixels in the same row are simultaneously reset, but not all pixels in the array.

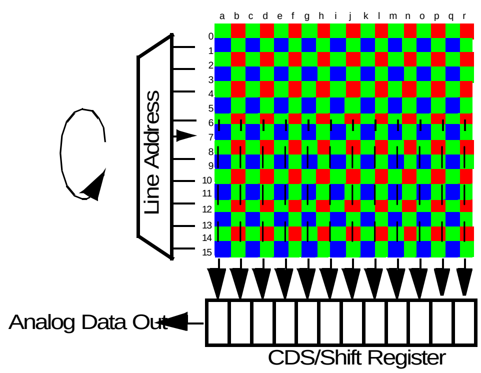


Figure 8: CMOS APS Row and Column addressing scheme

At the end of the integration time, the timing and control circuit will address each row and simultaneously transfer the integrated value of the pixel to a correlated double sampling circuit and then to a shift register as shown in Figure 8.

Once the correlated double sampled data has been loaded into the shift register, the timing and control circuit will shift them out one pixel at a time starting with column "a".

The pixel data is then fed into an analog video amplifier, where a user programmed gain is applied (see Figure 9).

After gain adjustment the analog value of each pixel is converted to a 12 bit digital data as shown in Figure 9.

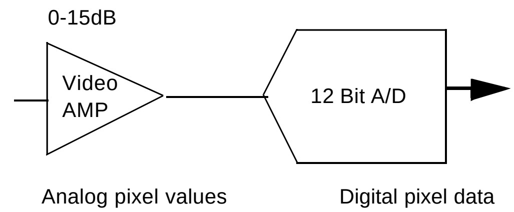


Figure 9: Analog Signals Conditioning & Conversion to Digital

The digital pixel data is further processed to:

- remove defects due to bad pixels,
- compensate black level, before being framed and presented on the digital output port. (see Figure 10).

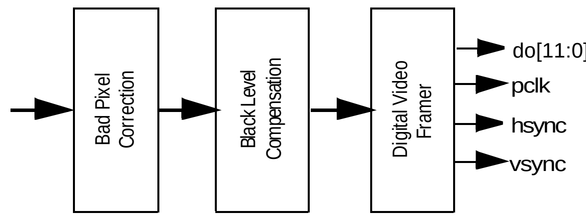


Figure 10. Digital Pixel Processing.

1.2 Program and Control Interfaces

The programming, control and status monitoring of the LM9627 is achieved through a two wire I²C compatible serial bus. In addition, a slave address pin is provided (see Figure 11).

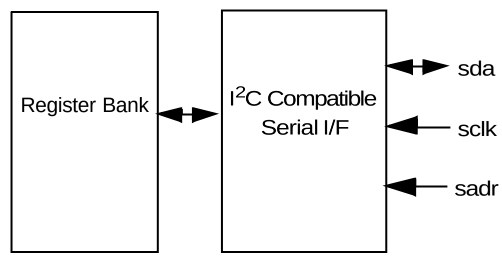


Figure 11. Control Interface to the LM9627.

Additional control and status pins: snapshot and external event synchronization are provided allowing the latency of the serial control port to be bypassed during single frame capture. An interrupt request pin is also available allowing complex snapshot operations to be controlled via an external micro-processor (see Figure 12).

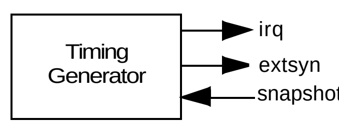


Figure 12. Snapshot & External Event Trigger Signals

Functional Description (continued)

2.0 WINDOWING

The integrated timing and control circuit allows any size window in any position within the active region of the array to be read out with a 1x1 pixel resolution. The window read out is called the "*Display Window*".

A "*Scan Window*" must be defined first, by programing the start and end row addresses as shown in Figure 13. Four coordinates (start row address, start column address, end row address & end column address) are programmed to define the size and location of the "*Display Window*" to be read out (*see Figure 13*).

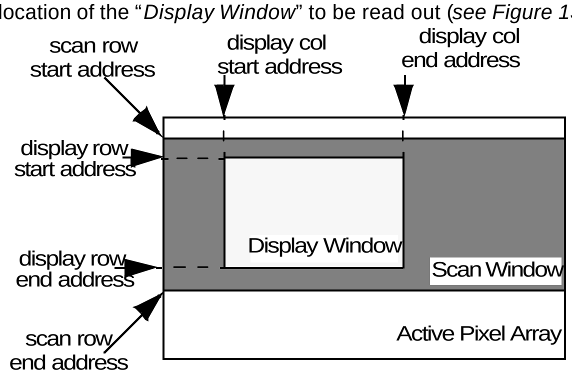


Figure 13. Windowing

Notes:
- The "*Display Window*" must always be defined within the "*Scan Window*".
- A "*Display Window*" can only be read out in the progressive scan mode.
- By default the "*Display Window*" is the complete array.

2.1 Programming the scan window

Two registers (SROWS & SROWE) are provided to program the size of the *scan window.* The start and end row address of the *scan window* is given by:

scan row start address = (2 SwStartRow) + SwLsb*

scan row end address = (2 SwEndRow) + 1 + SwLsb*

Where:

SwStartRow
: is the contents of the *Scan Window* start row register (SROWS)

SwEndROW
: is the contents of the *Scan Window* end row register (SROWE)

SwLsb
: is bit 6 of the *Display Window* LSB register (DWLSB)

2.2 Programming the display window

Five register (DROWS, DROWE, DCOLS, DCOLE and DWLSB) are provided to program the display window as described in the register section of this datasheet.

3.0 READ OUT MODES

3.1 Progressive Scan Readout Mode

In progressive scan readout mode, every pixel in every row in the display window is consecutively read out, one pixel at a time, starting with the left most pixel in the top most row. Hence, for the example shown in Figure 14, the read out order will be *a0,b0,...,r0* then *a1,b1,...,r1* and so on until pixel *r20* is read out.

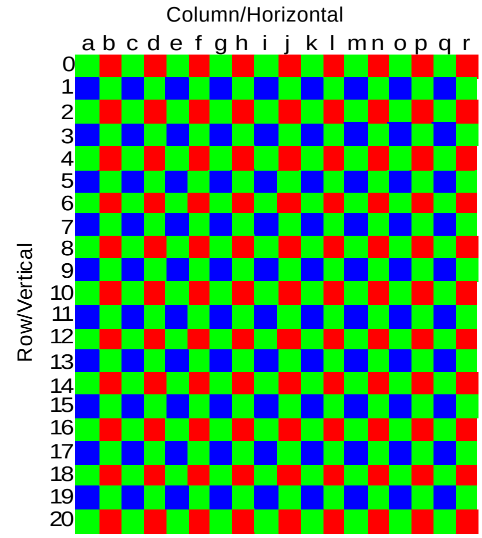


Figure 14: Progressive Scan Read Out Mode

3.2 Interlaced Readout Mode

In interlaced readout mode, pixels are read out in two fields, an *Odd Field* followed by an *Even Field*.

The *Odd Field,* consisting of all even row pairs contained within the display window, is read out first. Each pixel in the "*Odd Field*" is consecutively read out, one pixel at a time, starting with the left most pixel in the top most row pair.

The *Even Field,* consisting of all odd row pairs contained within the display window, is then read out. Each pixel in the "*Even Field*" is consecutively read out, one pixel at a time, starting with the left most pixel in the top most row pair.

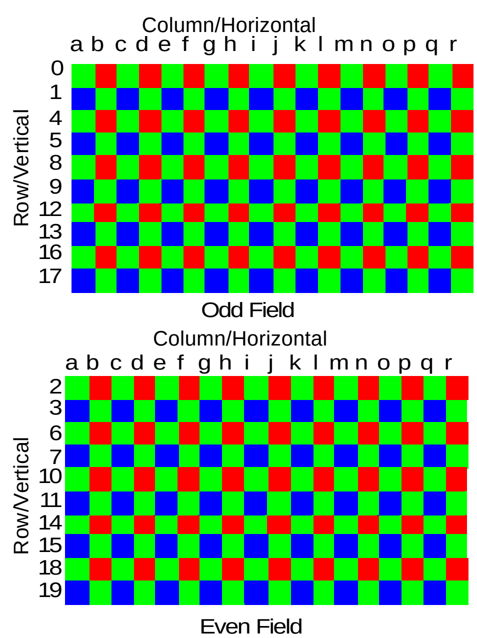


Figure 15: Interlace Read Out Mode

Hence, for the example shown in Figure 15, the display window is broken up into two fields, as shown in Figure 15. Pixels *a0,b0,...,r0* and *a1,b1,...,r1 are readout first* and so on until pixels *a17,b17,...r17* in the even field are read out. The even field read out is followed by pixels in the odd field, a2,b2,...,r2 then a3,b3,...,r3 until pixels a19,b19,...,r19

Functional Description (continued)

4.0 SUBSAMPLING MODES

4.1 2:1 Sub-Sampling

The timing and control circuit can be programmed to sub-sample pixels in the display window vertically, horizontally or both, with an aspect ratio of 2:1 as illustrated in Figure 16.

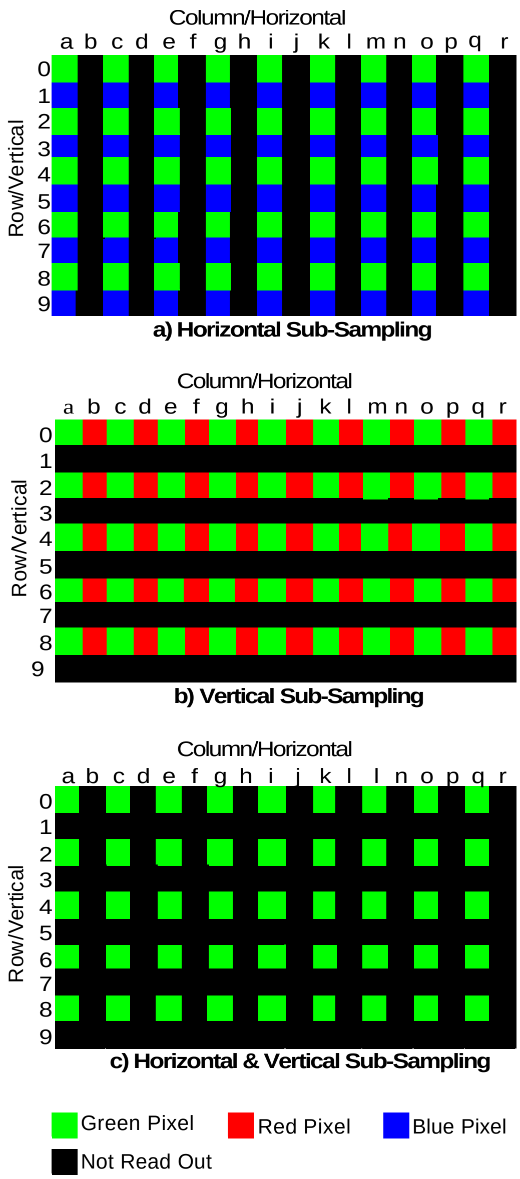


Figure 16: Example of 2:1 Sub-sampling

4.2 4:2 Sub-Sampling

The timing and control circuit can be programmed to sub-sample pixels in the display window vertically, horizontally or both, with an aspect ratio of 4:2 as illustrated in Figure 17

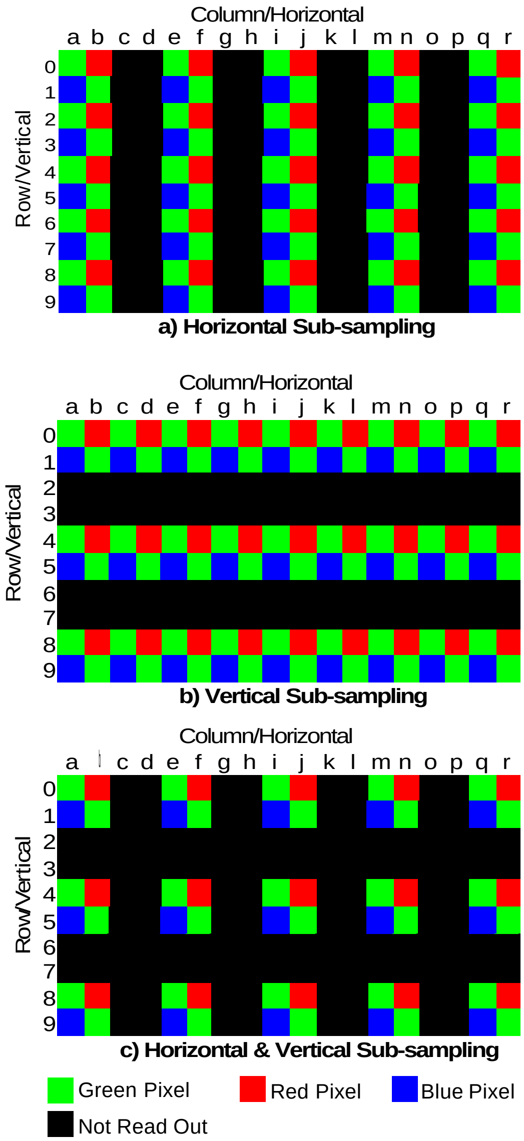


Figure 17: Example 4:2 Sub-sampling

Functional Description (continued)

5.0 SNAPSHOT MODE

The LM9627 is capable of capturing a single frame of an image under hardware or software control, with or without the aid of an external shutter. Two registers, SNAPSHOTMODE0 & SNAPSHOTMODE1, are provided to program, monitor and control all snapshot sequences.

5.1 Software Controlled Snapshots

The snapshot mode events can be software controlled by writing to and reading from the snapshot mode registers over the I^2C compatible interface.

5.2 Hardware Controlled Snapshots

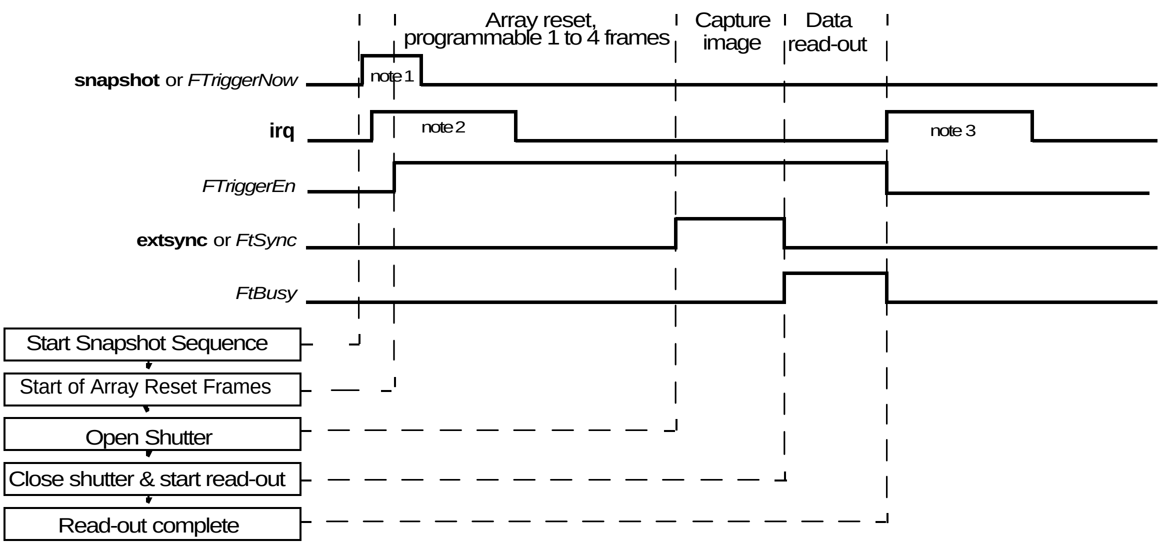
Two dedicated pins are provided on the LM9627, **snapshot** & **extsync**, allowing the snapshot mode events to be controlled by hardware. The **snapshot** pin must be enabled by writing to the *SnapEnable* bit of the MCFG0 register.

5.3 Auto Snapshot Mode

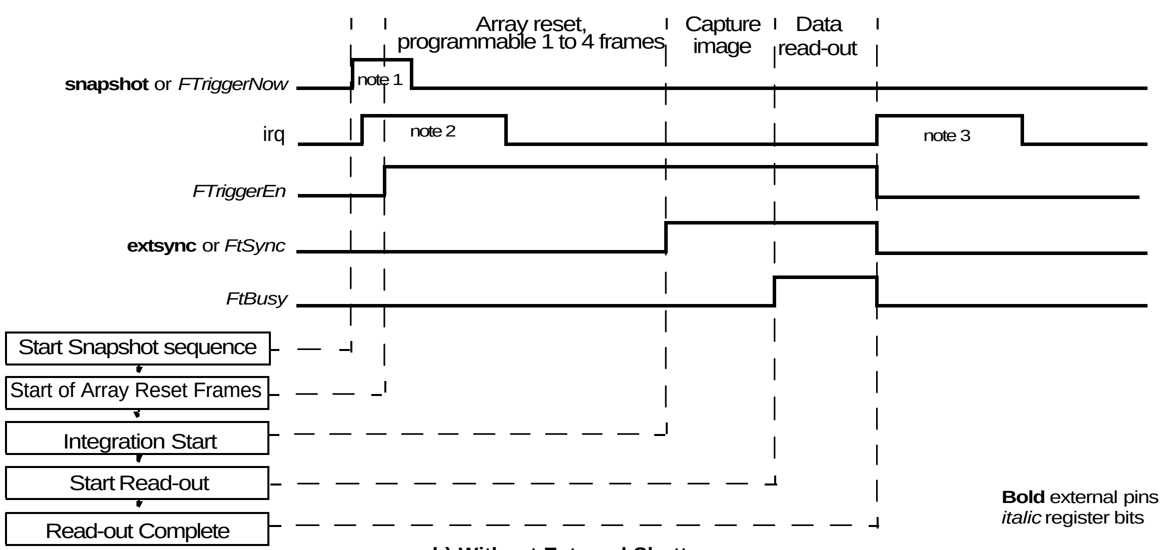
In auto snapshot mode (see figure 20), upon the receipt of a **snapshot** or *FTriggerNow* trigger signal, the integrated timing and control circuit will set the *FTriggerEN* bit and generate an internal TRIGGER signal (see figure 19), thus resetting the array one row at a time. At end of the reset cycle the timing and control circuit will signal the shutter to open via **extsync** pin or *FtSync* bit. At the end of the programmed integration time the shutter will be signalled to close, and the pixel read-out will commence as shown in figure 18a. At the end of the read-out sequence the *FTriggerEN* will be automatically reset and the sensor will return to video capture mode as shown in figure 20.

If an external shutter is not available then at least two frames need to be taken so that the pixels can be integrated over one frame as shown in Figure 18b.

To use auto snapshot mode the *SsEngage* bit of the SNAPSHOTMODE1 register must be set to zero.



a) With External Shutter



b) Without External Shutter

Note 1: This wave form shows the **snapshot** pin programmed to the default pulse mode.
Note 2: The **irq** pulse is taken low when the snapshot trigger interrupt flag (*SsTrigFlag*) in the snapshot mode1 (*SNAPMODE1*) register is read.
Note 3: The **irq** pulse is taken low when the snapshot trigger interrupt flag (*SsRdFlag*) in the snapshot mode1 (*SNAPMODE1*) register is read.

Figure 18. Snapshot Mode

Functional Description (continued)

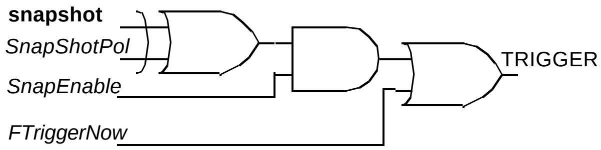


Figure 19. Snapshot Trigger Generation Logic

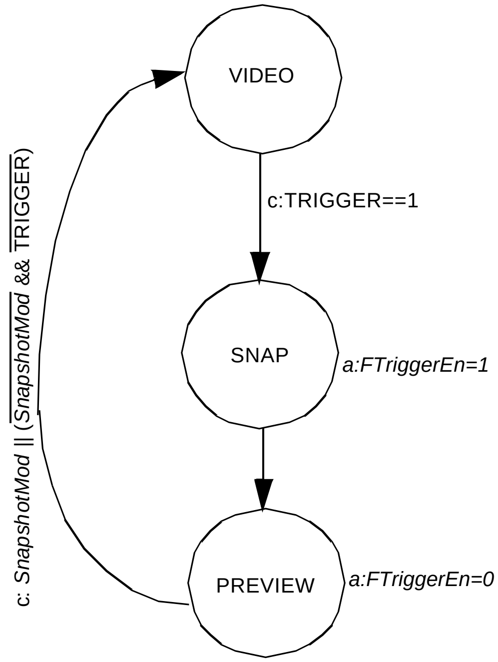


Figure 20. Auto Snapshot Mode State Diagram

5.4 CPU Snapshot Mode

In CPU snapshot mode, the *FTriggerEN* is not set automatically and an Interrupt generator can be enabled.

Hence, upon the receipt of a **snapshot** or *FTriggerNow* trigger signal, the integrated timing and control circuit will generate an internal TRIGGER signal as shown in figure 19 and then wait in the IRQ state for the *FTriggerEN* bit to be manually set as shown in figure 21.

Once the *FtriggerEn* bit is set the integrated timing and control circuit will start resetting the array one row at a time. At end of the reset cycle the timing and control circuit will signal the shutter to open via **extsync** pin or *FtSync* bit. At the end of the programmed integration time the shutter will be signalled to close, and the pixel read-out will commence as shown in figure 18a. At the end of the read-out sequence the *FTriggerEN* will be automatically disabled and the sensor will return to video capture mode as shown in figure 20.

If an external shutter is not available then at least two frames need to be taken so that the pixels can be integrated over one frame as shown in Figure 18b.

To use CPU snapshot mode the *SsEngage* bit of the SNAPSHOTMODE1 register must be set to one.

An interrupt generator can be enabled in CPU snapshot mode by setting the *SnapIntEn* bit of SNAPSHOTMODE1 register. An interrupt will be generated on the external interrupt pin, **irq**, when a snapshot sequence is triggered (TRIGGER=1) or when the array readout is complete at the end of the snapshot sequence as shown figure 21.

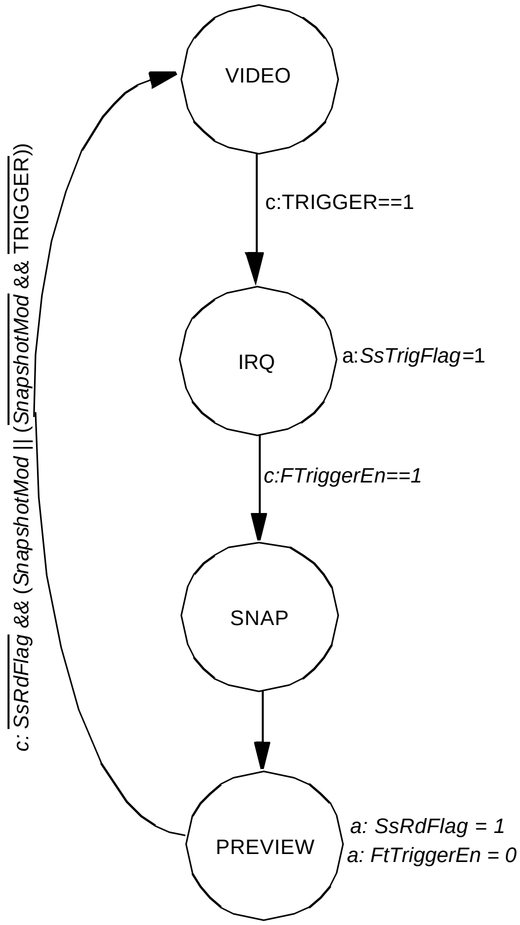


Figure 21. CPU Snapshot Mode State Diagram

When an interrupt is generated by a TRIGGER event, the *SsTrigFlag* bit in the SNAPSHOTMODE1 register is set. Similarly when an interrupt is generated at the completion of a readout the *SsRdFlag* in the SNAPSHOTMODE1 register is set.

The polarity of the **irq** pin can be programmed. The interrupt can only be cleared by reading *SsTrigFlag* and the *SsRdFlag* as shown in figure 22.

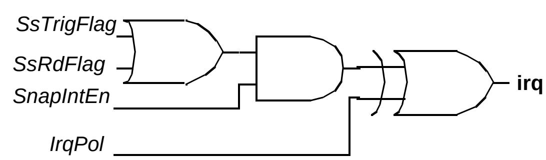


Figure 22. Interrupt Request Generation Logic

5.5 Pulse & Level Trigger Mode

The **snapshot** pin can be programmed to operate in *pulse trigger mode* where one snapshot sequence is executed per active pulse or in *level trigger mode* where by snapshot sequences are repeated as long as the level on the **snapshot** pin is held active. (see figures 20 and 21).

Pulse and level trigger modes can be set by programming the *SnapshotMod* bit in the SNAPSHOTMODE0 register.

Functional Description (continued)

6.0 CLOCK GENERATION MODULE

The LM9627 contains a clock generation module that will create two clocks as follows:

Hclk, the horizontal clock. This is an internal system clock and can be programmed to be the input clock *(mclk)* or *mclk* divided by any number between 1 and 255.

CLK_{pixel} the pixel clock. This is the external pixel clock that appears at the digital video port. It can be *Hclk* or *Hclk* divided by 2. This clock cannot be programed.

7.0 FRAME RATE PROGRAMING

A frame is defined as the time it takes to reset every pixel in the array, integrate the incident light, convert it to digital data and present it on the digital video port. This is not a concurrent process and is characterized in a series of events each needing a certain amount of time as shown in Figure 23.

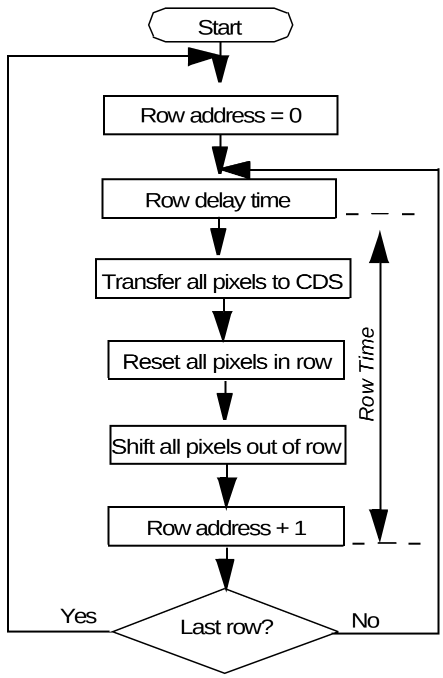


Figure 23. Frame Readout Flow Diagram

7.1 Full Frame Integration

Full frame integration is when each pixel in the array integrates light incident on it for the duration of a frame (see Figure 24).

The number of *Hclk* clock cycles required to process & shift out one row of pixels is given by:

$$RN_{Hclk} = R_{opcycle} + R_{delay}$$

Where:

$R_{opcycle}$ is a fixed integer value of 780 representing the *Row Operation Cycle Time* in multiples of *Hclk* clock cycles. It is the time required to carry out all fixed row operations outlined in Figure 23.

R_{delay} a programmable value between 0 & 2047 representing the *Row Delay Time* in multiples of *Hclk*. This parameter allows the *Row Operation Cycle* time to be extended. (See the Row Delay High and Row Delay Low registers).

The number of rows in a scan window is given by:

$$SWN_{rows} = (RAD_{end} - RAD_{start}) + 1$$

Where:

RAD_{end} is the end row address of the defined scan window. (See section 2.1)

RAD_{start} is the start row address of the defined scan window. (Scan section 2.1).

The number of *Hclk* clocks required to process a full frame is given by:

$$FN_{Hclk} = [(M_{factor} * SWN_{rows}) + F_{delay}] * RN_{Hclk}$$

Where:

M_{factor} is a Mode Factor which must be applied. It is dependent on the selected mode of operation as shown in the table below:

Progressive Scan	1
Sub-sampling or Interlace	0.5

SWN_{rows} is the *Number of Rows in Selected Scan Window.*

F_{delay} a programmable value between 0 & 4097 representing the *Inter Frame Delay* in multiples of RN_{Hclk}. This parameter allows the frame time to be extended. (See the Frame Delay High and Frame Delay Low registers).

The frame rate is given by:

$$Frame\ Rate = \frac{Hclk}{FN_{Hclk}}$$

7.2 Partial Frame Integration

In some cases it is desirable to reduce the time during which the pixels in the array are allowed to integrate incident light without changing the frame rate.

This is known as *Partial Fame Integration* and can be achieved by resetting pixels in a given row ahead of the row being selected for readout as shown in Figure 24. The number of *Hclk* clocks required to process a partial frame is given by:

$$FP_{Hclk} = RN_{Hclk} * I_{time}$$

Where:

RN_{Hclk} is the number of *Hclk* clock cycles required to process & shift out one row of pixels.

I_{time} is the number of rows ahead of the current row to be reset. (See the Integration Time High and Low registers).

The Integration time is subject to the following limits:

Mode	Limit
Progressive Scan	$I_{time} <= SWN_{rows} + F_{delay}$
Interlace	$I_{time} <= SWN_{rows} + 2 * F_{delay}$
Sub-Sampled	$I_{time} <= SWN_{rows} + 0.5 * F_{delay}$

Functional Description (continued)

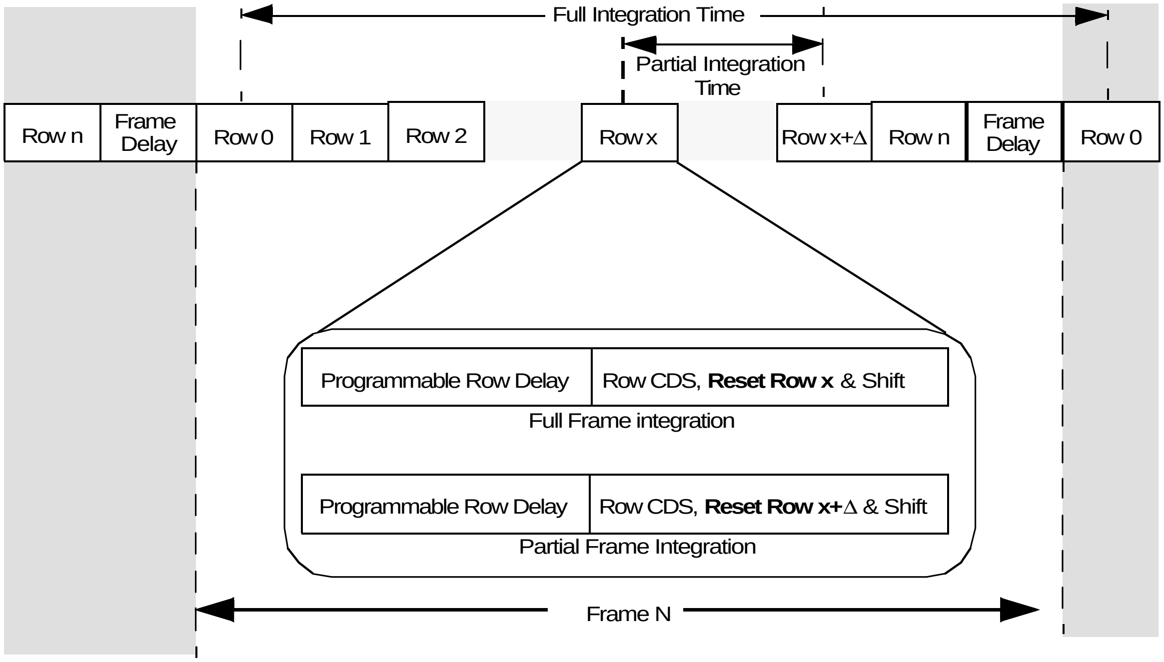


Figure 24. Partial and Full Frame Integration

7.3 Frame Rate Programming Guide

The table bellow can be used as a guide for programming the sensor. Note that it is assumed that the sensor is being driven with a 48MHz clock. All programmed values are given in decimal.

register	vclkgen	rdelayh	rdelayl	fdelayh	fdelayl	srows	srowe	dwlsb
address	05hex	15hex	16hex	17hex	18hex	0Bhex	0Chex	12hex
fps		[10:8]	[7:0]	[11:8]	[7:0]	[8:1]	[8:1]	
30	4	0	0	0	9	0	251	50
15	4	0	0	2	40	0	251	50
7.5	4	0	0	6	12	0	251	50
3.75	4	3	12	6	12	0	251	50
25	4	0	172	0	0	0	251	50
12.5	5	0	0	1	226	0	251	50
6.25	5	0	0	5	188	0	251	50
3.125	4	0	156	14	14	0	251	50
5	4	2	255	4	23	0	251	50
4	5	0	0	10	12	0	251	50
3	5	0	0	14	14	0	251	50
2	6	0	200	13	248	0	251	50
1	6	3	241	15	126	0	251	50

Functional Description (continued)

8.0 SIGNAL PROCESSING

8.1 Bad Pixel Detection & Correction

The LM9627 has a built-in bad pixel detection and correction block that operates on the fly. This block can be switched off by the user.

8.2 Black Level Compensation

In addition to the programmable gain the LM9627 has a built in black level compensation block as illustrated in Figure 25. This block can be switched off.

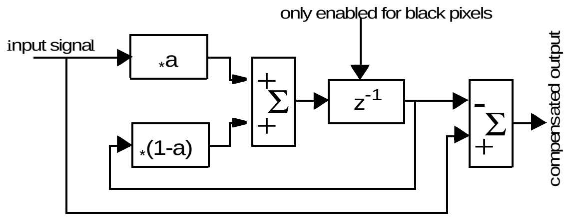


Figure 25. Digital Black Level Compensation.

The black level compensation block will subtract the average signal level of the black pixels around the array from the digital video output to compensate for the temperature and integration time dependent dark signal level of the pixels. The exponential averaging circuit shown in figure 25 only operates on the least significant 8 bits of the video data.

9.0 POWER MANAGMENT

9.1 Power Up and Down

The LM9627 is equipped with an on-board power management system allowing the analog and digital circuitry to be switched off (power down) and on (power up) at any time.
The sensor can be put into power down mode by asserting a logic one on the "*pdwn*" pin or by writing to the power down bit in the main configuration register via the I^2C compatible serial interface.

To power up the sensor a logic zero can be asserted on the "*pdwn*" pin or write to the power down bit in the main configuration register via the I^2C compatible serial interface.
It will take a few milli seconds for all the circuits to power up. The power management register contains a bit indicating when the sensor is ready for use. During this time the sensor cannot be used for capturing images. A status bit in the power management register will indicate when the sensor is ready for use.

9.2 Advanced Power Features

In addition to the power up/power down features of the sensor, sections of the analog video processing chain can be powered down and re-routed during normal operation. This flexibility allows power dissipation to be traded of with signal gain as shown in the table below:

PGA Amp	Power Saving
on	0mW
off	10mW

Figure 26. Power Control

10.0 ANALOG GAIN ADJUSTMENT

The integrated analog programmable gain amplifier is capable of applying a linear gain 1X to 5.6X in 64 linear steps. This can be programmed using the VGAIN register as shown in the table below:

VidGain Dec Code	VidGain Hex Code	Gain Amp Value	VidGain Dec Code	VidGain Hex Code	Gain Amp Value
0	00	1	32	20	3.34
1	01	1.07	33	21	3.41
2	02	1.15	34	22	3.48
3	03	1.22	35	23	3.56
4	04	1.29	36	24	3.63
5	05	1.37	37	25	3.7
6	06	1.44	38	26	3.77
7	07	1.51	39	27	3.85
8	08	1.58	40	28	3.92
9	09	1.66	41	29	3.99
10	0A	1.73	42	2A	4.07
11	0B	1.8	43	2B	4.14
12	0C	1.88	44	2C	4.21
13	0D	1.95	45	2D	4.29
14	0E	2.02	46	2E	4.36
15	0F	2.1	47	2F	4.43
16	10	2.17	48	30	4.5
17	11	2.24	49	31	4.58
18	12	2.31	50	32	4.65
19	13	2.39	51	33	4.72
20	14	2.46	52	34	4.8
21	15	2.53	53	35	4.87
22	16	2.61	54	36	4.94
23	17	2.68	55	37	5.02
24	18	2.75	56	38	5.09
25	19	2.83	57	39	5.16
26	1A	2.9	58	3A	5.23
27	1B	2.97	59	3B	5.31
28	1C	3.04	60	3C	5.38
29	1D	3.12	61	3D	5.45
30	1E	3.19	62	3E	5.53
31	1F	3.26	63	3F	5.6

Functional Description (continued)

11.0 OFFSET ADJUSTMENT

For maximum image quality over a wide range of light conditions it is necessary to set an appropriate offset voltage before using the sensor to capture images. This offset voltage must be applied to the offset pin (38) of the sensor, and is used to adjust the analogue video signal being fed to the internal A/D.

The level of the offset voltage determines the black level of the image and has a direct impact on the image quality. Too high an offset results in a white washed or hazy looking image, while too low of an offset results in a dark image with low contrast even though the light conditions are good.

A fine offset adjustment should be applied to each part by programming the offset voltage via the I^2C compatible serial interface. To program an offset voltage the following procedure should be followed:
The sensor's *offset, fine_i* & *fine_ctrl* pins should be connected as shown in figure 2.

The following procedure should be followed to calibrate the offset

- Disable the black level compensation block by writing a logic 1 to bit 4 of the **Main Configuration Register 0** (MCFG0: address 02Hex).
- The offset can be adjusted by writing to the **Offset Compensation Registers** (OCR: addresses 1F, 22 & 25 hex). Writing 00hex will give the largest voltage, while writing FF hex will give the smallest value.
- Run the following binary search algorithm
- For n=7 to 0 step -1
- {

    Set bit n in the OCR registers (addresses 1F, 22 & 25 Hex) to a logic one by writing over the I^2C compatible interface.
    Read a full frame and calculate the average black level ($BL_{average}$) of the first and last 5 black pixels in the every row of the array
    If ($BL_{average}$ < 100) then
        Reset bit n in the OCR registers (addresses 1F, 22 & 25 Hex) to 0
    else
        Keep bit n set to one.

  }
- Enable the black level compensation block (if desired) by writing a logic 0 to bit 4 of the **Main Configuration Register 0** (MCFG0: address 02Hex).

12.0 OFFSET & GAIN

The fine offset adjustment and calibration method described in section 11.0 will ensure that the sensor's black level is optimized for a fixed analog gain setting. However, when the analog gain is changed substantially, the black level of the sensor will shift resulting in a white washed image.
To stop this effect from occurring, the black level needs to be re-calibrated. This can be done as part of the contrast adjustment which is carried out by most digital image processors. If this is not possible then the following method can be used.
The relationship between the gain and the offset can be described with the following equation.

$$Offset(G) = Offset(0) + C * G^{0.4}$$

where:

Offset(G)	is the offset that needs to be programmed in the OCR1, OCR2 & OCR3 registers to ensure the correct black level setting for an analog gain setting of *G.*
Offset(0)	is the offset that needs to be programmed in the OCR1, OCR2 & OCR3 registers to ensure the correct black level setting for unity analog gain, (*G*=0).
C	is a constant and will vary from sensor to sensor
G	is the value programmed in the VGAIN register of the sensor which determines the sensor's analog gain.

The following procedure should be used to calculate the value of *C*:
Use the calibration procedure described in section 11.0 to determine the offset at unity gain, *offset(0)*. Note the VGAIN register should be set to 0.
Set the sensor's analog gain register (VGAIN) to its max setting, 31, and repeat the calibration procedure described in section 11.0. This will allow the offset at full gain, 31, that needs to be programmed in the OCR1, OCR2 & OCR3 registers to ensure the correct black level setting to be determined.
The value of C for a particular sensor can be calculated using the following formula:

$$C = \frac{Offset(31) - Offset(0)}{3.95}$$

Once the value of C has been calculated, offset values for different gain settings can be calculated using equation 1. It is recommended that a two decimal point accuracy for C is maintained.

Functional Description (continued)

13.0 SERIAL BUS

The serial bus interface consists of the *sda* (serial data), *sclk* (serial clock) and *sadr* (device address select) pins. The LM9627 can operate only as a slave.

The *sclk* pin is an input, it only and controls the serial interface, all other clock functions within LM9627 use the master clock pin, *mclk*.

13.1 Start/Stop Conditions

The serial bus will recognize a logic 1 to logic 0 transition on the *sda* pin while the *sclk* pin is at logic 1 as the ***start*** condition. A logic 0 to logic 1 transition on the *sda* pin while the *sclk* pin is at logic 1 is interrupted as the ***stop*** condition as shown in Figure 27.

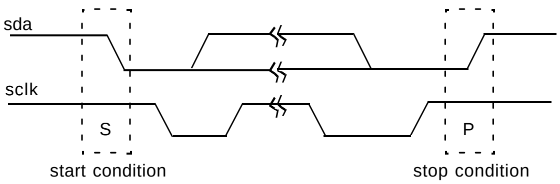


Figure 27. Start/Stop Conditions

13.2 Device Address

The serial bus *Device Address* of the LM9627 is set to 1010101 when *sadr* is tied low and 0110011 when *sadr* is tied high. The value for s*adr is* set at power up.

13.3 Acknowledgment

The LM9627 will hold the value of the *sda* pin to a logic 0 during the logic 1 state of the *Acknowledge* clock pulse on *sclk* as shown in Figure 28.

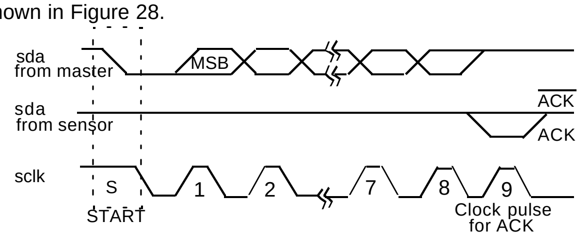


Figure 28. Acknowledge

13.4 Data Valid

The master must ensure that data is stable during the logic 1 state of the *sclk* pin. All transitions on the *sda* pin can only occur when the logic level on the sclk pin is "0" as shown in Figure 29.

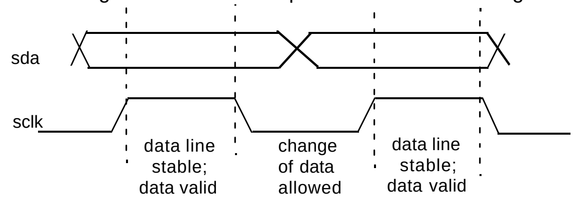


Figure 29. Data Validity

13.5 Byte Format

Every byte consists of 8 bits. Each byte transferred on the bus must be followed by an *Acknowledge*. The most significant bit of the byte is should always be transmitted first. See Figure 30.

13.6 Write Operation

A write operation is initiated by the master with a *Start Condition* followed by the sensor's *Device Address* and *Write* bit. When the master receives an *Acknowledge* from the sensor it can transmit 8 bit internal register address. The sensor will respond with a second *Acknowledge* signaling the master to transmit 8 write data bits. A third *Acknowledge* is issued by the sensor when the data has been successfully received.

The write operation is completed when the master asserts a *Stop Condition* or a second *Start Condition*. See Figure 31.

13.7 Read Operation

A read operation is initiated by the master with a *Start Condition* followed by the sensor's *Device Address* and *Write* bit. When the master receives an *Acknowledge* from the sensor it can transmit the internal *Register Address* byte. The sensor will respond with a second *Acknowledge*. The master must then issue a new *Start Condition* followed by the sensor's *Device Address* and *read* bit. The sensor will respond with an Acknowledged followed by the *Read Data* byte.
The read operation is completed when the master asserts a *Not Acknowledge* followed by *Stop Condition* or a second *Start Condition*. See Figure 32.

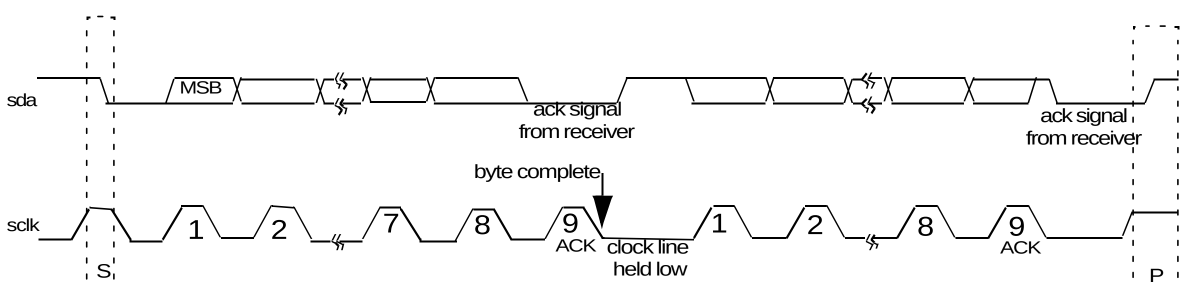


Figure 30. Serial Bus Byte Format

S	Device Address	$\overline{W}$	A	Register Address	A	Data Byte	A	P

bold **sensor action**

Figure 31. Serial Bus Write Operation

S	Device Address	$\overline{W}$	A	Register Address	A	S	Device Address	R	A	Data Byte	$\overline{A}$	P

bold **sensor action**

Figure 32. Serial Bus Read Operation

Functional Description (continued)

14.0 DIGITAL VIDEO PORT

The captured image is placed onto a flexible 12-bit digital port as shown in Figure 10. The digital video port consists of a programmable 12-bit digital Data Out Bus (*d[11:0]*) and three programmable synchronisation signals (*hsync, vsync, pclk*).

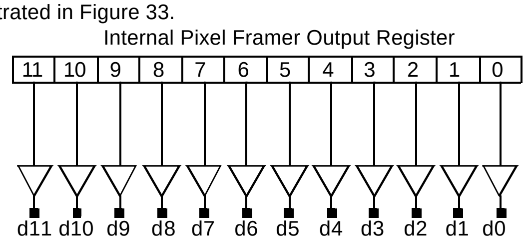
By default the synchronisation signals are configured to operate in "*master*" mode. They can be programed to operate in "*slave*" mode.

The following sections are a detailed description of the timing and programming modes of digital video port.

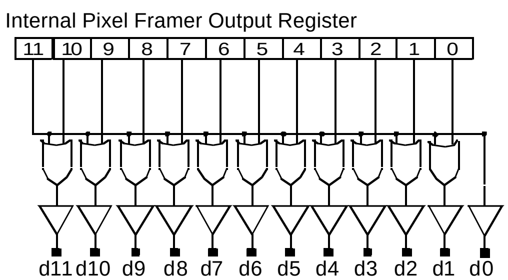
Pixel data is output on a 12-bit digital video bus. This bus can be tri-stated by asserting the *TriState* bit in the VIDEOMODE1 register.

14.1 Digital Video Data Out Bus (d[11:0])

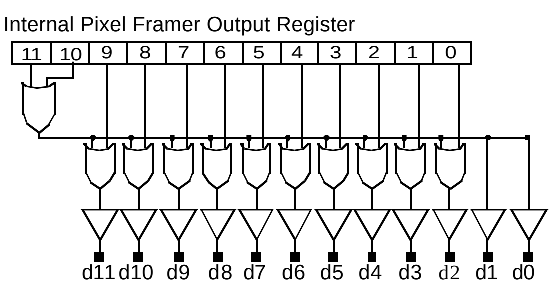
A programmable matrix switch is provided to map the output of the internal pixel framer to the pins of the digital video bus as illustrated in Figure 33.



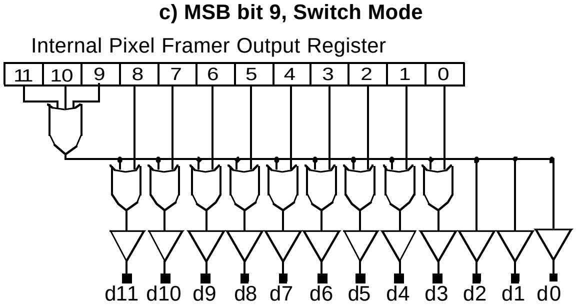
a) MSB Bit 11, Switch Mode (default)



b) MSB Bit 10, Switch Mode



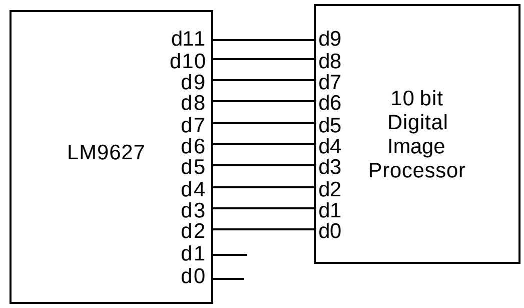
c) MSB bit 9, Switch Mode



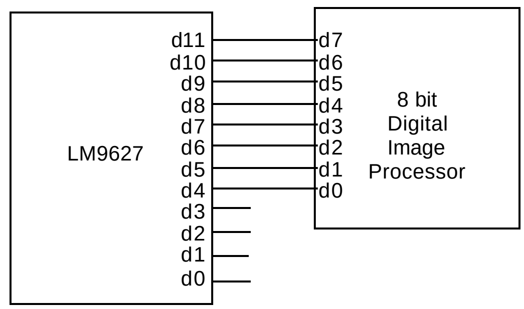
d) MSB bit 8, Switch Mode

Figure 33. Digital Video Bus Switching Modes

This feature allows a programmable digital gain to be implemented when connecting the sensor to 8 or 10 bit digital video processing systems as illustrated in Figure 34. The unused bits on the digital video bus can be optionally tri-stated.



a) LM9627 Connected to a 10 bit Digital Image Processors



b) LM9627 Connected to a 8 bit Digital Image Processors

Figure 34. Example of connection to 10/8 bit systems

Synchronisation Signals in Master Mode

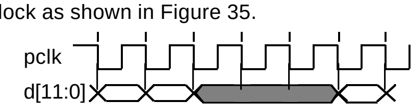
By default the sensor's digital video port's synchronisation signals are configured to operate in master mode. In master mode the integrated timing and control block controls the flow of data onto the 12-bit digital port, three synchronisation outputs are provided:

pclk	is the pixel clock output pin.
hsync	is the horizontal synchronisation output signal.
vsync	is the vertical synchronisation output signal.

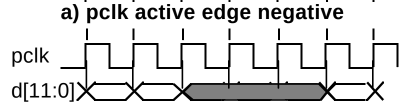
14.2 Pixel Clock Output Pin (pclk) (Master Mode)

The pixel clock output pin, *pclk,* is provided to act as a synchronisation reference for the pixel data appearing at the digital video out bus pins d[11:0]. This pin can be programmed to operate in two modes:

- In free running mode the pixel clock output pin, *pclk,* is always running with a fixed period. Pixel data appearing on the digital video bus *d[11:0]* are synchronized to a specified active edge of the clock as shown in Figure 35.



a) pclk active edge negative



b) pclk active edge positive (default)

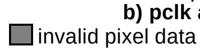


Figure 35. *pclk* in Free Running Mode

- In data ready mode, the pixel clock output pin (*pclk*) will produce a pulse with a specified level every time valid pixel data appears on the digital video bus *d[11:0]* as shown in Figure 36.

Functional Description (continued)

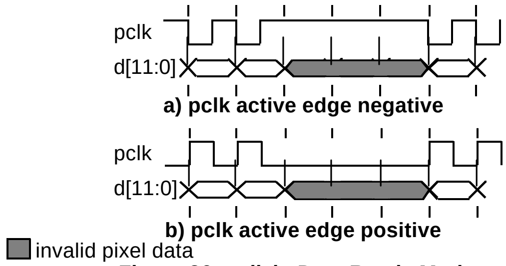


Figure 36. *pclk* in Data Ready Mode

By default the pixel clock is a free running active low (pixel data changes on the positive edge of the clock) with a period equal to the internal *hclk*. The active edge of the clock can be programmed such that pixel data changes on the positive or negative edge of the clock.

14.3 Horizontal Synchronisation Output Pin (hsync)

The horizontal synchronisation output pin, *hsync*, is used as an indicator for row data. The hsync output pin can be programmed to operate in two modes as follows:

- Level mode should be used when the pixel clock, *pclk,* is programmed to operate in *free running mode.* In level mode the *hsync* output pin will go to the specified level (high or low) at the start of each row and remain at that level until the last pixel of that row is read out on d[11:0] as shown in Figure 37. The *hsync* level is always synchronized to the active edge of *pclk.*

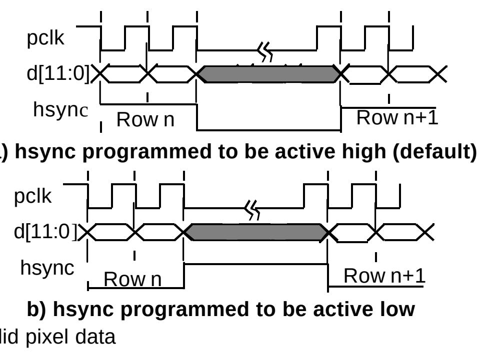


Figure 37. *hsync* in Level Mode

- Pulse mode should be used when the pixel clock, *pclk,* is programmed to operate in *data ready mode.* In pulse mode the *hsync* output pin will produce a pulse at the end of each row. The width of the pulse will be a minimum of four *pclk* cycles and its polarity can be programmed as shown in Figure 38. The *hsync* level is always synchronized to the active edge of *pclk*

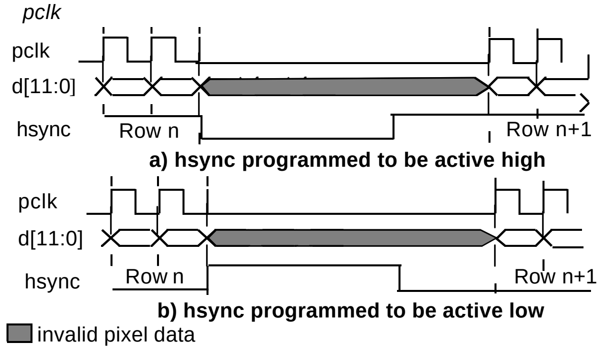


Figure 38. *hsync* in Pulse Mode

By default the first pixel data at the beginning of each row is placed on the digital video bus as soon as *hsync* is activated. It is possible to program up to 15 dummy pixels to be readout at the beginning of each row before the real pixel data is readout. This feature is supported for both *level* and *pulse* mode.

14.4 Vertical/Horizontal Synchronisation Pin (vsync)

The vertical synchronisation output pin, *vsync,* is used as an indicator for pixel data within a frame. The *vsync* output pin can be programmed to operate in two modes as follows:

- Level mode should be used when the pixel clock, *pclk,* is programmed to operate in *free running mode.* In level mode the *vsync* output pin will go to the specified level (high or low) at the start of each frame and remain at that level until the last pixel of that row in the frame is placed on d[11:0] as shown in Figure 39. The *hsync* level is always synchronized to the active edge of *pclk*.

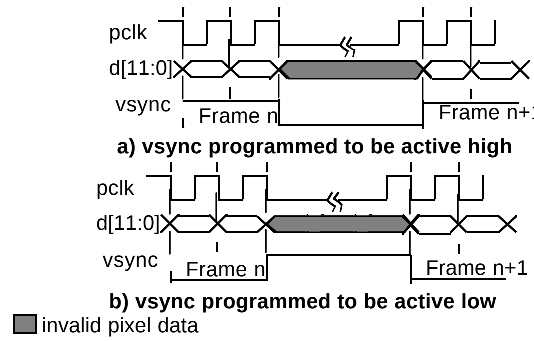


Figure 39. vsync in Level Mode

- Pulse mode should be used when the pixel clock, *pclk,* is programmed to operate in *data ready mode.* In pulse mode the *vsync* output pin will produce a pulse at the end of each frame. The width of the pulse will be a minimum of four *hclk* cycles and its polarity can be programmed as shown in Figure 40. The *vsync* level is always synchronized to the active edge of *pclk*.

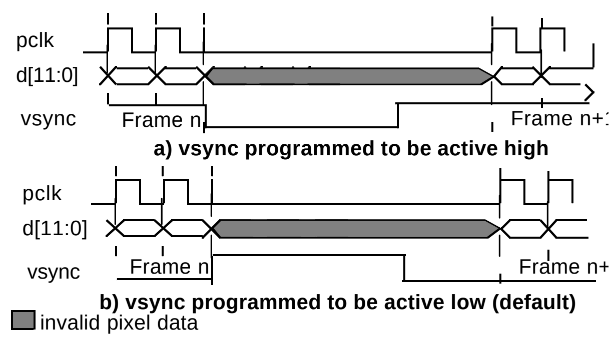


Figure 40. vsync in pulse mode

14.5 Odd/Even Mode

In odd/even mode the *vsync* signal is used to indicate when pixel data from an odd and even field is being placed on the digital video bus *d[11:0]*. The polarity of *vsync* can still be programmed in this mode as shown in Figure 41

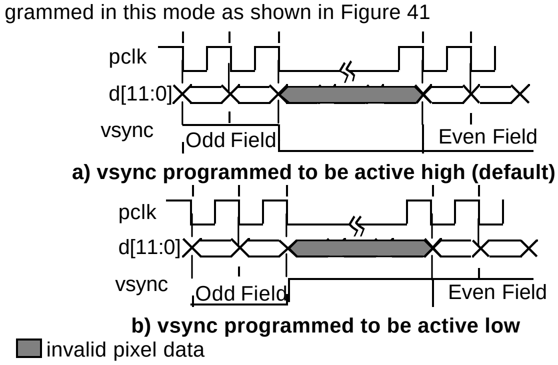


Figure 41. *vsync* in odd/even Mode

Functional Description (continued)

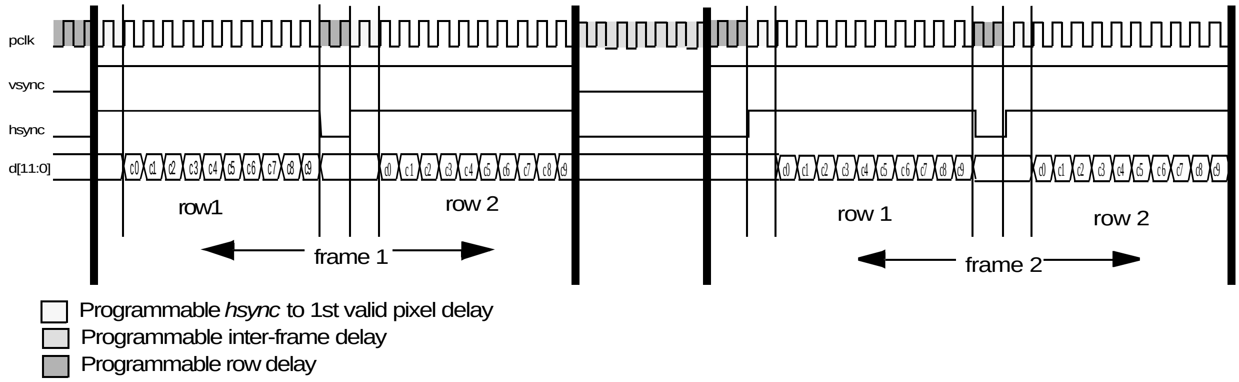


Figure 42. Example of Digital Video Port Timing in Progressive Scan Mode

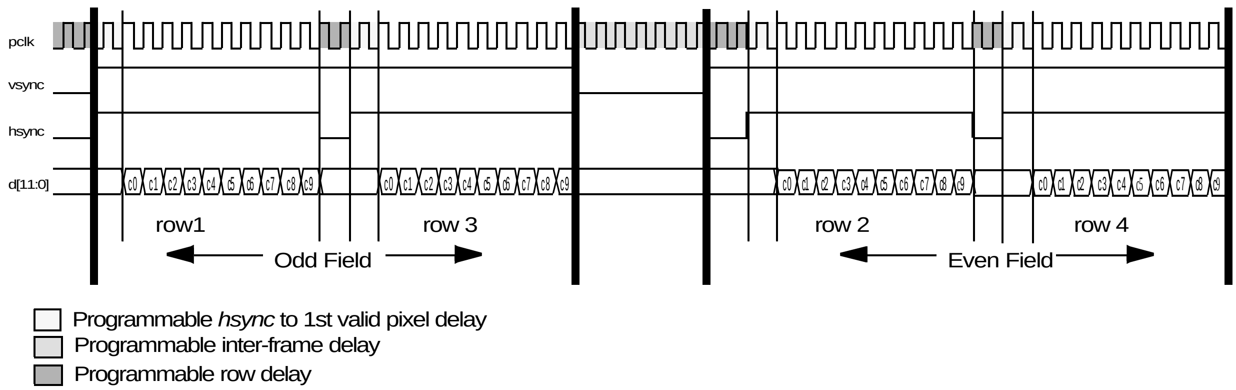


Figure 43. Example of Digital Video Port Timing in Interlaced Mode

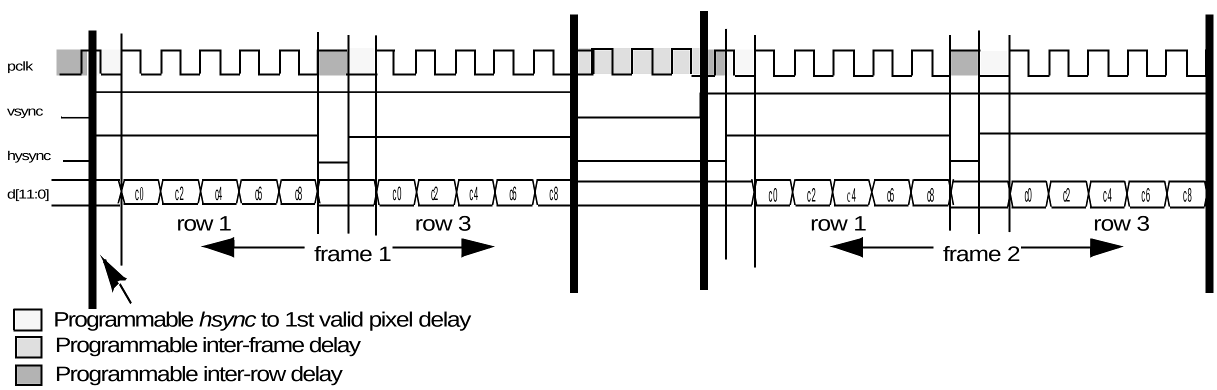


Figure 44. Example of Digital Video Port Timing in 2:1 Sub-sampling Mode

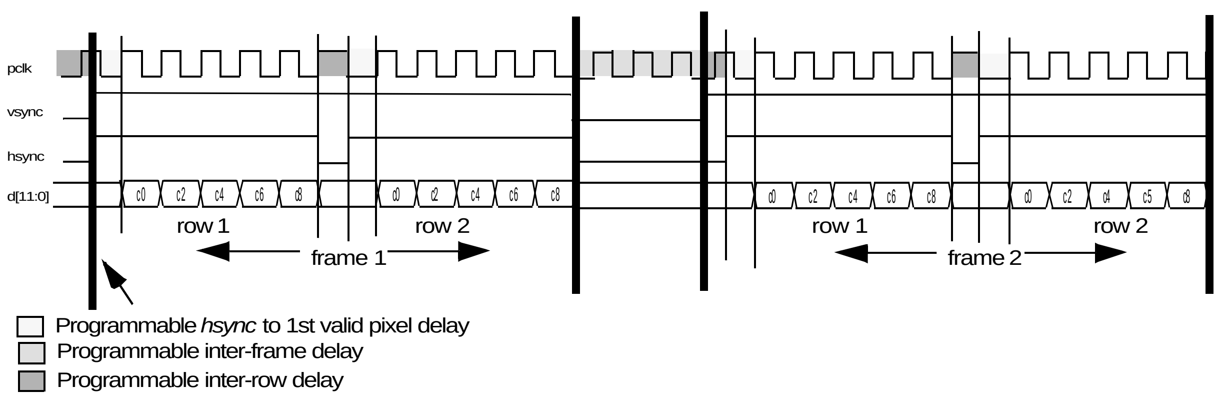


Figure 45. Example of Digital Video Port Timing in 4:2 Sub-sampling Mode

Functional Description (continued)

14.6 Synchronisation Signals in Slave Mode

The sensor's digital video port's synchronisation signals can be programmed to operate in slave mode. In slave mode the integrated timing and control block will only start frame and row processing upon the receipt of triggers from an external source.

Only two synchronization signals are used in slave mode as follows:

hsync is the row trigger input signal.
vsync is the frame trigger input signal.

Figure 46 shows the LM9627's digital video port in slave mode connected to a digital video processor master DVP.

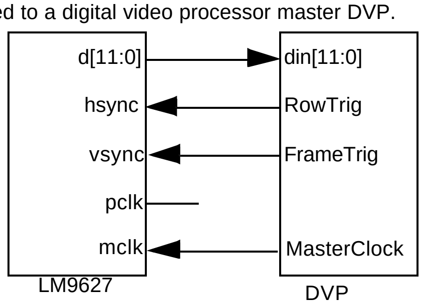


Figure 46. LM9627 in slave mode

14.7 Row Trigger Input Pin (hsync)

The row trigger input pin, *hsync*, is used to trigger the processing of a given row. It must be activated for at least two "*mclk*" cycle. The first pixel data will appear at *d[11:0]* "X_{mclk}"periods after the assertion of the row trigger, were X_{mclk} is given by:

$$X_{mclk} = 124 + DW_{StAd}$$

Where:

DW_{StAd} is the value of the display window column start address.

The polarity of the active level of the row trigger is programmable. By default it is active high.

14.8 Frame Trigger Input Pin (vsync)

The frame trigger input pin, *vsync*, is used to reset the row address counter and prepare the array for row processing. It must be activated for at least one "*mclk*" cycle and no more than 96 mclk cycles after the activation of *hsync* as illustrated in Figure 48.

The polarity of the active level of the row trigger is programmable. By default it is active high.

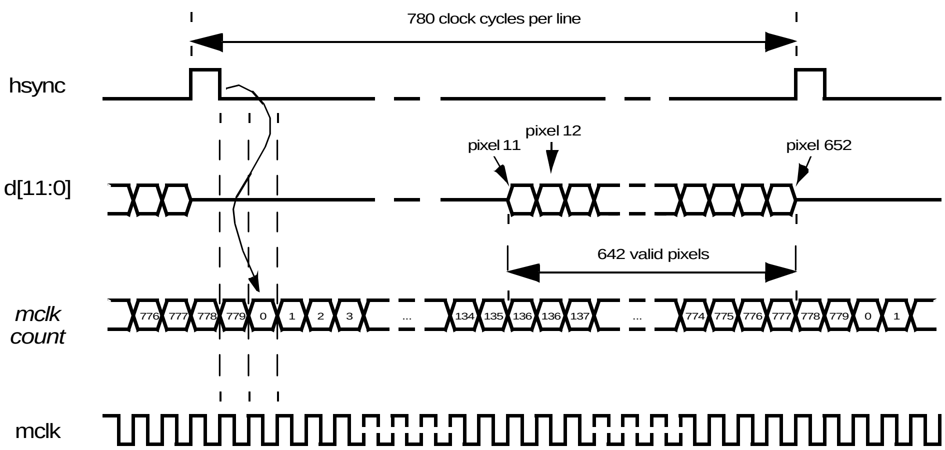


Figure 47. hsync slave mode timing diagram for centred display window of 642 pixels

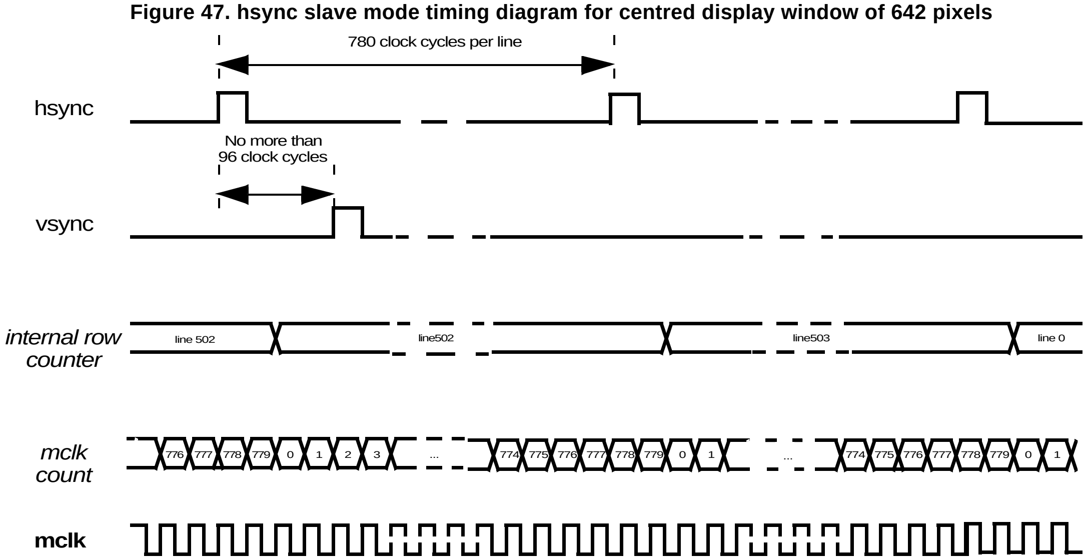


Figure 48. vsync slave mode timing diagram for scan window of 504 rows.

MEMORY MAP

ADDR	Register	Reset Value	Description
00h			Reserved for future use.
01h	REV	02h	Revision Register
02h	MCFG0	00h	Main Configuration Register 0
03h	MCFG1	00h	Main Configuration Register 1
04h	PCR	00h	Power Control Register.
05h	VCLKGEN	04h	Video Clock Generator
06h	VMODE0	00h	Video Mode 0 Register
07h	VMODE1	00h	Video Mode 1 Register
08h	VMODE2	00h	Video Mode 2 Register
09h	SNAPMODE0	00h	Snapshot Mode 0 Register
0Ah	SNAPMODE1	00h	Snapshot Mode 1 Register
0Bh	SROWS	00h	Scan Window Row Start Register
0Ch	SROWE	FBh	Scan Window Row End Register
0Dh			Reserved for future use.
0Eh	DROWS	00h	Display Window Row Start Register
0Fh	DROWE	FBh	Display Window Row End Register
10h	DCOLS	00h	Display Window Column Start Register
11h	DCOLE	A5h	Display Window Column End Register
12h	DWLSB	32h	Display Window LSB Register.
13h	ITIMEH	00h	Integration Time High Register
14h	ITIMEL	00h	Integration Time Low Register
15h	RDELAYH	00h	Row Delay High Register
16h	RDELAYL	00h	Row Delay Low Register
17h	FDELAYH	00h	Frame Delay High Register
18h	FDELAYL	00h	Frame Delay Low Register
19h	VGAIN	00h	Video Gain Register
1Fh	OCR1	00h	Offset Compensation Register 1
22h	OCR1	00h	Offset Compensation Register 1
25h	OCR2	00h	Offset Compensation Register 2
26h	BLCOEFF	00h	Black Level Compensation Coefficient Register
27h	BPTH0H	00h	Bad pixel Threshold 0 High Register
28h	BPTH0L	00h	Bad pixel Threshold 0 Low Register
29h	BPTH1H	00h	Bad pixel Threshold 1 High Register
2Ah	BPTH1L	00h	Bad pixel Threshold 1 Low Register

Register Set

The following section describes all available registers in the LM9627 register bank and their function.

Register Name **Device Rev Register**
Mnemonic **REV**
Address **01 Hex**
Type **Read Only.**

Bit	Bit Symbol	Description
7:0	SiRev	The silicon revision register.

Register Name **Main Configuration 0**
Address **02 Hex**
Mnemonic **MCFG0**
Type: **Read/Write**
Reset Value **00 Hex**

Bit	Bit Symbol	Description
7	PwrUpBusy	**(Read Only Bit)** Indicates that power on initialization is in progress. The sensor is ready for use when this bit is at logic 0.
6	PwrDown	Assert to power down the sensor. Writing a logic 1 to this register bit has the same effect as taking the *pdwn* pin high. Clear (the default) this bit to power up the sensor.
5	BPCorrection	Assert to enable the bad pixel detection and correction circuit. Clear (the default) to switch it off.
4	$\overline{\text{BlkLComp}}$	Assert to disable the black level compensation circuit. Clear (the default) to switch it on.
3	SnapEnable	Assert to enable the external *snapshot* pin. Clear (the default) to disable the external *snapshot* pin.
2:0		Reserved

Register Name **Main Configuration 1**
Address **03 Hex**
Mnemonic **MCFG1**
Type **Read/Write**
Reset Value **00 Hex**

Bit	Bit Symbol	Description
7	$\overline{\text{ColorMode}}$	Assert when using a monochrome sensor. When this bit is at a logic 1, Sub-Sampling is set to 2:1 and every other row is read out during interlace mode. Clear (the default) when using a color sensor. When this bit is at logic 0, sub-sampling is set to 4:2 and every other row pair is read out during interlace mode.
6	ScanMode	Assert to set the sensor to interlace readout mode. Clear (the default) to set the sensor to progressive scan read out mode.
5	HSubSamEn	Assert to enable horizontal sub-sampling. Clear (the default) to disable horizontal sub-sampling.
4	VSubSamEn	Assert to enable vertical sub-sampling. Clear (the default) to disable vertical sub-sampling.
3		Reserved
2	SlaveMode	Use to configure the digital video port's synchronisation signal to operate in slave mode. By default the digital video's port's synchronization signals are configured to operate in master mode.
1:0		Reserved

Register Name **Power Control Register 1**
Address **04 Hex**
Mnemonic **PCR**
Type **Read/Write**
Reset Value **00 Hex**

Bit	Bit Symbol	Description
7	ByPassGain	Assert to route the analog video signal from the output of the CDS to the input of the 12 bit A/D. Clear (the default) to route the signal to the video gain amplifier.
6:4		Reserved
3	PwdnPGA	Assert to power down the programmable video gain amplifier. Clear (the default) to power up the video gain amplifiers.
2:1		Reserved
0	PwDnADC	Assert to power down the 12 bit analog to digital convertor. Clear (the default) to power up the 12 bit analog to digital convertor.

Register Set (continued)

Register Name Hclk Generator Register
Address 05 Hex
Mnemonic VCLKGEN
Type Read/Write
Reset Value 04 Hex.

Bit	Bit Symbol	Description
7:0	HclkGen	Use to divide the frequency of the sensors master clock input, *mclk* to generate the internal sensor clock, *Hclk.* Program 00 Hex (the default) for *Hclk* to equal *mclk* or divide *mclk* by any number between 1 and FF Hex.

Register Name Digital Video Mode 0
Address 06 Hex
Mnemonic VMODE0
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:6	PixDataSel	Use to program the number of active bits on the digital video bus *d[11:0]*, starting from the MSB (*d[11]*). Inactive bits are tri-stated.: 00 – 12 bit mode, bits *d[11:0]* of the digital video bus are active. This is the default. 01 – 10 bit mode, bits *d[11:2]* of the digital video bus are active. 10 – 8 bit mode, bits *d[11:4]* of the digital video bus are active. 11 – Reserved.
5:4	PixDataMsb	Use to program the routing of the MSB output of the internal video A/D to a bit on the digital video bus. 00 – A/D [11:0] -> d[11:0]. 01 – A/D [10:0] -> d[11:1] 10 – A/D [9:0] -> d[11:2] 11 – A/D [8:0] -> d[11:3]
3:0		Reserved

Register Name Digital Video Mode 1
Address 07 Hex
Mnemonic VMODE1
Type Read/Write
Reset Value 00 Hext

Bit	Bit Symbol	Description
7	PixClkMode	Assert to set the *pclk* to “data ready mode”. Clear, the default, to set *pclk* to “*free running mode*”.
6	VsyncMode	Assert to set the *vsync* pin to “pulse mode”. Clear (the default) to set the *vsync* signal to “level mode”.
5	HsyncMode	Assert to force the *hsync* signal to pulse for a minimum of four pixel clocks at the end of each row. Clear (the default) to force the *hsync* signal to a level indicating valid data within a row.
4	PixClkPol	Assert to set the active edge of the pixel clock to negative. Clear (the default) to set the active edge of the clock to positive.
3	VsynPol	Assert to force the *vsync* signal to generate a logic 0 during a frame readout *(Level Mode),* or a negative pulse at the end of a frame readout *(Pulse Mode)*. Clear (the default) to force the *vsync* signal to generate a logic 1 during a frame readout *(Level Mode),* or a negative pulse at the end of a frame readout *(Pulse Mode)*.
2	HsynPol	Assert to force the *hsync* signal to generate a logic 0 during a row readout *(Level Mode),* or a negative pulse at the end of a row readout *(Pulse Mode)*. Clear (the default) to force the *hsync* signal to generate a logic 1 during a row readout *(Level Mode),* or a negative pulse at the end of a readout *(Pulse Mode)*.
1	OddEvenEn	Assert to force the *vsync* pin to act as an odd/even field indicator. Clear (the default) to force the *vsync* pin to act as a vertical synchronization signal.
0	TriState	Assert to tri-state all output signals (data and control) on the digital video port. Clear (default) to enable all signals (data and control) on the digital video port.

Register Name Digital Video Mode 2
Address 08 Hex
Mnemonic VMODE2
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:4	HsyncAdjust	Use to program the leading edge of *hsync* to the first valid pixel at the beginning of each row. This can be 0-hex to F-hex corresponding to 0 - 15 pixel clocks. Default 0.
3:0		Reserved

Register Set (continued)

Register Name **Snapshot Mode Configuration Register 0**
Address **09 Hex**
Mnemonic **SNAPMODE0**
Type **Read/Write**
Reset Value **00 Hex**

Bit	Bit Symbol	Description
7.6	SsFrames	Program to set the number of frames required before readout during a snapshot with no external shutter, (see Figure 18). By default these two bits are set to 00 resulting in one frame before readout: 0 – one frame 01 – two frames 10 – three frames 11 – four frames
5	ShutterEn	Assert to indicate that an external shutter will be used during snapshot mode. Clear (the default) to indicate that snapshot mode will be carried out without the aid of an external shutter.
4	ExtSynPol	Assert to set the active level of the *extsync* signal to 0. Clear (the default) to set the active level of the *extsync* signal to 1.
3		Reserved
2	SnapshotMod	Assert to set the *snapshot* pin to level mode. In level mode the sensor will continually run snapshot sequences as long as the *snapshot* pin is held to the active level. Clear (the default) to set the *snapshot* signal to pulse mode. In pulse mode the sensor will only carry out one snapshot sequence per pulse applied to the *snapshot* pin.
1	SnapShotPol	Assert to set the snapshot pin to be active on the positive edge. Clear (the default) to set the snapshot pin to be active on the negative edge.
0	IrqPol	Assert to set the active level of the *irq* signal to 0, Clear (the default) to set the active level of the *irq* signal to 1.

Register Name **Snapshot Mode Configuration Register 1**
Address **0A Hex**
Mnemonic **SNAPMODE1**
Type **Read/Write**
Reset Value **00 Hex.**

Bit	Bit Symbol	Description
7	SnapIntEn	Assert to enable the snapshot interrupt generator. Clear (the default) to disable the interrupt generator.
6	SsTrigFlag	**(Read Only Bit)** Snapshot trigger interrupt flag. A logic 1 in this bit indicates that the generated interrupt on the *irq* pin is due to a snapshot trigger. This bit is cleared when read.
5	SsRdFlag	**(Read Only Bit)** Snapshot read done interrupt flag. A logic 1 in this bit indicates that the generated interrupt on the *irq* pin is due to the completion of a snapshot readout sequence. This bit is cleared when read.
4	$\overline{\text{SsEngage}}$	Assert to allow a CPU controlled snapshot sequence. In this mode the snapshot trigger will only generate an interrupt to the CPU and the CPU must manually start the snapshot sequence by asserting the *FTriggerEn* bit of this register. Clear (the default) engage an automatic snapshot sequence. In auto mode the snapshot sequence is started as soon as a snapshot trigger is asserted.
3	FtSync	**(Read Only Bit)** The internal synchronisation signal. A logic 1 on this bit indicates a synchronization event is required. This bit is functionally equivalent to the external *extsync* pin.
2	FtBusy	**(Read Only Bit)** The Frame Trigger Busy bit. A logic 1 on this bit indicates that the sensor is busy reading out pixel data as shown in Figure 18.
1	FTriggerNow	Assert to start a snapshot sequence. The frame trigger now is functionally equivalent to the external *snapshot* pin. The default is 0.
0	FTriggerEn	Assert to enable a snapshot sequence (see the *SsEngage* bit of this register). The default is 0.

Register Set (continued)

Register Name Scan Window Row Start Register
Address 0B Hex
Mnemonic SROWS
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:0	SwStartRow	Use to program the scan window's start row address MSBs. If bit 6 of register DWLSB is set to 1 the start row address is incremented by 1 else the raw value is used.

Register Name Scan Window Row End Register
Address 0C Hex
Mnemonic SROWE
Type Read/Write
Reset Value FB Hex

Bit	Bit Symbol	Description
7:0	SwEndRow	Use to program the scan window's end row address MSBs. If bit 6 of register DWLSB is set to 1 the end row address is incremented by 1. else the raw value is used.

Register Name Display Window Row Start Register
Address 0E Hex
Mnemonic DROWS
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:0	DwStartRow	Use to program the display window's start row address MSBs. The LSB can be programmed using the DWLSB register.

Register Name Display Row End Register
Address 0F Hex
Mnemonic DROWE
Type Read/Write
Reset Value FB Hex

Bit	Bit Symbol	Description
7:0	DwEndRow	Use to program the scan window's end row address. The LSB can be programmed using the DWLSB register.

Register Name Display Window Column Start Register
Address 10 Hex
Mnemonic DCOLS
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:0	DwStartCol	Use to program the display window's start column address MSBs. The two LSBs can be programmed using the DWLSB register.

Register Name Display Window Column End Register
Address 11 Hex
Mnemonic DCOLE
Type Read/Write
Reset Value A5 Hex

Bit	Bit Symbol	Description
7:0	DwEndCol	Use to program the scan window's end column address MSBs. The two LSBs can be programmed using the DWLSB register.

Register Name Display Window LSB register
Address 12 Hex
Mnemonic DWLSB
Type Read/Write
Reset Value 32 Hex

Bit	Bit Symbol	Description
7		Reserved
6	SwLsb	Assert to increment the value of the scan window start and end row addresses by 1. Clear (the default) to use the raw values.
5	DwCel[1]	Use to program bit 1 of the display window's end column address. Default is 1.
4	DwCel[0]	Use to program bit 0 of the display window's end column address. Default is 1.
3	DwCSL[1]	Use to program bit 1 of the display window's start column address. Default is 0.
2	DwCSL [0]	Use to program bit 0 of the display window's start column address. Default is 0.
1	DwERLsb	Use to program bit 0 of the display window's end row address. Default is 1.
0	DwSRLsb	Use to program bit 0 of the display window's start row address. Default is 0.

Register Set (continued)

Register Name Integration Time High Register
Address 13 Hex
Mnemonic ITIMEH
Type Read/Write
Reset Value 00 Hex.

Bit	Bit Symbol	Description
7:4		Reserved
3:0	Itime[11:8]	Program to set the integration time of the array. The value programmed in the register is the number of rows ahead of the selected row to be reset.

Register Name Integration Time Low Register
Address 14 Hex
Mnemonic ITIMEL
Type Read/Write
Reset Value 00 Hex.

Bit	Bit Symbol	Description
7:0	Itime[7:0]	Program to set the integration time of the array. The value programmed in the register is the number of rows ahead of the selected row to be reset.

Register Name Row Delay High Register
Address 15 Hex
Mnemonic RDELAYH
Type Read/Write
Reset Value 00 Hex.

Bit	Bit Symbol	Description
7:3		Reserved
2:0	Rdelay[10:8]	Use to program the MSBs of the row delay.

Register Name Row Delay Low Register
Address 16 Hex
Mnemonic RDELAYL
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:0	Rdelay[7:0]	Use to program the LSBs of the row delay.

Register Name Frame Delay High Register
Address 17
Mnemonic FDELAYH
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:4		Reserved
3:0	FDelay[11:8]	Use to program the MSBs of the frame delay.

Register Name Frame Delay Low Register
Address 18 Hex
Mnemonic FDELAYL
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:0	FDelay [7:0]	Use to program the LSBs of the frame delay.

Register Name Video Gain Register
Address 19 Hex
Mnemonic VGAIN
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:6		Reserved
5:0	VidGain	Use to program the overall video gain. 00hex corresponds to a gain of 0dB while 3Fhex corresponds to a gain of 15dB. Steps are in linear increments.

Register Name Offset Compensation Register 0
address 1FHex
Mnemonic OCR0
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:0	OffsetVol	This register defines the voltage level appearing on the *offset_ctrl* pin.

Register Name Offset Compensation Register 1
address 22 Hex
Mnemonic OCR1
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:0	OffsetVol	This register defines the voltage level appearing on the *offset_ctrl* pin.

Register Name Offset Compensation Register 2
address 25 Hex
Mnemonic OCR2
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:0	OffsetVol	This register defines the voltage level appearing on the *offset_ctrl* pin.

Register Set (continued)

Register Name **Black Level Compensation Coefficient Register**
Address **26 Hex**
Mnemonic **BLCOEFF**
Type **Read/Write**
Reset Value **00 Hex**

Bit	Bit Symbol	Description
7:0	Alpha[7:0]	Exponential averaging coefficient for black pixels

Register Name **Threshold 0 High Register**
Address **27 Hex**
Mnemonic **BPTH0H**
Type **Read/Write**
Reset Value **00 Hex.**

Bit	Bit Symbol	Description
7:0	BpT0 [11:4]	Use to program the MSBs of the bad pixel correction threshold 0.

Register Name **Threshold 0 Low Register**
Address **28 Hex**
Mnemonic **BPTH0L**
Type **Read/Write**
Reset Value **00 Hex**

Bit	Bit Symbol	Description
7:4	BpT0 [3.0]	Use to program the LSBs of the bad pixel correction threshold 0.
3:0		Reserved

Register Name **Threshold 1 High Register**
Address **29 Hex**
Mnemonic **BPTH1H**
Type **Read/Write**
Reset Value **00 Hex**

Bit	Bit Symbol	Description
7:0	THR1[11.4]	Use to program the MSBs of the bad pixel correction threshold 1.

Register Name **Threshold 1 Low Register**
Address **2A Hex**
Mnemonic **BPTH1L**
Type **Read/Write**
Reset Value **00 Hex**

Bit	Bit Symbol	Description
7:4	THR1 [3.0]	Use to program the LSBs of the bad pixel correction threshold 1.
3:0		Reserved

Timing Information

1.0 DIGITAL VIDEO PORT MASTER MODE TIMING

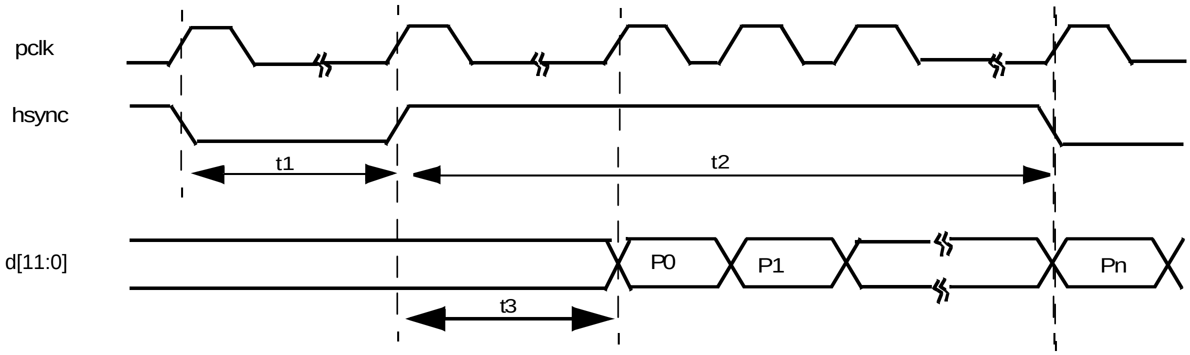


Figure 49. Row Timing Diagram

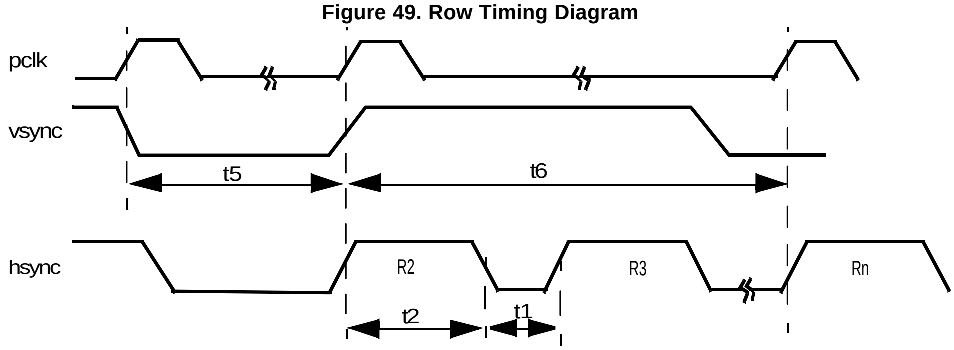


Figure 50. Frame Timing

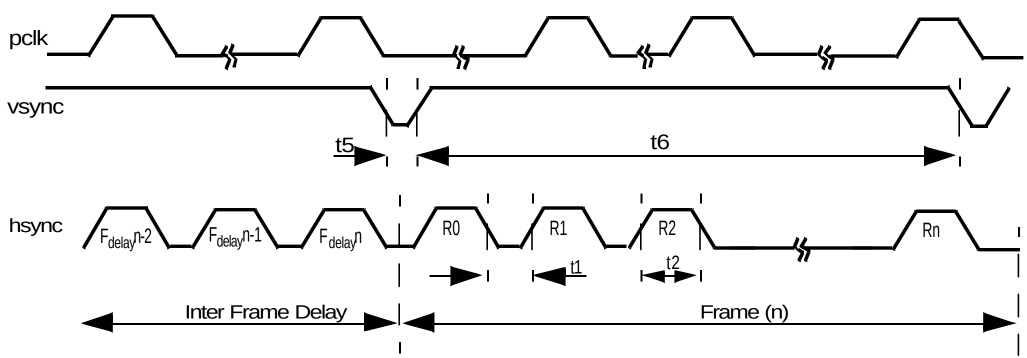


Figure 51. Frame Delay Timing (With Inter Frame Delay).

Label	**Descriptions**	**Min**	**Typ**	**Max**
t0	pclk period	74.4ns	83.3ns	1.0µs

t1	hsync low	level mode pulse mode	(116-*HsyncAdjust*) * pclk 16 * *pclk*	(see note a & b)
t2	hsync high	level mode pulse mode	(664 -*HsyncAdjust*) * *pclk* 764 * *pclk*	(see note a & b)
t3	first valid pixel data after *hsync* active		*HsyncAdjust* * *pclk*	(see note a & b)
t5	vsync low	level mode pulse mode	116 * *pclk* 16 * *pclk*	(see note a & b)
t6	vsync high	level mode pulse mode	(*FN*$_{Hclk}$ - 116) * *pclk* 16 * *pclk*	(see note a & b)

Note a: See *Frame Rate Programming* section for more details
Note b: See *Digital Video Port Registers* for more details

Timing Information (continued)

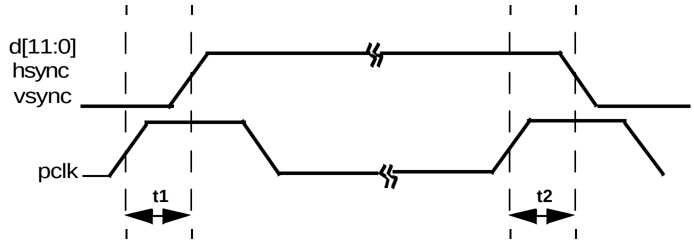


Figure 52. *d[11:0]*, *hsync* & *vsync* to Active High *pclk* Timing

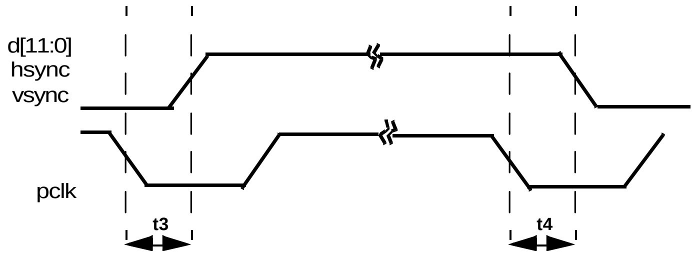


Figure 53. *d[11:0]*, *hsync* & *vsync* to Active Low *pclk* Timing

The following specifications apply for all supply pins = +3.3V and C_L = 10pF unless otherwise noted. **Boldface limits apply for TA = T_{MIN} to T_{MAX}:** all other limits $T_A = 25^oC$ (Note 7)

Label	Descriptions	Min	Typ	Max
t1	Rising *pclk* to Rising *hsync, vsync* or *d[11:0]*		25ns	
t2	Rising *pclk* to Falling *hsync, vsync* or *d[11:0]*		23ns	
t3	Falling *pclk* to rising *hsync, vsync* or *d[11:0]*		25ns	
t4	Falling *pclk* to falling *hsync, vsync* or *d[11:0]*		23ns	

Timing Information (continued)

2.0 DIGITAL VIDEO PORT SLAVE MODE TIMING

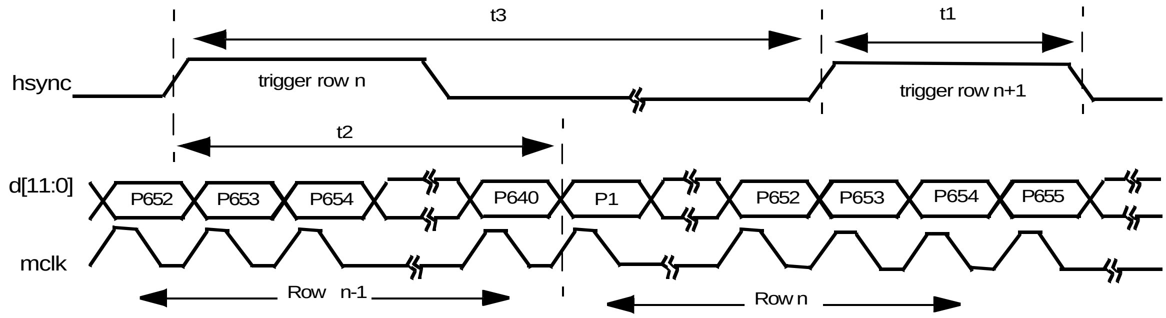


Figure 54. Slave Mode Row Trigger and Readout Timing

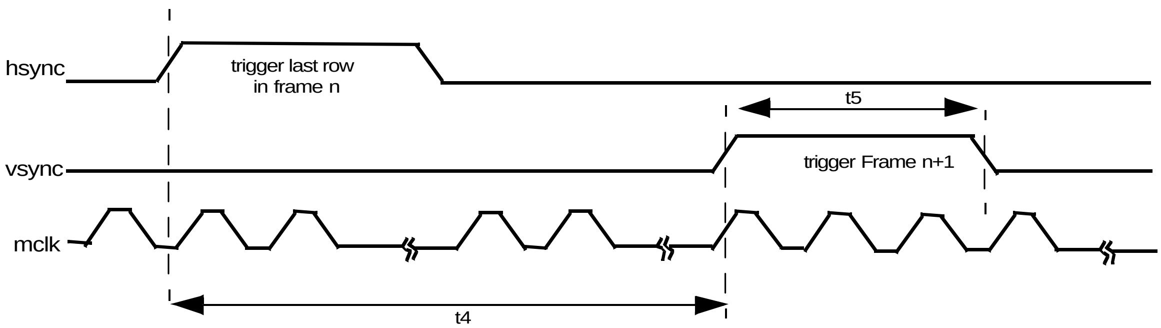


Figure 55. Slave Mode *d[11:0]*, *hsync* & *vsync* to *pclk* Timing

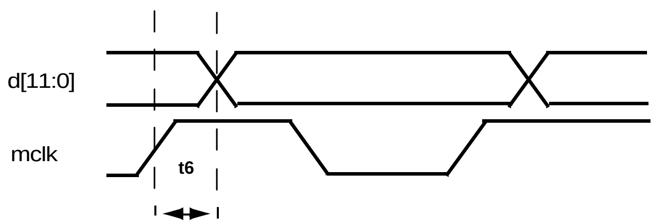


Figure 56. Rising Edge of *mclk* to Valid Pixel Data

The following specifications apply for all supply pins = +3.0V & C_L = 10pF unless otherwise noted. **Boldface limits apply for TA = T_{MIN} to T_{MAX}**: all other limits T_A = 25^{o}C (Note 7)

Label	Descriptions	Min	Typ	Max
t1	Pulse width of row trigger	2 * mclk		
t2	First pixel out after rising edge of row trigger	124 * mclk		124 * mclk
t3	Minimum time between row triggers.	780 * mclk		
t4	Max time to assert next frame trigger after last row trigger.			96 * mclk
t5	Pulse width of Frame trigger	2 * mclk		
t6	Time to valid pixel data after rising edge of mclk		44ns	

Timing Information (continued)

3.0 DIGITAL VIDEO PORT SINGLE FRAME CAPTURE (SNAPSHOT MODE) TIMING

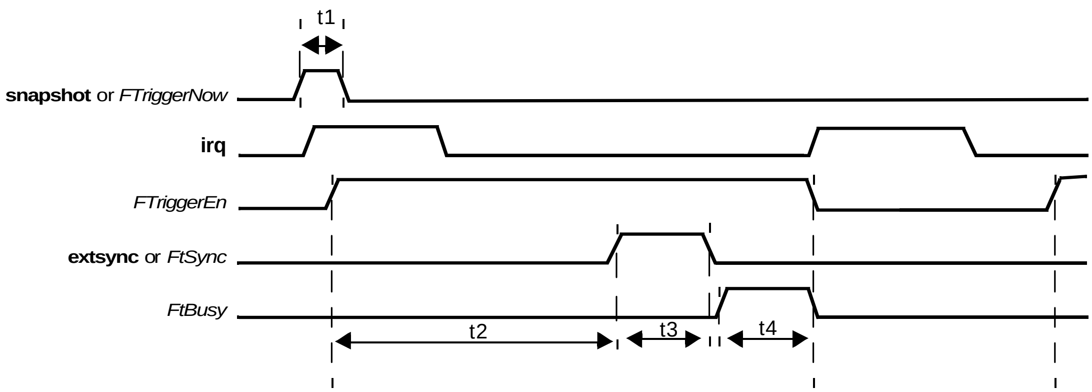


Figure 57. Snapshot Mode Timing With External Shutter

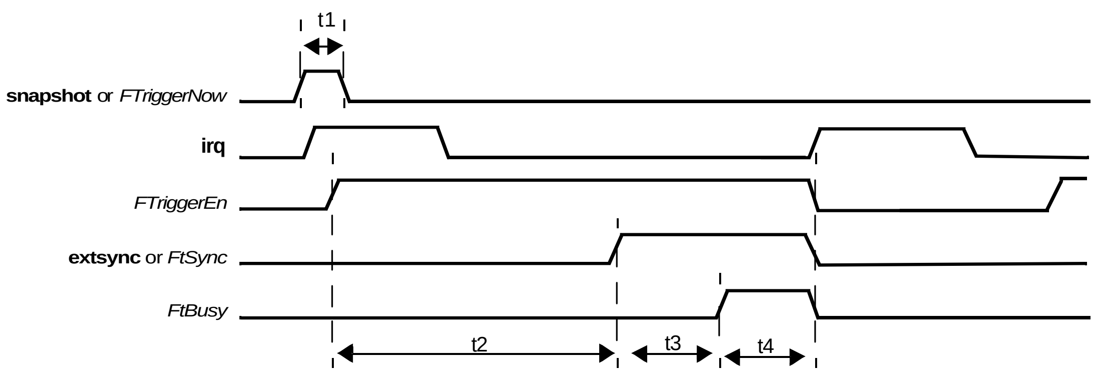


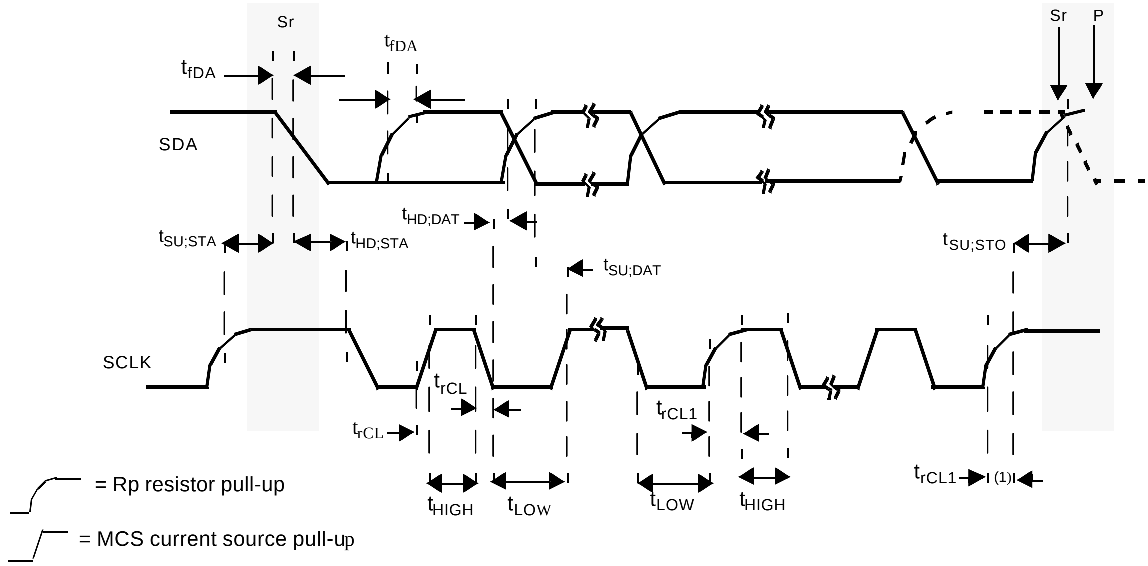
Figure 58. Snapshot Timing Without External Shutter

Label	Descriptions	Equation	
t1	Minimum Snapshot Trigger Pulse Width	2 * *mclk*	(see notes a & b)
t2	Minimum time from Snapshot Pulse to *extsync*	FN_{Hclk}	(see notes a & b)
t3	Array Integration Time	FN_{Hclk}	(see notes a & b)
t4	Pixel Read Out	FN_{Hclk}	(see notes a & b)

Note a: See 7.0 *Frame Rate Programming* section for more details
Note b: See *Snapshot Mode* for more details

Timing Information (continued)

4.0 SERIAL BUS TIMING



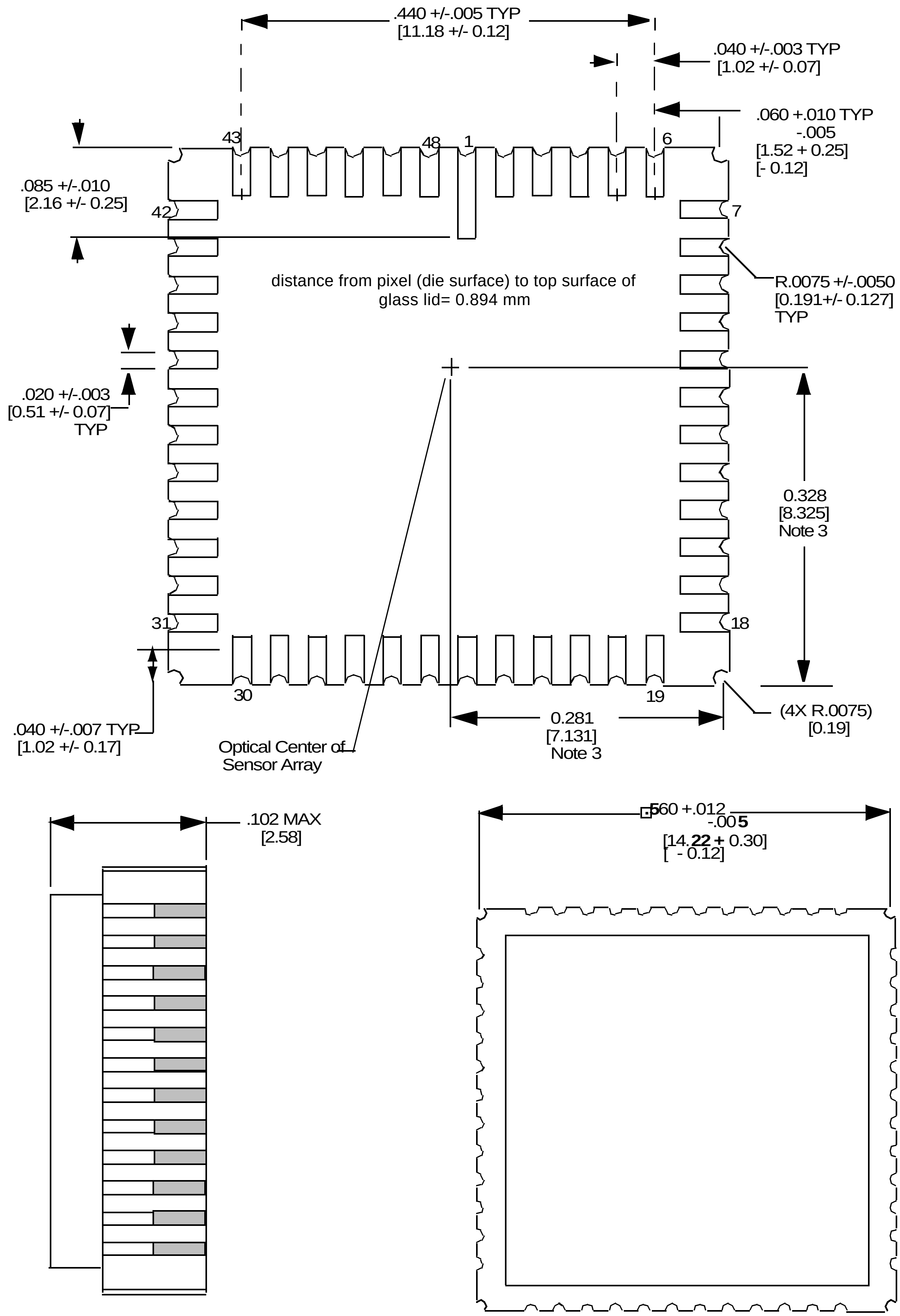
(1) Rising edge of the first SCLK pulse after an acknowledge bit.

Figure 59. I^2C Compatible Serial Bus Timing.

The following specifications apply for all supply pins = +3.3V, C_L = 10pF, and *sclk* = 400KHz unless otherwise noted. **Boldface limits apply for TA = T_{MIN} to T_{MAX}:** all other limits T_A = 25°C (Note 7)

PARAMETER	SYMBOL	MIN	MAX	UNIT
sclk clock frequency	f_{SCLH}	0	400	KHz
Set-up time (repeated) START condition	$t_{SU;STA}$	0.6	-	µS
Hold time (repeated) START condition	$t_{HD;STA}$	0.6	-	µS
LOW period of the *sclk* clock	t_{LOW}	1.3	-	µS
HIGH period of the *sclk* clock	t_{HIGH}	0.6	-	µS
Data set-up time	$t_{SU;DAT}$	180	-	nS
Data hold time	$t_{HD;DAT}$	0	0.9	µS
Set-up time for STOP condition	$t_{SU;STO}$	0.6		µS
Capacitive load for *sda* and *sclk* lines	C_b		400	pF

Array Mechanical Information



Notes:
1. Controlling dimensions are in inches, values in [] are in millimeters
2. All Exposed metallized areas shall be gold plated 60 micro-inches [1.52 micrometers] minimum thickness over nickel plate
3. Reference dimensions only. Tolerance will depend on die placement [+/-0.1 mm].
4. Reference JEDEC registration MS-009, variation AF issue A, dated 9/29/1980.

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