National Semiconductor

LM96570 PRODUCT BRIEF

PRELIMINARY
November 30, 2010

Ultrasound Configurable Transmit Beamformer

General Description

The LM96570 is an eight-channel monolithic beamformer for pulse generators in multi-channel medical ultrasound applications. It is well-suited for use with National's LM965XX series chipset which offers a complete medical ultrasound solution targeted towards low-power, portable systems.

The LM96570 offers eight P and N output channels with individual delays of up to 102.4 µs operating at pulse rates of up to 80 MHz. A pulse sequence is launched on all channels simultaneously through a single firing signal. Advanced features include delay resolution down to 0.78 ns and programmable patterns of up to 64 pulses. Pulse patterns and delay settings are pre-programmed through a serial interface, thereby simplifying the timing requirements on the driving circuitry.

The LM96570 is packaged in a 32-pin LLP.

Notice: This document is not a full datasheet. For more information regarding this product or to order samples please contact your local National Semiconductor sales office or visit http://www.national.com/support/dir.html

Applications

- Ultrasound Imaging

Features

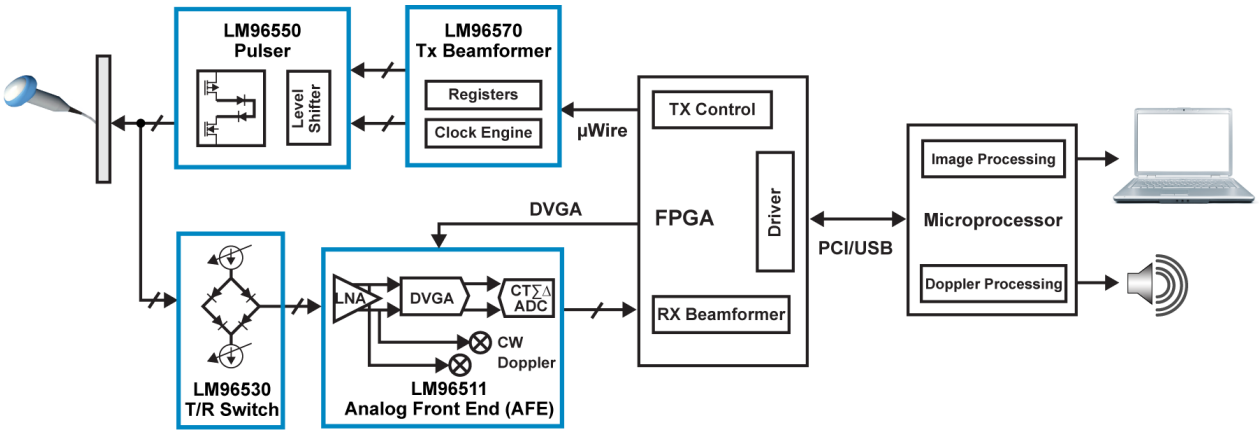
- Full control over selecting beam directions and pulse patterns by programming individual channel parameters
- Outputs interface seamlessly with positive and negative inputs on octal high-voltage pulser ICs
- Beamformer timing provides:
  - Delay resolution of 0.78 ns
  - Delay range of up to 102.4 µs
- Pulse patterns are locally generated with:
  - Sequences of up to 64 pulses
  - Adjustable Pulse widths
- 2.5V to 3.3V CMOS logic interface

Key Specifications

I/O voltage	2.5 to 3.3	V
Core supply voltage	1.8	V
Output pulse rate	80	MHz
Reference frequency	40 (±5%)	MHz
1σ Output Jitter (@ 5MHz)	25	ps
Output Phase Noise (@ 5MHz, 1kHz offset)	−116	dBc/Hz
Delay resolution	0.78	ns
Delay range	102.4	µs
Max. pattern length	64	pulses
Serial interface speed	80	Mbps
Total Power	0.063	Watts
Operating Temp.	0 to +70	°C

Typical Application

8-Channel Transmit/Receive Chipset



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Connection Diagram

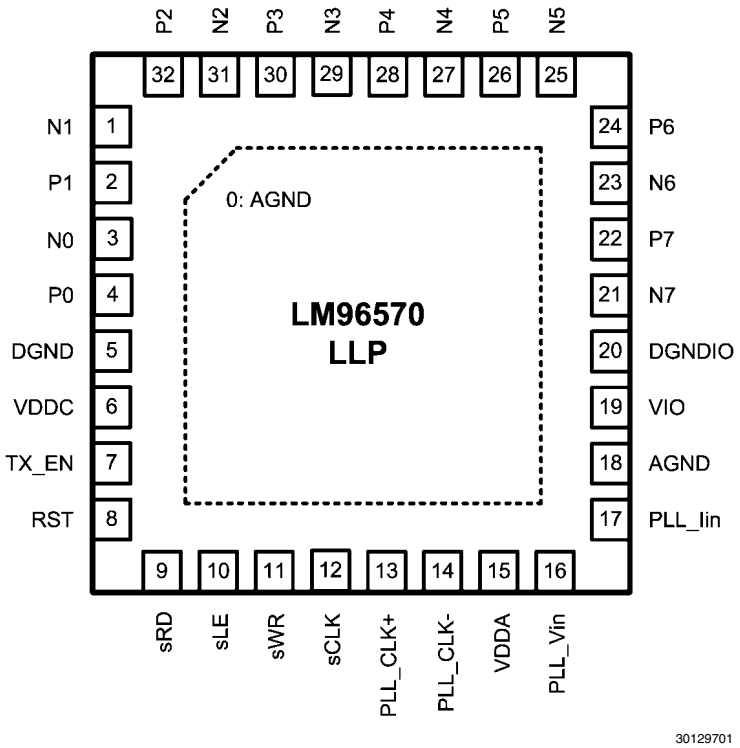


FIGURE 1. Pin Diagram of LM96570

Ordering Information

Part Number	Package	NSC Drawing	Quantity
LM96570SQ	32–Lead LLP	SQA32A	1000
LM96570SQE			250
LM96570SQX			4500

Pin Descriptions

Pin No.	Name	Type	Function and Connection
1 – 4, 21 – 32	P0-7, N0-7	Output	Control signals for pulser. P outputs control positive pulses and N outputs control negative pulses..
13	PLL_CLK+	Input	PLL Reference Clock PLUS Input, LVDS compatible or Single-Ended LV CMOS input, programmable through 4-Wire Serial Interface (Register 1Bh[0])
14	PLL_CLK-	Input	PLL Reference Clock MINUS input, LVDS compatible. For Single-Ended PLL Reference Clock operation, tie this pin to AGND or VDDA.
7	TX_EN	Input	1 = Beamformer starts firing 0 = Beamformer ceases firing
16	PLL_Vin	Input	Voltage range 0.8-1.2V for tuning internal PLL noise performance. Under normal conditions, 0.94V is recommended.
17	PLL_Iin	Input	100 µA current input
8	RST	Input	Asynchronous Chip Reset 1 = Reset 0 = No Reset
12	sCLK	Input	4-Wire Serial Interface Clock
10	sLE	Input	4-Wire Serial Interface Latch Enable
11	sWR	Input	4-Wire Serial Interface Data Input for writing data registers
9	sRD	Output	4-Wire Serial Interface Data Output for reading data registers
15	VDDA	Power	Analog supply voltage (1.8V)
6	VDDC	Power	Digital core supply voltage (1.8V)
19	VIO	Power	Digital I/O supply voltage (2.5 to 3.3V)
0, 18	AGND	Ground	PLL Analog ground
5	DGND	Ground	Digital core ground
20	DGNDIO	Ground	Digital I/O ground

Absolute Maximum Ratings (*Note 1*)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (*Note 4*)

Human Body Model	2kV
Machine Model	200V
Charge Device Model	750V
Maximum Junction Temperature (T_{JMAX})	+150°C
Storage Temperature Range	−40°C to +125°C
Supply Voltage (VDDA)	−0.3V to +2.0V
Supply Voltage (VDDC)	−0.3V and +2.0V
Supply Voltage (VIO)	−0.3V and +3.6V
Voltage at Analog Inputs	−0.3V and VDDA+0.3V
Voltage at Logic Inputs	−0.3V and VIO+0.3

Operating Ratings (*Note 1*)

Operating Temperature Range(T_A)	0°C to + 70°C
VDDA, Analog Supply	+1.71V to +1.89V
VDDC, Digital Core Supply	+1.71V to +1.89V
VIO, Digital IO Supply	+2.37 to +3.47
Package Thermal Resistance (θ_{JA}) (*Note 3*)	37°C/W

Analog Electrical Characteristics

Unless otherwise stated, the following conditions apply VIO = +3.3V, VDDA = VDDC = +1.8V, T_A = 25°C.

Pin	Parameter	Conditions	Min	Typ	Max	Units
	PLL Phase Noise	5MHz pulse rate, 1kHz offset		−116		dBc/Hz
VDDA	Power Supply Current	Register with No Pattern (08h - 19h)			18.5	mA
VDDC					2.4	
VIO					0.3	
VDDA	Power Supply Current	Register Default Pluse Pattern (08h - 19h), TX_EN = 15 kHz, Pulse rate = 5 MHz		16.0		mA
VDDC				6.50		
VIO				13.4		
PLL_CLK+	PLL Reference Clock Frequency		38	40	42	MHz

Beamformer Output Timing Characteristics

Unless otherwise stated, the following conditions apply VIO = +3.3V, VDDA = VDDC = +1.8V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Output Pulse Rate		0.625		80	MHz
	Output Delay Range			102.4		µs
	Output Delay Resolution			0.78		ns
	Output Pattern Length				64	Pulses
t_{OD}	Output Propagation Delay	Delay Profile (00–07h) = 0 Asynchronous TX_EN	32		47.5	ns
$t_{R/F}$	Output Rise/Fall	I_{LOAD} = 2mA		0.5	1.9	ns

Digital Electrical Characteristics

Unless otherwise stated, the following conditions apply VIO = +3.3V, VDDA = VDDC = +1.8V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PLL DIFFERENTIAL REFERENCE CLOCK DC SPECIFICATIONS						
V_{ID}	PLL Reference Clock Differential Input Amplitude	AC Coupled to pins 13 & 14. 1B[0] = 0 (see (*Note 2*))	200	400		mV
V_{ICM}	PLL Reference Clock Input Common Mode Voltage	Pins 13 & 14 bias voltage, VICM ≈ 0.5 X VDDA		0.9		V
R_{IN}	Single-ended Input Resistance			11		kΩ
PLL 1.8V LVCMOS SINGLE-ENDED REFERENCE CLOCK DC SPECIFICATIONS						
V_{IH}	LVCMOS Input “HI” Voltage	Pin 13. Register 1B[0] = 1	1.5			V
V_{IL}	LVCMOS Input “LO” Voltage	Pin 13. Register 1B[0] = 1			0.3	
R_{IN}	LVCMOS Input Resistance	Pin 13 = 0V or VIO		11		kΩ
3.3V I/O DC SPECIFICATIONS						
V_{IH}	Logic Input “HI” Voltage		2.2			V
V_{IL}	Logic Input “LO” Voltage				0.5	
$I_{IN-H/L}$	Input Current		–1		1	µA
V_{OH}	Logical Output “HI” Voltage	I_{OH} = 2 mA	2.9			V
V_{OL}	Logical Output “LO” Voltage	I_{OL} = 2 mA			0.34	
$I_{O-H/L}$	Logic Output Current			±10		mA

Serial Interface Timing Characteristics

Unless otherwise stated, the following conditions apply VIO = +3.3V, VDDA = VDDC = +1.8V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{LES}	sLE Setup Time		1.4			ns
t_{LEH}	sLE Hold Time		1.9			
t_{LEHI}	sLE HI Time		2.4			
t_{WS}	sWR Setup Time		1.4			
t_{WH}	sWR Hold Time		2.4			
t_{RS}	sRD Data Valid Setup Time			6.3		
t_{RH}	sRD Data Valid Hold Time			6.2		
t_{SCLKR}	sCLK Rise Time			1.7		ns
t_{SCLKF}	sCLK Fall Time			1.7		
t_{SCLKH}	sCLK High Time		2.4			ns
t_{SCLKL}	sCLK Low Time		3.4			
f_{SCLK}	sCLK Frequency				80	MHz

Note 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device can or should be operated at these limits.

Operating Ratings indicate conditions for which the device is guaranteed to be functional, but do not guarantee specific performance limits. Guaranteed specifications and test conditions are specified in the Electrical Characteristics section. Operation of the device beyond the Operating Ratings is not recommended as it may degrade the lifetime of the device.

Note 2: The combination of common mode and voltage swing on the clock input must ensure that the positive voltage peaks are not above VDDA and the negative voltage peaks are not below AGND.

Note 3: The maximum power dissipation is a function of T_{JMAX}, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{JMAX} - T_A)/ \theta_{JA}$. All numbers apply for package soldered directly into a 2 layer PC board with zero air flow.

Note 4: Human Body Model, applicable std. JESD22–A114–C. Machine Model, applicable std. JESD22–A115–A. Field induced Charge Device Model, applicable std. JESD22–C101–C.

Timing Diagrams

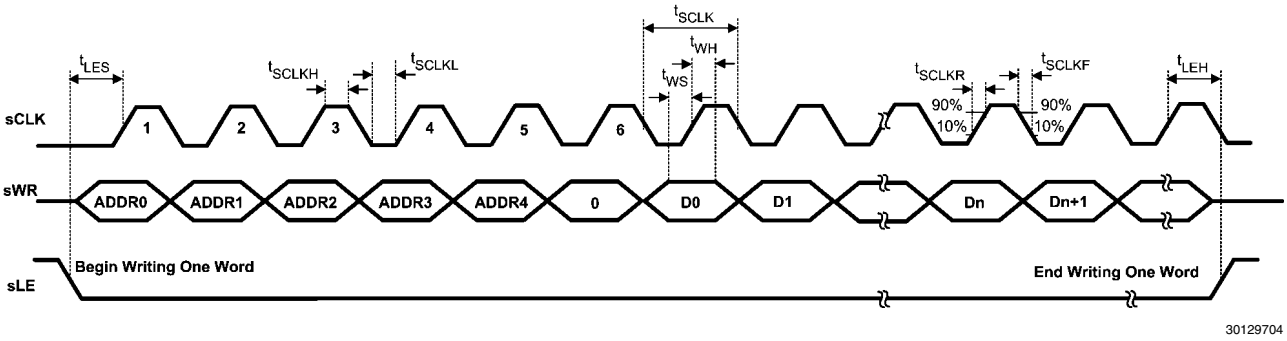


FIGURE 2. 4-Wire Serial Interface WRITE Timing

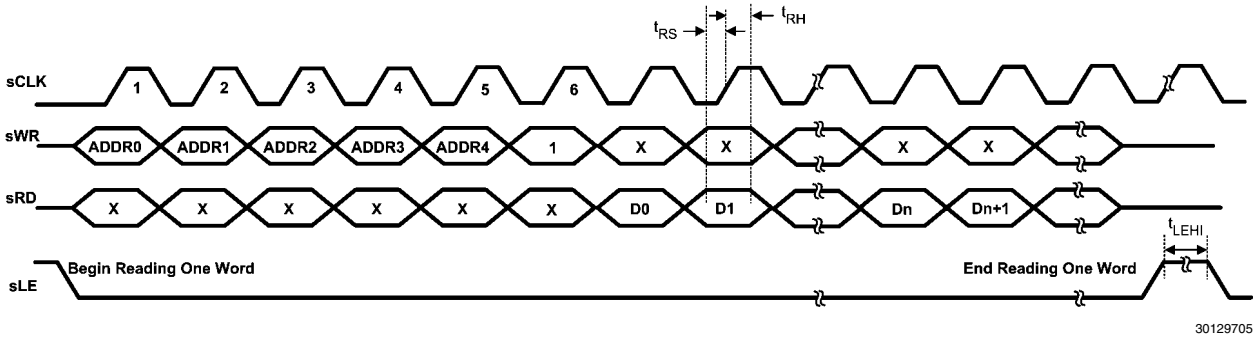
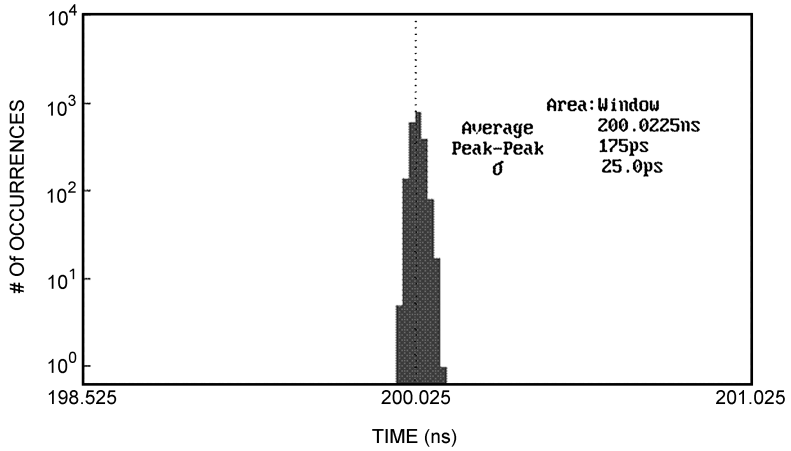


FIGURE 3. 4-Wire Serial Interface READ Timing

Typical Performance Characteristics

1δ Output Jitter



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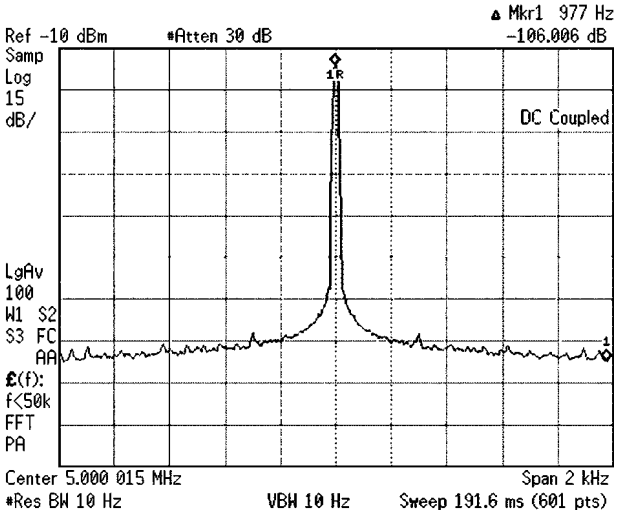
Output Phase Noise



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Overview

The LM96570 beamformer provides an 8-channel transmit side solution for medical ultrasound applications suitable for integration into multi-channel (128 / 256 channel) systems. Its flexible, integrated pulse pattern generation and delay architecture enables low-power designs suitable for ultra-portable applications. A complete system can be designed using National's companion LM9655x chipset.

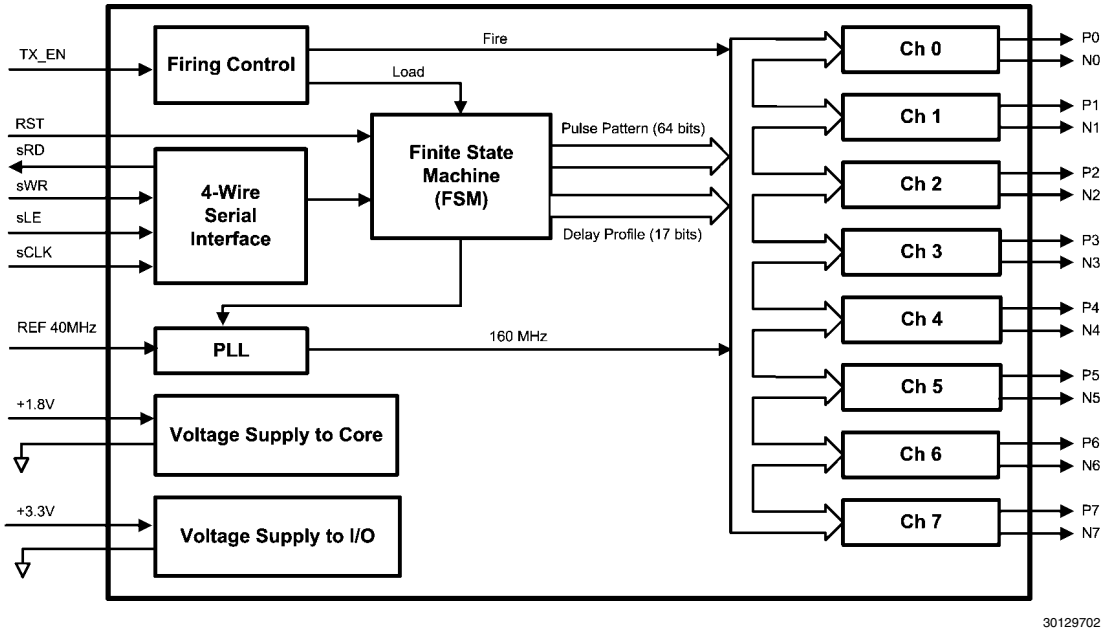


FIGURE 4. Block Diagram of Beamformer with Pattern and Delay Generator

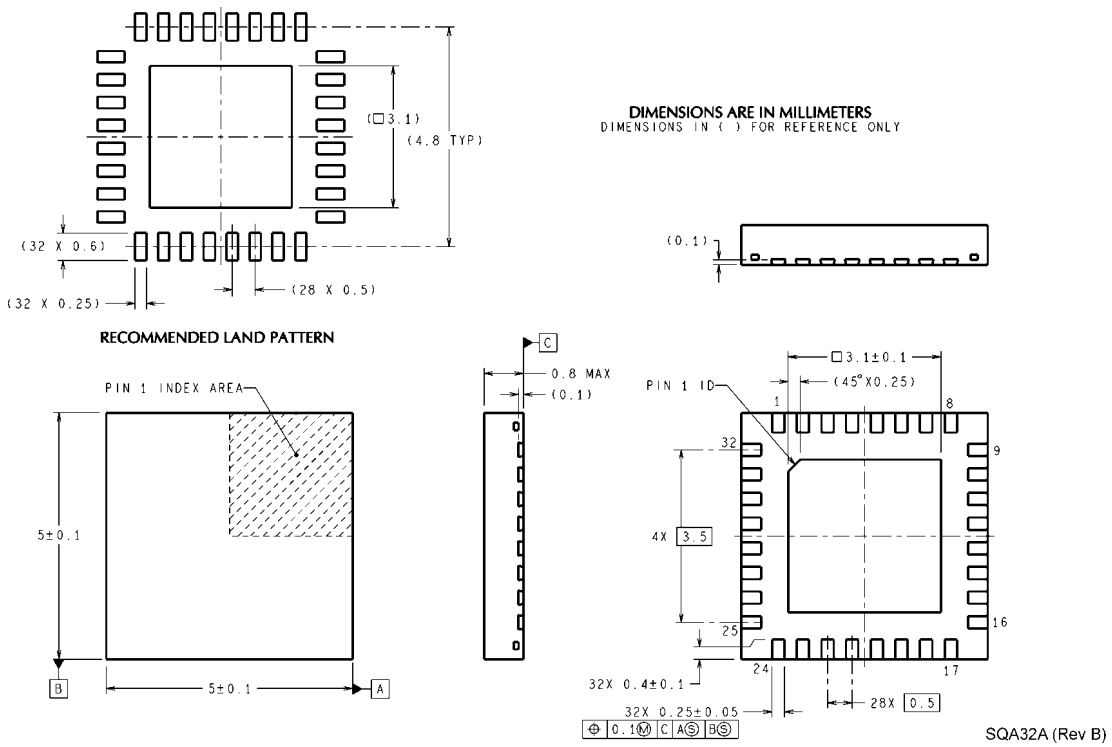
A functional block diagram of the IC is shown in *Figure 4*. Each of the 8 output channels are designed to drive the positive and negative pulse control inputs, Pn and Nn, respectively, of a high-voltage ultrasound pulser, such as the LM96550. Upon assertion of the common firing signal, each channel launches an individually programmable pulse pattern with a maximum delay of 102.4µs in adjustable in increments of 0.78 ns. The length of a fired pulse pattern can extend up to 64 pulses. Accurate timing of the pulse generation is enabled by an on-chip PLL generating 8-phase 160 MHz internal clocks derived from an external differential or single-ended 40MHz reference.

The pulse patterns and delay settings can be programmed into and read out from the individual channel controls via a four-wire serial interface. When the Latch Enable signal (sLE) is low, the targeted on-chip registers can be written though the serial data Write pin (sWR) at the positive clock edge (sCLK). In the same way, they can also be read out through the serial data Read pin (sRD). The writing and reading operations have the same timing requirements, which are shown in *Figure 2* and *Figure 3*. The serial data stream starts with a 6-bit address, in which the first 5-bits identify the mode of updating which is interpreted by the Finite State Machine (FSM), and the sixth bit of the address indicates the 4-wire serial operation, either "WRITE" (0) or "READ" (1). The address is followed by the data word, whose length can vary from 8 bits to 64 bits. The data stream starts with the LSB and ends with the MSB. The first 5-bit address indicates which of the 27 registers is being accessed. In each 4-wire serial operation, only one register can be written to or read from at a time. TX_EN must be inactive during 4-wire serial interface operation.

Upon a rising edge of the transmit signal "TX_EN", the internal "Fire" signal is pulled high after an internal propagation delay relative to TX_EN elapses. Then the delay counter of each channel begins counting according to the programmable delay profile. When the counter reaches the 17-bit programmed delay value, the programmed pulse pattern is sent out continuously at the programmed frequency until it reaches the length of the pulse pattern.

The interface is compatible with CMOS logic powered at 2.5V or 3.3V. The internal core supply is derived from 1.8V referenced to 0V.

Physical Dimensions inches (millimeters) unless otherwise noted



32-Lead LLP Package
NS Package Number SQA32A

Notes

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